The Invariance of the Noise Impedance in n-MOSFETs across Technology Nodes and its Application to the Algorithmic Design of Tuned Low Noise Amplifiers

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***Abstract*— The measured noise impedance of MOSFETs is found to be invariant across technology nodes. Together with the invariance of the optimum noise figure current density, $J_{\rm OPT}$, this allows for optimally noise matched LNAs to be ported without redesign between technology nodes and for a given design to be scaled in frequency. The design porting and frequency scaling are validated experimentally on record low noise LNAs fabricated in 90 nm and 130 nm CMOS technology.**

***Index Terms*— Noise parameters, optimum source impedance, algorithmic design, tuned low-noise amplifiers, design scaling and porting.**

I. Introduction

We have shown recently that the peak $f_{\rm T}$, peak $f_{\rm MAX}$ and the optimum $NF_{\rm MIN}$ current densities of n-MOSFETs, which are approximately 0.3 mA/μm, 0.2 mA/μm and 0.15 mA/μm, respectively, are largely invariant between foundries, technology nodes and circuit topologies [1]. This suggests that all low noise amplifiers (LNAs) should be biased at the optimum $NF_{\rm MIN}$ current density ($J_{\rm OPT}$), which is also independent of frequency (Fig. 1). In this paper, we explore for the first time the frequency behaviour and the scaling of the noise parameters of n-MOSFETs between technology nodes as the critical missing step in the development of an algorithmic CMOS LNA design scaling and porting methodology, as predicted theoretically in [2]. In the second part, we validate this methodology on 14, 28 and 60 GHz LNAs fabricated in 130 nm and 90 nm CMOS technologies.

II. Invariance of Optimum Source Impedance

To investigate the frequency behaviour of n-MOSFET noise parameters, transistor test structures were fabricated in STMicroelectronics' 130 nm and 90 nm bulk CMOS processes. Their noise parameters were measured between 10 and 26 GHz with a Focus Microwaves tuner system. The parasitics of the pad were de-embedded from measured noise parameter data with the matrix technique described in [3]. The real and imaginary parts of the optimum noise impedance ($Z_{\rm SOPT}$) of 130 nm and 90 nm transistors with identical gate finger width are plotted in Fig. 2 and 3, showing that they remain largely invariant across technology nodes. Note that $Z_{\rm SOPT}$ follows a $1/f$ characteristic that allows the centre frequency of an LNA to be scaled. The frequency scaling will eventually break down at millimetre-wave frequencies where the contribution of the source and gate resistance, R_S (approximately 200 $\Omega\,\mu$m) and R_G (about 200 Ω for a 90 nm finger with $W_f = 1\mu$m and contacted on one side only), respectively, becomes a large part of $\Re\{Z_{\rm SOPT}\}$.

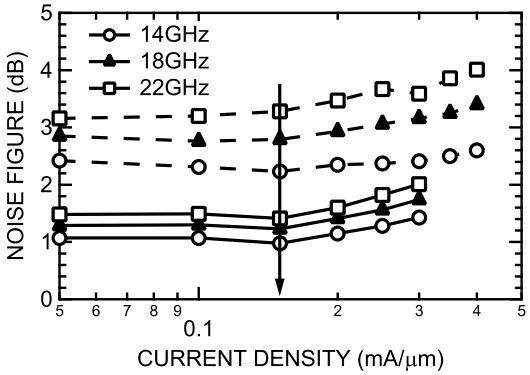

Fig. 1. Measured $NF_{\rm MIN}(I_{DS}/W)$ characteristics of the 90nm (solid line) and the 130nm (dashed line) n-MOSFETs with 80 gate fingers, each 1μm wide.

III. Tuned LNA Algorithmic Design and Porting

A. Design Methodology

An algorithmic methodology for simultaneously noise and input impedance matched bipolar and MOSFET LNAs was proposed in [4], [5]. It has been widely applied in the design of HBT-based LNAs, but has only recently been used to design MOSFET LNAs and only at millimetre-wave frequencies [2], [6]. Alternative design methodologies include the power constrained noise optimization technique [7], which ignores noise matching, and the power-constrained simultaneously noise and input matching tech-

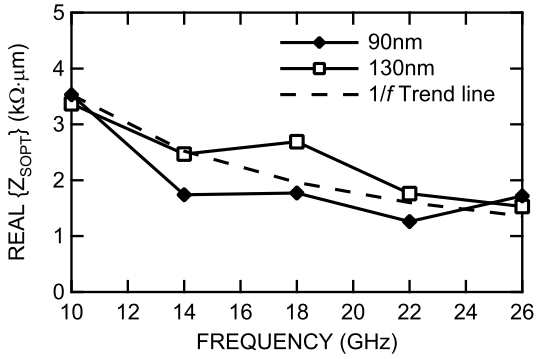

Fig. 2. Measured $\Re\{Z_{\rm SOPT}\}$ of the 130 nm and 90 nm transistors. The devices are $80 \times 90\,\text{nm} \times 1\,\mu\text{m}$ and $80 \times 130\,\text{nm} \times 1\,\mu\text{m}$.

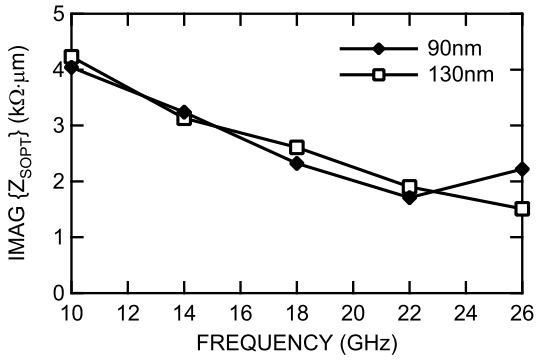

Fig. 3. Measured $\Im\{Z_{\rm SOPT}\}$ of the 130 nm and 90 nm devices in Fig. 2.

nique [8]. The latter method introduces an extra capacitance in parallel with the $C_{\rm GS}$ of the common-source transistor to provide an extra degree of freedom for power optimization. However, as pointed out in [9], the main drawbacks are a reduction in the gain and an increase in the R_n of the LNA.

Based on the demonstrated invariance of $J_{\rm OPT}$ and $Z_{\rm SOPT}$, an algorithmic design methodology for a cascode CMOS LNA (Fig. 4) at a given centre frequency f_0 can be devised as follows.

1) Choose an optimal finger width W_f that minimizes $NF_{\rm MIN}$, striking a balance between gate resistance and capacitive parasitics (*c.f.* [1]).
2) With the bias current density held constant at $J_{\rm OPT}$ and W_f unchanged, determine N_f such that $\Re\{Z_{\rm SOPT}\}$ equals the signal source resistance, $\Re\{Z_0\}$, typically 50Ω.
3) Add source inductance
$$L_S = \frac{\Re\{Z_0\}}{2\pi f_{\rm T}}, \tag{1}$$
where $f_{\rm T}$ is that of the cascode biased at $J_{\rm OPT}$. This step does not affect $\Re\{Z_{\rm SOPT}\}$, because it is invariant to lossless impedance transformations and lossless feedback.

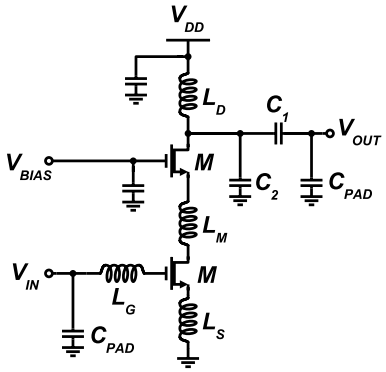

Fig. 4. Single-stage cascode LNA schematic.

4) Add gate inductance
$$L_G = \frac{1}{\omega^2 C_{\rm IN}} - L_S, \tag{2}$$
where $C_{\rm IN}$ is the input capacitance and ω is the angular frequency of the LNA, to simultaneously tune out the imaginary parts of $Z_{\rm IN}$ and $Z_{\rm SOPT}$.
5) Add drain inductance L_D and output matching network C_1 and C_2.

This optimized LNA design can be scaled to another frequency $f = \alpha f_0$, where α is the scaling factor, simply by dividing N_f, L_G, L_D, C_1 and C_2 by α, while L_S and $J_{\rm OPT}$ remain constant.

Unlike HBT LNAs, a CMOS LNA can also be ported to another technology node with little redesign effort. Since $Z_{\rm SOPT}$ and $J_{\rm OPT}$ are invariant between nodes (Figs. 1-3), the transistor gate width W, bias current, and output matching network remain unchanged. $L_S + L_G$ is invariant because it tunes out $\Im(Z_{\rm IN})$, which is itself constant across technology nodes. The only changes involve L_S (and W_f) which scales with $1/f_{\rm T}$ and, to a smaller extent, L_G.

B. Experimental Results

For verification, five single-stage casocode LNAs were designed and scaled according to the above methodology in 130 nm and 90 nm CMOS technologies. The LNA component values are compiled in Table I. As mentioned, at a given frequency, the 90 nm and 130 nm LNAs have identical transistor size and bias current. However, because no parasitic extractor was available at the time of the 130 nm tapeout, the input capacitance was underestimated and hence the gate inductor L_G was overestimated by about 20% in the two 130 nm LNAs. The output matching network was also slightly modified from that in the 90 nm designs to compensate for the larger (60 fF vs. 20 fF) pad capacitance.

The measured S and noise parameters of these LNAs are shown in Figs. 5-9. The validity of the algorithmic

TABLE I
SINGLE-STAGE CASCODE LNA COMPONENT VALUES.

LNA	N_f	W_f (μm)	I_{DS} (mA)	V_{DD} (V)	L_S (pH)	L_G (pH)	L_D (pH)	L_M (pH)	C_1 (fF)	C_2 (fF)	C_{PAD} (fF)
14 GHz, 90 nm	90	1	13.5	1.5	128	1100	545	0	145	70	20
28 GHz, 90 nm	45	1	6.75	1.5	128	535	235	0	75	59	20
60 GHz, 90 nm	20	1	3	1.5	55	190	140	190	30	0	20
12 GHz, 130 nm	90	1	13.5	1.8	177	1340	492	0	122	135	60
24 GHz, 130 nm	45	1	6.75	1.8	177	718	251	0	80	58	60

LNA design methodology is confirmed by the fact that s_{11} and $\Gamma_{\rm OPT}$ are simultaneously better than -20 dB at the designed frequencies. The 90 nm CMOS LNAs, which have all matching inductors on die, exhibit record 50-Ω noise figures of 2.1 dB at 14 GHz and 2.5 dB at 26 GHz. The resonant frequency of the 130 nm LNAs is shifted down by as much as 20% due to the three times larger pad capacitance, 20% larger L_G, and due to the capacitive parasitics of the interconnect that were not accounted for in the design process. Even so, as the normalized results in Figs. 10 and 11 indicate, the scaling of the 130 nm CMOS LNAs in frequency from 12 GHz to 24 GHz has better than 96% accuracy, while the frequency scaling of the 90nm CMOS LNAs from 14 GHz to 28 GHz and even to 60 GHz, exhibits less than 8% error. This frequency scaling error, lower than the typical process spread of a given CMOS technology, is remarkable because no redesign was involved, just component size scaling to follow exactly the ratio of the LNA centre frequencies.

Fig. 12 indicates that RF designs are as easy to scale as conventional CMOS logic and that performance improves with each new technology node. The fact that s_{11} and $\Gamma_{\rm OPT}$ simultaneously resonate provides irrefutable evidence, for the first time at the circuit level, that in MOSFETs, $\Im\{Z_{\rm SOPT}\}$ and $-\Im\{Z_{\rm IN}\}$ are almost identical. Indirectly, this also confirms that the correlation between the drain noise current and the gate induced noise current of a MOSFET is negligible [10]. Finally, Fig. 13 indicates that lossless feedback does not change R_n and that the drain noise current coefficient P is smaller than 1.

IV. CONCLUSION

It has been experimentally demonstrated that the optimum source impedance ($Z_{\rm SOPT}$) of an n-MOSFETs is invariant between the 130 nm and 90 nm CMOS technology nodes and follows a $1/f$ characteristics. From this observation, an algorithmic design methodology for simultaneously noise and input impedance matched tuned CMOS cascode LNAs is developed and validated experimentally. An optimized LNA can be scaled to another frequency and ported to a more advanced technology node to benefit from the improved gain and noise figure with minimal redesign effort. The fact that the imaginary parts of $Z_{\rm SOPT}$ and $Z_{\rm IN}$ can be simultaneously tuned out indicate that the statistical correlation between the drain and gate noise currents is negligible below 26 GHz in 130 nm and 90 nm n-MOSFETs.

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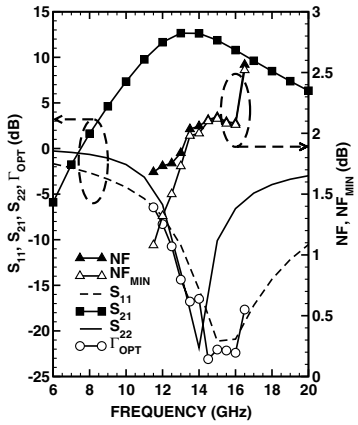

Fig. 5. Measured S and noise parameters at J_{OPT} of the 14 GHz LNA in 90nm CMOS.

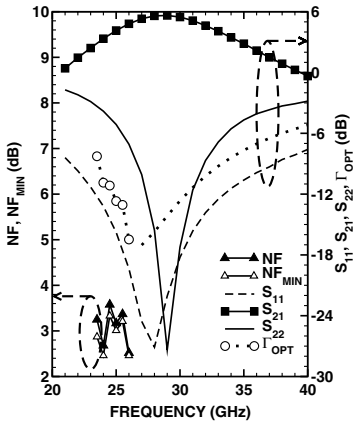

Fig. 6. Measured S and noise parameters at J_{OPT} of the 28 GHz LNA in 90nm CMOS.

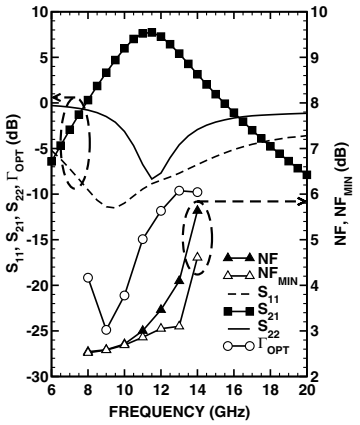

Fig. 7. Measured S and noise parameters at J_{OPT} of the 12 GHz CMOS LNA in 130nm CMOS.

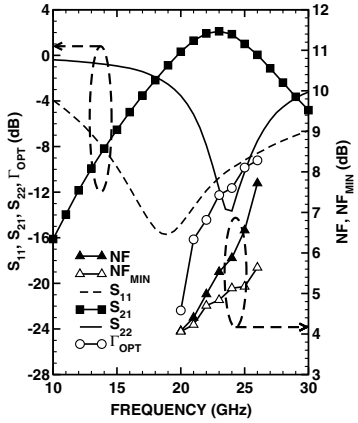

Fig. 8. Measured S and noise parameters at J_{OPT} of the 24 GHz CMOS LNA in 130nm CMOS.

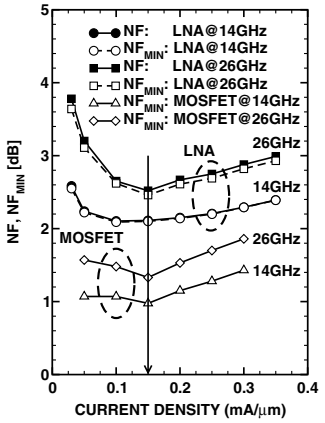

Fig. 9. Measured $NF_{\mathrm{MIN}}\,(I_{DS}/W)$ characteristics for 90 nm MOSFET and LNAs.

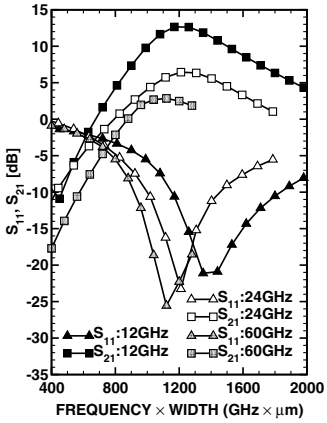

Fig. 10. Measured s_{11} and s_{21} of different LNAs fabricated in the 90 nm node vs. frequency-gate width product.

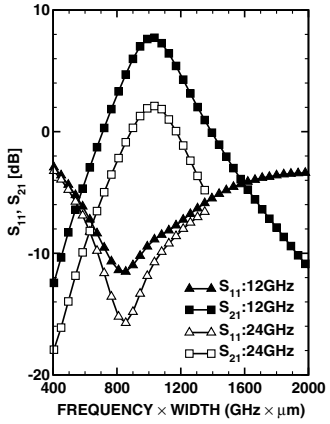

Fig. 11. Measured s_{11} and s_{21} of different LNAs fabricated in the 130 nm node vs. frequency-gate width product.

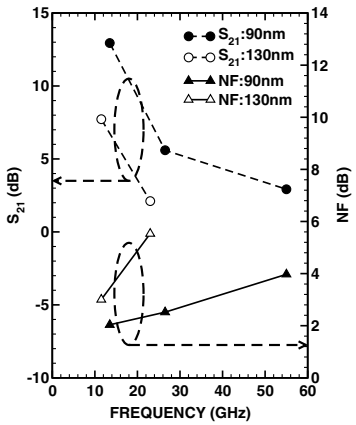

Fig. 12. Impact of technology scaling on the s_{21} and noise figure of LNAs.

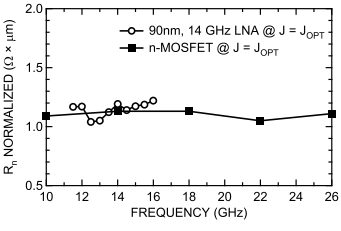

Fig. 13. Measured R_n normalized to total gate width vs. frequency at J_{OPT} for 90 nm MOSFET and LNA.