System-on-Chip Design Beyond 50 GHz

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Abstract

Candidate topologies and design methodologies for millimeter-wave IC building blocks such as LNAs, mixers, VCOs, and power amplifiers are discussed and recent experimental results obtained in SiGe BiCMOS and 90-nm RF CMOS technologies using inductors and transformers above 50 GHz are presented.

1. Introduction

During the past 4 years we have witnessed a tremendous improvement in silicon-based transistor performance to the point where the cutoff f_T and oscillation f_{MAX} frequencies of production 90-nm CMOS transistors, both above 150 GHz, have leaped ahead of those of production III-V technologies and are on par with those of the most advanced SiGe HBTs. RFICs and fiberoptic transceivers, the main high-speed technology drivers in the 1990's, have practically stalled for the past ten years at 2-5 GHz and 10 Gb/s, respectively. Perhaps ironically, the clock signal of microprocessors has surpassed by more than a factor of two the highest "radio frequencies" in cell phones and is fast approaching that of OC192 systems.

This disconcerting outlook for high-speed and RFIC research can be brightened up by taking on new applications beyond 50 GHz. The latter have yet to benefit from the large scale integration capability and digital signal processing power of CMOS and SiGe BiCMOS technologies.

Rather than trying to "mimic" GaAs and InP MMIC techniques which rely on large area transmission lines, hybrid couplers, and distributed topologies, this paper proposes to extend trusted analog and RFIC CMOS and SiGe BiCMOS design styles and topologies to millimeter wave (mm-wave) frequencies, and to apply them in emerging, and potentially large volume, applications in the 60-GHz to 100-GHz range. The latter include, but are not limited to, wireless gigabit Ethernet, automotive radar, and mm-wave imagers.

2. Optimal biasing and sizing of active devices

Transistors present three characteristic current densities (defined per unit gate width or unit emitter length) that are relevant for optimal design of circuits at mm-wave frequencies: the peak f_T, the peak f_{MAX}, and the minimum noise figure current densities, denoted as J_{pfT}, J_{pfMAX}, and J_{opt}, respectively. In SiGe HBTs, J_{pfT} and J_{pfMAX} are identical, about 1.2 mA/μm for the 160-GHz generation (Fig. 1), and may vary slightly from foundry to foundry. J_{opt} increases with frequency and is typically several times lower than $J_{pfMAX,}$ about 0.3 mA/μm at mm-wave frequencies. As a result, when biasing SiGe HBTs for lowest noise the power gain is compromised, albeit not as much as at 5 to 10 GHz.

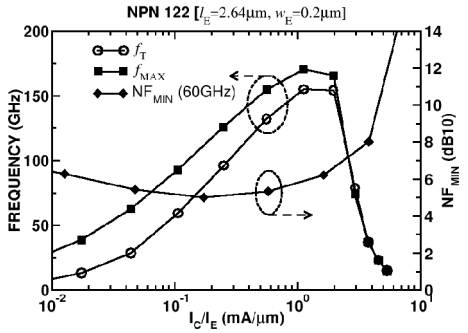

Figure 1. Measured f_T, f_{MAX} and NF_{MIN} at 60 GHz as functions of current density in SiGe HBTs.

In n-MOSFETs, as a result of constant-field scaling rules being applied rigorously by most foundries, the characteristic current densities are approximately 0.3 mA/μm, 0.2 mA/μm, and 0.15 mA/μm, respectively, irrespective of foundry and technology node. Furthermore, because J_{opt} is frequency-independent and close to $J_{pfMAX,}$, optimal noise bias and maximum gain bias almost coincide. Based on these observations, very simple rules can be derived for the optimal design of silicon mm-wave circuits: (i) minimize the number of transistors in order to improve circuit bandwidth, minimize noise, and maximize

linearity, (ii) inductors and transformers, rather than t-lines, should be employed for impedance matching to minimize die area, (iii) in LNAs, receive mixers and VCOs, transistors must be biased at J_{opt}, and (iv) in power amplifiers and upconverters, transistors must be biased at the peak f_{MAX}/f_T current density. In MOSFET circuits, (iii) and (iv) above result in identical size and bias current, irrespective of technology node. The latter simplifies porting of designs between technology nodes, making it a rather effortless exercise.

3. Millimetre-wave passives

Inductors, transformers [1,2], and MIM capacitors can simply be scaled down in size to minimize their footprint above the lossy silicon substrate and, by doing so, improve their quality factor and self-resonant frequency. Q's between 10 and 20 can be easily achieved in the 50-GHz to 100-GHz range with conventional CMOS copper metallization even as metal stripe width is reduced below 2 µm. Furthermore, by vertically-stacking inductors and transformer coils, the inductance per unit area is increased while reducing the footprint to less than 20µm per side [1].

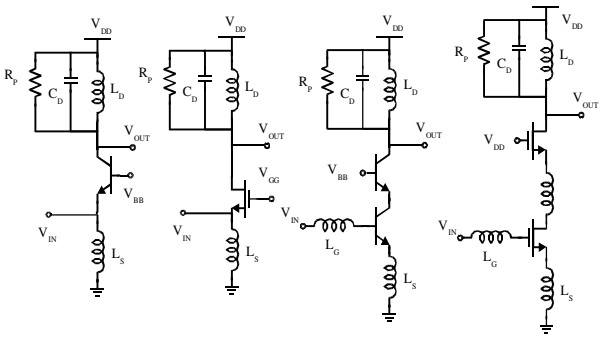

Figure 2. Mm-wave LNA topologies

4. IC building blocks

Common-base (CB) [3], MOSFET cascodes [4], bipolar cascodes [5], and common-gate (CG) [6] topologies, illustrated in Fig. 2, have been considered for LNAs operating above 50 GHz. In all cases, the transistor size and bias current that result in optimal noise impedance matching to 50 Ω is significantly smaller, in the 1-to-5 mA range, than at 10 GHz. This may look good from the power dissipation point of view but, in conjunction with the lower breakdown voltages typical of transistors suitable for the mm-wave region, it results in poor linearity [2,5] and ultimately reduced system dynamic range. Linearity is particularly bad in CB and CG stages. To satisfy input impedance matching conditions, the bias current is set to 3 mA or less limiting the linear input range to less than 150 mV_{pp}. The difficulty of simultaneously matching the input and noise impedance of CB/CG stages adds to their list of problems.

Just as at 2-5 GHz, the CS/CE and cascode stages can be simultaneously noise and input impedance matched at mm-wave frequencies [5]. Furthermore, their linearity is much better than that of CB/CG stages and can be improved simply by increasing the transistor size and current, without affecting the input impedance match and with negligible impact on noise matching. As the measured data in Fig. 3 indicate, the MOSFET cascode has relatively low f_T. In compensation, an inductor may be placed between the two transistors to tune out the middle pole (Fig. 2). Nevertheless, for applications above 50 GHz, a CS stage should be preferred to a MOSFET cascode stage in both LNAs and power amplifiers.

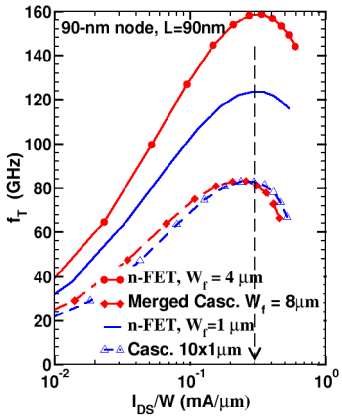

Figure 3. Measured f_T as a function of drain current density for 90-nm MOSFETs and cascodes.

The bipolar cascode continues to be the preferred LNA topology because it combines the excellent isolation of the CB/CG stage with the high power gain, good linearity and ease of simultaneous noise and input impedance matching, typical of the CE/CS stage. Furthermore, the high g_m/I_C ratio and small noise resistance make this stage, unlike a MOSFET one, insensitive to impedance mismatch and model inaccuracy. Fig. 4 shows the schematics of a 2-stage SiGe-HBT LNA whose design was scaled from 6 GHz. Unlike other LNAs reported in this frequency range [3,4,6] it uses inductors, regular 60µmx60µm pads, and it includes all bias circuitry in a 300µmx400µm die [5]. It was fabricated in a production 0.18-µm SiGe BiCMOS process by Jazz Semiconductor. More recently, we have scaled the same design to 65 GHz and 77 GHz. Its layout is shown in Fig.5, side by side with that of a 90-nm RF-CMOS, single-stage cascode LNA fabricated at TSMC. The CMOS LNA uses the same inductors as the SiGe LNA and, not surprisingly, its gain peaks at the same frequency as that of the SiGe LNA (Figs. 6

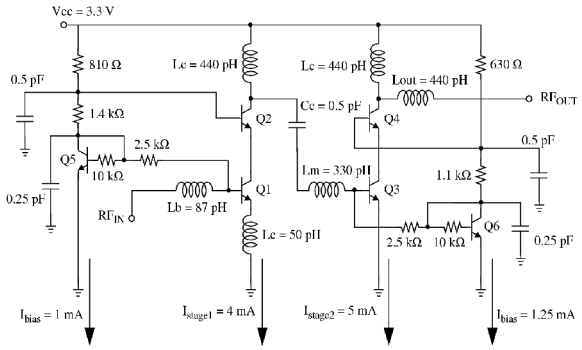

Figure 4. 52-GHz SiGe HBT LNA schematics.

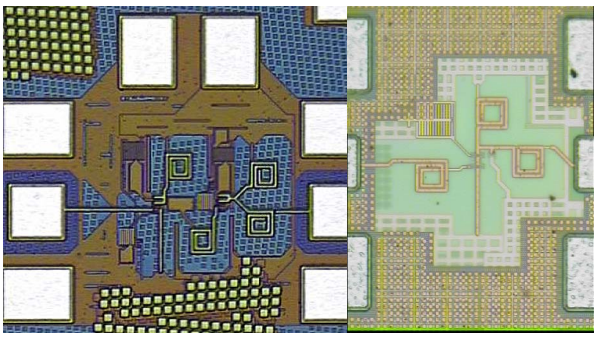

Figure 5. a) SiGe HBT 2-stage and b) 90-nm CMOS 1-stage cascode LNAs.

and 7). This result points to the importance of accurate passive component models. The 2.5-dB gain of the CMOS LNA (Fig. 7), much smaller than the 20-dB gain of the HBT LNA (Fig. 6), can be explained by the fact that only a 5-mA cascode stage is used to drive the 50-Ω load directly. Simulations indicate that, with a two-stage 90-nm CMOS cascode design now in fab, over 15 dB of gain is achievable at 65 GHz.

As illustrated in Fig. 8, the input compression point of the SiGe-HBT LNA, measured at 50 GHz, is -14 dBm, 8 dB higher than those of the CB [3] and CG [6] LNAs, and slightly better than that of the CMOS cascode LNA in [4]. The latter consumes 3 times larger current and dissipates twice the power.

The larger breakdown voltage of SiGe HBTs gives them a significant advantage in power amplifiers and low-noise oscillators. Since voltage swings of 3 V_{pp} are safe in CB stages while only 1.2 V_{pp} can be reliably accommodated in 90-nm MOSFETs, the phase noise and output power levels reported for SiGe-HBT VCOs [2] are typically 10 dB better than those of 60-GHz VCOs fabricated in advanced 90-nm SOI CMOS [7].

Fig. 9 shows the schematics, layout and tuning characteristics of a push-push SiGe-HBT VCO [2] operating between 64 and 78 GHz. The 21% tuning range is accomplished using inductors and accumulation-mode varactor diodes, and is typically

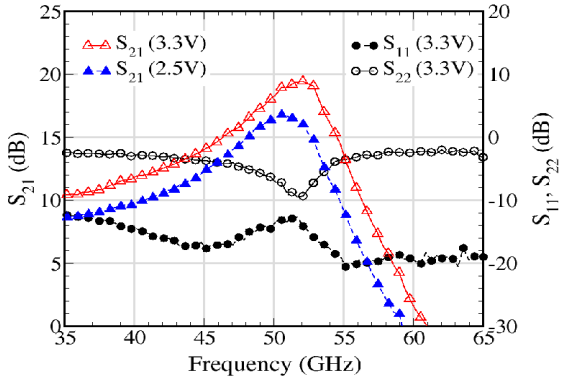

Figure 6. Measured S parameters of SiGe-HBT LNA.

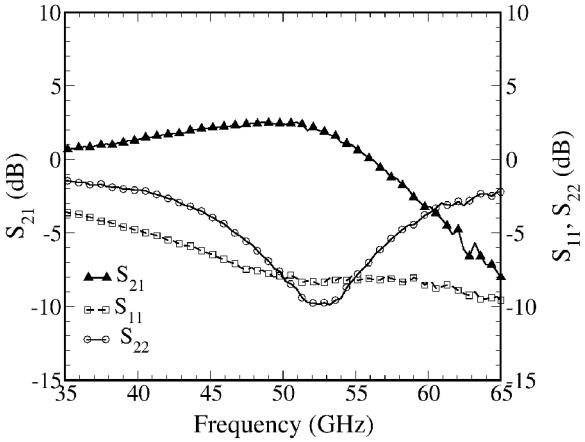

Figure 7. Measured S parameters of 90-nm CMOS LNA.

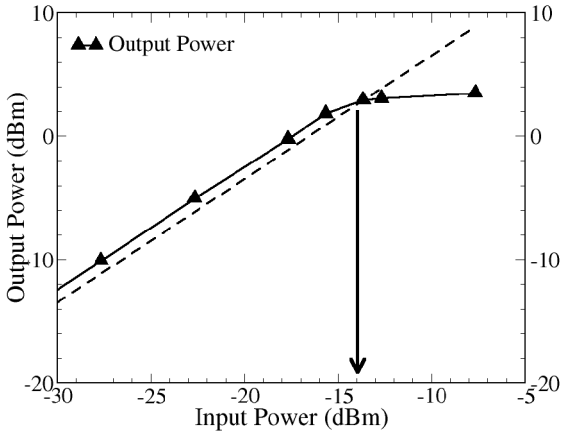

Figure 8. Input and output compression points of SiGe-HBT LNA measured at 50 GHz.

needed to cover the 5-GHz bandwidth of a 60-GHz radio, as well as process and temperature variations. Finally, Fig. 10 reproduces the schematics and

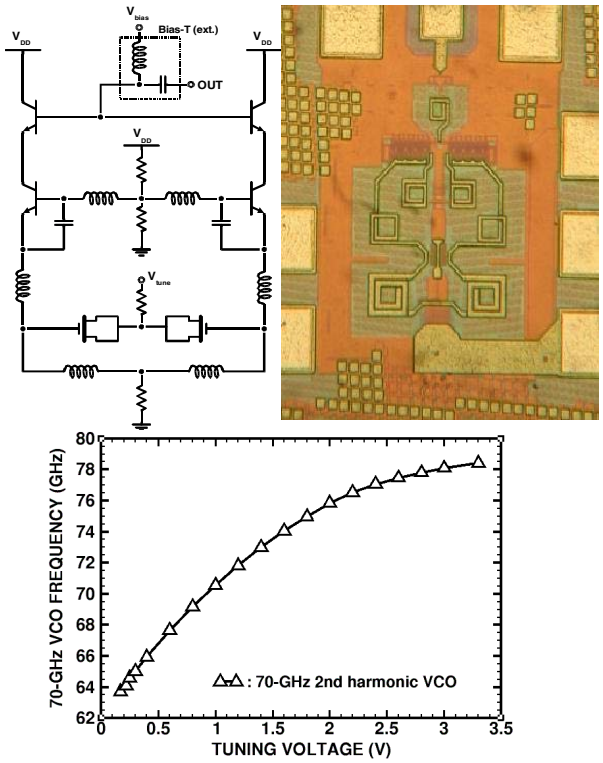

Figure 9. Schematics, layout and tuning characteristics of push-push SiGe-HBT VCO.

spectrum of a directly modulated BPSK transmitter operating at 65 GHz.

5. Conclusions

It was demonstrated that, by optimally sizing and biasing transistors, simplifying circuit topologies, and taking advantage of the reduced dimensions of inductors and transformers at mm-wave frequencies, it is possible to repeatably design and fabricate high performance mm-wave SiGe BiCMOS and 90-nm CMOS ICs with smaller die area and lower cost than corresponding wireless ICs in the 2-10 GHz range.

Acknowledgments

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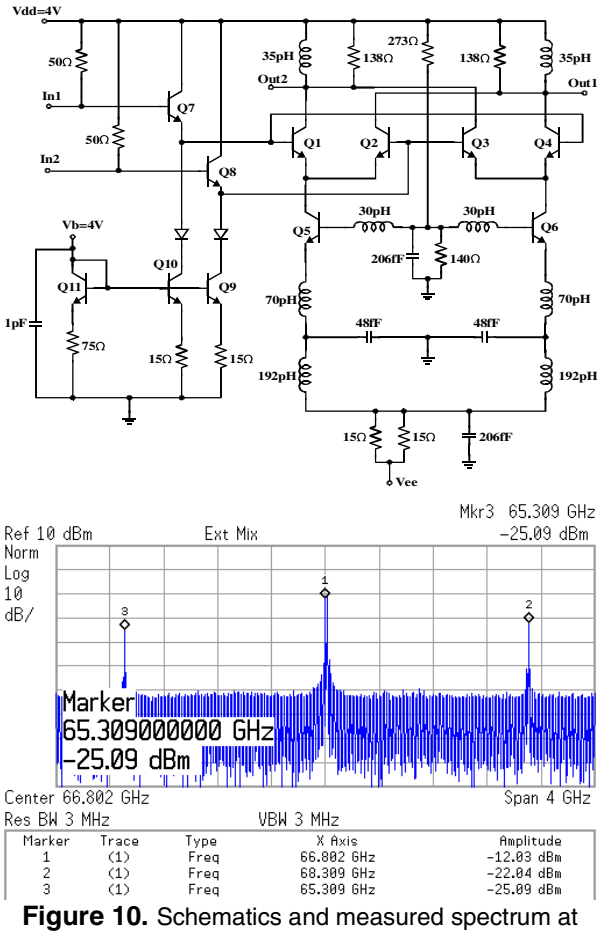

Figure 10. Schematics and measured spectrum at the output of 65-GHz BPSK transmitter for a 1.5 GHz data input.