System-on-Chip Design Beyond 50 GHz

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Outline

- Motivation
- Optimal sizing of active and passive devices at mm waves
- 60-GHz building block design methodologies
- 60-GHz SOC example
- Conclusions

Why mm-waves ?

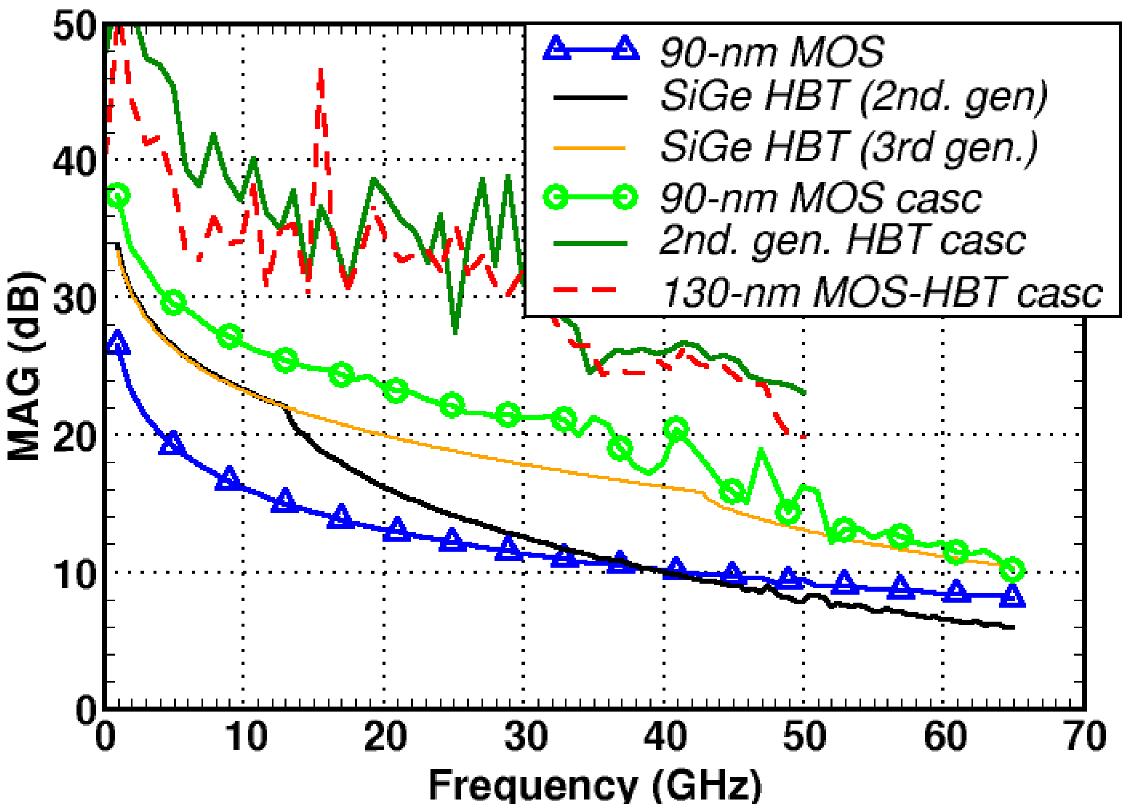
- Speed is free ... if you can afford CMOS mask costs!
- With TI's 2-GHz digital transceiver ... the days of RF are (almost) over
- Larger bandwidth => higher data rates, simpler radio architectures
- MOSFET scaling improves f_T, f_{MAX}, NF_{MIN}, g_m/I, R_n while V_{DD} saturates
- Smaller passives with higher Q (except varactors), on-chip antenna feasible for some applications

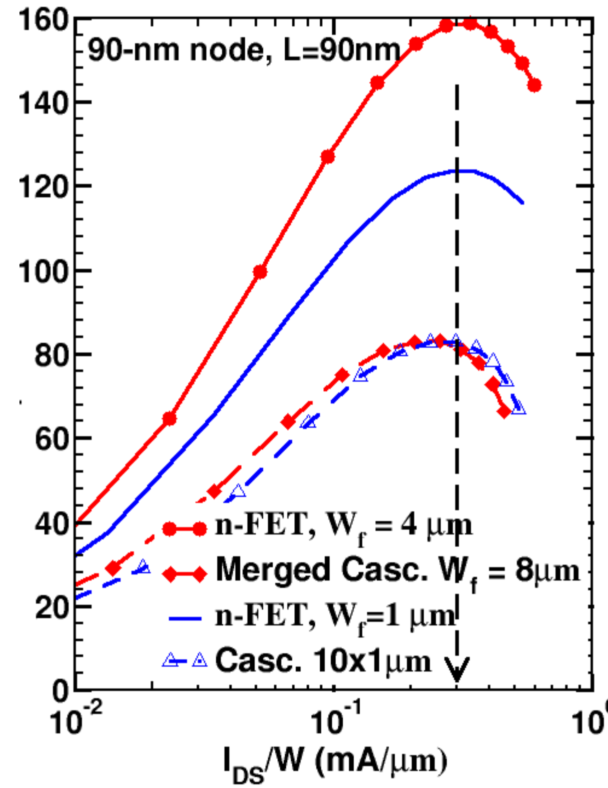
Simpler, smaller area, and lower cost circuits

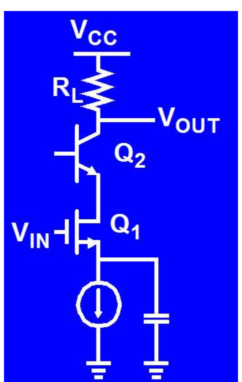
Applications

- 77-GHz automotive radar (60 million cars produced in 2002) and others ...
  - Mm-wave imaging (dental, airport security, 3D inspection of objects)
  - Mm-wave sampling ADCs
  - 60/80 GHz WLAN and Gigabit Ethernet
    - Mm-wave sensors and motes
    - Instrumentation
    - High-speed data communications

What can you count on in production today?



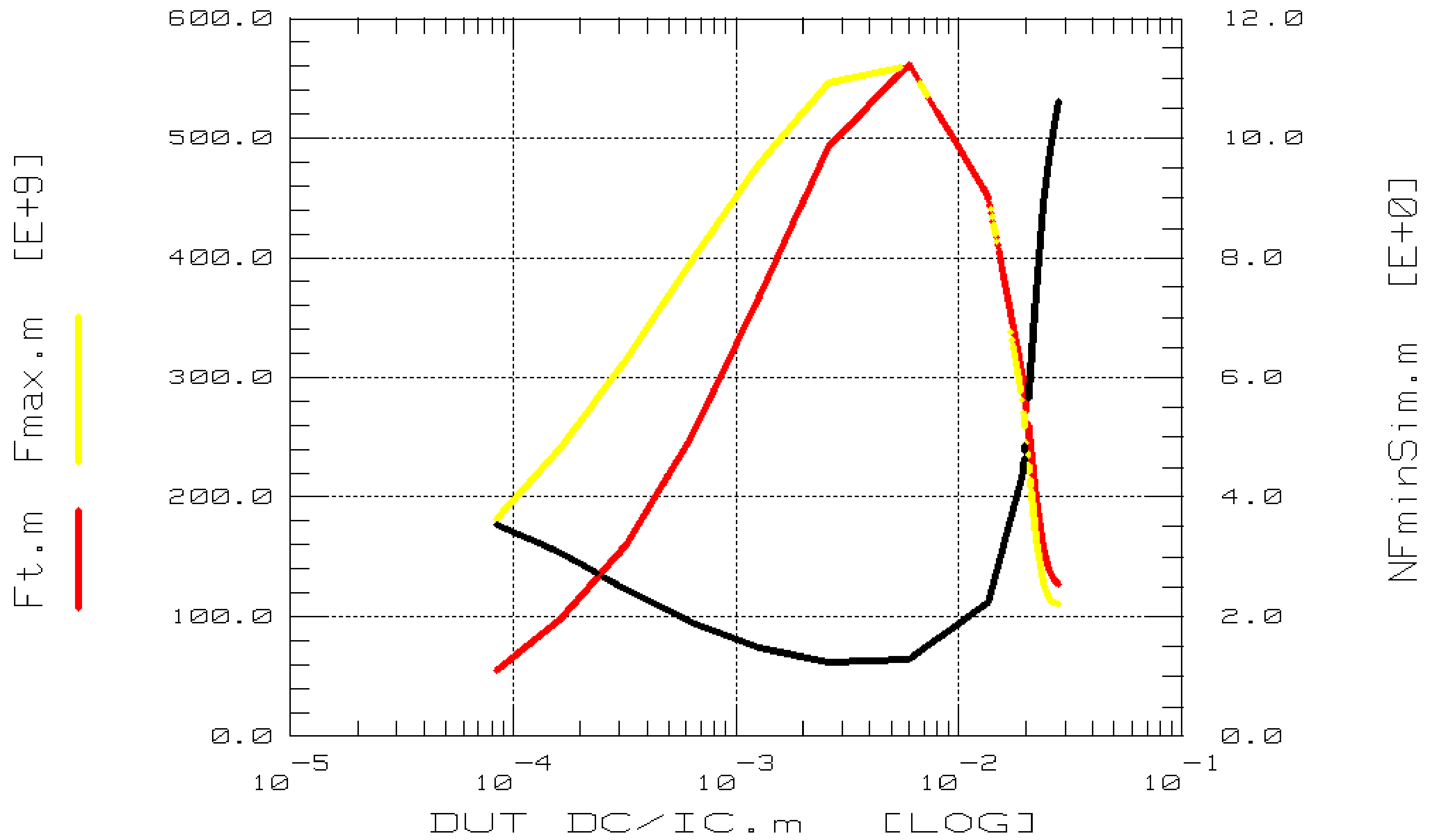




MOS-HBT Cascode

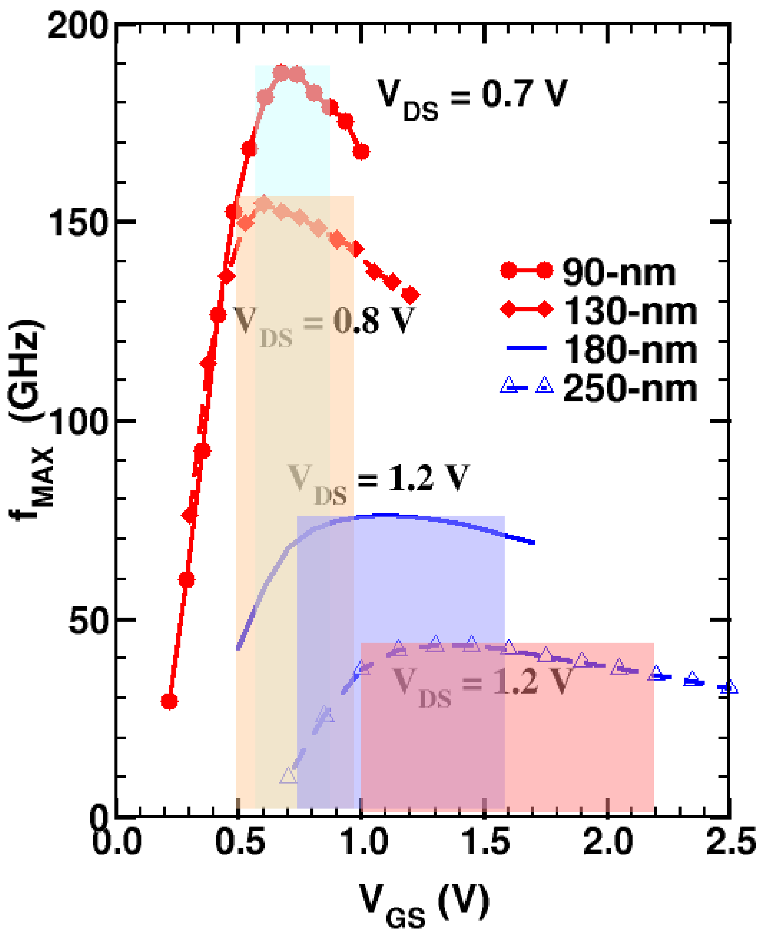
- f_T, f_{MAX} > 140 GHz for both HBTs and FETs
- f_T of MOSFET cascode is < 60% of MOSFET f_T
- Use CS/CE or HBT-based cascodes

Device scaling: Can SiGe HBTs reach 500 GHz?



- 45-nm n-MOSFETs with strain > 400 GHz?
- SiGe HBT > 500 GHz with NF_{MIN}=1.6 dB @ 60 GHz

Impact of scaling on OP_{1dB}

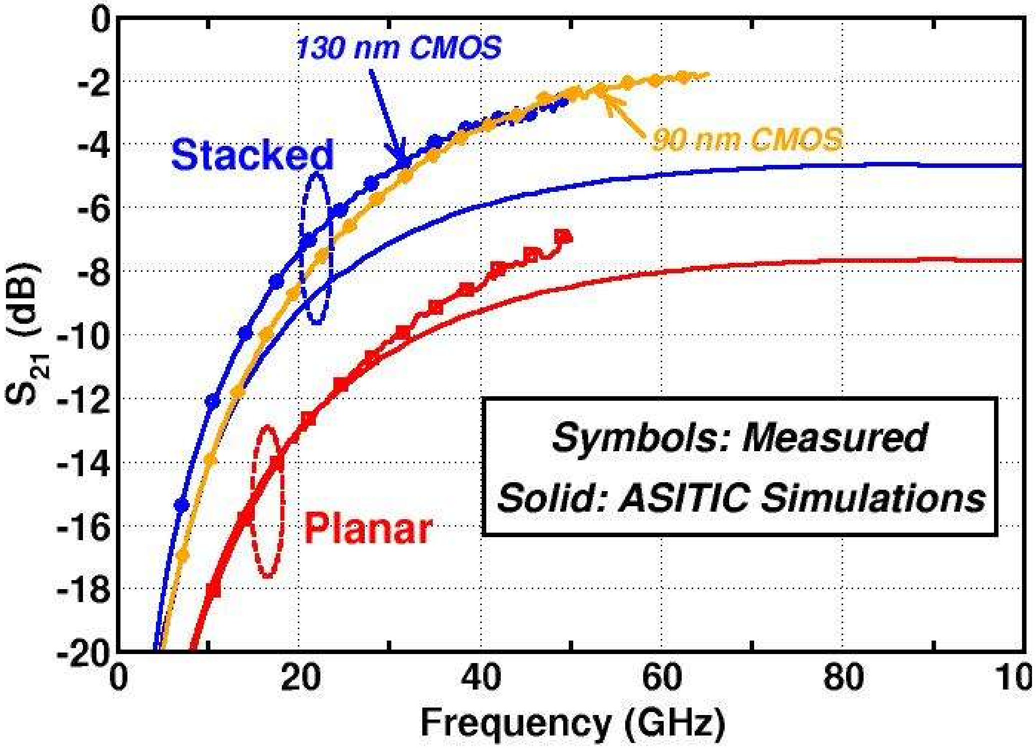


- Linearity depends on $f_{MAX}(V_{GS})$ flatness at peak
- Linear voltage swing at input/output decreases with every new node
- current swing is constant over nodes
- Current and transistor size must be increased to generate the same power as in older nodes

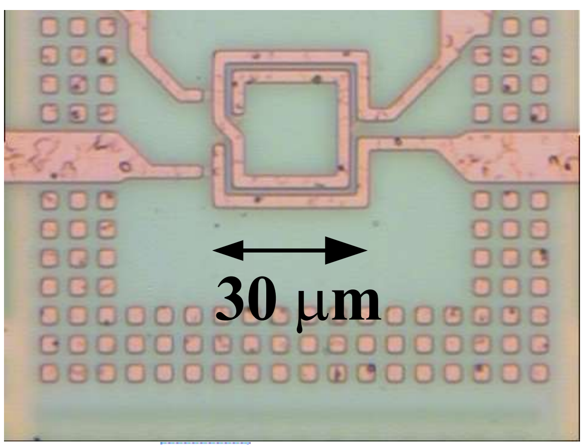
$$OP_{1dB} \propto \frac{\Delta I_{DS} \times V_{MAX}}{8} = 50 \frac{\mu W}{\mu m} \text{ in 90-nm MOSFETs}$$

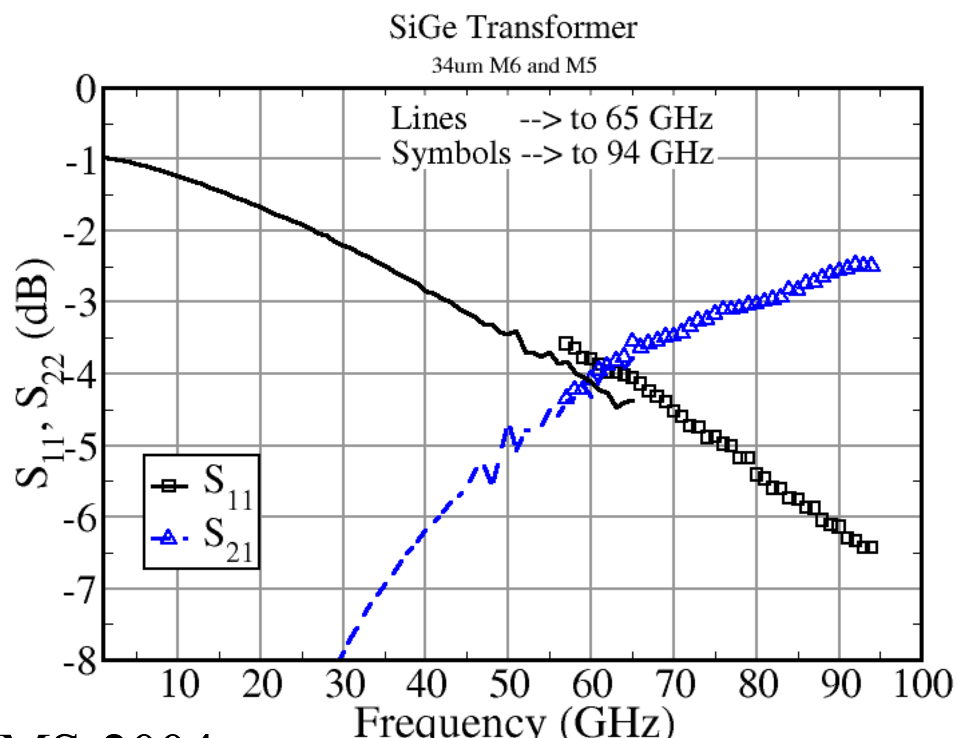
$$OP_{1dB} \propto \frac{\Delta I_{C} \times V_{MAX}}{8} = 376 \frac{\mu W}{\mu m} \text{ in SiGe HBTs}$$

Inductors & transformers ... are getting smaller



- Minimize footprint and stripe width to reduce substrate loss
- Use series-staked multi-layer design





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Mm-wave vs. RF/microwave design

- The Good
  - Inductor size becomes comparable to transistor size
  - Optimal transistor size, bias current and power dissipation decrease with frequency
  - CG/CB noise matching becomes coincidental with 50-Ω matching around 70 GHz
- The Bad
  - Higher noise, reduced gain, and reduced output power
  - Linearity (IIP1, IIP3) and dynamic range suffer due to lower bias currents, exacerbated by lower breakdown voltages
  - R_n increases making noise matching more sensitive to process variations.
- The Ugly
  - Test setups are cumbersome and test equipment cost is prohibitive

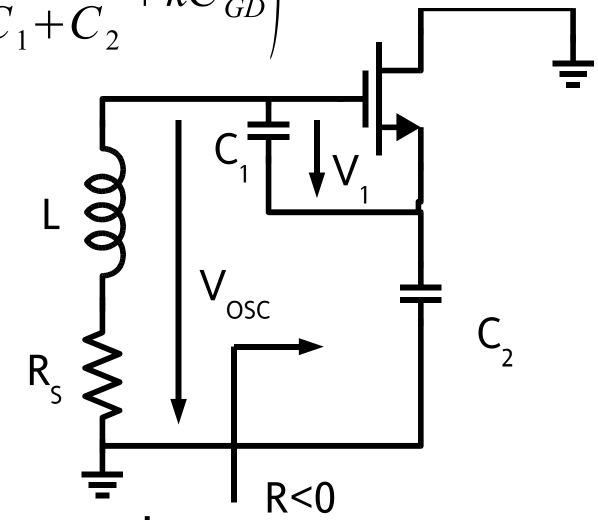
Mm-wave VCO design

$$\frac{1}{f_{osc}} = 2\pi\sqrt{L\left(\frac{C_1 C_2}{C_1+C_2}+kC_{GD}\right)}$$

- Colpitts has higher f_{OSC} and built-in buffering over cross-coupled topology

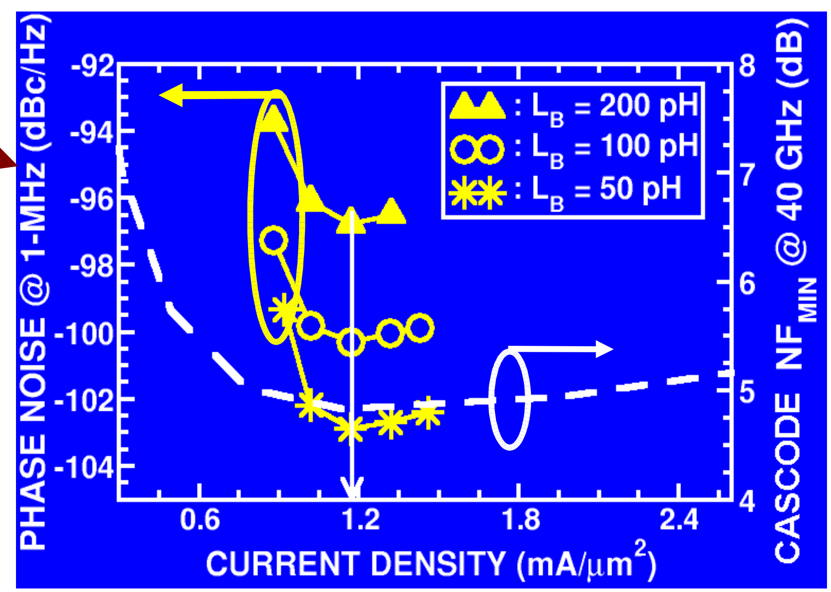
$$\omega_{osc}(n-MOS) \le \frac{g'_m Q_{eff}}{C'_{gs}+4C'_{gd}+C'_{db}+\frac{C_L}{W}}$$

$$\omega_{osc}(Colpitts) \le \frac{g'_m Q_{eff}}{C'_{gs}+C'_{sb}}$$



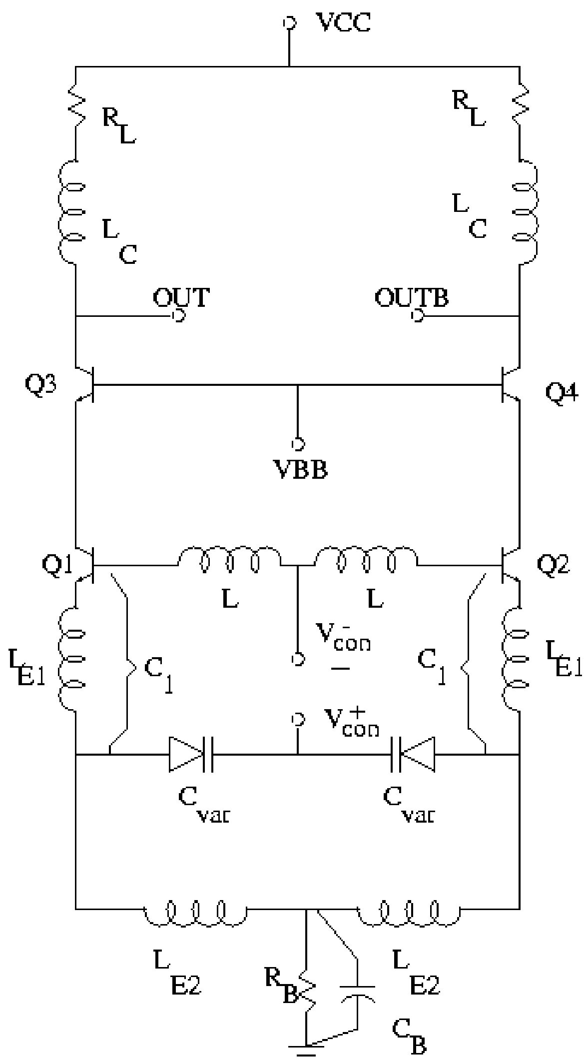
$$R_S = \frac{\omega_{osc} L}{Q} \qquad R = \frac{-g_m}{\omega^2 C_1 C_2}$$

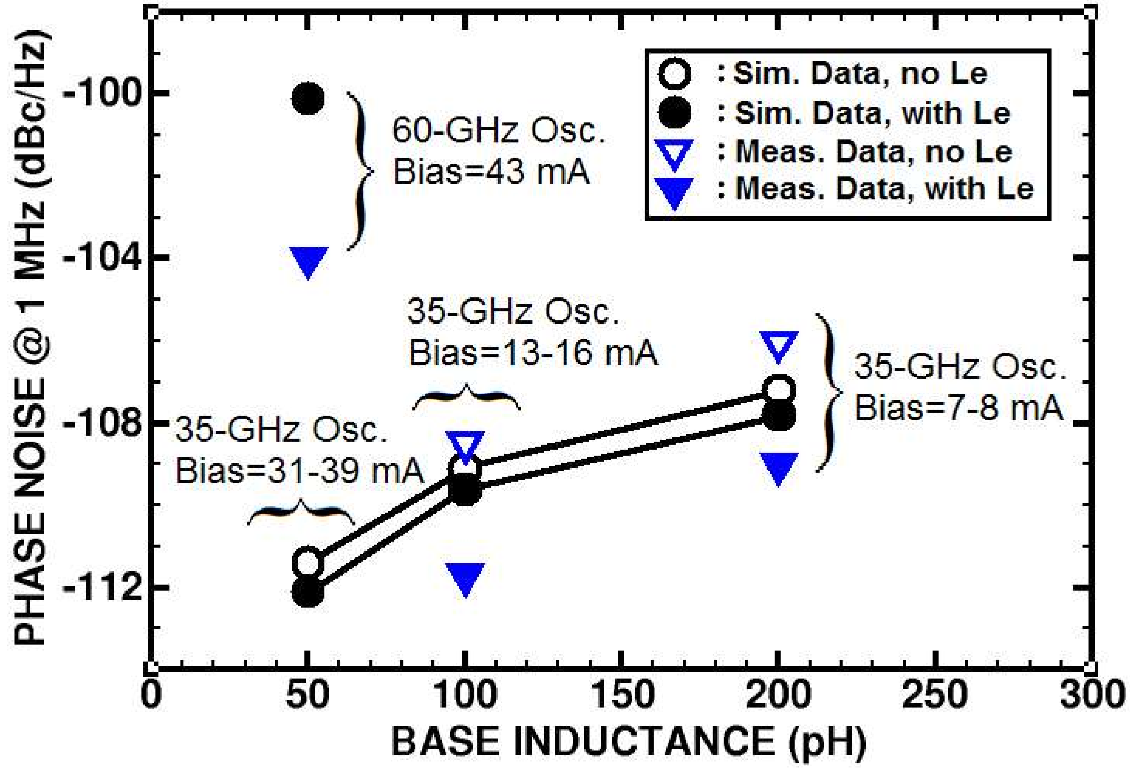
- Bias at optimal NF_{MIN} current density (J_{opt}) of transistor/cascode
- HBT version has 6-10 dB better phase noise due to to higher V_{OSC}



$$L(f_m) = \frac{|I_n|^2}{V_{osc}^2} \times \frac{1}{f_m^2} \times \frac{1}{C_1^2\left(\frac{C_1}{C_2}+1\right)^2}$$

Record low phase noise SiGe BiCMOS VCOs





- Cascode stage for improved buffering
- Inductive degeneration for linearity and low noise
- AMOS varactors for high Q and C ratio

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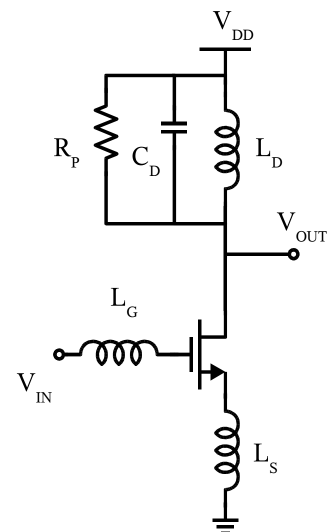
Optimal of mm-wave LNA topology: largely unchanged

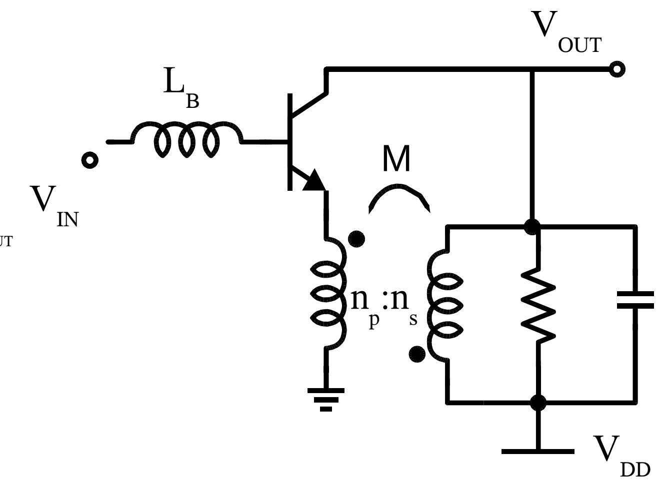
Common emitter/source

- low-voltage, low-noise, good linearity,
- poor isolation => difficult to separately design input/output network



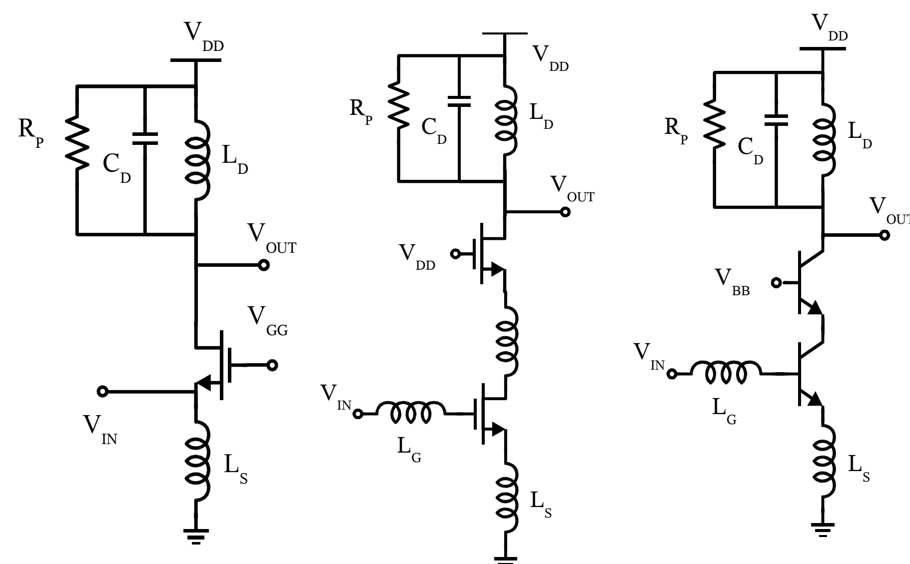
Common base/gate

- low-to-moderate noise, good isolation
- poor linearity, difficult to simultaneously match noise and source impedance



Cascode **(CE+CB, CS+CG,CS+CB)**

- best isolation, low-to-moderate noise, easy to match, good linearity
- higher supply voltage



RF LNA design methodology works beyond 50 GHz!

$$L_S = \frac{Z_0}{\omega_T(cascode)}$$

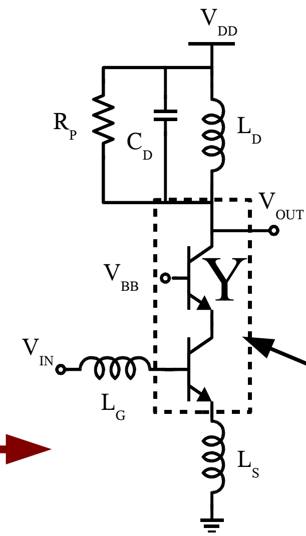
$$G \approx \left(\frac{f_T}{f}\right)^2 \frac{R_P}{Z_0}$$

$$Z_{in} \approx Z_O + j\omega(L_G + L_S) + \frac{1}{j\omega C_{in}}$$

$$L_G \approx \frac{1}{\omega^2 C_{in}} - L_S$$

$Z_{SOPT} = Z_O$

$Z_{IN} = Z_O$

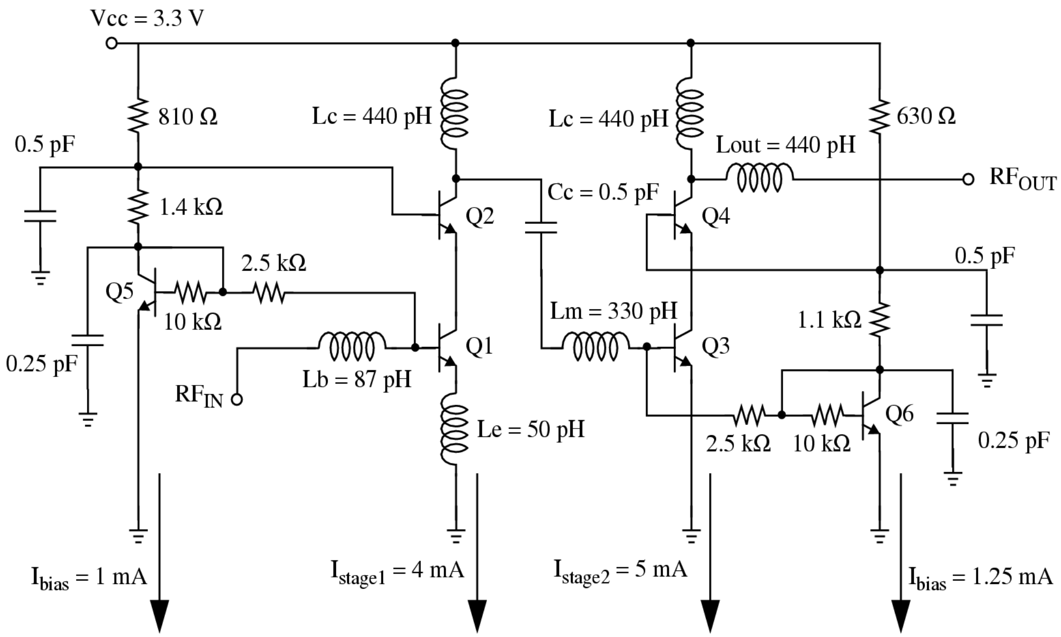


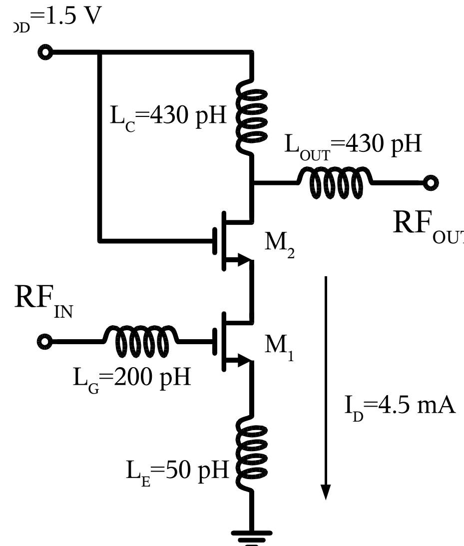
$$h_{21} = \frac{y_{21}}{y_{11}} = \frac{f_T}{jf}$$

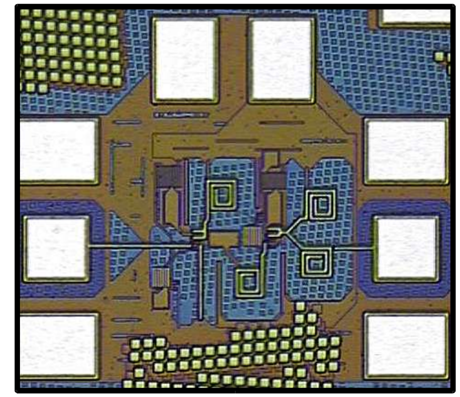
$$y_{11} = \frac{f}{f_T} y_{21} \approx j\frac{f}{f_T} g_m$$

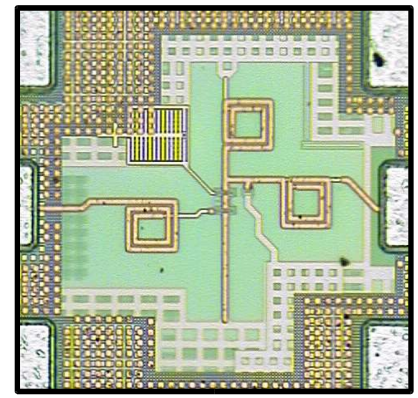
- Matching of real part of input impedance is
  - broadband,
  - independent of transistor size, and
  - independent of bias current => can increase current for better linearity
- Increasing Z_0 (to save power) degrades gain.

180-nm SiGe HBT vs. 90-nm CMOS LNAs @ 52 GHz

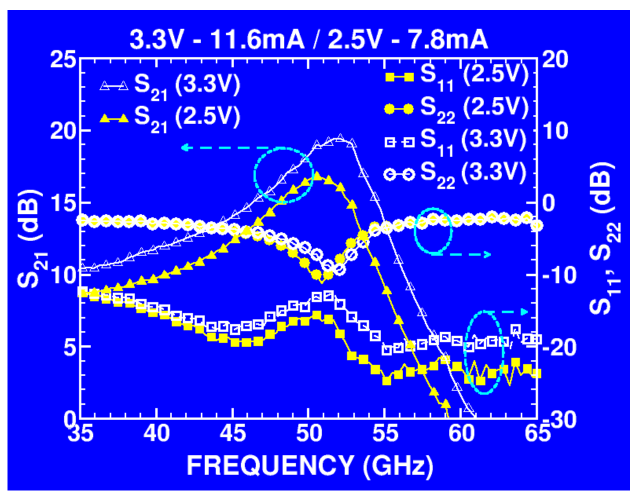


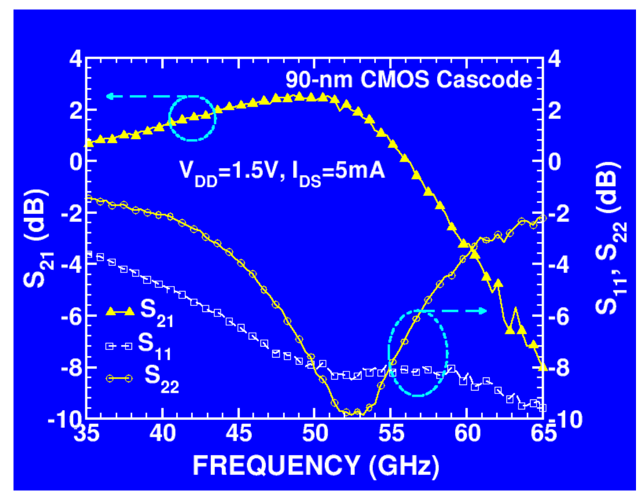






- identical inductors
- identical centre frequency
- g_m & inductors dictate performance





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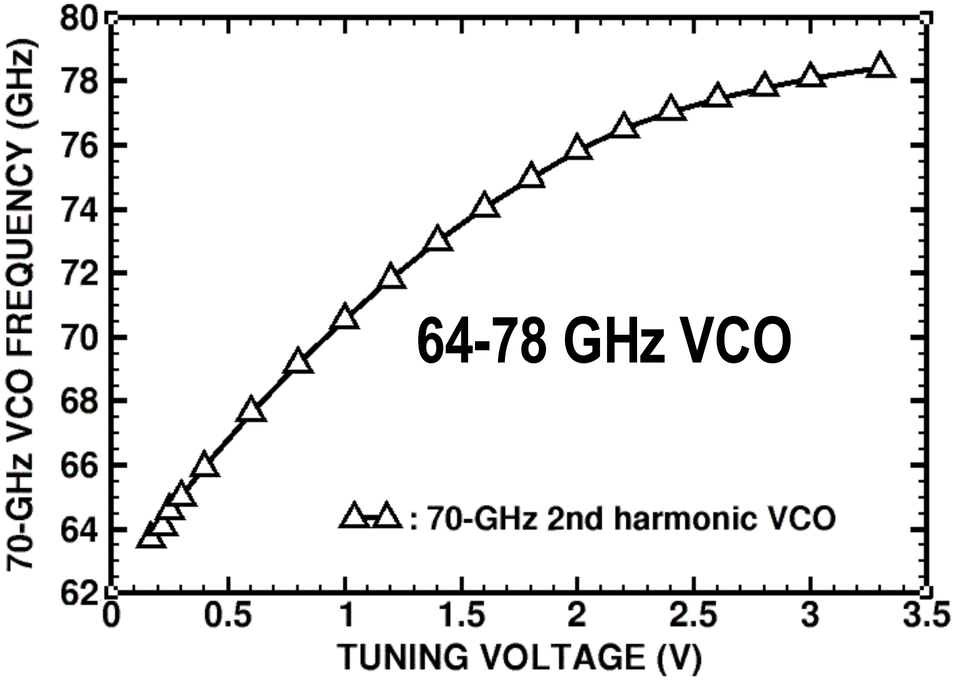
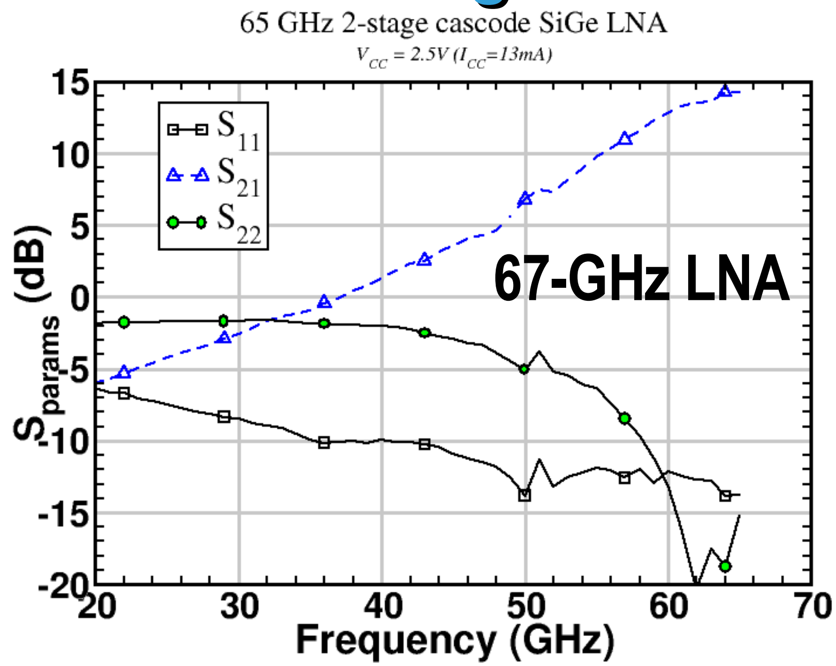
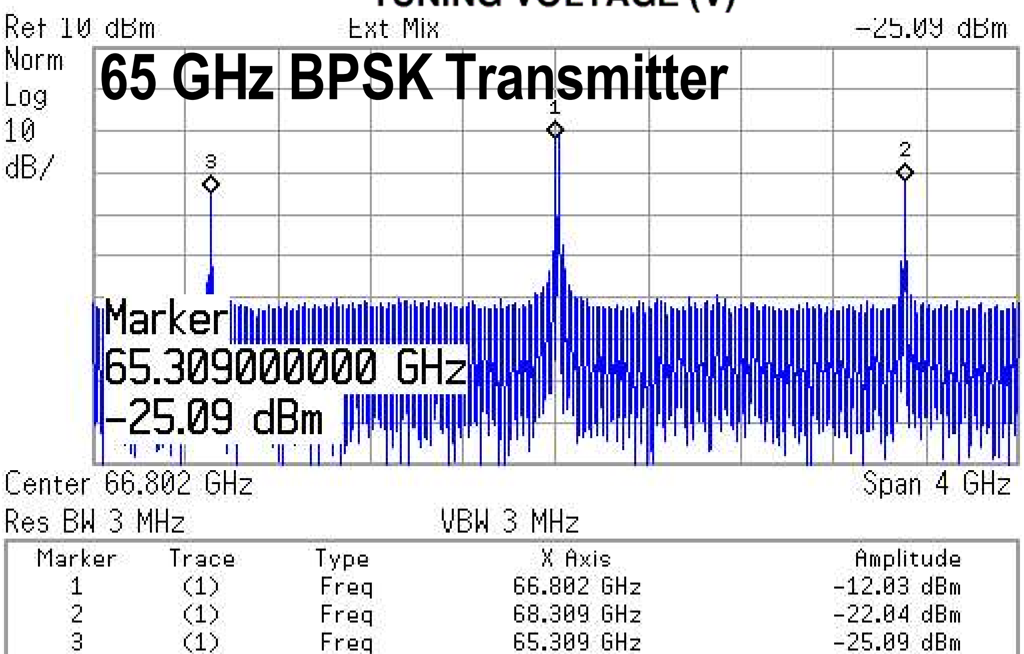
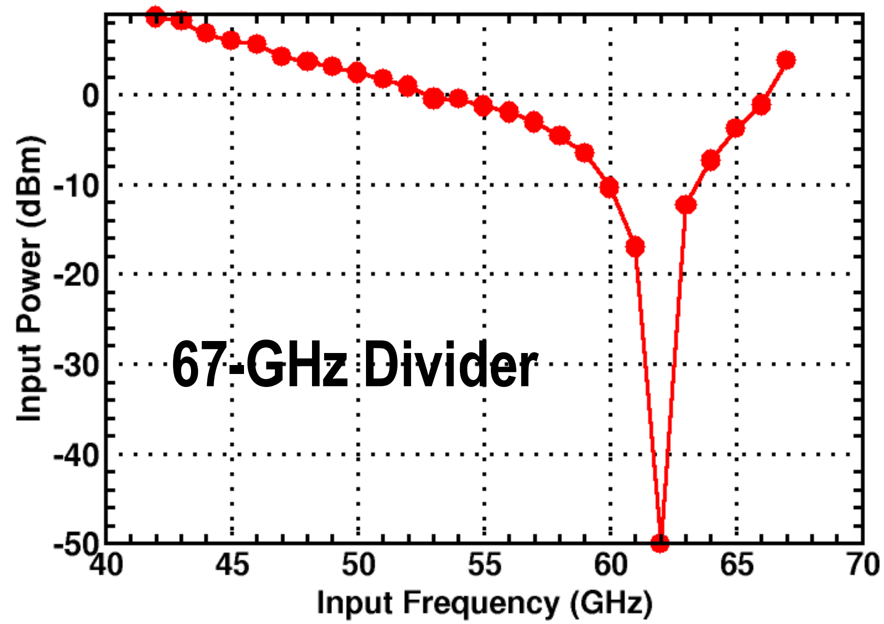
Portfolio of 65-GHz SiGe BiCMOS building blocks

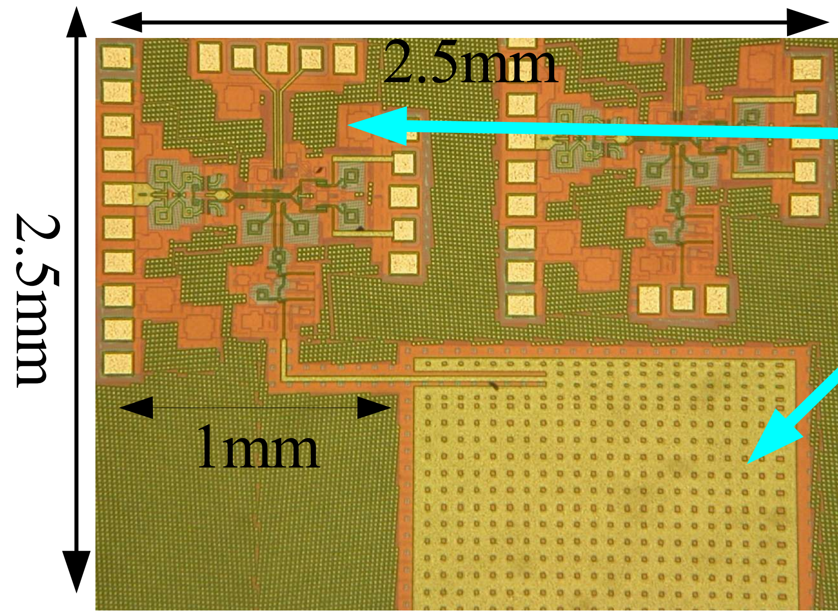


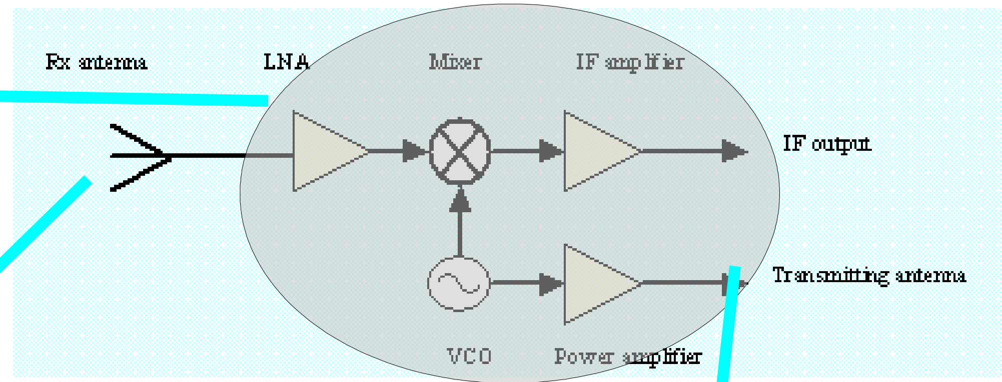




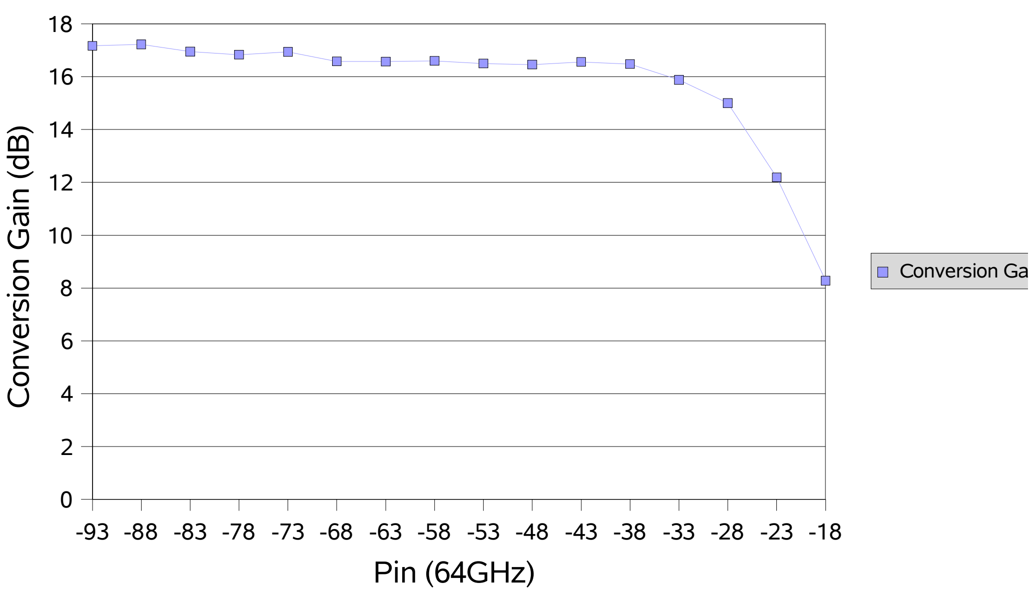


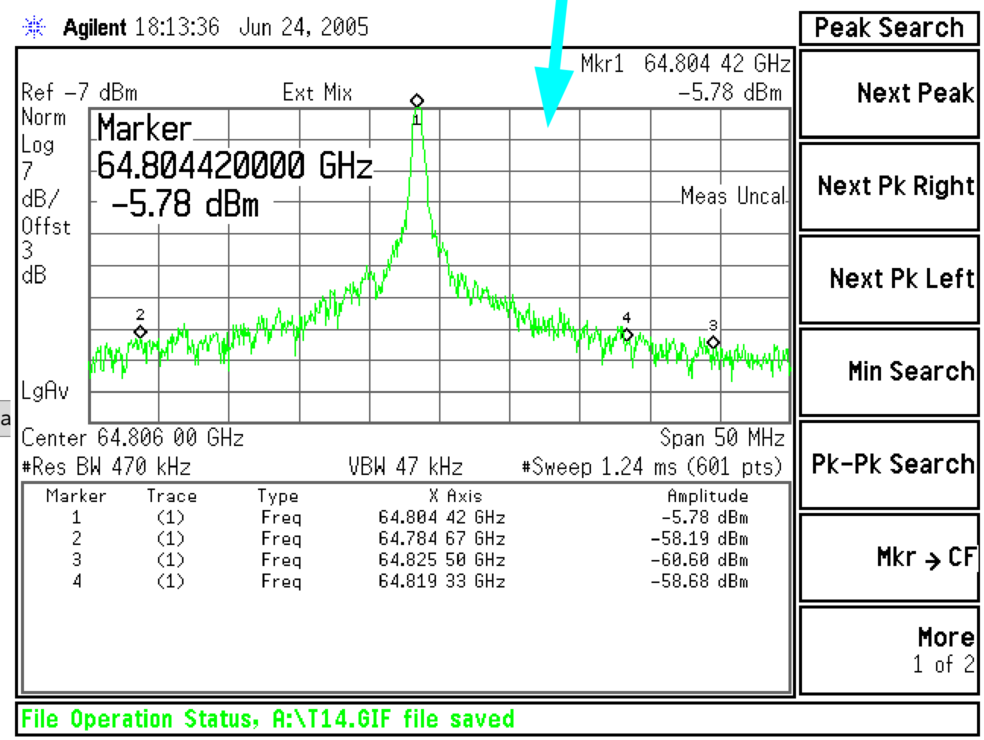
65-GHz Doppler radar transceiver with patch antenna





RX single-ended conversion gain at IF=730MHz





Conclusions

- Mm-wave SOCs can be realized in today's production 180-nm SiGe BiCMOS and 90-nm RFCMOS technologies.
- Circuit topologies and design methodologies are largely unchanged from those used at 2-10 GHz.
- Mm-wave die size and cost (significantly) smaller than at 2-10 GHz.
- Low-to-moderate volume products make economic sense in coarser lithography SiGe BiCMOS technology.
- Testing is the bottleneck ... but why bother testing at mm-waves?

Acknowledgements

- Jazz Semiconductor and TSMC for chip fabrication
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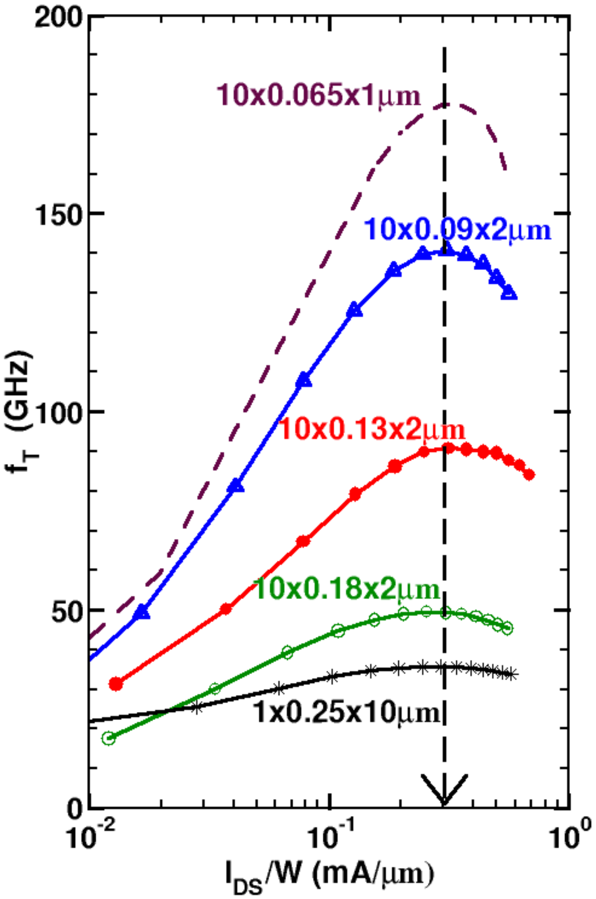
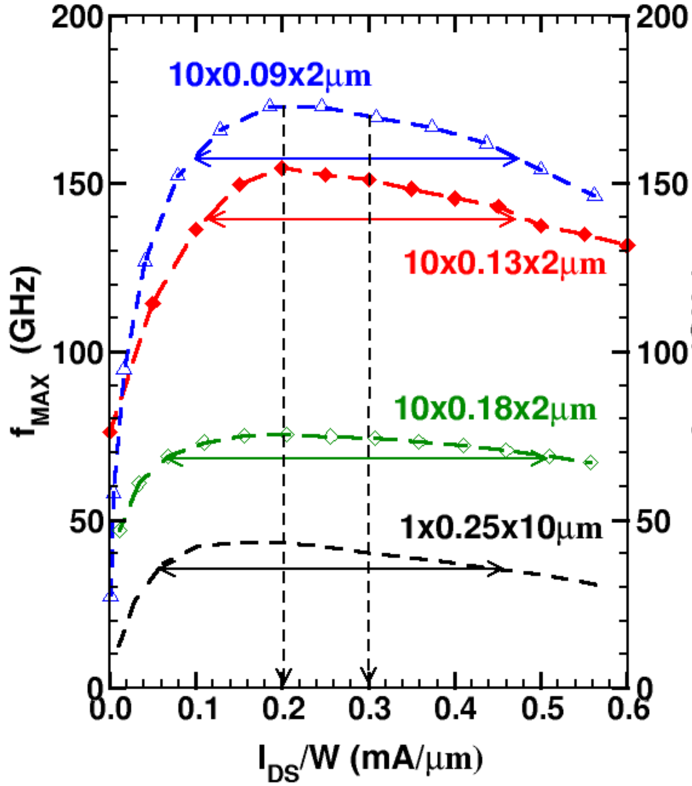
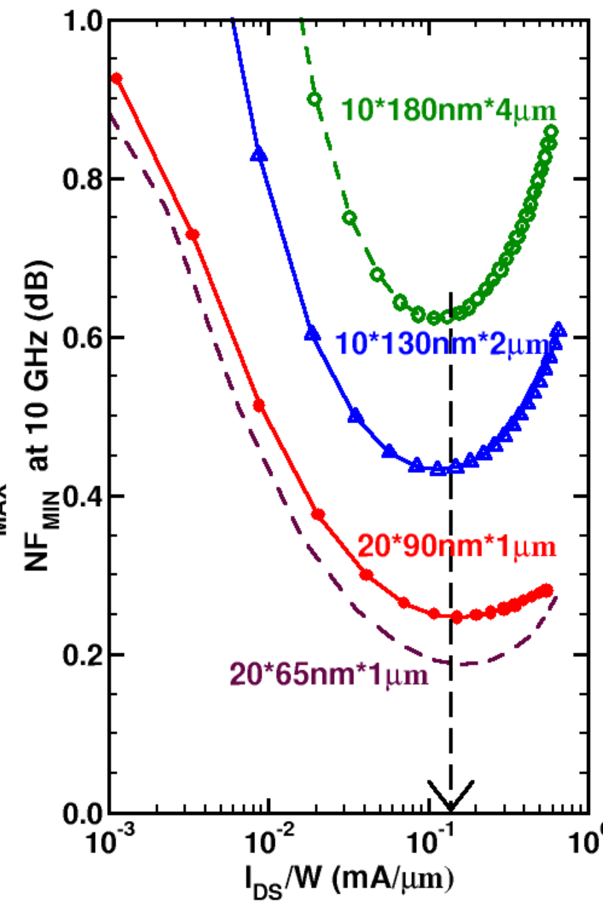
- CFI and OIT for equipment grants
- CMC and Jaro Pristupa for CAD support

n-MOSFET characteristic current densities invariant across technology nodes and foundries (65-nm sims only)





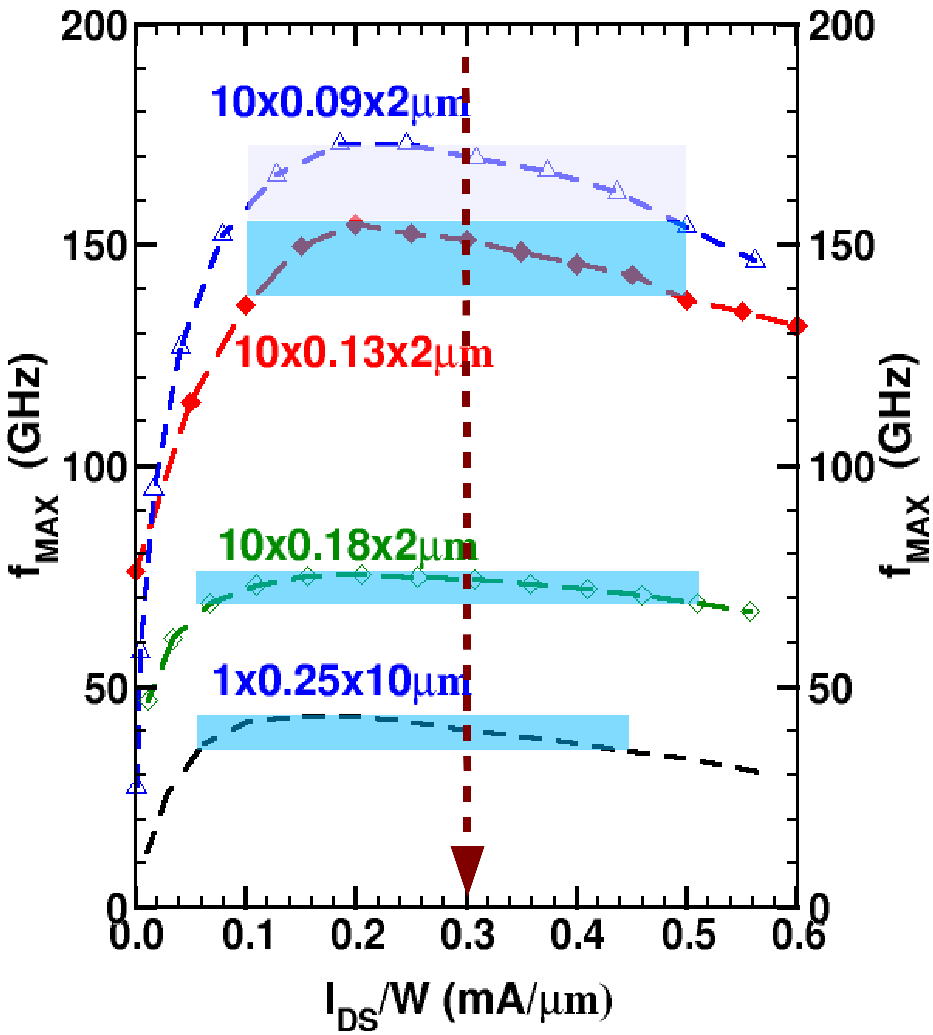


Peak f_T @ 0.3 mA/µm

Peak f_{MAX} @ 0.2 mA/µm

NF_{MIN} @ 0.15 mA/µm

Biasing at I_{peakfT} in power amplifier, linear amplifier, or upconvert mixer

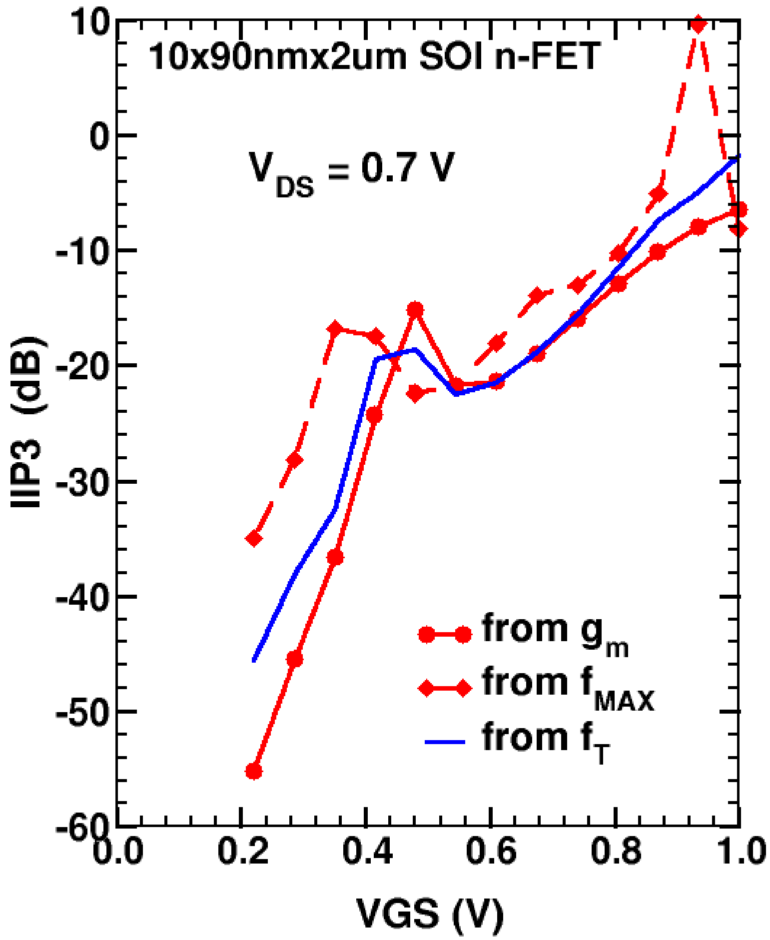


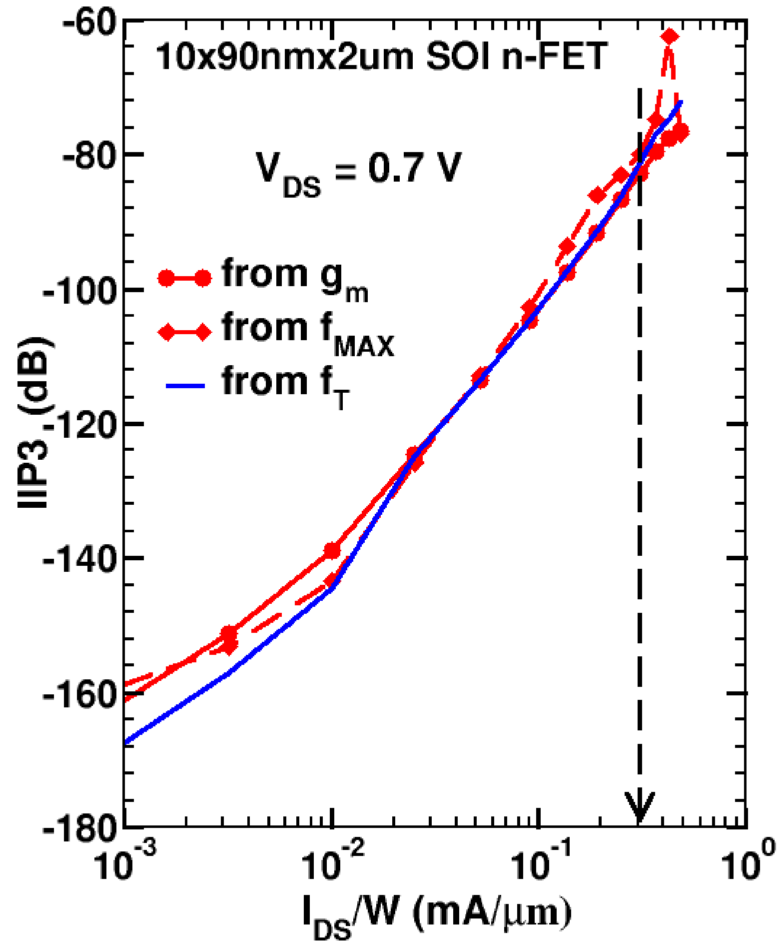
- Linearity depends on $f_{MAX}(I_{DS})$ flatness

$$OIP3 \sim \frac{f_{MAX}}{\frac{\partial^2 f_{MAX}}{\partial I^2_{C(DS)}}} \quad vs. \quad \frac{g_m}{\frac{\partial^2 g_m}{\partial I^2_{C(DS)}}}$$

- f_{MAX} captures both input (through f_T) and output linearity (through g_{ds})
- But optimal linearity bias corresponds to peak f_T : 0.3 mA/μm
- Allows for 400 μA/μm$_{(p-p)}$ or 460 mV$_{p-p}$ of linear swing

The mirage of the linearity "sweet-spot"





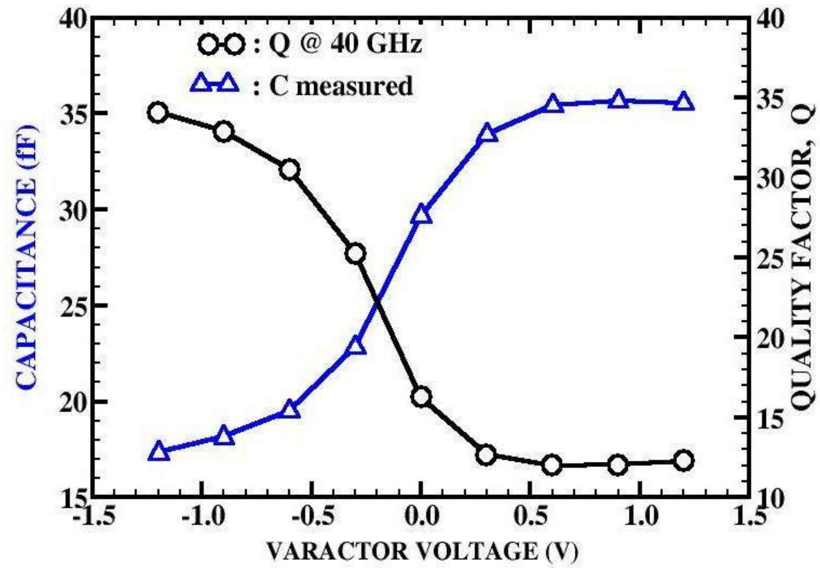
$$OIP3 \sim \frac{f_{MAX}}{\frac{\partial^2 f_{MAX}}{\partial V_{GS}^2}} \text{ vs. } \frac{g_m}{\frac{\partial^2 g_m}{\partial V_{GS}^2}}$$

$$OIP3 \sim \frac{f_{MAX}}{\frac{\partial^2 f_{MAX}}{\partial I_{C(DS)}^2}} \text{ vs. } \frac{g_m}{\frac{\partial^2 g_m}{\partial I_{C(DS)}^2}}$$

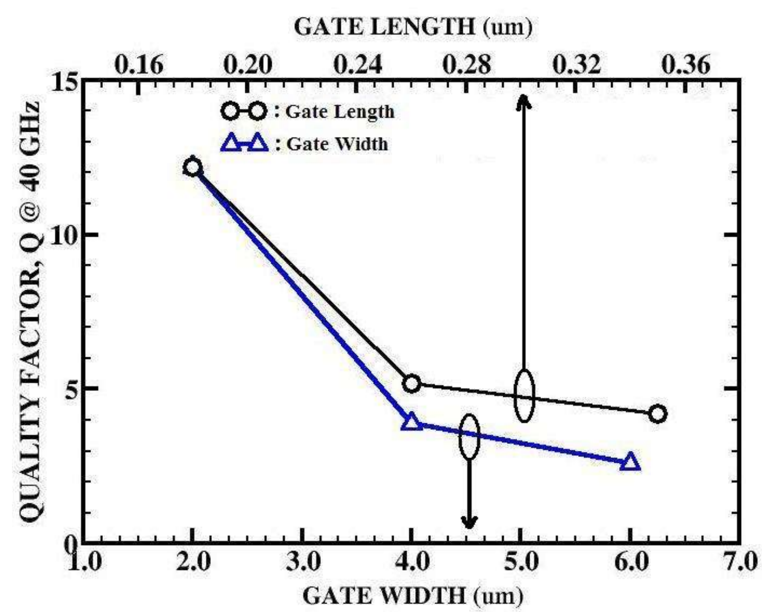
Small signal linearity (oxymoron?) vs. large signal linearity!

Why AMOS vs. pn-junction varactors @ mm-waves?

- Higher Q
- Larger cap. ratio
- Linear tuning curve
- Lower supply voltage



Use minimum finger length and width for highest Q



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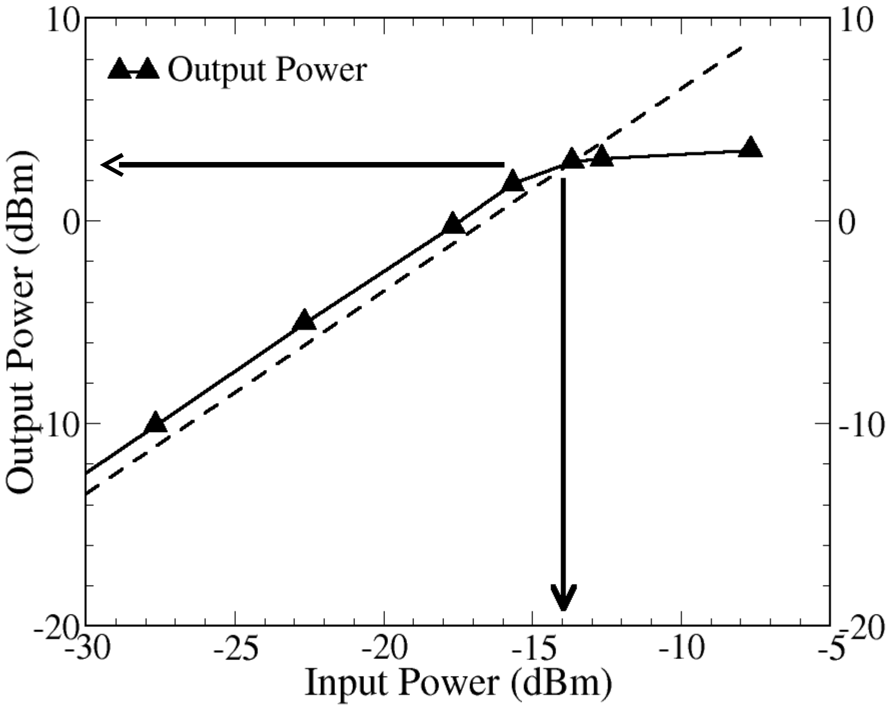
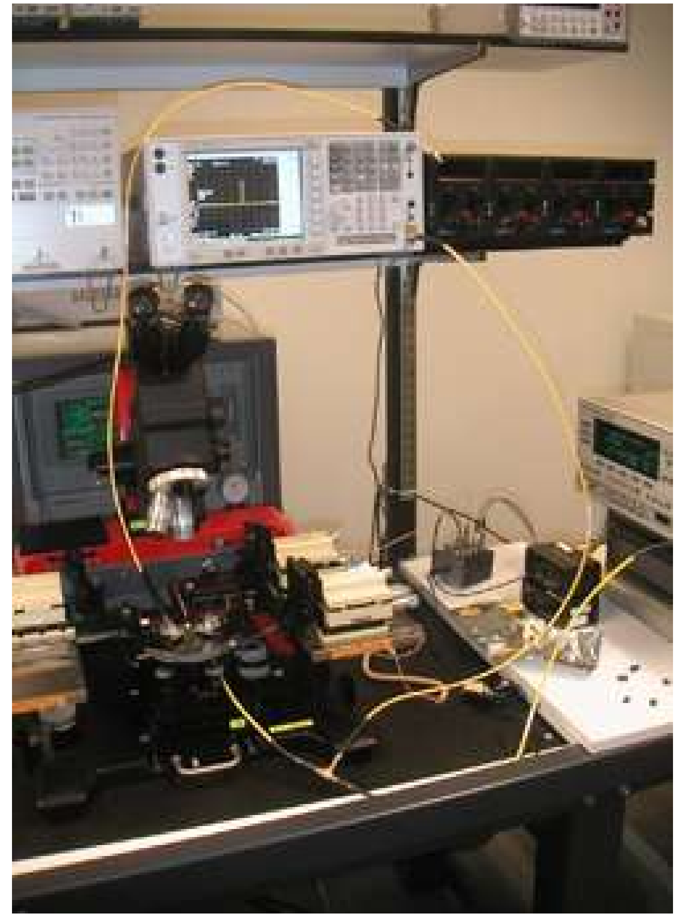
Mm-wave circuit design guidelines

- Use RF-like lumped rather than distributed passives:
  - Inductor vs. t-line tanks and matching networks
  - Transformers vs. hybrid couplers
  - Inductor/MIM poly-phase filter vs. 90deg hybrid coupler
- Isolation remains biggest issue:
  - Possible to have ground plane below inductors to improve isolation
  - Patch antenna with M1 ground plane

SiGe HBT LNA: Linearity Measurements

Measured 1dB compression at 50 GHz (V_{CC}=3.3V)





- Input 1 dB compression point of **-14 dBm**
- Output 1 dB compression point of **3 dBm**

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