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VLSI Compatible Si/SiGe/Si p-MOSFET's

by

Petre Sorin Voinigescu

A thesis submitted in conformity with the requirements
for the degree of Doctor of Philosophy
Graduate Department of Electrical and Computer Engineering
University of Toronto

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VLSI Compatible Si/SiGe/Si p-MOSFET's

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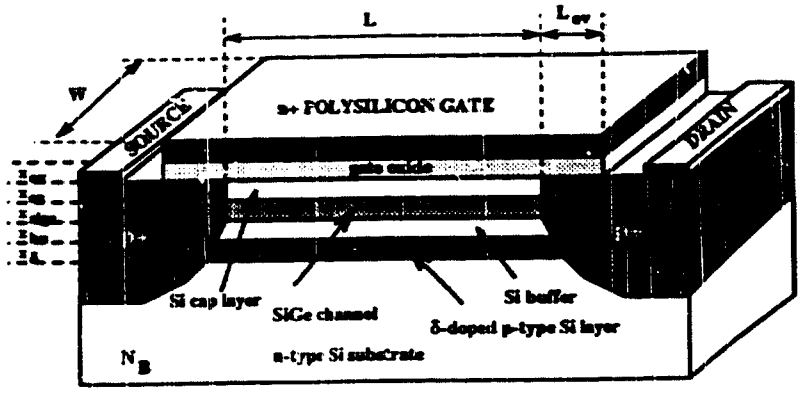

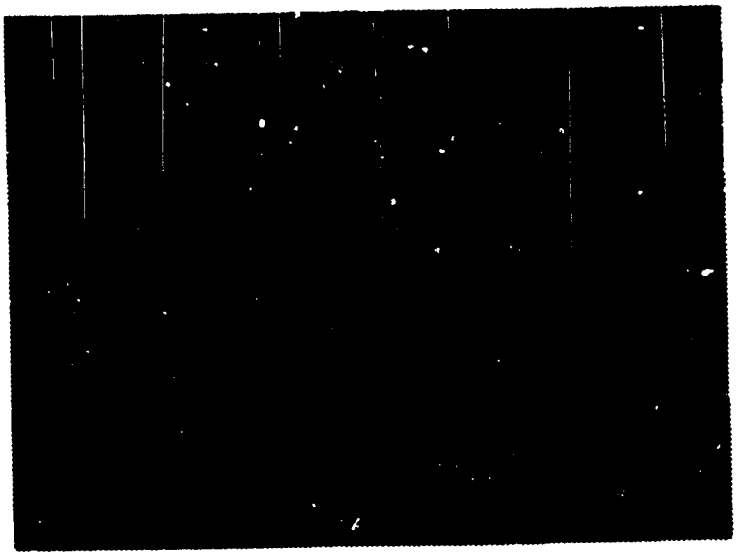

University of Toronto

VLSI Compatible Si/SiGe/Si p-MOSFET's

Doctor of Philosophy Degree, 1994

Petre Sorin Voinigescu

Graduate Department of Electrical and Computer Engineering

University of Toronto

ABSTRACT

Silicon-Germanium (SiGe) has emerged as a promising vehicle for expanding the performance bounds of silicon-based VLSI technology. Attempts are now underway worldwide to demonstrate that SiGe field effect transistors can reach industrial maturity. In particular, SiGe p-MOSFET's require the most urgent attention because of the poor performance of silicon p-channel devices. A novel Si/SiGe/Si p-MOSFET structure is proposed here, whereby the effective hole mobility is maximized by employing a buried SiGe channel with triangular Ge profiles. The benefits of the triangular Ge channel, in comparison with the established rectangular Ge channel profile, were demonstrated both theoretically and experimentally. The SiGe p-MOSFET's were implemented in-house, in a VLSI compatible process that allowed for the integration of silicon and SiGe p-MOSFET's on the same chip. Hole mobilities of 400 cm^2/Vs and 250 cm^2/Vs were measured for devices with 0-50% Ge triangular and 25% Ge rectangular channels, respectively. A factor of two improvement in transconductance with respect to the equivalent, on-chip silicon p-MOSFET was obtained. When compared to rectangular Ge profile devices, the MOSFET's with triangular Ge channel profiles demonstrated 30-40% improvement in mobility, transconductance and cutoff frequency. New methods to characterize the band offset and doping concentration in Si/SiGe layers, as well as the mobility profiles inside the channel, were also developed and validated experimentally.

ACKNOWLEDGMENTS

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I would also like to acknowledge several external collaborators without whose contribution this work would not have been possible. These are Dr. Derek C. Houghton and Dr. Jean-Pierre Noël from the National Research Council of Canada, Ottawa, who have been kind enough to grow the MBE Si/SiGe layers, and Dr. Theodore I. Kamins of Hewlett-Packard Laboratories, Palo Alto, Ca., whom I have never met in person, but who presented me with the gift of CVD grown Si/SiGe wafers. My thanks also go to Dr. Peter B. Rabkin of Silvaco International, Santa Clara, Ca., who has provided us with free copies of the first commercial two-dimensional heterostructure device simulator. Without his help and prompt advice the Si/SiGe/Si p-MOSFET's discussed in this thesis would have taken much longer to understand and design.

I would like to thank Jaro Pristupa and Dana Reem for being there whenever I needed their help (and that was not infrequent, I may add), as well as the students and staff in the Integrated Circuits Lab at the University of Toronto for creating an excellent working environment.

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Last, and not least, I thank my family for having endured through it all.

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CHAPTER 1

INTRODUCTION

1.1. Why Silicon-Germanium ?

Silicon technology has reached a very mature stage at which incremental progress is achieved with increasing difficulty. Further improvements in the performance of silicon IC's can be expected by using novel materials and device structures. One of these possibilities is being offered by an alloy of silicon and germanium SiGe, grown on Si substrates, which can form the basis for a host of new high speed electronic and optoelectronic devices [1-4].

While compatible with existing silicon chip-fabrication lines [3], SiGe offers a significant increase in device performance due to its superior transport properties as compared to silicon. Carrier mobilities are larger in SiGe than in Si [1,5] and result in higher speed of operation of SiGe devices. The energy bandgap of SiGe is smaller than that of silicon [5] and linearly scales with the Ge content, opening up exciting opportunities to build devices based on bandgap engineering concepts. These favorable properties of SiGe have spurred great interest in the IC community over the last few years.

One possible system application for SiGe devices is a portable digital transceiver. As illustrated in Fig.1.1. a state of the art version of such a transceiver is built

up from four chips, three of which are implemented in silicon and one in GaAs.

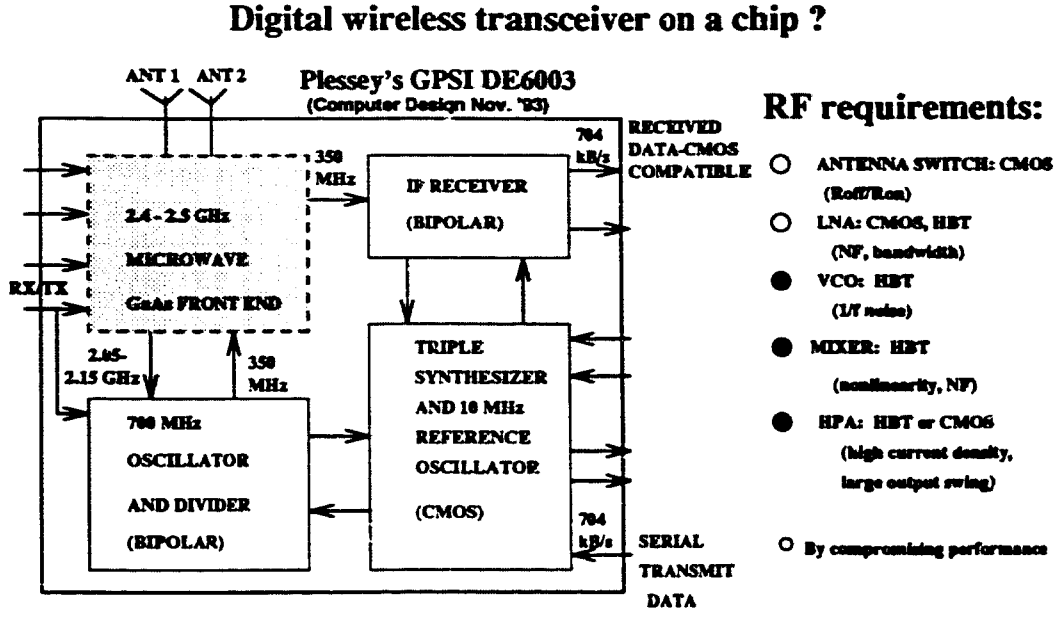

Figure 1.1 *Possible application of Si/SiGe technology in a single-chip digital wireless transceiver. Current Si/SiGe device performance allows for the replacement of the GaAs block by a Si/SiGe circuit.*

State of the art Si/SiGe HBT's can deliver most functions currently implemented in the RF GaAs block, with the exception of the low noise amplifier and antenna switching functions. Si/SiGe CMOS devices would be more suitable for the latter two circuits. High speed Si/SiGe CMOS devices would also facilitate a significant increase in the digital data rate. With its high speed, low voltage and low power features, Si/SiGe technology has the potential to integrate all these functions on a single chip, thus making the wristwatch personal communicator a possibility in the near, rather than distant, future.

1.2. Silicon-Germanium Material Properties

1.2.1. Lattice Constant and Film Growth

Irrespective of the Ge mole fraction Y, $Si_{1-Y}Ge_Y$ maintains a diamond structure, which is characteristic for both silicon and germanium [2,5]. The lattice constant of $Si_{1-Y}Ge_Y$ depends on the mole fraction Y and, for low Y, can be expressed as [5]

$$a_{SiGe} = a_{Si} + Y(a_{Ge} - a_{Si}) \tag{1.1}$$

where a_{Si} is the lattice constant of silicon and a_{Ge} is the lattice constant of germanium. Since a_{Si} (0.5431 nm) and a_{Ge} (0.5646 nm) have different values, a lattice mismatch of 4.17% occurs at room temperature. Because of the lattice mismatch, only thin layers of SiGe can be grown free of misfit dislocations on a silicon substrate. As illustrated schematically in Fig. 1.2, two situations can occur when a SiGe layer is grown on top of a Si substrate **a)** an in-plane compressed (coherently) strained SiGe lattice with a corresponding lattice expansion along the growth direction and **b)** generation of dislocations at the SiGe/Si interface.

In the first case, known as pseudomorphic growth [5], coherent mechanical strain builds up in the SiGe film to retain a dislocation free interface between Si and SiGe. The in-plane lattice constant of the SiGe film thus grown is given by the equation [5]

$$a_{in-plane} = \frac{a_{SiGe}x_{SiGe} + a_{Si}x_{Si}}{x_{SiGe} + x_{Si}} \tag{1.2}$$

where x_{SiGe} and x_{Si} are the thicknesses of the SiGe film and of the Si substrate, respectively.

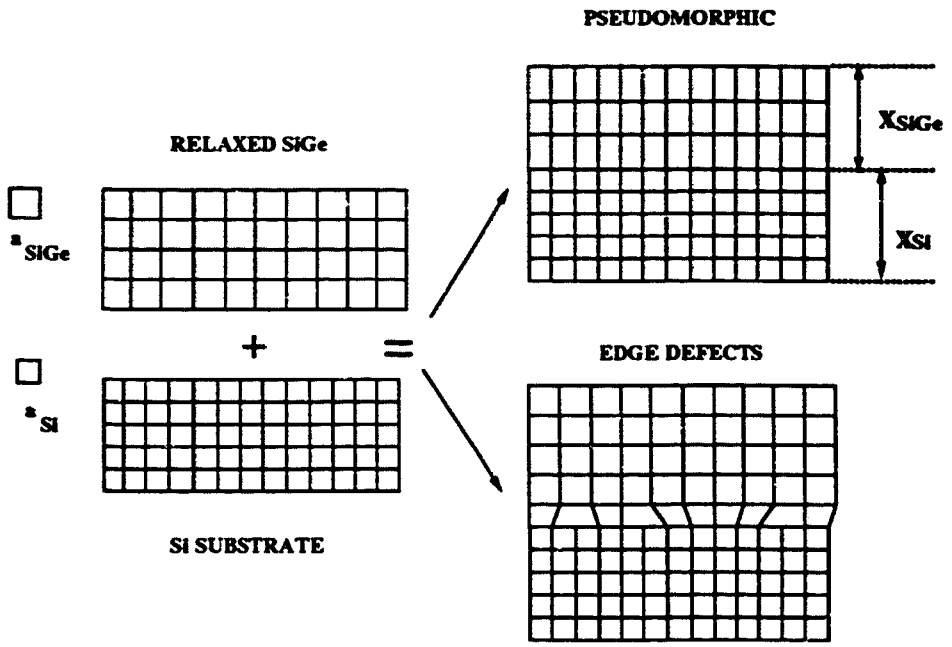

Figure 1.2 *Schematic illustration of the mechanisms by which thin SiGe films can be grown on a Si substrate.*

The second case, generation of dislocations, produces a very defective interface between SiGe and Si which results in a poor quality SiGe film being grown on top of the silicon substrate. For these reasons, only pseudomorphic SiGe films are of interest for device and circuit applications.

For the film to be strained and dislocation free during and after growth, two conditions must be met. First, the SiGe film must be thin enough to accommodate the strain, i.e. $x_{SiGe} \ll x_{Si}$. The thickness of the film is bound by the Matthews-Blakeslee

critical value [6], which is a function of the lattice mismatch. For SiGe films, the critical thickness decreases strongly as the Ge mole fraction increases [5]. Second, the temperature during the growth and during all subsequent processing steps must be sufficiently low in order to prevent strain relaxation. The requirement for low temperature processing results from the typically metastable character of most strained SiGe films used in semiconductor devices. Under high temperature conditions, the film cannot maintain the strain and misfit dislocations are generated. In fact, both the temperature and the duration of the process, i.e. the thermal budget, are important. As an example, temperatures up to 600 °C applied for tens of minutes are considered to be "safe", while those up to about 900 °C are "acceptable" for time intervals up to two minutes before strain relaxation and generation of dislocations set in [7]†.

In the example considered in Fig. 1.2, the SiGe film was grown on a silicon substrate. In some device applications a complementary processing sequence, the growth of a tensile strained silicon layer on top of a relaxed SiGe layer, is important. Both systems, strained SiGe on relaxed Si and strained Si on relaxed SiGe, can be grown either by Molecular Beam Epitaxy (MBE) [8], or by one of several variants of Chemical Vapor Deposition (CVD) techniques such as High Vacuum (HV-CVD) [1], Rapid Thermal (RT-CVD) [9] or Limited Reaction Processing (LRP-CVD) [7]. Because of the better quality of the grown layers and because of the possibility of processing a batch of wafers in one run, HV-CVD has emerged as the industry

† The MOSFET structures described in this thesis are within the Mathews-Blakeslee critical thickness. While this and other strain-relaxation models are still debated, these experimental results, as well as IBM's SiGe MOSFET's [2] indicate that average Ge mole fractions of 25% over 15 nm are technologically feasible.

standard for the growth of Si/SiGe heterojunctions [1-3].

1.2.2. Bandgap

One of the key features of SiGe is its energy bandgap $E_{G_{SiGe}}$, which is lower than that of silicon $E_{G_{Si}}$. The bandgap of SiGe depends on the Ge mole fraction Y and changes from 1.17eV for Y = 0 to 0.78 eV for Y = 0.5 [5]. In this range of Ge mole fractions, the dependence has an approximately linear character [5].

$$\Delta E_G = E_{G_{Si}} - E_{G_{SiGe}} = 0.74*Y \tag{1.3}$$

In addition to the energy bandgap, a critical issue for device operation is the actual bandgap alignment between SiGe and Si. The two combinations of Si and SiGe that are relevant for device operation and the corresponding energy bands alignments are illustrated schematically in Fig. 1.3.

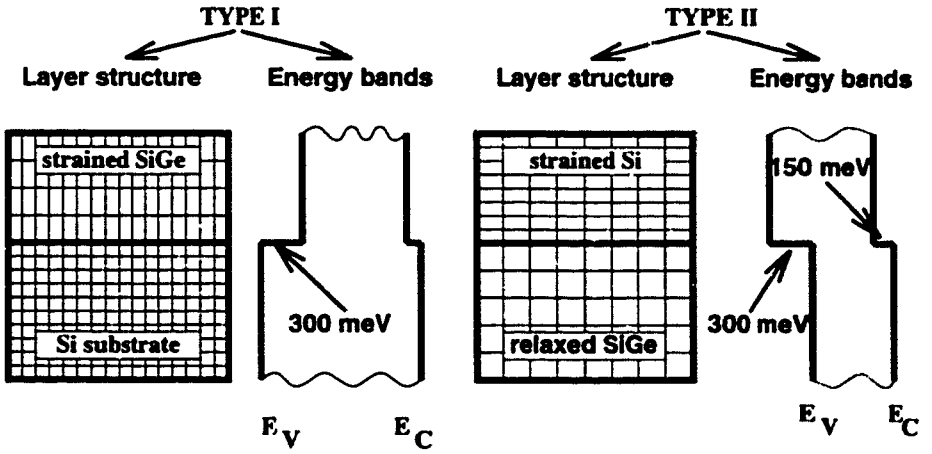

Figure 1.3 *Schematic illustration of the energy bands alignment and of the layer structure in type I and type II Si/SiGe heterostructures. In both cases the Ge mole fraction Y is 0.5.*

The band alignment shown in the left side of Fig. 1.3 is of the type I character, i.e. the SiGe bandgap lies within the Si bandgap. The bandgap difference ΔE_G is the sum of the valence band ΔE_V and of the conduction band ΔE_C offsets

$$\Delta E_G = \Delta E_V + \Delta E_C \tag{1.4a}$$

and is accommodated almost entirely in the valence band (i.e. $\Delta E_V \gg \Delta E_C$) [1,5]. The large valence band discontinuity and its monotonic increase with the Ge mole fraction are two of the most attractive features of the type I Si/SiGe alignment that can be used to control hole confinement in field effect transistors and hole injection and electron transport in npn heterostructure bipolar transistors [1].

The band diagram is significantly different for the second case, that of strained silicon on a relaxed SiGe substrate. This band alignment, in which the SiGe bandgap lies partially above the silicon bandgap, is defined as type II. In this case, eqn.(1.4a) must be replaced by

$$\Delta E_G = \Delta E_V - \Delta E_C \tag{1.4b}$$

The type II energy bands alignment scheme allows for the separate confinement of electrons and holes at the heterojunction, i.e. holes in the SiGe layer and electrons in the strained Si layer. This property of the type II system is used in both n-channel and p-channel FET's.

1.2.3. Carrier Transport in Silicon-Germanium Alloys

The in-plane electron and hole mobilities in SiGe are complex functions of the mechanical strain, of the Ge mole fraction Y, and of the various scattering

mechanisms in the SiGe and adjacent layers. For example, increasing the Ge mole fraction will reduce the effective mass and, consequently, enhance mobility. This trend competes with a reduction in mobility caused by alloy (up to mole fractions of 50%) and interface scattering. It was demonstrated both theoretically [10-12] and experimentally [13-16] that carrier mobilities are larger in strained SiGe and strained silicon films than in conventional silicon. Electron mobilities as large as 2700 cm^2/Vs have been obtained at room temperature in strained silicon layers grown on a SiGe substrate[1], while SiGe hole mobilities of 1300 cm^2/Vs have been measured [16]. It is noteworthy that hole mobilities in SiGe quantum layers are theoretically predicted to be larger than in pure germanium [10], indicating that mobility cannot be simply extrapolated between Si and Ge.

It must be mentioned that, despite the larger mobilities, the saturation drift velocities of electrons and holes in SiGe layers are comparable to those of silicon [14, 15]. Therefore, small geometry devices in which the velocity saturation effect is the current limiting mechanism might not benefit from the presence of SiGe to the extent suggested by the mobility data.

1.3. Silicon-Germanium Devices

By inserting a precisely controlled SiGe layer in the vertical structure of a Si bipolar or field effect transistor an additional design freedom is obtained. As a consequence, the current and voltage gain, unity gain cutoff frequency and the maximum frequency of oscillation can be optimized over wider voltage and temperature ranges, as compared to the original silicon devices. Because of the possibility of controlling

both the bandgap and the index of refraction, SiGe has also been successfully applied to heterostructure photodetectors and optical waveguides. For a recent overview of silicon-based optoelectronics, reference [17] may be consulted.

In the case of Heterostructure Bipolar Transistors (HBT's) [1-3], the interest in a SiGe base was first driven by the ability to tailor the bandgap of SiGe so that an exponential increase in the current gain β could be traded off for a reduction in the base resistance, thus simultaneously improving the gain, the maximum frequency of oscillation and the noise figure of the device. Later refinements involved grading the Ge profile along the base in order to maximize the electron velocity and, thereby, the cutoff frequency of the transistor [1,3]. The SiGe HBT is by now a mature device that has already been integrated in a commercial BiCMOS process [3,4]

Even though research interest in SiGe FET's [18] predated that in SiGe HBT's, they have yet to make a significant impact on Si technology. The conventional way of enhancing the performance of field effect transistors is to scale down the gate length. Another technique is to use a material with better transport properties as the conductive channel between source and drain. SiGe is the ideal material to boost the speed of both n and p-channel Si MOSFET's. Developments over the last decade have demonstrated that high speed FET action can be achieved with both type I and type II Si/SiGe heterostructure alignments, employing either Schottky or MOS gates [18-27]. Record breaking electron and hole mobilities have so far been the exclusive domain of type II Si/SiGe FET's [17, 21-25]. However, these devices, which require a relaxed SiGe substrate, have proved until now very difficult to integrate in conven-

tional Si technology. Furthermore, the defect density in type II Si/SiGe layers is still too high to meet VLSI specifications. For these reasons, only type I Si/SiGe devices will be discussed.

1.4. Why Si/SiGe/Si p-MOSFET's ?

First, because the performance of state of the art silicon CMOS and BiCMOS circuits is limited by the slow p-channel MOSFET, upgrading the p-FET requires urgent attention. Secondly, while undoubtedly a worthy pursuit, the implementation of n-channel devices raises more severe hurdles. Due to the negligible conduction band offset in the type I Si/SiGe system, there is minimal electron confinement to increase n-MOSFET speed. n-MOSFET's have therefore been attempted primarily in the Type II system, beset by fabrication problems.

Recently reported type I Si/SiGe/Si p-channel MOSFET's, which are relatively easy to fabricate in a VLSI process [26,27], have exhibited hole mobilities higher than in Si devices, but well below those measured in type II Schottky gate, Modulation-Doped FET's (MODFET's). Based on very recent experiments [28], which indicate a monotonic increase in hole mobility with the Ge mole fraction, it is highly probable that a significant increase in performance can only be attained if very large (in excess of 40-50%) Ge mole fractions are used in the channel. Practical implementations of large Ge mole fractions in Type I p-MOSFET's have been precluded by the necessity of complying with the Matthews-Blakeslee critical layer thickness [6], by the rectangular or trapezoidal shape [29] of the Ge profile in the channel, and by interface scattering at very abrupt Si/SiGe interfaces [1]. The latter

severely degrades mobility. The thrust of the thesis is to demonstrate, through theory and experiments, that a practical solution to these problems may be achieved by using a triangular Ge profile in the channel of the MOSFET.

1.5. Thesis Objectives and Outline

The objectives of this thesis are to demonstrate the feasibility of a VLSI compatible type I Si/SiGe/Si p-MOSFET with triangular Ge profiles and to develop electrical characterization techniques for Si/SiGe/Si MOSFET technology.

In order to meet these goals, a theory is developed in Chapter 2 to model and interpret the C-V characteristics of heterostructure MOS capacitors [30]. This model is followed up in the second part of that chapter by the proposal and experimental validation of a C-V characterization technique that extracts the parameters of the Si/SiGe heterojunction, which are critical in the design of Si/SiGe/Si p-MOSFET's [31]. The material and process information obtained from these measurements include the valence band offset and the Ge composition at the Si/SiGe interface, as well as the doping level in the Si substrate. The concept of a Si/SiGe/Si p-MOSFET with triangular Ge channel profiles [32] is proposed in Chapter 3 and its benefits in comparison with current Si/SiGe/Si p-MOSFET's are discussed based on newly developed analytical models and on two-dimensional simulation results [33,34]. A fabrication process, compatible with conventional silicon VLSI process lines, whereby SiGe and Si p-MOSFET's are integrated on the same chip, is described in Chapter 4 [35,36]. Experimental characteristics of Si and SiGe transistors implemented in this technology are also presented. Finally, in Chapter 5, conclusions are

drawn regarding the implications of this work for the short and medium term prospects of Si/SiGe IC's. Possible related topics for future research are also discussed.

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CHAPTER 2

THE HETEROSTRUCTURE MOS CAPACITOR

2.1. Introduction

A salient feature of the Si/SiGe heterostructure system† is the possibility of growing high quality oxides, comparable to those obtained on Si [1,2]. The aim of this chapter is to demonstrate - based on analytical models, numerical simulation and experimental results - that, like its silicon counterpart, the Si/SiGe heterostructure MOS capacitor is a useful tool in the understanding of the underlying physics of Si/SiGe/Si MOSFET's. It is also shown that it can become an effective characterization vehicle for Si-based heterostructure technology.

This chapter is organized as follows. First the Si/SiGe MOS capacitor structure is defined and the main assumptions in the derivation of the threshold voltages and of the charge distribution are discussed. The energy band diagram and the charge distribution in the three regimes - inversion, depletion, and accumulation - are compared with those of a conventional MOS capacitor. Analytical expressions for the threshold voltages are also derived. Their dependence on structural parameters such as the Ge mole fraction Y, the silicon cap layer thickness x_{ca} and the impurity dose in the δ-doped layer is investigated using analytical and one dimensional (1D) simulation

† For simplification purposes, the term SiGe will be used throughout the thesis to refer to a SiGe alloy with a Ge mole fraction Y, and a Si mole fraction 1-Y.

results. The capacitance-voltage (C-V) characteristics are discussed next. Finally, a technique is developed for the reverse engineering of the layer structure from high-frequency (HF) and low-frequency (LF) C-V measurements. The limitations of the technique and the sources of errors associated with the measurements are documented. Experimental validation is provided.

The analytical derivation of the threshold voltages, of the semiconductor charge, and of the semiconductor capacitance is described in detail in Appendix A. An overview of the one-dimensional numerical simulation technique, which selfconsistently solves Poisson's and Schrödinger's equations to obtain the potential and carrier distributions inside the capacitor structure, is presented in Appendix B.

2.2. Physics of Heterostructure MOS Capacitors

Consider the schematic of the p-channel heterostructure MOS capacitor shown in Fig.2.1. The structure is similar to that of a conventional silicon MOS capacitor, except for the presence of the undoped SiGe channel, of thickness x_{SiGe}, separated from the Si/SiO_2 interface by a thin undoped silicon cap layer of thickness x_{ca}. A δ-doped boron layer, of thickness x_δ, is usually inserted below the SiGe channel [3]. Separation between the SiGe film and the δ-doped film is provided by an undoped silicon buffer, of thickness x_{bu}. This separation is necessary in order to prevent the mobile holes in the SiGe film from scattering by the ionized acceptors of the δ-doped region. The primary role of the δ-doped layer is to control the threshold voltage of the SiGe channel. This sandwich of layers is grown by CVD or MBE techniques on top of a uniformly-doped, n-type silicon substrate.

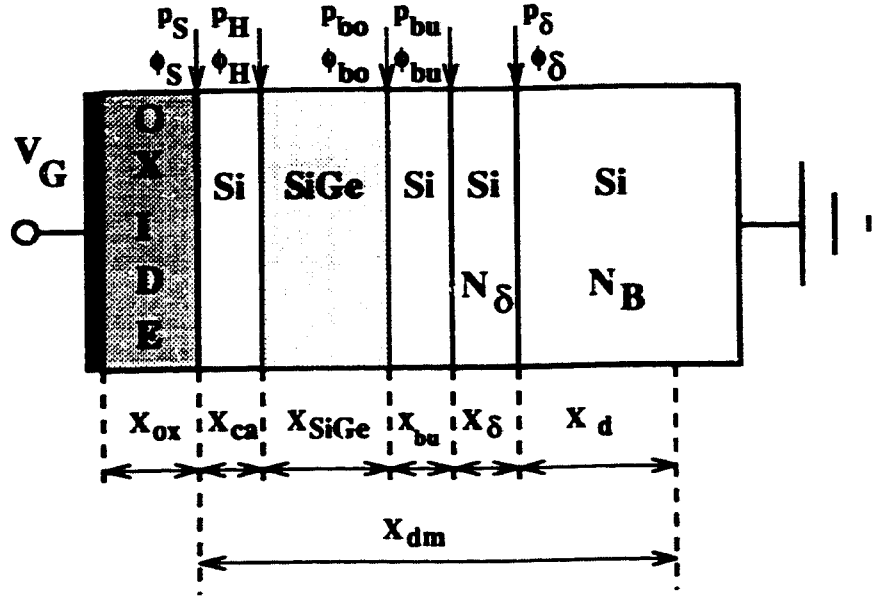


Figure 2.1 *Si/SiGe MOS capacitor structure and notation employed for potential and hole concentration at each interface.*

Basic assumptions

In order to facilitate understanding of the operation of the heterostructure MOS capacitor and to render the problem analytically tractable, the following assumptions are made

- the bandgap difference ΔE_G between Si and SiGe lies entirely in the valence band, i.e. $\Delta E_G = \Delta E_V$ [4],
- the contribution of the fixed charge in the undoped layers is negligible,
- the Ge mole fraction Y is either constant throughout the SiGe layer, or it varies linearly from Y_{bo}, at the bottom of the SiGe film, to Y_H at the top.

- the Ge profile is constrained by the assumption of positive grading i.e.

$$\delta Y(x) = Y_H - Y(x) \geq 0$$

implying that, as illustrated in Fig. 2.2, only **rectangular** ($\delta Y_{bo} = 0$), **trapezoidal** ($\delta Y_{bo} > 0$) or **triangular** ($\delta Y_{bo} = Y_H$ and $Y_{bo} = 0$) profiles are allowed.

The latter restriction is not really a limitation since all cases of practical interest are covered.

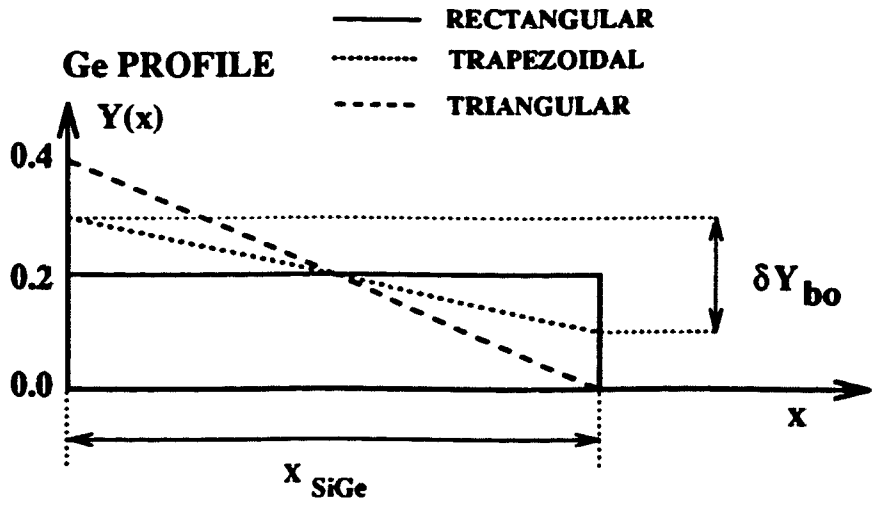


Figure 2.2 *Three types of Ge profiles considered for the Si/SiGe MOS capacitor structure.*

Because of their linear dependence on the Ge mole fraction, the valence band offset ΔE_V and the permittivity in the SiGe film ε_{SiGe}, become position dependent [4] and can be expressed as

$$\Delta E_V(x) = \Delta E_{VH} - 0.74\delta Y(x) = \Delta E_{VH} - qF_{bi}x \qquad (2.1)$$

$$\varepsilon_{SiGe}(x) = \varepsilon_{SiGeH} - 4.2\delta Y(x) \tag{2.2}$$

where $F_{bi} = \frac{0.74\delta Y_{bo}}{x_{SiGe}}$ is the built-in electric field due to Ge profile grading. The total Ge dose in the SiGe film can be expressed in cm, (Y is dimensionless), as

$$\text{Dose(Ge)} = \int_0^{x_{SiGe}} Y(x)dx = \left[Y_H - \frac{\delta Y_{bo}}{2} \right] x_{SiGe} \tag{2.3}$$

In the above equations, the values at the top heterojunction (subscript H) are considered as reference.

2.2.1. Charge Distribution and Threshold Voltages

Figure 2.1 illustrates the definitions of the potential $\phi(x)$ and of the hole concentration $p(x)$ at the substrate/δ-doped layer interface (subscript δ), at the buffer/δ-doped layer interface (subscript bu), at the bottom Si/SiGe heterojunction (subscript bo), at the top Si/SiGe heterojunction (subscript H) and at the Si/SiO_2 interface (subscript S).

The Fermi potential in the bulk corresponds to that of an n type silicon substrate with uniform ionized donor concentration N_B

$$\phi_F = -\frac{KT}{q} \ln\left[\frac{N_B}{n_{iSi}} \right] \tag{2.4}$$

By accounting for the position-dependent bandgap, the concentration of mobile holes $p(x)$ is expressed as

$$p(x) = N_B \exp\left[\frac{2q\phi_F + \Delta E_G(x) - q\phi(x)}{KT} - \ln\left[\frac{N_{VSi}}{N_{VSiGe}} \right] \right] \tag{2.5}$$

Because of the negligible conduction band offset, the electron concentration is identical to that in a silicon MOS capacitor

$$n(x) = N_B \exp\left[\frac{\phi(x)}{\phi_T}\right] \tag{2.6}$$

Similarly, the gate voltage V_G, and the total semiconductor charge Q_T, can be described in terms of the surface potential ϕ_S [5]

$$V_G = V_{FB} + \phi_S + V_{ox} = V_{FB} + \phi_S - \frac{\sqrt{2q\varepsilon_{Si}N_B\phi_T f(\phi_S)}}{C_{ox}} \tag{2.7}$$

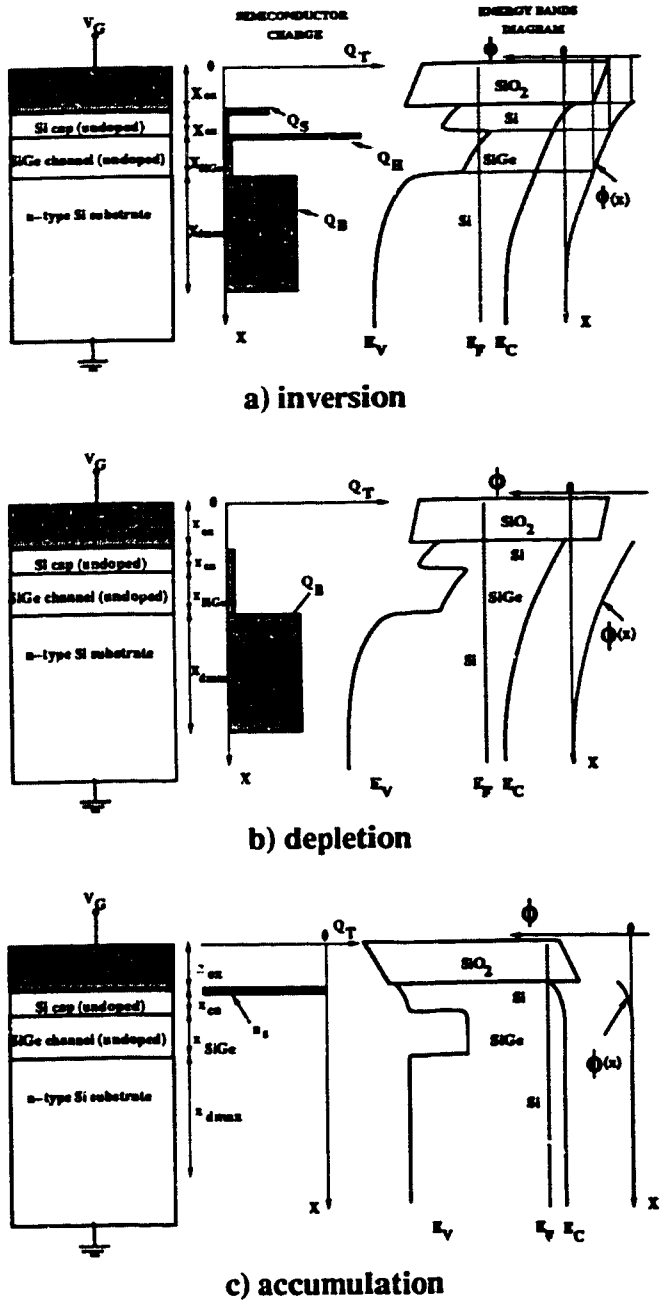
$$Q_T = \sqrt{2q\varepsilon_{Si}N_B\phi_T f(\phi_S)} \tag{2.8}$$

where $C_{ox} = \varepsilon_{ox}/x_{ox}$ is the gate oxide capacitance per unit area, x_{ox} is the gate oxide thickness, V_{FB} is the flatband voltage which includes the contribution of the work-function difference ϕ_{MS} between the gate and the silicon substrate and that of the fixed charge Q_f at the Si–SiO_2 interface. $f(\phi_S)$ contains the heterojunction-specific information and its expression is derived in Appendix A.

Figure 2.3 shows the schematic energy bands diagram and the corresponding charge distribution in the **a)** inversion, **b)** depletion and **c)** accumulation regimes. For the sake of simplicity, the δ-doped layer is not included.

The distinctive feature of the charge distribution is the presence of mobile holes in strong inversion at both the Si/SiO_2 interface p_S, and at the top Si/SiGe heterojunction p_H. Since the type I Si/SiGe heterojunction has a negligible conduction band offset, the accumulation and depletion charges are similar to those of a MOS capacitor fabricated in silicon. Therefore, the focus next is on the investigation of the

threshold voltages and of the inversion charge.



a) inversion

b) depletion

c) accumulation

Figure 2.3 *Schematic energy bands diagrams and charge distribution in a) inversion, b) depletion and c) accumulation in a Si/SiGe MOS capacitor.*

The onset of strong inversion at the top Si/SiGe interface corresponds to the gate voltage at which the concentration of minority holes at the top Si/SiGe heterojunction is equal to the substrate doping concentration N_B [6]

$$p_H\Big|_{V_G = V_{TH}} = N_B \exp\left[\frac{2q\phi_F + \Delta E_{VH} - q\phi_H}{KT} - \ln\left[\frac{N_{VSi}}{N_{VSiGe}}\right]\right] = N_B \qquad (2.9)$$

This leads to the following condition for the threshold potential ϕ_{TH} at the top hetero-junction

$$\phi_{TH} = \phi_H\Big|_{V_G = V_{TH}} = 2\phi_F + \frac{\Delta E_{VH}}{q} - \phi_T \ln\left[\frac{N_{VSi}}{N_{VSiGe}}\right] \qquad (2.10)$$

where N_{VSi} and N_{VSiGe} are the densities of states in the valence band for silicon and for SiGe, respectively, and ϕ_T is the thermal voltage. The gate voltage which causes strong inversion at the top Si/SiGe interface is denoted by V_{TH}, the threshold voltage of the SiGe channel.

Similarly, strong inversion at the Si/SiO_2 interface is defined as

$$p_S\Big|_{V_G = V_{TS}} = N_B \exp\left[\frac{2\phi_F - \phi_S}{\phi_T}\right] = N_B \qquad (2.11)$$

and the corresponding threshold surface potential ϕ_{TS} must satisfy the condition

$$\phi_{TS} = \phi_S\Big|_{V_G = V_{TS}} = 2\phi_F \qquad (2.12)$$

The gate voltage which causes strong inversion at the surface of the silicon cap layer is denoted by V_{TS}, the threshold voltage of the surface channel [6].

A simplified version of $f(\phi_S)$ is plugged into eqn. (2.7) to derive expressions for the threshold voltages V_{TH} and V_{TS}. The fixed charge in the depletion layer and the mobile hole charge in the SiGe film are accounted for. The hole charge in the silicon cap is neglected since, for a properly designed structure, $V_{TH}>V_{TS}$, indicating that strong inversion occurs first at the top Si/SiGe heterointerface. As detailed in Appendix A, for $V_{TS} \leq V_G$, the following relation holds

$$V_G = V_{FB} + \phi_H - Q_B\left[\frac{x_{ca}}{\varepsilon_{Si}} + \frac{x_{ox}}{\varepsilon_{ox}}\right]\sqrt{1+H(\phi_H)} \qquad (2.13)$$

where $Q_B = q(N_B x_d - N_\delta x_\delta)$ is the fixed charge in the depletion layer, accounting for the contribution of the δ-doped layer and of the uniformly-doped substrate. $H(\phi_H)$ represents the contribution of holes in the SiGe layer to the potential drop across the silicon cap.

The expression for V_{TH} is derived directly from eqn. (2.13) as

$$V_{TH} = V_G\Big|_{\phi_H=\phi_{TH}} = V_{FB} + \phi_{TH} - Q_{Bmax}\left[\frac{x_{ca}}{\varepsilon_{Si}} + \frac{x_{ox}}{\varepsilon_{ox}}\right]\sqrt{1+H(\phi_{TH})} \qquad (2.14)$$

In eqn.(2.14), x_d and Q_B assume their maximum values x_{dmax} and Q_{Bmax}, respectively, corresponding to the onset of strong inversion.

Eqn. (2.14) can be simplified by noting that, at the onset of strong inversion at the top heterointerface, the hole contribution is very small. Therefore, the $H(\phi_{TH})$ term can be neglected. Simulation revealed that, under typical conditions, this results in an error of at most 70 mV. However, it should be emphasized that the impact of Ge mole fraction grading (through F_{bi}) on the threshold voltage is also contained in this

term. Grading affects the subthreshold slope and the MOSFET small signal parameters [7], as will be explained in Chapter 3, but hardly at all the threshold voltage.

The threshold voltage V_{TS}, is obtained from eqns.(2.7), using a simple formula for $f(\phi_S)$, valid in strong inversion

$$V_{TS} = V_G\Big|_{\phi_S = \phi_{TS}} = V_{FB} + \phi_{TS} - \frac{Q_{Bmax}}{C_{ox}}\sqrt{1 + H(\phi_H)} \tag{2.15}$$

In this case, the contribution of the holes in the SiGe layer is important. $H(\phi_H)$ is much larger than 1 and eqn. (2.15) can be rewritten as

$$V_{TS} = V_{FB} + \phi_{TS} - \frac{\sqrt{2q\varepsilon_{SiGe_H} N_B \phi_T}}{C_{ox}\sqrt{1 + \dfrac{\varepsilon_{SiGe_{bo}} F_{bi}}{Q_B}}} \exp\left[\frac{\phi_{TH} - \phi_H}{2\phi_T}\right] \tag{2.16}$$

The potential at the top heterointerface ϕ_H, needed to calculate V_{TS}, can be obtained by iteration [6]. However, it is quite reasonable to assume that, at $V_G = V_{TS}$, the Fermi level in the buried channel is pinned at the valence band. Therefore,

$$\phi_H = \phi_{TH} - \phi_T \ln\left[\frac{N_{VSiGe}}{N_B}\right]$$

is a good approximation.

In order to verify the validity of the analytical model, the impact of the structural parameters Y_H, x_{ca}, $N_\delta x_\delta$, x_{ox} and N_B on V_{TH} and V_{TS}, as obtained from eqns. (2.14) and (2.16), was investigated and compared with simulation. The results are shown in Figs. 2.4 through 2.8. The agreement between the analytical model and the numerical simulation results is excellent for V_{TH} and good for V_{TS}. A better match

for V_{TS} can be obtained by replacing the exponential in eqn. (2.16) and in $H(\phi_H)$ with the Fermi-Dirac function of order 3/2. Fermi-Dirac statistics are thus accounted for, and the analytical form can still be retained. Conclusions, useful in MOSFET design, are summarized below.

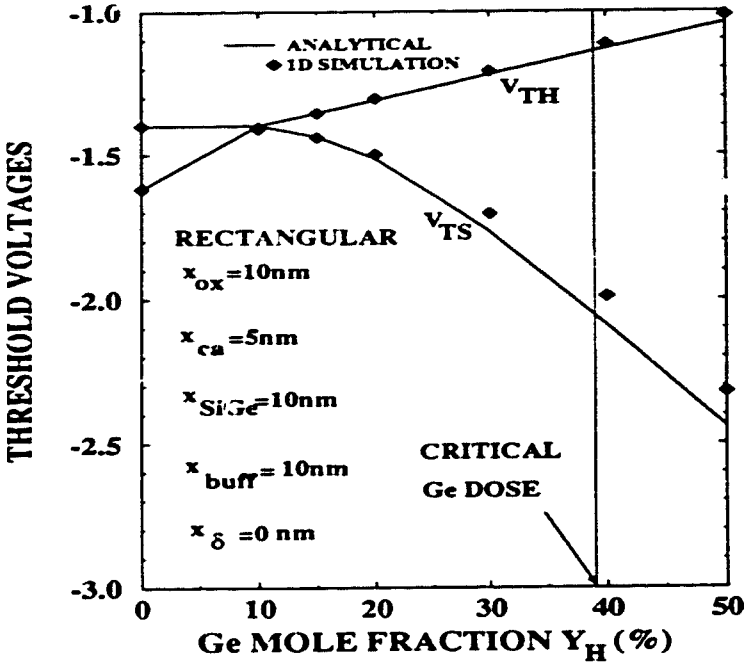


Figure 2.4 *Numerically and analytically computed threshold voltages in a Si/SiGe MOS capacitor as functions of Ge mole fraction* Y_H.

a) Ge mole fraction Y_H

The Ge mole fraction at the top of the channel affects both V_{TH} and V_{TS}. This dependence is linear for V_{TH}, primarily due to the ϕ_{TH} term, and superlinear for V_{TS}.

b) Ge mole fraction grading δY_{bo}

For a fixed Ge mole fraction at the top of the channel, changing the amount of grading δY_{bo} has little bearing on V_{TH} and V_{TS}.

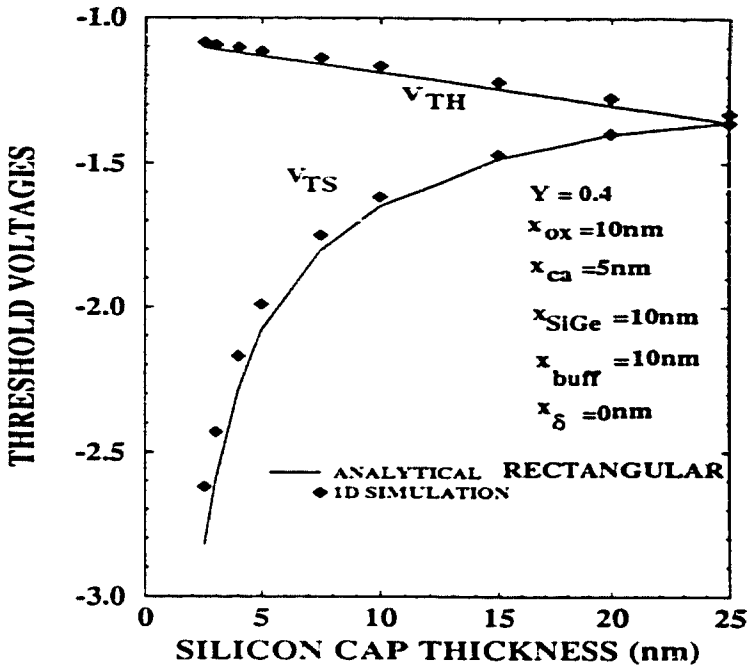


Figure 2.5 *Numerically and analytically computed threshold voltages in a Si/SiGe MOS capacitor as functions of the silicon cap thickness* x_{ca}.

c) Silicon cap thickness x_{ca}

The thickness of the silicon cap layer determines the values of both threshold voltages. It changes V_{TH} linearly and V_{TS} exponentially, via ϕ_H.

d) Dose of the δ-doped layer $N_\delta x_\delta$

The δ-doped layer dose can be employed to independently control the SiGe channel threshold V_{TH} without affecting the value of the surface channel threshold V_{TS}. For a wide range of values, V_{TH} is linearly dependent on the dose. However, there is a critical dose beyond which control over V_{TH} is lost, because the depletion region fails to extend below the δ-doped layer. In this case, inversion occurs first in the low mobility, δ-doped layer, which is undesirable for MOSFET's.

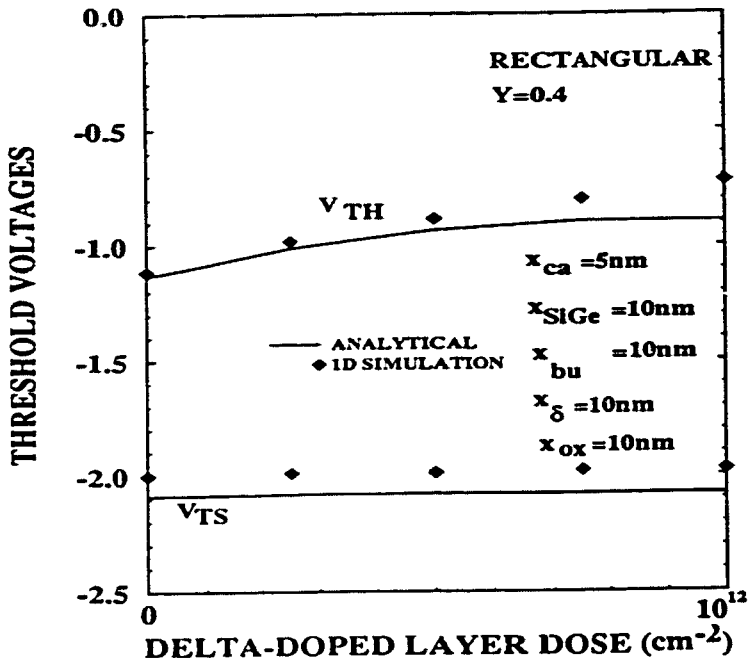


Figure 2.6 *Numerically and analytically computed threshold voltages in a Si/SiGe MOS capacitor as functions of the δ-doped layer dose* $N_\delta x_\delta$.

Likewise, because the assumption that the δ-doped layer is fully depleted of holes breaks down, the analytical model fails to accurately predict the buried channel threshold voltage for large values of the dose.

e) Oxide thickness x_{ox}

Both V_{TH} and V_{TS} depend linearly on x_{ox}. When x_{ox} decreases (as required by the constant field scaling law) the gate voltage window between V_{TS} and V_{TH} is reduced.

f) Substrate doping N_B

The magnitudes of both V_{TH} and V_{TS} increase with N_B. When N_B is increased (as required by the constant field scaling law), the degradation of the gate voltage window between V_{TS} and V_{TH} is not as severe as in the case of x_{ox}.

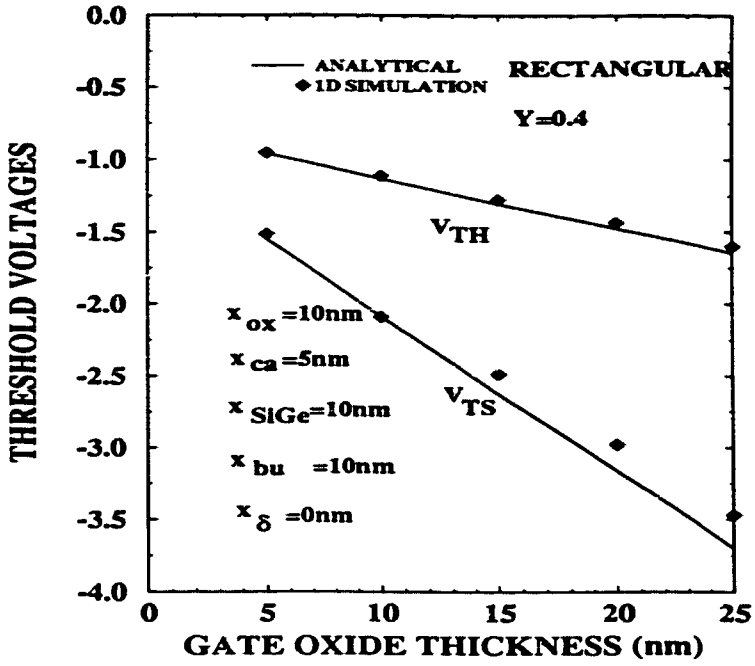


Figure 2.7 *Numerically and analytically computed threshold voltages in a Si/SiGe MOS capacitor as functions of the gate oxide thickness* x_{ox}.

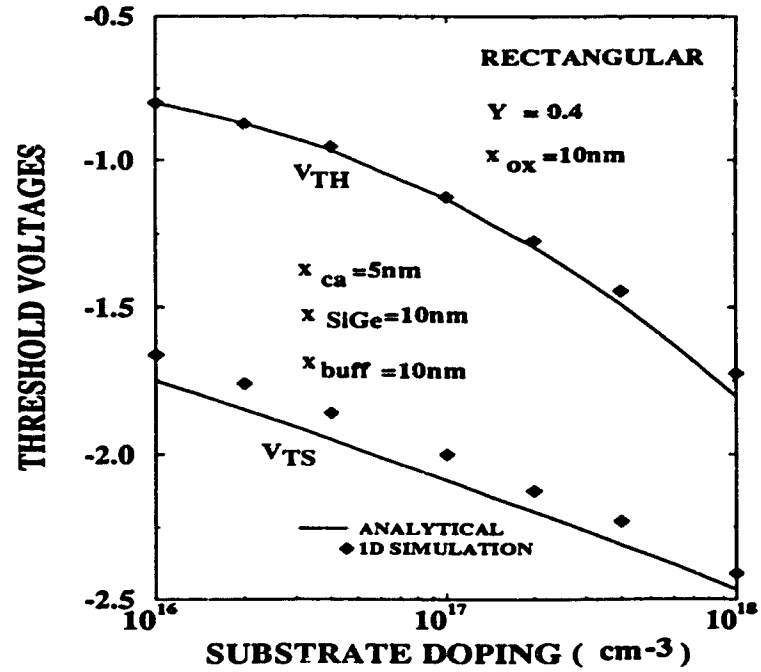


Figure 2.8 *Numerically and analytically computed threshold voltages in a Si/SiGe MOS capacitor as functions of the substrate doping* N_B.

2.2.2. Capacitance-Voltage Characteristics

Numerically simulated $C_{LF}(V_G)$ characteristics are compared in Fig.2.9 for Si and Si/SiGe MOS capacitors. The depletion and accumulation regions of the C_{LF}–V_G characteristics are nearly identical to those of Si MOS capacitors, allowing for the simple extraction of the flat-band voltage. The differences become apparent only in the inversion regime of the C_{LF}–V_G characteristics and are discussed below.

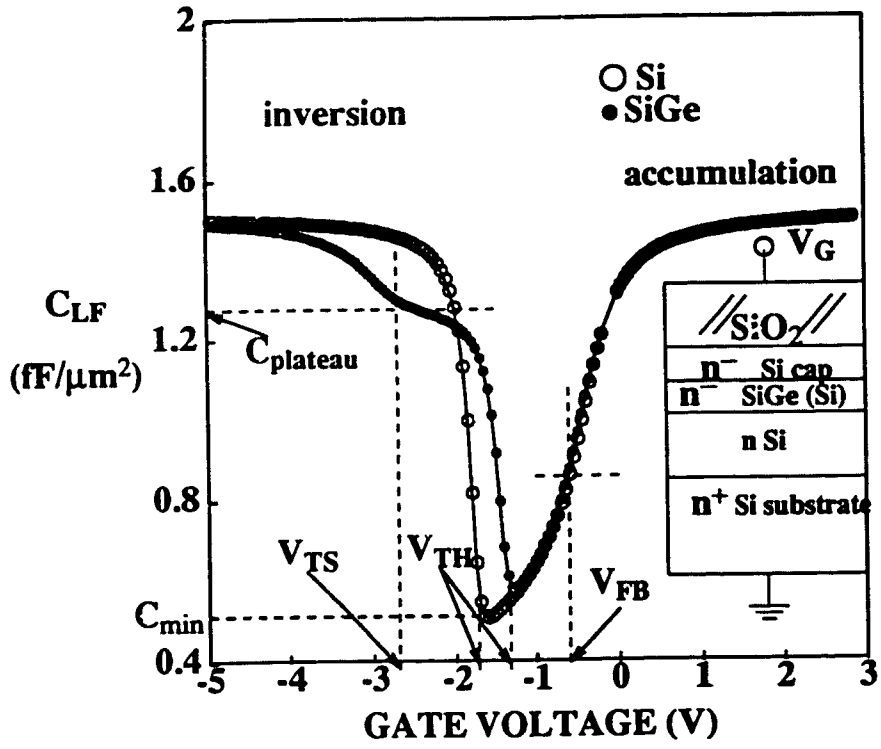


Figure 2.9 *Typical* C_{LF}–V_G *characteristics of Si and Si/SiGe MOS capacitors indicating threshold voltages,* $C_{plateau}$ *and* C_{min}. *The layer structure is shown in the inset. The Ge mole fraction Y is graded from 0 to 0.5 over 15 nm,* $N_B = 5\times10^{16}$ *cm*$^{-3}$, $x_{ca} = 10$nm *and* $x_{ox} = 20$nm.

(i) The minimum capacitance C_{min}

$$\frac{1}{C_{min}} = \frac{x_{ox}}{\varepsilon_{ox}} + \frac{x_{ca}}{\varepsilon_{Si}} + \frac{x_{SiGe}}{\varepsilon_{SiGe}} + \frac{x_{bu} + x_{\delta} + x_{dmax}}{\varepsilon_{Si}} \qquad (2.17)$$

is larger for the heterostructure capacitor and increases with the Ge mole fraction. This is caused by the smaller depletion depth in the heterostructure than in the silicon MOS capacitor.

(ii) Due to the change in threshold voltage, the inversion region of the C_{LF}-V_G characteristics of the heterostructure capacitor is shifted towards more positive gate voltages.

(iii) The C_{LF}–V_G characteristics of the heterostructure capacitor show a plateau of slow-varying capacitance. There is no capacitance plateau in the case of the Si structure.

The value of the plateau capacitance depends on the thickness of the silicon cap layer x_{ca}. Its width is denoted as the gate voltage window $\Delta V_T = V_{TH} - V_{TS}$. The latter is determined by the valence band offset ΔE_{VH} at the top Si/SiGe interface, by the thickness of the silicon cap layer x_{ca}, and by the dose of the δ-doped layer. Ideally, the plateau capacitance should be equal to

$$C_{plateau} = \frac{\varepsilon_{ox}\varepsilon_{Si}}{\varepsilon_{ox}x_{ca} + \varepsilon_{Si}x_{ox}} = \frac{C_{ox}}{(1+\alpha)} \qquad (2.18)$$

where $\alpha = \frac{x_{ca}}{3x_{ox}}$. In reality, in the plateau region, the capacitance varies slowly. As shown in Appendix A, in strong inversion, the dependence of the semiconductor capacitance C_S on the surface potential is approximated by

$$C_S = \sqrt{\frac{q\varepsilon_{Si}N_B}{2\phi_T}}\left[e^{\frac{2\phi_F-\phi_S}{\phi_T}} + \frac{\varepsilon_{Si}}{\varepsilon_{SiGe_H}}\frac{1}{1+\frac{F_{bi}}{F_{bo}}}e^{\frac{\phi_{TH}-\phi_H}{\phi_T}}\right]^{1/2} \quad (2.19)$$

The second term is absent in the case of a Si MOS capacitor.

In fact, the C_{LF}–V_G characteristics cannot directly provide very accurate values for V_{TH}, V_{TS} and x_{ca}, because the transitions between the various regions of the inversion regime tend to be smoothed out at room temperature. To precisely identify V_{TH} and V_{TS}, the low frequency apparent doping characteristics N_{appLF}–V_G must be examined.

Since the response of the inversion charge is very slow, the high frequency C_{HF}–V_G characteristics of Si/SiGe capacitors are identical in shape to those of their silicon counterparts. The part corresponding to the inversion regime is flat and equal to C_{min}.

2.3. The Si/SiGe MOS Capacitor as a Process and Device Characterization Vehicle

The detailed structure and composition of the Si/SiGe layers is well controlled during the MBE or CVD growth, and can be verified by destructive characterization techniques such as Auger Electron Spectroscopy (AES). It is, however, extremely important for process control and device modeling, that the cap layer thickness and the Ge mole fraction be extracted by non-destructive electrical probing on the actual fabricated devices. Such a reverse engineering technique, based on high frequency and low frequency capacitance-voltage measurements, is proposed next [8].

The similarities between the C-V characteristics of heterostructure and silicon MOS capacitors, discussed in the previous section, make it apparent that the oxide thickness x_{ox}, substrate doping N_B, maximum depletion depth $x_{dm} = x_{ca} + x_{SiGe} + x_{bu} + x_{\delta} + x_{dmax}$, and the flat-band voltage V_{FB}, can be extracted directly from the experimental high frequency C_{HF}–V_G curves according to techniques established for silicon MOS capacitors.

In addition to the data provided by conventional MOS capacitor measurements, the features of the C_{LF}–V_G characteristics of the heterostructure capacitor can be used to extract accurate material-related information for the heterostructure, most importantly, the valence band offset ΔE_{VH}.

To achieve the latter goal, one needs to **a)** determine the cap layer thickness and the threshold voltages and **b)** to quantify the relation between ΔE_{VH} on one side and V_{TH}, V_{TS} and x_{ca}, on the other.

To avoid complications caused by the extraction of additional structural parameters, the MOS capacitor investigated in the remainder of this chapter has a rectangular Ge profile and no δ-doped layer.

2.3.1. Apparent Doping Profiles and Extraction of the Silicon Cap Thickness

From the calculated C_{LF}–V_G characteristics, the depletion depth x_{dLF},

$$x_{dLF}(V_G) = \varepsilon_{Si}\left[\frac{1}{C_{LF}(V_G)} - \frac{1}{C_{ox}}\right] \qquad (2.20)$$

and the apparent doping N_{appLF},

$$\frac{1}{N_{appLF}(V_G)} = \frac{q\varepsilon_{Si}}{2} \frac{\partial\left[\frac{1}{C_{LF}^2(V_G)}\right]}{\partial V_G} \tag{2.21}$$

are obtained as functions of the applied gate voltage. The term "apparent doping" refers to the contributions of both fixed and mobile charges. Further, the computed C_{LF}–V_G and N_{appLF}–V_G profiles are correlated with the voltage dependence of the peak hole concentrations at the top heterojunction p_H and at the Si/SiO_2 interface p_S.

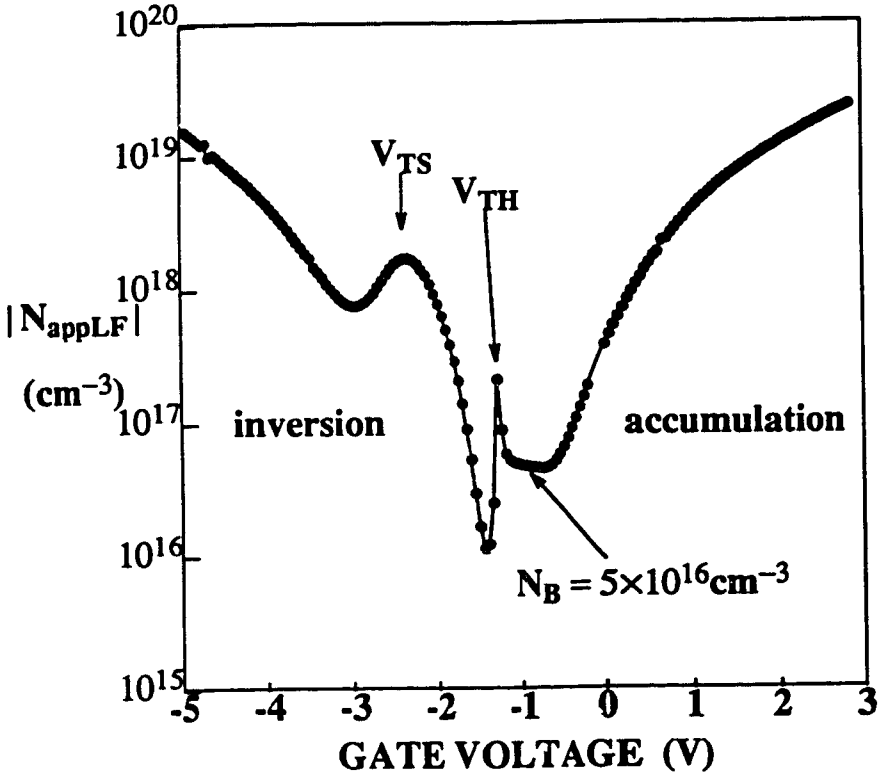


Figure 2.10 *LF apparent doping vs. gate voltage characteristics of a Si/SiGe MOS capacitor determined from the simulated* C_{LF}–V_G *characteristics of Fig.2.9.*

If the high frequency capacitance voltage characteristics are employed in eqns. (2.20) and (2.21), then the corresponding high frequency depletion depth and apparent doping, x_{dHF} and N_{appHF}, respectively, are obtained.

Apparent doping characteristics for the structure in Fig. 2.9 are plotted in absolute values in Fig. 2.10. They exhibit two regions in which the apparent doping is high and dominated by the mobile charge; one for large positive bias corresponding to accumulation of electrons and another, for large negative bias, associated with strong inversion. Between them lie the regions of interest to the characterization method; namely a plateau corresponding to the depletion regime whose value gives the substrate doping, ($N_B = N_D - N_A$) and sharp transitions with local maxima related to the thresholds. The onset of strong inversion at the top heterojunction is marked by a change of sign and an abrupt transition on the N_{appLF}–V_G characteristics. Inversion at the Si/SiO_2 interface is signaled by a local maximum of the apparent doping. This local maximum is the distinctive footprint of SiGe structures and gives the value of V_{TS}.

The thickness of the cap layer can be extracted from the apparent doping versus depth profile N_{appLF}–x_{dLF}, as shown in Fig. 2.13. This curve is obtained by combining the x_{dLF}–V_G and N_{appLF}–V_G characteristics from eqns. (2.20) and (2.21), respectively. There are two apparent doping values, of opposite sign, for each position x_{dLF}, one corresponding to the inversion- and one to the accumulation/depletion regime of the C_{LF}–V_G characteristics. The apparent doping obtained from the inversion region exhibits three peaks, corresponding (from the left to right) to a) the accu-

mulation of mobile holes at the Si/SiO_2, **b)** accumulation of holes at the top Si/SiGe heterojunction and **c)** to the maximum depletion depth, where the change of sign in the apparent doping occurs. The thickness of the silicon cap layer can be directly extracted from the position of the second peak.

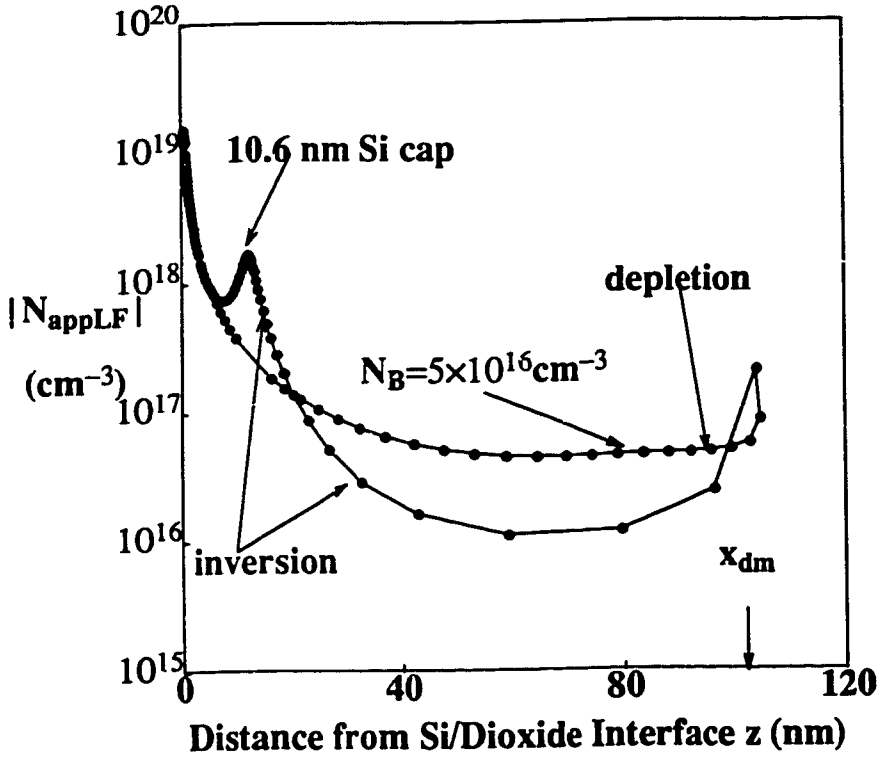


Figure 2.11 *LF apparent doping vs. depth profiles in a Si/SiGe MOS capacitor determined from the simulated* C_{LF}–V_G *characteristics of Fig 2.9.*

2.3.2. Calculation of the Valence Band Offset

By subtracting eqn. (2.15) from eqn. (2.14) (neglecting the δ-doped region dose and the built-in field) and rearranging, a system of two nonlinear equations (2.22) and (2.23), with ΔE_{VH} and ϕ_H as unknowns, is obtained

$$\Delta E_{VH} = \phi_H - 2\phi_F + \phi_T \ln\left[\frac{\left[1+C_{ox}\left(\frac{x_{ca}}{\varepsilon_{Si}}+\frac{C_{ox}(\Delta V_T+\Delta E_{VH})}{qN_B x_{dmax}}\right)\right]^2 - 1}{hfo}\right] \quad (2.22)$$

$$\phi_H = \phi_{TH} - \phi_T \ln\left[\frac{\left[\frac{\varepsilon_{Si}(\phi_H - 2\phi_F)}{qN_B x_{dmax} x_{ca}}\right]^2 - 1}{hfo}\right] \quad (2.23)$$

where

$$hfo = \frac{2q\varepsilon_{SiGe_H} N_B \phi_T}{Q_B^2}$$

One can calculate the valence band offset by iterating eqns. (2.22) and (2.23) until a solution is found. The valence band offset determined in this manner refers to the properties of the SiGe region in the vicinity of the top Si/SiGe interface. If the SiGe layer is graded, the measured band offset reflects the Ge content at the interface and not to the average Ge content in the channel [7].

2.3.3. Sources of Error Affecting the Valence Band Offset

Errors in the determination of the valence band offset may be attributed to **a)** equipment limitations, **b)** interface and/or bulk traps and **c)** model limitations.

a) Equipment limitations

The sensitivity of the measured valence band offset to inaccuracies in the values of the structural parameters was simulated. It was found that errors in C_{ox}, x_{ca}, x_{dmax} and N_B affect ΔE_{VH} linearly. Of these, x_{ca} requires corrections to account for quantum effects. Simulations using two-dimensional (2D) hole gas statistics indicate that the hole charge centroid is located about 2 nm away from the top Si/SiGe heteroin-

terface. This offset has to be subtracted from the experimentally extracted value of x_{ca}.

It should also be underlined that x_{dmax} cannot be extracted directly, but indirectly from the measured values of x_{dm} and x_{ca}. This is not an additional source of errors because the combined thickness of the SiGe, buffer and δ-doped layers, $x_{SiGe} + x_{bu} + x_{\delta}$, remains unchanged during device processing and it is usually precisely known from the initial growth. At least a part of the initial silicon cap thickness is consumed during subsequent processing steps. It is thus important that the final cap layer thickness be determined from measurements performed at the end of the fabrication process.

b) Interface and bulk traps

According to eqns. (2.14) and (2.15), both V_{TH} and V_{TS} depend on the flat-band voltage V_{FB}. However, because the effect of V_{FB} cancels out in ΔV_T, the fixed surface charge Q_f and the metal-semiconductor work function difference ϕ_{MS}, do not affect the value of the measured valence band offset. The uncertainty associated with the value of ϕ_{MS} is thus eliminated.

Even a small interface trapped charge concentration, D_{it}, (of the order of 10^{11} $cm^{-2}eV^{-1}$) changes the shape of the low frequency apparent doping profile $N_{appLF}-x_{dLF}$, in the depletion regime, raising its value and reducing the maximum depletion depth. In order to eliminate any inaccuracies in ΔE_{VH} caused by incorrect maximum depletion depth and substrate doping values, both x_{dm} and N_B must be determined from the high frequency apparent doping profile $N_{appHF}-x_{dHF}$, since traps

do not respond to high frequency signals.

In strong inversion, the impact of the interface traps on the $N_{appLF}-x_{dLF}$ profile is eliminated by the large concentration of holes piling up at the Si/SiO_2 and Si/SiGe interfaces. The cap layer thickness, given by the position of the hole charge centroid should therefore be insensitive even to a relatively high trap density.

The interface trapped charge distribution, $D_{it}(E)$, located between the positions of the Fermi level at the Si/SiO_2 interface corresponding to V_{TH} and V_{TS}, respectively, also alters the measured gate voltage window ΔV_T. Simulation results indicate that a uniformly distributed interface trap density of $2\times10^{11}cm^{-2}eV^{-1}$ causes errors of 25 mV in the gate voltage window ΔV_T and of 0.5 nm in the cap layer thickness. It may be safely concluded that, by simultaneously using experimental low frequency and high frequency apparent doping profiles, the error caused by the interface trapped charge density on the extracted valence band offset can be minimized.

Errors in ΔE_{VH} can also be caused by bulk traps in SiGe [9] if the trap concentration is larger than one fifth of the active doping. Their presence is signaled by a kink in the depletion region of the $C_{LF}-V_G$ characteristics which in turn causes an easily identifiable local peak on the $N_{appLF}-x_{dLF}$ profile.

c) Model limitations

Due to the lack of reliable experimental data for the valence band density of states in SiGe, the densities of states in Si and SiGe were tacitly assumed to be identical in the derivation presented in the preceding section. Therefore, the analytical model actually gives an "apparent" valence band offset

$$\Delta E_{V_{app}} = \Delta E_{V_H} - kT \ln\left[\frac{N_{VSi}}{N_{VSiGe}}\right] \tag{2.24}$$

By neglecting the contribution of the second term in eqn. (2.24) the error will not be larger than +/- 25 meV at room temperature.

For Ge mole fractions smaller than 30%, the hole charge at the top Si/SiGe heterojunction is screened by the charge at the Si/SiO_2 interface and neither the cap layer thickness nor the surface conduction threshold V_{TS} can be precisely identified at room temperature. To overcome this problem the sample must be cooled. At 77 K, even samples with 15% Ge clearly exhibit the hole charge accumulation at the top Si/SiGe interface.

Finally, but importantly, eqns. (2.14) and (2.15) are based on Boltzmann statistics. ΔV_T, through V_{TS}, may be therefore underestimated by up to 50 mV. The error can be eliminated by using Fermi-Dirac statistics.

2.3.4. Proposed Characterization Technique

Based on the discussion above, the following steps can be used to characterize the Si/SiGe layers

a) The oxide capacitance, flatband voltage, maximum depletion depth and the effective substrate doping are extracted from experimental the $C_{HF}-V_G$ characteristics and the $N_{appHF}-x_{dHF}$ profiles, respectively, as for a Si MOS capacitor. Interface trapped charge density and bulk traps, which do not respond to the high frequency signal, will thus not influence the extracted values of the sub-

strate doping and maximum depletion depth.

b) Eqns. (2.20) and (2.21) are then applied to the experimental $C_{LF}-V_G$ characteristics to determine the $N_{appLF}-V_G$ characteristics and the $N_{appLF}-x_{dLF}$ profile. From the inspection of the latter, accurate values of the threshold voltages V_{TH}, V_{TS} and of the cap layer thickness x_{ca}, are obtained in the manner outlined in the preceding section.

c) The data obtained in steps a) and b) are fed into eqns. (2.22) and (2.23) to determine the valence band offset.

d) D_{it} is estimated from the difference between the experimental $C_{LF}-V_G$ and $C_{HF}-V_G$ characteristics [10] and by matching the simulated and measured low frequency apparent doping profiles.

e) Q_f is extracted from the difference between the measured and calculated flatband voltage, after the contribution of the interface trapped charge on the flatband voltage has been removed.

As in the case of Si MOS capacitors, the accuracy of the interface trapped charge density determined in step d) is limited to the midgap region.

2.3.5. Experimental Results

For experimental confirmation, Si/SiGe wafers were grown by MBE with the following layer structure n^+ substrate doped $2\times10^{19}cm^{-3}$, n-type silicon epitaxial layer doped $2\times10^{17}cm^{-3}$ and 0.3 μm thick, n-type silicon buffer doped $5\times10^{16}cm^{-3}$ and 200 nm thick, undoped SiGe layer 15 nm thick and undoped silicon cap layer 10

nm thick. The Ge mole fraction was graded from 0% (bottom) to 50% (top). A low thermal-budget process was employed to create the gate oxide 1 min. RTO at 850 °C, followed by a 3 min. LPCVD (139 mTor, 12% O_2, 6.7% SiH_4) at 410 °C and followed by a 1 min. RTO at 850 °C. Capacitors with areas varying from 6.25×10^{-6} to 1.52×10^{-2} cm^2 were defined by Al deposition and wet-etch patterning. Al was also sputtered on the back side to provide a large-area ohmic contact. A post-metallization anneal was performed in forming gas at 420 °C for a duration of 20 minutes.

The doping profile was independently confirmed by spreading resistance measurements. Auger electron spectroscopy was used to verify the Ge profile. The depth resolution was 5 nm, sufficient to confirm the thickness of the SiGe film and its graded profile (approximately 20 nm), but not accurate enough to determine the thickness of the cap layer and the precise Ge concentration at the top Si/SiGe interface. The Ge profile linearly increases from 0% Ge for about 12 nm, saturates at just above 40% Ge and then drops steeply back to 0%. If one extrapolates the slope of Ge grading in the linear region, a value close to 50% Ge is found at the top Si/SiGe interface.

The C_{LF}–V_G and C_{HF}–V_G characteristics were measured using Hewlett Packard's 4280A 1MHz C Meter and the 4140B pA Meter and are plotted in Fig. 2.12. Corrections were made for parasitic capacitances and leakage currents, but no attempt was made to smooth out the experimental data by interpolation. First, the oxide thickness, x_{ox} = 22.3 nm, was determined from the C_{HF}–V_G characteristics

presented in Fig. 2.12 and the substrate doping $N_B = 5\times10^{16}cm^{-3}$ was obtained from the associated N_{appHF}–x_{dHF} profile, shown in Fig. 2.13. Then, from the inversion region of the experimental C_{LF}–V_G characteristics, plotted in Fig. 2.14, the N_{appLF}–V_G and N_{appLF}–x_{dLF} profiles were calculated and are presented in Figs. 2.15 and 2.16, respectively.

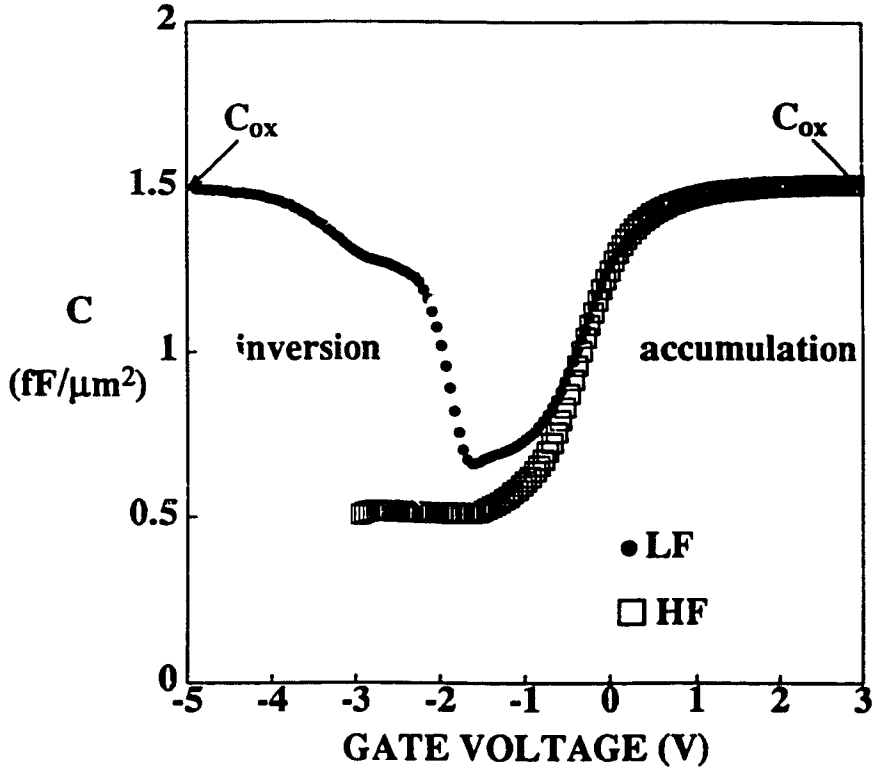


Figure 2.12 *Typical experimental* C_{LF}–V_G *and* C_{HF}–V_G *characteristics of triangular (0-47% Ge) Si/SiGe MOS capacitors. The capacitor layer structure is similar to that shown in the inset of Fig.2.9.*

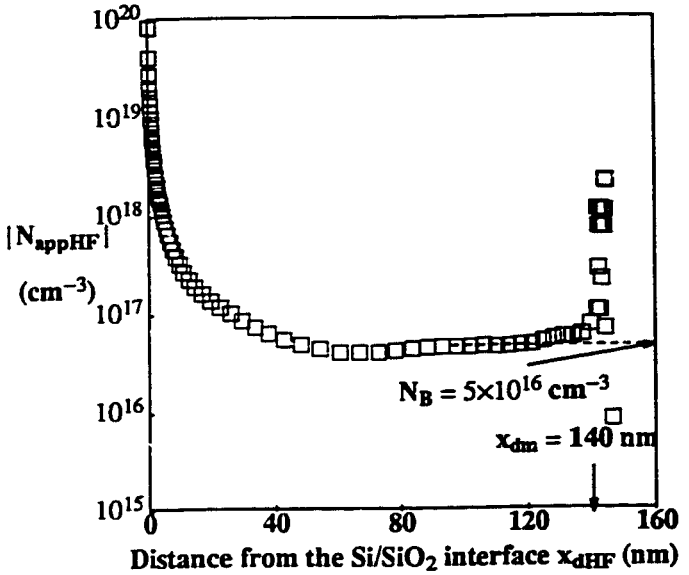


Figure 2.13 *Experimental apparent doping vs. depth profiles in Si/SiGe MOS capacitors obtained from the measured* C_{HF}–V_G *characteristics of Fig.2.12.*

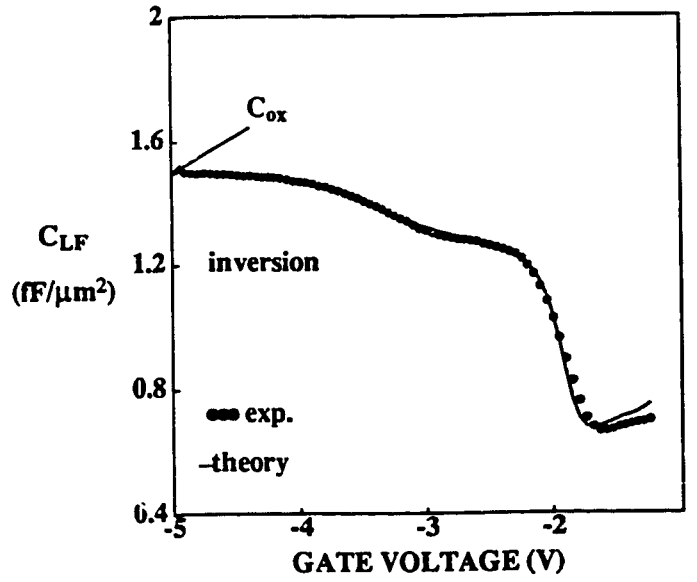


Figure 2.14 *Comparison of measured and simulated* C_{LF}–V_G *characteristics of Si/SiGe MOS capacitors based on the extracted structural and material data.*

The two thresholds, V_{TH} = -1.65 V and V_{TS} = -2.8 V, were identified from the experimental trace in Fig. 2.15 and the cap layer thickness, t_{ca} = 10.6 nm, was deduced from the apparent doping versus depth profile, as shown in Fig. 2.16. Even though it is not evident from the experimental characteristics in Fig. 2.15, V_{TH} can be easily identified because it corresponds to a change of sign in the apparent doping.

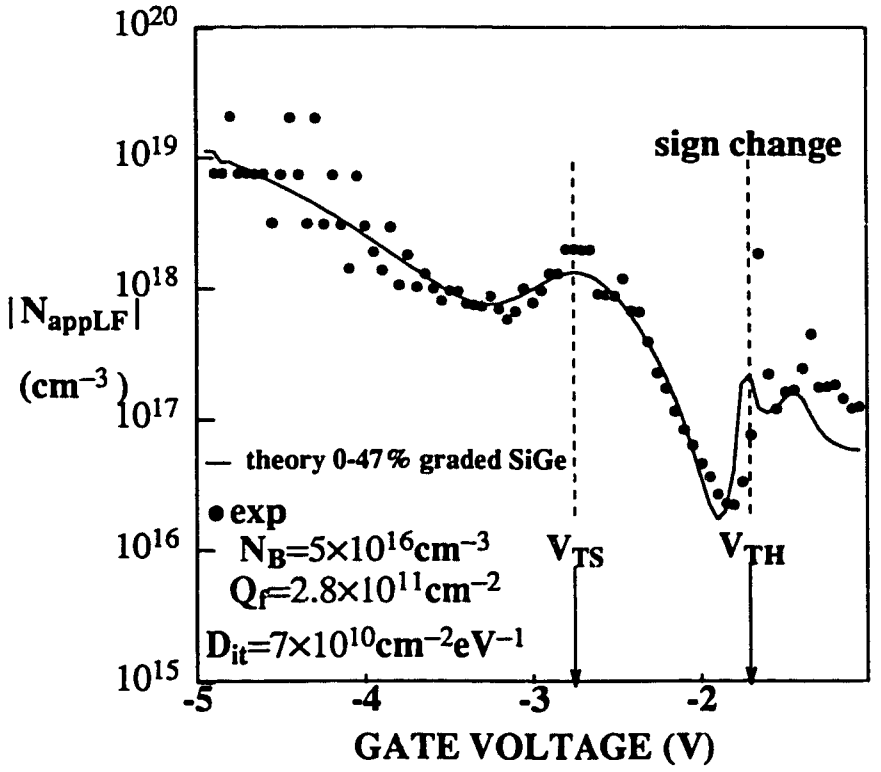


Figure 2.15 *Comparison of measured and simulated low-frequency apparent doping vs. gate voltage characteristics of Si/SiGe MOS capacitors as determined from the* C_{LF}–V_G *characteristics shown in Fig.2.12.*

Using these data, the valence band offset ΔE_{VH} = 347 meV was extracted by solving eqns. (2.22) and (2.23). This corresponds to a Ge mole fraction of 47%.

The average interface trap density $D_{it} = 7\times10^{10}cm^{-2}eV^{-1}$ was estimated from the difference between the experimental low frequency and high frequency C-V curves. As explained earlier, this value is low enough not to significantly affect the accuracy of the measured valence band offset.

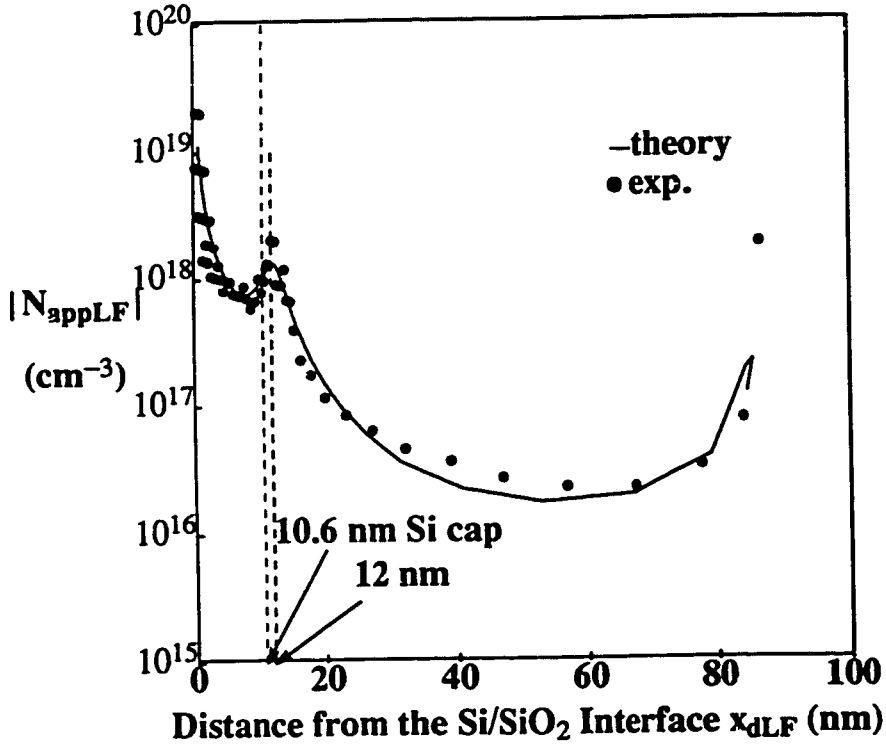


Figure 2.16 *Comparison of measured and simulated low-frequency apparent doping versus depth profiles of Si/SiGe MOS capacitors as determined from the* C_{LF}–V_G *characteristics (inversion region only) shown in Fig.2.14. The size-quantization-induced offset between the top Si/SiGe heterojunction and the position of the hole charge centroid, is also illustrated.*

To validate the characterization technique, the extracted structural and material parameters, were used as input data into the heterostructure MOS capacitor simulator. A uniformly distributed interface trap density of $7\times10^{10}cm^{-2}eV^{-1}$ was included in the simulation and a fixed charge density, $Q_f = 2.8\times10^{11}$ cm^{-2}, was determined by superimposing the calculated and experimental $C_{LF}(V_G)$ characteristics, as shown in Fig. 2.14. The simulated and experimentally derived $N_{appLF}-V_G$ and $N_{appLF}-x_{dLF}$ characteristics, are plotted in Figs. 2.15 and 2.16, respectively. They all show good agreement between theory and experiment.

2.4. Conclusions

A theory of the heterostructure MOS capacitor was developed. Ge profile grading and the presence of the δ-doped layer are accounted for. The main features in the operation of the Si/SiGe MOS capacitor, and the similarities and differences as compared to conventional Si devices, were discussed and explained based on this analytical model and on numerical simulation results. The impact of the structural parameters on device characterisristics and on the design of the corresponding Si/SiGe MOSFET was also investigated. Finally, starting from the interpretation of the low frequency and high frequency C-V characteristics, a technique was developed for the extraction of the layer structure and of valence band offset at the top Si/SiGe heterojunction from experimental C-V data. Experimental support for this characterization technique was provided.

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CHAPTER 3

THE Si/SiGe/Si p-MOSFET

3.1. Introduction

The aim of this chapter is to **a)** propose a triangular SiGe channel concept as leading to the best performance in deep submicrometer Type I p-channel MOSFET devices, **b)** develop a physically based compact model to explain the dc and high frequency characteristics of Si/SiGe/Si MOSFET's, **c)** discuss design guidelines for Si/SiGe/Si p-MOSFET's, and **d)** estimate the scaling limits of Si/SiGe/Si MOSFET's.

The chapter is organized as follows. First, in Section 3.2, existing Si/SiGe/Si FET concepts are analyzed and an optimized structure, with a triangular SiGe channel, is proposed. Section 3.3 discusses the dc and high frequency performance of Si/SiGe/Si p-MOSFET's. This discussion is supported by analytical and two-dimensional simulation results. The influence of Ge compositional grading on hot carrier injection is assessed based on energy balance simulations. Design issues are addressed in Section 3.4 and a design methodology is proposed. In Section 3.5, the potential of scaled Si/SiGe/Si MOSFET's with triangular Ge profiles is predicted based on the analytical model and is verified by numerical simulations for channel lengths as small as 0.06 μm. Finally, in Section 3.6, conclusions are drawn regarding the prospect of Si/SiGe/Si MOSFET's for low-voltage, high-speed digital and analog

applications.

As in the treatment of the Si/SiGe MOS capacitor, the detailed derivation of the analytical model is left to Appendix C. The two-dimensional (2D) simulations, required to realistically predict MOSFET behavior, were performed using the commercial heterostructure device simulator ATLASII/BLAZE.† Both the drift diffusion (DD) and the energy balance (EB) formalisms have been employed. For a detailed account of the simulation techniques, and of the models employed to describe the material properties of SiGe, Appendix D should be consulted. Finally, Appendix E describes techniques for the extraction of the dc and high frequency model parameters which are specific to Si/SiGe/Si MOSFET's. These are the mobility vs. gate voltage characteristics and the elements of the small signal equivalent circuit.

3.2. Basic Concept and Proposed Structure

The layer structure of a typical Si/SiGe/Si p-MOSFET [1-4] is shown in Fig.3.1. It features a thin (10-15 nm), buried channel of undoped SiGe, acting as a 2-Dimensional Hole Gas (2DHG). The SiGe film is separated from the gate oxide by an undoped Si cap. Because the bandgap difference between Si and SiGe is almost entirely accommodated in the valence band, the thin SiGe film forms a rectangular quantum well for holes. A 5 - 10 nm thick, p-type δ-doped region is inserted below the channel, in the Si substrate, to adjust the threshold voltage [3,4]. It also helps to maximize the number of carriers in the channel over a wide range of gate voltages

† ATLASII-BLAZE is a trademark of Silvaco International, Santa Clara, CA.

[5]†. Separation between the channel and the δ-doped layer is provided by an undoped Si buffer, 5 - 10 nm thick. Both undoped Si layers are intended to alleviate mobility degradation caused by interface and impurity scattering, respectively.

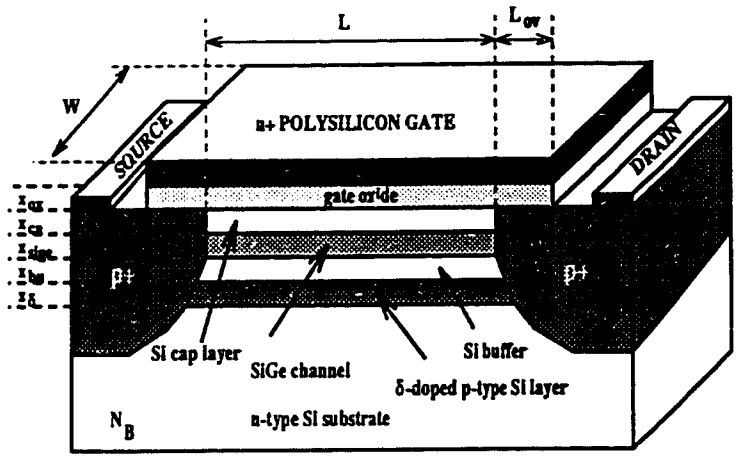

Figure 3.1 *Layer structure of the Si/SiGe/Si p-MOSFET. The Ge profile in the channel can be rectangular, trapezoidal or, as proposed here, triangular.*

Besides the ubiquitous gate length reduction, maximizing the transconductance of a FET requires that the gate to channel spacing be minimized, and that the effective velocity of the mobile carriers in the channel be maximized. The reduction of the gate to channel spacing is also instrumental in suppressing short channel effects. In order to improve the cutoff frequency, the effective carrier velocity must also be maximized.

† As shown recently [6], one can also control the charge distribution by inserting an insulating layer (such as SIMOX) immediately below the channel.

The gate to channel spacing has three components (i) the gate oxide thickness x_{ox}, (ii) the thickness of the silicon cap layer x_{ca}, and (iii) the gate-voltage-dependent distance between the channel/cap interface and the position of the charge centroid in the channel $\Delta x(V_{GS})$. Minimum practical limits of x_{ox} and x_{ca} are around 3 nm [7], and 5 nm, respectively. Both figures are comparable to the value of $\Delta x(V_{GS})$, which, under normal operating conditions, varies between 1 and 8 nm, depending on the energy bands profiles in the channel.

The effective hole velocity in the Si/SiGe/Si p-MOSFET is determined by the transport properties of the semiconductor material along the channel, and by the quantum distribution of mobile charge along the direction perpendicular to the channel. The transport properties of holes in the SiGe channel can be improved by employing a large Ge mole fraction Y. The benefit is two-fold. First, there is now compelling experimental evidence to show that hole mobility increases with Y [8,9]. Second, the large Ge mole fraction near the top of the channel provides a large barrier in the path of the high energy holes, precluding their transfer from the SiGe film to the Si cap layer, and increasing the number of carriers in the high mobility SiGe film.

The placement of the δ-doped film below the channel has a negative impact on $\Delta x(V_{GS})$ because carriers will be accumulated at the bottom of the channel. In deep submicrometer devices, this leads to transconductance degradation, and to a large subthreshold slope.

An alternative solution is proposed here, whereby the δ-doped region is maintained to control the threshold voltage, but its negative impact on transconductance is overcome by engineering the Ge mole fraction in the channel so that $\Delta x(V_{GS})$ is minimized over the entire bias range. As suggested earlier [5], full compositional grading can be employed to simultaneously maximize the velocity of holes in the channel and reduce the gate to 2DHG spacing. This is possible if the Ge mole fraction is linearly ramped up towards the gate, from 0% to 50%, in a triangular shape. As a result of the composition gradient, an electric field F_{bi} is induced in the channel. This field is directed from the substrate towards the gate and pushes the holes closer to the gate, where the Ge mole fraction and mobility are the largest.

The expected outcome of this grading scheme is performance leverage over a wide range of gate voltages as compared to Si, or rectangular Ge profile devices, as well as suppressed hot carrier injection. Large Ge mole fractions are typically accompanied by larger lattice mismatch and more dislocations. However, a device with triangular Ge channel profile alleviates this problem by maintaining a relatively small integrated Ge dose, while offering enhanced carrier confinement and faster transport along the channel.

The energy bands diagrams of the rectangular and of the proposed triangular SiGe channel are shown in Figs.3.2.a and b, respectively. In both cases the average Ge mole fraction is 25%, but it reaches a maximum value of 50% in the triangular channel device. The spacing between the top Si/SiGe interface and the actual location of the hole charge centroid in the channel Δx is also illustrated in Fig. 3.2. Δx is con-

siderably reduced in the device with triangular Ge profile.

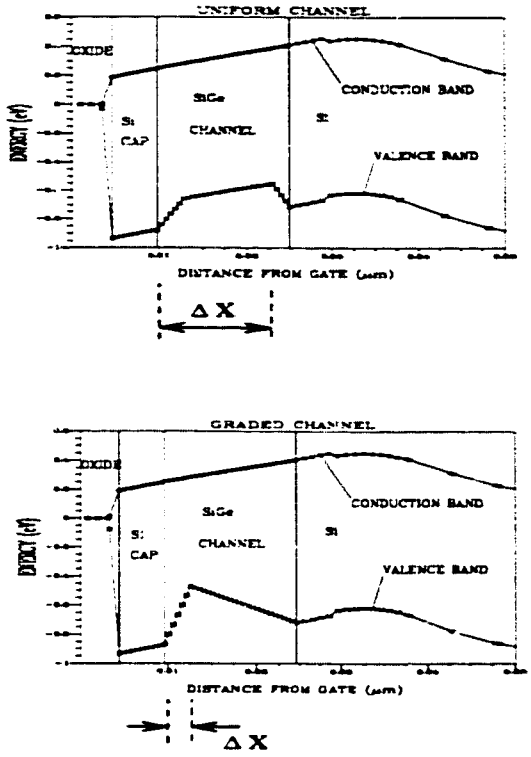

Figure 3.2 *Energy bands (a) of the rectangular (uniform) profile device, and (b) of the proposed triangular (graded) profile Si/SiGe/Si p-MOSFET.*

The Type I Si/SiGe/Si p-channel MOSFET structures investigated in this chapter are designed for 0.25 μm nominal gate lengths, and consist of (from substrate to the top gate oxide): an n-type Si substrate doped $6\times10^{17}cm^{-3}$, an 8 nm thick p-type Si layer δ-doped ~ $10^{18}cm^{-3}$, an undoped 5 nm thick Si buffer, an undoped 15 nm thick SiGe channel, an undoped 5 nm thick Si cap layer and a 5 nm gate oxide.

The Ge mole fraction in the channel is either constant at 25%, or graded from 0%, at the bottom of the channel, to 50% over 12 nm and then back to 0%, over 3 nm,

at the top of the channel, as shown in Fig.3.2.b. The "abrupt" heterojunctions are in fact graded over 3 nm in order to avoid mobility degradation caused by interface scattering. The total Ge dose is identical for the two profiles and is within the Matthews-Blakeslee critical layer thickness [10]. For other gate lengths, unless otherwise stated, the substrate doping and the gate oxide thickness are scaled according to the rules presented in Section 3.5. The rest of the structural parameters are left unchanged.

3.3. Si/SiGe/Si p-MOSFET Model

Even though charge control models have been developed [11,12], there is as yet no compact, physically based model to predict the circuit behavior of Si/SiGe/Si MOSFET's. Ideally, the special features associated with the charge dynamics of the buried and surface channels should be seamlessly grafted onto any of the standard Si MOSFET models [13]. Such a twin-channel, Si/SiGe/Si p-MOSFET model is proposed and discussed here. The complete derivation is presented in Appendix C. The model can be used as a tool in the interpretation of the simulated dc and ac characteristics of the device.

3.3.1. Threshold Voltage and Body Effect

The threshold voltage V_T, expressed as a function of the substrate bias V_{BS}, is

$$V_T = V_{T0} - \gamma\left[\sqrt{V_{BS} - \phi_{TH} + \phi_o} - \sqrt{-\phi_{TH} + \phi_0}\right] \qquad (3.1)$$

where

$$V_{T0} = V_{FB} + \phi_{TH} - \gamma\left[\sqrt{-\phi_{TH} + \phi_o} - \sqrt{\phi_1}\right]$$

and γ is the body factor defined as

$$\gamma = \frac{(1+\alpha)\sqrt{2q\varepsilon_{Si}N_B}}{C_{ox}}$$

ϕ_o and ϕ_1 are constants which depend on the doping profile (Appendix C) and α was defined in Chapter 2. Eqn. (3.1) predicts that the body effect is $(1+\alpha)$ times larger than in an equivalent Si p-MOSFET. Indeed, the model is validated by simulation, as shown in Fig. 3.3. The plots can be fitted by a straight line, indicating that, as in the case of a Si MOSFET, γ can be extracted from experimental data using a simple line fitting algorithm.

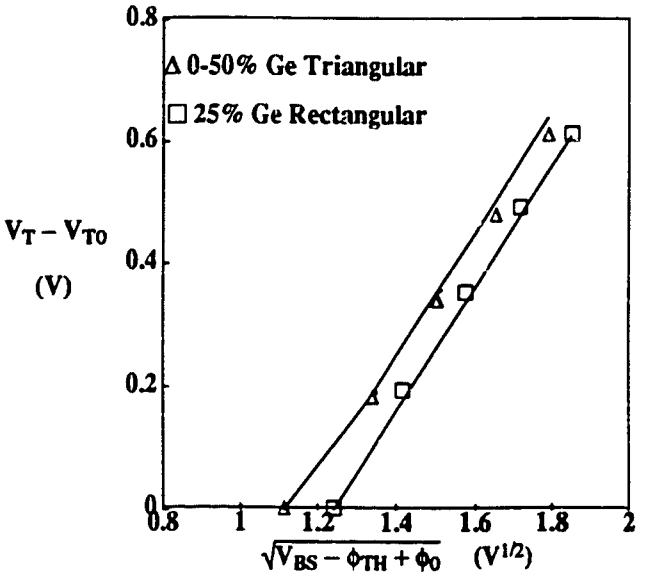

Figure 3.3 *Numerically (Δ, □) and analytically (solid line) computed body effect in Si/SiGe/Si p-MOSFET's.* V_{BS} *varies from 0 to 2 V.*

3.3.2. Threshold Voltage Roll-Off†

Threshold voltage roll-off is a short channel effect, whereby, for small gate lengths, the threshold voltage becomes a function of the gate length. This effect, which occurs in both Si and Si/SiGe/Si p-MOSFET's [14], is caused by the lowering of the potential barrier between the source and the drain, as a result of the drain to source lateral field. The voltage-doping transformation developed for Si MOSFET's [15] can be applied to model threshold voltage roll-off. This approach offers very good modeling accuracy, is physically based, and does not involve iterative computation [16].

According to the voltage-doping transformation, the relation for the long channel threshold voltage can still be used for the short channel device if the real doping concentration N_B is replaced by an effective doping concentration N_B^*. The latter is both bias and channel length dependent [15] and is given by

$$N_B^* = N_B + \frac{2\varepsilon_{Si} V_{DS}^*}{qL^2} \tag{3.2}$$

where V_{DS}^* is the effective drain to source voltage and, in the absence of substrate bias, is expressed as [15]

$$V_{DS}^* = V_{DS} - 2(V_{bi} + \phi_{TH}) - 2\sqrt{(V_{bi} + \phi_{TH})(V_{bi} + \phi_{TH} - V_{DS})} \tag{3.3}$$

where V_{bi} is the built-in voltage of the drain-substrate p-n junction.

In the limiting case of very small V_{DS}, eqn. (3.3) can be simplified as

† This part is adapted from [14]

$$V_{DS}^{*} = -4(V_{bi} + \phi_{TH}) \tag{3.4}$$

and substituted into eqn (3.2) to obtain the effective doping concentration N_B^*. Subsequently the latter is plugged into eqn. (3.1) to calculate the threshold voltage roll-off.

Fig.3.4 presents the numerically simulated threshold roll-off for devices with rectangular and triangular Ge channel profiles. They are qualitatively similar to those of an equivalent Si MOSFET.

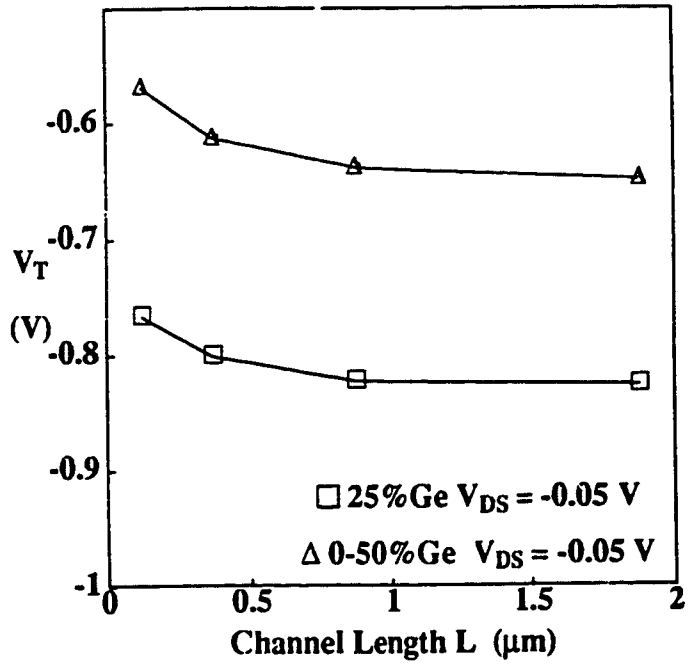

Figure 3.4 *Numerically computed threshold voltage roll-off in Si/SiGe/Si MOSFET's with triangular (Δ) and rectangular (□) Ge profiles. The doping and Ge profiles correspond to the 0.25 μm design.*

The simulation results are easily understood if the threshold roll-off effect is

interpreted as a reduction in the substrate doping. According to the analysis presented in Chapter 2, this causes a "roll-off" in the magnitude of the buried channel threshold, and an increase in the surface channel threshold. Eqn. (3.2) indicates that, in order to suppress the threshold voltage roll-off, the following condition must hold

$$N_B \gg \frac{2\varepsilon_{Si}|V_{DS}^*|}{qL^2} \tag{3.5}$$

3.3.3. I-V Characteristics

A. Subthreshold Region

As in a Si MOSFET, the subthreshold current is determined by the diffusion of carriers from the source to the drain. Since only the buried layer charge is important in weak inversion, the subthreshold current has an exponential dependence on the gate voltage, similar to that of Si MOSFET's

$$I_{DS} = I_o \exp\left[-\frac{V_{GS}}{\left[1+\frac{C_S}{C_{ox}}\right]\phi_T}\right]\left[\exp\left[\frac{V_{DS}}{\phi_T}\right]-1\right] \tag{3.6}$$

From eqn. (3.6) the subthreshold slope S, too, can be described by a Si MOSFET formula [7]

$$S = \frac{I_{DS}\ln(10)}{\frac{\partial I_{DS}}{\partial V_{GS}}} = \left[1+\frac{C_S}{C_{ox}}\right]\phi_T \ln(10) \tag{3.7}$$

where C_S is the semiconductor capacitance in weak inversion.

The impact of the Ge mole fraction grading δY_{bo} on the subthreshold slope is contained in the C_S term. The subthreshold slope is smaller for devices with a triangular Ge channel profile, as compared to those with a rectangular profile, but is still larger than in a Si MOSFET, as shown in Fig.3.5.

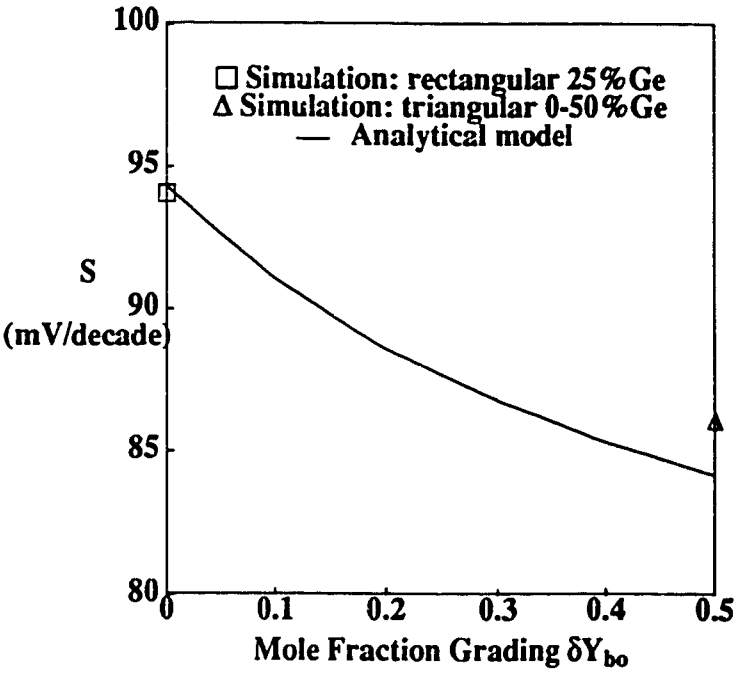

Figure 3.5 *Analytically and numerically computed subthreshold slope S in Si/SiGe/Si MOSFET's, as a function of Ge mole fraction grading* δY_{bo}. □ *and* Δ *indicate simulation results for devices with 25%Ge rectangular and 0-50% Ge triangular profiles, respectively. Between these extreme cases, the analytical subthreshold slope corresponds to trapezoidal Ge profiles.*

Similarly, the subthreshold transconductance is comparable to that of the Si device

$$g_m = \frac{I_{DS}}{S}\ln(10) = \frac{I_{DS}}{\phi_T}\frac{1}{1+\frac{C_S}{C_{ox}}} \tag{3.8}$$

indicating a steeper turn-on for the triangular profile as compared to rectangular ones.

B. Strong Inversion

The inclusion of the twin-channel charge dynamics in the theoretical I-V characteristics of the Si/SiGe/Si p-MOSFET amounts to replacing C_{ox} with an effective gate capacitance C_{eff}, and μ_p with an effective channel mobility μ_{eff}, in the Si p-MOSFET equations. In order to ensure the continuity of the drain current and of its first order derivatives with respect to the terminal voltages, the gate voltage dependence of C_{eff} and μ_{eff} must be modeled.

The effective gate capacitance is described by the following function

$$C_{eff} = \frac{C_{ox}}{1+\frac{\alpha}{g(V_{GS},V_{TS})}} \tag{3.9}$$

where

$$g(V_{GS},V_{TS}) = \sqrt{1+\exp\left[\frac{V_{TS}-V_{GS}-V_{on2}}{n_1\phi_T}\right]} \tag{3.10}$$

$$n_1 = \frac{\partial V_{GS}}{\partial \phi_S} = 1+\frac{C_S(\phi_S = 2\phi_F)}{C_{ox}} = 1+\frac{1}{\alpha}$$

$$V_{on2} = n_1 \phi_T \ln\left[\frac{N_{VSiGe}}{N_B}\right]$$

$g(V_{GS}, V_{TS})$ models the transition from the plateau capacitance $C_{ox}/(1+\alpha)$, corresponding to the accumulation of holes only at the top Si/SiGe heterojunction, to C_{ox}, which describes the situation when the parasitic surface channel is fully open for conduction.

According to Appendix C, the effective mobility can be expressed as

$$\mu_{eff} = \frac{C_{ox}}{C_{eff}} \frac{\left[\mu_{pSi} u(V_{GS}, V_{TS}) + \frac{\mu_{pSiGe}}{1+\alpha} h(V_{GS}, V_{TS})\right]}{1 + \theta(V_T - V_{GS})} \tag{3.11}$$

where

$$h(V_{GS}, V_{TS}) = 1 - 2n_1 \phi_T \frac{\ln[g(V_{GS}, V_{TS})]}{V_T - V_{GS}}$$

$$u(V_{GS}, V_{TS}) = 2n_1 \phi_T \frac{\ln[g(V_{GS}, V_{TS})]}{V_T - V_{GS}}$$

and mobility degradation, caused by the vertical electric field, is described by θ.

By considering a realistic velocity-field relationship (Appendix C), the impact of the longitudinal electric field on carrier mobility (velocity saturation) can be accounted for. The drain current expressions that follow become accurate for both long and short channel devices. In the nonsaturation region ($V_{DS} \geq V_{DSAT}$)

$$I_{DS} = \frac{W}{L} \frac{\mu_{eff} C_{Geff}}{1 - \frac{\mu_{eff}}{v_{psat}} \frac{V_{DS}}{L}} \left[V_T - V_{GS} + \frac{V_{DS}}{2}\right] V_{DS} \tag{3.12}$$

while in saturation ($V_{DS} < V_{DSAT}$)

$$I_{DSAT} = -\frac{2W}{L}\frac{\mu_{eff}C_{Geff}\left[V_T - V_{GS}\right]^2}{\left[1+\sqrt{1+\frac{2\mu_{eff}(V_T - V_{GS})}{v_{psat}L}}\right]^2} \tag{3.13}$$

where

$$V_{DSAT} = \frac{v_{psat}L}{\mu_{eff}}\left[1-\sqrt{1+\frac{2\mu_{eff}(V_T - V_{GS})}{v_{psat}L}}\right] \tag{3.14}$$

In the limit case of a long channel device $(V_T - V_{GS}) \ll \frac{v_{psat}L}{\mu_{eff}}$, the drain current and the saturation voltage expressions revert to the usual ones.

The ratio of the gain parameters $\frac{\beta_{SiGe}}{\beta_{Si}}$, plotted in Fig.3.6, is the best indicator of the performance leverage expected from the SiGe channel. Because of the smaller effective gate capacitance of the Si/SiGe/Si FET (1.5 times in this particular case), the gain parameter ratio is everywhere lower than $\frac{\mu_{pSiGe}}{\mu_{pSi}}$. As an artifact of the velocity saturation effect, the ratio increases steadily when the surface channel threshold is approached and drops when the magnitude of the gate to source voltage becomes larger than V_{TS}. Also as a result of velocity saturation effects, the gain parameter ratio decreases as the channel length is reduced.

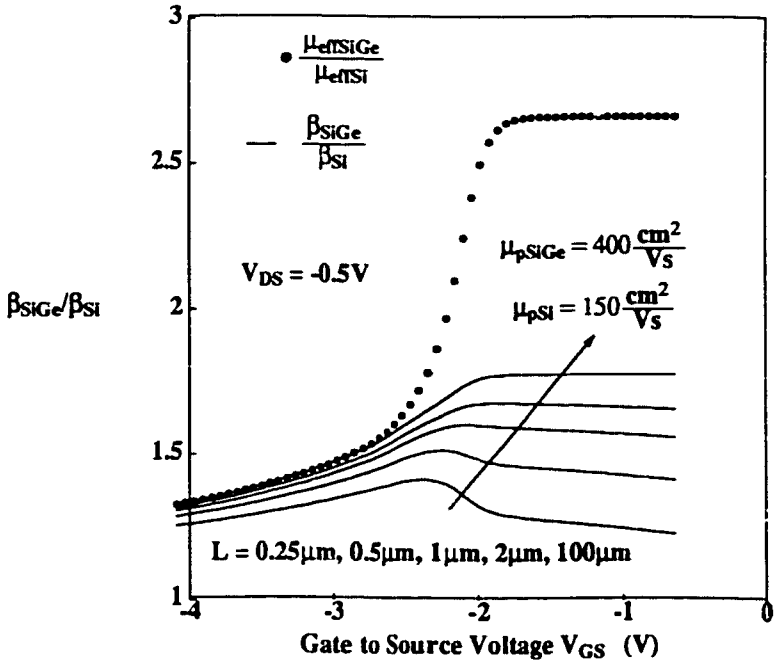

Figure 3.6 *Analytically computed gain parameter ratios, in the linear region, as a function of the gate voltage. The channel length,* L, *is a variable parameter. The ratio of the effective hole mobilities is plotted as reference. The hole mobility values in Si and SiGe are based on experimental data to be presented in Chapter 4.*

Eqns. (3.6), (3.12), and (3.13) can be used to interpret the simulated transfer characteristics, plotted in Fig. 3.7 for the triangular and rectangular SiGe channel p-MOSFET's with 0.25 μm gate length. Because of the larger gain parameter, the drain current of the triangular profile MOSFET is everywhere larger than that of the rectangular Ge channel one. The higher valence band offset in the device with a triangular Ge profile and the built-in electric field induced by Ge mole fraction grading are responsible for the difference in threshold voltages.

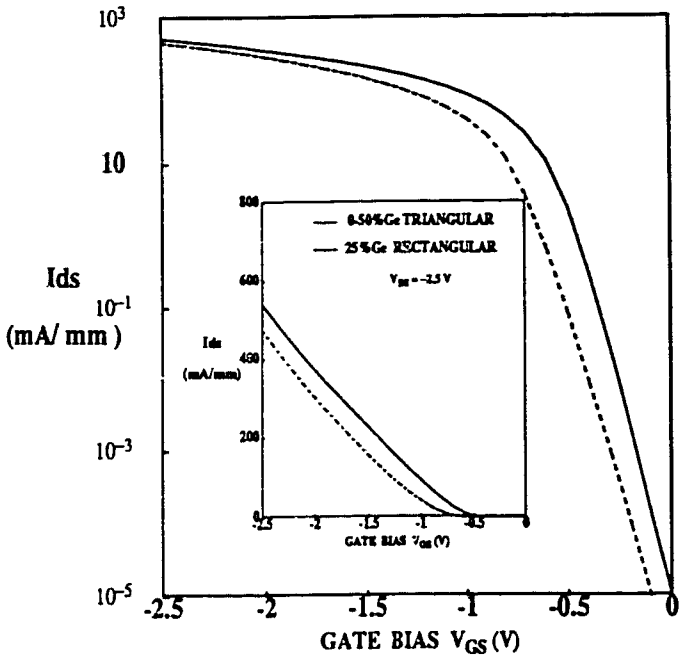

Figure 3.7 *Simulated transfer and subthreshold characteristics for 0% -50%Ge triangular (solid line) and 25%Ge rectangular (dotted line) channel p-MOSFET's obtained with the drift diffusion model.*

3.3.4. Hot Carrier Effects

Energy Balance simulations were performed in order to analyze the impact of non-local transport effects and carrier heating on the DC characteristics of 0.25 μm Si/SiGe/Si p-MOSFET's. As shown in Fig.3.8, in the subthreshold region, where small currents and gate voltages are involved, Drift-Diffusion (DD) and Energy Balance (EB) results are in close agreement. This situation is maintained at moderate current levels, slightly above threshold. It is only for large gate voltages that, because velocity overshoot is neglected, the DD model underestimates the drain current.

It was found that, for V_{DS} = -2.5 V and V_{GS} = -2.5 V, the temperature of the hot holes at the drain end of the channel was similar in triangular and rectangular channel FET's . However, the temperature of holes residing in the Si cap layer was 2500 K in the device with triangular Ge profile, and 4000 K in the rectangular one. This confirms that the higher valence band energy barrier between the triangular channel and the Si cap limits hot carrier injection in the cap layer and in the oxide.

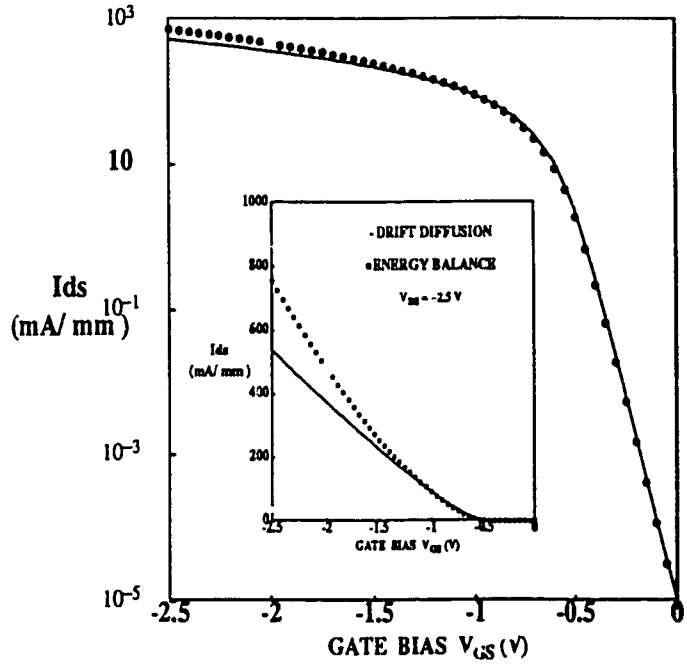

Figure 3.8 *A comparison of simulated subthreshold and transfer (inset) characteristics for the triangular profile Si/SiGe/Si p-MOSFET obtained using the Drift-Diffusion (solid line) and the Energy Balance models (bullets).*

Additional evidence to support the suppressed hot carrier injection in p-MOSFET's with triangular Ge profiles is provided by the ratio of the substrate and drain currents.

Fig.3.9 shows this ratio as a function of the drain to source voltage. A factor of two improvement is obtained for the triangular device at high drain bias. The shape of the characteristics is similar to that experimentally observed in Si MOSFET's [17].

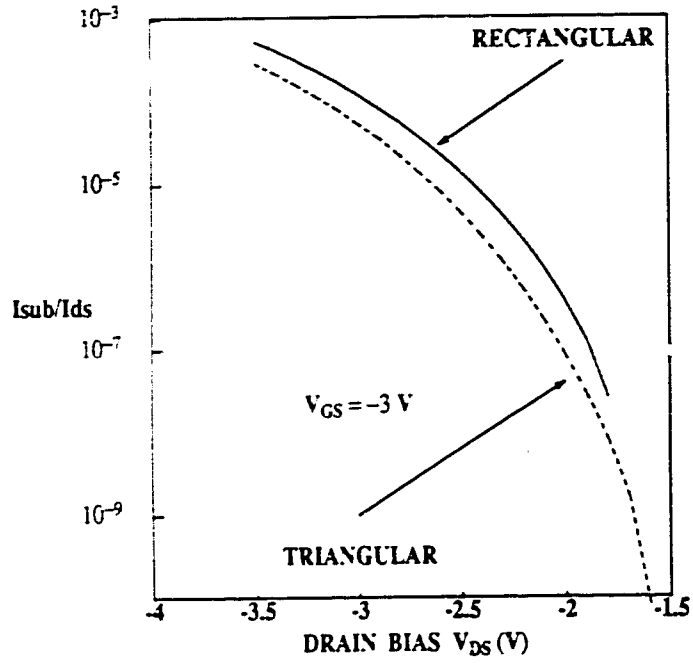

Figure 3.9 *The ratio of the substrate and drain currents in triangular and rectangular profile p-MOSFET's with 0.25 μm gate lengths.*

In general, a comparison between DD and EB simulation results suggests that the impact of hot carrier transport on the DC and high frequency characteristics of Si/SiGe/Si MOSFET's is more significant than in Si/SiGe/Si HBT's [18] and cannot be overlooked for linewidths smaller than 0.25 μm. To conclude the discussion on the I-V characteristics, it should be noted that, in spite of quantitative differences, their shape is similar to that of Si MOSFET's. The distinctive features of Si/SiGe/Si p-

MOSFET's become apparent in the ac parameters, to be discussed next.

3.3.5. Small Signal Equivalent Circuit

The small signal circuit model of a Si/SiGe/Si p-MOSFET can be derived by applying a transmission line analysis [19]. Such an approach, applicable to all types of FET's [20], is analytically feasible only in the nonsaturation regime, when the channel can be approximated by a uniform, active transmission line, as illustrated in Fig.3.10. This approximation breaks down in the saturation regime. Instead, the parameters that model the intrinsic part of the lumped small signal circuit can be accurately obtained from two-dimensional numerical simulation results using frequency domain perturbation analysis [21].

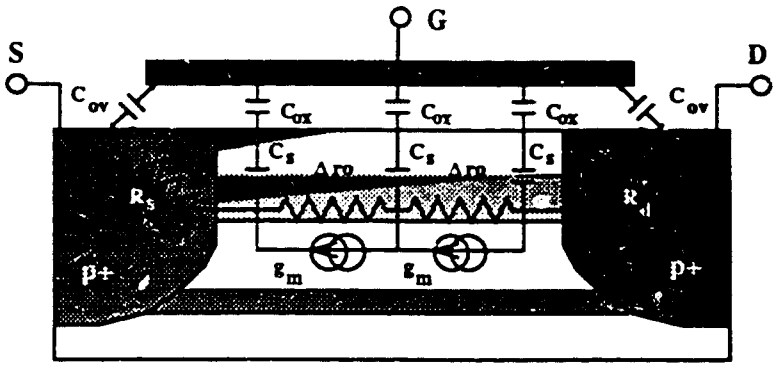

Figure 3.10 *Schematic representation of a Si/SiGe/Si MOSFET as an active transmission line. Both the buried and the surface channels are shown. The device is assumed to be operating in velocity saturation regime.*

The most relevant of these parameters - the transconductance g_m, the output conductance g_{ds}, the gate to source capacitance C_{gs}, the gate to drain capacitance C_{gd}

and the drain to source capacitance C_{ds} - can be directly obtained from the low frequency values of the simulated Y parameters. Others, important only at high frequency, such as the resistance of the nonsaturated part of the channel R_i, the gate-drain access resistance R_{gd} and the transconductance delay τ, can be extracted indirectly, from the frequency dependence of the simulated Y parameters, according to the technique described in Appendix E.

The second group of model parameters, R_i, R_{gd} and τ, are not usually considered in the Si MOSFET model. It is important to note that, for small values of the drain to source voltage V_{DS}, R_i and R_{gd} become equal [19]. In deep saturation though, only R_i has a nonzero value. The transconductance delay τ represents the transit time of carriers traversing the pinched-off (or saturated velocity) part of the channel, located at the drain end. In the non-saturation regime τ becomes vanishingly small.

The complete small signal model, including parasitics, is shown in Fig.3.11. As in GaAs MESFET's and HEMT's [20], the gate inductance L_g is gate voltage dependent

$$L_g = \frac{\mu_0 x_{ox}\left[1 + \dfrac{\alpha}{g(V_{GS}, V_{TS})}\right] W}{m^2 L} \tag{3.15}$$

where μ_0 is the permeability of free space, x_{ox} is the thickness of the gate oxide and m is the number of gate fingers. α and $g(V_{GS}, V_{TS})$ have already been defined. The gate voltage dependence of the gate inductance can be explained as follows. The gate

electrode and the channel act as conductive layers, separated by a nonuniform "insulator" consisting of the gate oxide and of the Si cap layer. However, as the gate voltage changes, so does the thickness of the "insulator" because carriers start to travel through the cap layer. The channel electrode effectively moves closer to the gate electrode. As a result, the gate acts like a microstrip line with a bias dependent characteristic impedance. Its lumped circuit approximation therefore consists of a bias dependent capacitance C_{gs} and a bias dependent inductance L_g [20].

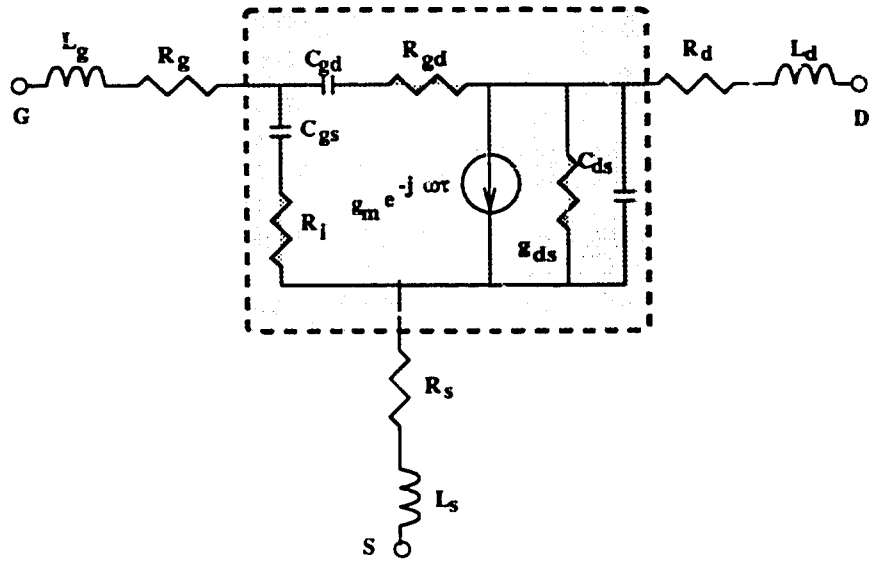

Figure 3.11 *Small signal lumped circuit model employed in the small signal analysis of Si/SiGe/Si MOSFET's. (The source and substrate terminals are shorted).*

The gate resistance R_g and the source/drain series resistances R_s and R_d are comparable to those of a Si MOSFET. The source/drain inductances L_s and L_d are associated with the metal interconnect from the pad to the actual device.

To underline the benefits of using a triangular profile in the channel, simulation results are discussed next. Numerically simulated transconductance versus gate voltage characteristics are plotted in Fig.3.12. To assess the impact of velocity saturation on transconductance, structures with 0.25 μm, 0.5 μm, 1 μm and 2 μm gate lengths were investigated. Devices with triangular channel profiles exhibit a sharper turn-on, immediately above threshold, and higher transconductance. This steep increase in transconductance, predicted by eqn. (3.8), is due to the higher mobility at the top of the triangular channel and to the built-in field.

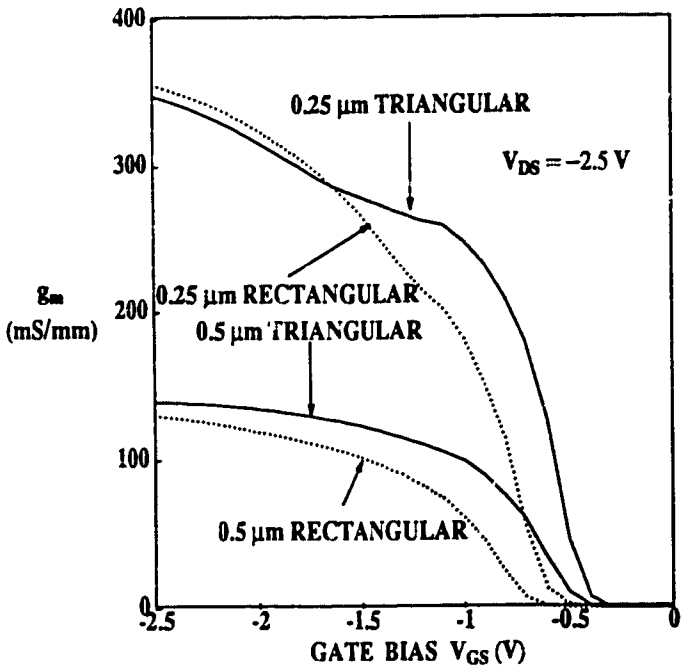

Figure 3.12 *Simulated transconductance characteristics for 0%-50% Ge triangular, and 25% Ge rectangular profile p-MOSFET's.*

For MOSFET's with 0.5 μm linewidths, the advantage of the triangular Ge profile is maintained throughout the investigated gate voltage range. The speed and gain improvements diminish as the device dimensions shrink. In the case of the 0.25 μm MOSFET's, the superiority of the triangular channel is lost at gate voltages beyond -1.75 V when, regardless of the compositional profile in the channel, transconductance saturates at 350 mS/mm. As suggested by eqn. (3.13), at a gate length of 0.25 μm, saturation velocity, rather than mobility, limits peak g_m.

Because of the better confinement of carriers in the channel, triangular profiles were also found to reduce the output conductance in the saturation region. As a consequence, the intrinsic voltage gain g_m/g_{ds} of the 0.5 μm device increased from 23 in the rectangular Ge channel, to 32 in the triangular Ge channel. For large gate voltages, the voltage gain of the 0.25 μm MOSFET's reduces to 25, regardless of the Ge profile in the channel. The reason is that, in this bias range, most of the conduction takes place in the cap layer, which is identical in the two structures.

The bias dependence of some of the elements of the small signal equivalent circuit is presented in Appendix E. Except for τ, all small signal circuit elements scale with respect to the gate width W

$$g_m = g'_m W, \quad g_{ds} = g'_{ds} W, \quad C_{gs} = C'_{gs} W, \quad C_{gd} = C'_{gd} W, \quad C_{ds} = C'_{ds} W$$

$$R_g = R'_g W, \quad Lg = Lg' W, \quad R_s = \frac{R'_s}{W}, \quad R_i = \frac{R'_i}{W}, \quad R_{gd} = \frac{R'_{gd}}{W}$$

As discussed next, the dependence on W is important in optimizing the high frequency and noise performance of Si/SiGe/Si MOSFET's.

3.3.6. High Frequency Performance

The frequency dependence of the current gain h_{21} and of the unilateral power gain GU_{max}, were calculated from the simulated S parameters. From the $h_{21}(f)$ and $GU_{max}(f)$ characteristics, the unity gain cutoff frequency f_T and the maximum frequency of oscillation f_{max} were determined according to their definition, without extrapolation

$$h_{21}\Big|_{f=f_T} = 1, \quad GU_{max}\Big|_{f=f_{max}} = 1$$

Analytical expressions, based on the single-pole, low-frequency extrapolation, were also employed to gain insight into the impact of the various equivalent circuit parameters on the cutoff frequency and on the maximum frequency of oscillation.

The cutoff frequency f_T can be estimated using

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{3.16}$$

In the limit of small V_{DS}, eqn. (3.16) can be expressed as

$$f_T = \frac{\mu_{eff}}{2\pi L} \frac{V_{DS}}{L + \frac{2C_{ox}L_{ov}}{C_{eff}}} \tag{3.17}$$

and can be used to extract the gate voltage dependence of the effective mobility, as explained in Appendix E. To avoid errors associated with the overlap capacitance, $C_{ov} = 2C_{ox}L_{ov}W$, the test structure must be a long and wide device (FATFET) with $L \gg \frac{2C_{ox}L_{ov}}{C_{eff}}$.

If velocity saturation occurs, eqn. (3.17) must be replaced by the equation

$$f_T = \frac{3v_{psat}}{4\pi} \frac{1}{L\left[1 + \frac{2V_1V_2}{(V_1+V_2)^2}\right] + \frac{3C_{ox}L_{ov}}{C_{eff}}} \tag{3.18}$$

where V_1 and V_2 depend on the terminal voltages V_{GS} and V_{GD} (Appendix C).

According to eqns. (3.17) and (3.18), the cutoff frequency is independent of the gate width and switches from a L^{-2} dependence in the linear region, to an L^{-1} dependence in the velocity saturation regime. Fig. 3.13 presents the simulated gate voltage dependence of the cutoff frequency in saturation for devices with rectangular and triangular Ge profiles in the channel.

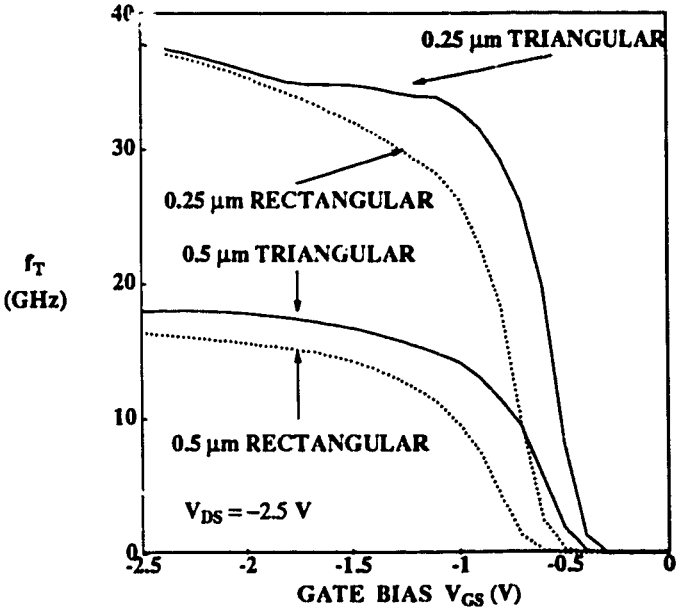

Figure 3.13 *Simulated cutoff frequency vs. gate voltage characteristics for 0%-50% Ge triangular, and 25% Ge rectangular profile p-MOSFET's.*

The behavior is very similar to that of the transconductance characteristics and the same interpretation applies. The triangular profile offers superior cutoff frequency in comparison to the rectangular one. As a result of velocity saturation, the advantage of the triangular profile diminishes in deep submicron devices if large gate and drain voltages are applied. Operation in the velocity saturation regime must, therefore, be avoided.†

The maximum frequency of oscillation f_{max} depends on both intrinsic and extrinsic circuit elements. It can be approximated by eqn. (3.19) [20]

$$f_{max} = \frac{f_T}{2[(R_g + R_i + R_s)g_{ds} + 2\pi k_g \sqrt{g_{ds} f_T}]^{1/2}} \tag{3.19}$$

In order to improve f_{max}, f_T must be increased and the drain to source conductance, g_{ds}, must be reduced. At the same time, the total input resistance, $R_g + R_s + R_i$, especially R_g, needs to be minimized. Fig.3.14 demonstrates that, primarily as a result of the larger cutoff frequency and lower output conductance, the superiority of the triangular profile is extended to include f_{max}.

Fig. 3.14 also shows that, unlike the cutoff frequency, because of the non-zero gate resistance, f_{max} is a strong function of the device gate width, W

$$f_{max}(W) = \frac{f_T}{2[W^2 R'_g(g'_{ds} + 2\pi f_T C'_{gd}) + (R'_i + R'_s)g'_{ds}]^{1/2}} \tag{3.20}$$

There is a maximum value of W below which the gate width dependence becomes

† There is little experimental evidence to indicate that the saturation velocity of holes in SiGe is larger than in Si.

negligible

$$W_{max\_osc} = \left[\frac{(R'_i + R'_s)g'_{ds}}{R'_g(g'_{ds} + 2\pi f_T C'_{gd})} \right]^{1/2} \tag{3.21}$$

It is recommended that, in order to avoid f_{max} degradation, the gate width be kept smaller than W_{max_osc}. An interdigitated layout should be employed if wide devices are required.

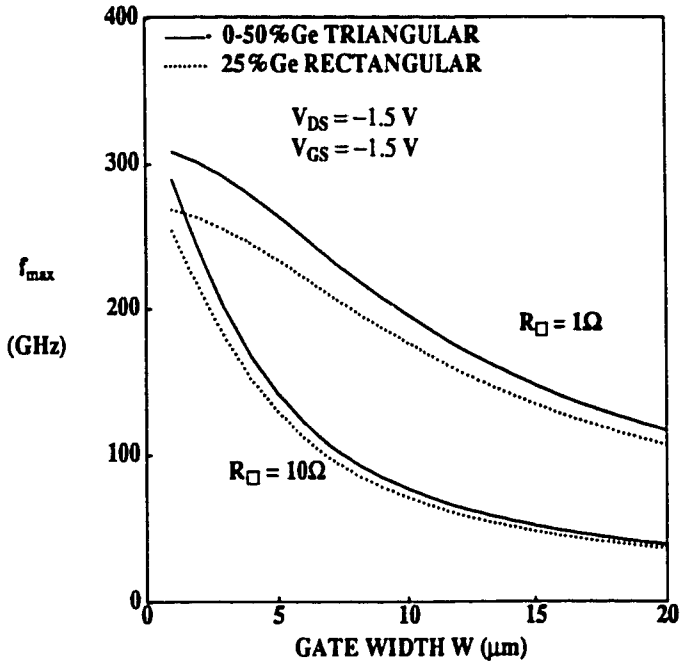

Figure 3.14 *Maximum frequency of oscillation vs. gate width for triangular and rectangular Ge channel profile p-MOSFET's with 0.25 μm gate lengths.* $R_\square$ *is the sheet resistance per square of the gate poly and is considered as a variable parameter.*

3.3.7. Noise Performance

The noise circuit model can be derived in conjunction with the small signal circuit model [19]. As for other FET's, the noise of the Si/SiGe/Si p-MOSFET is represented by two internal noise currents

$$\overline{i^2}_{nd}(f) = 4kTPg_m + \frac{k_f g_m{}^2}{f^{af} C_{eff} WL} \tag{3.22}$$

$$\overline{i^2}_{ng}(f) = 4kTR\omega^2 \frac{C_{gs}^2}{g_m} \tag{3.23}$$

Their correlation is modeled by an imaginary coefficient

$$jC = \frac{\overline{i_{ng} \times i^*_{nd}}}{\sqrt{\overline{i^2}_{nd} \times \overline{i^2}_{ng}}} \tag{3.24}$$

P, R and C are *intrinsic noise parameters* that describe the medium and high frequency noise added by the device. They depend on the local temperature of the carriers in the channel [19]. k_f and *af* are *intrinsic noise parameters* that account for the 1/f noise of the device, which is important at low frequencies.

As shown in Appendix C, the minimum noise figure F_{min}, is well modeled at moderate and high frequencies by the following equation

$$F_{min} = 1 + 2\sqrt{k_1}\frac{f}{f_T}\sqrt{(R_s + R_g)g_m + k_2[1 + (\omega R_i C_{gs})^2]} \tag{3.25}$$

where k_1 and k_2 can be expressed in terms of the intrinsic noise parameters (Appendix C).

The non-zero gate resistance R_g causes F_{min}, just like f_{max}, to become dependent on the gate width W. To emphasize it, eqn. (3.25) is rewritten as

$$F_{min} = 1+2\sqrt{k_1}\frac{f}{f_T}\sqrt{R'_s g'_m + k_2[1+(\omega R_i C_{gs})^2] + R'_g W^2} \qquad (3.26)$$

A maximum gate width, below which the gate width dependence of F_{min} becomes negligible, can also be defined. The maximum gate width W_{max_noise} is frequency dependent, but this effect is important only at frequencies higher than f_T.

$$W_{max\_noise} = \frac{k_2[1+(\omega R_i C_{gs})^2] + g'_m R_s'}{R_g'} \qquad (3.27)$$

Fig. 3.15 shows that, as a result of the larger transconductance and cutoff frequency, the noise figure of the triangular channel MOSFET is smaller than that of the rectangular channel device. In the noise figure calculations, P, R, and C were determined according to the formulae given in [19], using the hole temperature values obtained from Energy Balance simulations. At the low-noise bias of V_{GS} = -1.5V and V_{DS} = -1.5V, the temperature of holes were 600 K and 750 K, in the triangular and rectangular channels, respectively. The noise figure was then calculated from eqn. (3.25), plugging in numerically simulated values of the small signal model parameters.

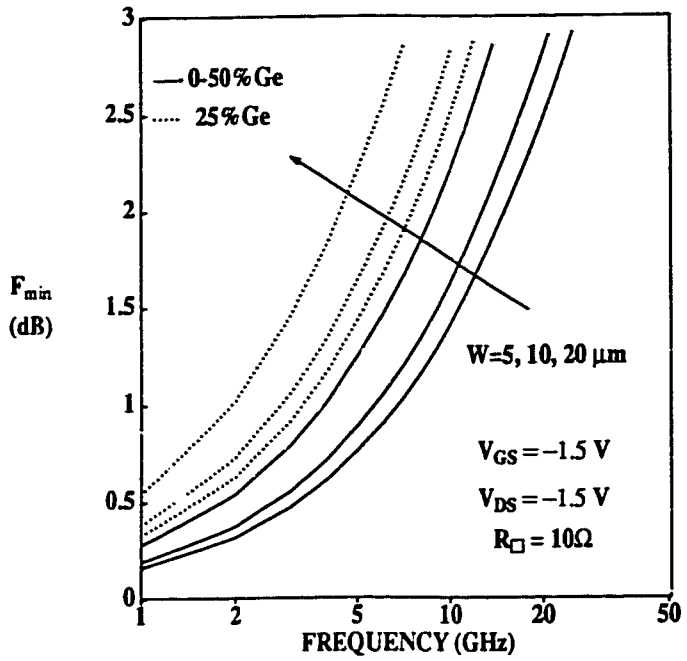

Figure 3.15 *Minimum noise figure vs. frequency for triangular and rectangular Ge channel profile p-MOSFET's. The gate width is a variable parameter. The gate length is 0.25 μm.* $R_{\square}$ *is the sheet resistance per square of the gate poly.*

3.4. Si/SiGe/Si p-MOSFET Design Methodology

There are five device parameters that impact significantly circuit performance. These are: transconductance g_m, output conductance g_{ds}, unity gain cutoff frequency f_T, maximum frequency of oscillation f_{max} and minimum noise figure F_{min}.

The transconductance, output conductance and the unity gain cutoff frequency characterize the intrinsic device and are important in both analog and digital applications. Their design is a 2D problem whereby the optimization of the vertical struc-

ture and the reduction of the length of the conduction path between source and drain are pursued.

f_{max} and F_{min} depend on the architecture of the whole device, including parasitics, and are relevant for analog applications. Any improvement in transconductance and cutoff frequency directly reflects on f_{max} and F_{min}. Additional leverage is obtained by minimizing the source and gate resistances, R_s and R_g, respectively. The design for optimized f_{max} and F_{min} is a 3D problem. Design guidelines are discussed next.

3.4.1. Guidelines for Vertical Layer Structure Design

The most critical aspect of Si/SiGe/Si p-MOSFET design involves the vertical layer structure. Based on the analytical equations and on the simulation results presented in Section 3.3, the following guidelines should be considered.

a) Select the appropriate oxide thickness x_{ox} for the desired supply voltage and gate length, as for a conventional Si MOSFET.

b) In order to avoid scattering with the Si/SiO_2 interface and to maximize the gate voltage window ΔV_T, the Si cap layer thickness x_{ca}, should be chosen in the 5 nm to 8 nm range.

c) Maximize the Ge mole fraction at the top of the channel Y_H, while keeping the total Ge dose below the critical limit. As illustrated in Fig.3.16 -- where the gate voltage window is plotted as function of the Ge mole fraction grading δY_{bo} -- this implies using a triangular profile in conjunction with a SiGe channel thick-

ness of 10 to 15 nm. In order to reduce interface scattering, the top Si/SiGe heterojunction must be graded over 3 nm.

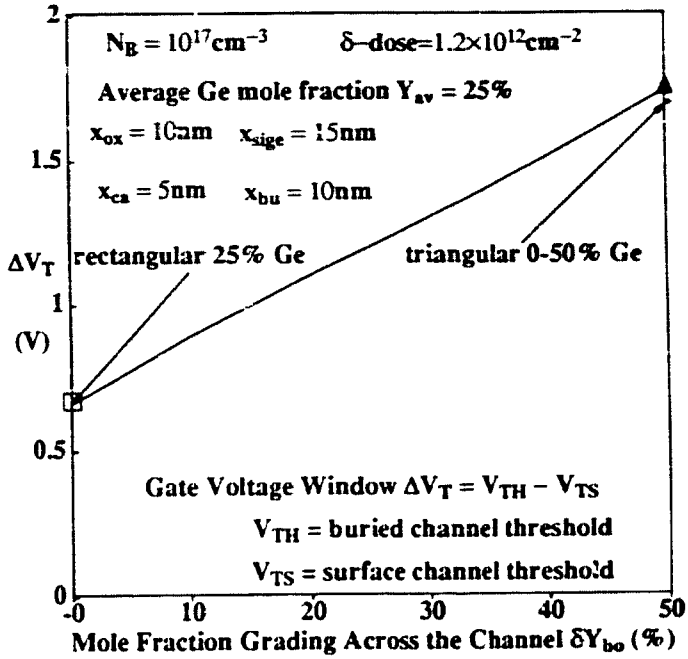

Figure 3.16: *Numerically computed gate voltage window* ΔV_T, *in a Si/SiGe/Si MOSFET, as function of the Ge mole fraction grading* δY_{bo}.

d) For the given supply voltage and gate length, select the substrate doping, N_B, from eqn. (3.5), that satisfies the condition for DIBL effect suppression.

e) Choose a suitable δ-doped layer dose to meet the threshold voltage specification. In order to minimize short channel effects, the thickness of the δ-doped layer must be 5 to 8 nm. For the same reason, and to avoid mobility degradation due to impurity scattering, x_{bu} = 5 nm to 10 nm.

f) Junction depths and lengths should be identical to those of the corresponding Si

p-MOSFET. LDD profiles are not necessary since hot carrier effects are reduced as compared to Si devices.

3.4.2. Guidelines for Layout Geometry Design

Since in non-LDD structures R_g is more of a problem than R_s, layout design must focus on the minimization of the parasitic gate resistance, the main culprit in the degradation of f_{max} and F_{min}. Two layout geometries can be considered: a) a π shape gate in which the effective gate width that determines the gate resistance is one quarter of the total physical gate width, W

$$R_g = \frac{R_\square W}{4L}$$

b) an interdigitated structure with m unit devices connected in parallel, whereby the gate resistance is reduced to $R_g = \frac{R_\square W}{m^2 L}$.

$R_\square$ is the sheet resistance of the polysilicon gate. Practical values for m lie between 2 and 8. As an example, if $R_\square$ = 10 Ω/□, W = 300 μm, L = 2 μm and m = 6, then R_g = 375 Ω for the π-shaped gate, and R_g = 42 Ω for the interdigitated one. It is important to note that R_s is identical for the two layout geometries.

3.5. Si/SiGe/Si p-MOSFET Scaling

The model equations presented in Section 3.3. can be employed to derive constant-field scaling rules for the Si/SiGe/Si p-MOSFET, in a similar way they were developed to predict conventional Si MOSFET scaling.

3.5.1. Scaling Rules

Table 3.1 summarizes constant field scaling rules as applied to Si/SiGe/Si p-MOSFET's. The rules by which the structural parameters and the bias voltage are scaled are postulated in the upper part of Table 3.1. From them, scaling rules for the device parameters that are relevant for circuit performance were derived, based on the model equations developed in Section 3.3. This second set of scaling rules are listed in the bottom part of the table. While many similarities exist with the Si MOSFET, some of the differences are worthy of close scrutiny.

(i) The "≤" sign in Table 3.1 indicates that, for devices with very short gate lengths, the scaling factor begins to depart from the Si MOSFET value. The culprit is the thickness of the Si cap layer x_{ca}, which cannot be scaled. The minimum practical limit for x_{ca} is about 5 nm, leading to a minimum gate length L_{min} that is approximately $1.33^{0.33}$ times larger than that of Si MOSFET's [22]

$$L_{min} = A\left[x_j x_{ox}(1+\alpha)(x_{dS}+x_{dD})^2\right]^{1/3} \qquad (3.28)$$

A, measured in $V^{-1/3}$, is a constant. x_{dS} and x_{dD} are the thicknesses of the depletion regions at the source/substrate and drain/substrate junctions, respectively. x_j is the junction depth of the source and drain contact regions.

(ii) Low-field mobility does not degrade in scaled-down devices because the doping level (or rather lack of intentional doping) in the channel remains unchanged. On the contrary, as a result of the reduced effective mass of holes in SiGe, velocity overshoot is expected to improve device speed at a higher rate than that predicted by

this scaling scheme.

TABLE 3.1
Constant Field Scaling Rules for Si/SiGe and Si p-MOSFET's

Device Parameter	SiGe MOSFET Scaling Factor	Si MOSFET Scaling Factor
L, W, x_{ox}	1/M	1/M
Junction length, L_j, and depth, x_j	1/M	1/M
x_{cs}, x_{SiGe}, x_{bu}, x_δ	1	-
N_{cs}, N_{SiGe}, N_{bu}	1	-
N_B, N_δ	M	M
V_{GS}	1/M	1/M
$A = W(L_j + x_j)$	$1/M^2$	$1/M^2$
x_d†	$\leq 1/\sqrt{M}$	$1/\sqrt{M}$
$V_{TH} - V_{FB} - \phi_{TH}$	$1/\sqrt{M}$	$1/\sqrt{M}$
$V_{TS} - V_{FB} - 2\phi_F$	1/M	-
ΔV_T	1/M	-
α	M	-
$\beta \rightarrow C_{ox}/(1+\alpha)$	$\leq$M	M
$I_{DS} \rightarrow \beta(V_{GS} - V_T)^2$	$\leq$1/M	1/M
S	$\geq$1	1
$g_m \rightarrow \beta(V_{GS} - V_T)$	$\leq$1	1
$g_{ds} \rightarrow \lambda I_{DS}$	1	1
C_{gs}, $C_{gd} \rightarrow WLC_{ox}/(1+\alpha)$	$\leq$1/M	1/M
C_{ds}, C_j	1/M	1/M
R_i, R_{gd}, L_g	1/M	1/M
τ	1/M	1/M
f_T	M	M
$A_V = g_m/g_{ds}$	$\leq$1	1
R_g	1	1
L_g	1/M	1/M
R_s, R_d	M	M
f_{max} (at $R_g = 0$)	$1/\sqrt{M}$	$1/\sqrt{M}$
$F_{min} - 1$ (at f = ct. & $R_g = 0$)	$1/\sqrt{M}$	$1/\sqrt{M}$

† Assuming V_{BS} is constant in V_T. Otherwise, x_d scales as 1/M.

3.5.2. Scaling Rules Verification by Simulation

The scaling scheme which was developed based on the simple analytical model. is verified next by 2D numerical simulation. As pointed out recently [23], the threshold voltage V_T and the subthreshold slope S are critical parameters in estimating the scaling limits of field effect transistors. Unlike predicting the cutoff frequency, which becomes problematic below 0.25 μm gate lengths due to lack of reliable models for the energy dependence of the transport parameters in SiGe, V_T and S can be accurately determined from both DD and EB simulations. Therefore, it is justifiable to investigate the threshold voltage and the subthreshold slope of devices scaled down below 0.25 μm.

Fig.3.17 presents the gate length dependence of the subthreshold slope in a Si/SiGe/Si p-MOSFET structure which was optimized for a feature size of 0.125 μm (i.e. the gate oxide thickness was reduced to 3 nm and the substrate doping was increased to 1.2×10^{18} cm^{-3}). The actual channel lengths of the 0.1 μm and 0.125 μm devices are 0.058 μm and 0.061 μm, respectively. These channel lengths are close to the envisioned limits of conventional Si MOSFET's [31]. The calculated threshold voltage difference of 230 mV between the rectangular and the triangular channel devices is partly due to the different peak Ge composition (185 mV), and partly caused by the build-in field F_{bi} Ge profile grading has a significant impact on the subthreshold slope. S increases from 100 mV/decade for devices with triangular Ge profiles and 0.125 μm nominal gate lengths, to 120 mV/decade for the corresponding rectangular channel p-MOSFET. The grading induced built-in field delays short

channel effects by pushing carriers closer to the gate. It can be concluded that, by ramping up the Ge composition in the channel, short channel effects are reduced and the channel length of Si/SiGe/Si MOSFET's can be shrunk below 0.1 μm.

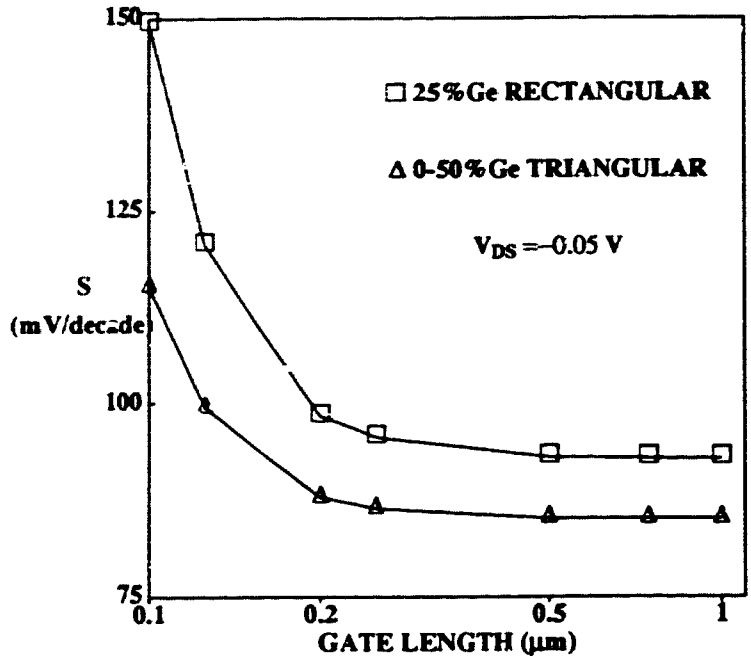

Figure 3.17: *Subthreshold slope dependence on the feature size for triangular and rectangular Ge channel profile p-MOSFET's. The vertical structure was optimized for 0.125 μm gate length.*

The gate voltage window scaling predicted in Table 3.1 is confirmed by the simulation results plotted in Fig.3.18 for devices with 0-50% Ge triangular channel profiles. The thickness of the SiGe channel is 15 nm. The results indicate that 100% hole confinement in the SiGe film is achievable for devices with 0.25 μm gate lengths if a threshold voltage of 0.5 V and a bias supply of 1.5 V are considered. Maintaining

the threshold voltage, similar confinement is expected of 0.125 μm devices with a bias supply of 1.2V. An even larger gate voltage window may be obtained if a 10nm thick, 0-70%Ge triangular channel, technologicaliy feasible, is employed.

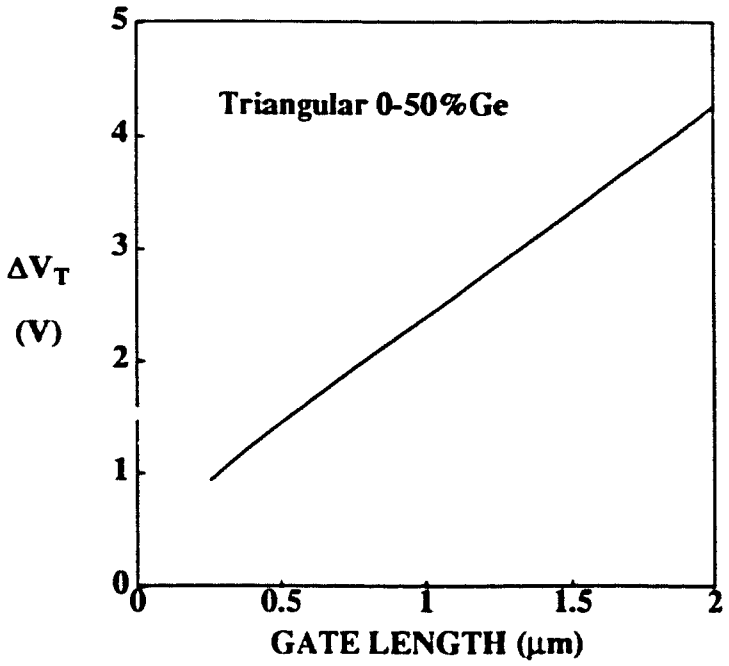

Figure 3.18: *Simulated gate voltage window scaling for p-MOSFET's with triangular Ge channel profiles.*

Fig.3.19 summarizes data referring to the dependence of the cutoff frequency of triangular channel MOSFET's on the gate length. The predicted cutoff frequency of the triangular SiGe channel p-MOSFET is only slightly below that of a type II n-MODFET [24] of identical linewidth (38 GHz as opposed to 42 GHz). This casts a favorable light on the prospect of CMOS technology in which the n and p channel devices have matched dc and ac characteristics.

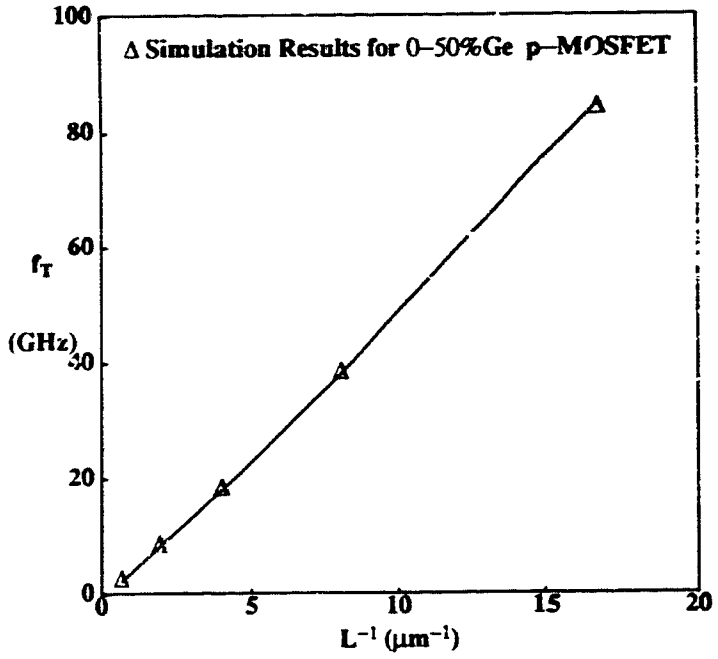

Figure 3.19: *Cutoff frequency scaling for triangular Ge channel p-MOSFET's. The simulation results are in agreement with the linear dependence of* f_T *on* L^{-1} *predicted in Table 3.1.*

Finally, the scaling of the maximum frequency of oscillation was investigated. If the contribution of the gate resistance is neglected, f_{max} is about one order of magnitude larger than f_T and scales according to the $L^{-1/2}$ law predicted in Table 3.1. However, when a realistic gate resistance R_g is considered, the maximum frequency of oscillation is severely degraded, as illustrated in Fig.3.20. The degradation is exacerbated as the device dimensions shrink. As a result, for gate lengths below 0.1 μm, f_{max} is expected to become smaller than f_T.† The reduction of R_g poses a major

† f_T is not affected by the gate resistance R_g.

problem in deep submicrometer CMOS technology. Metal, or metal-reinforced polysilicon gates [25] have to be used in conjunction with multiple-finger layout geometries in order to attenuate its impact on f_{max}.

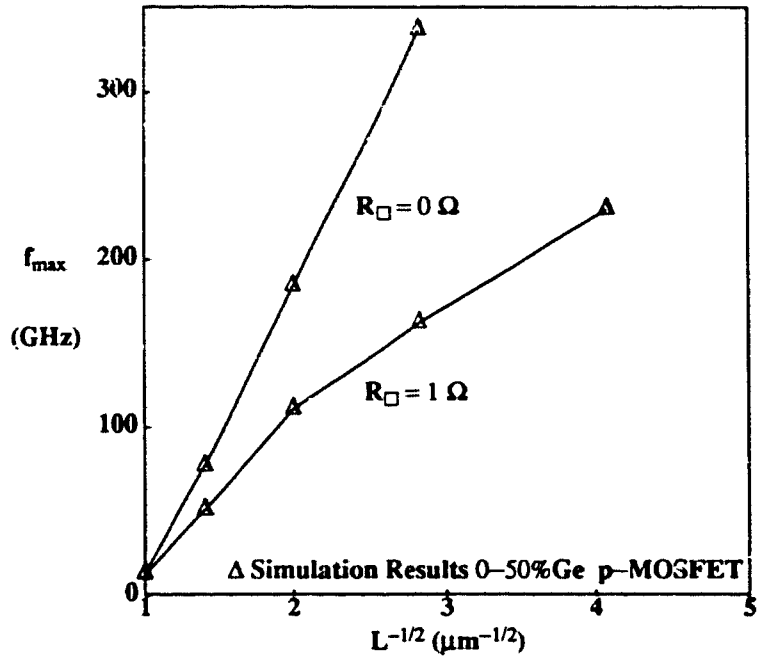

Figure 3.20: *Maximum frequency of oscillation scaling for triangular Ge channel p-MOSFET's with the gate resistance as variable parameter. The sheet resistance of the gate poly/metal* $R_\square$ *is considered as a parameter. The linear dependence on* $L^{-1/2}$ *is verified by simulation results in the ideal case* ($R_\square = 0$).

3.6. Conclusions

The performance of submicrometer Si/SiGe/Si MOSFET's was investigated using a newly developed analytical model and 2D numerical simulation. It was found that, irrespective of the Ge profile, Si/SiGe/Si p-MOSFET's, offer a number of

advantages over their Si-only counterparts: **a)** higher effective carrier mobility and velocity, **b)** reduced hot carrier effects, and **c)** easier scaling of the threshold voltage for devices which employ n^+ polysilicon gates. On the other hand, some of the problems associated with deep submicron Si MOSFET's **a)** subthreshold slope, **b)** body effect, and **c)** minimum gate length, become more severe in Si/SiGe/Si p-MOSFET's.

It was proposed that Ge profile engineering could be employed to maximize the benefits and to attenuate the problems associated with heterostructure Si/SiGe/Si MOSFET's. It was demonstrated that, by using a triangular Ge profile in the channel, the channel lengths of heterostructure MOSFET's can be shrunk below 0.1 μm, without degradation from short channel effects. The triangular SiGe channel was also found to improve the subthreshold slope, transconductance, voltage gain, cutoff frequency, maximum frequency of oscillation and the noise figure, as compared to devices with rectangular Ge profiles in the channel. This improvement is particularly significant at small effective gate voltages. Energy balance simulations revealed that hot carrier injection at the Si/SiO_2 interface was at least 50% lower in triangular than in rectangular Ge channel profile devices.

Finally, as illustrated in Fig.3.21, it may be concluded that Si/SiGe/Si p-MOSFET's, if integrated with Si n-MOSFET's in a Si/SiGe CMOS technology, can provide up to 50% improvement in the speed of the basic CMOS inverter with the additional advantage of a reduced size p-FET. This is significant in low-voltage digital and analog applications where device performance is not degraded by velocity saturation effects.

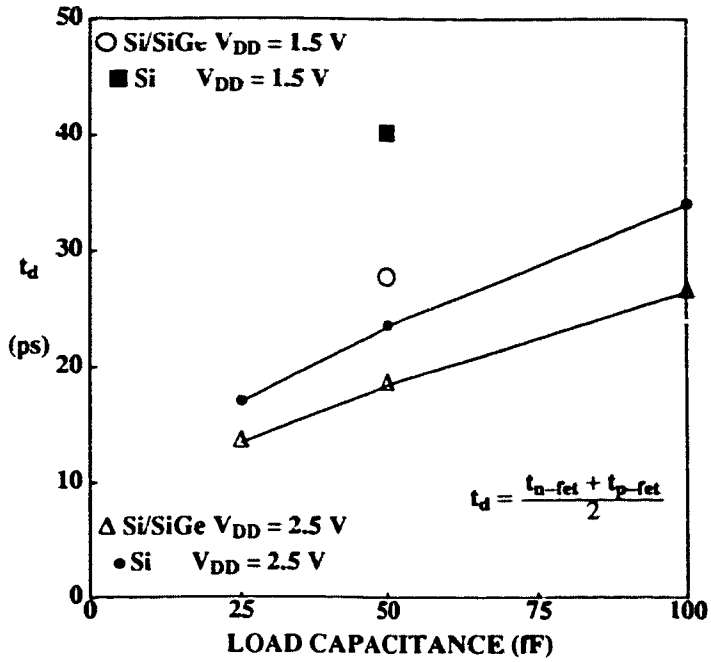

Figure 3.21: *0.25 μm Si/SiGe vs. Si CMOS inverter delay obtained by 2D mixed-mode device circuit simulation.*

References

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CHAPTER 4

Si/SiGe/Si p-MOSFET FABRICATION AND CHARACTERIZATION

4.1. Introduction

The purpose of this chapter is to provide experimental support for the concept of a Si/SiGe/Si p-MOSFET with triangular Ge channel profile, which was proposed in Chapter 3. To that end, a VLSI compatible fabrication process was developed whereby Si and Si/SiGe/Si p-MOSFET's are fabricated side by side, in separate device wells. The process features a self-aligned n^+ polysilicon gate, LOCOS isolation between devices, boron and phosphorus implants for source/drain and substrate contacts, respectively.

Section 4.2 provides a full description of the process flow and elaborates on its critical steps. The test chip and process characterization results are documented in Section 4.3, and Section 4.4, respectively. Experimental dc, low frequency and high frequency device characteristics are presented in Section 4.5. Comparisons between Si and Si/SiGe/Si p-MOSFET's, as well as between devices with rectangular and triangular Ge channel profiles are provided. Experimental characteristics of MBE and CVD grown Si/SiGe/Si p-MOSFET's are discussed. Finally, Section 4.6. summarizes the conclusions regarding the experimental results.

4.2. MBE and CVD Process Description

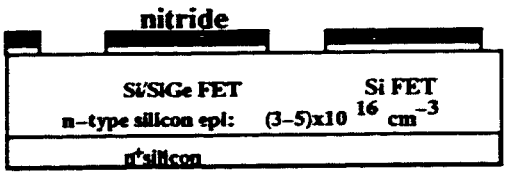
One of the most attractive aspects of SiGe devices is their potential for seamless integration in conventional silicon VLSI technology [1,2]. Both MBE† and CVD‡ Si/SiGe/Si wafers were used in the implementation of self-aligned, n^+ polysilicon gate, p-channel MOSFET's compatible with conventional CMOS technology.

4.2.1. MBE Wafers

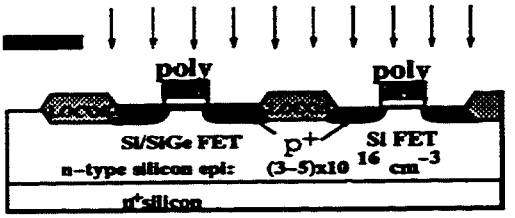
The main features of the process flow are shown in Fig.4.1. It starts with LOCOS isolation (mask #1) on 3' n/n^+ Si epitaxial wafers. The epitaxial layer is 3 μm thick and n-doped to a level of 3×10^{16} cm^{-3}. In order to accommodate Si p-MOSFET's on the same wafer with SiGe devices, the Si device wells were masked with a thermally grown, 50 nm thick SiO_2 layer (mask #2). The Si/SiGe/Si layer sandwich was then grown by MBE, all over the LOCOS patterned wafer, in the following sequence: $2\times10^{18}cm^{-3}$ δ-doped (boron) p-layer, 8 nm thick; undoped 10 nm thick Si spacer; 15 nm undoped SiGe layer and 15 nm undoped silicon cap layer. Two wafers with triangular Ge profiles and one with rectangular Ge profiles, were processed. In the case of triangular Ge profiles, the Ge mole fraction was graded over 12.5 nm, with a positive gradient, from 0% at the bottom, to 40% or 50%, respectively, at the top. In order to minimize interface scattering caused by the very abrupt Si/SiGe heterojunction, the Ge profile at the top heterojunction was retrograded over 2.5 nm from the peak value of 40% or 50% Ge to 0% Ge.

† From the National Research Council of Canada, Ottawa.

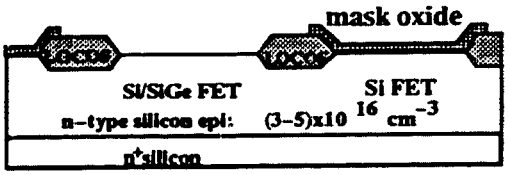
‡ From the Hewlett Packard Laboratories, Palo Alto, CA.



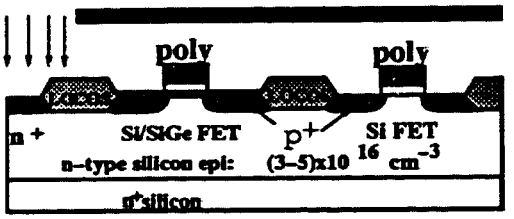
mask#1: LOCOS



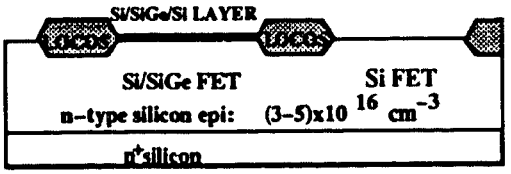
mask#5: p+ implant



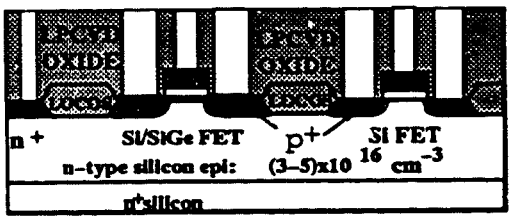
mask#2: SiGe wells



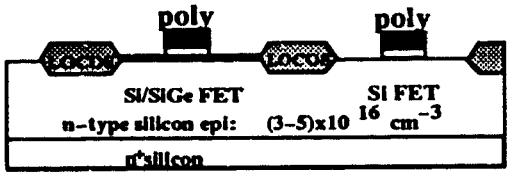
mask#6: n+ implant



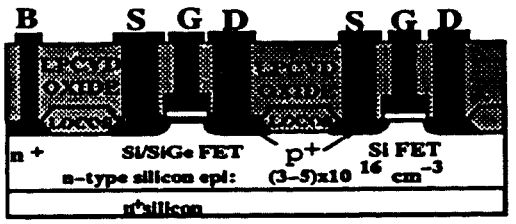
mask#3: Si wells



mask#7: contact windows



mask#4: Poly gate



mask#8: contact metal

Figure 4.1 *MBE-grown Si/SiGe/Si p-MOSFET process flow. Si p-MOSFET's were fabricated side by side with the Si/SiGe/Si devices.*

In the case of the rectangular Ge profiles, both the bottom and the top heterojunctions were graded over 2.5 nm, while the central region of the SiGe channel, 10 nm thick,

has a flat 25% Ge concentration.

The Si/SiGe/Si film was subsequently removed from above the oxide-protected Si p-MOSFET wells. The Si/SiGe/Si layers are crystalline in the device wells and polycrystalline on top of the oxide. The Si/SiGe/Si layers were delineated by using a photoresist mask (mask #3). This approach avoids degradation of the Si cap surface, and the same mask can be used to remove the protective SiO_2 layer from the Si device wells.

The 16 nm gate oxide was formed in a three step, low-thermal-budget sequence. First, an ultra thin (1-2 nm) oxide layer was grown by RTO at 850 °C for 15 s. This was immediately followed by an LPCVD step, carried out at 415 °C for 3 min. The deposition rate was 4 nm/min and the uniformity was better than 10%. Finally, a second RTO at 850 °C for 15 s was used to anneal the gate oxide. This combination of RTO and LPCVD growth was found to result in an interface trapped charge density lower than 10^{11} $cm^{-2}eV^{-1}$ [3]. Repeated experiments have indicated that the first RTO was responsible for a 50% reduction in both the fixed and the interface trapped charge. About 7 nm of the silicon cap layer thickness were consumed during oxidation and during the two RCA cleans prior to gate oxide formation.

The remainder of the process closely follows a typical, self-aligned n^+-poly gate MOS process. The gate poly was deposited by LPCVD, at 625 °C, in two steps. An undoped, 80 nm thick, polysilicon film - employed as a buffer to stop the diffusion of impurities into the gate oxide - was followed by the deposition of an *in situ* doped, 440 nm thick, n-type polysilicon layer. The polysilicon layer was implanted

with phosphorus ($5\times10^{15}cm^2$, 40 keV) to further reduce the sheet resistivity and to prevent the subsequent source/drain boron implant from changing the sign of the net dopant concentration in the gate. The gates were then patterned (mask #4) by dry-etching.

Next, the source and drain contact regions were implanted with boron ($5\times10^{15}cm^2$, 100 keV) to obtain a 0.45 μm deep junction. The substrate contact windows were covered with photoresist (mask #5) during the boron implantation. A second phosphorus implant ($5\times10^{15}cm^2$, 80 keV) was performed in order to dope the substrate contact region (and the Si n-MOSFET source/drain regions if required). A single 15 s anneal at 800 °C was used to activate the n^+ poly gates, boron (source/drain) and phosphorus (substrate) implants. Finally, Al-Si contacts were deposited, patterned and annealed at 425 °C for 20 min in forming gas.

4.2.2. CVD Wafers

Si/SiGe/Si p-MOSFET's were also fabricated on blanket CVD-grown wafers [4]. Germanium and boron profiles were similar to those in the MBE-grown wafers. In this case, the final silicon cap layer thickness was reduced to about 2 nm from an initial value of 8 nm. Isolation between devices was provided by an 800 nm thick RTO/LPCVD/RTO field oxide. After growing the gate oxide to a thickness of 10 nm, the CVD and MBE wafers were processed together. No Si devices were fabricated on the blanket CVD wafers.

4.2.3. Critical Processing Steps

The critical steps in the fabrication process are **a)** the selective growth/removal of the Si/SiGe/Si layers in the p-channel device wells [4]; **b)** the precise control of the silicon cap layer thickness during the processing steps preceding the polysilicon gate deposition [5]; **c)** the growth of a thin, high quality gate oxide within a strict thermal budget [6,7]; **d)** preventing the outdiffusion of boron from the δ-doped layer into the SiGe channel during the two thermal steps, i.e. gate oxide growth and implant anneal [5].

It is now generally accepted that boron outdiffusion poses a more stringent constraint on the overall thermal budget of the process than strain relaxation in the SiGe film [5]. The last two of the difficulties mentioned above are no longer confined to SiGe processing. In fact they are now typical for state of the art Si VLSI processes.

4.3. Test Chip Description

The test chip was laid out using 3 μm layout rules and contains process test inserts as well as MOSFET's. The process test inserts include on-wafer standards for de-embedding of the transistor S parameters, one heterostructure MOS capacitor for material, process and device characterization, transmission line patterns for sheet resistivity measurements of the boron and phosphorus implanted regions, and a cross pattern for assessing the resistance of the polysilicon gate [8]. The following is a description of the transistors included in the test chip.

(i) Four interdigitated gate 3×290 μm Si/SiGe/Si p-MOSFET's for dc and high fre-

quency (S-parameter) measurements and one Si p-MOSFET of identical layout. These devices have 110×110 μm input and output pads laid-out for S parameter probing using the signal-ground (SG) probes, as shown in Fig.4.2.

Figure 4.2 *Photomic..)graph of a fabricated 3×290μm Si/SiGe/Si p-MOSFET with interdigitated gate (six gate fingers, each 48 μm long).*

(ii) One π-shaped gate 3×180 μm Si/SiGe/Si p-MOSFET for dc and high frequency (S-parameter) measurements and an identical Si p-MOSFET, located side by side on the layout. These devices have 50×50 μm input and output pads laid-out for S parameter prcbing using the ground-signal-ground (GSG) coplanar probes.

(iii) Four π-shaped gate, 180 μm wide Si/SiGe/Si p-MOSFET's with 2 μm, 4 μm, 8 μm and 16 μm gate lengths. These devices have 110×110 μm input and output pads laid-out for S parameter probing using the ground-signal-ground (GSG) coplanar probes. However, they are primarily intended for the extraction of the

effective gate length from dc measurements.

(iv) One long and wide (FATFET) 100×100 μm Si/SiGe/Si p-MOSFET, with 110×110 μm input and output pads, intended for C-V and mobility profiling.

4.4. Process Characterization

Five wafers (three MBE and two CVD) were used in the fabrication process. The process parameters such as the gate oxide thickness, Si cap layer thickness and substrate doping were measured using the C-V technique discussed in Chapter 2. The sheet resistivity of the n^+ implant, p^+ implant and n-poly gate were characterized using transmission line measurements [8]. Table 4.1. summarizes the process parameters for the five wafers in question.

TABLE 4.1: PROCESS CHARACTERIZATION DATA

Wafer / Parameter	#21 MBE	#23 MBE	#24 MBE	#89-2 CVD	#90-2 CVD
Ge Profile	○ 0-40%	□ 25%	△ 0-50%	▲ 0-50%	■ 25%
Gate Oxide Thickness (nm)	16	16	16	10	10
Si Cap Thickness (nm)	8	8	8	2	2
Substrate Doping (cm^{-3})	3×10^{16}	3×10^{16}	3×10^{16}	8×10^{16}	8×10^{16}
L_{MASK} (μm)	3	3	3	3	3
L_{EFF} (μm)	1.8	1.7	1.8	1.8	1.8
S/D Junction Depth (μm)	0.52	0.52	0.52	0.52	0.52
B Implant Sheet Resistance (Ω/□)	330	320	330	340	360
S/D Contact Resistance (Ω*μm)	1150	1100	1050	1100	3400†
P Implant Sheet Resistance (Ω/□)	2	2	2	2	2
Gate Poly Sheet Resistance (Ω/□)	780	780	780	770	770

† Caused by contact window alignment problems, as a result of the wafer being broken during transportation to and from the implant center in California.

The low resistivity of the n^+ substrate contact implant is an indication that the single implant anneal is sufficient for activation. The relatively large sheet resistance in the source/drain regions is the result of using a single deep boron implant, rather than the more common dual implant, involving both a deep boron implant and a surface BF^+_2 implant. Even so, because of the high temperature at which the Al contacts have been sintered, the contact resistance is low (1050 Ωμm). This figure compares favorably with those reported for state of the art Si p-MOSFET's.

The gate poly resistance is also larger than expected, but, except for the maximum frequency of oscillation and the noise figure, it has a minor impact on device characteristics. The gate resistance can be reduced by more than one order of magnitude if the gate is protected with a thicker oxide during the source/drain boron implant and if the undoped polysilicon layer in the vicinity of the gate oxide is *in situ* doped.

Finally, Ge profiles in the fabricated MOSFET channels were verified using Auger Electron Spectroscopy (AES). The experimental AES profiles are shown in Figs.4.3 and 4.4 for MBE and CVD wafers, rerspectively. These results confirm that the peak Ge mole fraction is approximately two times larger in the wafers with triangular Ge profiles as compared to those with rectangular profiles. The Ge profile is graded both at the top and at the bottom heterojunction, thereby reducing interface scattering.

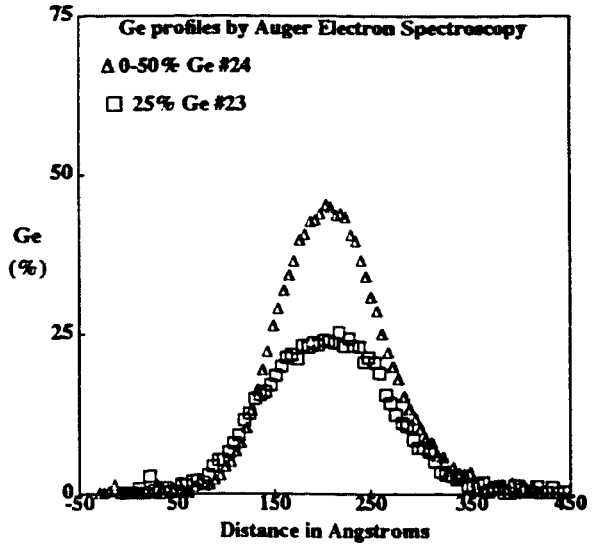


Figure 4.3 *Experimental MBE grown Ge profiles obtained by Auger Electron Spectroscopy (AES) with a depth resolution of 0.5 nm.*

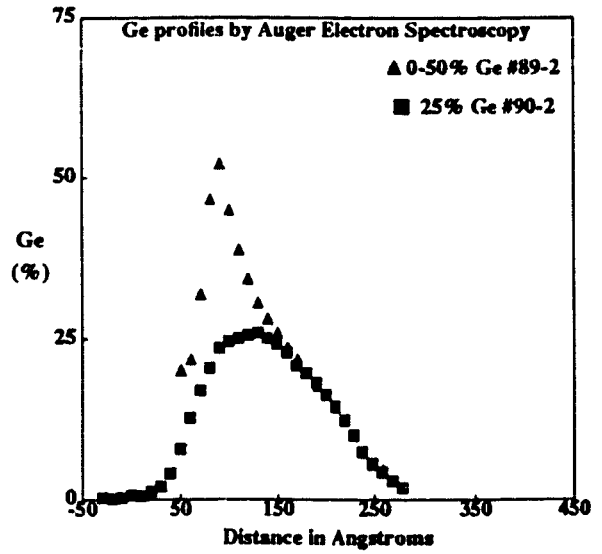


Figure 4.3 *Experimental CVD grown Ge profiles obtained by Auger Electron Spectroscopy (AES) with a depth resolution of 0.5 nm.*

4.5. Device Characterization

In order to confirm the performance leverage expected for devices with triangular Ge channel profiles, the dc, low frequency and high frequency characteristics of both long (100×100μm) and short (3×100μm) channel transistors were measured.

4.5.1. C-V Characteristics and Mobility Profiling

C-V characteristics are illustrated in Fig. 4.5 for MBE MOSFET's with three different Ge profiles in the channel. Note that there is no "plateau" region in the case of the device with a rectangular Ge channel profile. Instead, a change of slope can be observed. Similar characteristics have been reported recently by IBM for a device with a trapezoidal profile and a peak Ge concentration of 25% [5]. In the case of the present, triangular 0-40% Ge profile devices, a narrow "shoulder" region, corresponding to the gate voltage window, becomes apparent on the C-V characteristics. The gate voltage window widens to about 2.5 V for the device with triangular 0-50% Ge profile. These results provide solid experimental support for the theoretical prediction that the gate voltage window and, hence, carrier confinement, depend on the Ge concentration at the top of the channel and not on the total Ge dose.

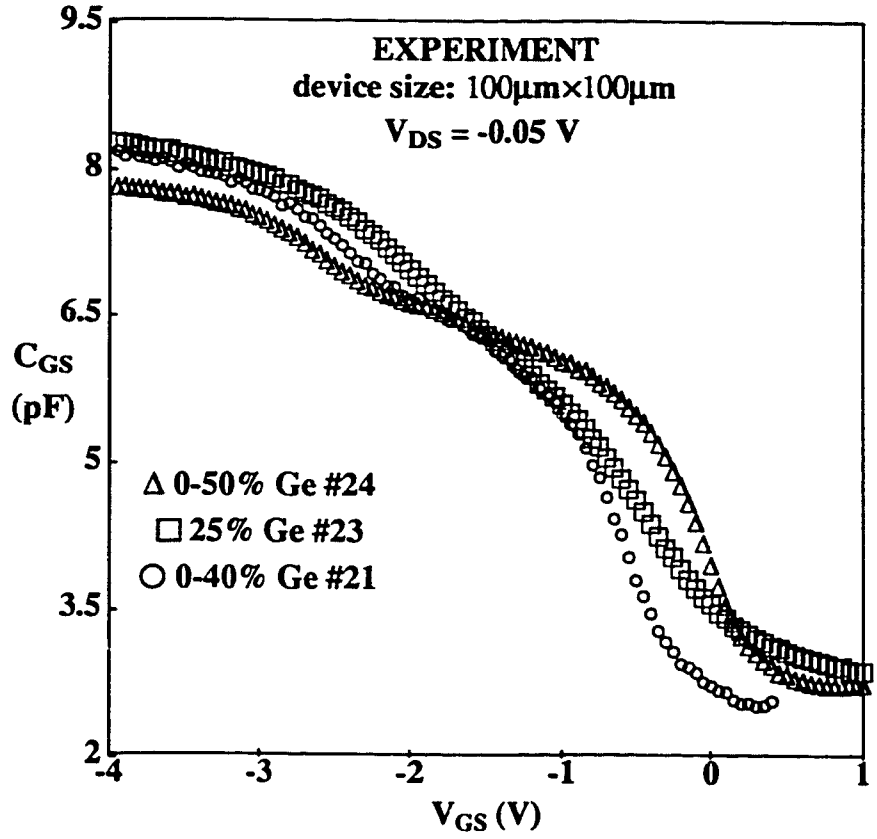


Figure 4.5 *Comparison of the gate to source capacitance characteristics for different Ge profiles as measured on the FATFET in the linear region* V_{DS} *= -0.05 V.*

The C-V measurements were combined with the linear region transconductance measurements, carried out on the FATFET and shown in Fig. 4.6, to obtain the effective mobility versus gate voltage characteristics. The latter are compared in Fig.4.7 for two MBE grown Ge profiles. The measured hole mobility increases from 250 cm^2/Vs in a rectangular 25%Ge MOSFET, to 400 cm^2/Vs for a device with triangular 0-50% Ge profiles.

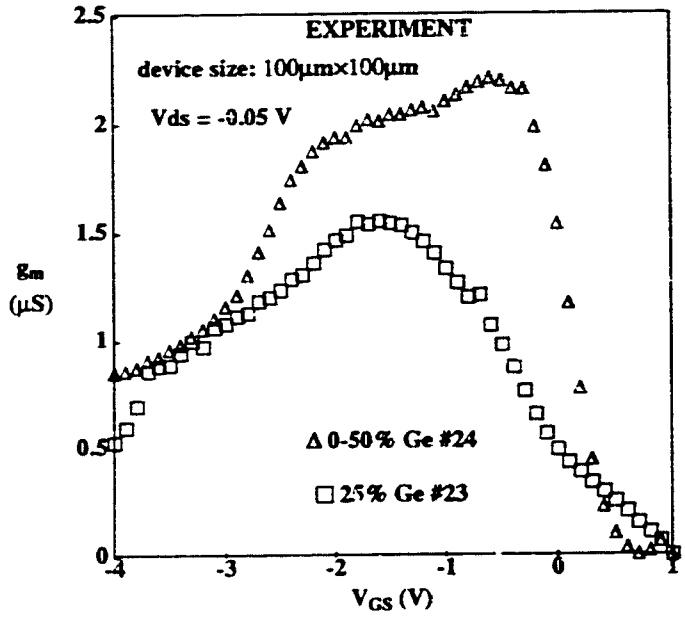


Figure 4.6 *Comparison of the transconductance characteristics for different Ge profiles as measured on the FATFET, in the linear region at* V_{DS}*=-0.05 V.*

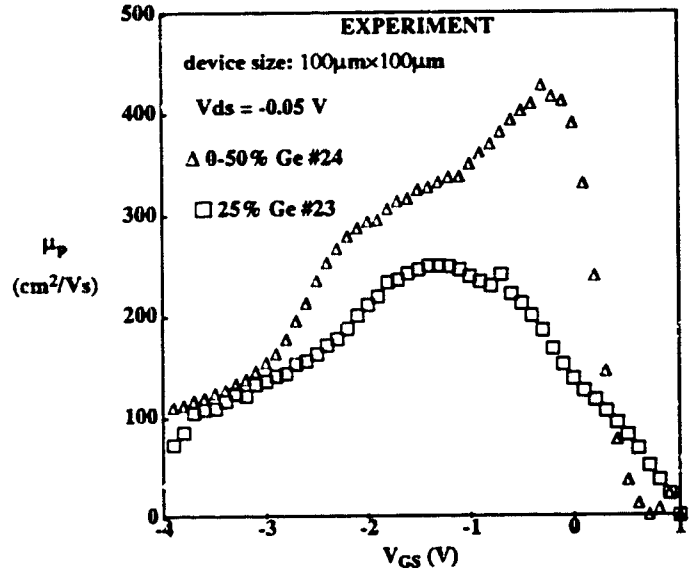


Figure 4.7 *Comparison of the mobility versus gate voltage characteristics for different Ge profiles as measured on the FATFET, in the linear region at* V_{DS}*=-0.05 V.*

The large Ge mole fraction and the grading of the top Si/SiGe interface over 2.5 nm (thereby reducing interface scattering), are responsible for the large hole mobility. This is the first experimental proof that the mobility of holes in type I Si/SiGe/Si channels improves as the Ge concentration is increased. The 400 cm^2/Vs figure is a record for this heterostructure alignment, and indicates a factor of 2.6 improvement over the room temperature hole mobility in Si p-MOSFET's, typically 150 cm^2/Vs.

It should be emphasized that, with the mobility measurement technique used, variations of the oxide thickness from wafer to wafer are cancelled out. Also, as a result of the large gate length (100 μm), wafer to wafer variations in the effective channel length are negligible. In addition, unlike the split C-V method [5] which relies on dc I-V measurements and on the integral of the C-V characteristics to determine the mobility, the technique employed in this work is not prone to errors introduced by interface traps. The immunity to errors caused by interface traps stems from the ac nature of the measurements and from the fact that the presence of interface traps leads to identical shifts in the C-V and g_m-V characteristics. These shifts are cancelled out when the hole mobility is extracted from the ratio of transconductance and capacitance.

Dwelling further on the linear transconductance and mobility characteristics, it is important to note the steeper slope of the transconductance characteristics, immediately above threshold, for the device with triangular Ge profile. As explained in Chapter 3, the built-in grading field is primarily responsible for this behavior. At the same time, the slow increase in transconductance in the case of the rectangular Ge

profile is also the result of the poorer separation between the carriers in the channel and the impurities located in the δ-doped layer.

4.5.2. Current Voltage Characteristics

Typical transfer characteristics from Si and Si/SiGe/Si devices with rectangular and triangular channel profiles are shown in Fig. 4.8. The effective channel length for these MOSFET's is 1.8 μm, as determined from saturation current measurements on devices with different gate lengths and identical gate widths.

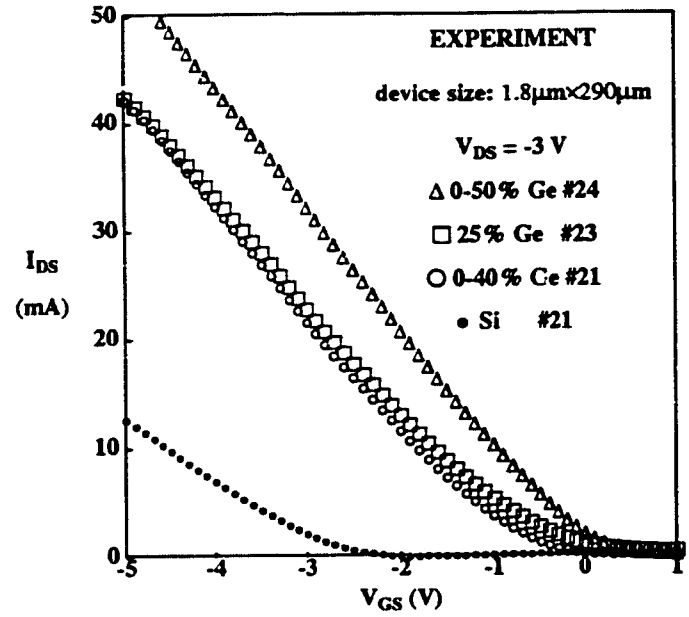


Figure 4.8 *Comparison between the transfer characteristics of Si, triangular and rectangular Ge channel profile Si/SiGe/Si p-MOSFET's with 1.8 μm channel lengths.*

A threshold voltage shift of about 2 V, is easily distinguishable between the Si p-MOSFET and all the Si/SiGe/Si p-MOSFET's. The most important contribution to

the threshold shift is due to the δ-doped layer, while up to 0.35 V is caused by the valence band offset at the top Si/SiGe heterojunction. Because of the larger hole mobility and better carrier confinement in the SiGe channel, the MOSFET with triangular 0-50% Ge channel profile exhibits the largest current driving capability and gain factor.

Despite its higher peak Ge concentration, the I-V characteristics of the triangular 0-40% Ge MOSFET are comparable to those of the device with rectangular 25% Ge channel profile. The lower total Ge dose and a smaller δ-doped region dose (that can be inferred from the threshold voltage) are responsible for this behavior. Even so, the gain factor β is slightly larger than that of the rectangular Ge channel MOSFET.

The output characteristics of Si and Si/SiGe/Si p-MOSFET's are presented in Figs.4.9 and 4.10, respectively. As expected, the drain current of the Si/SiGe/Si p-MOSFET is larger than that of the Si one. Drain breakdown voltage occurs at around 9 V, for both devices, and it is caused by the breakdown of the gate oxide, rather than by drain/substrate junction breakdown. The smaller bandgap of the SiGe channel has little bearing on the breakdown voltage. This is in line with simulation results which indicate that the highest electric field inside the semiconductor part of the device is located primarily in the silicon region.

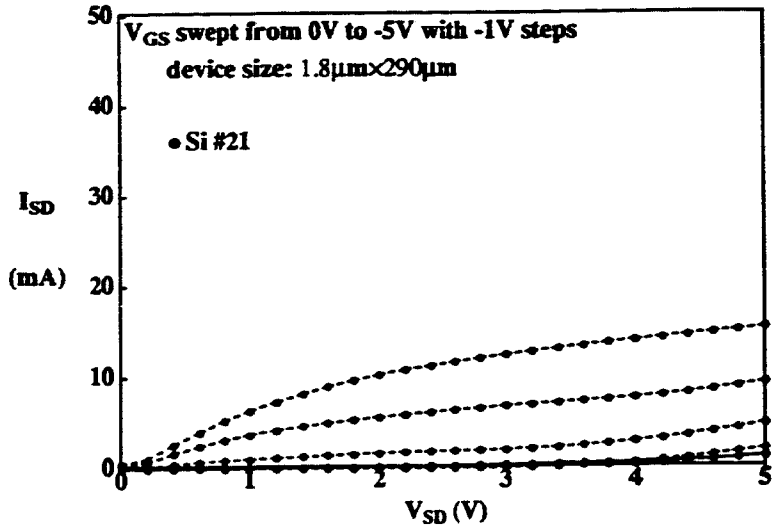


Figure 4.9 *Output characteristics of a Si p-MOSFET fabricated on the MBE wafers.*

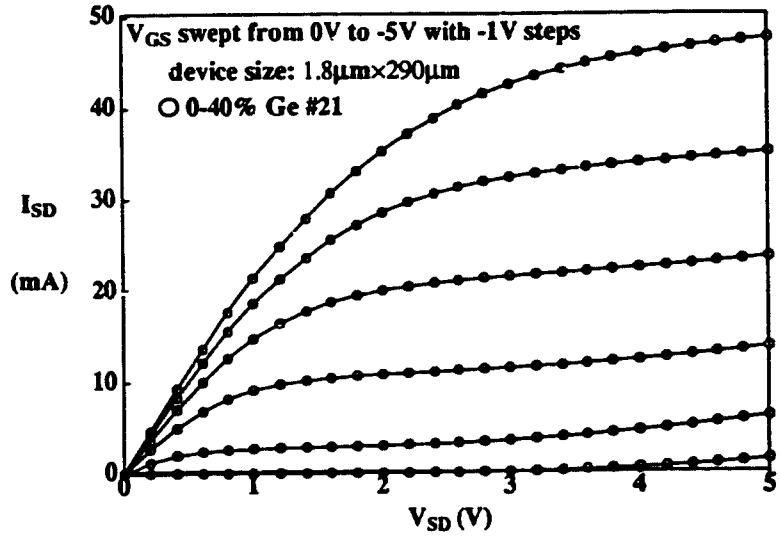


Figure 4.10 *Output characteristics of a Si/SiGe/Si p-MOSFET's with triangular 0-40% Ge profile fabricated side by side with the Si device presented in Fig.4.9.*

4.5.3. Transconductance and Output Conductance

For Si/SiGe/Si MOSFET's with 1.8 μm channel lengths, typical, peak transconductance values, measured in the saturation region at V_{GS} = - 2.5 V and V_{DS} = - 2.5 V, vary between 30 and 40 mS/mm. The largest figure was obtained for devices with triangular 0-50% Ge channel profiles. Fig.4.11. illustrates that the peak transconductance increases by 20% when switching from a rectangular to a triangular Ge profile. However, the improvement is as high as 100% if the device is biased at an effective gate voltage (V_{GS} - V_T) of up to 1.5 V. Such bias conditions are common in low-voltage/low-power applications.

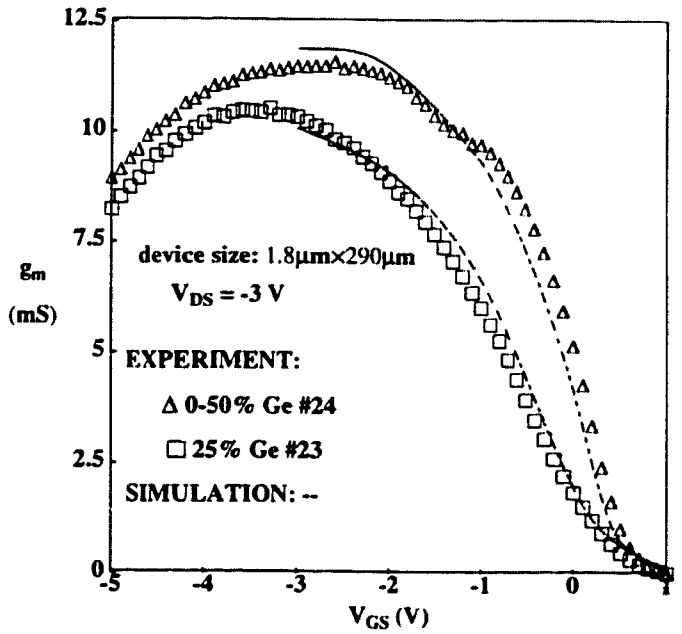


Figure 4.11 *Comparison of the measured and simulated transconductance for triangular and rectangular Ge profile Si/SiGe/Si p-MOSFET's.*

A comparison of the transconductance characteristics of Si and Si/SiGe/Si devices is shown in Fig.4.12. Si MOSFET's systematically revealed a 50% lower transconductance of around 20 mS/mm. As a reference, the transconductance of Si p-MOSFET's in a state of the art, 0.8 μm BiCMOS process is 40 mS/mm. These results dispel any doubts that may have lingered about the prospects of delivering excellent Si/SiGe/Si p-MOSFET's, without degrading the performance of the Si MOSFET's fabricated on the same chip.

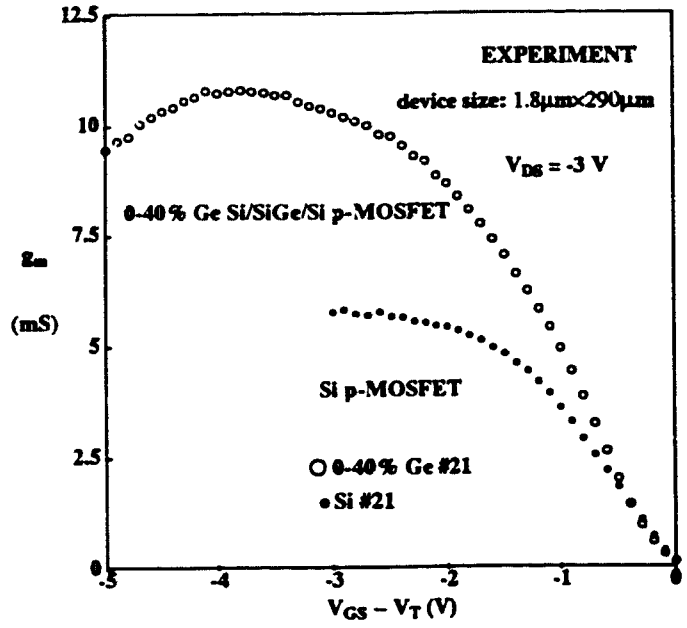


Figure 4.12 *Comparison of the transconductance of Si and triangular 0-40% Ge profile Si/SiGe/Si p-MOSFET's fabricated side by side, on the same wafer.*

Fig. 4.13. shows the output conductance of a CVD grown Si/SiGe/Si p-MOSFET with triangular Ge profile. Because of the larger substrate doping (8×10^{16}, as opposed to 3×10^{16} cm^{-3}) and because of the thinner gate oxide (10 nm, as opposed to

16 nm), the CVD device has a smaller output conductance in the saturation region than the equivalent MBE MOSFET. The small signal, intrinsic voltage gain g_m/g_{ds} in deep saturation is 30.

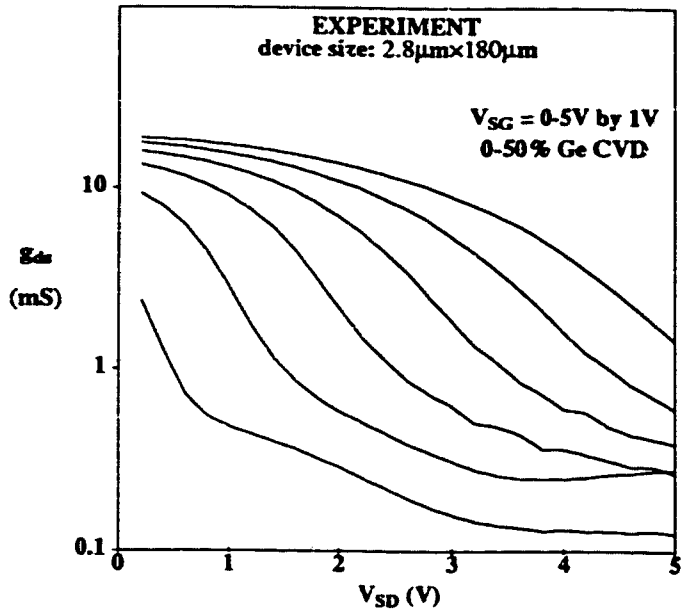


Figure 4.13 *Output conductance of a CVD grown Si/SiGe/Si p-MOSFET with triangular 0-50% Ge profiles.*

4.5.4. High Frequency Characteristics

On-wafer S parameter measurements were carried out in order to assess the high frequency performance. The effect of the parallel and series parasitics, associated with the pads, was eliminated by employing a three-step de-embedding algorithm [9]. On-wafer input and output shorts, through, and dummy open devices have been measured and included in the de-embedding procedure. Typical, de-embedded

current gain versus frequency characteristics are shown in Fig.4.14 for Si/SiGe/Si and Si MOSFET's with 1.8μm channel lengths. The cutoff frequency of the 0-40% Ge MOSFET is 1.1 GHz, while that of the Si device is 0.8 GHz.

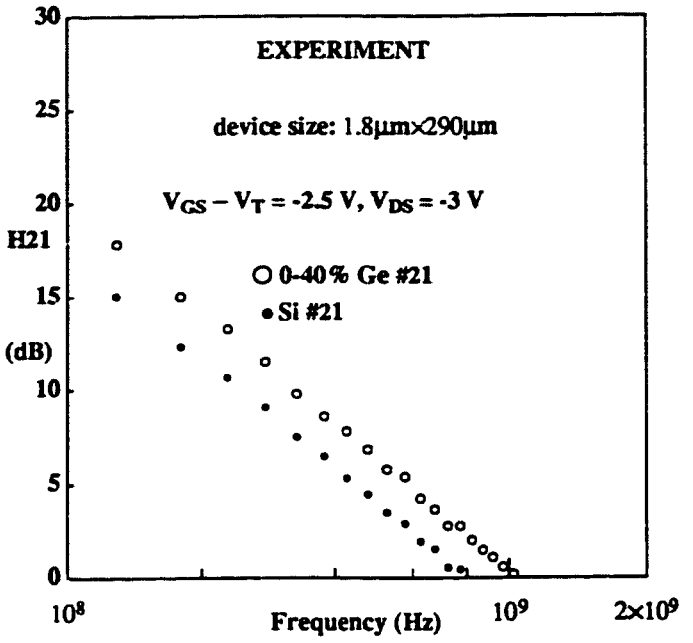


Figure 4.14 *Comparison of the current gain vs. frequency characteristics of Si and Si/SiGe/Si p-MOSFET's.*

These experimental results were obtained for both interdigitated and π-shaped gate devices with gate widths of 290 μm and 180 μm, respectively. They are in good agreement with numerical simulations, which predict a cutoff frequency of 1.2 GHz for the Si/SiGe/Si MOSFET. As a result of the parasitic capacitance associated with the relatively large (0.75 μm) gate overlap of the source/drain regions, the improvement in the cutoff frequency from the Si to the Si/SiGe/Si MOSFET's is not as impressive as that seen in transconductance. This can be remedied if more

sophisticated photolithography and dry-etching techniques are employed.

Finally, Fig. 4.15 presents a comparison between the cutoff frequency characteristics of Si/SiGe/Si p-MOSFET's with triangular and rectangular Ge channel profiles.

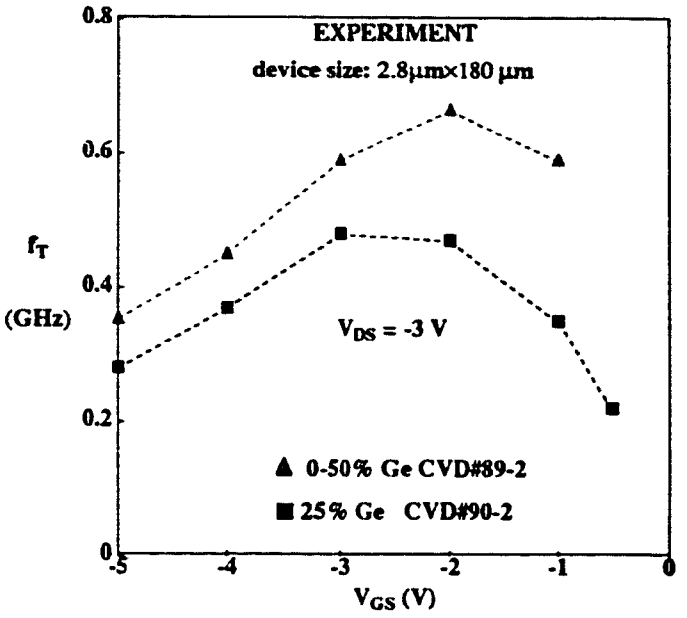


Figure 4.15 *Comparison of cutoff frequency of CVD grown Si/SiGe/Si p-MOSFET's with rectangular and triangular Ge profiles.*

The peak cutoff frequency is at least 20% larger for devices with triangular profiles, irrespective of the growth technique. This is in confirmation of the results obtained from mobility profiling measurements. Cutoff frequency, which depends on hole mobility, is larger in devices with triangular Ge profiles in the channel.

4.6. Conclusion

A VLSI compatible Si/SiGe/Si p-MOSFET process was developed to implement the first MBE and CVD-grown Si/SiGe/Si p-MOSFET's with triangular Ge profiles in the channel. The measured dc, ac and high frequency characteristics of these devices demonstrate the largest reported improvement in the room temperature performance of type I Si/SiGe/Si p-MOSFET's over Si p-MOSFET's fabricated on the same wafer. It has also been shown that, by employing a triangular Ge profile in the channel, peak Ge mole fractions as high as 50% become experimentally feasible, leading to increased carrier confinement, mobility, transconductance and cutoff frequency, as compared to MOSFET's with rectangular Ge channel profiles. These experiments prove that Si/SiGe/Si p-MOSFET's can be seamlessly integrated into a Si CMOS process.

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CHAPTER 5

CONCLUSIONS

5.1. Thesis Summary

The focus of this thesis has been the theoretical and experimental study of Si/SiGe/Si p-channel MOSFET's. Its goal was to find a practical solution, within the bounds of conventional silicon VLSI technology, that allowed for a sizable increase in the mobility of holes in the SiGe channel and thereby enhancing the performance of the p-MOSFET to match that of the corresponding n-channel device. As a prerequisite in the understanding of the operation of the Si/SiGe/Si p-MOSFET, the study and modeling of the heterostructure MOS capacitor was undertaken in Chapter 2. The outcome of the capacitor investigation was the development of a technique to characterize the parameters of the Si/SiGe layer sandwich based on C-V measurements. A triangular Ge channel profile was proposed in Chapter 3 as the optimal solution to the thesis objectives. The performance of the triangular Ge channel profile Si/SiGe/Si p-MOSFET was then thoroughly investigated based on analytical models and comprehensive two-dimensional numerical simulations. Finally, in Chapter 4, the concept was experimentally verified through dc, low frequency and high frequency measurements on Si and Si/SiGe/Si p-MOSFET's with both triangular and rectangular Ge channel profiles, fabricated in-house, using a VLSI compatible process, which allowed for the integration of Si and Si/SiGe/Si transistors on the same chip. Highest

reported hole mobilities and a factor of two improvement in transconductance were obtained as compared to conventional Si p-MOSFET's, making the proposed structure a potential solution to the implementation of a high performance Si/SiGe CMOS/BiCMOS process.

5.2. Thesis Contributions

A series of original, theoretical and experimental contributions were made, including:

(i) the design and fabrication of a VLSI compatible Si/SiGe/Si p-MOSFET with a triangular Ge profile in the channel;

(ii) the development of a model to describe the characteristics of the heterostructure MOS capacitor and of an experimental technique for the characterization of Si/SiGe layers based on C-V measurements;

(iii) the development of an experimental technique for profiling the hole mobility in SiGe channels;

(iv) a complete theoretical treatment, including scaling, of Si/SiGe/Si p-MOSFET's using both analytical models and 2D numerical simulations;

(v) demonstration of a sizable increase in the mobility of holes in type I Si/SiGe/Si p-MOSFET's through the use of triangular (420 cm^2/Vs), as opposed to rectangular (250 cm^2/Vs), Ge profiles;

(vi) a factor of two increase in the transconductance of Si/SiGe/Si p-MOSFET's with respect to equivalent Si p-MOSFET's.

5.3. Suggestions for Future Work

Further theoretical work is necessary in order to elucidate a number of issues which have not been treated in this thesis. First, the topic of velocity overshoot effects in deep submicron SiGe channels and the energy dependence of the transport properties of SiGe need additional investigation. Even though good device design can be relied upon to make the most of the higher hole mobility typical of SiGe channels, performance in the deep submicron regime is ultimately limited by velocity saturation effects. Therefore, the way in which SiGe material properties and device dimensions interplay in the sub-tenth micrometer realm will undoubtedly influence the long term prospects of Si/SiGe/Si as a viable, "industrial" quality device.

Second, a complete, compact, SPICE model that would augment the model equations of Section 3.3 with analytical expressions to describe the small signal model parameters, is urgently required in order to facilitate the design of large circuits and systems in this technology. A large body of circuit performance data is necessary before the true benefits of Si/SiGe/Si p-MOSFET's can be appreciated.

In terms of experimental investigations, several problems should be pursued. First, a simple and useful endeavor would be the fabrication of a Si/SiGe/Si p-MOSFET with a 0-70%Ge triangular channel. Such a device is technologically feasible if the channel is 10 nm thick and should provide even larger hole confinement and hole mobility than the devices reported in this thesis.

Second, with one addition (a p-well) to the experiments performed in this thesis, a Si/SiGe CMOS fabrication process can be implemented, whereby the Si/SiGe/Si p-

MOSFET is integrated with a conventional Si n-MOSFET to obtain symmetrical n and p-channel characteristics. As a result of its significant area savings and improved speed, such a process would be extremely useful for digital applications.

Third, a reliability study of Si/SiGe MOSFET's and HBT's should be undertaken in order to more realistically assess the long term impact of Si/SiGe device integration into large circuits and systems.

Last and most challenging, as an ultimate goal of Si and SiGe device integration, a Si/SiGe BiCMOS process could be conceived that would feature Si/SiGe/Si npn HBT's, Si/SiGe/Si p-MOSFET's and Si n-MOSFET's. This would require two selective epitaxial Si/SiGe layer growths, the first for the channel of the p-MOSFET and the second for the base of the HBT. This, too, appears technologically feasible with state of the art technology. Such a Si/SiGe BiCMOS process would be useful for analog and RF applications, where the p-channel device limits circuit performance.

Appendix A

Analytical Solution to Poisson's Equation

This appendix presents a complete analytical derivation of the semiconductor charge, threshold voltages and semiconductor capacitance for a Si/SiGe MOS capacitor.

A.1 Derivation of the semiconductor charge Q_T

To calculate the semiconductor charge, the approach used for conventional MOS capacitors is taken but the position-dependent semiconductor material composition is accounted for. The hole and electron concentrations are expressed as

$$p(x) = N_B \exp\left[\frac{2q\phi_F + \Delta E_G(x) - q\phi(x)}{KT} - \ln\left[\frac{N_{VSi}}{N_{VSiGe}}\right]\right] \tag{A1}$$

$$n(x) = N_B \exp\left[\frac{\phi(x)}{\phi_T}\right] \tag{A2}$$

Poisson's equation can be cast in the following form

$$\frac{d}{dx}\left[\varepsilon(x)\frac{d\phi(x)}{dx}\right] = -qN_B\left[\frac{N(x)}{N_B} - e^{\frac{\phi}{\phi_T}} + e^{\frac{2\phi_F + \frac{\Delta E_V}{q}}{\phi_T}}\left[e^{-\frac{\phi}{\phi_T}} - \frac{N(x)}{N_B}\right]\right] \tag{A3}$$

By multiplying both sides of Poisson's equation with $2\varepsilon\frac{d\phi(x)}{dx}$, one obtains

$$\frac{d}{dx}\left[\varepsilon(x)\frac{d\phi(x)}{dx}\right]^2 = -2qN_B\varepsilon(x)\frac{d\phi(x)}{dx}\left[\frac{N(x)}{N_B} - e^{\frac{\phi}{\phi_T}} + e^{\frac{2\phi_F + \frac{\Delta E_V}{q}}{\phi_T}}\left[e^{-\frac{\phi}{\phi_T}} - \frac{N(x)}{N_B}\right]\right] \tag{A4}$$

Since in most of the SiGe layer the potential ϕ is a linear function of x, the position-

dependent valence band offset and the permittivity in the SiGe layer can be described by linear functions of the potential ϕ

$$\Delta E_V(\phi) = \Delta E_{VH} - \frac{F_{bi}}{F_{bo}}\phi \tag{A5}$$

$$\varepsilon(\phi) = \varepsilon_{SiGe_H} - \varepsilon_1\phi \tag{A6}$$

where F_{bo} is the electric field at the bottom of the SiGe film (to be derived later), and

$$\varepsilon_1 = \frac{4.2\delta Y_{bo}}{F_{bo}}$$

The LHS, and RHS of eqn. (A4) can be integrated with respect to $\left[\varepsilon(x)\frac{d\phi(x)}{dx}\right]^2$, and ϕ, respectively. After applying the Neumann boundary conditions in the bulk of the semiconductor

$$\varepsilon_{Si}\frac{d\phi(x)}{dx}\Big|_{x=\infty} = 0, \quad \phi\Big|_{x=\infty} = 0$$

the total semiconductor charge at the Si/SiO_2 is obtained

$$Q_T^2 = \left[\varepsilon_{Si}\frac{d\phi(x)}{dx}\right]^2\Bigg|_{x=0} = 2q\varepsilon_{Si}N_B\phi_T f(\phi_S) \tag{A7}$$

where

$$f(\phi_S) = e^{\frac{\phi_S}{\phi_T}} - 1 - \left[\frac{\phi_\delta}{\phi_T} + \frac{N_\delta}{N_B \phi_T}(\phi_\delta - \phi_{bu})\right]\left[1 - e^{\frac{2\phi_F}{\phi_T}}\right] + e^{\frac{2\phi_F}{\phi_T}}\left[e^{-\frac{\phi_S}{\phi_T}} - 1\right] \quad (A8)$$

$$(R_{\epsilon H} - 1)e^{\frac{\phi_H}{\phi_T}} - e^{\frac{2\phi_F - \phi_H}{\phi_T}} + \frac{R_{\epsilon H}}{1+\frac{F_{bi}}{F_{bo}}}e^{\frac{\phi_{TH} - \phi_H}{\phi_T}} - (R_{\epsilon bo} - 1)e^{\frac{\phi_{bo}}{\phi_T}} + e^{\frac{2\phi_F - \phi_{bo}}{\phi_T}} - \frac{R_{\epsilon bo}}{1+\frac{F_{bi}}{F_{bo}}}e^{\frac{\phi_{Tbo} - \phi_{bo}}{\phi_T}} -$$

$$\frac{\epsilon_1}{\epsilon_{Si}}\left[(\phi_H - \phi_T)e^{\frac{\phi_H}{\phi_T}} + \left[\phi_H - \frac{\phi_T}{1+\frac{F_{bi}}{F_{bo}}}\right]\frac{e^{\frac{\phi_{TH} - \phi_H}{\phi_T}}}{1+\frac{F_{bi}}{F_{bo}}} - (\phi_{bo} - \phi_T)e^{\frac{\phi_{bo}}{\phi_T}} - \left[\phi_{bo} - \frac{\phi_T}{1+\frac{F_{bi}}{F_{bo}}}\right]\frac{e^{\frac{\phi_{Tbo} - \phi_{bo}}{\phi_T}}}{1+\frac{F_{bi}}{F_{bo}}}\right]$$

$R_{\epsilon H} = \frac{\epsilon_{Si}}{\epsilon_{SiGe_H}}$ is the ratio of semiconductor permittivities in silicon, and at the top of the SiGe film, respectively. $R_{\epsilon bo} = \frac{\epsilon_{Si}}{\epsilon_{SiGe_{bo}}}$ is the ratio of semiconductor permittivities in silicon, and at the bottom of the SiGe film, respectively.

$$\phi_{TH} = 2\phi_F + \frac{\Delta E_{VH}}{q} - \phi_T \ln\left[\frac{N_{VSi}}{N_{VSiGe}}\right] \quad (A9)$$

and

$$\phi_{Tbo} = 2\phi_F + \frac{\Delta E_{VB}}{q} - \phi_T \ln\left[\frac{N_{VSi}}{N_{VSiGe}}\right] \quad (A10)$$

are the threshold potentials at the top, and at the bottom Si/SiGe heterojunction,

respectively. The expression for $f(\phi_S)$ can be simplified for each of the regimes of operation of the capacitor

In strong inversion: $\phi_H < \phi_{TH}$

$$f(\phi_S) = e^{\frac{2\phi_F - \phi_S}{\phi_T}} + \frac{R_{\varepsilon H} - \frac{\varepsilon_l \phi_H}{\varepsilon_{Si}}}{1+\frac{F_{bi}}{F_{bo}}} e^{\frac{\phi_{TH} - \phi_H}{\phi_T}} \tag{A11}$$

In depletion and weak inversion: $\phi_{TH} < \phi_H < 0$

$$f(\phi_S) = -\frac{\phi_\delta}{\phi_T} - \frac{N_\delta}{N_B \phi_T}(\phi_\delta - \phi_{bu}) + \frac{R_{\varepsilon H}}{1+\frac{F_{bi}}{F_{bo}}} e^{\frac{\phi_{TH} - \phi_H}{\phi_T}} - \frac{R_{\varepsilon bo}}{1+\frac{F_{bi}}{F_{bo}}} e^{\frac{\phi_{Tbo} - \phi_{bo}}{\phi_T}} \tag{A12}$$

$$- \frac{\varepsilon_l}{\varepsilon_{Si}} \left[\left[\phi_H - \frac{\phi_T}{1+\frac{F_{bi}}{F_{bo}}} \right] \frac{e^{\frac{\phi_{TH} - \phi_H}{\phi_T}}}{1+\frac{F_{bi}}{F_{bo}}} - \left[\phi_{bo} - \frac{\phi_T}{1+\frac{F_{bi}}{F_{bo}}} \right] \frac{e^{\frac{\phi_{Tbo} - \phi_{bo}}{\phi_T}}}{1+\frac{F_{bi}}{F_{bo}}} \right]$$

In accumulation: $\phi_H > 0$

$$f(\phi_S) = e^{\frac{\phi_s}{\phi_T}} \tag{A13}$$

A.2 Derivation of the threshold voltage

To derive the expressions of the internal potentials ϕ_{bu}, ϕ_δ, and ϕ_H as functions of ϕ_S, and to derive the threshold voltages V_{TH} and V_{TS}, Poisson's equation has to be

integrated twice. An analytical solution can be obtained by taking into account the fixed charge in the depletion layer Q_B, and the hole charge in the SiGe layer Q_H. The hole charge in the silicon cap is neglected since, for a properly designed structure, $V_{TH}>V_{TS}$, indicating that strong inversion occurs first at the top Si/SiGe heterointerface.

Under these assumptions, the one-dimensional Poisson's equation can be written for each region of the structure as follows

$$\varepsilon_{Si}\frac{d^2\phi}{dx^2} = -qN_B \quad , \quad x_{ca}+x_{SiGe}+x_{bu}+x_{\delta} < x < x_{ca}+x_{SiGe}+x_{bu}+x_{\delta}+x_d$$

$$\varepsilon_{Si}\frac{d^2\phi}{dx^2} = qN_{\delta} \quad , \quad x_{ca}+x_{SiGe}+x_{bu} < x < x_{ca}+x_{SiGe}+x_{bu}+x_{\delta}$$

$$\varepsilon_{Si}\frac{d^2\phi}{dx^2} = 0 \quad , \quad x_{ca}+x_{SiGe} < x < x_{ca}+x_{SiGe}+x_{bu}$$

$$\varepsilon_{Si}\frac{d^2\phi}{dx^2} = -qp(x)R_{\varepsilon} \quad , \quad x_{ca} < x < x_{ca}+x_{SiGe}$$

$$\varepsilon_{Si}\frac{d^2\phi}{dx^2} = 0 \quad , \quad 0 < x < x_{ca} \qquad \text{(A14)}$$

where x_{bu} is the thickness of the silicon buffer, x_{SiGe} is the thickness of the SiGe film, x_{ca} is the thickness of the silicon cap layer.

The set of the equations (A14) can be solved using the following boundary conditions for the potential

$$\phi\Big|_{x=x_{ca}+x_{SiGe}+x_{bu}+x_{\delta}+x_d} = 0$$

$$\phi\Big|_{x=x_{ca}+x_{SiGe}+x_{bu}+x_{\delta}^-} = \phi\Big|_{x=x_{ca}+x_{SiGe}+x_{bu}+x_{\delta}^+}$$

$$\phi\Big|_{x=x_{ca}+x_{SiGe}+x_{bu}^-} = \phi\Big|_{x=x_{ca}+x_{SiGe}+x_{bu}^+}$$

$$\phi\Big|_{x=x_{ca}+x_{SiGe}^-} = \phi\Big|_{x=x_{ca}+x_{SiGe}^+}$$

$$\phi\Big|_{x=x_{ca}^-} = \phi\Big|_{x=x_{ca}^+} = \phi_H \qquad \text{(A15)}$$

From Gauss's law the additional boundary conditions are

$$\left.\frac{d\phi}{dx}\right|_{x=x_{ca}+x_{SiGe}+x_{bu}+x_{\delta}+x_d} = 0$$

$$\left.\frac{d\phi}{dx}\right|_{x=x_{ca}+x_{SiGe}+x_{bu}+x_{\delta}^-} = \left.\frac{d\phi}{dx}\right|_{x=x_{ca}+x_{SiGe}+x_{bu}+x_{\delta}^+}$$

$$\left.\frac{d\phi}{dx}\right|_{x=x_{ca}+x_{SiGe}+x_{bu}^-} = \left.\frac{d\phi}{dx}\right|_{x=x_{ca}+x_{SiGe}+x_{bu}^+}$$

$$\left.\frac{d\phi}{dx}\right|_{x=x_{ca}+x_{SiGe}^-} = R_{\varepsilon bo}\left.\frac{d\phi}{dx}\right|_{x=x_{ca}+x_{SiGe}^+}$$

$$R_{\varepsilon H}\left.\frac{d\phi}{dx}\right|_{x=x_{ca}^-} = \left.\frac{d\phi}{dx}\right|_{x=x_{ca}^+} \qquad \text{(A16)}$$

Using the boundary conditions, and carrying out a first integration of Poisson's equation the following relations are obtained

$$\varepsilon_{Si}\frac{d\phi}{dx} = qN_B(x_{ca}+x_{SiGe}+x_{bu}+x_{\delta}+x_d-x) \;,\; x_{ca}+x_{SiGe}+x_{bu}+x_{\delta} < x < x_{ca}+x_{SiGe}+x_{bu}+x_{\delta}+x_d$$

$$\varepsilon_{Si}\frac{d\phi}{dx} = qN_B x_d - qN_\delta(x_{ca}+x_{SiGe}+x_{bu}+x_\delta-x) \ , \ x_{ca}+x_{SiGe}+x_{bu}< x <x_{ca}+x_{SiGe}+x_{bu}+x_\delta$$

$$\varepsilon_{Si}\frac{d\phi}{dx} = qN_B x_d - qN_\delta x_\delta \ , \ x_{ca}+x_{SiGe}< x <x_{ca}+x_{SiGe}+x_{bu}$$

$$\varepsilon_{Si}\frac{d\phi}{dx} = (qN_B x_d - qN_\delta x_\delta)R_\varepsilon\sqrt{1+H(\phi)} \ , \ x_{ca}< x <x_{ca}+x_{SiGe}$$

$$\varepsilon_{Si}\frac{d\phi}{dx} = (qN_B x_d - qN_\delta x_\delta)\sqrt{1+H(\phi_H)} \ , \ 0< x <x_{ca} \qquad \text{(A17)}$$

where ϕ_H is the potential at the top SiGe/Si heterointerface as defined in eqn. (A15). $H(\phi)$ represents the contribution of holes to the electric field in the SiGe film and is given by

$$H(\phi) = \frac{2q\varepsilon_{SiGe_H}N_B\phi_T}{Q_B{}^2(1+\frac{F_{bi}}{F_{bo}})}\left[\exp\left[\frac{\phi_{TH}-\phi}{\phi_T}\right] - \frac{\varepsilon_{SiGe_{bo}}}{\varepsilon_{SiGe_H}}\exp\left[\frac{\phi_{Tbo}-\phi(x=x_{ca}+x_{SiGe})}{\phi_T}\right]\right] \qquad \text{(A18)}$$

where

$$Q_B = qN_B x_d - qN_\delta x_\delta$$

is the fixed charge in the depletion region, and

$$F_{bo} = \frac{Q_B}{\varepsilon_{SiGe_{bo}}}$$

is the electric field at the bottom Si/SiGe heterojunction.

To obtain the potential distribution, a second integration of Poisson's equation is required. In order to make possible an analytical solution, the contribution of holes (the $H(\phi)$ term) to the potential drop in the SiGe film is neglected. This approximation introduces a small error, as verified by comparison to numerical results.

Using this approximation, the potential at the top heterointerface ϕ_H and the potential at the surface ϕ_S are obtained respectively as

$$\phi_H = \phi\Big|_{x=x_{ca}} = -\frac{qN_B x_d}{2\varepsilon_{Si}}\left[x_d + 2(x_\delta + x_{bu} + R_\varepsilon x_{SiGe})\right] \qquad \text{(A19)}$$

$$+ \frac{qN_\delta x_\delta}{2\varepsilon_{Si}}\left[x_\delta + 2(x_{bu} + R_\varepsilon x_{SiGe})\right]$$

and

$$\phi_S = \phi\Big|_{x=0} = \phi_H - (qN_B x_d - qN_\delta x_\delta)\frac{x_{ca}}{\varepsilon_{Si}}\sqrt{1 + H(\phi_H)} \qquad \text{(A20)}$$

The $H(\phi_H)$ term in eqn. (A20) represents the contribution of free holes in the SiGe layer to the potential drop across the silicon cap. It is obtained from (A18) by dropping the last exponential term, which is negligible, and can be expressed as

$$H(\phi_H) = \frac{2q\varepsilon_{SiGe_H} N_B \phi_T}{Q_B{}^2\left[1 + \frac{\varepsilon_{SiGe_{bo}} F_{bi}}{Q_B}\right]} \exp\left[\frac{\phi_{TH} - \phi_H}{\phi_T}\right] \tag{A21}$$

By taking into account all potential drops across the structure, the expression for the gate voltage V_G can be written as

$$V_G = \phi_{MS} - \frac{Q_f}{C_{ox}} + \phi_H - (qN_B x_d - qN_\delta x_\delta)\left[\frac{x_{ca}}{\varepsilon_{Si}} + \frac{x_{ox}}{\varepsilon_{ox}}\right]\sqrt{1 + H(\phi_H)} \tag{A22}$$

The maximum depletion depth x_{dmax} can be derived from eqn. (A19)

$$x_{dmax} = -x_\delta - x_{bu} - R_\varepsilon x_{SiGe} +$$

$$\sqrt{\frac{2\varepsilon_{Si}}{qN_B}(-\phi_{TH}) + (x_\delta + x_{bu} + R_\varepsilon x_{SiGe})^2 + \frac{N_\delta x_\delta}{N_B}\left[x_\delta + 2(x_{bu} + R_\varepsilon x_{SiGe})\right]} \tag{A23}$$

For the depletion regimes and for most of the inversion regime, the internal potentials ϕ_H, ϕ_{bo}, ϕ_{bu}, and ϕ_δ can be expressed as functions of the surface potential, ϕ_S

$$\phi_H = \phi_S + Q_B \frac{x_{ca}}{\varepsilon_{Si}}\sqrt{1 + H(\phi_H)} \tag{A24}$$

$$\phi_{bo} = \phi_H + Q_B \frac{x_{SiGe}}{\varepsilon_{SiGe}} \tag{A25}$$

$$\phi_{bu} = \phi_{bo} + Q_B \frac{x_{bu}}{\varepsilon_{Si}} \tag{A26}$$

$$\phi_\delta = \phi_{bu} + \frac{qN_B x_d x_\delta}{\varepsilon_{Si}} - \frac{qN_\delta x_\delta{}^2}{2\varepsilon_{Si}} \tag{A27}$$

A.3 Derivation of the semiconductor capacitance C_S

Eqns. (A24) - (A27) and the derivative of f (ϕ_S) are required in the calculation of the semiconductor capacitance

$$\phi_T \frac{df(\phi_S)}{d\phi_S} = e^{\frac{\phi_s}{\phi_T}} - 1 - e^{\frac{2\phi_F}{\phi_T}}\left(e^{-\frac{\phi_s}{\phi_T}} - 1\right) - \frac{R_{\varepsilon H}}{1+\frac{F_{bi}}{F_{bo}}} e^{\frac{\phi_{TH}-\phi_H}{\phi_T}} + \frac{R_{\varepsilon bo}}{1+\frac{F_{bi}}{F_{bo}}} e^{\frac{\phi_{Tbo}-\phi_{bo}}{\phi_T}} \quad \text{(A28)}$$

In strong inversion: $\phi_H < \phi_{TH}$

$$C_S = \sqrt{\frac{q\varepsilon_{Si}N_B}{2\phi_T}}\left[e^{\frac{2\phi_F-\phi_s}{\phi_T}} + \frac{R_{\varepsilon H}}{1+\frac{F_{bi}}{F_{bo}}} e^{\frac{\phi_{TH}-\phi_H}{\phi_T}}\right]^{1/2} \quad \text{(A29)}$$

In depletion and weak inversion: $\phi_{TH} < \phi_H < 0$

$$C_S = \left[\frac{q\varepsilon_{Si}N_B}{2[-\phi_\delta - \frac{N_\delta(\phi_\delta-\phi_{bu})}{N_B}]}\right]^{1/2}\left[1 + \frac{R_{\varepsilon H}}{1+\frac{F_{bi}}{F_{bo}}} e^{\frac{\phi_{TH}-\phi_H}{\phi_T}} - \frac{R_{\varepsilon bo}}{1+\frac{F_{bi}}{F_{bo}}} e^{\frac{\phi_{Tbo}-\phi_{bo}}{\phi_T}}\right] \quad \text{(A30)}$$

In accumulation: $\phi_H > 0$

$$C_S = \sqrt{\frac{q\varepsilon_{Si}N_B}{2\phi_T}} e^{\frac{\phi_s}{2\phi_T}} \quad \text{(A31)}$$

In eqns. (A29) - (A31), the contribution of the term describing the position dependence of the permittivity has been neglected (i.e. $\varepsilon_1 = 0$). Note that eqn. (A28) - (A31) reduce to those corresponding to a Si MOS capacitor.

Appendix B

1D Self-Consistent Schrödinger and Poisson Equations Solver

This appendix describes an one-dimensional numerical simulation program which was developed in order to investigate the electrostatics of the SiO_2/Si/SiGe/Si heterostructure system.

Numerical simulations have been carried out to investigate the quantitative link between the internal layer structure and the C_{LF}–V_G characteristics of Si/SiGe MOS capacitors. A classical approach using Fermi-Dirac statistics does not explain the size-quantization induced offset between the heterojunction and the position of the centroid of the accumulated charge. Because this quantum effect has to be accounted for in the C-V characterization, a numerical simulator was developed that selfconsistently solves Poisson's equation

$$\nabla(\varepsilon\nabla\phi) = -q[N_D^+ - N_A^- - n + p] \tag{B1}$$

and Schrödinger's equation

$$-\frac{\tilde{h}^2}{2}\nabla\left[\frac{1}{m_h}\nabla\psi_i\right] + (\phi - E_i)\psi_i = 0 \tag{B2}$$

in one dimension to obtain the potential ϕ, hole wavefunctions ψ_i, corresponding to each eigenenergy E_i, and the concentration of holes p throughout the structure [1]:

$$p = \frac{m_h kT}{\pi\tilde{h}^2}\sum_{i=1}^{\infty}|\psi_i|^2 \ln\left[1 + \exp\left[\frac{E_i - E_F}{kT}\right]\right] \tag{B3}$$

Since only the inversion region of the C_{LF}–V_G characteristics is of interest, the electron concentration is assumed to obey Boltzmann statistics and is included as such in Poisson's equation:

$$n = N_C \exp\left[\frac{E_F - E_C}{kT}\right] \tag{B4}$$

The analysis also accounts for interface trapped charge D_{it}, fixed interface charge Q_f and for the contribution of deep level N_{DT}, N_{AT}, and shallow level traps N_D, N_A, located either in the Si or in the SiGe film. The ionized fixed charge densities N_D^+ and N_A^- are calculated as functions of the trap energies: E_{DT}, E_D, E_{AT}, E_A, according to the formulae [2]:

$$N_D^+ = \frac{N_D}{1 + 2\exp\left[\frac{E_F - E_D}{kT}\right]} + \frac{N_{DT}}{1 + 2\exp\left[\frac{E_F - E_{DT}}{kT}\right]} \tag{B5}$$

$$N_A^- = \frac{N_A}{1 + 4\exp\left[\frac{E_A - E_F}{kT}\right]} + \frac{N_{AT}}{1 + 4\exp\left[\frac{E_{AT} - E_F}{kT}\right]} \tag{B6}$$

The simulator calculates the potential ϕ_H and the peak hole concentration p_H at the top Si/SiGe heterojunction, and at the Si/SiO_2 interface ϕ_S, p_S, respectively, the overall charge

$$Q_T(V_G) = \int_{\infty}^{0} q[N_D^+(x, V_G) - N_A^-(x, V_G) - n(x, V_G) + p(x, V_G)]dx \tag{B7}$$

and the hole charge centroid location

$$x_{av}(V_G) = \frac{\int_{-\infty}^{0} x\, p(x, V_G)dx}{\int_{-\infty}^{0} p(x, V_G)dx} \tag{B8}$$

all as functions of the gate voltage V_G. Next, the low frequency capacitance, which is a measurable terminal function, is calculated:

$$C_{LF}(V_G) = \frac{\partial Q_T(V_G)}{\partial V_G} \tag{B9}$$

References

1. S. Voinigescu, and A. Müller, "Charge Dynamics in Heterostructure Schottky-Gate Capacitors and Their Influence on the Transconductance and Low-Frequency Capacitance of MODFET's," *IEEE Trans. Electron. Dev.* vol. **ED-36**, pp. 2320-2328, 1989.

2. S. M. Sze, *Physics of Semiconductor Devices,* Second Edition, Chap.1, John Wiley & Sons, New-York, 1981.

APPENDIX C

Analytical Model for Si/SiGe/Si p-MOSFET's

In this Appendix, the elements of an analytical model to describe the operation of the Si/SiGe/Si p-MOSFET are developed.

C.1 Threshold Voltage and Body Effect

V_{T0}, obtained from eqns. (2.14), is the buried channel threshold voltage with no substrate bias applied

$$V_{T0} = V_{FB} + \phi_{TH} - \gamma\left[\sqrt{-\phi_{TH} + \phi_o} - \sqrt{\phi_1}\right] \tag{C1}$$

where

$$\gamma = \sqrt{2q\varepsilon_{Si}N_B}\left[\frac{x_{ca}}{\varepsilon_{Si}} + \frac{x_{ox}}{\varepsilon_{ox}}\right]$$

is the "body factor", and

$$\phi_o = \frac{qN_B(x_\delta + x_{bu} + R_\varepsilon x_{SiGe})^2}{2\varepsilon_{Si}} + \frac{qN_\delta x_\delta[x_\delta + 2(x_{bu} + R_\varepsilon x_{SiGe})]}{2\varepsilon_{Si}}$$

$$\phi_1 = \frac{qN_B\left[x_\delta\left[1 + \frac{N_\delta}{N_B}\right] + x_{bu} + R_\varepsilon x_{SiGe}\right]^2}{2\varepsilon_{Si}}$$

The threshold voltage of the Si/SiGe/Si p-MOSFET, V_T, can be expressed as a function of the substrate bias, V_{BS}

$$V_T = V_{T0} - \gamma\left[\sqrt{V_{BS} - \phi_{TH} + \phi_o} - \sqrt{-\phi_{TH} + \phi_o}\right] \tag{C2}$$

C.2 I-V Characteristics

Subthreshold Region

As for Si MOSFET's, the subthreshold current is a diffusion current. Only the buried layer charge is significant in weak inversion, and therefore, the following expression holds

$$I_{DS} = -WD_{pSiGe}\frac{\partial Q_H}{\partial z} = \frac{W}{L}\mu_{pSiGe}\phi_T\left[Q_H(L) - Q_H(0)\right] \tag{C3}$$

The total and the depletion semiconductor charges are obtained from eqn. (2.8)

$$Q_T = \sqrt{2q\epsilon_{Si}N_B\phi_T f(\phi_S)} \tag{C4}$$

$$Q_D = \sqrt{2q\epsilon_{Si}N_B\phi_T f_D(\phi_S)} \tag{C5}$$

where, by neglecting the term due to the permittivity gradient in eqn. (A11)

$$f(\phi_S) = \frac{R_{\epsilon H}}{1+\frac{F_{bi}}{F_B}}e^{\frac{\phi_{TH}-\phi_H}{\phi_T}} - \frac{\phi_\delta}{\phi_T} - \frac{N_\delta}{N_B\phi_T}(\phi_\delta - \phi_{bu}) \tag{C6}$$

$$f_D(\phi_S) = -\frac{\phi_\delta}{\phi_T} - \frac{N_\delta}{N_B\phi_T}(\phi_\delta - \phi_{bu}) \tag{C7}$$

In weak inversion, ϕ_S, ϕ_{bu}, and ϕ_δ, are linear functions of ϕ_H (eqns. (A23), (A25), and (A26)).

$$Q_H = \sqrt{\frac{q\epsilon_{Si}N_B\phi_T}{2f_D(\phi_S)}}\left[f(\phi_S) - f_D(\phi_S)\right] = \sqrt{\frac{q\epsilon_{Si}N_B\phi_T}{2f_D(\phi_S)}}\frac{R_{\epsilon H}}{1+\frac{F_{bi}}{F_B}}e^{\frac{\phi_{TH}-\phi_H}{\phi_T}} \tag{C8}$$

At the source end of the channel

$$Q_H(0) = \sqrt{\frac{q\varepsilon_{Si}N_B\phi_T}{2f_D(\phi_S)}}\frac{R_{\varepsilon H}}{1+\frac{F_{bi}}{F_B}}e^{\frac{\phi_{TH}-\phi_H}{\phi_T}} \tag{C9}$$

At the drain end

$$Q_H(L) = \sqrt{\frac{q\varepsilon_{Si}N_B\phi_T}{2f_D(\phi_S)}}\frac{R_{\varepsilon H}}{1+\frac{F_{bi}}{F_B}}e^{\frac{\phi_{TH}-\phi_H+V_{DS}}{\phi_T}} \tag{C10}$$

As a result, the subthreshold current can be written as

$$I_{DS} = \frac{W}{L}\mu_{pSiGe}\phi_T{}^2\sqrt{\frac{q\varepsilon_{Si}N_B}{2\phi_T f_D(\phi_S)}}\frac{R_{\varepsilon H}}{1+\frac{F_{bi}}{F_B}}e^{\frac{\phi_{TH}-\phi_H}{\phi_T}}\left[e^{\frac{V_{DS}}{\phi_T}}-1\right] \tag{C11}$$

As shown in Fig.C.1, in weak inversion, the potential at the top heterojunction ϕ_H is a linear function of the gate voltage. As a consequence, the following relationship holds

$$n_o = \frac{\partial V_{GS}}{\partial \phi_H} = 1+\frac{C_S(\phi_H = 1.5\phi_F - \Delta E_{VH}/q)}{C_{ox}} \tag{C12}$$

and the subthreshold current can be expressed as a function of the gate and drain voltages

$$I_{DS} = \frac{W}{L}\mu_{pSiGe}\phi_T{}^2\frac{C_{ox}}{1+\alpha}e^{\frac{V_{on}-V_{GS}}{n_o\phi_T}}\left[e^{\frac{V_{DS}}{\phi_T}}-1\right] \tag{C13}$$

where the following approximation was considered valid

$$C_S\Big|_{\phi_H=\phi_{TH}} = \frac{C_{ox}}{1+\alpha}$$

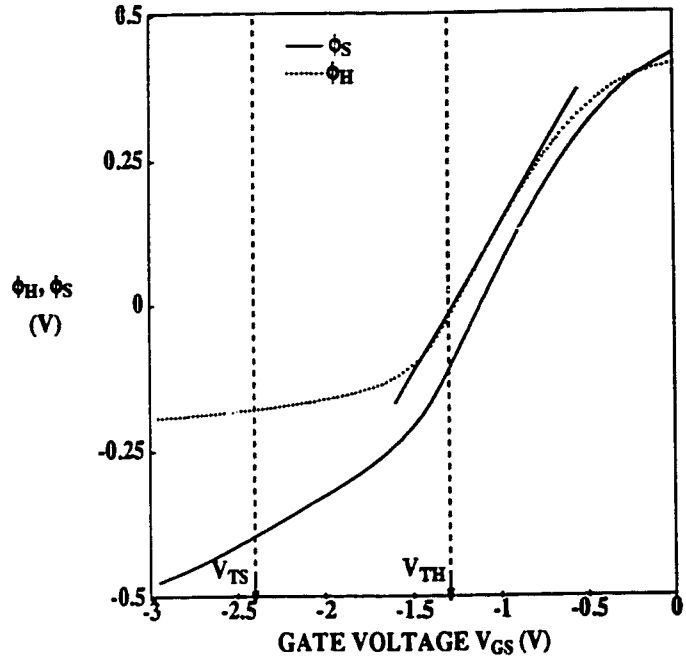

Figure C.1 *Simulated gate voltage dependence of the heterostructure potential* ϕ_H *and of the surface potential* ϕ_S *in a typical Si/SiGe/Si p-MOSFET structure. The linear region of the* $\phi_H - V_{GS}$ *characteristics is also shown.*

Effective gate capacitance

In strong inversion ($\phi_H < \phi_{TH}$), from eqn. (A29)

$$C_S = \sqrt{\frac{q\epsilon_{Si}N_B}{2\phi_T}}\left[\frac{R_{\epsilon H}}{1+\frac{F_{bi}}{F_{bo}}}\right]^{1/2} \exp\left[\frac{\phi_{TH}-\phi_H}{2\phi_T}\right]\sqrt{1+D_g\exp\left[\frac{\phi_H-\phi_S-\Delta E_{VH}/q}{\phi_T}\right]} \quad \text{(C14)}$$

Fig.C.2 illustrates that, in the bias range corresponding to strong inversion in the

buried channel alone, $V_{TS} < V_{GS} < V_T$, $\phi_H - \phi_S$ is a linear function of V_{GS}. At the same time, ϕ_H is pinned close to ϕ_{TH}.

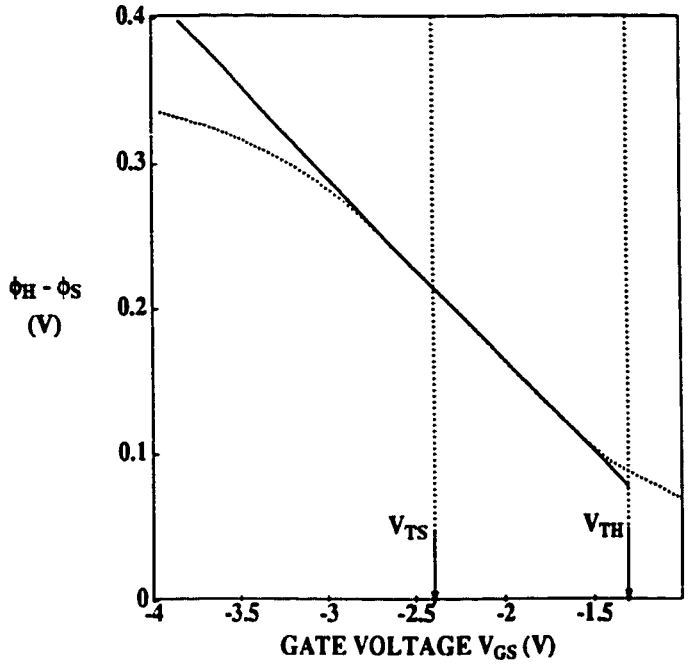

Figure C.2 *Simulated gate voltage dependence of the difference between the heterostructure potential ϕ_H and of the surface potential ϕ_S in a typical Si/SiGe/Si p-MOSFET structure. The linear portion of the characteristics is emphasized.*

As a result, in strong inversion, the semiconductor capacitance can be modeled by

$$C_S = \frac{\varepsilon_{Si}}{x_{ca}} g(V_{GS}, V_{TS}) \tag{C15}$$

and the effective gate capacitance becomes

$$C_{Geff} = \frac{C_{ox}}{1 + \frac{\alpha}{g(V_{GS}, V_{TS})}} \tag{C16}$$

where

$$g(V_{GS},V_{TS}) = \sqrt{1 + D_g \exp\left[\frac{V_{TS} - V_{GS} - V_{on2}}{n_1 \phi_T}\right]} \tag{C17}$$

$$n_1 = \frac{\partial V_{GS}}{\partial \phi_S} = 1 + \frac{C_S(\phi_S = 2\phi_F)}{C_{ox}} = 1 + \frac{1}{\alpha} \tag{C18}$$

$$D_g = \frac{1 + \dfrac{F_{bi}}{F_{bo}}}{R_{\epsilon H}}, \quad V_{on2} = n_1 \phi_T \ln\left[\frac{N_{VSiGe}}{N_B}\right] \tag{C19}$$

Effective mobility

In order to retain the same form for the drain current expression as in the case of the Si MOSFET, the effective mobility is defined as

$$\mu_{eff} = \frac{1}{1 + \theta(V_T - V_{GS})} \frac{1}{Q_{inv}} \left[\mu_{pSi} Q_S + \mu_{pSiGe} Q_H\right] \tag{C20}$$

where Q_S, shown in Fig.C.3, is the areal hole charge in the surface channel and is described by

$$Q_S = 2C_{ox} n_1 \phi_T \ln[g(V_{GS},V_{TS})] \tag{C21}$$

Q_H, the areal hole charge in the buried SiGe channel, can be expressed as a function of the gate voltage

$$Q_H = \frac{C_{ox}}{1 + \alpha}\left[V_{TH} - V_{GS} - 2n_1 \phi_T \ln[g(V_{GS},V_{TS})]\right] \tag{C22}$$

and Q_{inv} is the total inversion hole charge

$$Q_{inv} = Q_H + Q_S \tag{C23}$$

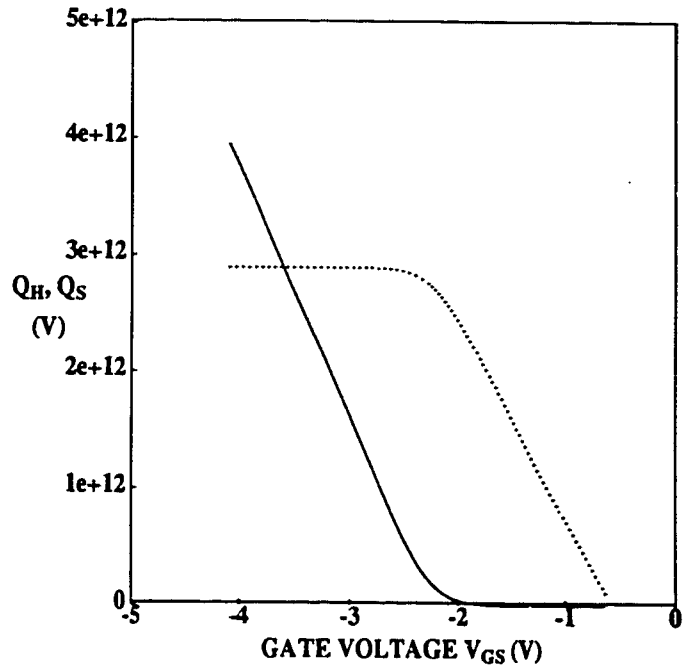

Figure C.3 *Modeled gate voltage dependence of the buried charge Q_H and surface channel charge Q_S in a typical Si/SiGe/Si p-MOSFET structure. Smooth transition between the strong inversion regime in the buried channel and the strong inversion regime in the surface channel is built into the model.*

As a result, the effective mobility becomes a function of the gate to source voltage V_{GS}

$$\mu_{eff} = \frac{C_{ox}}{C_{Geff}} \frac{\left[\mu_{pSi} m(V_{GS}, V_{TS}) + \frac{\mu_{pSiGe}}{1+\alpha} h(V_{GS}, V_{TS})\right]}{1 + \theta(V_T - V_{GS})} \tag{C24}$$

where

$$h(V_{GS},V_{TS}) = 1 - 2n_1\phi_T \frac{\ln[g(V_{GS},V_{TS})]}{V_T - V_{GS}} \tag{C25}$$

$$m(V_{GS},V_{TS}) = 2n_1\phi_T \frac{\ln[g(V_{GS},V_{TS})]}{V_T - V_{GS}} \tag{C26}$$

For $V_{GS} > V_{TS}$

$$C_{Geff} = \frac{C_{ox}}{1+\alpha}, \quad \mu_{eff} = \frac{\mu_{pSiGe}}{1+\theta(V_T - V_{GS})}$$

and for $V_{GS} < V_{TS}$

$$C_{Geff} = C_{ox}, \quad \mu_{eff} = \frac{\mu_{pSi}}{1+\theta(V_T - V_{GS})}$$

Drain Current Expression in Strong Inversion

By assuming a realistic velocity-field characteristics

$$v(F) = \frac{\mu_{eff}F}{1 + \frac{\mu_{eff}F}{v_{psat}}} \tag{C27}$$

one can derive the expression of the drain current to account for mobility degradation caused by the longitudinal field F

$$I_{DS}dx = \frac{WC_{Geff}\mu_{eff}\frac{d\phi}{dx}}{1 + \frac{\mu_{eff}\frac{d\phi}{dx}}{v_{psat}}}\left[V_T - V_{GS} + \phi\right]dx \tag{C28}$$

Eqn. (C28) can be rearranged

$$I_{DS}dx + \frac{\mu_{eff}}{v_{psat}} I_{DS}d\phi = W\mu_{eff}C_{Geff}\left[V_T - V_{GS} + \phi\right]d\phi$$

After integrating with respect to x and ϕ, from 0 to L, and from 0 to V_{DS}, respectively

$$I_{DS}L - \frac{\mu_{eff}}{v_{psat}} I_{DS}V_{DS} = W\mu_{eff}C_{Geff}\left[V_T - V_{GS} + \frac{V_{DS}}{2}\right]V_{DS} \qquad (C29)$$

Finally, the drain current equation in the nonsaturation region is cast as

$$I_{DS} = \frac{W}{L}\frac{\mu_{eff}C_{Geff}}{1 - \frac{\mu_{eff}}{v_{psat}}\frac{V_{DS}}{L}}\left[V_T - V_{GS} + \frac{V_{DS}}{2}\right]V_{DS} \qquad (C30)$$

Assuming velocity saturation is the mechanism responsible for the saturation of the drain current, the drain to source saturation voltage and the saturation current are obtained from the current continuity condition

$$I_{DS}\Big|_{V_{DS} = V_{DSAT}} = -Wv_{psat}Q_{inv}(L) \qquad (C31)$$

as

$$V_{DSAT} = \frac{Lv_{psat}}{\mu_{eff}}\left[1 - \sqrt{1 + \frac{2\mu_{eff}(V_T - V_{GS})}{Lv_{psat}}}\right] \qquad (C32)$$

and

$$I_{DSAT} = -\frac{2W}{L}\frac{\mu_{eff}C_{Geff}\left[V_T - V_{GS}\right]^2}{\left[1 + \sqrt{1 + \frac{2\mu_{eff}(V_T - V_{GS})}{Lv_{psat}}}\right]^2} \qquad (C33)$$

respectively.

Channel Length Modulation

The equations which apply for Si MOSFET's [1] are modified to reflect the case of the buried SiGe channel

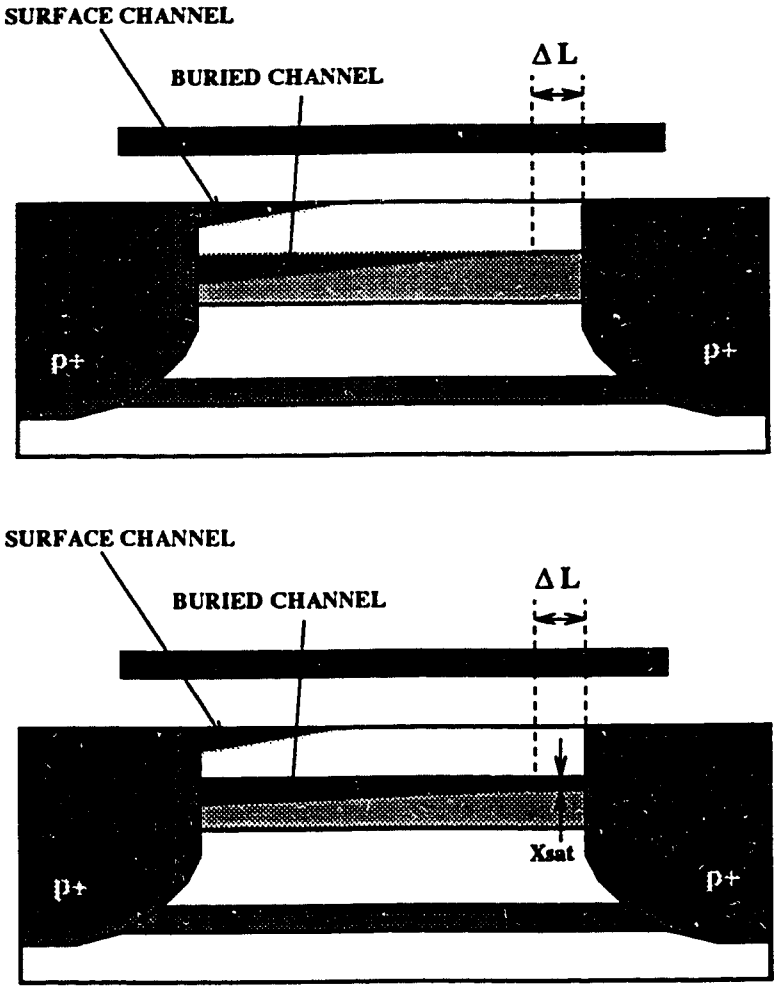

Figure C.4 *Illustration of channel length modulation in Si/SiGe/Si MOSFET's. a) Pinched-off device. b) Velocity saturated device.*

$$\Delta L = \frac{L}{A}\left[\sqrt{(F_C L)^2 - 2A(V_{DS} - V_{DSAT})} - F_C L\right] \qquad \text{(C34)}$$

where

$$A = \frac{qN_B L^2}{2\varepsilon_{Si}}\left[1 + \frac{C_{ox}(V_{GS} - V_T + V_{DSAT})}{(1+\alpha)qN_B x_{sat}}\right] \quad \text{(C35)}$$

F_C is the critical field at which velocity saturation occurs. x_{sat} is the thickness of the inversion layer at L - ΔL, and can be approximated by $\frac{x_{SiGe}}{2}$. Note that at L - ΔL the surface channel is depleted, only the buried channel is on. Therefore, $C_{Geff} = \frac{C_{ox}}{(1+\alpha)}$.

C.3 Small Signal Equivalent Circuit

The elements of the small signal equivalent circuit can be derived by differntiating the DC characteristics. Several approximations, neglecting the gate voltage dependence of μ_{eff} and C_{Geff}, are provided below.

transconductance (nonsaturation)

$$g_m = \frac{W}{L}\frac{\mu_{eff}C_{Geff}}{1 - \frac{\mu_{eff}}{v_{psat}}\frac{V_{DS}}{L}}V_{DS} \quad \text{(C36)}$$

transconductance (saturation and long channel)

$$g_m = \frac{W}{L}\mu_{eff}C_{Geff}(V_T - V_{GS}) \quad \text{(C37)}$$

output conductance (nonsaturation)

$$\frac{W}{L}\mu_{eff}C_{Geff}(V_T - V_{GS} + V_{DS}) \quad \text{(C38)}$$

output conductance (saturation)

$$g_{ds} = \left[\frac{L}{L-\Delta L}\right]^2 \frac{I_{DSAT}}{\sqrt{(F_C L)^2 - 2A(V_{DS} - V_{DSAT})}} \tag{C39}$$

gate-source capacitance

$$C_{gs} = \frac{2WL}{3} C_{Geff}\left[1 - \left[\frac{V_2}{V_1 + V_2}\right]^2\right] + WL_{ov}C_{ox} \tag{C40}$$

gate-drain capacitance

$$C_{gd} = \frac{2WL}{3} C_{Geff}\left[1 - \left[\frac{V_1}{V_1 + V_2}\right]^2\right] + WL_{ov}C_{ox} \tag{C41}$$

where [2]

$$V_1 = V_T(V_{SB}) - V_{GS}, \qquad V_2 = V_T(V_{DB}) - V_{GD} \tag{C42}$$

$$C_{ov} = WL_{ov}C_{ox} \tag{C43}$$

drain-source(substrate) capacitance

$$C_{ds} = C_{db} = \frac{C_j A_D}{(1 - V_{SB}/\phi_j)^{m_j}} + \frac{C_{jsw} P_D}{(1 - V_{SB}/\phi_j)^{m_{jsw}}} \tag{C44}$$

where C_j is the 0-bias capacitance per unit area, C_{jsw} is the 0-bias side-wall capacitance per unit length, A_D is the area of the drain implant region, P_D is the perimeter of the drain implant region, ϕ_j is the built-in voltage of the drain/substrate junction. m_j and m_{jsw} are the substrate-junction and the perimeter capacitance grading coefficients, respectively.

C.4 Noise Performance

The noise of the Si/SiGe/Si p-MOSFET is represented by two internal noise currents

$$\overline{i^2}_{nd}(f) = 4kTPg_m + \frac{k_f g_m{}^2}{f^{af} C_{Geff} WL} \tag{C45}$$

$$\overline{i^2}_{ng}(f) = 4kTR\omega^2 \frac{C_{gs}^2}{g_m} \tag{C46}$$

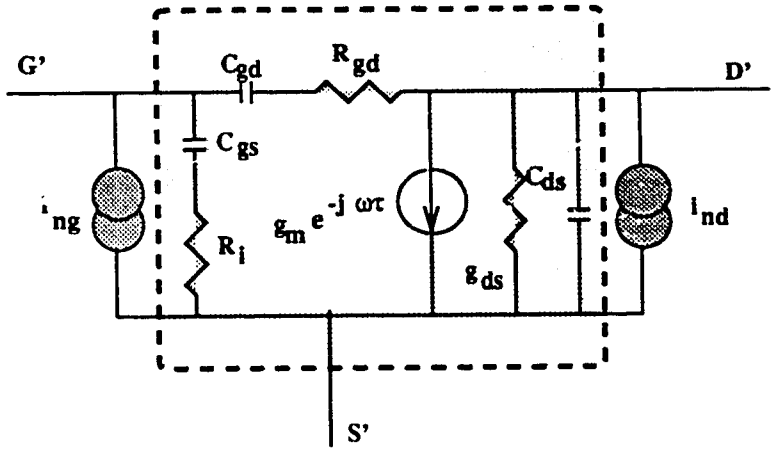

Figure C.5 *Noise equivalent circuit of the intrinsic Si/SiGe/Si MOSFET.*

Their correlation is modeled by an imaginary coefficient

$$jC = \frac{\overline{i_{ng} \times i^*_{nd}}}{\sqrt{\overline{i^2}_{nd} \times \overline{i^2}_{ng}}} \tag{C47}$$

P, R and C are *intrinsic noise parameters* that describe the medium and high frequency noise added by the device. k_f and *af* are *intrinsic noise parameters* that describe 1/f noise [3].

The two-port noise parameters of the MOSFET in the noise impedance formalism are given by

$$r_n = R_s + R_g + k_2 \frac{1+(\omega R_i C_{gs})^2}{g_m} = \frac{R'_s + k_2 \dfrac{1+(\omega R_i C_{gs})^2}{g'_m}}{W} + R'_g W \quad \text{(C48)}$$

$$g_n = k_1 g_m \left[\frac{f}{f_T}\right]^2 = k_1 g'_m \left[\frac{f}{f_T}\right]^2 W \quad \text{(C49)}$$

$$r_{cor} = R_s + R_g + k_3 R_i = \frac{R'_s + k_3 R'_i}{W} + R'_g W \quad \text{(C50)}$$

$$x_{cor} = \frac{k_3}{j\omega C_{gs}} = \frac{k_3}{j\omega C'_{gs}} \frac{1}{W} \quad \text{(C51)}$$

$$R_{sop} = \sqrt{\frac{r_n}{g_n} + r_{cor}^2}, \quad X_{sop} = -x_{cor} \quad \text{(C52)}$$

$$F_{min} = 1 + 2g_n(r_{cor} + R_{sop}) \quad \text{(C53)}$$

where

$$k_1 = P + R - 2C\sqrt{PR}, \quad k_2 = \frac{PR(1-C^2)}{k_1} \quad k_3 = \frac{P - C\sqrt{PR}}{k_1} \quad \text{(C54)}$$

Since $r_{cor}^2 \ll \frac{r_n}{g_n}$, the term r_{cor} can be neglected. The simplified expression for the minimum noise figure becomes

$$F_{min} = 1 + 2\sqrt{g_n r_n} = 1 + 2\sqrt{k_1} \frac{f}{f_T} \sqrt{(R_s + R_g) g_m + k_2 [1 + (\omega R_i C_{gs})^2]} \quad \text{(C55)}$$

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APPENDIX D

2D Numerical Modeling of Si/SiGe/Si p-MOSFET's

The purpose of this appendix is to describe the features of the commercial program used for the two-dimensional numerical simulation of Si/SiGe/Si p-MOSFET's. Some additions to this program were made in order to calculate the S parameters and to study the impact of the series parasitics on the high frequency performance. These additions are now part of the latest commercial release of the program.

D.1 General Features

The ATLAS/BLAZE 2D heterostructure device simulator [1] is used to analyze type I and type II heterostructures. Both the conventional Drift-Diffusion (DD) and the more sophisticated Energy Balance (EB) model, which accounts for non-local transport effects, are employed for simulations of the DC characteristics. Frequency domain performance is simulated using the DD model. The EB model for semiconductor devices with nonuniform bandgap [2,3] is obtained by combining the approach proposed by Stratton for Si devices [4], with the DD heterojunction model as developed in [5,6]. The system of five independent semiconductor equations is solved with potential ϕ, electron concentration n, hole concentration p, electron temperature T_n and hole temperature T_p, as variables.

D.2 Mobility and Impact Ionization Models

In the case of DD simulations, a field dependent mobility model is employed

for SiGe

$$\mu_p(F) = \frac{\mu_{op}}{1+\frac{\mu_{op}F}{v_{sp}}} \qquad \mu_n(F) = \frac{\mu_{on}}{\sqrt{1+\left[\frac{\mu_{on}F}{v_{sn}}\right]^2}} \tag{D1}$$

where F is the electric field parallel to the heterointerface, v_{sn} and v_{sp} are the saturation velocities of electrons and holes.

In EB simulations carrier mobilities are expressed as functions of the local carrier temperatures

$$\mu_p(T_p) = \frac{\mu_{op}}{1+\alpha_p(T_p-T_o)} \qquad \mu_n(T_p) = \frac{\mu_{on}}{\sqrt{1+\alpha_n^2(T_n-T_o)^2}} \tag{D2}$$

where

$$\alpha_p = \frac{3}{2}\frac{k_B\mu_{op}}{qv_{sp}^2\tau_{mp}} \qquad \alpha_n = \frac{3}{2}\frac{k_B\mu_{on}}{qv_{sn}^2\tau_{mn}}$$

and $\tau_{mn} = \tau_{mp} = 0.4$ ps in both Si and SiGe.

The low-field mobility values in undoped SiGe are derived from experimental data [7-9] and a silicon-like doping dependence, based on the Arora model [10], is assumed. This dependence was confirmed by hole mobility measurements in the base of Si/SiGe/Si HBT's [11]. The low-field hole mobility in undoped $Si_{0.5}Ge_{0.5}$ is assumed to be 40% higher than in $Si_{0.75}Ge_{0.25}$. The saturation velocities in SiGe are set equal to those in Si, in accordance with experimental [12,13] and Monte Carlo simulation results [14,15].

The temperature dependent impact ionization is calculated based on the model

proposed in [16]

$$G=A_n\,|J_n|\exp\left[-\frac{T_{ncr}}{T_n}\right]+A_p\,|J_p|\exp\left[-\frac{T_{pcr}}{T_p}\right] \qquad (D3)$$

where

$$T_{ncr}=\frac{2}{3}\frac{qv_{sn}\tau_{in}}{k_B}E_{ncr} \quad T_{pcr}=\frac{2}{3}\frac{qv_{sp}\tau_{ip}}{k_B}E_{pcr}$$

and $\tau_{in}=\tau_{ip}=0.4$ ps in both Si and SiGe.

Other Si and SiGe material parameters were taken from the literature [17,18].

Experimental transconductance characteristics for a submicrometer 20%Ge p-MOSFET [8] and DD simulation results are shown in Fig.3.3. They confirm the accuracy of the material models employed, and the validity of the DD model at these channel lengths (0.25 μm).

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APPENDIX E

Parameter Extraction for Si/SiGe p-MOSFET's

This appendix presents two parameter extraction techniques developed for the characterization and modeling of Si/SiGe/Si p-MOSFET's. The first is a low-frequency extraction technique which provides the specific mobility-gate voltage characteristics in a Si/SiGe/Si p-MOSFET. The second is a high frequency extraction technique whereby the elements of the small signal equivalent circuit are obtained from S parameter measurements.

E.1 Mobility Profiling in Long and Wide (FAT) Si/SiGe/Si p-MOSFET's

By definition, the cutoff frequency in the triode (linear) region is expressed as

$$f_{TL}(V_{GS}) = \frac{g_m}{2\pi C_{Ggate}} = \frac{V_{DS}}{2\pi L^2} \frac{\frac{d}{dV_{GS}} \int_0^\infty p(x)\mu(x)dx}{\frac{d}{dV_{GS}} \int_0^\infty p(x)dx} \tag{E1}$$

in which the contributions of the ionized and free electron charge in inversion were considered negligible. Equation (E1) shows that the cutoff frequency is a function of the device length and of the effective free carrier mobility and can be expressed as

$$f_{TL}(V_{GS}) = \mu_{eff}(V_{GS}) \frac{V_{DS}}{2\pi L^2} \tag{E2}$$

where

$$\mu_{eff}(V_{GS}) = \frac{\frac{d}{dV_{GS}} \int_0^\infty p(x)\mu(x)dx}{\frac{d}{dV_{GS}} \int_0^\infty p(x)dx} \tag{E3}$$

As shown in Fig. E.1, the gate voltage dependence of the effective mobility can be extracted from the linear region transconductance and gate to source capacitance measurements, using eqns. (E2), (E3) and (E4) [1]

$$\mu_{eff}(V_{GS}) = \frac{g_m L^2}{2V_{DS}C_{gs}} \tag{E4}$$

The simulation results indicate that the extracted mobility closely reproduces the actual hole mobility used in the simulation model, which was assumed independent of the vertical field. The experiments confirm the simulated gate voltage window, but also reflect the impact of the vertical field on mobility, both in the Si cap and in the SiGe channel.

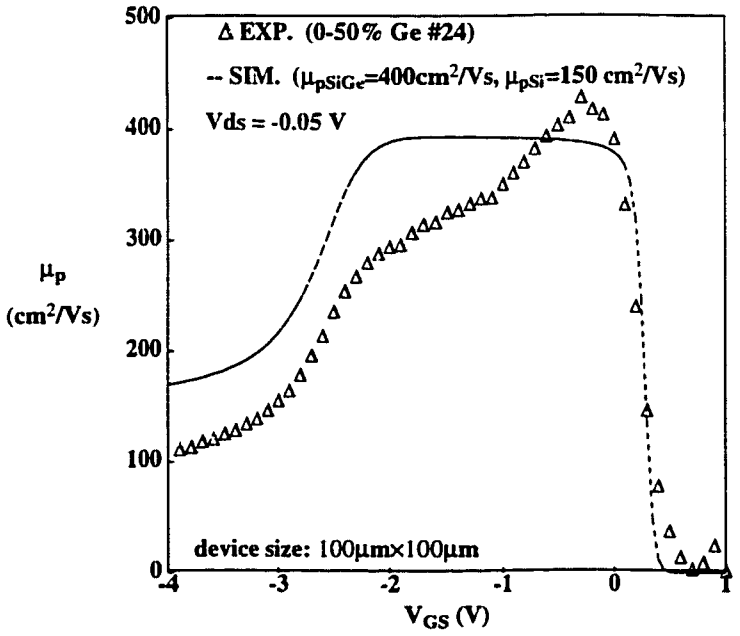

Figure E.1 *Effective mobility vs. gate voltage characteristics for triangular Ge channel profile p-MOSFET's, as extracted from experimental (Δ) and simulated (--) transconductance and capacitance characteristics.*

E.2 Extraction of the Small Signal Equivalent Circuit from S-parameter Measurements.

Motivation

- Allows for capacitance extraction. Capacitances are very difficult to measure directly in small devices where the capacitance is of the order of a few fF.
- Allows for extraction of circuit elements which cannot be determined otherwise, like R_i, R_{gd} or τ.
- Allows for extraction of parasitic inductances L_g, L_s, and L_d which can be done only in the high frequency range.

This direct extraction technique has several important features, as described below.

- The intrinsic FET equivalent circuit is such that a y-parameter analysis of the equivalent circuit results in relatively simple expressions that can be equated to the measured y-parameter data [2, 3].
- The intrinsic equivalent circuit parameters are obtained by line fitting on a restricted frequency range, thus measurement errors can be easily eliminated.
- This technique assumes that the series parasitic resistances R_s, R_g, and R_d are known from other measurements (usually dc).
- No assumptions about the parasitic inductances are made. The method provides the bias dependence of the parasitic inductances (L_g, L_s, L_d).
- If values for R_s, R_g, and R_d are not known, the extraction can be combined with optimization to obtain the parasitic resistances. The results will be more

reliable than those obtained from straight optimization.

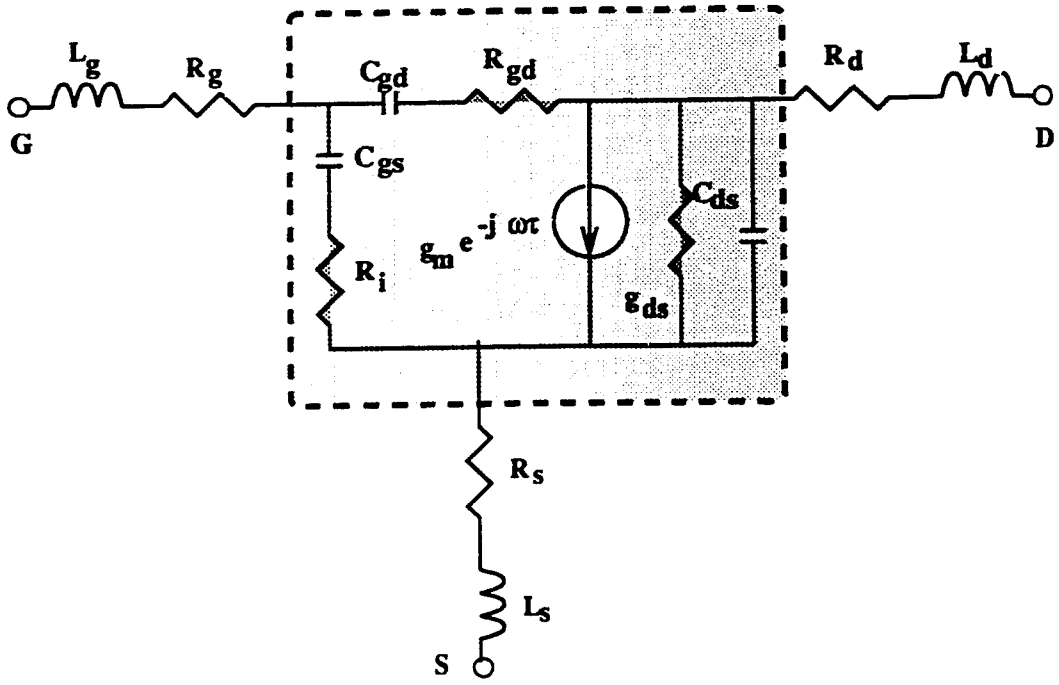

Figure E.2 *Small signal equivalent circuit of a Si/SiGe/Si p-MOSFET in common source configuration. Both the intrinsic (boxed region) and the extrinsic elements of the lumped equivalent circuit are shown.*

Physical Interpretation of the Equivalent Circuit Elements

- C_{gs} and C_{gd} represent the major components of the gate capacitance. C_{ds} represents the coupling between drain and source through the bulk and the drain to substrate junction capacitance.
- R_i, in series with C_{gs}, represents the access channel resistance from the source side. R_{gd}, in series with C_{gd}, represents the access resistance from the drain side

and in the limit of very small drain voltage is equal to R_i.

- g_{ds} models output conductance.
- Transconductance g_m includes the delay τ of the drain current with respect to the gate voltage.
- Parasitic resistances are represented by R_g, R_s and R_d.
- Parasitic inductances are represented by L_s, L_d, and L_g. They become important at very high frequencies. In addition, L_g is bias dependent.

The extraction procedure consists of 7 steps.

1. Conversion from the measured $[S]_m$ parameters to the measured $[z]_m$ parameters
2. Subtraction of the parasitic series resistances from the $[z]_m$ matrix
3. Conversion from the intrinsic $[z]_m$ parameters to the $[y]_m$ matrix
4. De-embedding 8 intrinsic equivalent circuit parameters using the $[y]_m$ matrix
5. Calculation of the extracted intrinsic $[y]_e$ parameters
6. Conversion of the calculated $[y]_e$ parameters to the $[z]_e$ matrix
7. Determination of the parasitic inductances L_s, L_g, and L_d by subtracting the $[z]_e$ matrix from the $[z]_m$ matrix

Each of these extraction steps are detailed and illustrated next.

1) Convert measured $[S]_m$ parameters to $[z]_m$ parameters.

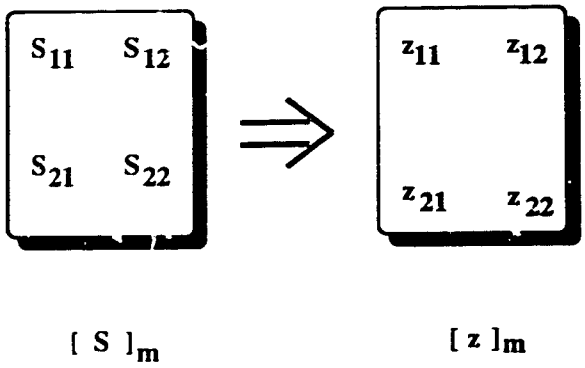

Figure E.3 *Conversion from the measured* $[S]_m$ *matrix to the normalized extrinsic* $[z]_m$ *matrix.*

- $[z]_m$ represents the matrix of normalized z parameters of the extrinsic device

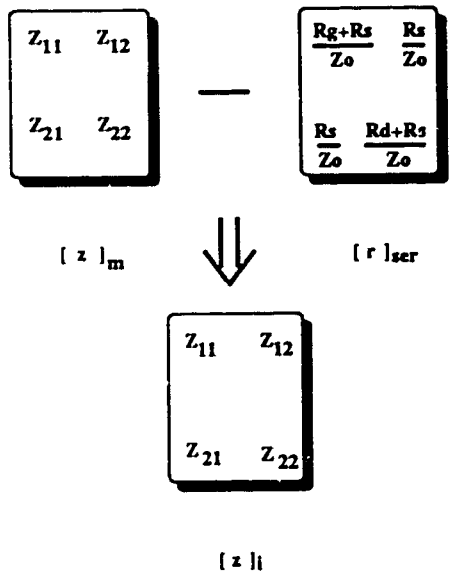

Figure E.4 *Subtraction of the parasitic series resistances from the normalized extrinsic* $[z]_m$ *matrix.*

2) Subtract the effect of the parasitic series resistances from the extrinsic $[z]_m$ matrix.

- The values of R_g, R_s, and R_d should be known at this stage from previous (dc) measurements.
- The impact of the series parasitic inductances is, for moment, neglected.

3) Convert the intrinsic $[z]_i$ parameter matrix to the intrinsic $[y]_i$ parameter matrix

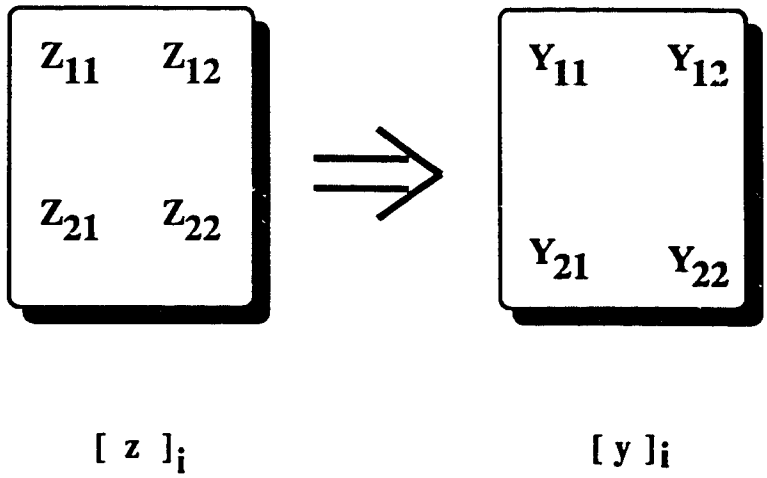

Figure E.5 *Convertion from the normalized intrinsic* $[z]_i$ *matrix to the normalized intrinsic* $[y]_i$ *matrix.*

4) De-embed the 8 (eight) intrinsic equivalent circuit parameters from the measured intrinsic y parameters, $[y]_i$, based on the equations:

$$y_{12} = Z_o \frac{R_{gd}(\omega C_{gd})^2 + j\omega C_{gd}}{1 + (\omega R_{gd} C_{gd})^2} \tag{E5}$$

$$y_{11} = Z_o \frac{R_i(\omega C_{gs})^2 + j\omega C_{gs}}{1 + (\omega R_{gd} C_{gd})^2} - y_{12} \tag{E6}$$

$$y_{21} = \frac{Z_o g_m e^{-j\omega\tau}}{1 + j\omega R_i C_{gs}} + y_{12} \tag{E7}$$

$$y_{22} = Z_o(g_{ds} + j\omega C_{ds}) - y_{12} \tag{E8}$$

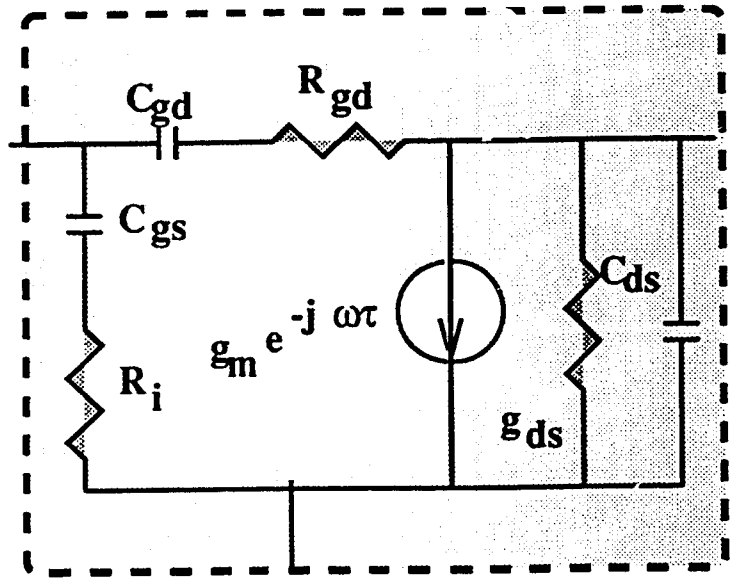

Figure E.6 *8-element intrinsic lumped equivalent circuit of the Si/SiGe/Si p-MOSFET.*

- C_{gd} is extracted from eqn. (E5) as the slope of the line

$$\frac{1}{\mathrm{Im}\left[\frac{Zo}{y_{12}}\right]} = \omega C_{gd}$$

Only the *lower frequency range* of the measured Y parameters is used.

- R_{gd} is extracted from eqn. (E5) as the average value of

$$\mathrm{Real}\left[\frac{Zo}{y_{12}}\right] = R_{gd}$$

Only the *lower frequency range* of the measured Y parameters is used.

- C_{gs} is extracted from eqn. (E6), as the slope of the line

$$\frac{1}{\mathrm{Im}\left[\dfrac{Zo}{y_{11}+y_{12}}\right]} = \omega C_{gs}$$

Only the *lower frequency range* of the measured Y parameters is used.

- R_i is extracted from eqn. (E6) as the average value of

$$\mathrm{Real}\left[\frac{Zo}{y_{11}+y_{12}}\right] = R_i$$

Only the *lower frequency range* of the measured Y parameters is used.

- C_{ds} is extracted from eqn. (E8), as the slope of the line

$$\mathrm{Im}(y_{22}+y_{12}) = \omega C_{ds}$$

Only the *lower frequency range* of the measured Y parameters is used.

- g_{ds} is extracted from eqn. (E8), as the average value of

$$\mathrm{Real}(y_{22}+y_{12}) = g_{ds}$$

Only the *lower frequency range* of the measured Y parameters is used.

- g_m is extracted from eqn. (E7), as the average of

$$\mathrm{Real}(y_{21}-y_{12}) = g_m$$

Only the *lower frequency range* of the measured Y parameters is used.

- τ is extracted from eqn. (E7), as the average value of

$$\frac{\text{atan}(gmr/gmi)}{\omega} = \tau$$

where

$$gmr = \frac{\text{Real}(y_{21}-y_{11})}{Zo} - \frac{\text{Im}(y_{21}-y_{11})}{Zo\omega R_i C_{gs}}$$

$$gmi = \frac{\text{Real}(y_{21}-y_{11})}{Zo\omega R_i C_{gs}} - \frac{\text{Im}(y_{21}-y_{11})}{Zo}$$

Only the ***higher*** frequency range of the measured Y parameters is used.

5) Calculate the extracted intrinsic Y parameters $[y]_e$ using eqns. (E5) - (E8).

6) Convert $[y]_e$ to $[z]_e$

7) Determine the series inductances L_s, L_g, and L_d by subtracting $[z]_e$ from $[z]_m$ and fitting to straight lines using only the high frequency range of the data.

As an illustration, Figs. E.8.a and b show the bias dependence of R_i and τ, respectively, as extracted from numerical simulation results, for a 0.25μm×30μm Si/SiGe/Si p-MOSFET.

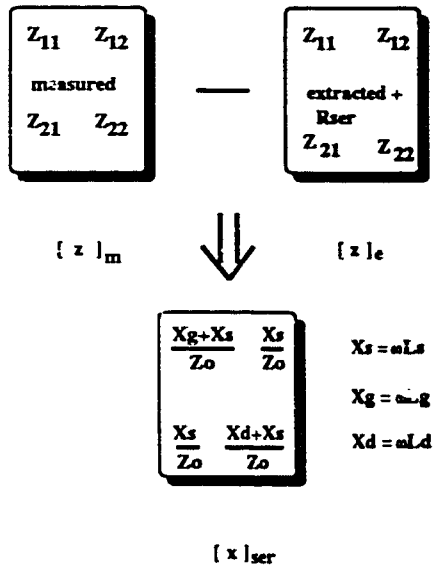

Figure E.7 *Extraction of the parasitic series inductances.*

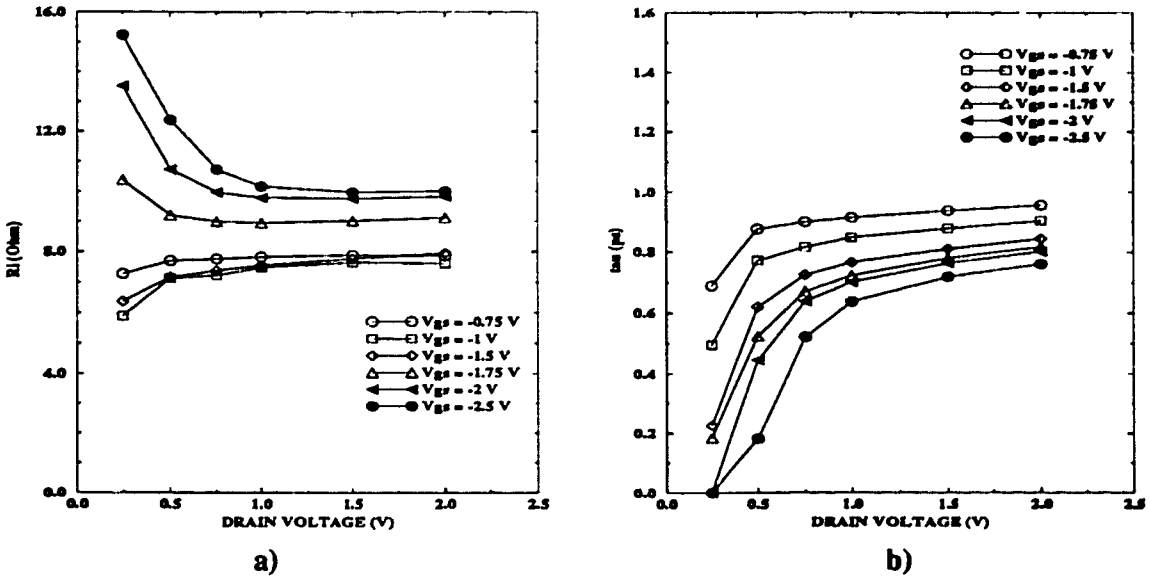

Figure E.8 *Bias dependence of the extracted channel access resistance* R_i *(a) and of the transconductance delay* τ *(b) for a* 0.25μm×30μm *Si/SiGe/Si p-MOSFET. Numerically simulated S parameters were used in the extraction.*

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