Towards a sub-2.5V, 100-Gb/s Serial Transceiver

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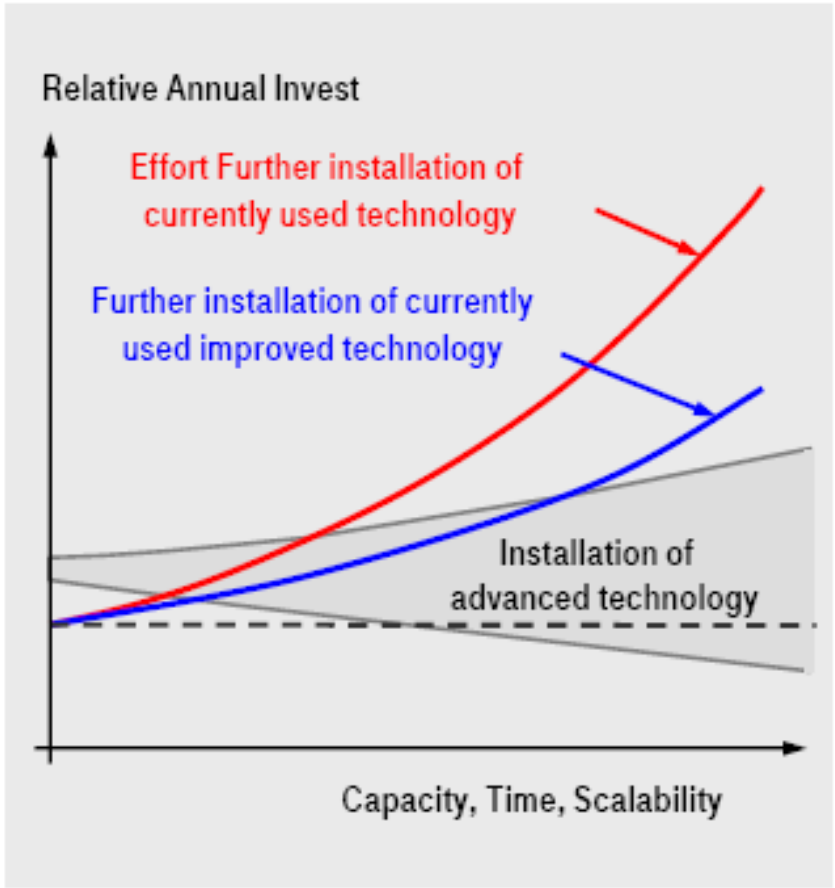
1) University of Toronto,
2) STMicroelectronics

Outline

- 100GE fundamentals
- Design methodology
  - Schematic level approach
  - Layout
- 90-Gb/s half-rate transceiver
- 100-Gb/s full-rate transceiver blocks
- Round-up

Why 100 Gb/s?

Network traffic growth (from IEEE802.3 HSSG)



- Increase of the network traffic capacity is expected to exceed Moore's Law.
- Forecasts expect 10 fold in 4 years

  ⇒ Factor of 100 in 8 Years
- The traffic of today would be only 1% of that traffic which is expected in about 8 years

  ⇒ Network build up for this demand

⇒ Need for high-speed interfaces at 100 Gbit/s or later on at 1 Tbit/s in the future networks

⇒ Technological breakthrough is required for cost effective solutions

Deutsche Telekom T-Systems

IEEE802.3 HSSG - 07/2007 – Plenary – San Francisco

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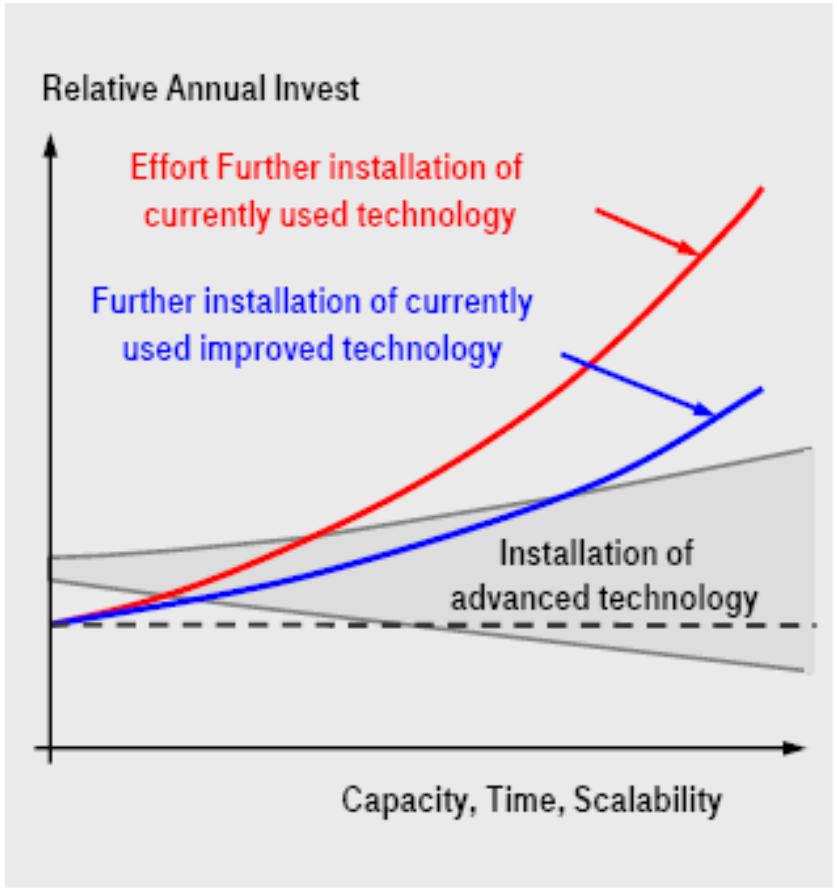

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Technological breakthrough demands a leap in serial data rate

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What are the applications?

Those that have demonstrated the need for bandwidth beyond existing capabilities:

- **High performance computing**
- **Video-on-demand delivery**
- **Data center**
- **Internet exchanges**
- **Metro: over 40km of SMF**

Blade Servers

1m over a backplane for inside-the-chassis communications

Rack Servers

10m over copper cables for switching within a server rack or row

Pedestal Servers

100m over OM3 MMF to connect systems across the data center

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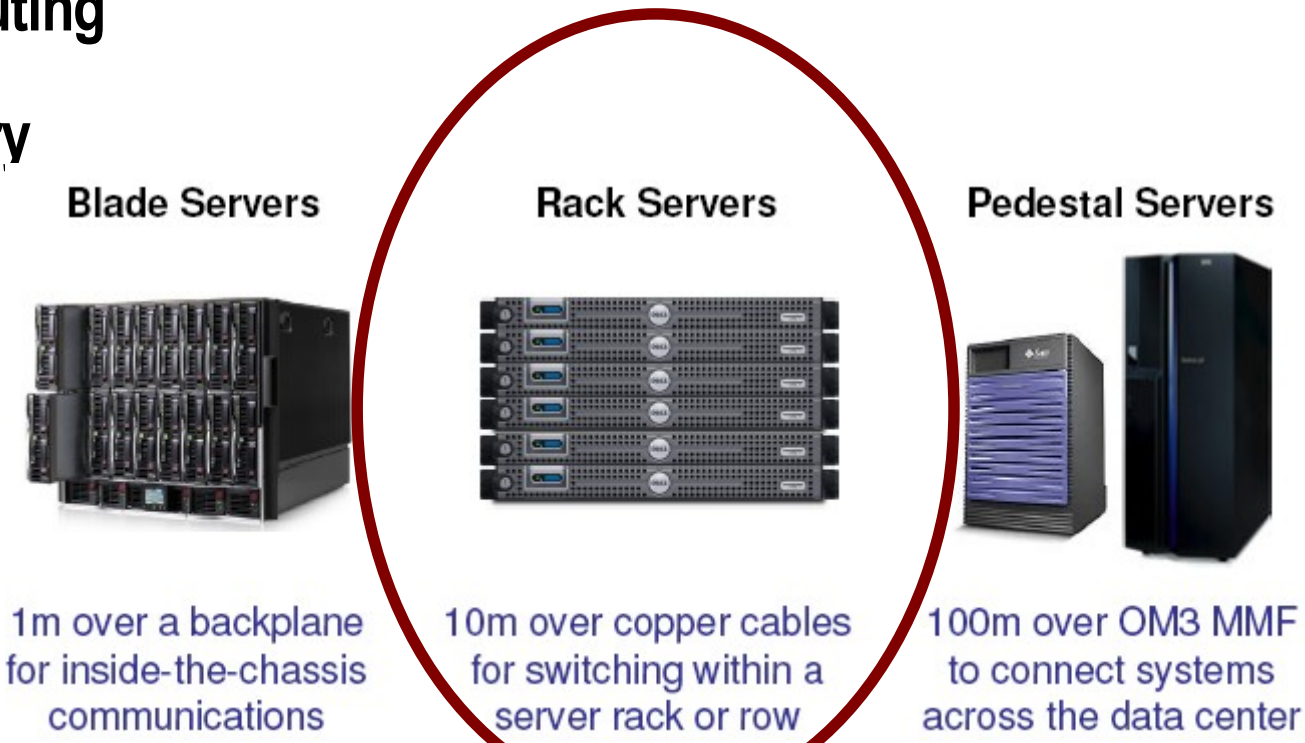

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- 107Gb/s serial OOK
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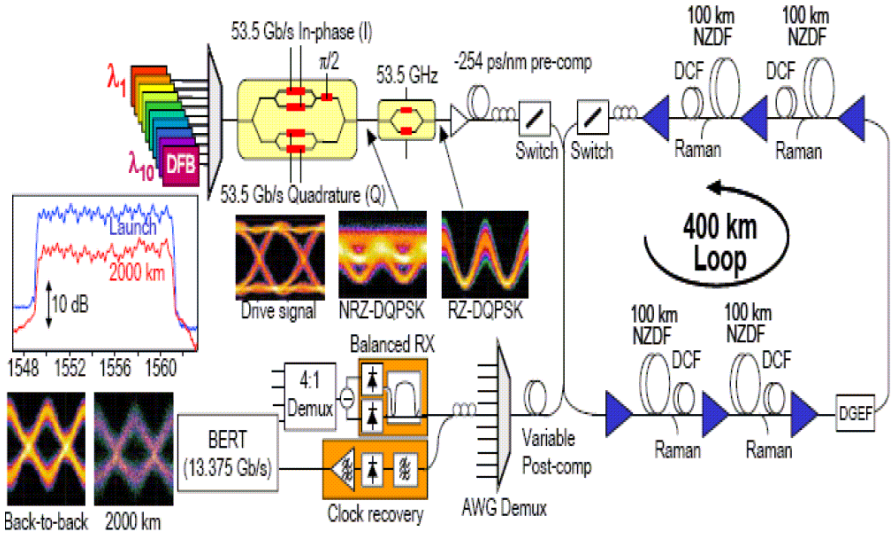

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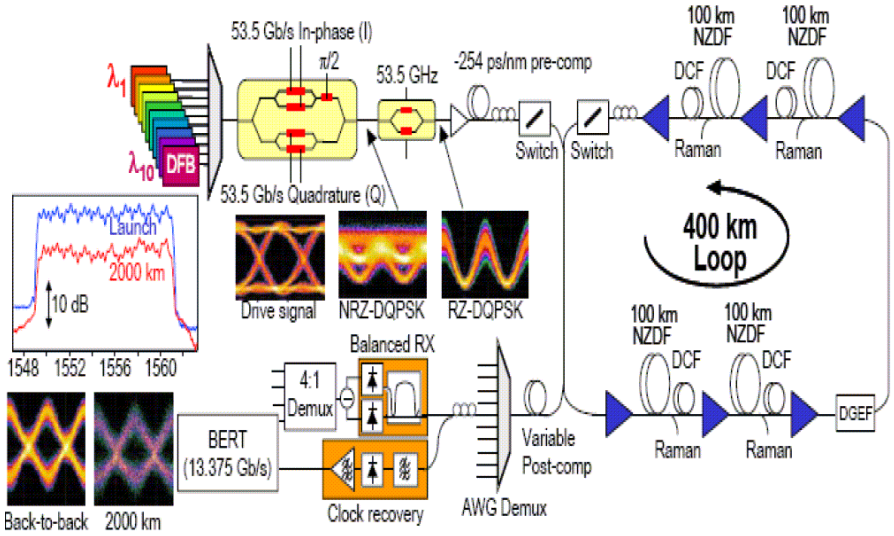
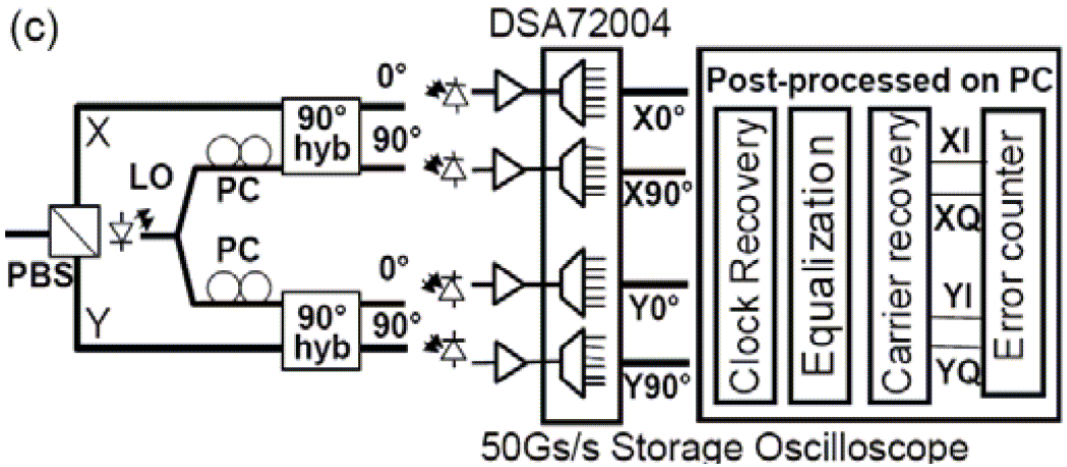
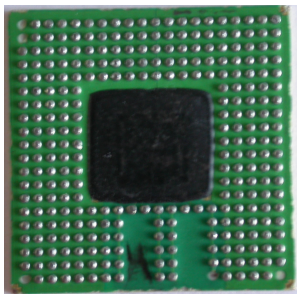
  - 4x 5-6bit, 54GS/s ADCs and DSP





100-Gb/s Serial Transceiver

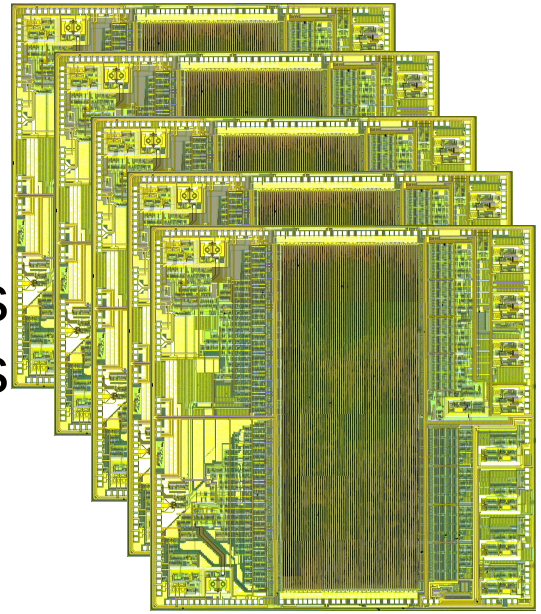
100 Gb/s

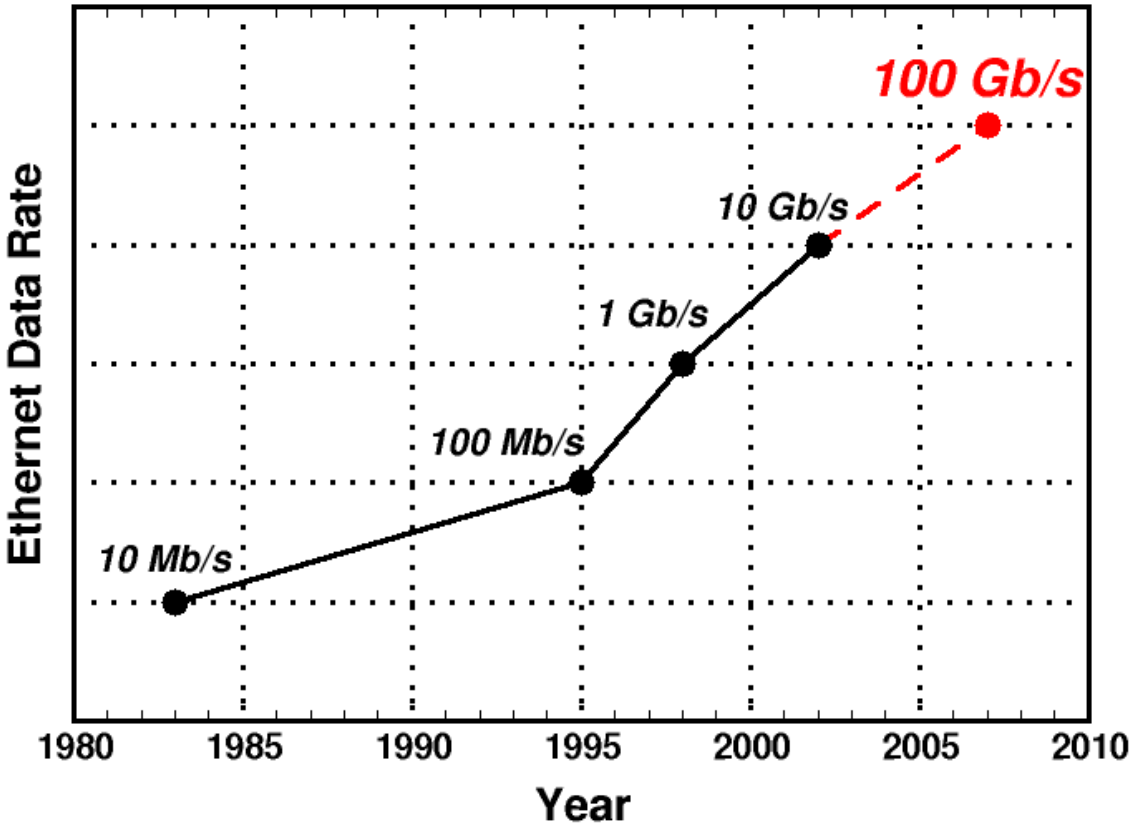


should consume less power and cost less than

3W, $250

5 x 10 Gb/s
2 x 40 Gb/s





- **10-GE CMOS transceiver**

0.8W from 1.2 V and < $50

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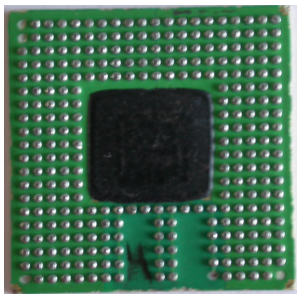

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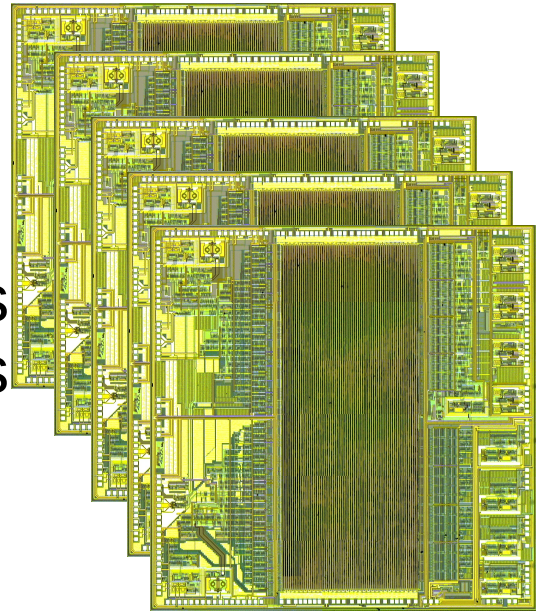

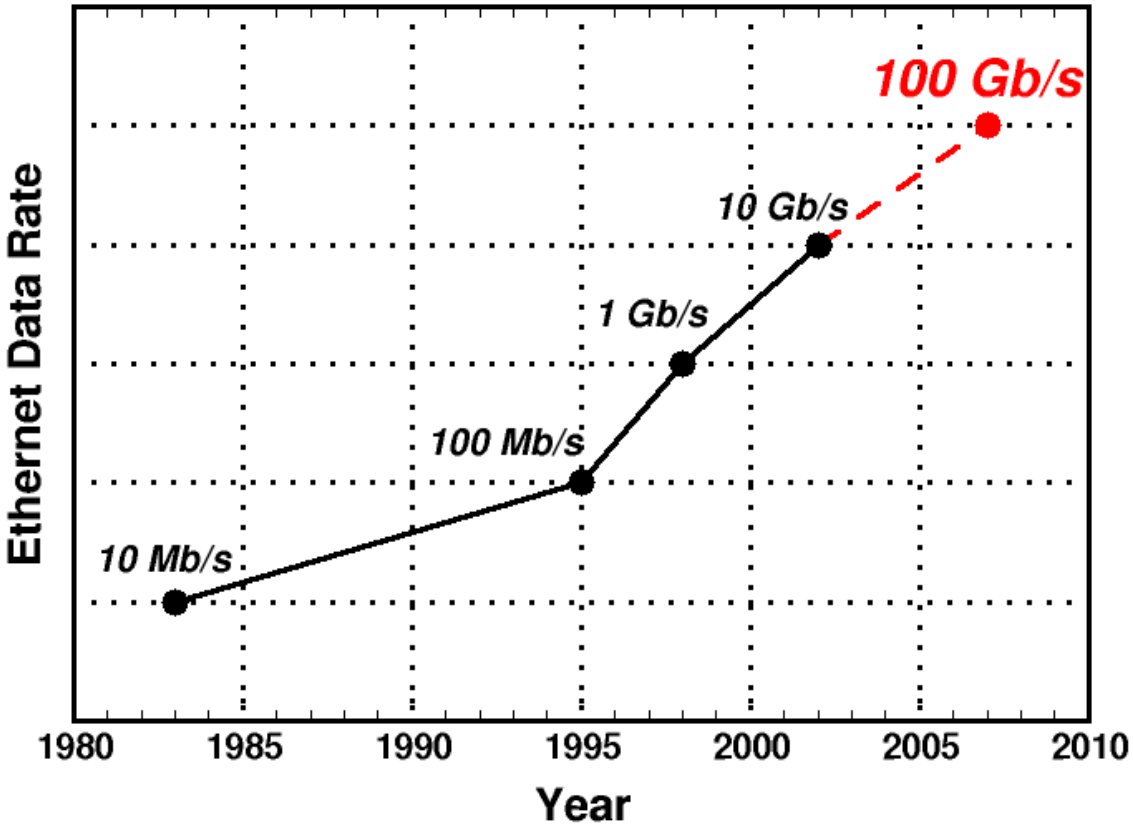

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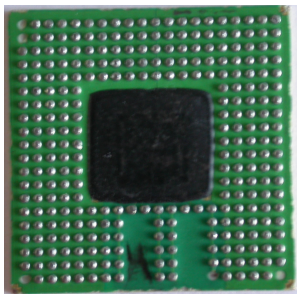

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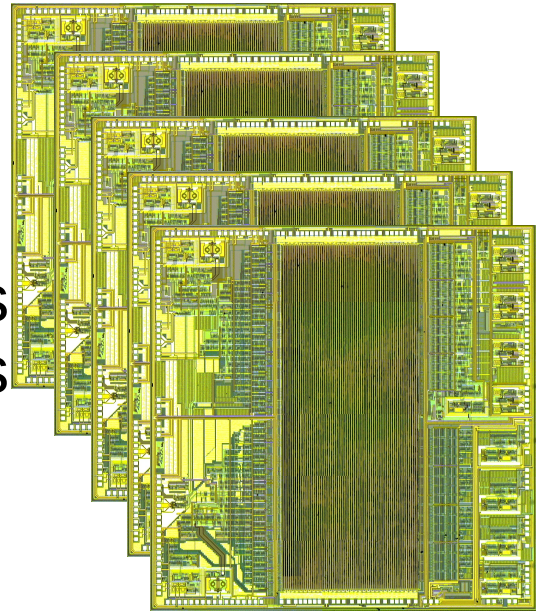

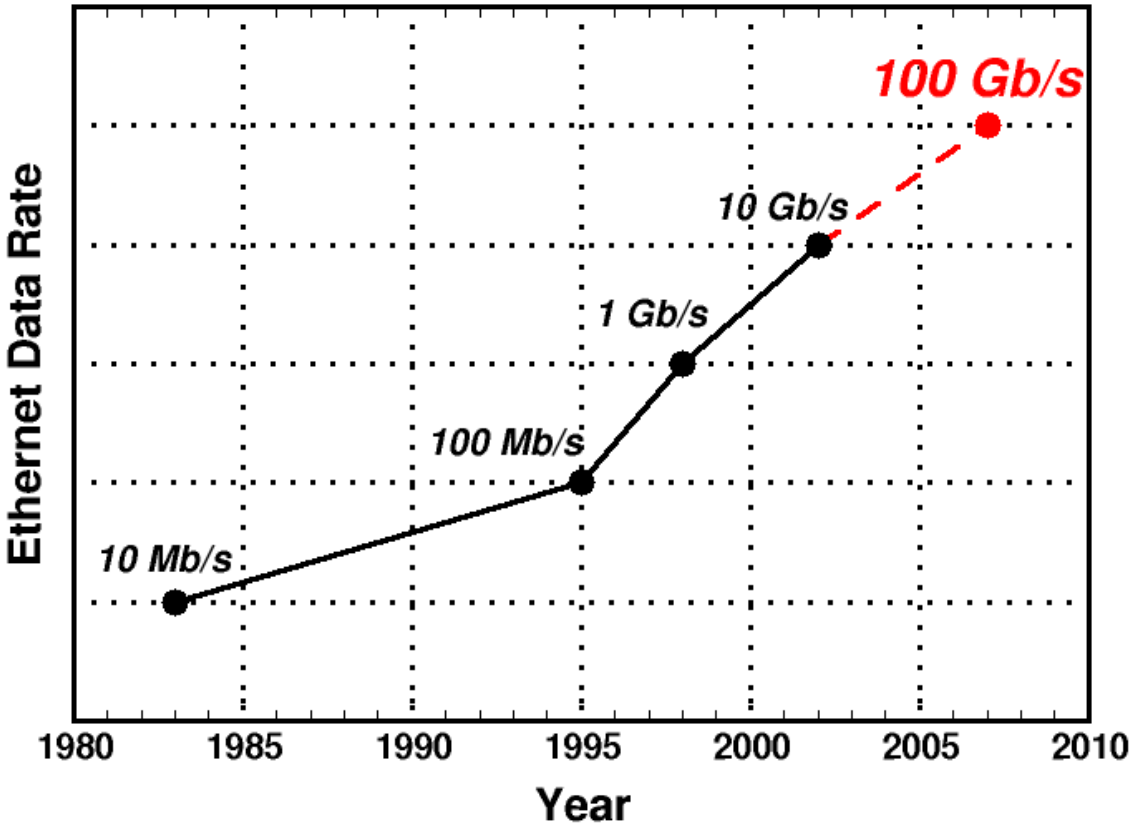

- **10-GE CMOS transceiver**

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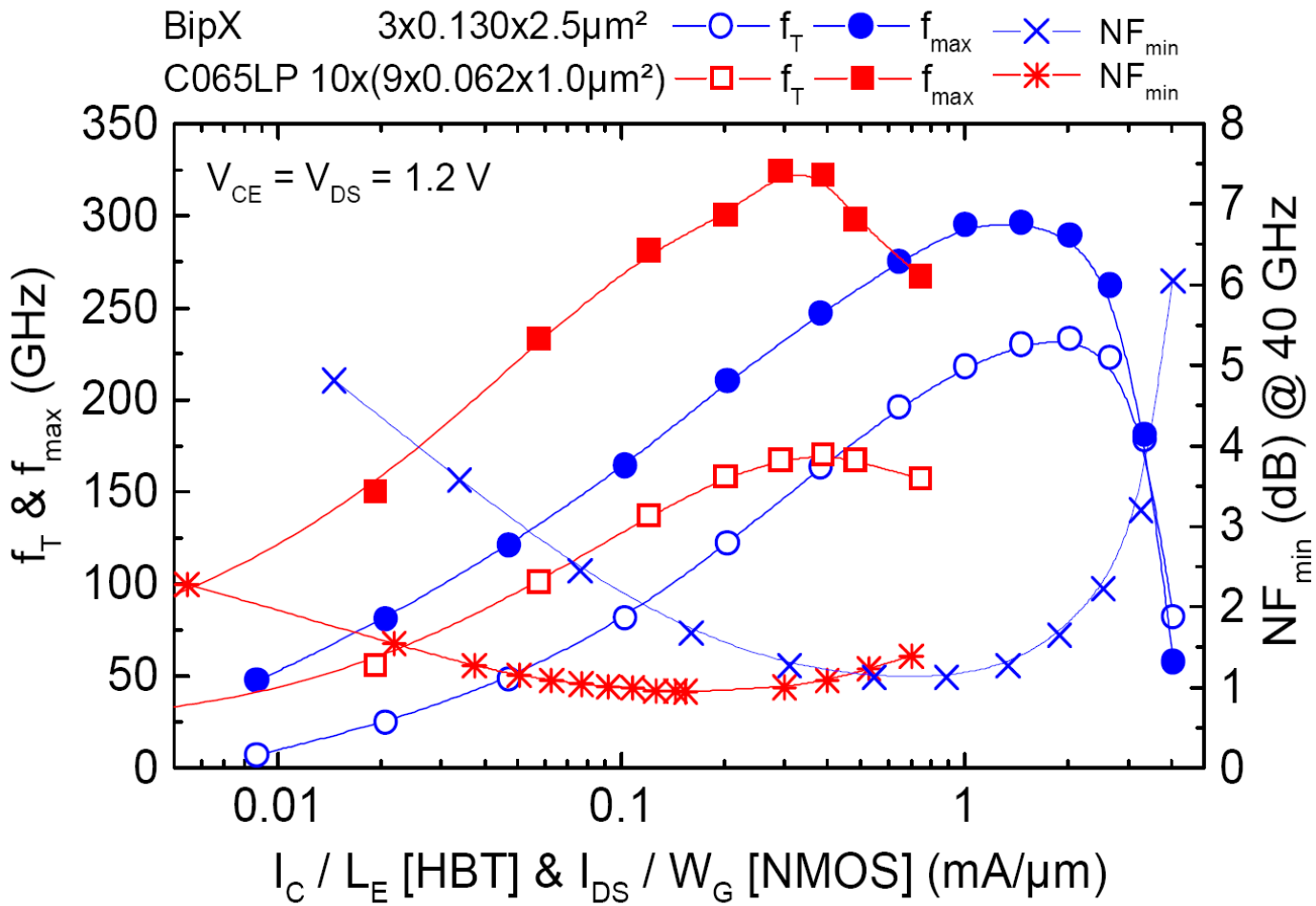
- **40+ Gb/s SiGe-HBT ICs too power hungry and 3.3V supply**

- **Need lower supply logic with fewer and lower tail currents per gate**

What are the options?

- Low-voltage (sub-2.5V) BiCMOS logic with 300-GHz HBTs
- 1.2V 45-nm GP CMOS CML logic without current source

65-nm LP n-MOS vs. SiGe HBT

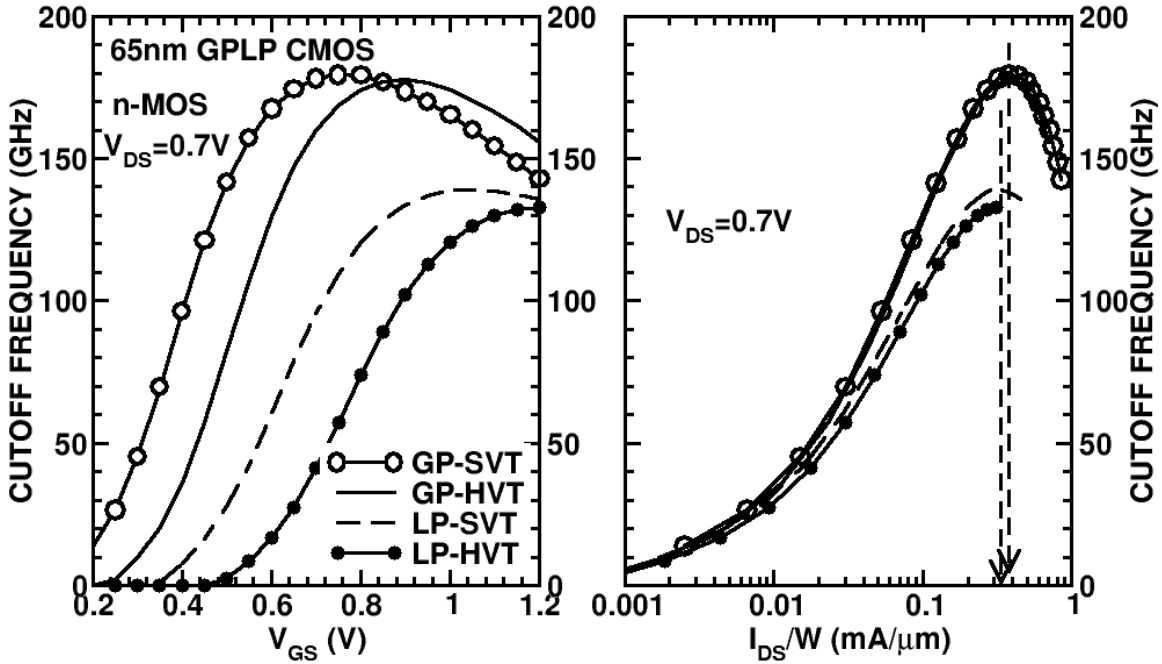


[P. Chevalier et al. CSICS-2006]

- Comparable high frequency performance
- Only difference: g_m/I (Gain/I), V_{swing} => HBT wins in dynamic range = length of data link

GP vs. LP 65-nm CMOS

- GP 30% faster than LP and 300mV lower V_{GS} => lower power!



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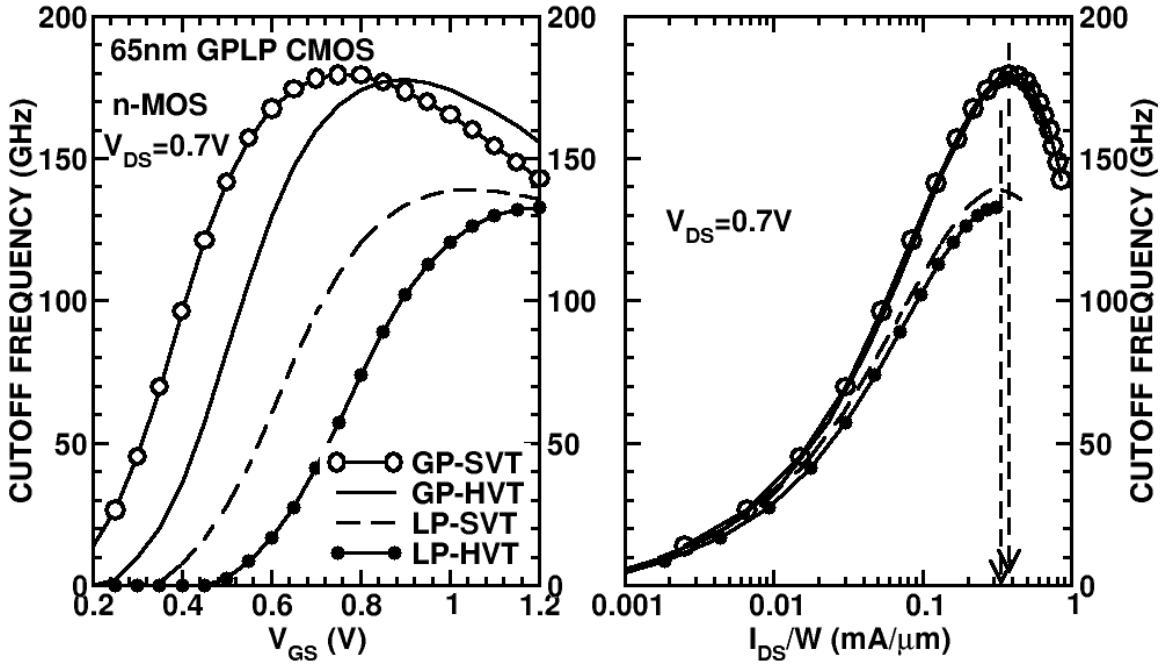

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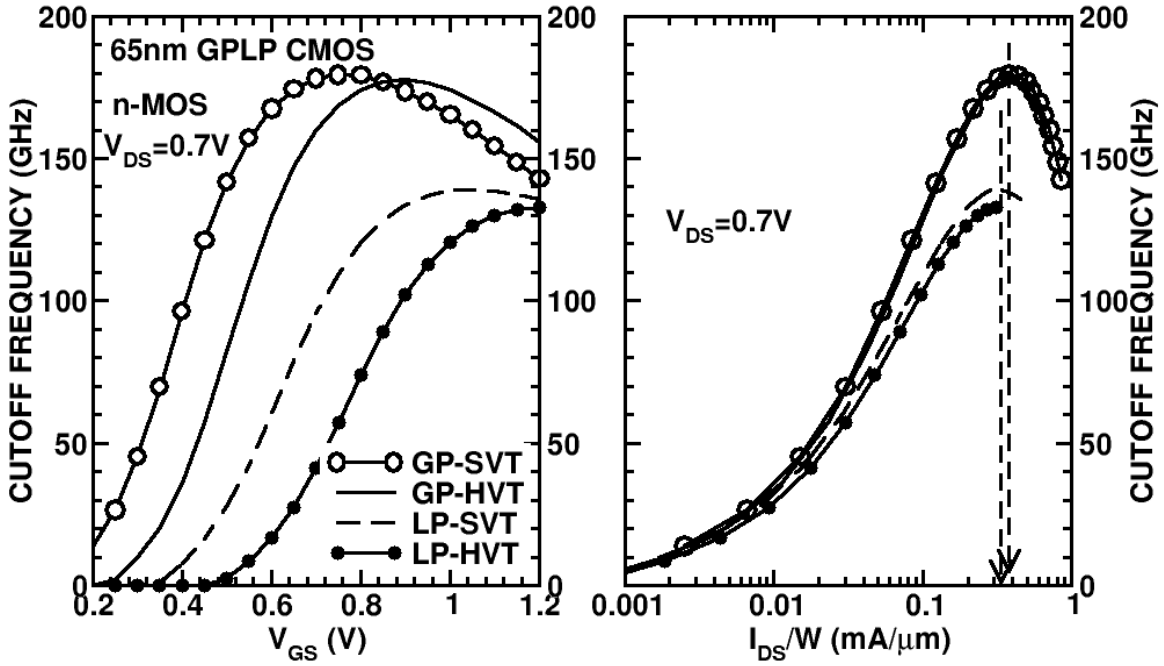

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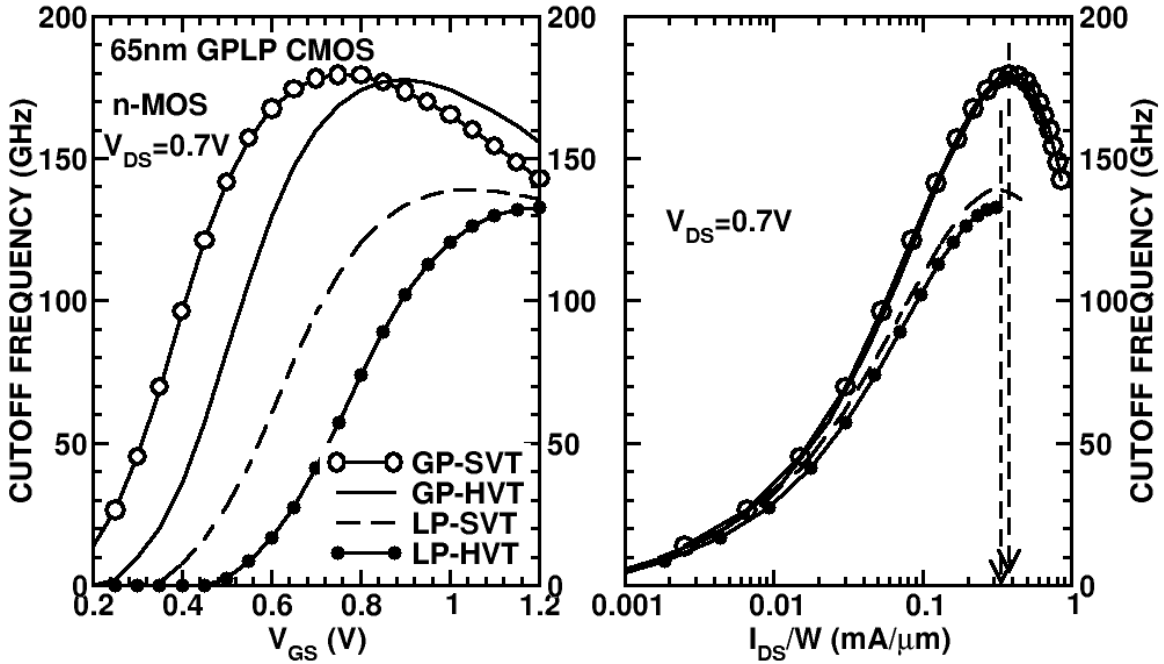
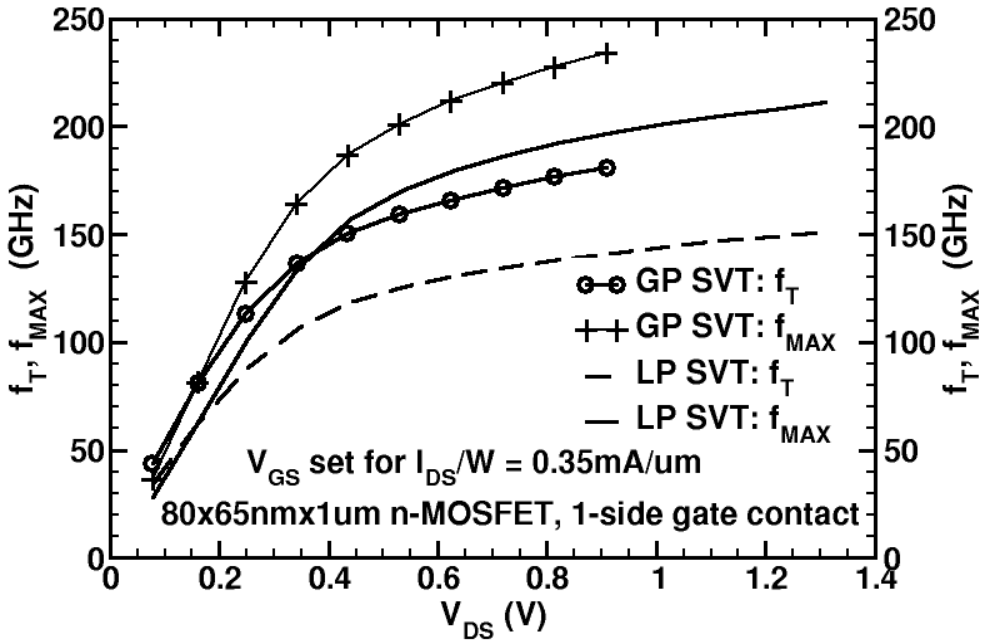
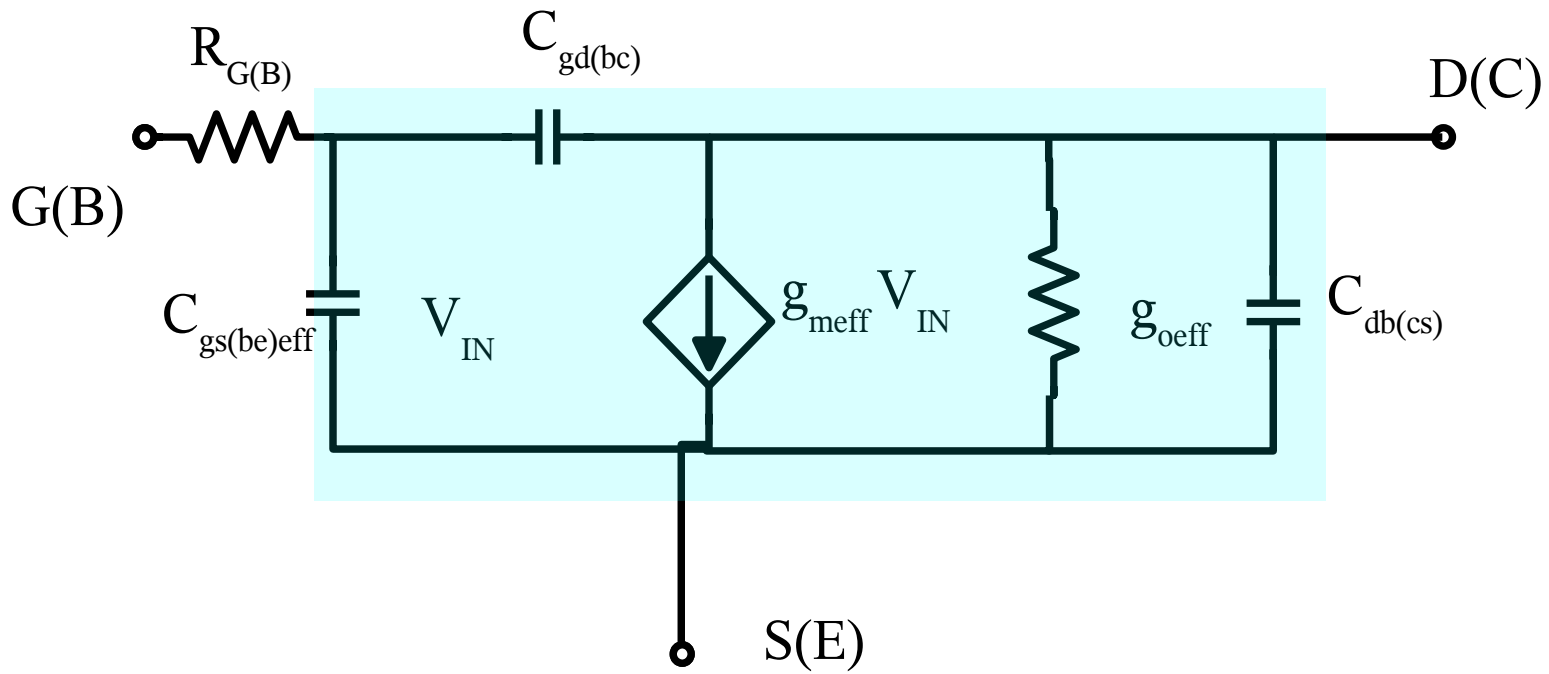
- f_T and f_{MAX} increase with V_{DS}



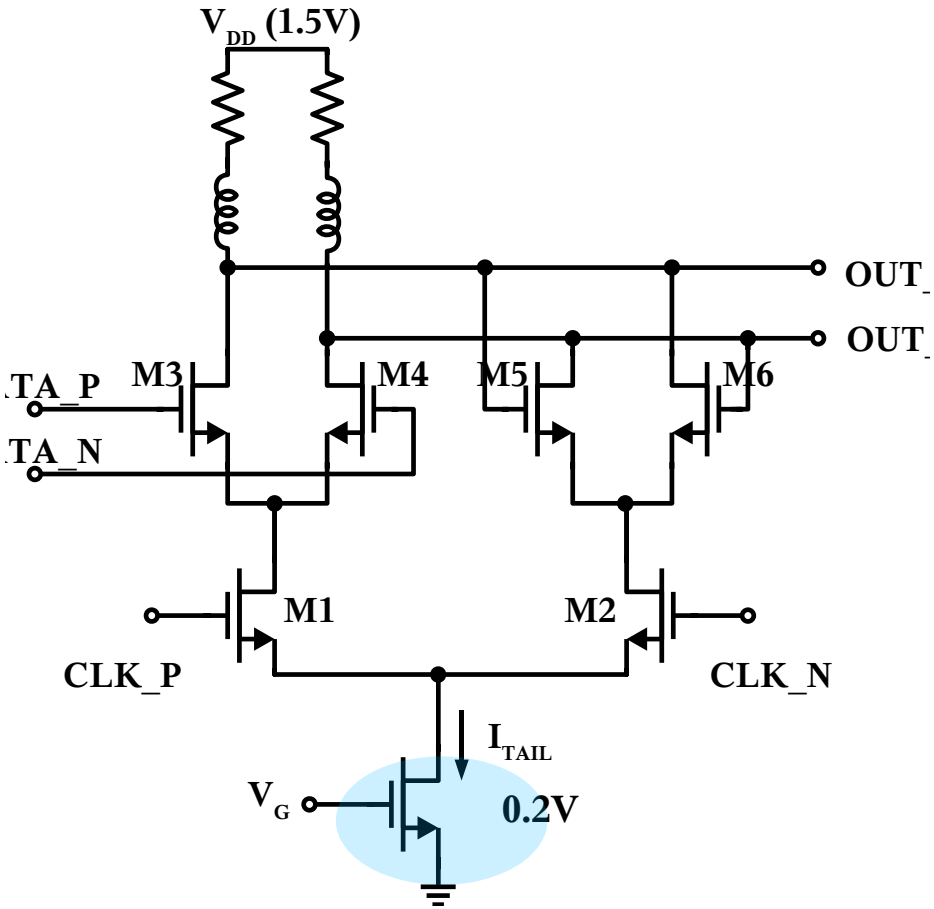


FET/HBT small-signal circuit including degeneration



- $R_s(R_E)$ included in $R_{G(B)}$, g_{meff}, g_{oeff}, f_T and C_{gseff}/C_{beeff}
- $Z_{in} \cong R_g + R_s - jf_T/(fg_{meff})$; $g_{meff} = g_m/(1+g_m R_S)$
- In 300-GHz SiGe HBTs $g_m R_E = 3.5$ => built-in feedback, stable over T

2-MOSFET stack topologies (S. Voinigescu et al. CICC-05)



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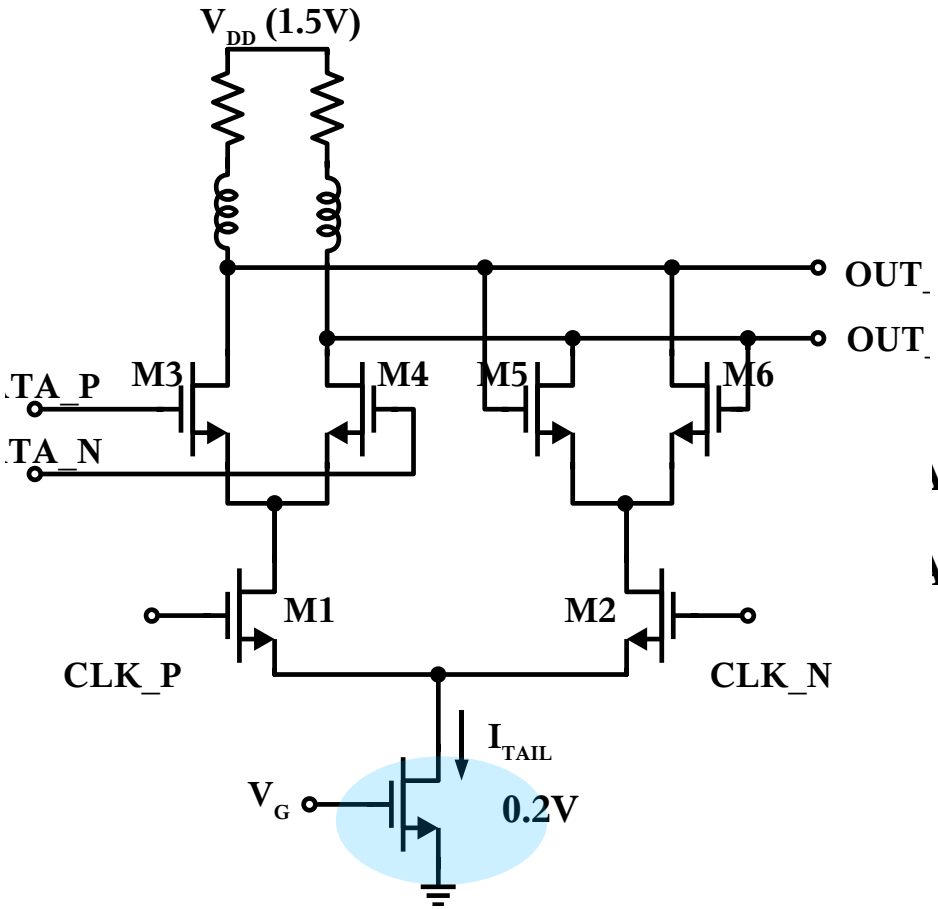

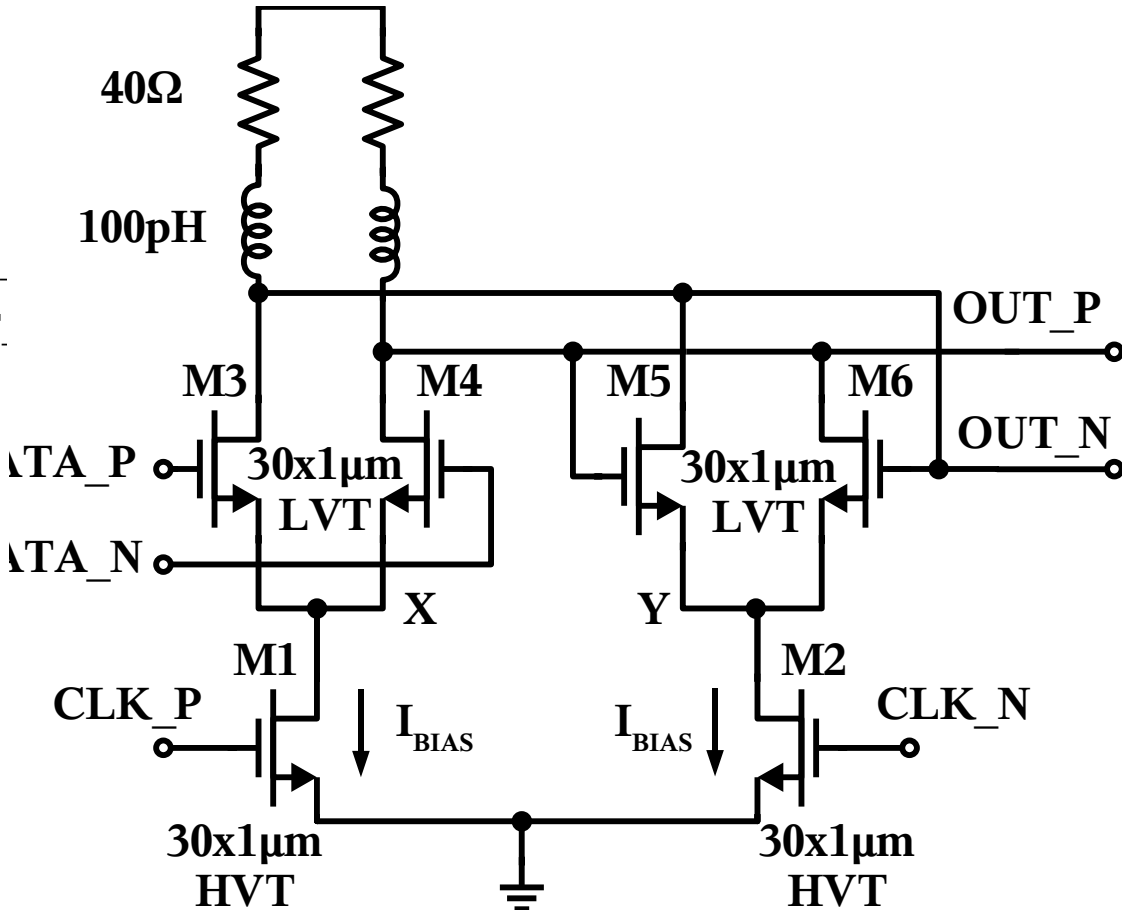

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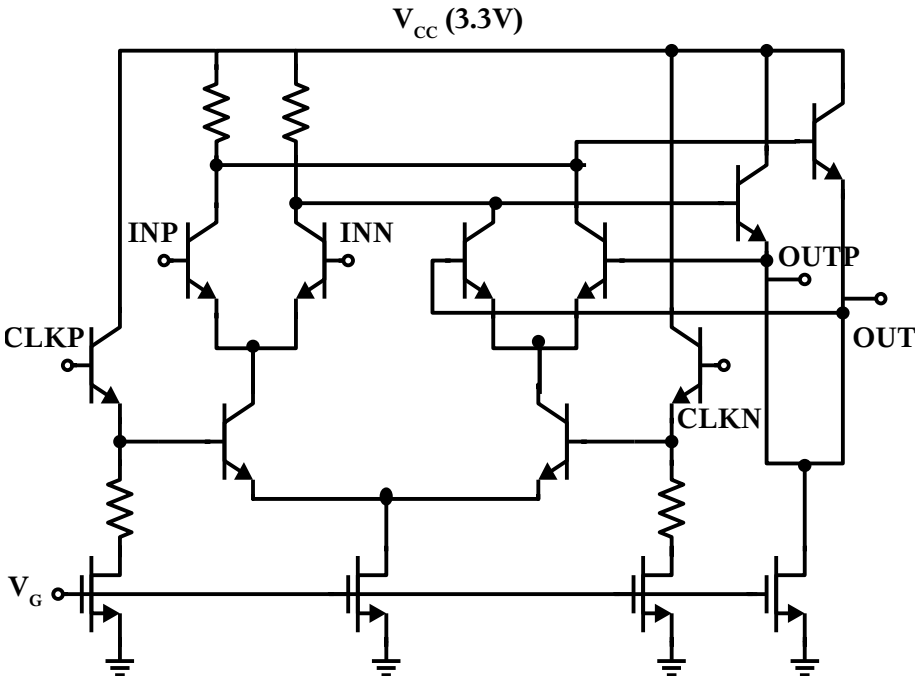
- V_{GS} of data FETs determines V_{DS} of clock FETs => LVT + HVT

High-speed, low-power BiCMOS latch (E. Laskin JSSC-Oct. 06)



- HBT ECL

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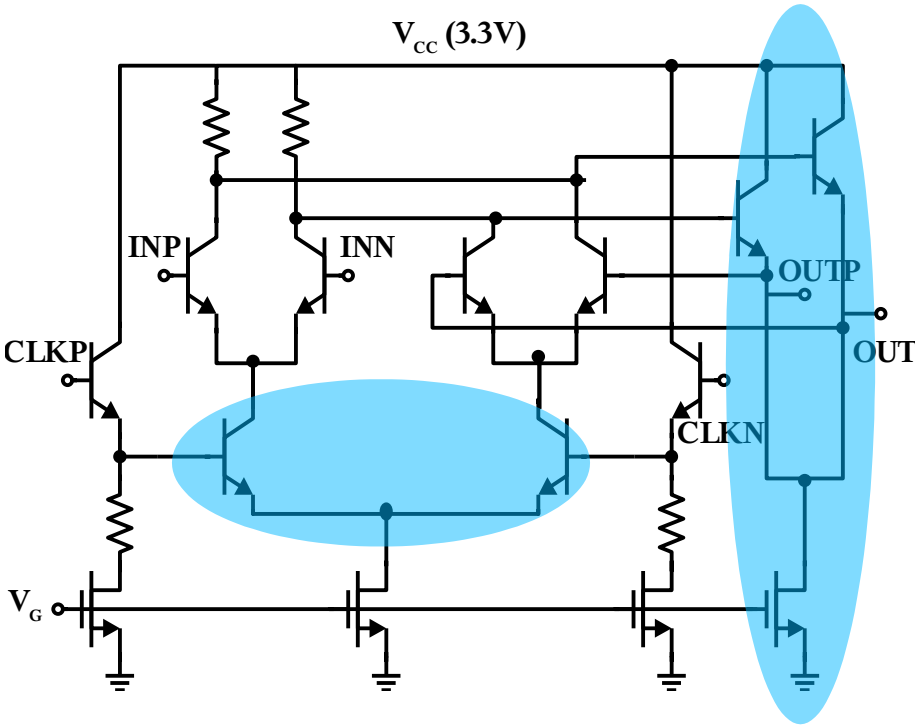

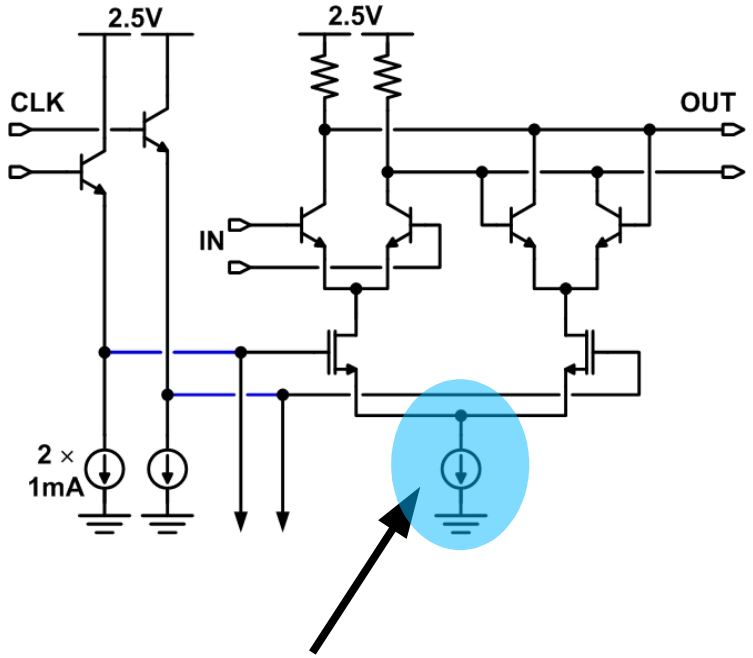

- HBT ECL to BiCMOS CML
- 3.3 V to 2.5 V and reduced number of tails

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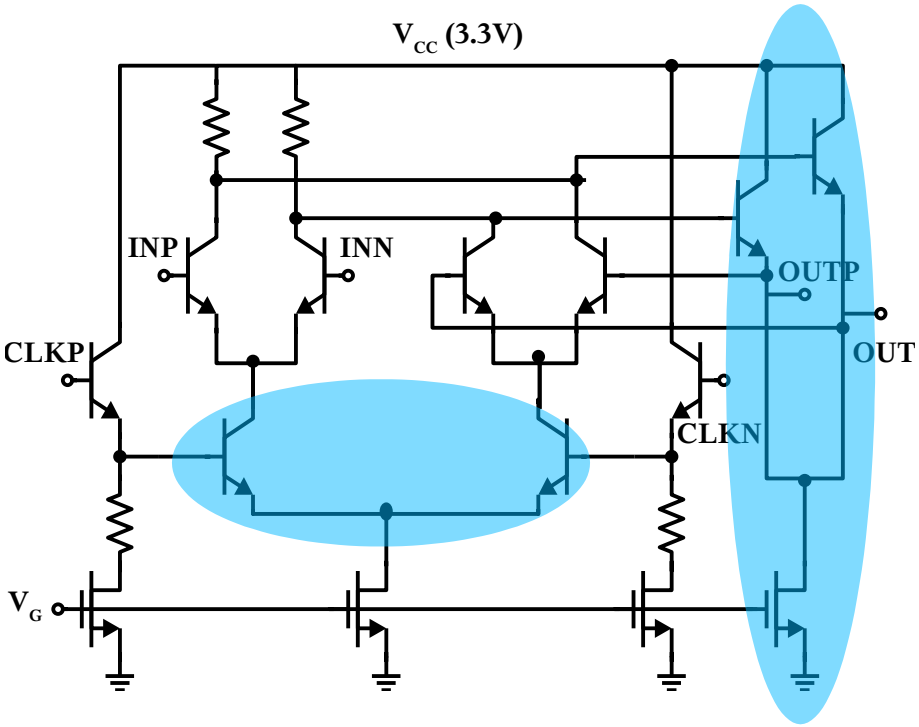
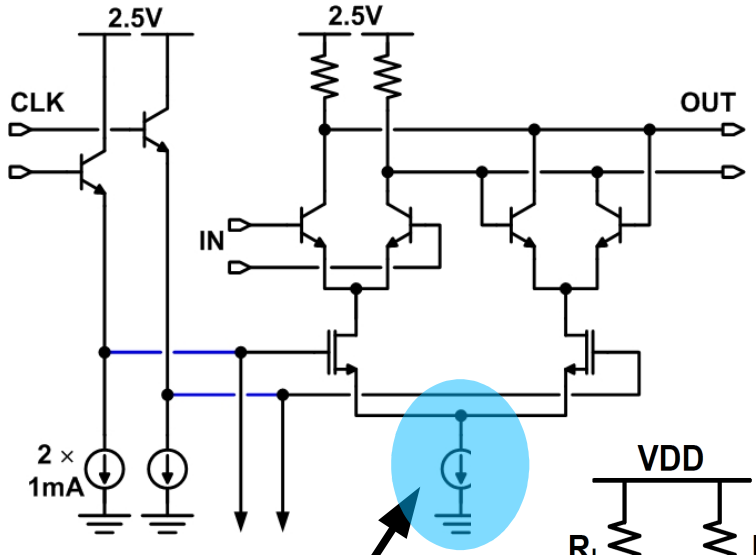
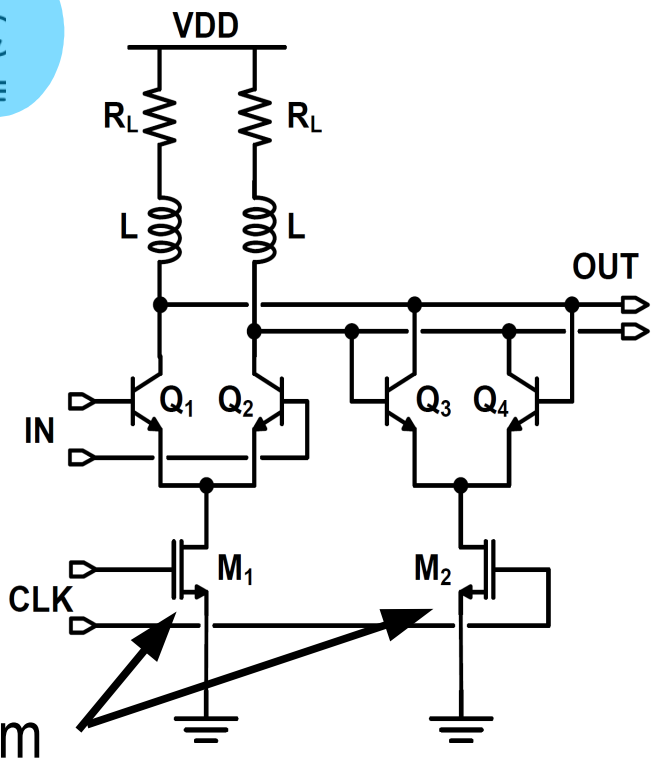




0.3 mA/μm



0.15 mA/μm

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- 1.8 V (lower power) at same speed

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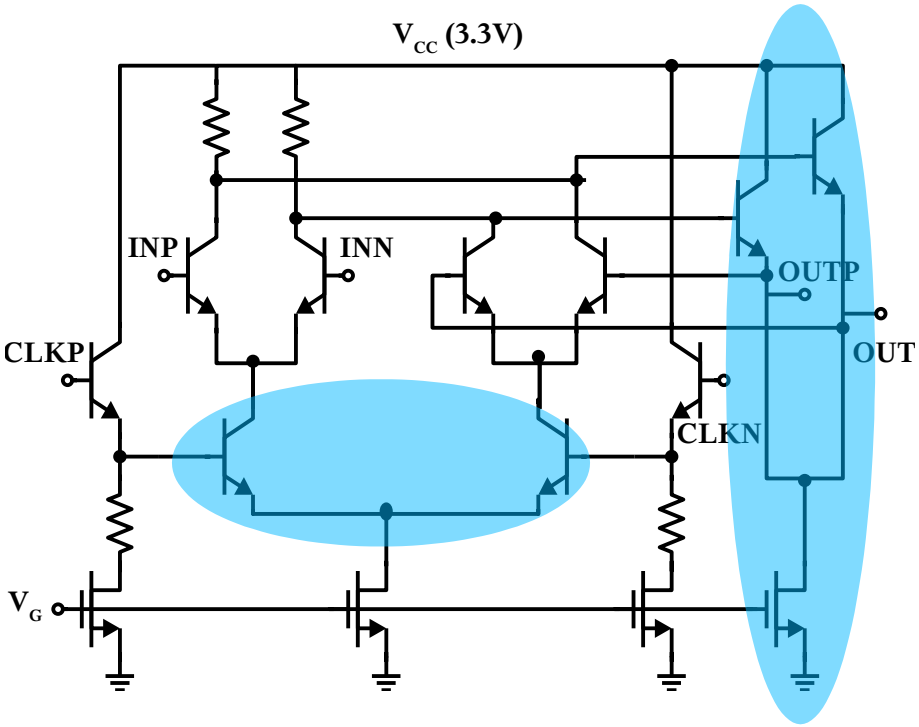

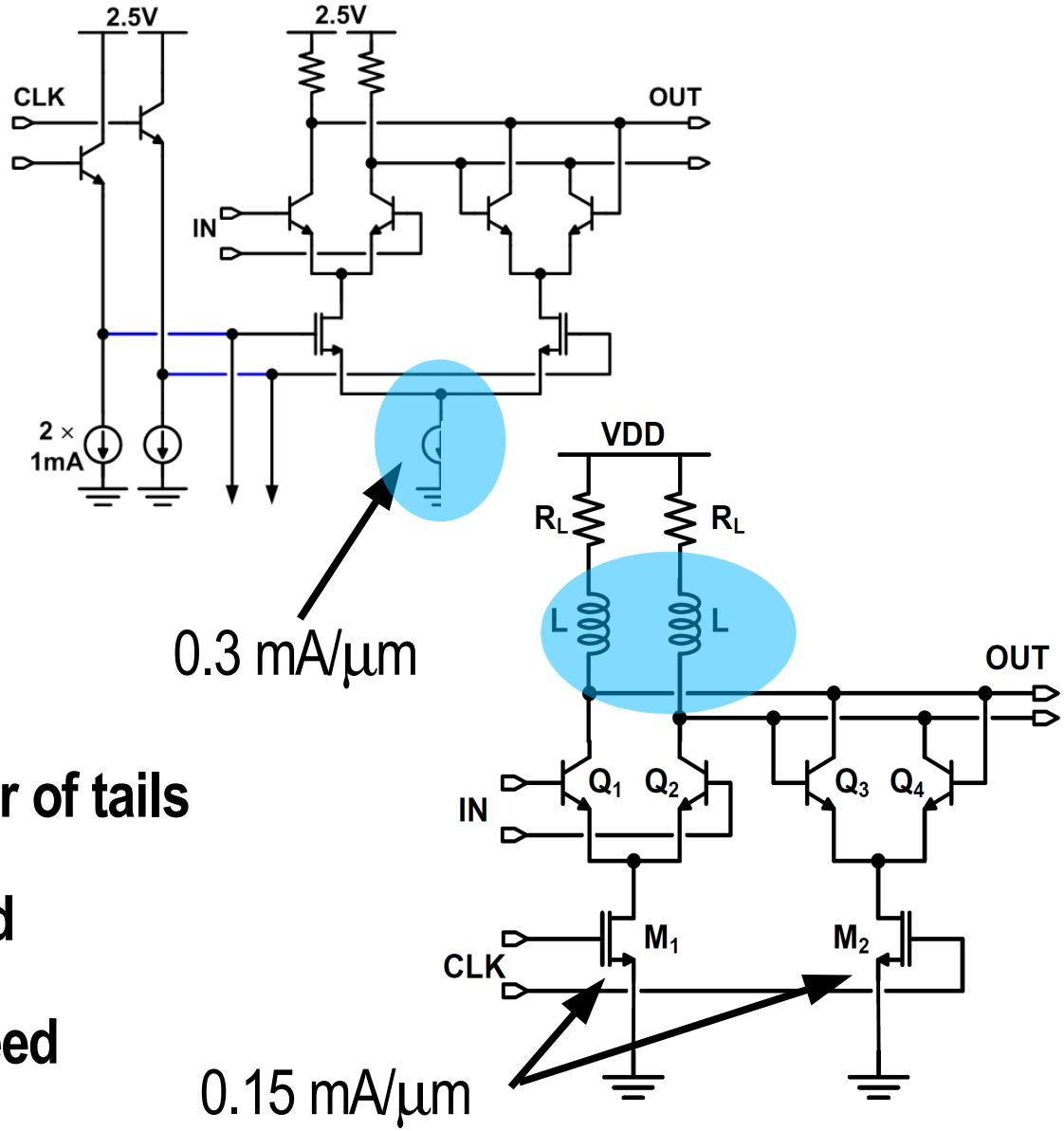

- HBT ECL to BiCMOS CML
- 3.3 V to 2.5 V and reduced number of tails
- 1.8 V (lower power) at same speed
- Inductive peaking to increase speed

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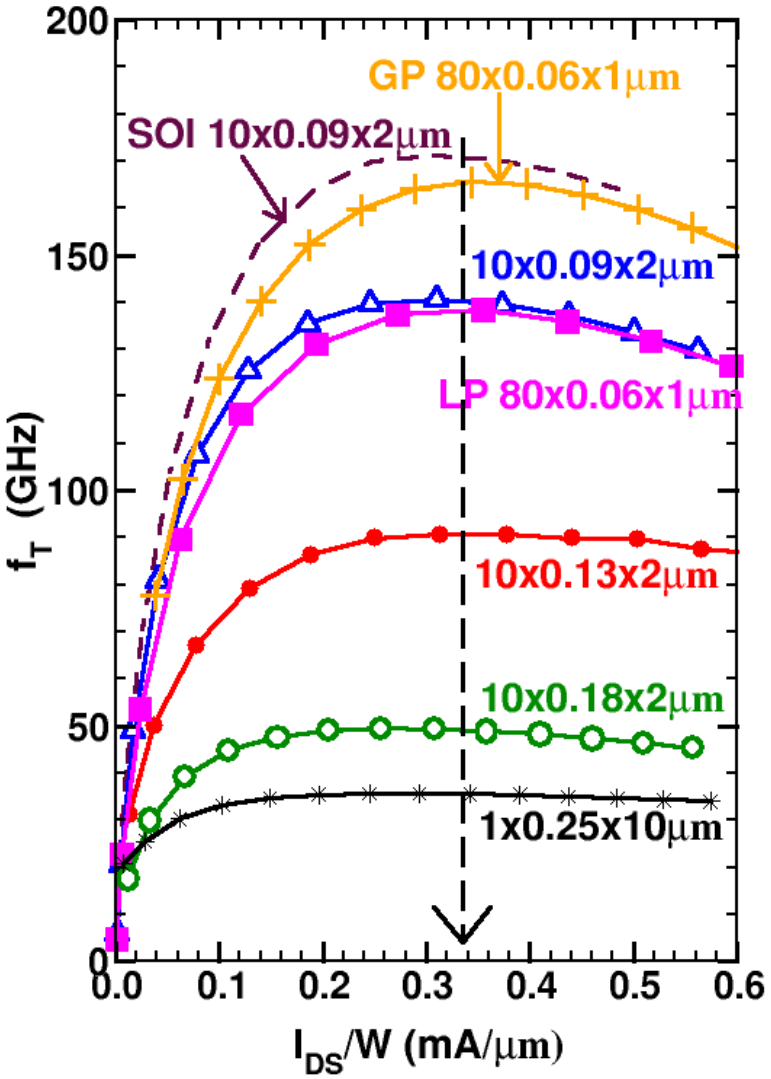
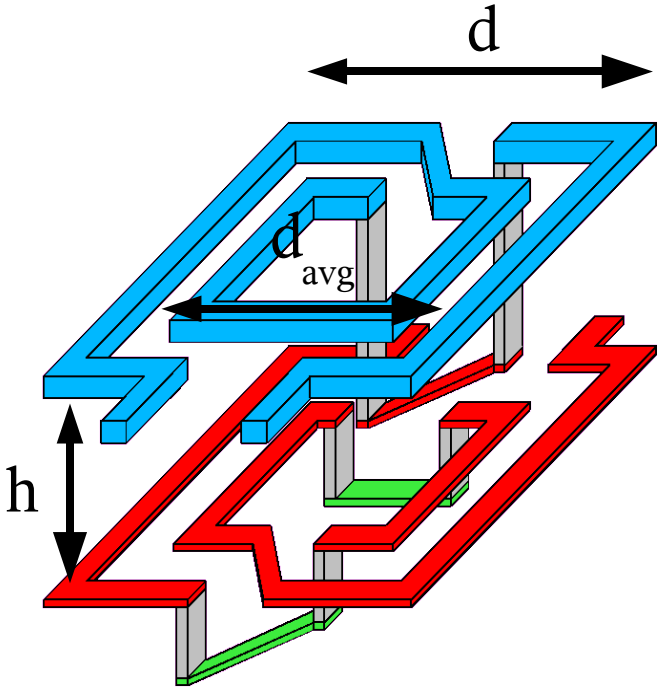
GP 65-nm CMOS scales as expected

- Future node performance is easy to predict from Dennard's 1974 constant-field scaling eqns.
- All MOSFETs (from all foundries) are practically the same.
- 0.15mA/μm to 0.45mA/μm is the recommended bias range



Scaling of inductors to 100+GHz

- f -> f×S, S = scaling factor, f = operation frequency
- W -> W/S, W= stripe width
- l -> l/S, l = total length of inductor winding
- d -> d/S, d = inductor external diameter
- d_{avg} -> d_{avg}/S, d = inductor average diameter
- h -> h/S, h = dielectric thickness
- t = constant, t = metal thickness



Frequency scaling equations of inductor π-model

$$L \approx \frac{6\mu_0 n^2 d_{avg}^2}{11d - 7d_{avg}} \longrightarrow \frac{L}{S} \approx \frac{6\mu_0 n^2 \left[\frac{d_{avg}}{S}\right]^2}{11\frac{d}{S} - 7\frac{d_{avg}}{S}}$$

$$C_{ox} = \frac{1}{2} l W \frac{\epsilon_{ox}}{h} \longrightarrow \frac{C_{ox}}{S} = \frac{1}{2}\frac{l}{S}\frac{W}{S}\frac{\epsilon_{ox}}{\frac{h}{S}}$$

$$C_p = n W^2 \frac{\epsilon_{ox}}{h_{M9-M8}} \longrightarrow \frac{C_p}{S} = n\left(\frac{W}{S}\right)^2 \frac{\epsilon_{ox}}{\frac{h_{M9-M8}}{S}}$$

$$SRF \approx \frac{1}{2\pi\sqrt{L(C_{OX} + C_p)}} \longrightarrow S \times SRF = \frac{1}{2\pi\sqrt{\frac{L}{S}\left(\frac{C_{OX}}{S} + \frac{C_p}{S}\right)}}$$

Scaling of inductors to 100+GHz (ii)

Outcome

- Inductors/transformers can be as small and inexpensive as transistors
- As in MOSFETs, series resistance does not scale

$$R_{DC} = \frac{\rho l}{W t} \rightarrow R_{DC} = \frac{\rho \frac{l}{S}}{\frac{W}{S} t}$$

$$R_{AC} = \frac{\rho \frac{l}{S}}{\frac{W}{S} \delta \left[1 - \exp\left(\frac{-t}{\delta} \right) \right]}$$

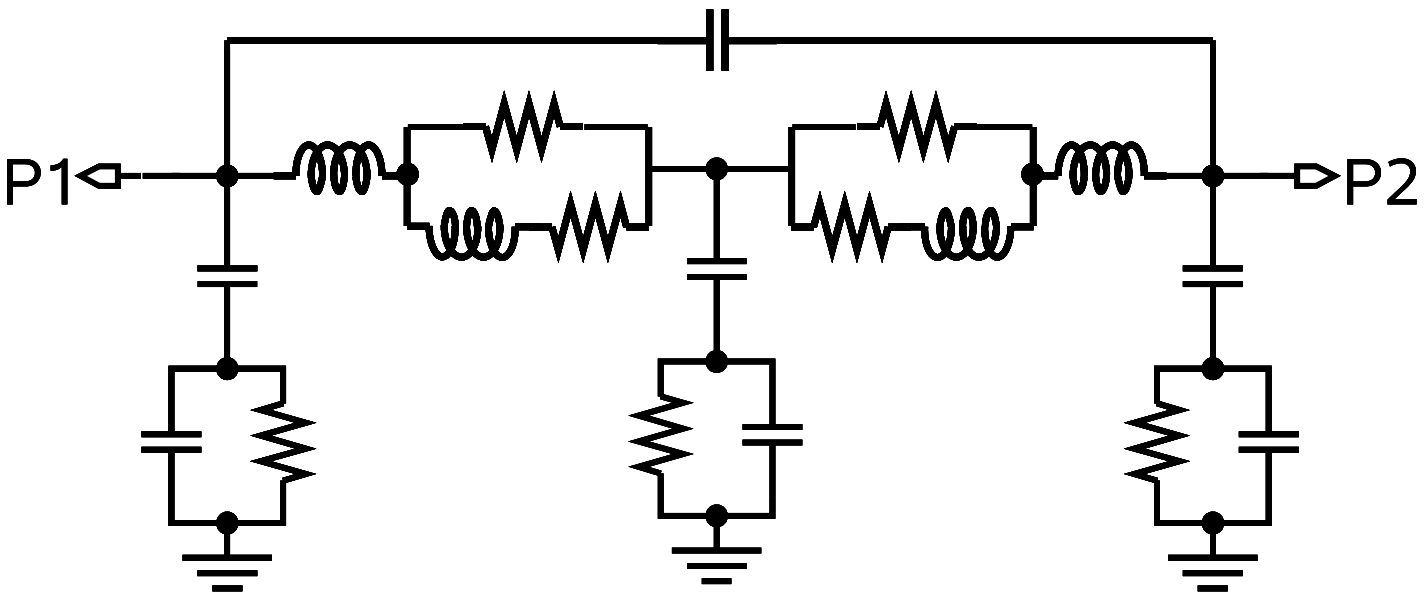
$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}}$$

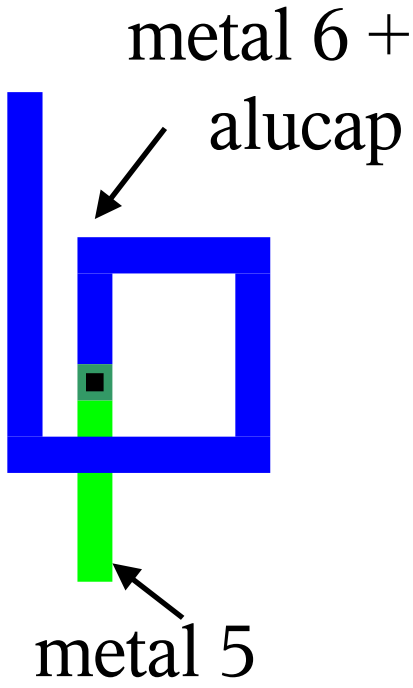
- The peak Q value remains the same, with PQF at f×S

$$Q = \frac{\omega \times S \frac{L}{S}}{R_{DC} + R_{AC}} = \frac{\omega L}{R_{DC} + R_{AC}}$$

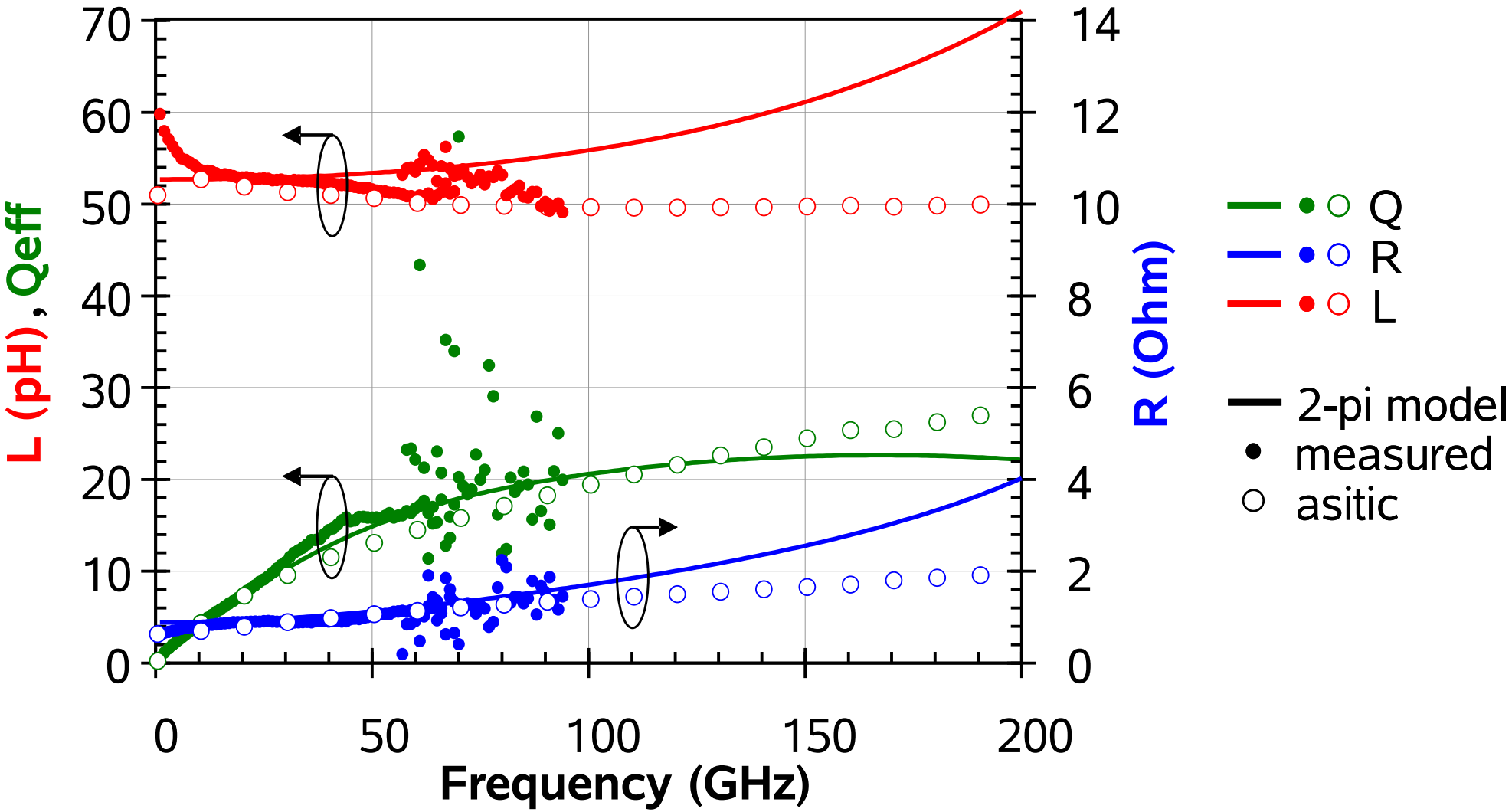
Inductor and interconnect modeling (E. Laskin RFIC-07)

- 44-pH inductor for the oscillator tank
- Shunted metals for low loss
- Designed using ASITIC, SRF > 400 GHz





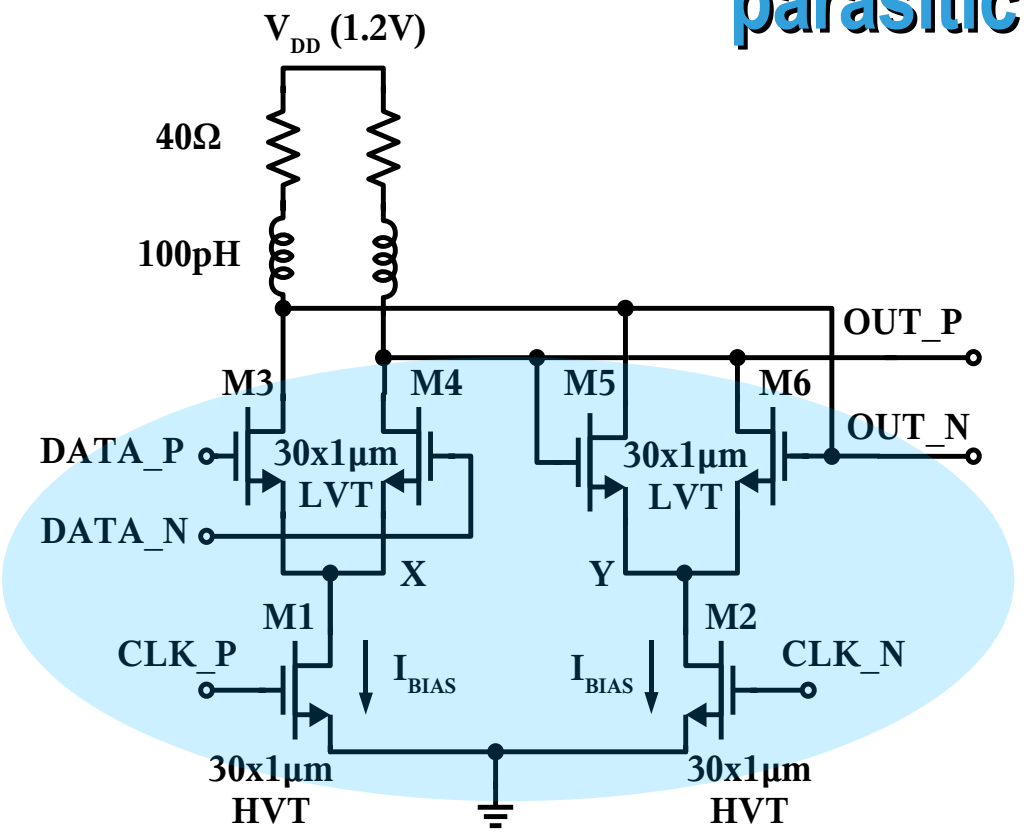
Inductor model verification through 94 GHz

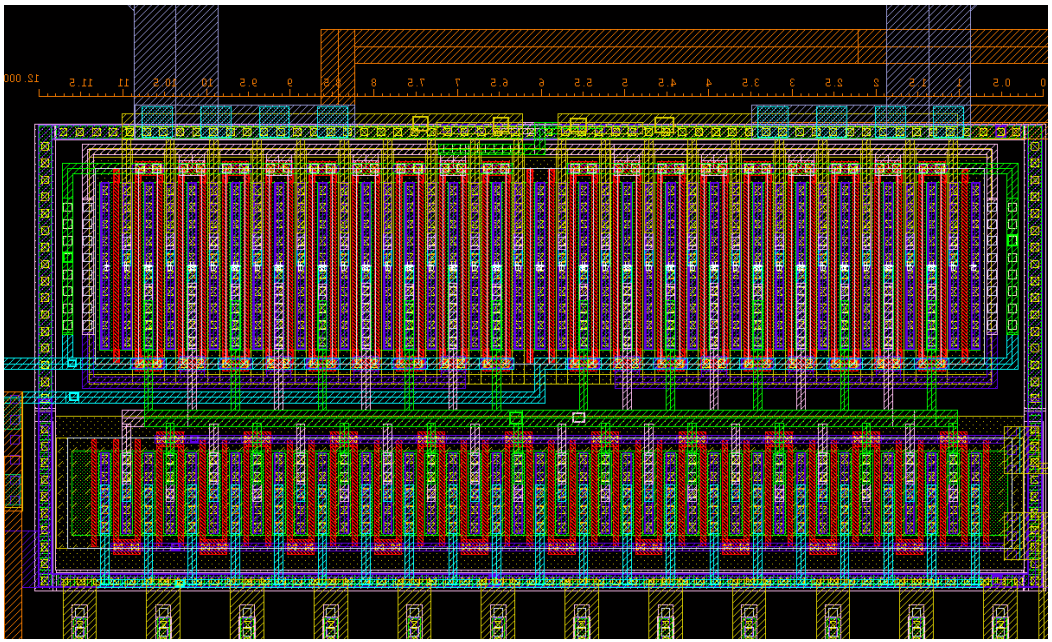


Key design methodology ideas

- Bias at constant current density to minimize PVT in nanoscale CMOS
- Avoid stacked-FET topologies to reduce impact of VT variation.
- Trade off bias current with inductive peaking to minimize tail currents
- Use analytical equations for 1st. cut design of all circuits
- Add gate resistance to digital CMOS model
- Layout in nanoscale CMOS is >> important than schematic

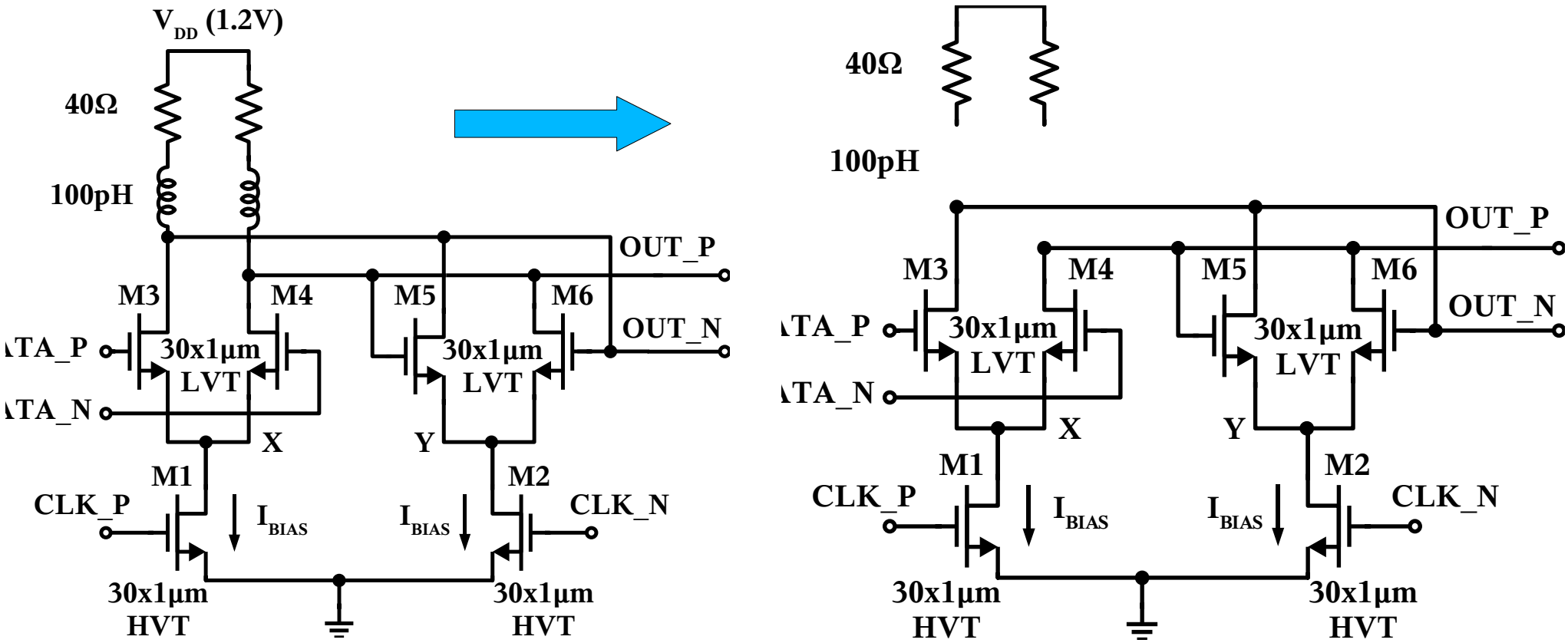
Example: Hierarchical design and breakout of cell for parasitic extraction





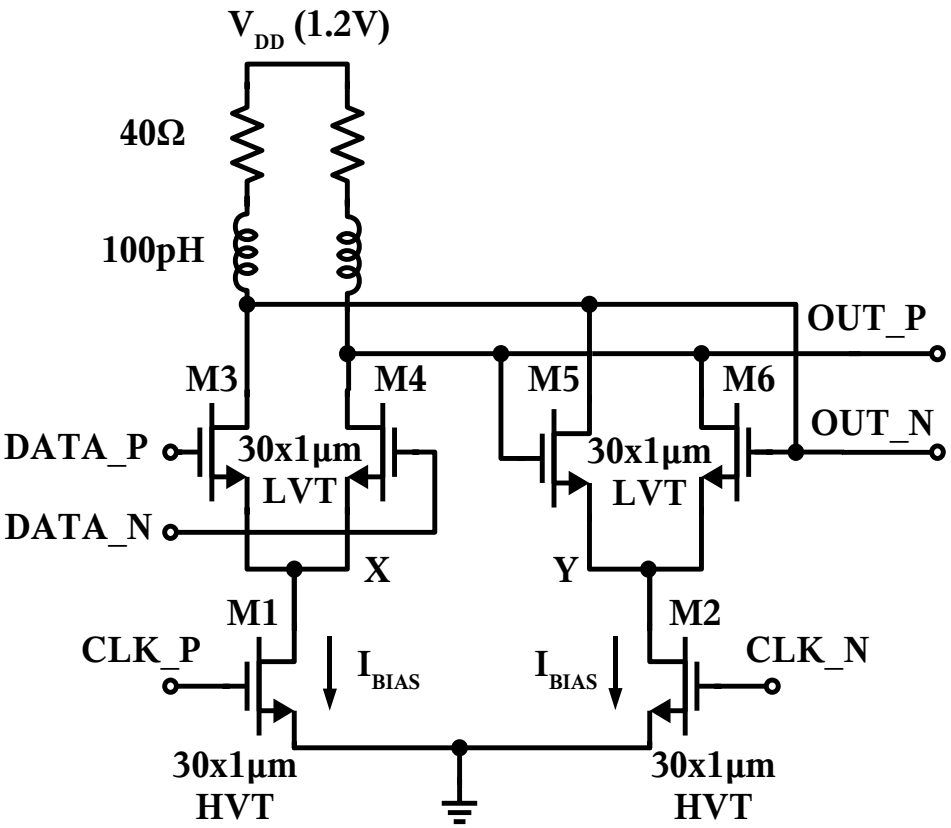
- Minimize footprint by merging transistors in diff. pairs, latching quads

Hierarchical breakout of cell for parasitic extraction (ii)



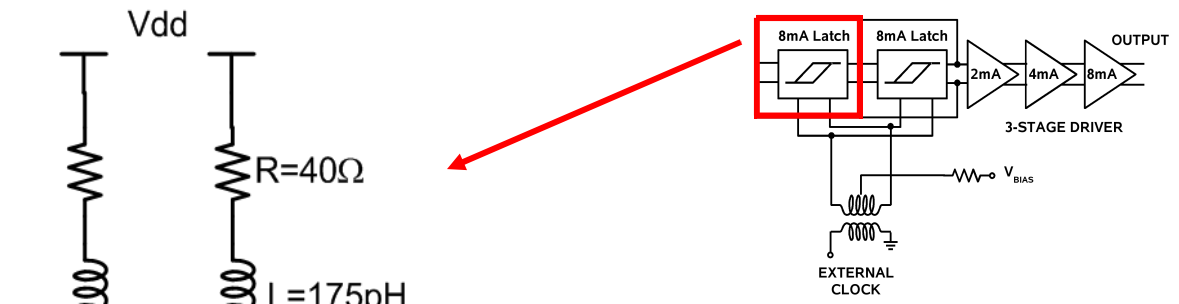
- Extract RC parasitics at cell level without inductors

Hierarchical breakout of cell for parasitic extraction (iii)



- Extract RC parasitics at cell level without inductors
- Model inductors and long interconnect as 2-π circuit with ASITIC

Impact of layout on 65-nm LP CMOS static frequency divider



Version 1 (v1)

$F_{self\text{-}osc}$ = 14.5 GHz

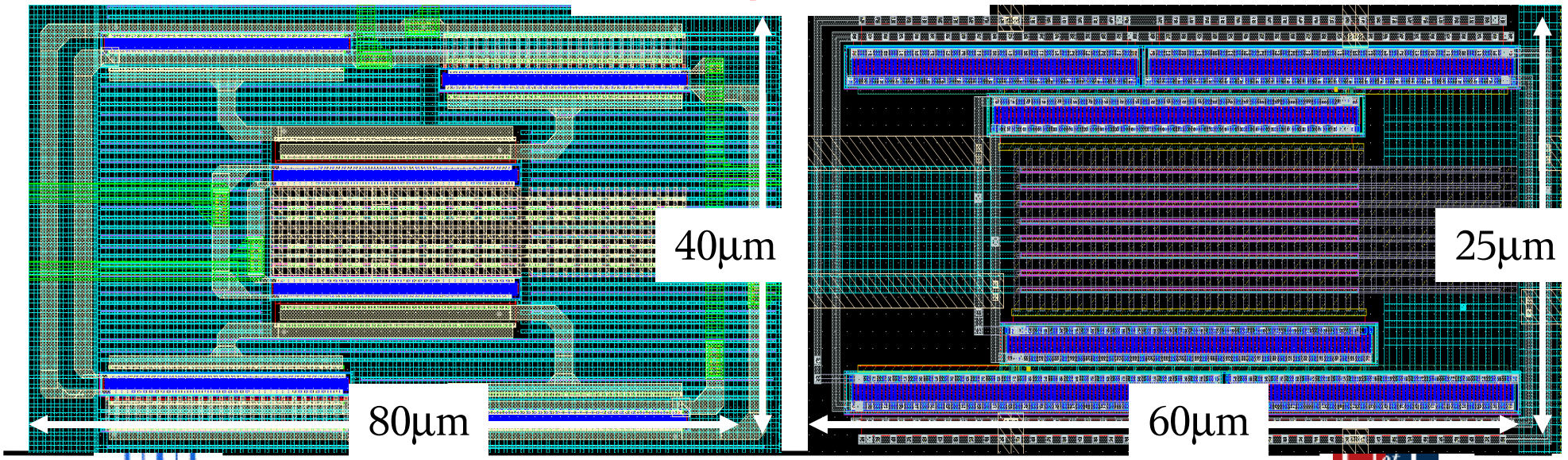
$F_{maximum}$ = 35 GHz

Version 2 (v2)

$F_{self\text{-}osc}$ = 22 GHz

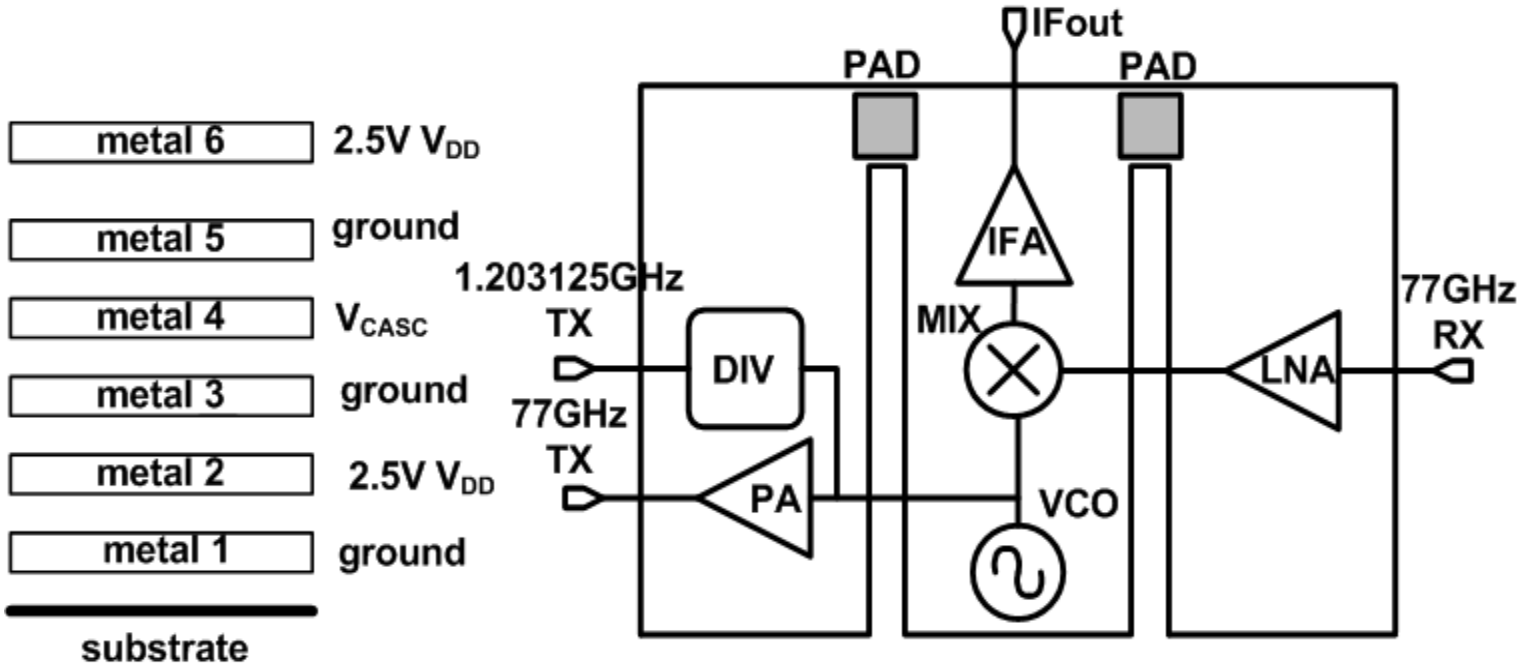
$F_{maximum}$ = 51 GHz

45% improvement



Modeling power/bias/GND distribution
(S. Nicolson et al., IMS-2007)

- Wide lines in metal mesh planes (max C, min. L and R)
- Surround bias/signal lines with GND-ed Faraday cage
- Isolate regions of the chip (grounded p-taps and DNW)
- Provide local de-coupling (< 0.5pF for 80 GHz)



Example: Bias/GND mesh satisfying metal density rules

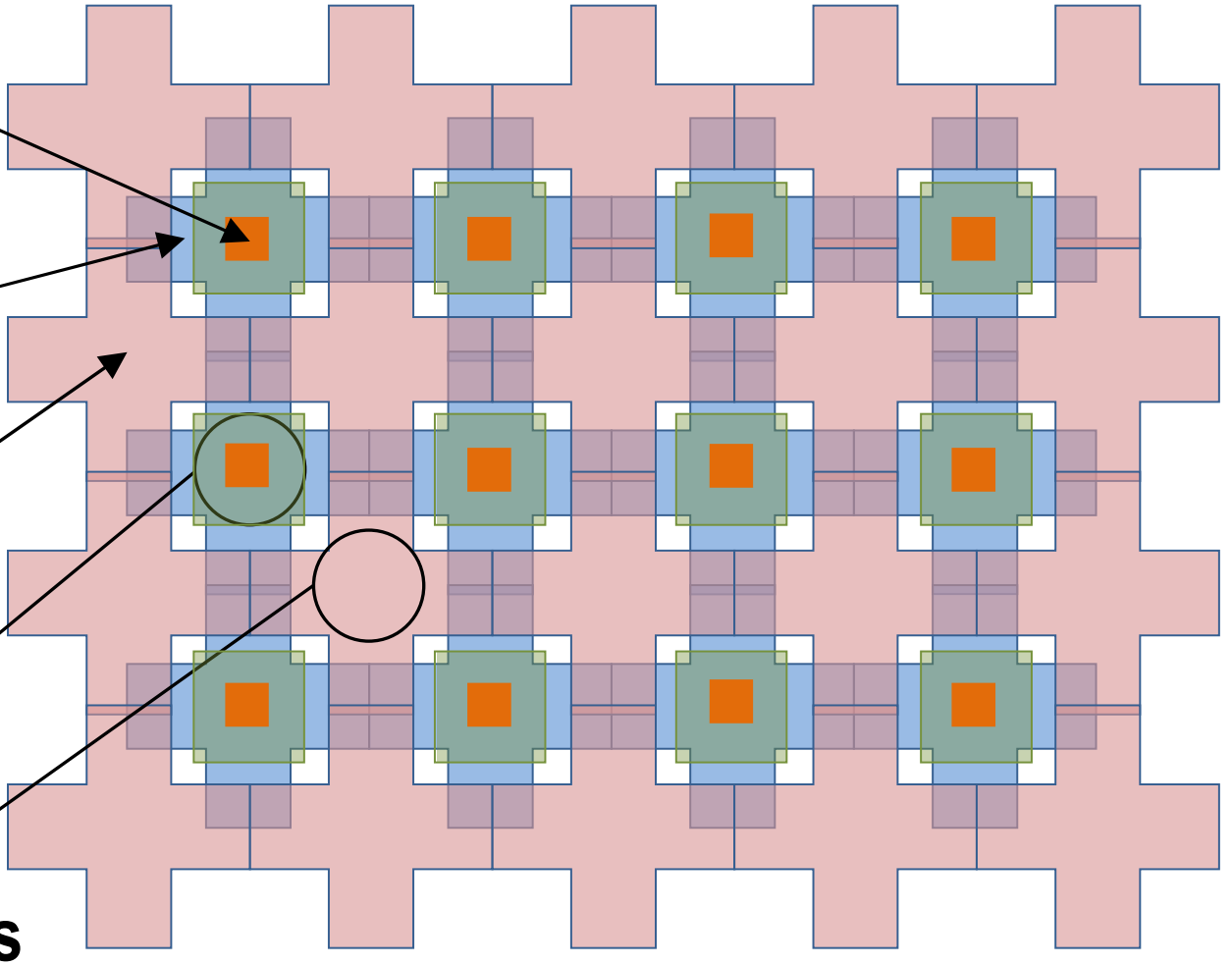
Substrate contact (active + CON)

GND: odd (1,3,5) metals in blue

V_{DD}:even (2,4,6) metals in red

VIAs shunting odd metals and SUB contact

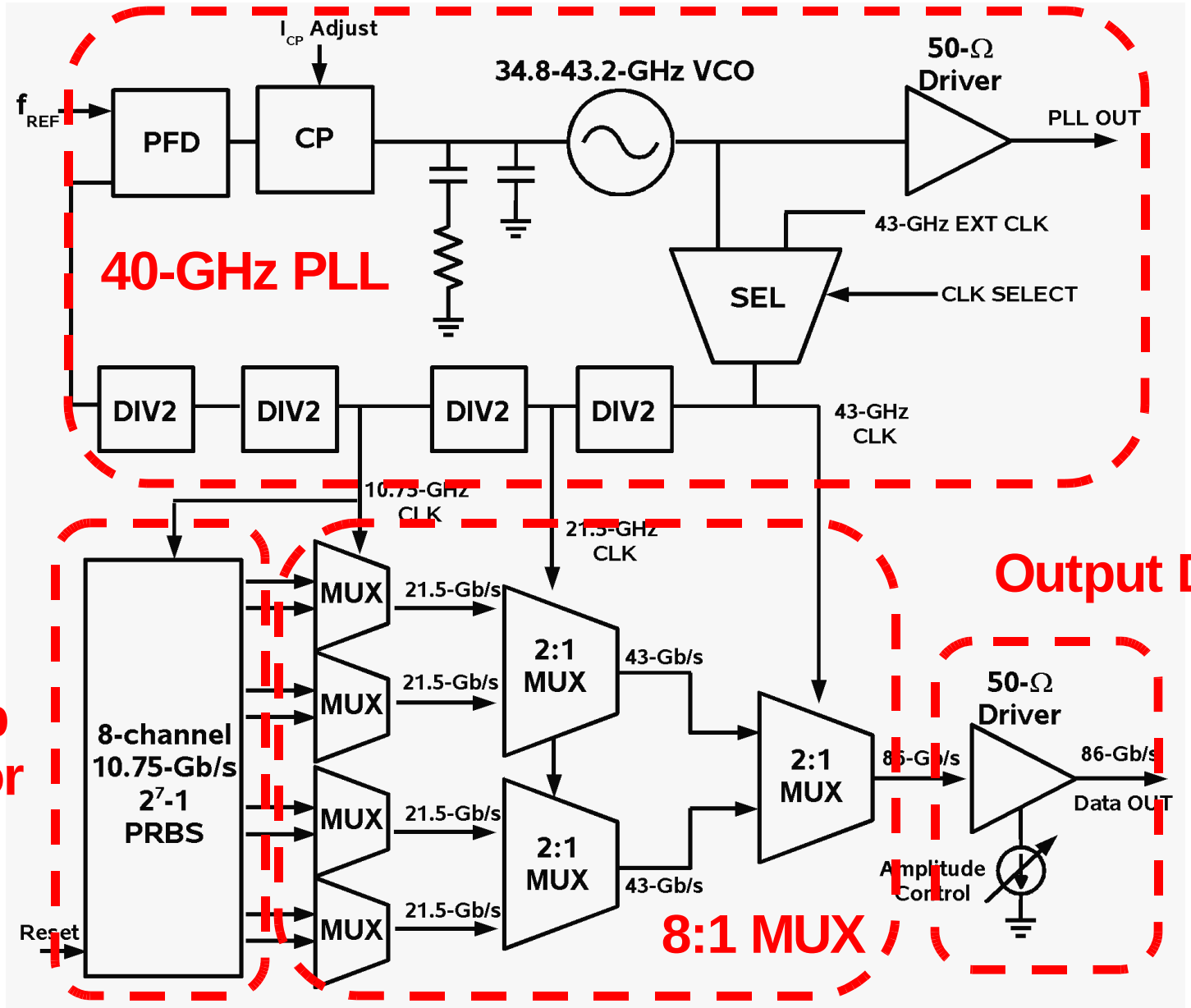
VIAs shunting even metals and DNW isolation



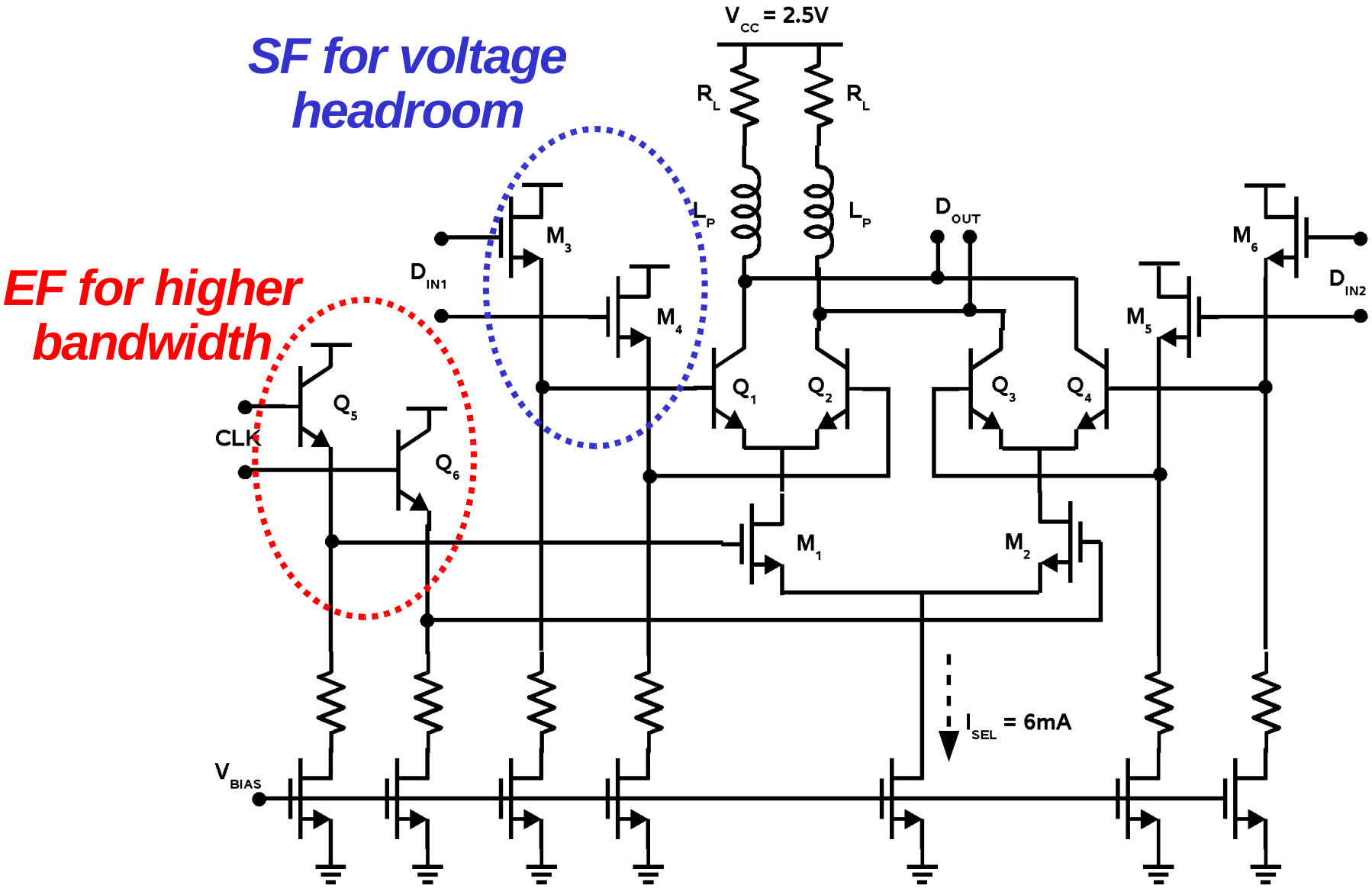
Outline

- 100GE system architectures
- Design methodology
- 90-Gb/s half-rate transceiver
- 100-Gb/s full-rate transceiver blocks
- Round-up

2.5-V, 1.4-W, 90-Gb/sTransmitter (T.Dickson et al. CSICS-06)

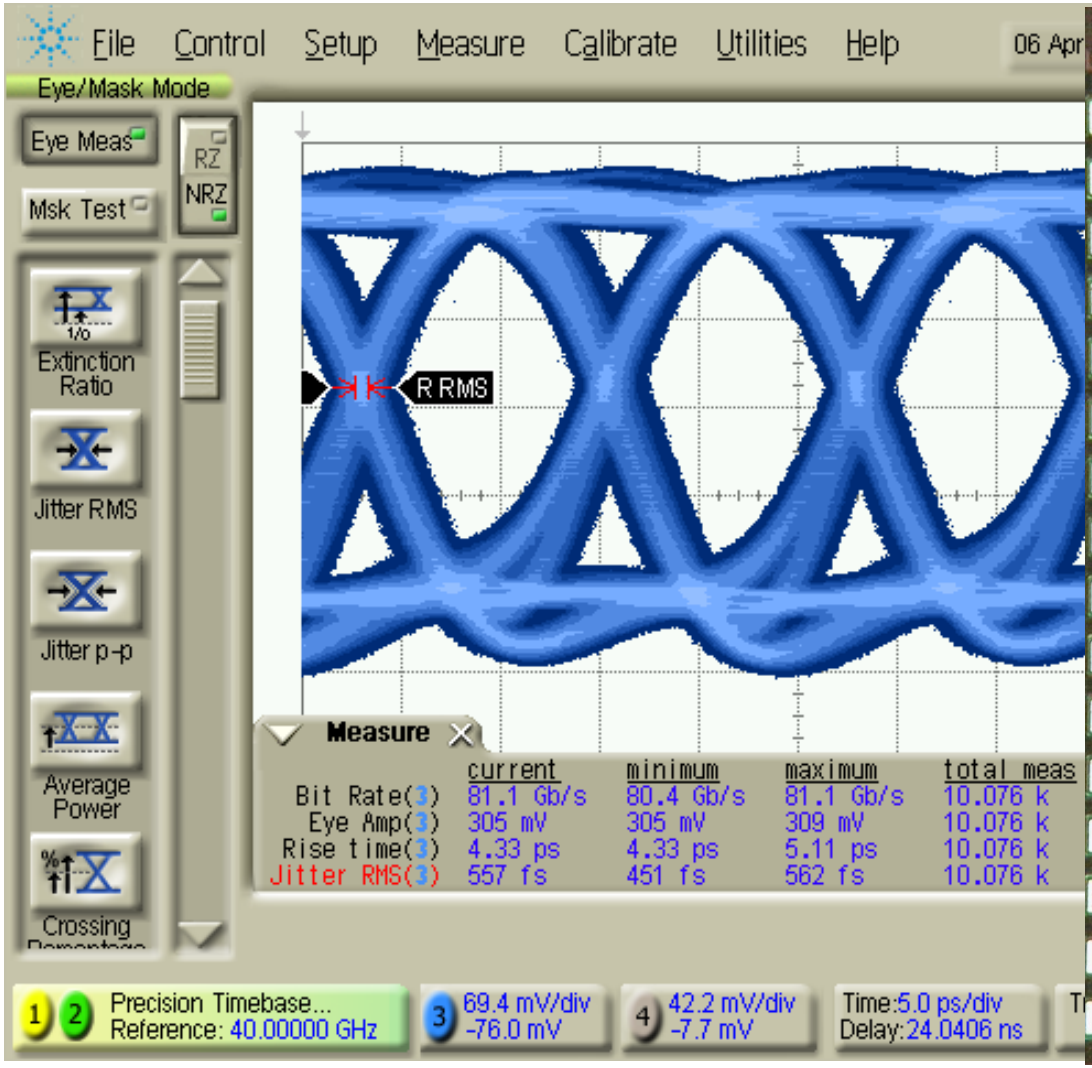


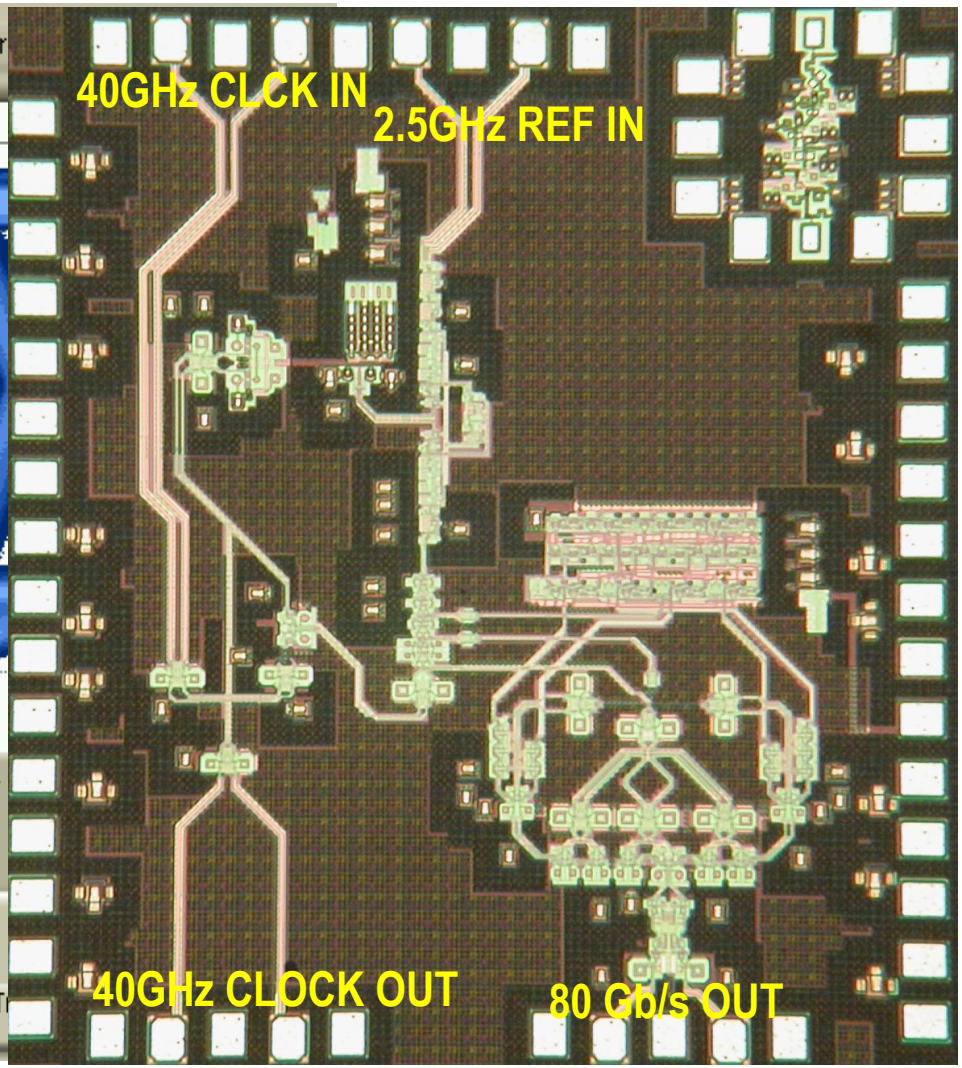
2.5-V, 90-Gb/s BiCMOS Selector



90-Gb/s selector consumes 60mW

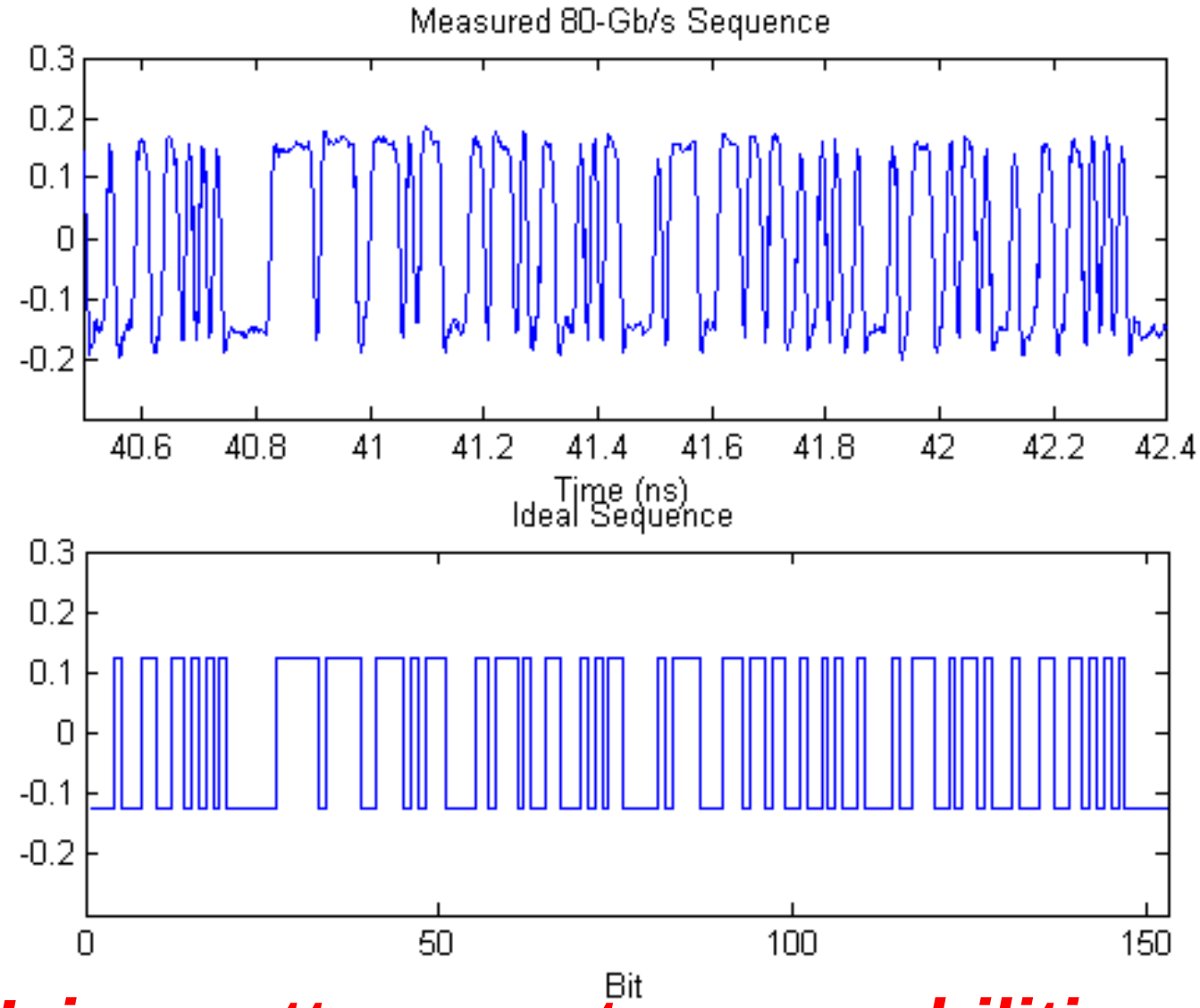
Measured results with external clock: 80 Gb/s





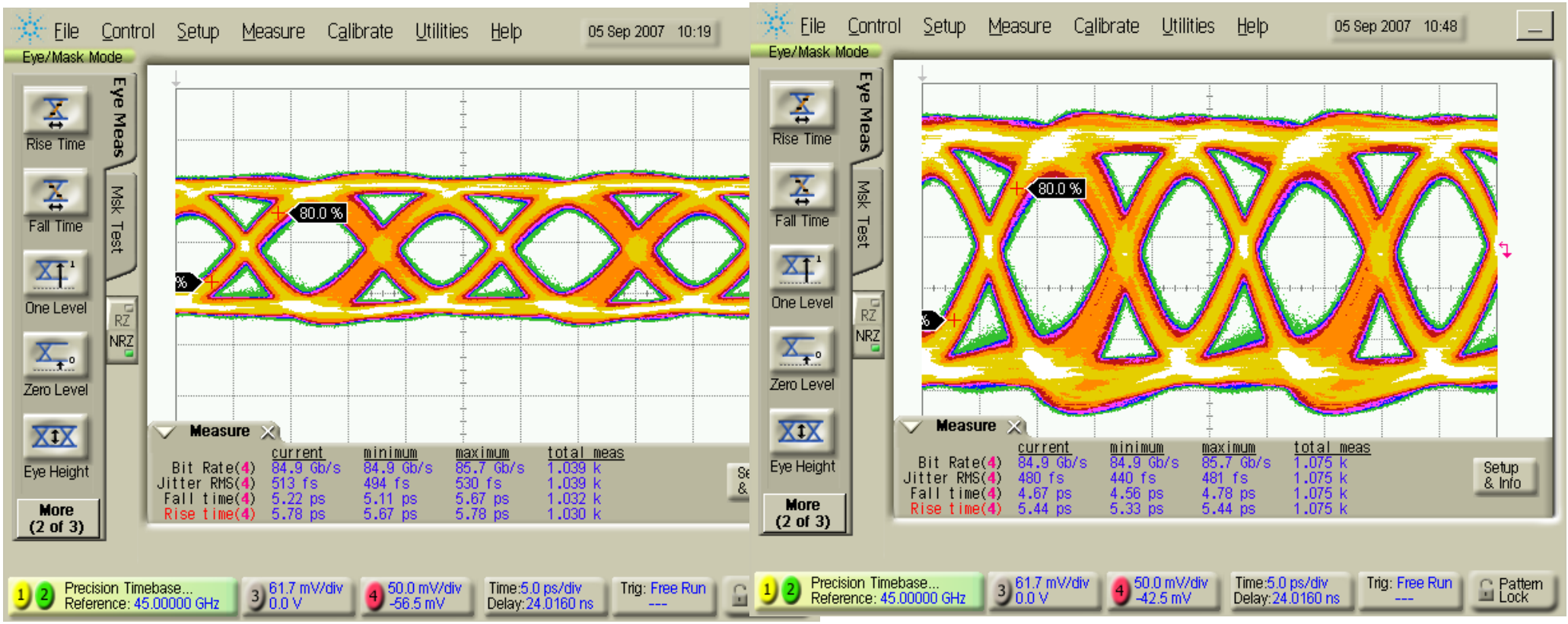
- Running for more than 1 hour continuously in the lab.
- Jitter: 560 fs (rms) , Rise/fall time: 4-5 ps, Amplitude: 300 mV_{pp} per side

Verification of correct multiplexing



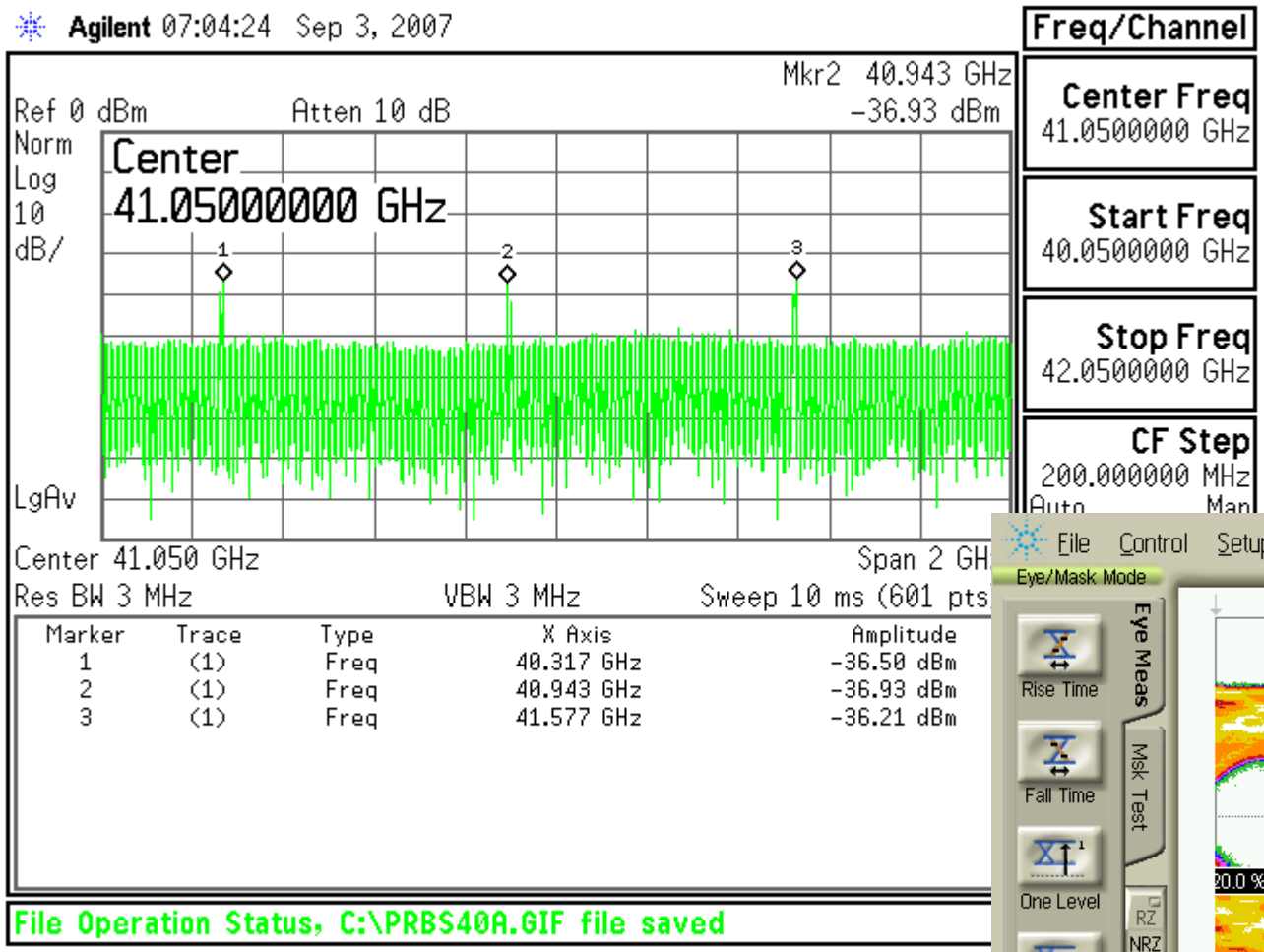
Using pattern capture capabilities of the Agilent 86100C DCA

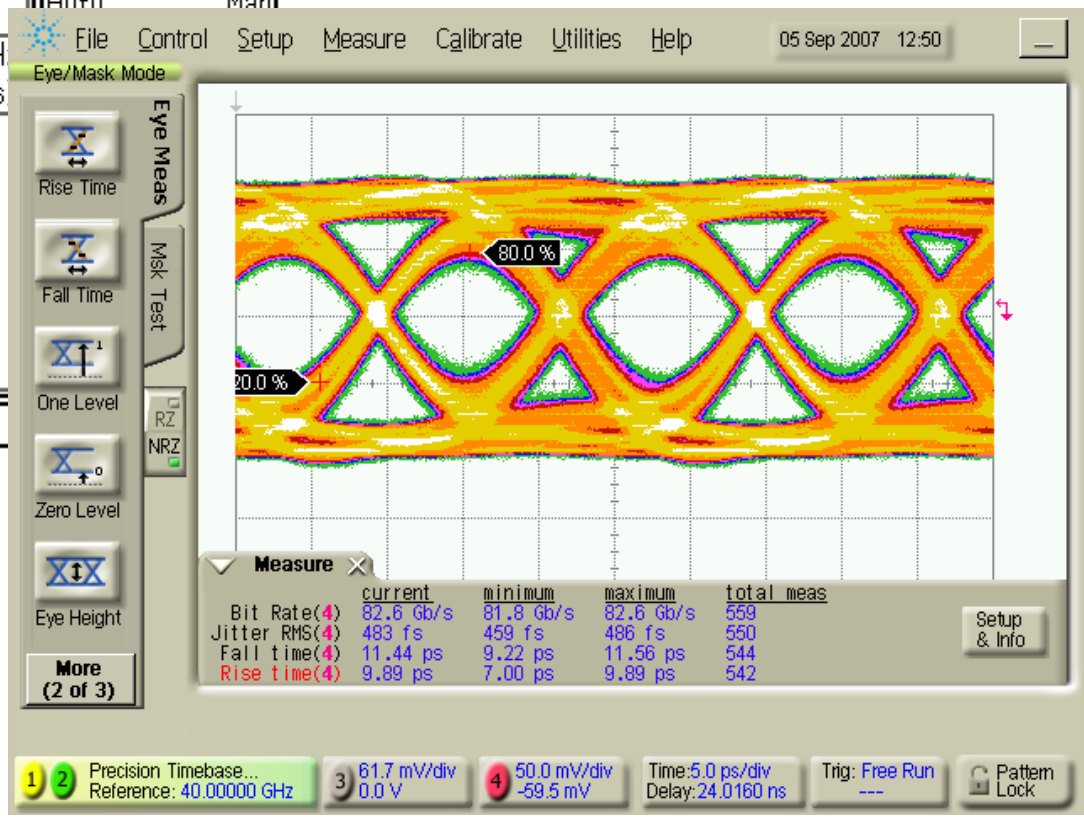
90 Gb/s: amplitude control (new spin)



Little degradation in eye quality as amplitude varies from 150 mV to 300 mV per side

80 Gb/s at 100 °C





Comparison

130-nm CMOS+170-GHz SiGe HBT = 2×speed + ½ power of 130-nm CMOS

Technology	f_T/f_{MAX}	Data Rate	Supply Voltage	Power
130-nm CMOS	85/90 GHz	40 Gb/s (half-rate)	1.5 V	2.7 W
InP HBT	150/150 GHz	43 Gb/s (full-rate)	-3.6/ -5.2 V	3.6 W
180-nm SiGe BiCMOS	HBT: 120/100 GHz	43 Gb/s (half-rate)	-3.6 V	1.6 W
180-nm SiGe BiCMOS	HBT: 120/100 GHz	43 Gb/s (full-rate)	-3.6 V	2.3 W
130-nm SiGe BiCMOS	MOS: 85/90 GHz HBT: 170/200 GHz	90 Gb/s (half-rate)	2.5 V	1.36 W

Outline

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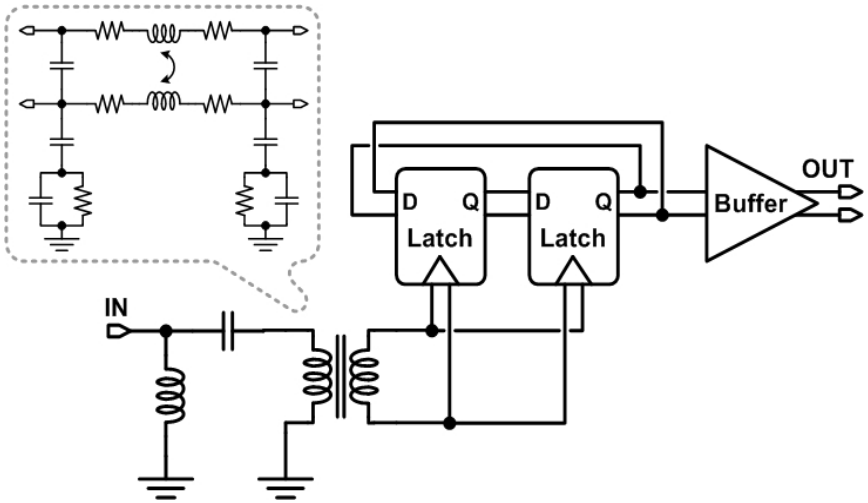
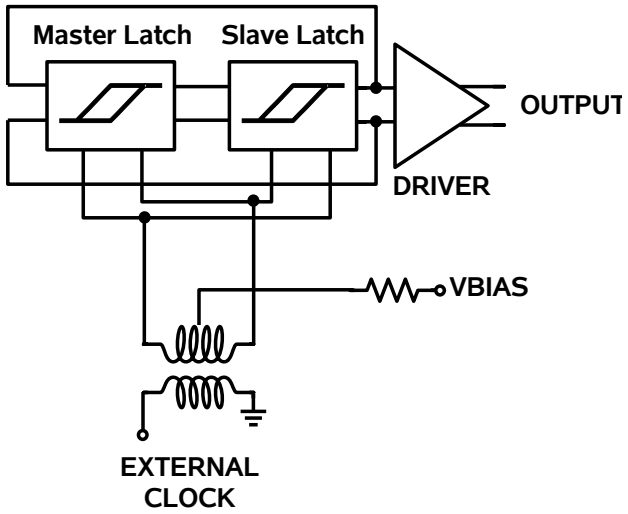
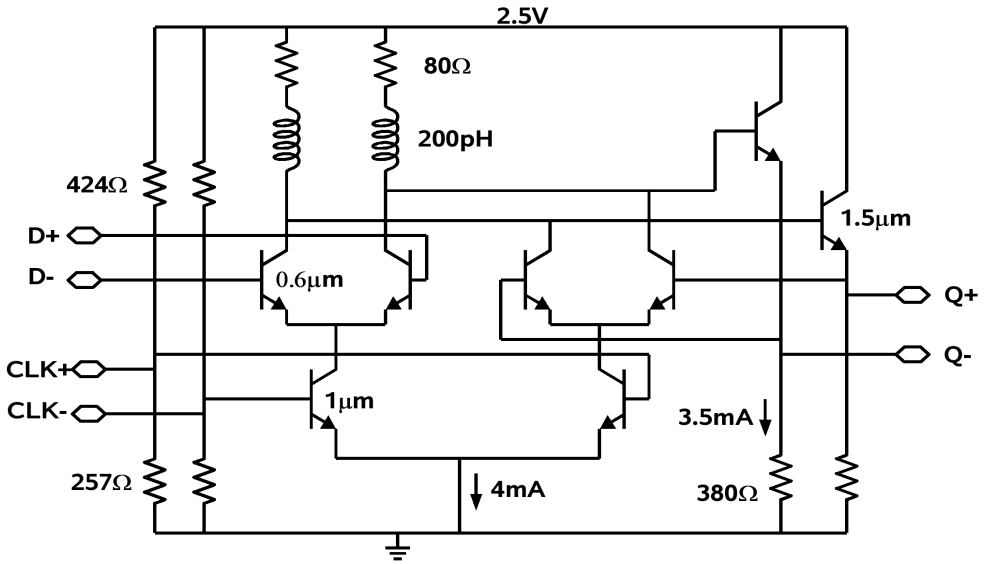
Critical 100-Gb/s full-rate circuit blocks

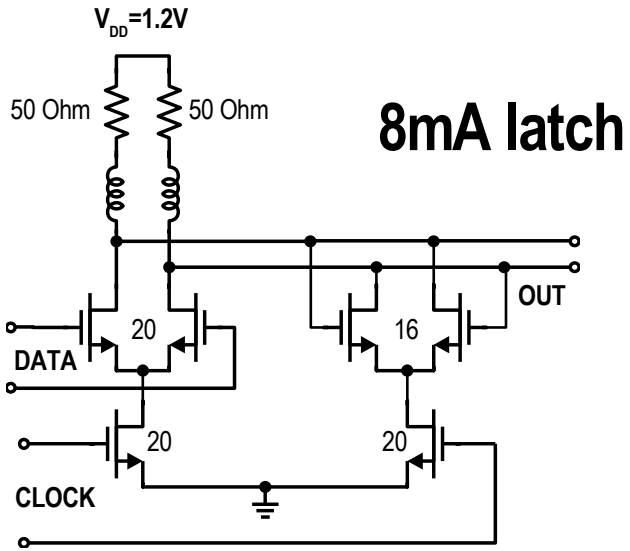
- 100-GHz flip-flop
- 100-GHz static frequency divider
- 100-GHz clock distribution network
- 100-GHz low-phase noise VCO

Divide-by-2 block diagram and latch schematics

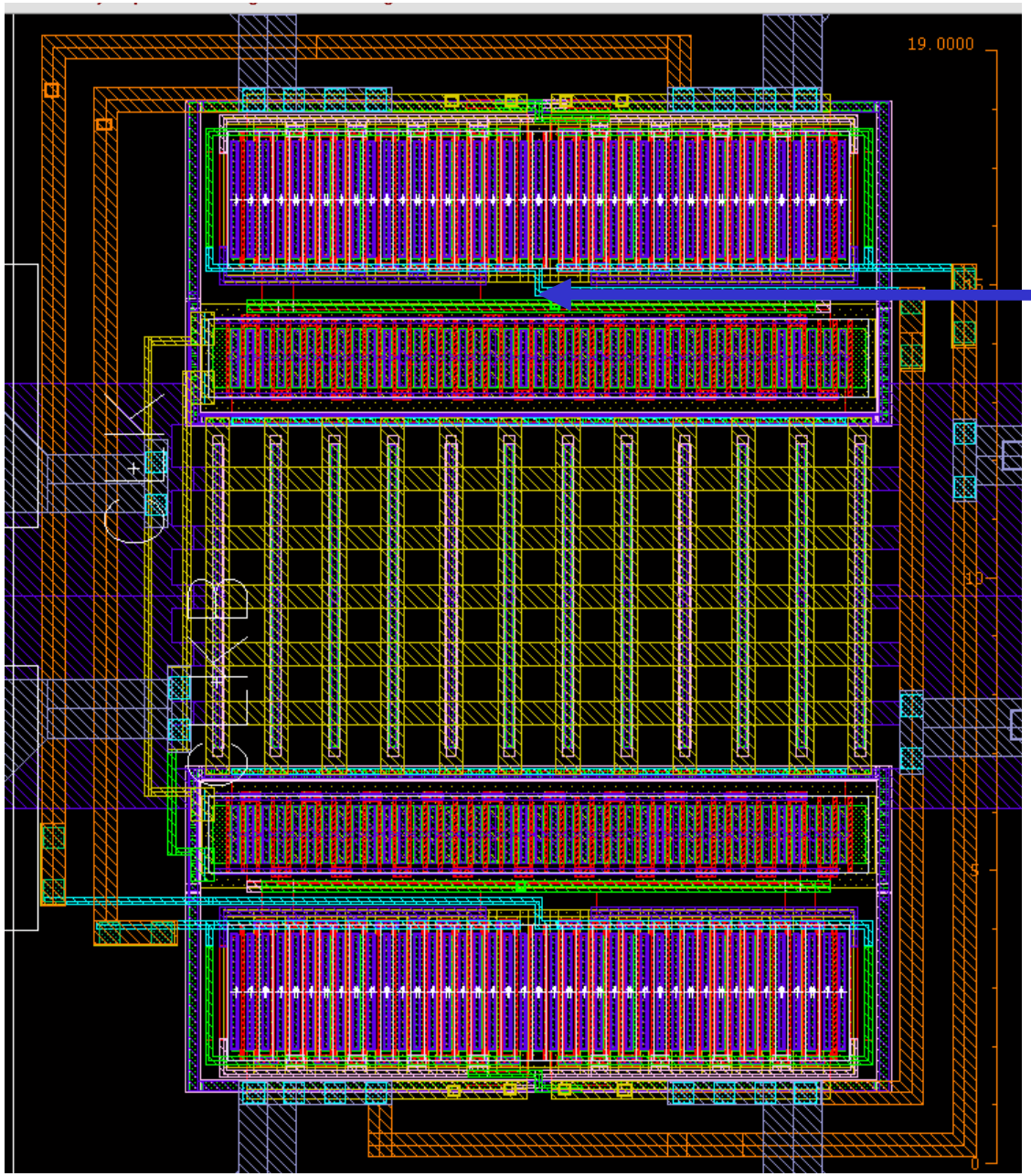




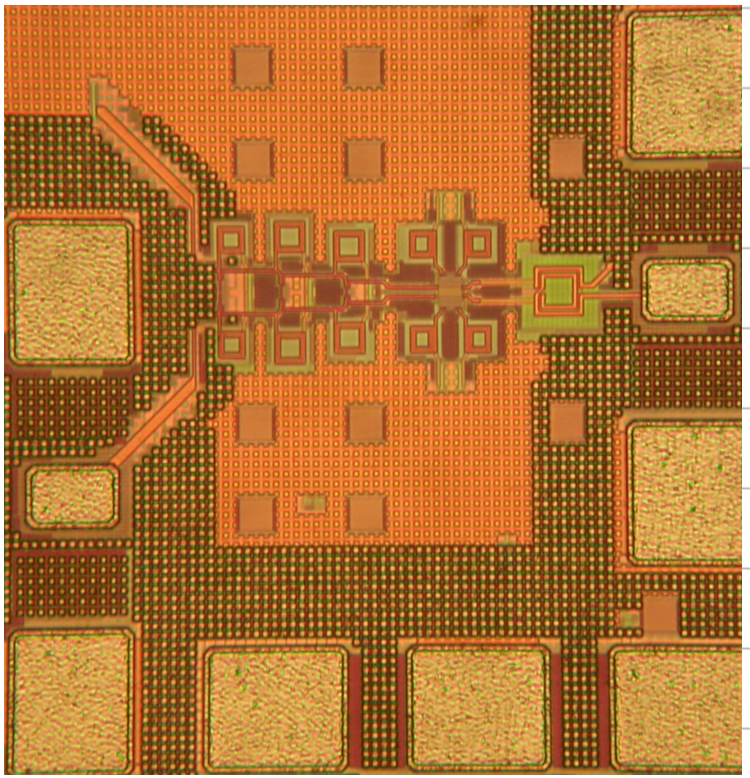




Divider layout (20 x 16 µm²)



90-GHz, 65-nm GP CMOS static divider: 2% variation



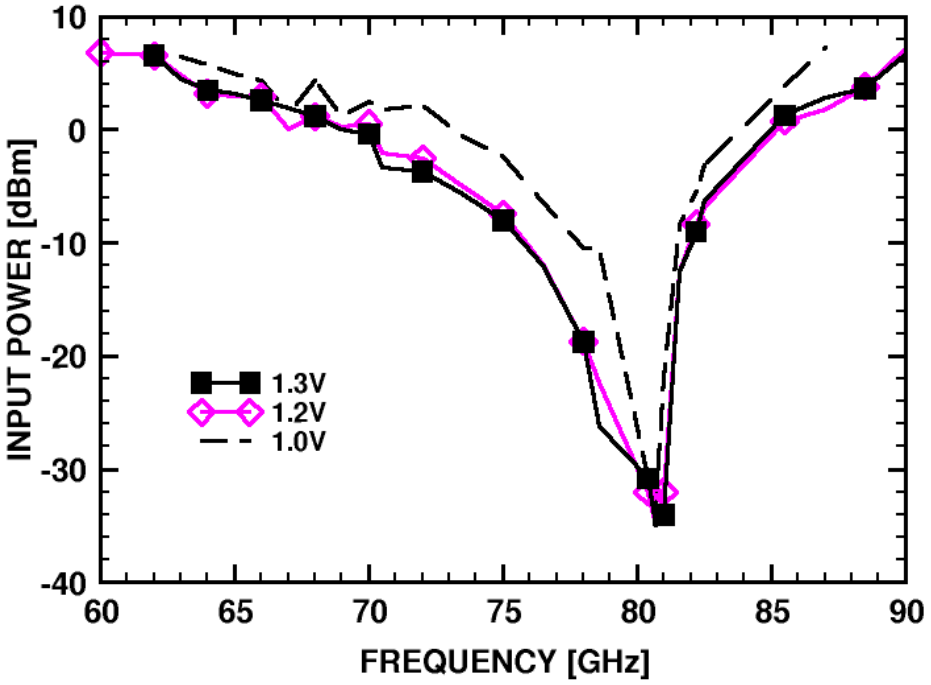
Power = 19.6mW per divider + 22.4mW for output buffer

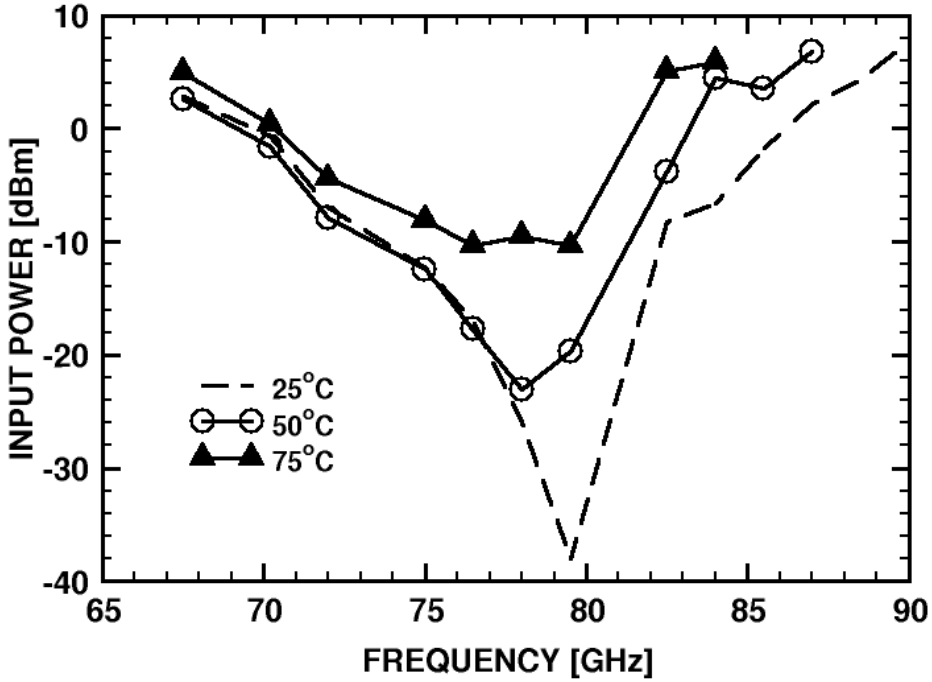
Average Self-Oscillation Frequency (SOF) =39.5GHz (@ the output)

WAFER 17 - SOF MAPPING (GHz)

	1	2	3	4	5	6	7	8	9	10
A										
B					39.25	39.14	39.26	39.3		
C					39.3	39.12	39.325	39.365		
D				39.38	39.4	39.593	39.78	39.173		
E				39.2	39.5	39.5	39.67	39.34	39.14	39.06
F				39.107	39.473	39.473	39.353	39.34	39.16	38.95
G				39.08	39.207	39.333	39.587	39.34	39.36	39.08
H				38.94	39.34	39.536	39.413	39.305	39.22	39.12
I				39.23	39.273	39.5	39.513	39.43	39.307	39.51
J				39.31	39.465	39.67	39.72	39.567	39.107	
K				39.42	39.395	39.455	39.44			
L					40.02	39.895	40.02			

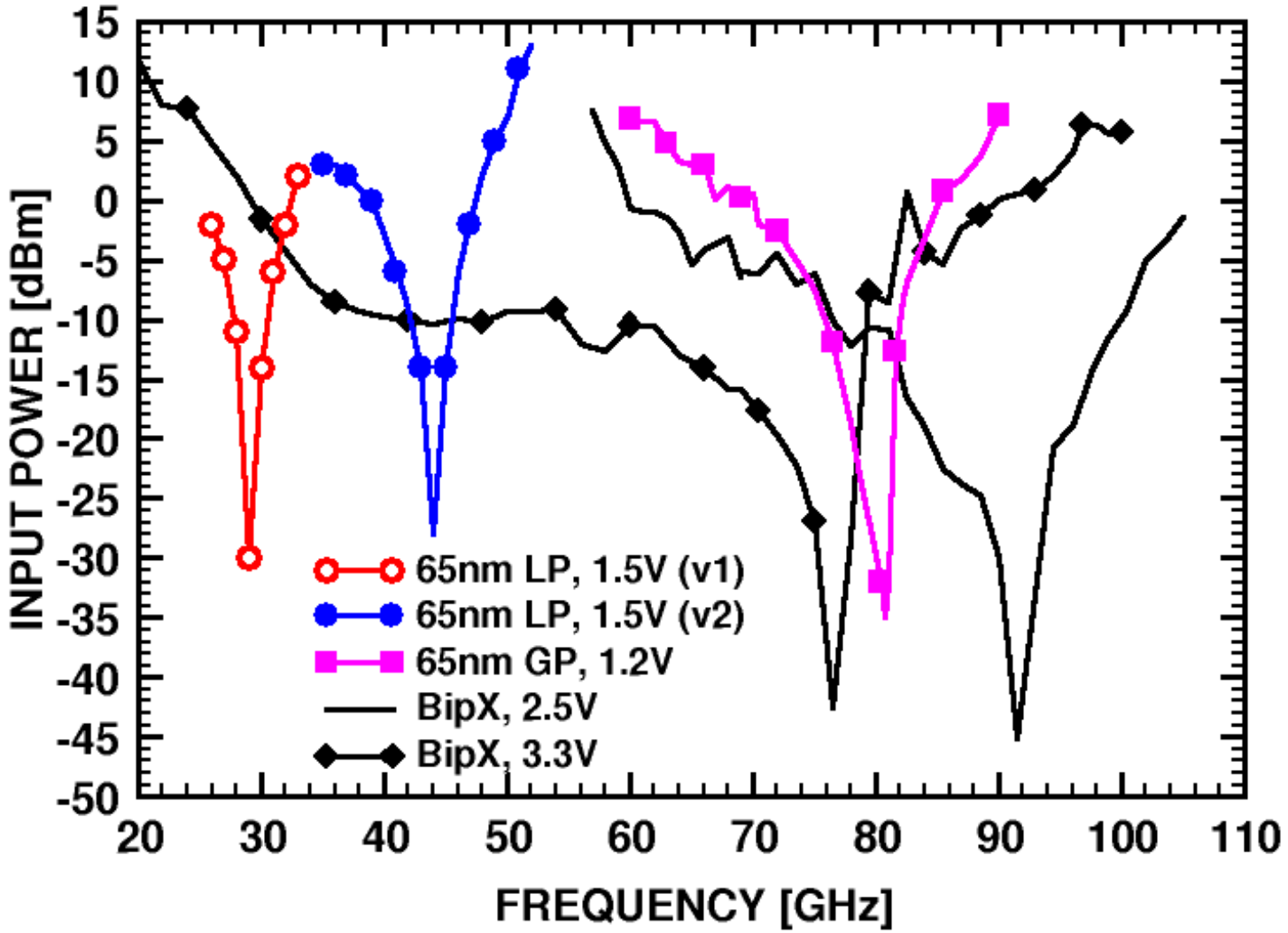
PVT performance of 65-nm GP CMOS divider





- Operates up to 78.5 GHz at 100 ^{0}C from 1.1V supply and at 80 GHz at 125 ^{0}C from 1.4 V
- Does not divide below 57GHz

65-nm GP/LP CMOS vs. SiGe HBT and BiCMOS dividers



Comparison with published 80+GHz static dividers

Reference	Self-Oscillation Freq.	Max. Divider Freq.	Power Consumption	Technology
This work	45 GHz	51 GHz	42mW(1.5V)	65nm LP-CMOS
This work	80 GHz	91 GHz	20 mW (1.2V)	65nm GP-CMOS
Plouchart ISCC-07	92 GHz	102 GHz	52.4mW(2.2V)	65nm HP SOI CMOS
Trotta CSICS-05	65 GHz	110 GHz	1.35 W (-5.2V)	225-GHz f_T SiGe HBT
Hitko CSICS-04	95 GHz	143.6 GHz	90 mW	400-GHz f_T InP
Rylyakov CSICS-04	71 GHz	96 GHz	770 mW (-5.0V)	210-GHz f_T SiGe HBT
Laskin BCTM-07	77 GHz	>100 GHz	122 mW (3.3-3.6V)	230-GHz f_T SiGe HBT
Nicolson IMS-07	81 GHz	>105 GHz	75 mW (2.5V)	230-GHz f_T SiGe HBT

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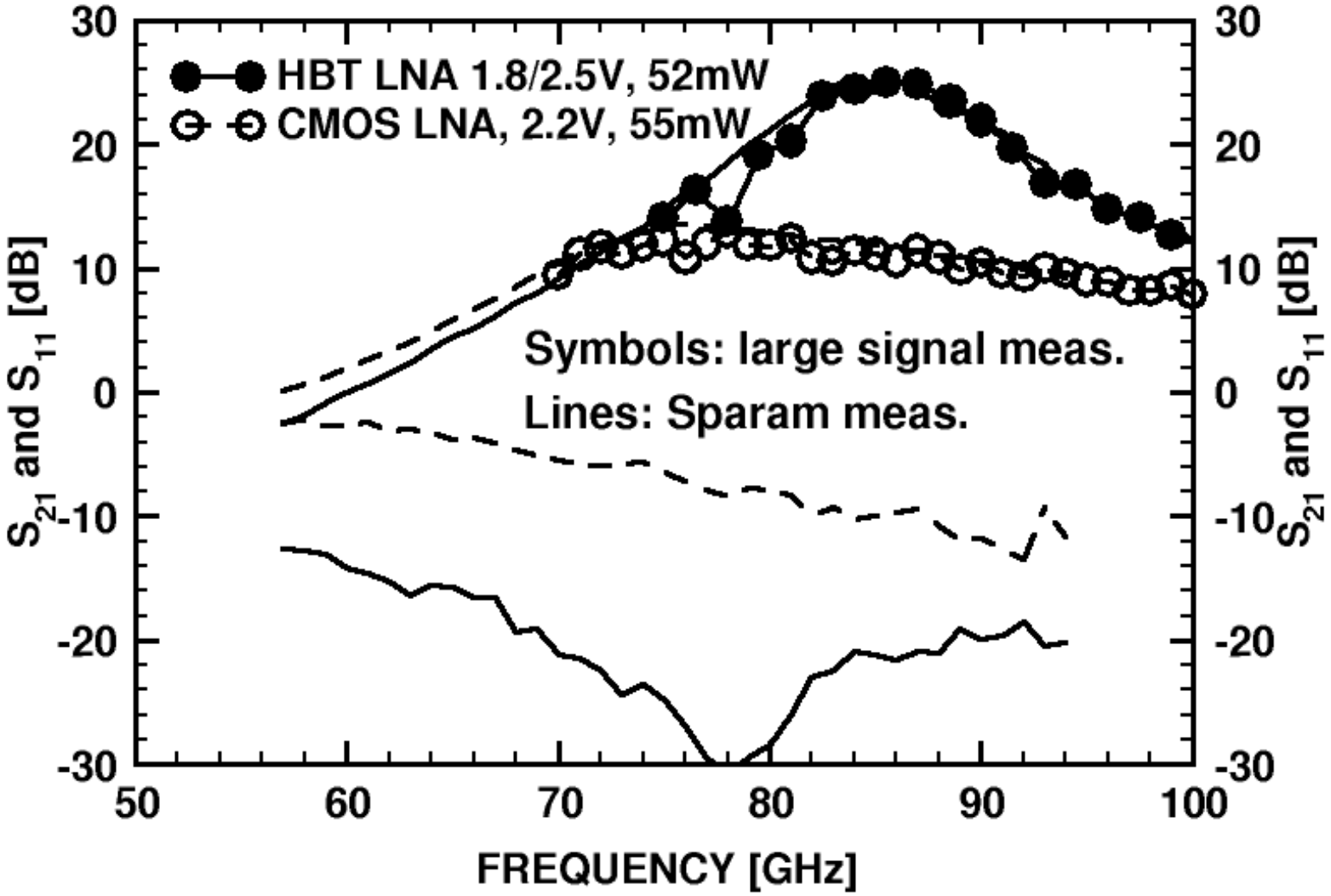
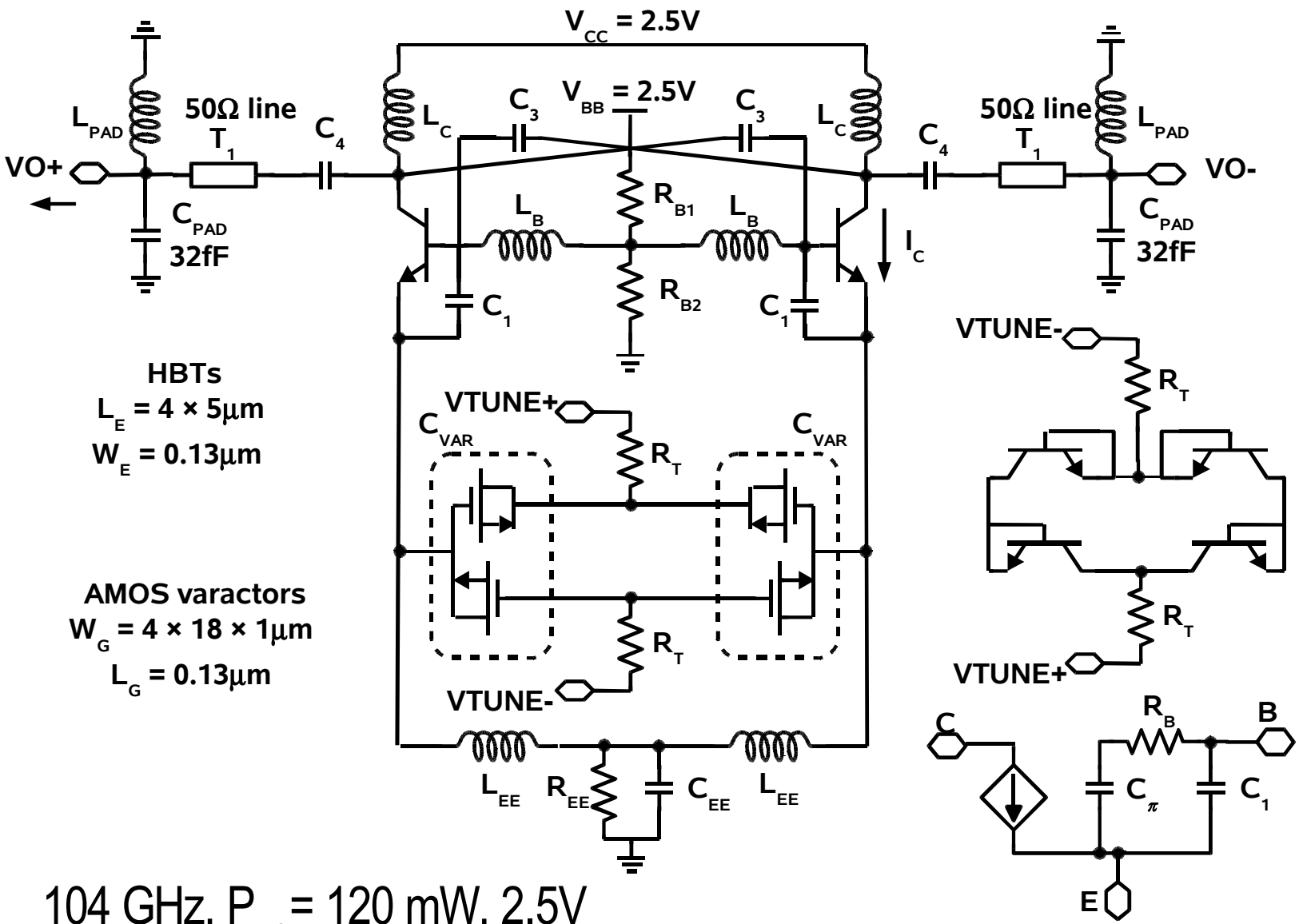
70-100 GHz 65-nm LP CMOS vs. SiGe HBT LNAs as clock buffers (S. Nicolson et al. IMS-07)



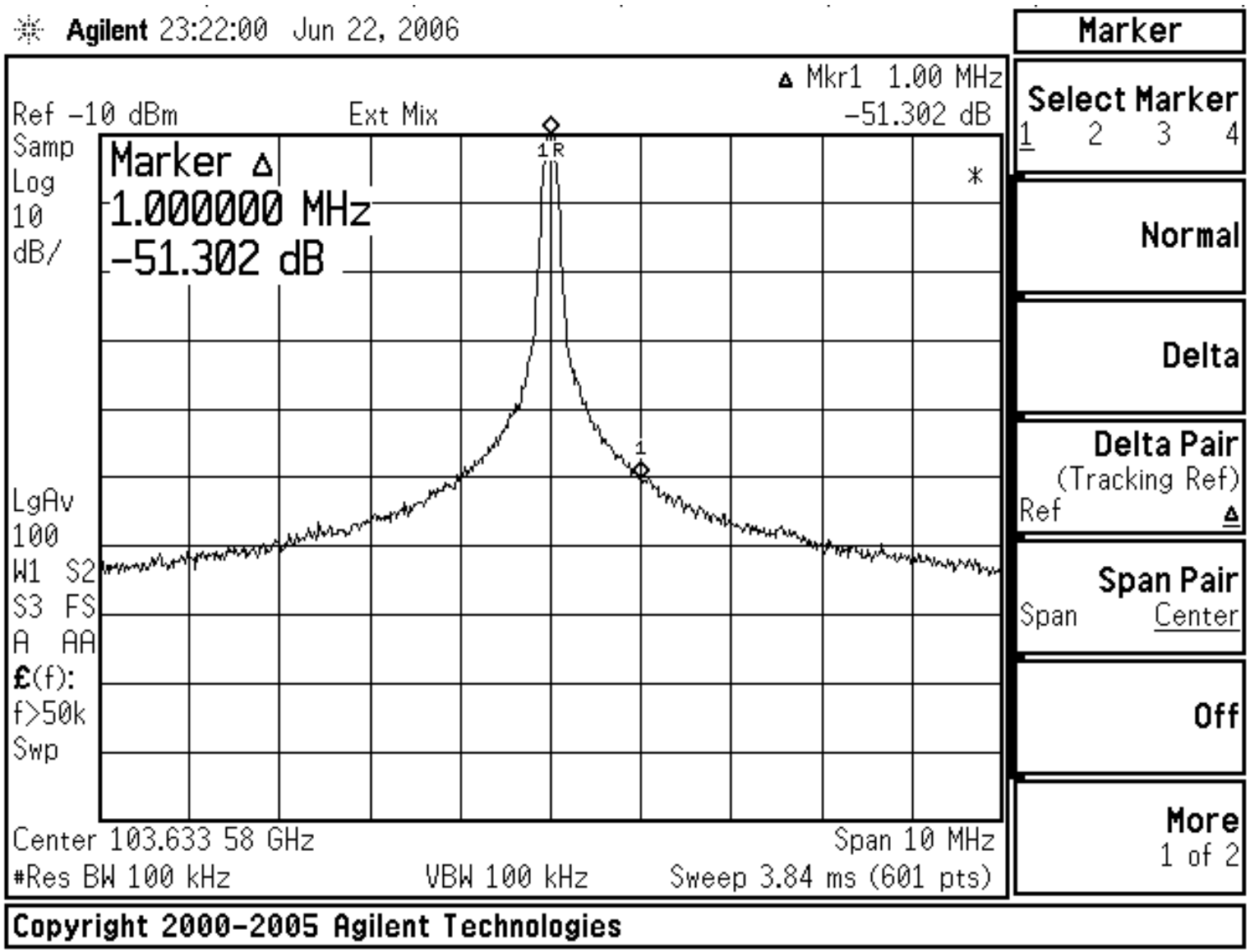
105-GHz SiGe HBT Colpitts VCO Schematics



104 GHz, P_{DC} = 120 mW, 2.5V

Die size: 0.4mmx0.5mm

104-GHz VCO phase noise: -101 dBc/Hz @ 1MHz



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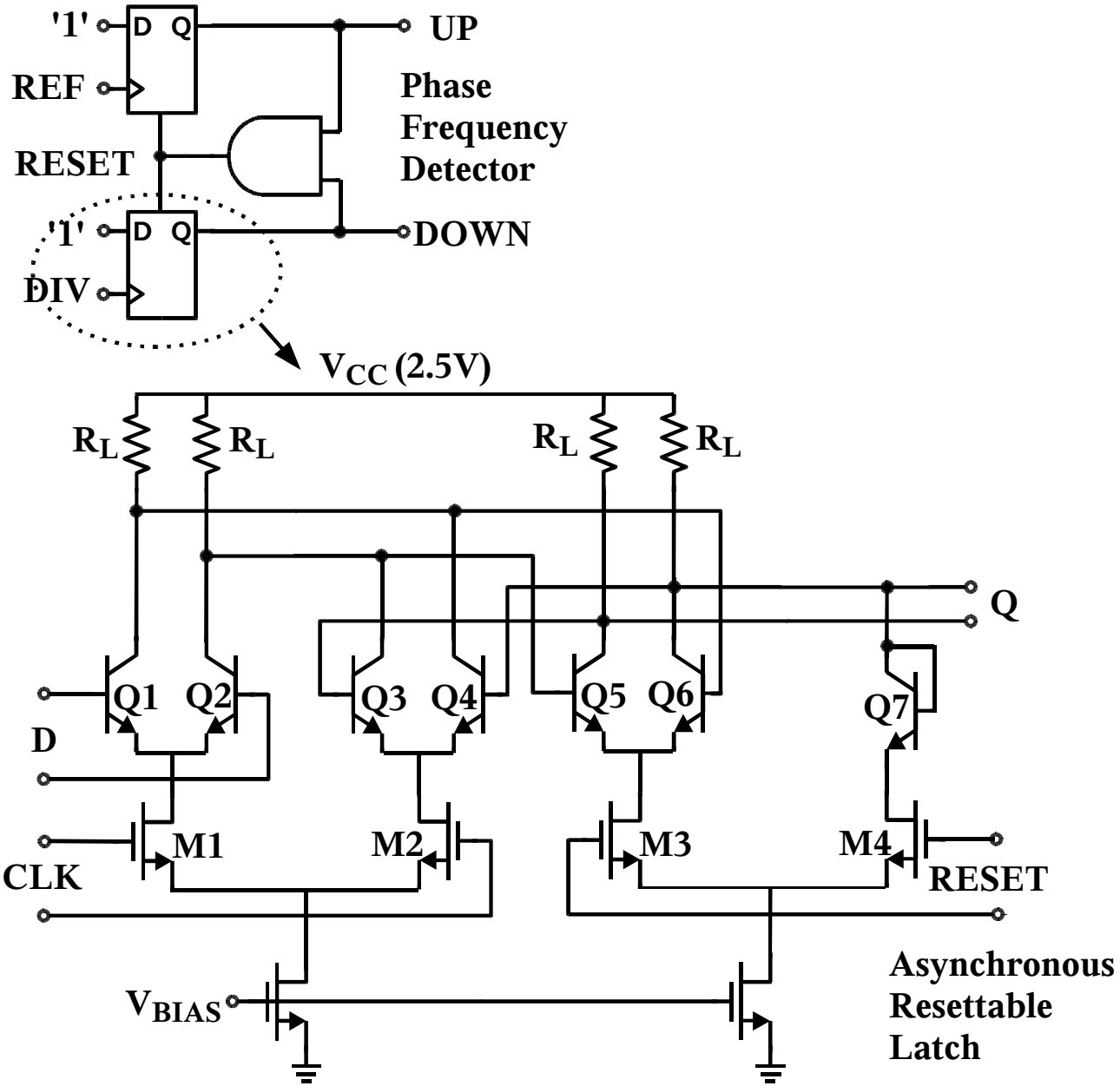
- A 3W, 100-Gb/s half-rate serial transceiver is feasible in 300-GHz SiGe BiCMOS technology now
- At least 45-nm GP CMOS is needed for half-rate 100-Gb/s transceiver

Acknowledgments

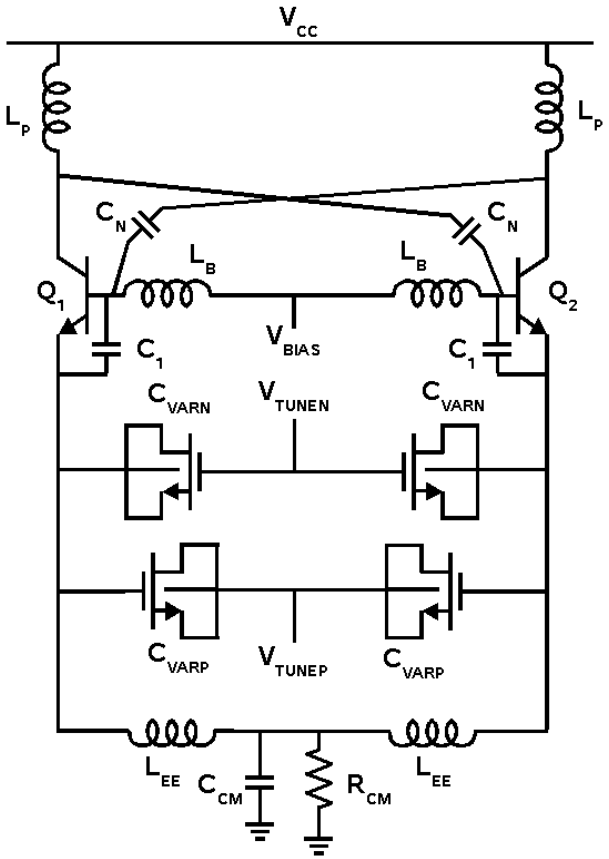
- Jaro Pristupa and CMC for CAD support
- OIT, CFI, ECTI for equipment

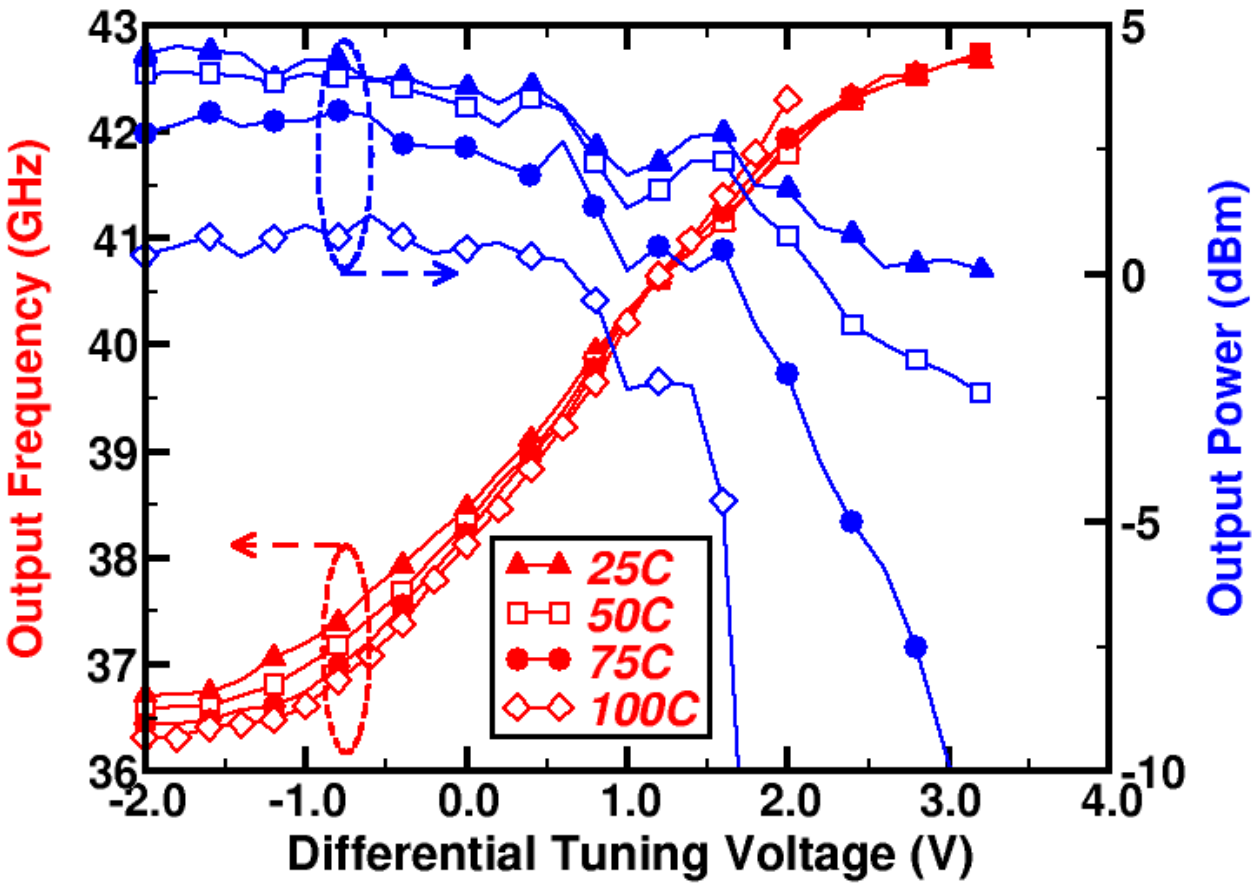
Back up

Phase frequency detector



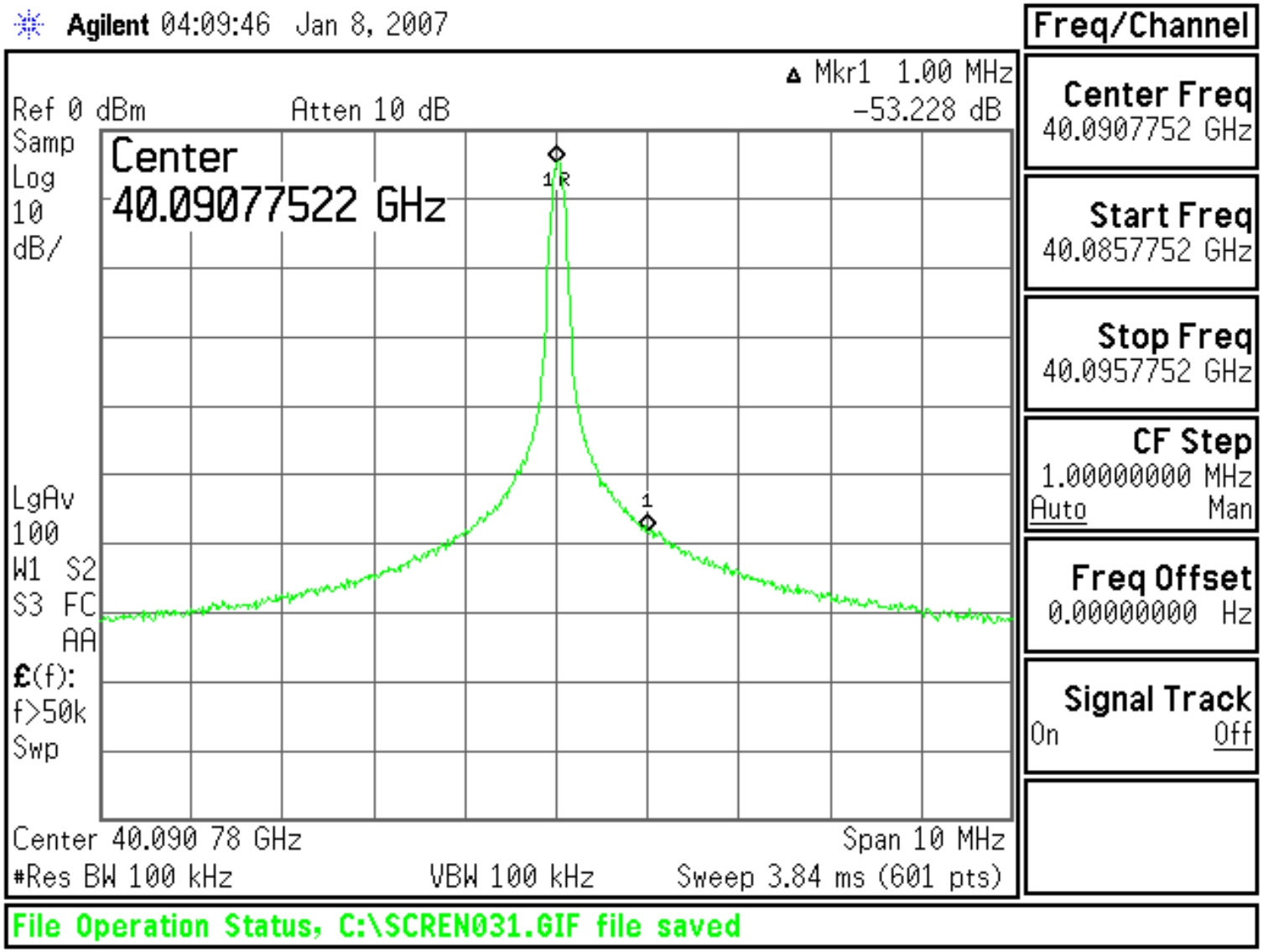
36-43 GHz Colpitts VCO





- SiGe HBTs used as negative resistance generators.
- Differential tuning to reject common-mode noise.
- Maximize tank swing, bias HBTs at NF_{MIN} for low phase noise

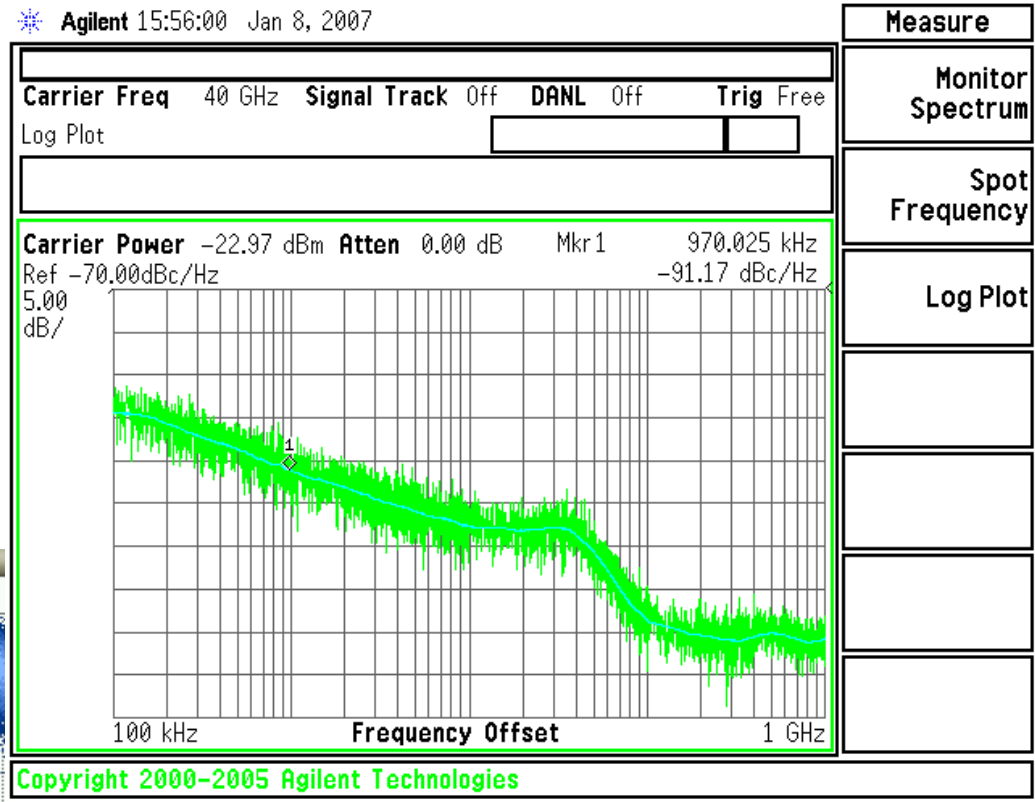
VCO Phase Noise

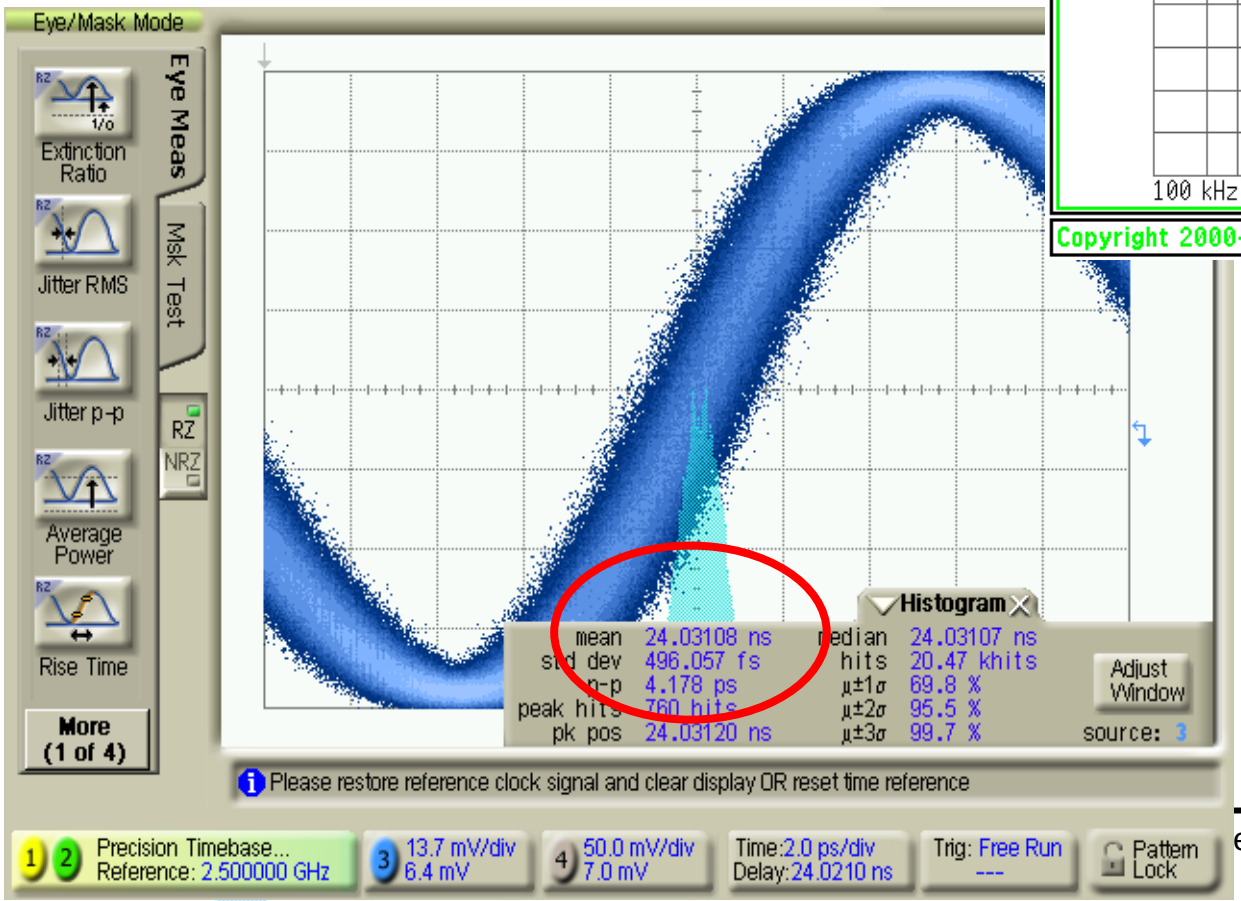


-103 dBc/Hz @ 1-MHz offset

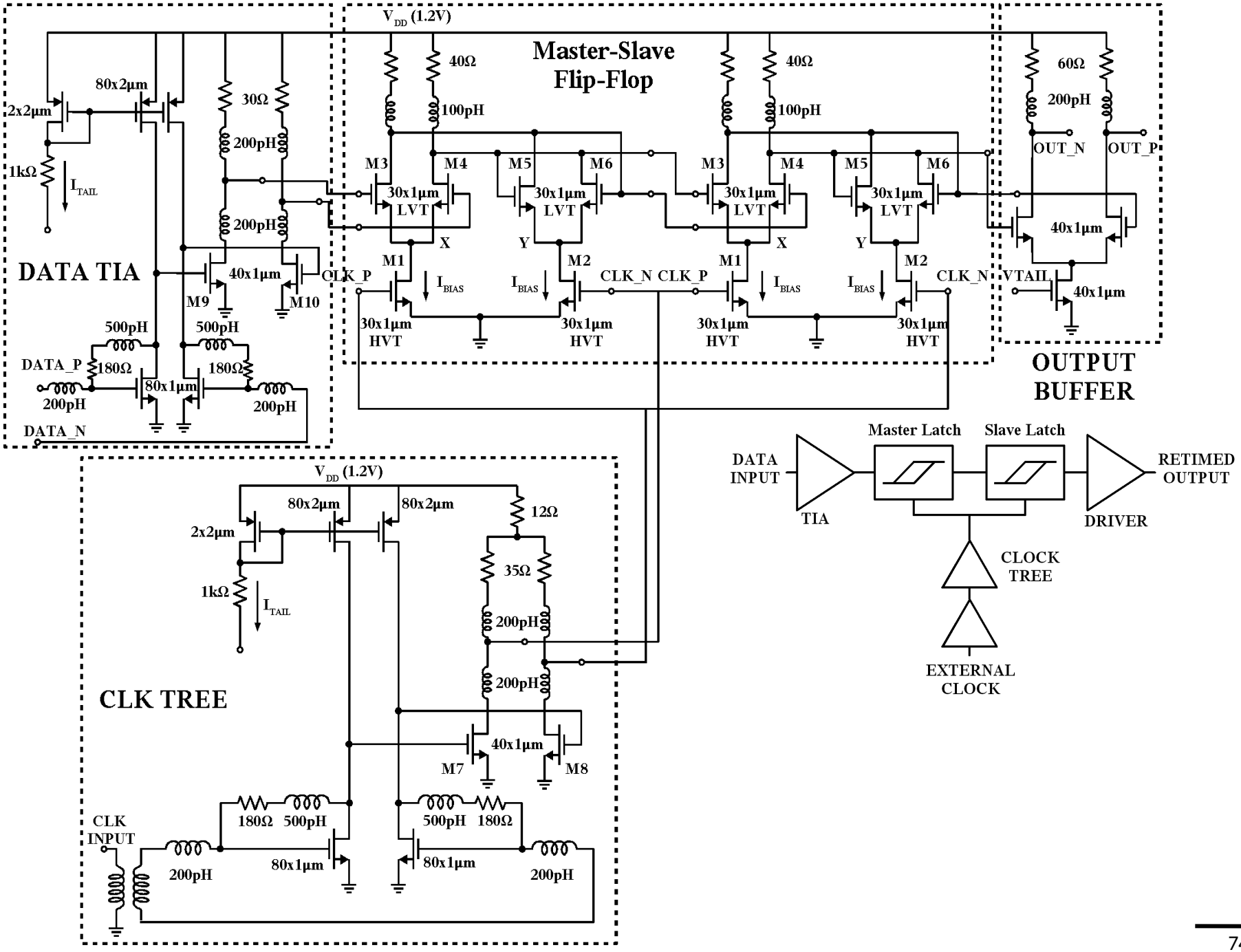
PLL measurements (T. Chalvatzis et al., VLSI-07)

- Locking range: 38-42 GHz
- RMS jitter: σ_t = 496 fs

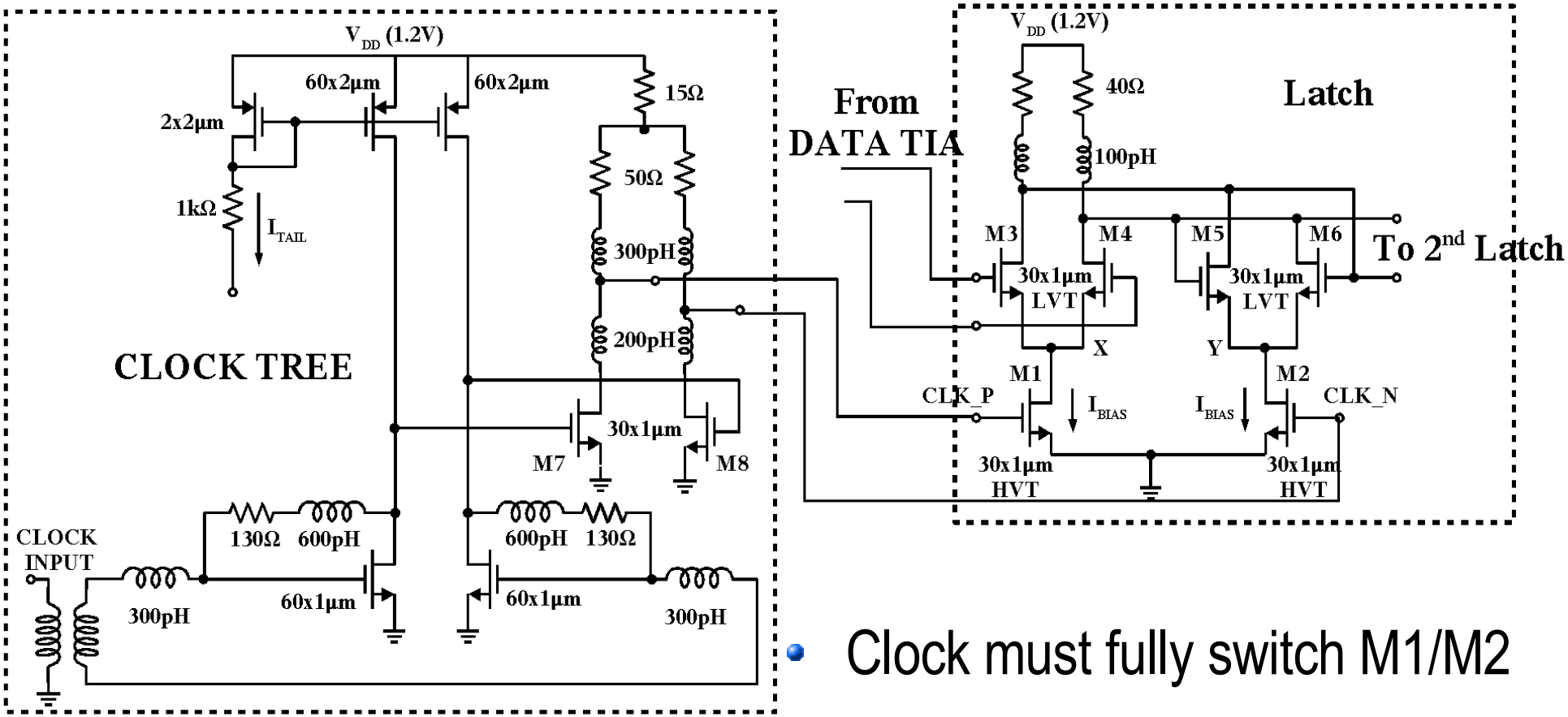




90nm CMOS retiming DFF (T. Chalvatzis et al. JSSC July 07)

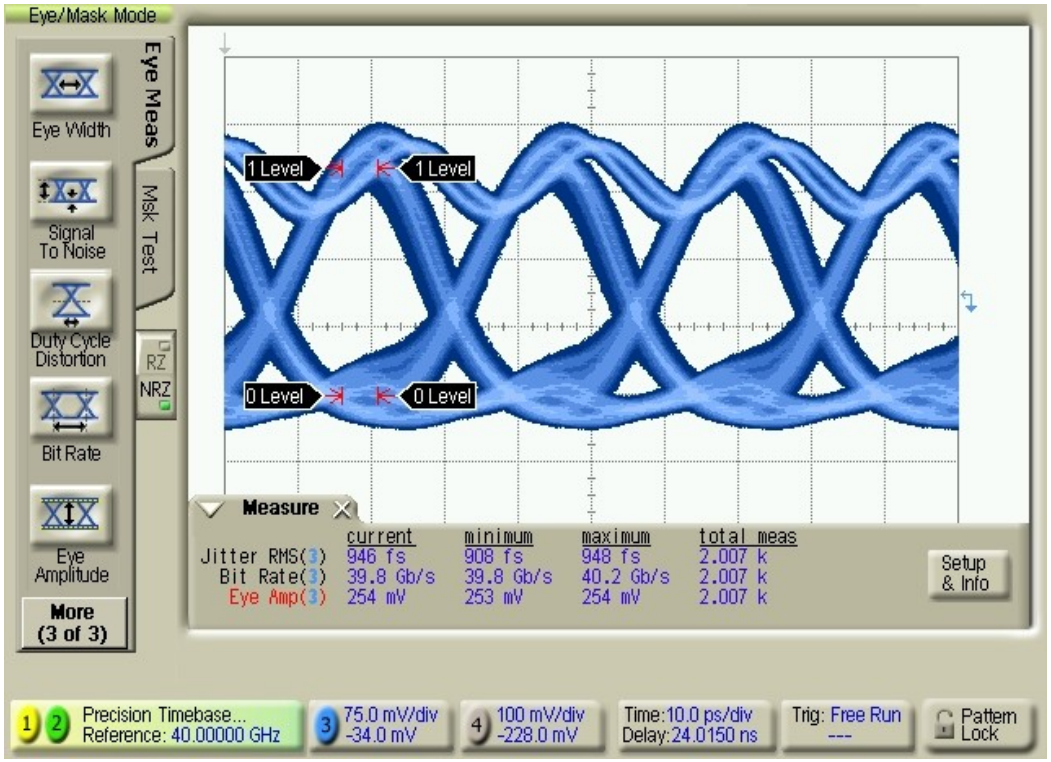


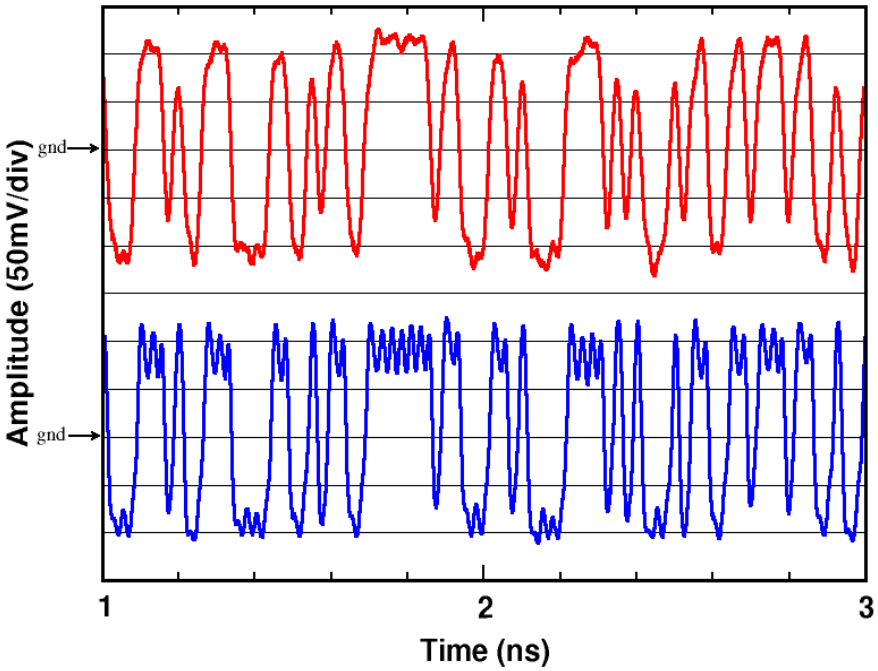
Clock-path biasing scheme



- Clock must fully switch M1/M2
- $V_{DS,M7/8}$ swings as low as V_T (M1/M2)
- Use high-V_T for M1/M2

Measurements at 40Gb/s and 1.2V





- Error-free 508-bit pattern
- Input (top), output (bottom)

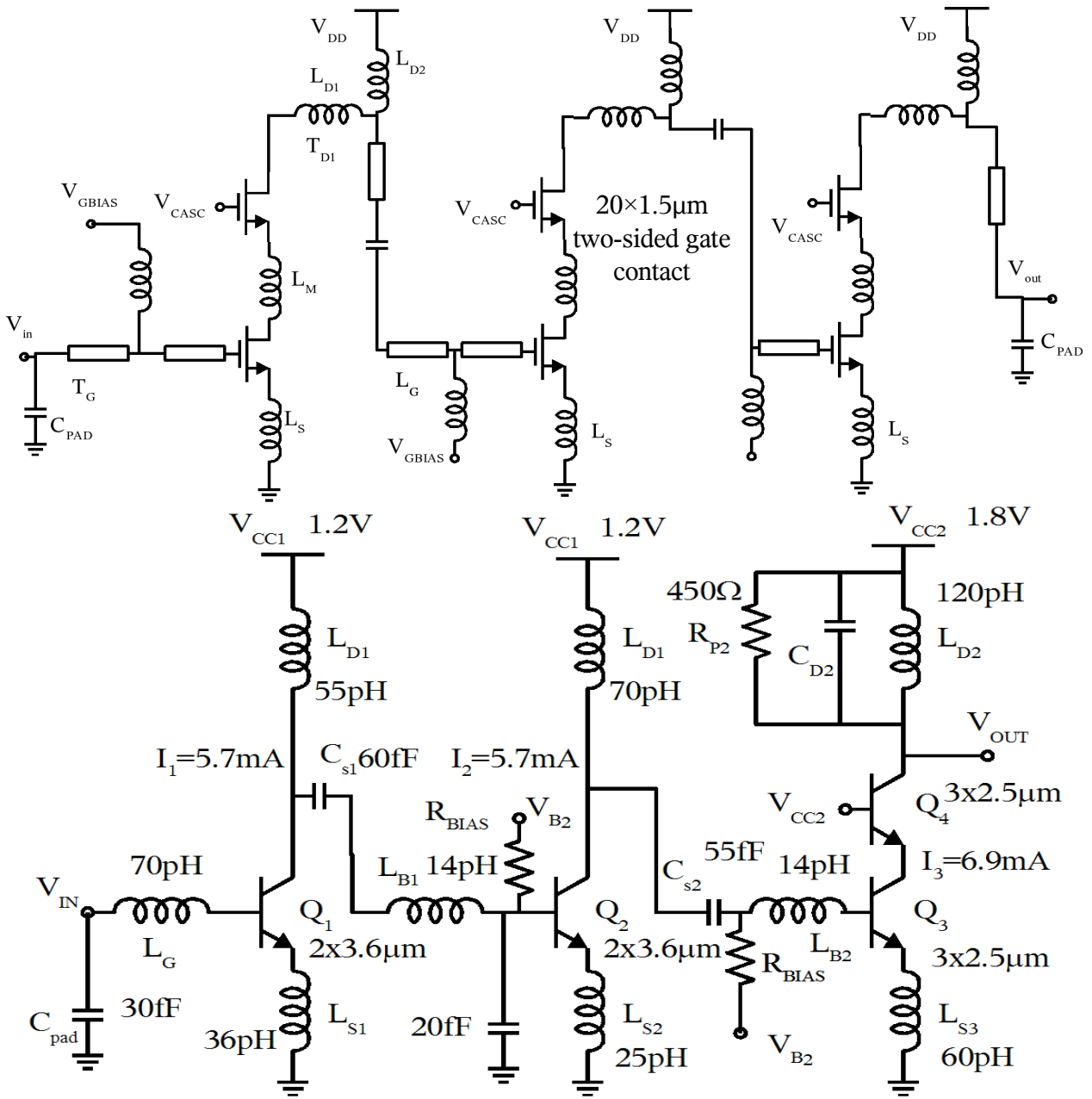
Reference	Technology	Rate	Supply	P_{LATCH}
[Suzuki,JSSC2004]	245-GHz InP HEMT	80Gb/s	5.7V	N/A
[Amamiya,JSSC2005]	150-GHz InP HBT	50Gb/s	1.5V	20mW
[Dickson,CSICS2006]	150-GHz SiGe BiCMOS	43.5Gb/s	2.5V	20mW
This work	120-GHz CMOS	40Gb/s	1.2V	10.8mW

CMOS vs. HBT amplifiers (useful as clock buffers)

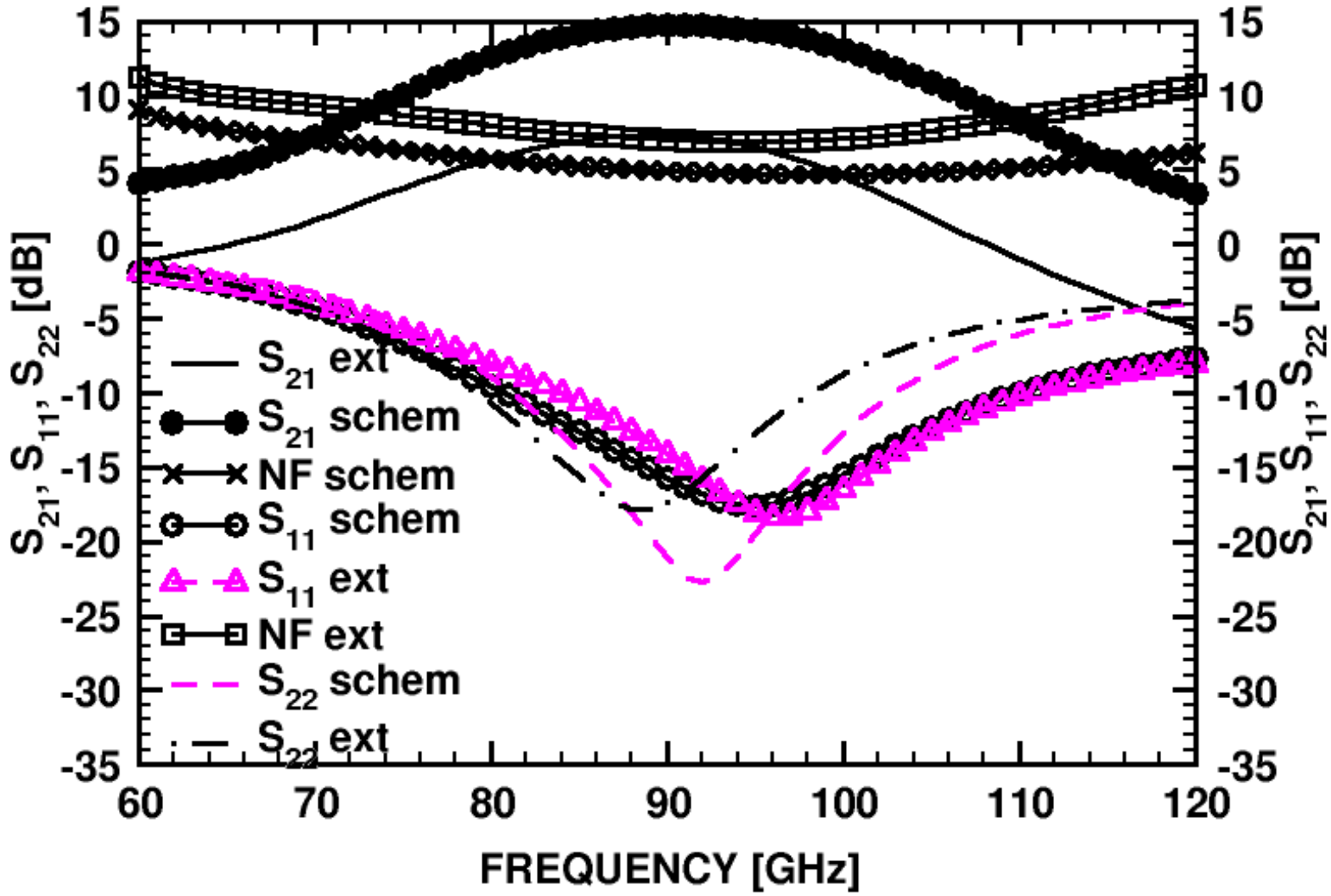
65nm LP CMOS
(55 mW, 13.5 dB)

290-GHz SiGe HBT
(52 mW, 25 dB)

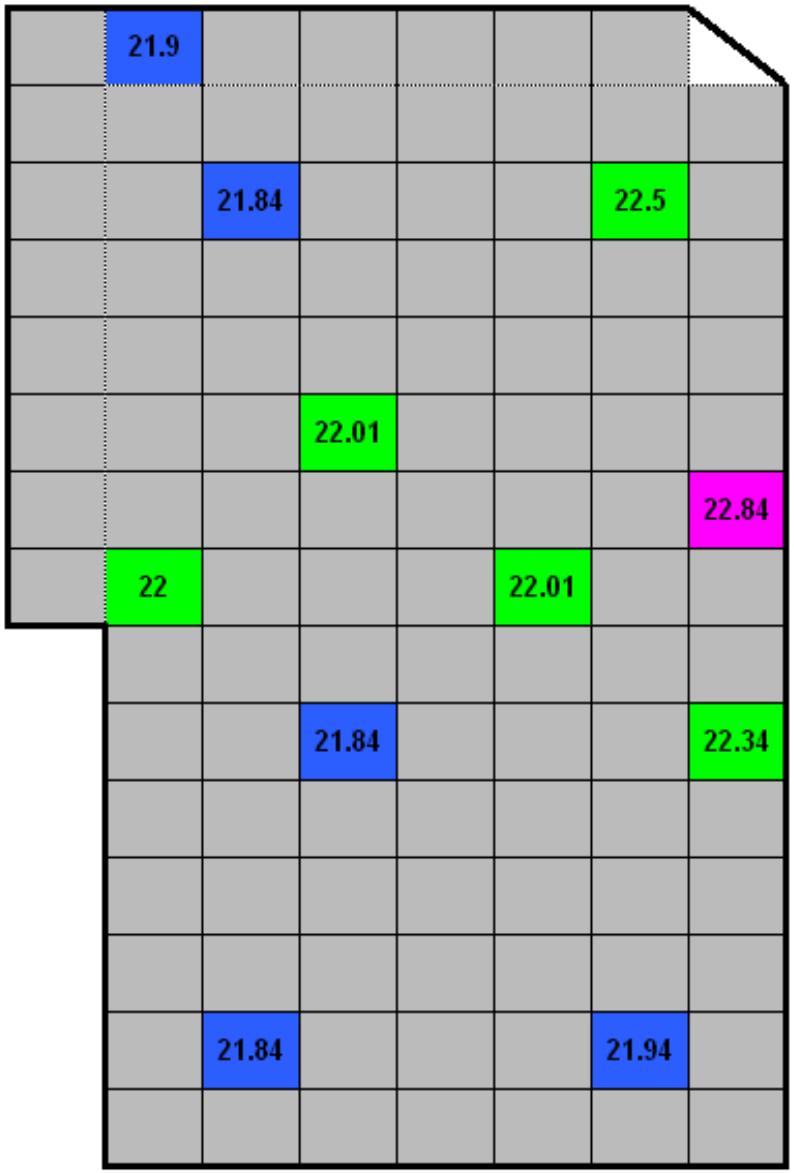
[S.T. Nicolson et al. IMS-07, CSICS-06]



Sims before and after extraction of transistor layout



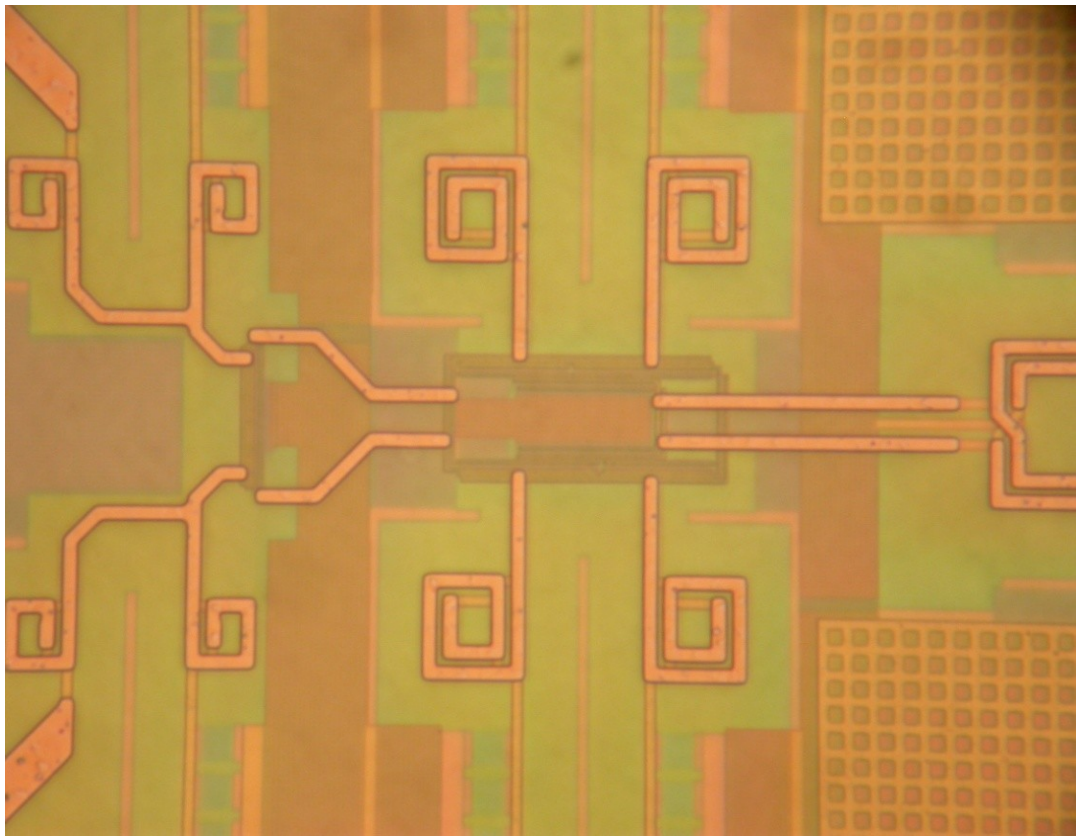
SOF Variation for 65nm LP Divider (v2): <4%



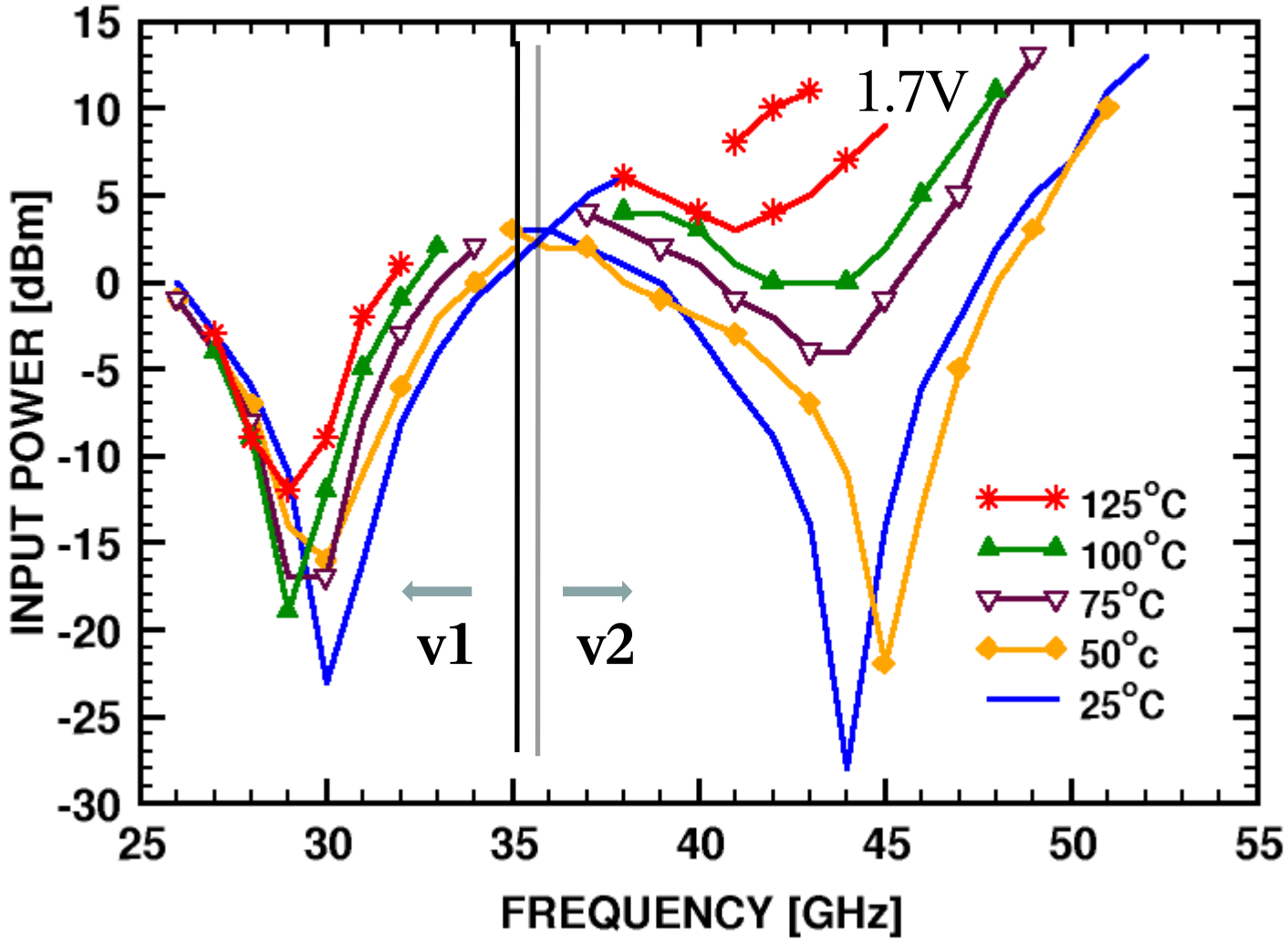
Mapping of 10 dies across the wafer shows < 4% variation in SOF

Average SOF = 22 GHz

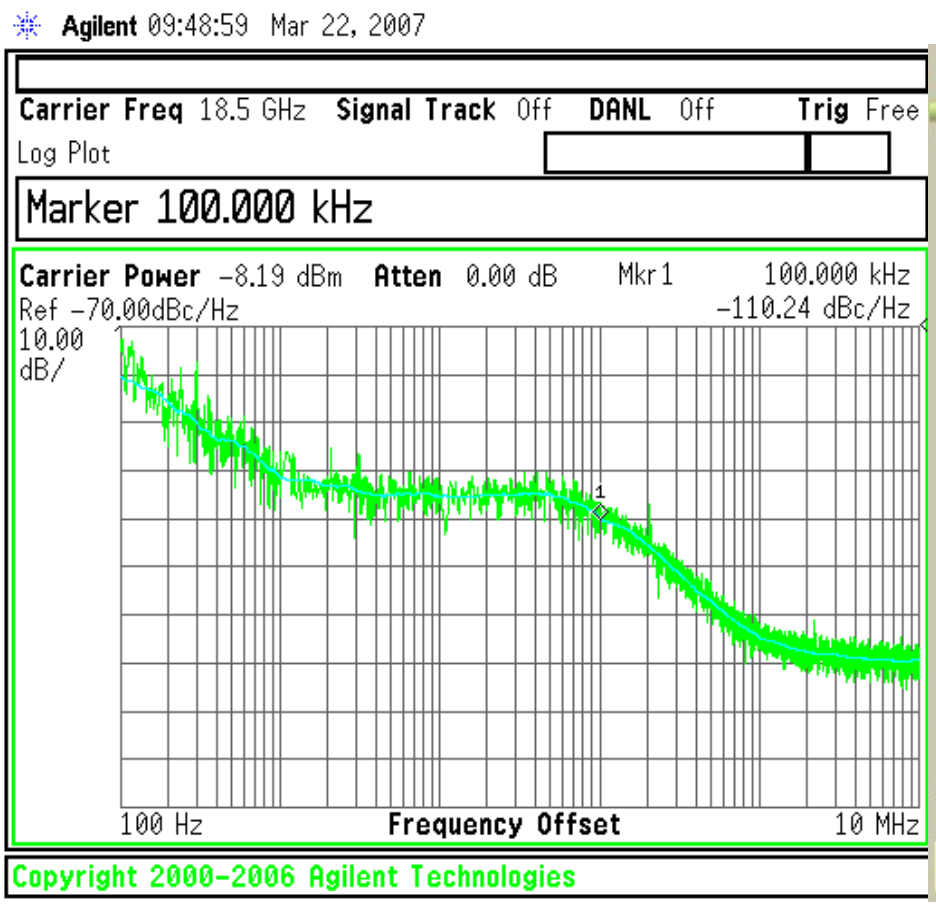
Power = 24mW / latch

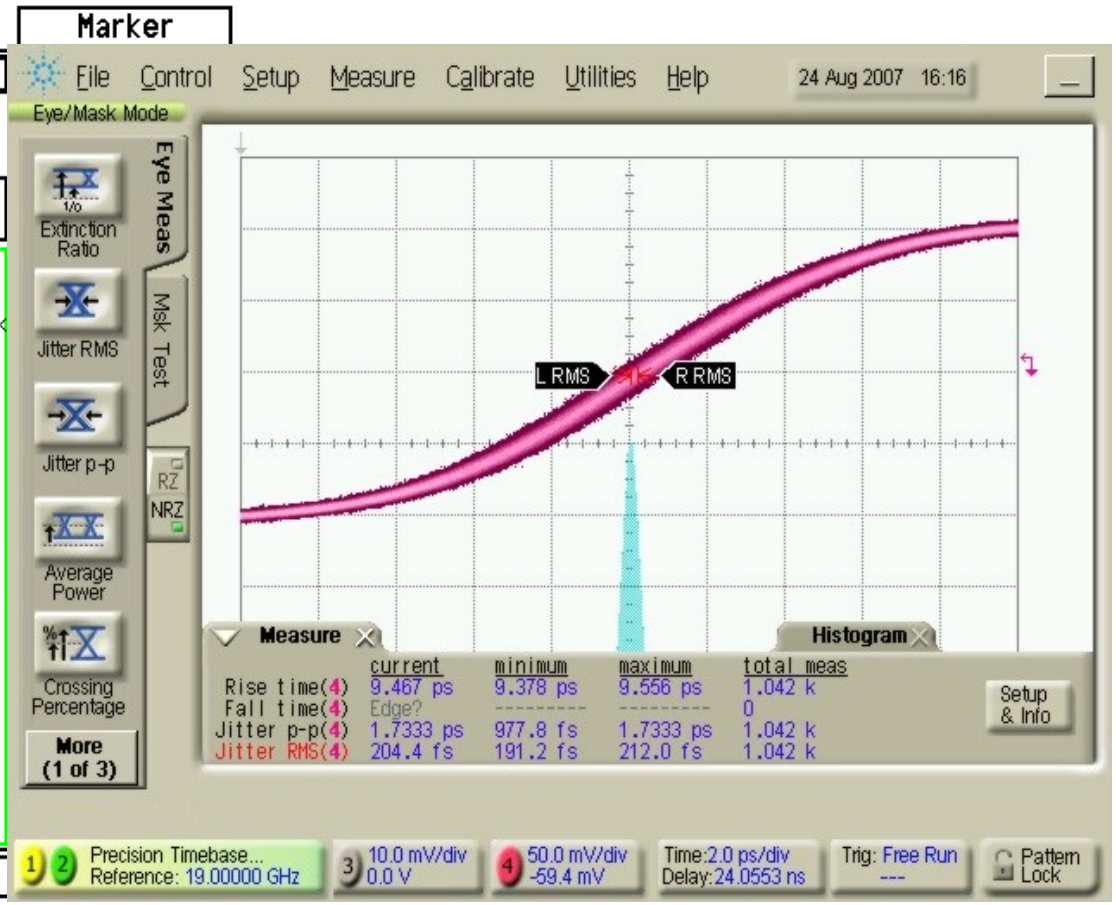


Measured sensitivity curves vs. temperature @ V_{DD}=1.5V



Phase Noise and Jitter Performance of 65nm LP Divider (v2) – 38GHz Input





18.5GHz divided down output

Output power = -8.2 dBm

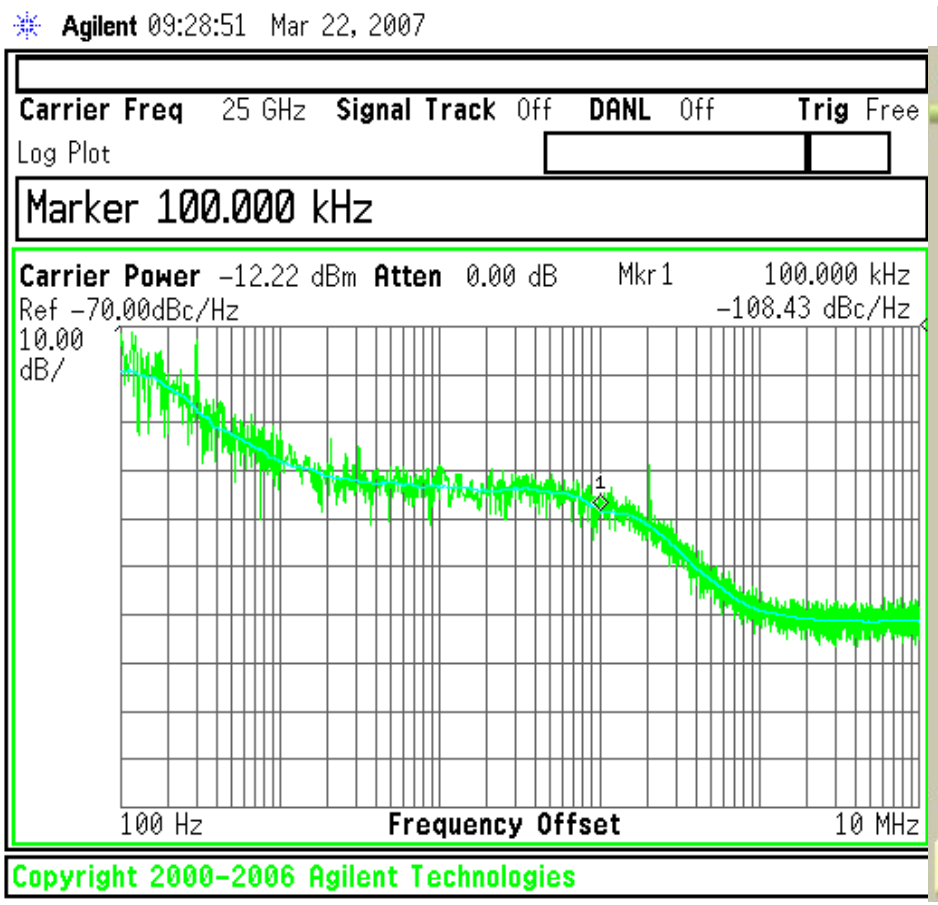
-110 dBc/Hz @ 100kHz offset

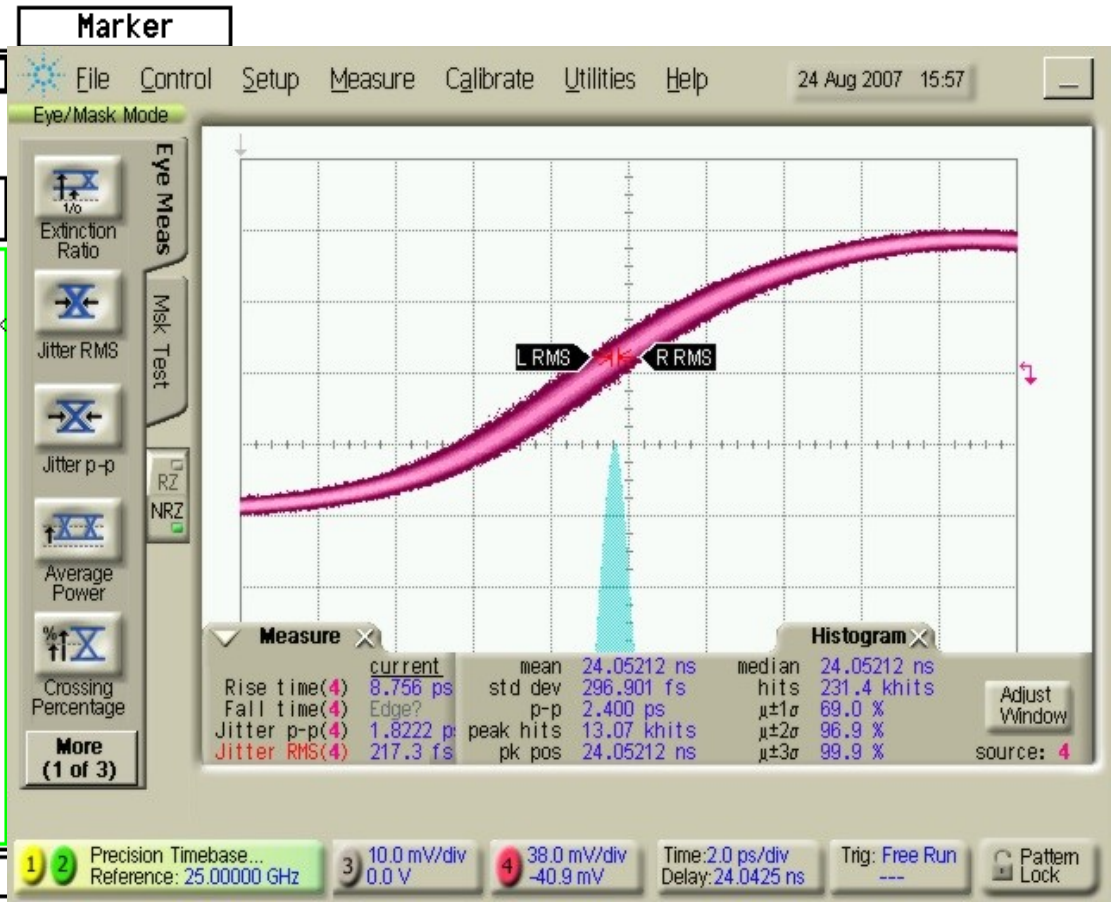
19GHz divided down output

Output swing = 200mV$_{pp}$

~200fs of RMS jitter

Phase Noise and Jitter Performance of 65nm LP Divider (v2) – 50GHz Input





25GHz divided down output

Output power = -12.2 dBm

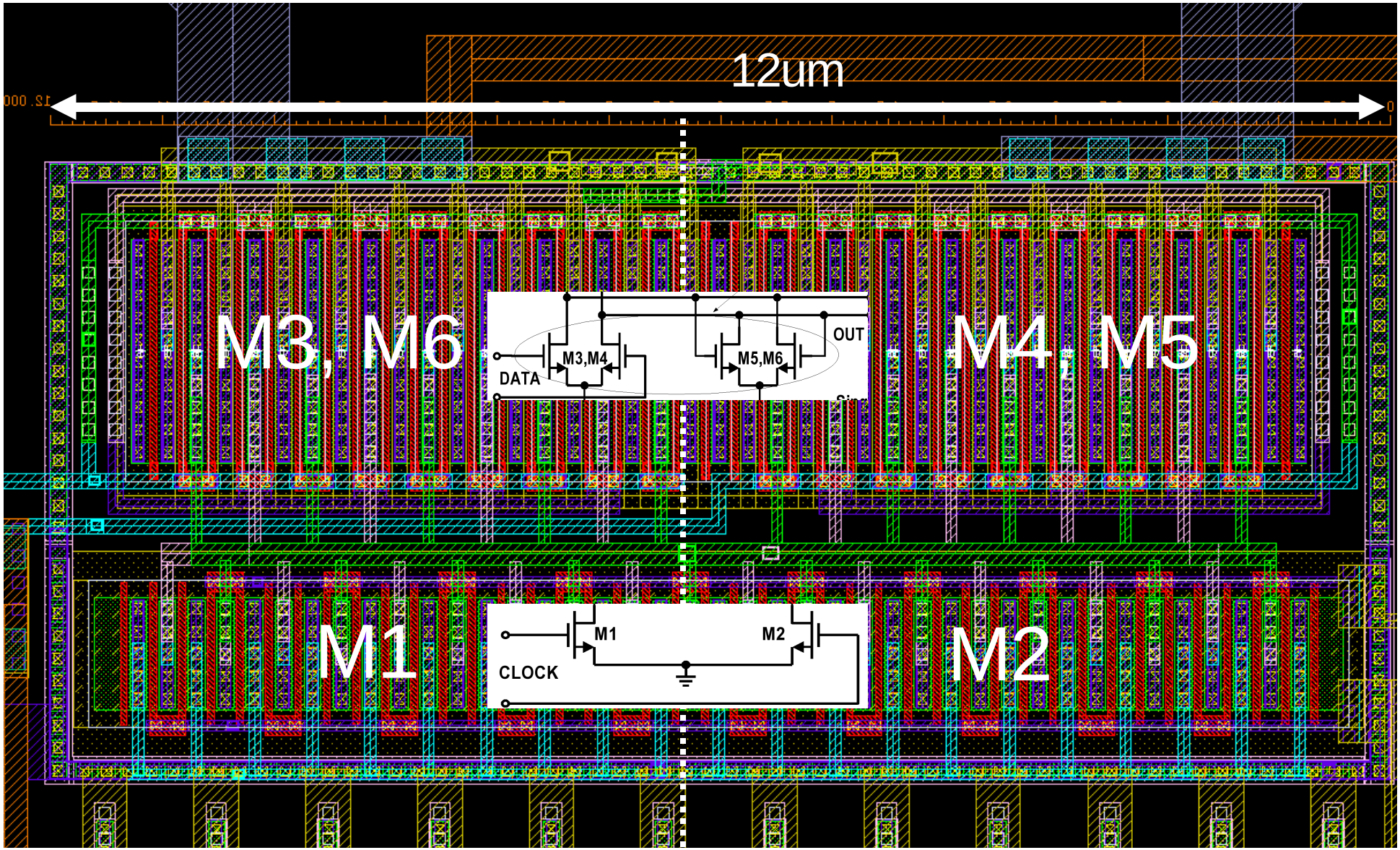
-108 dBc/Hz @ 100kHz offset

25GHz divided down output

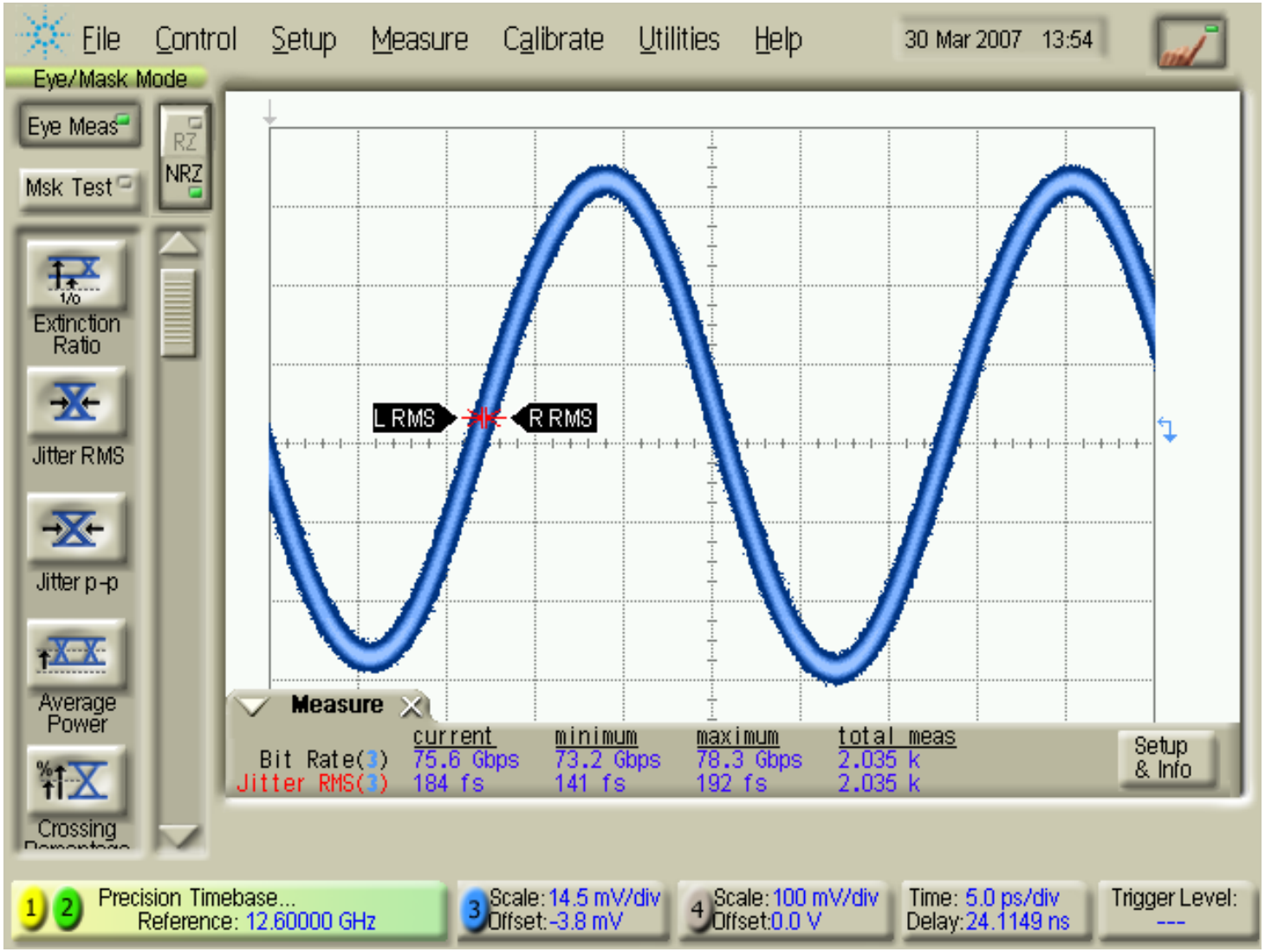
Output swing = $150mV_{pp}$

~217fs of RMS jitter

Latch layout (12 x 6 µm²)

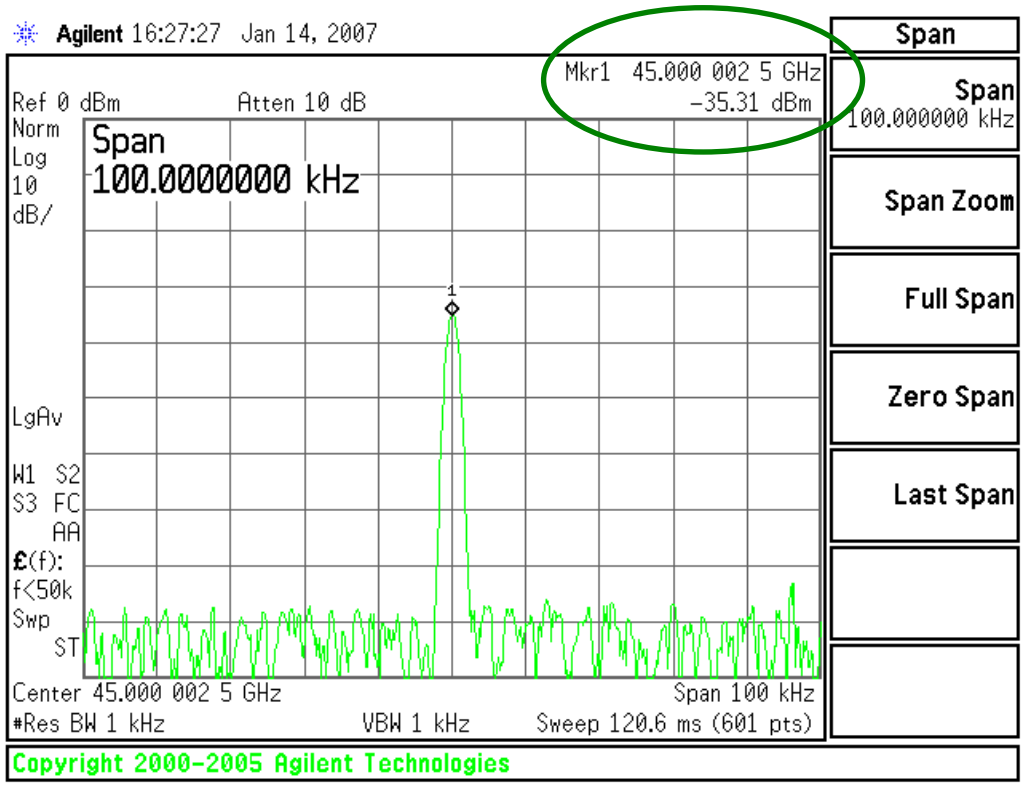


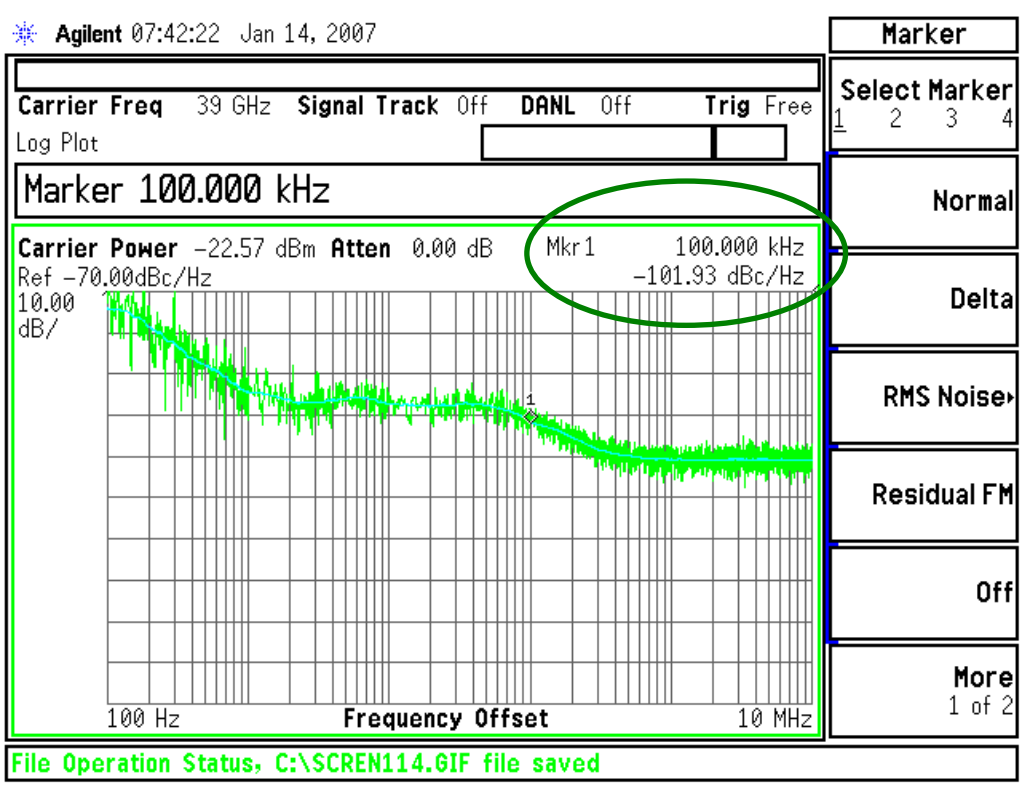
65nm GP CMOS time domain measurements



- 76 GHz divided down output signal showing low timing jitter

Output spectrum and phase noise





- 90GHz divided down spectrum
- 1.2V supply @ 25°C

- Output phase noise for 78GHz input
- 1.2V supply @ 25°C