Towards a sub-2.5V, 100-Gb/s Serial Transceiver

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***Abstract*-This paper describes first a half-rate, 2.5-V, 1.4-W, 87-Gb/s transmitter with on-chip PLL fabricated in a production 130-nm SiGe BiCMOS process. Next, the most critical blocks required for the implementation of a full-rate 100-Gb/s serial transceiver are explored. State-of-the art 105-GHz, SiGe HBT static frequency dividers and VCOs operating from 2.5-V supply, as well as 65-nm CMOS, 1.2-V, 90-GHz static frequency dividers, low-phase noise VCOs, and 100-GHz clock distribution network amplifiers are fully characterized over power supply and process spread, and over temperature up to 100°C. Inductor and transformer modeling and scaling beyond 200 GHz in nanoscale CMOS and SiGe BiCMOS technologies, are also described.**

I. Introduction

The volume of data transported over optical fiber and wireline networks continues to increase, most recently fueled by demands for bandwidth-intensive high-definition video broadcasts. Next generation serial communication systems are expected to operate at data rates in the 100-110 Gb/s range, as evidenced by recent calls for 100-Gb/s Ethernet (100GE). High-speed building blocks with low-levels of integration, such as multiplexers (MUX), demultiplexers (DeMUX), and clock and data recovery (CDR) circuits have been reported in the literature, operating at or above 80 Gb/s and implemented primarily in SiGe HBT or InP HBT technologies [1]-[4].

In SiGe HBT technology, such high data rates have been achieved at considerable power dissipation because of the heavy use of ECL topologies which, in addition to the higher supply voltage, exceeding 3.3V, require a larger number of tail current sources for a given logic function than CML circuits. For example, a 4:1 100-Gb/s ECL multiplexer dissipates at least 1.4 W, while a 100-Gb/s ECL CDR and 1:2 DeMUX consumes over 5 W [4]. A recently reported 70-Gb/s transceiver consumes 15 W [5], despite the fact that it was integrated in a technology with SiGe HBT cutoff frequencies exceeding 200 GHz. Such numbers, significantly higher than those obtained in InP HBT technology [6],[7] do not bode well for the integration of a single-chip 100GE serializer-deserializer (SERDES). In contrast, a state-of-the-art 10GE SERDES in 130-nm CMOS consumes only 800 mW [8], indicating that a more power efficient 100GE solution could be realized by operating ten 10GE channels in parallel. However, the latter solution increases system complexity and cost because of the commensurate increase in the number of optoelectronic components, which are significantly more expensive than the electronics. If a single-chip 100GE SERDES is to become economically feasible, power consumption must be lowered in SiGe BICMOS-based transceivers or a 1.2V CMOS technology capable of 100-Gb/s speeds must be developed.

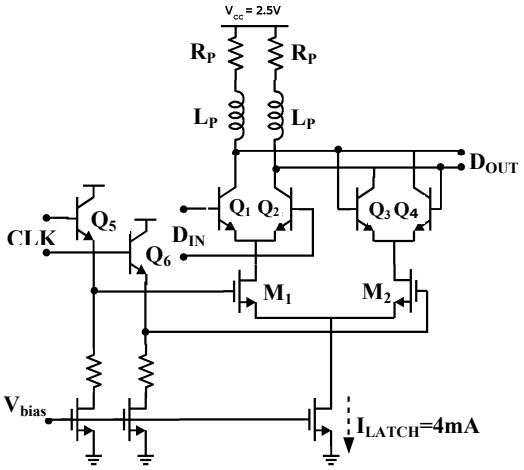

Fig. 1 20-mW, 43-Gb/s SiGe BiCMOS CML latch. Emitter followers are used only for level-shifting on the clock path but not on the data path [9].

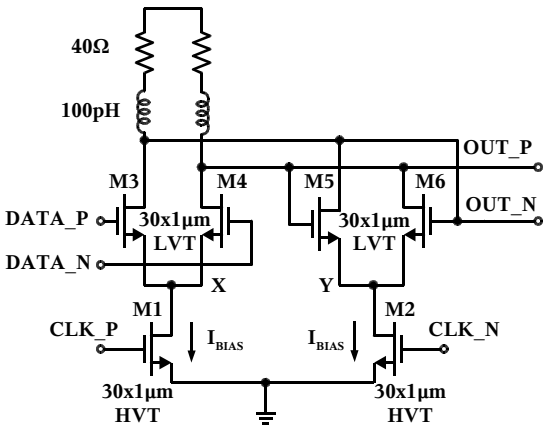

Fig.2 10-mW, 40-Gb/s MOS CML latch employing HVT and LVT devices [10].

This paper investigates the design of low-voltage BiCMOS [9] (Fig. 1) and 1.2-V CMOS [10] (Fig. 2) topologies required for a 100-Gb/s serial transceiver. In Section II, the transistor small signal model, the frequency scaling of inductors and transformers, as needed in mm-wave and 100-Gb/s digital circuits, and the design flow are discussed. Next, Section III

describes in detail the circuit design and experimental characterization of the 87-Gb/s transceiver. Finally, new 100-GHz SiGe BiCMOS and 65-nm CMOS building blocks that can form the core of a future full-rate 100-Gb/s transceiver are reviewed in Section IV.

II. Design Methodology

A. Emitter and Source Degeneration in Sate-of the-Art HBTs and Nanoscale MOSFETs

State-of-the-art SiGe HBTs and MOSFETs suffer from considerable emitter (source) degeneration. For example, at the peak f_T current density bias of 15mA/μm^2, the DC voltage drop on the parasitic emitter resistance R_E of a 300-GHz SiGe HBT [11] is 65-70 mV. One of the few benefits of the increased emitter degeneration is that the gain of the basic inverter or latch (Fig.1) is reduced by the amount of feedback ($1+g_m \times R_E \approx 3.5$) with a commensurate decrease of the Miller and base-emitter capacitance. As a result, the CML speed can approach that of ECL topologies while requiring both lower supply voltage, due to fewer transistors being stacked up vertically, and fewer current source tails, because of the elimination of emitter-follower stages. Indeed, recent publications have demonstrated that state-of-the-art 80-100 Gb/s SiGe [9] and InP HBT [7] CML circuits biased from 2.5V supply consume significantly less power than ECL ones [1],[4],[5],[12]. Moreover, it has been shown that by removing current tail transistors from the BiCMOS CML latch of Fig.1, the supply voltage can be further lowered to 1.8 V [11],[13].

Boosted by technology scaling, the intrinsic g_m of 65-nm GP n-MOSFETs approaches 1.8 mS/μm. However, due to the source resistance R_s of at least 200 Ω×μm, the effective g_{meff}, which controls small signal gain and switching speed, is degraded by the feedback loop gain $g_m \times R_s$ to only 1.32mS/μm. As a consequence, 65-nm GP n-MOSFETs are only 30% faster than 90-nm GP n-MOSFETs, while, even worse, 65-nm LP ("low-power") devices are about as fast as 90-nm FETs but, require higher V_{GS} and supply voltage in CML gates [14].

The source degeneration problem is further exacerbated in 65-nm or finer lithography CMOS by the high resistance, larger than 40 Ω, of every via contact between metal 1 and the salicided polysilicon gate or the source/drain regions. For the most part, high-speed and mm-wave circuit design in 65-nm CMOS is concerned not with schematics, but rather with maximizing the number of contacts per MOSFET gate finger and source stripe, and with layout optimization. To illustrate the impact of the series resistive parasitics in the MOSFET layout, Fig. 3 reproduces simulations before and after parasitic R-Cc extraction of the MOSFET layout for a 90-GHz, single-ended 3-stage cascode LNA implemented in 65-nm LP CMOS [14]. All other components are unchanged between the two simulations. The 8-dB degradation in gain and 2-dB increase in noise figure, without a significant shift in the center frequency of the LNA clearly point to the fact that resistive rather than layout capacitance parasitics are responsible. This significant drop in performance is commensurate with the expected improvement when ICs are scaled from 90-nm to 65-nm technology. It has important ramifications on where design effort should be directed.

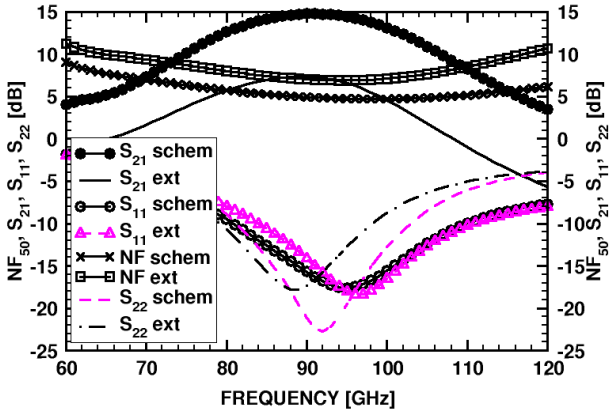

Fig. 3 Impact of transistor layout RC-parasitics on 90-GHz 65nm LP-CMOS amplifier gain and noise figure.

Constant-field scaling has allowed for a continued reduction in supply voltage with each new technology node, saturating at 1V in 90-nm and 65-nm GP technologies. However, for MOS-CML gates to operate above 40 Gb/s, the n-MOSFET requires a drain-source voltage of at least 0.5 V. The latter limits the number of vertically-stacked transistors to only 2, as illustrated in the MOS-CML latch of Fig. 2 and in the associated 40-GHz clock distribution network shown in Fig. 4 [10]. Note that, for the same reason, the data (top) path transistors in Fig. 2 must have a low threshold voltage (LVT), while the clock transistors must feature a high threshold voltage (HVT) to maintain the V_{DS} of the output buffer in the clock distribution network (Fig. 4) above 0.5 V. In addition, common-mode DC level shifting is provided by the 15-Ω resistor on the clock path to appropriately set the bias on the clock pair in the latch of Fig. 2 [10].

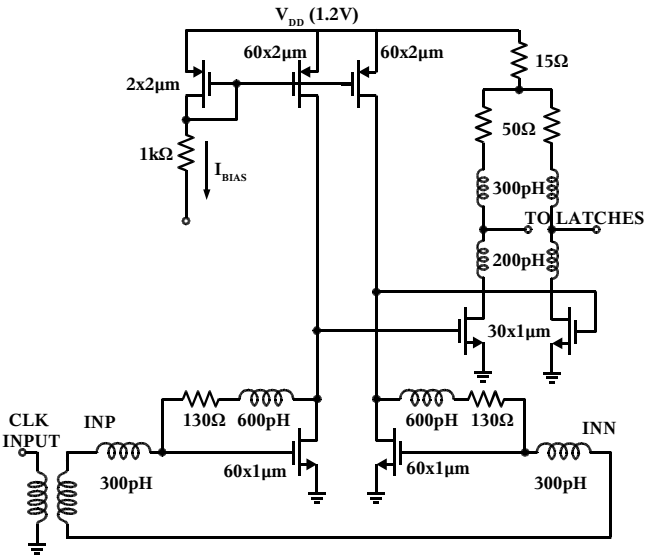

Fig. 4 40-GHz clock distribution network in 90-nm CMOS providing proper bias levels at the gates of the clock pair in the latch of Fig. 2 [10].

B. Frequency Scaling of Inductors and Transformers

Inductive peaking can be employed to maximize the bandwidth of CML circuits or to minimize their power consumption at a given speed [15]. One perceived drawback of using inductive peaking is the area occupied by the inductors. This can be mitigated by using the multiple metal layers available in CMOS or BiCMOS technologies to create stacked (or 3D) structures to obtain a larger inductance for a given area [16].

It is important to note that, like MOSFETs, spiral inductors also follow scaling laws. One can estimate the inductance L of a spiral constructed from *m* metal layers based on the number of turns *n*, outer diameter *d* and average diameter d_{avg} [17], [18].

$$L \approx \frac{6\mu_0 m^2 n^2 d_{avg}^2}{11d - 7d_{avg}} \tag{1}$$

From (1), it is observed that if the diameter is scaled by a factor *S*, the inductance also reduces by the same factor.

$$\frac{L}{S} \approx \frac{6\mu_0 m^2 n^2 \left(\frac{d_{avg}}{S}\right)^2}{\left(\frac{1}{S}\right)\left(11d - 7d_{avg}\right)} \tag{2}$$

Moreover, the oxide capacitance from the bottom metal layer to the substrate is a function of the total metal line length in one layer (*l*), the trace width (*W*), and the distance from the bottom metal layer to the substrate. If the length and width are scaled by the same factor *S*, the inductor area is reduced by a factor of S^2, as is the parasitic capacitance to ground.

$$C_{OX} \approx \frac{1}{2} lW \frac{\varepsilon_{OX}}{h} \Rightarrow \frac{C_{OX}}{S^2} \approx \frac{1}{2}\left(\frac{l}{S}\right)\left(\frac{W}{S}\right)\frac{\varepsilon_{OX}}{h} \tag{3}$$

This suggests that it is reasonable to integrate a large number of inductors on a single-chip, particularly at high frequencies where the required inductance value is not large. In the design to be presented in Section III, stacked inductors can be realized with outer diameters of between 10 μm and 20 μm. Interestingly, this is on the same order as the gate widths of the MOSFETs employed in 80-Gb/s logic circuits. The inductor quality factor is not of particular importance in shunt-peaking applications, as it can be absorbed in the resistive load. However for completeness it is instructive to see how *Q* scales with the inductor size. The DC resistance in a single metal layer can be determined by introducing the metal thickness *t* and metal resistivity ρ.

$$R_{DC} \approx \frac{\rho l}{Wt} \Rightarrow R_{DC} \approx \frac{\rho\left(\frac{l}{S}\right)}{\left(\frac{W}{S}\right)t} \tag{4}$$

While *l* and *W* are both reduced by *S*, the metal thickness and sheet resistance cannot be changed and the total series resistance remains constant. The same is true at high frequencies when the skin depth δ of the conductor is considered.

$$R_{AC} \approx \frac{\rho l}{W\delta\left[1-\exp\left(\frac{-t}{\delta}\right)\right]} \Rightarrow R_{AC} \approx \frac{\rho\left(\frac{l}{S}\right)}{\left(\frac{W}{S}\right)\delta\left[1-\exp\left(\frac{-t}{\delta}\right)\right]} \tag{5}$$

As a result, the peak quality factor of the scaled inductor is unchanged, but its peak-Q frequency becomes S times higher. Consequently spiral structures are as suitable for use at mm-wave frequencies above 30 GHz as they were for RF applications at 2 GHz.

C. Design Flow for High-Speed and Millimeter-Wave ICs in Nanoscale CMOS

Compared to analog and RF design flows, the design flow for mm-wave ICs is complicated by the need to model every piece of interconnect longer than 15..20 μm as a distributed transmission line. An effective way to contain the modelling effort is to include all interconnect leading to and from an inductor in the inductor itself, and to extract the 2π equivalent circuit of the ensemble using ASITIC, as in [16]. At the cell level, the main goal is to alleviate the impact of contact resistance on the source stripes and to minimize footprint by merging the transistor layouts of differential pairs and latching quads. This approach places via and contact resistances in common mode. The small cell-footprint reduces overall cell capacitance to the substrate and shrinks the length and parasitic resistance, inductance and capacitance of local interconnect. The accurate extraction of RC parasitics at the cell layout level is critical for the accurate modelling of the significant gain and noise figure degradation in circuits with nanoscale MOSFETs. Because of the larger R_E and R_b and smaller C_{bc}/C_{be} ratio (i.e. reduced Miller effect) for the same current, circuits realized with HBTs are less sensitive to layout parasitics than those with MOSFETs.

Based on these general observations, a design flow that has been found to work well up to 160 GHz is summarized below:

- Optimize the transistor/varactor emitter length l_E or gate finger width W_f to balance the degradation of f_{MAX} and NF_{MIN} due to R_E/R_s, R_b/R_g and minimize C_{bc}/C_{gd}. In circuits with MOSFETs and accumulation-mode MOS (AMOS) varactors, fix W_f and vary N_f to contain the impact of channel strain variation with W_f.
- Design the circuit at schematic level with R_g added to the MOSFET digital model. The latter is sufficient to turn a "digital" into a good "RF" model. R_S and R_d are normally already included in the digital model.
- Optimize the transistor, cascode, latch, or CMOS inverter cell layout through proper choice of metal stack on drain/collector and source/emitter, by monitoring f_{MAX} and NF_{MIN}. The optimal transistor layout depends on the stage topology: CE/CS, CB/CG, CC/CD, cascode, latch, CMOS inverter, etc.
- Include RC-extracted transistor layout in schematic.

- Design and model inductors and interconnect in ASITIC based on the desired inductance obtained from schematic-level design with extracted transistors and pad capacitance.
- Add the ground-plane and power-plane metal mesh and the metal fill patterns to the cell and extract the layout of the cell, excluding inductors.
- Add inductor and interconnect models to schematic of RC-extracted cell.
- Add interconnect between cells and model it in ASITIC, ADS or HFSS.

With this approach, the number of iterations between layout and schematic simulations is minimized and first-pass success with at least 10% accuracy is assured, even in the absence of RF foundry models for MOSFETs and varactors.

III. 2.5V, 87-Gb/s Half-Rate Transceiver

A. Circuit Design

Using the low-power design techniques presented in Section II, and the transistor biasing and sizing techniques from [15], an 80-Gb/s serial transmitter was designed in a 130-nm SiGe BiCMOS technology with 150-GHz f_T HBTs [19]. The block diagram of the transmitter is shown in Fig. 5. It consists of an 87-Gb/s, 8:1 multiplexer (MUX), an 87-Gb/s output driver with adjustable amplitude control, and a 43-GHz 16:1 frequency divider. Additionally, a low-power 10.7-Gb/s 2^7-1 PRBS generator is also included for built-in self-test [13]. For testing purposes, the 8 inputs to the MUX were aligned such that the 87-Gb/s output would also be pseudo-random.

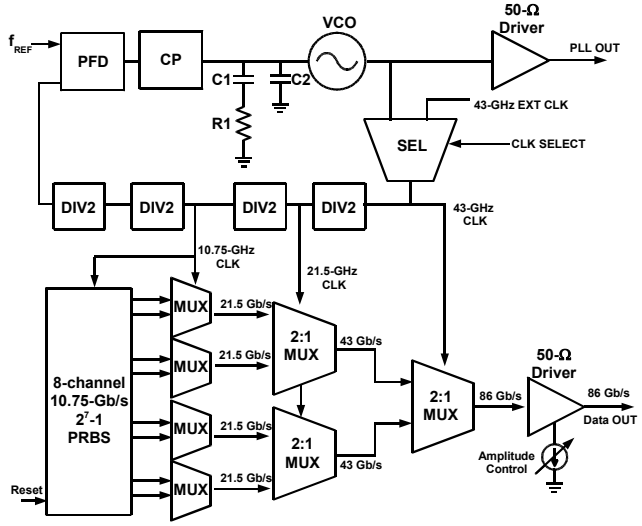

Fig. 5 Block diagram of the 80-Gb/s transmitter IC [9].

The 8:1 MUX is implemented by connecting several 2:1 multiplexers in a tree architecture. The final 2:1 multiplexer consists of five 43-GHz latches which align the data going into the 87-Gb/s selector. Note that the lower speed 2:1 multiplexers employ the same 5-latch architecture. The BiCMOS implementation of a 43-GHz latch was illustrated in Fig. 1. The schematic of the BiCMOS 87-Gb/s selector is shown in Figure 6. A combination of MOS source followers and HBT emitter followers are employed on the data and clock paths, respectively. The latter have higher bandwidth, making them more suitable for use on the 43-GHz clock path. Headroom considerations prevent the use of HBT followers on the input data paths if the circuit is to operate from 2.5 V. Instead, MOS source followers are employed on the 43-Gb/s input data paths. It is interesting to note that the combination of MOS and HBT devices on high speed paths gives rise to important DC biasing considerations. Of primary concern is the V_{DS} of transistors M_1 and M_2 in the selector. If the data and clock signals at the input to the source followers have the same common-mode level, it can be seen that the V_{DS} of both M_1 and M_2 at the quiescent point is nearly zero. This results in a significant degradation in the f_T of the MOSFETs and prevents the devices from switching at the required 43-GHz clock rate. To avoid this situation, a common-mode resistor is inserted in the clock buffer in a similar manner as in Fig.4. The voltage drop across this resistor sets the V_{DS} of M_1 and M_2 to ensure sufficient f_T/f_{MAX} for 43-GHz operation.

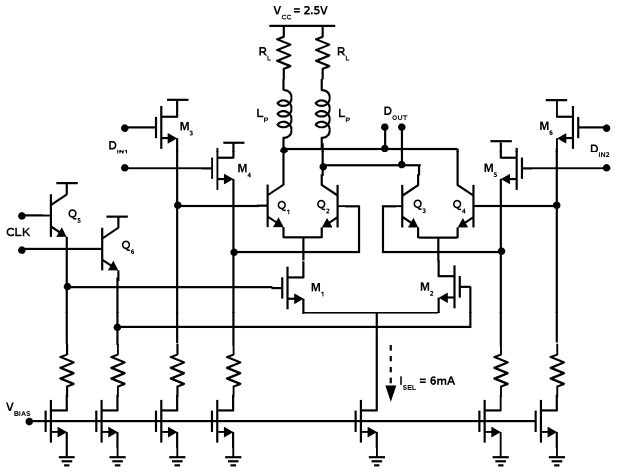

Fig. 6 60-mW. 87-Gb/s BiCMOS selector.

The 87-Gb/s selector is followed by a 50-Ω output driver with a BiCMOS cascode and adjustable amplitude control. Measured S-parameters of a breakout of this driver were presented previously [15], which show that the output match is unaffected by the change of tail bias current in the BICMOS cascode. Intentional gain peaking at higher frequencies is introduced to compensate for losses in the cables and probes anticipated in the measurement setup. Note that the 130-nm n-MOSFETs with f_T of 85 GHz switch at the full-rate of 87Gb/s, the fastest for any MOSFET digital circuit reported to date.

The critical blocks of the 2.5-V, 40-GHz BiCMOS PLL are the Colpitts VCO and the phase frequency detector, implemented for the first time with BiCMOS CML logic, as illustrated in Fig. 7. The VCO employs SiGe HBTs and differentially-tuned accumulation-mode MOS varactors [20]. It is noted that the base-to-collector capacitance C_{bc} loads the tank and degrades the oscillator tuning range. To compensate for C_{bc}, cross-coupled neutralization capacitors are introduced [20]. The output of the VCO is taken from the collector, resulting in improved isolation.

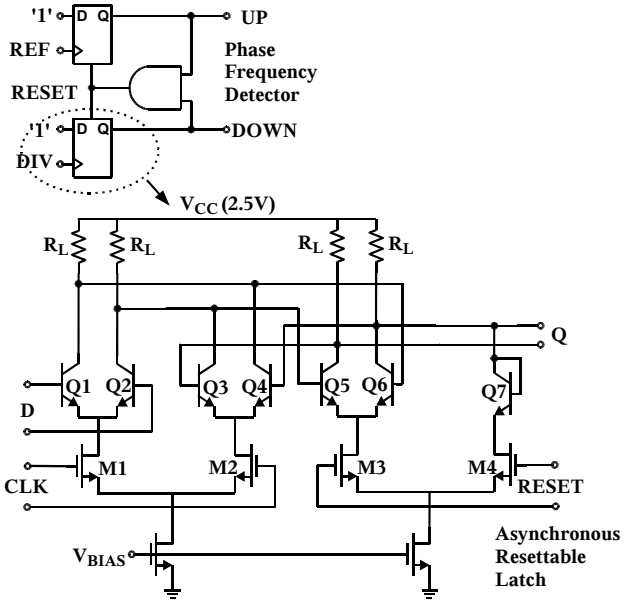

Fig. 7 Phase-frequency detector and schematic of the resettable latch.

B. Experimental Results

The transmitter IC and associated test structures were fabricated in a 130-nm SiGe BiCMOS technology with SiGe HBT f_T of 150 GHz [17]. A separate VCO test structure was also fabricated and measured on-die using an Agilent E4448A PSA and E4419B power meter with DC-to-50-GHz power sensor. The tuning range and output power are depicted in Fig. 8 showing that the VCO is tunable from 36.7 to 42.7 GHz (15.1%) at room temperature. The oscillation frequency remains remarkably constant over temperatures from 25°C to 100°C, a direct result of employing a tank which does not rely on base-to-emitter capacitances to set the oscillation frequency. A MIM capacitor C_1 is placed across C_{BE} of the tank transistor to reduce the impact of its variation with bias and temperature on the oscillation frequency. Furthermore, the oxide capacitance of the AMOS varactor is less temperature-sensitive than the capacitance of a pn-junction varactor. The measured phase noise is -103 dBc/Hz at a 1-MHz offset and the power consumption is 20 mA from a 2.5-V supply.

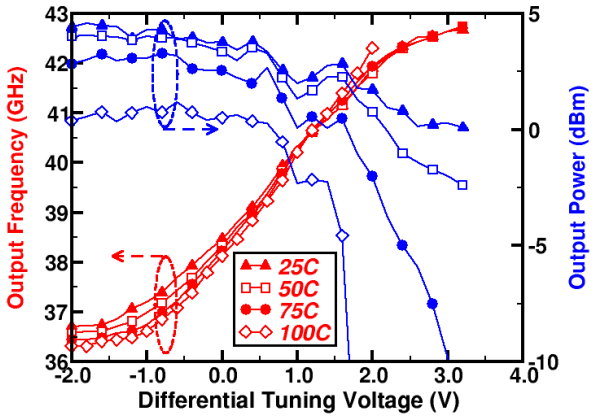

Fig. 8. Measured VCO tuning range and output power vs. temperature.

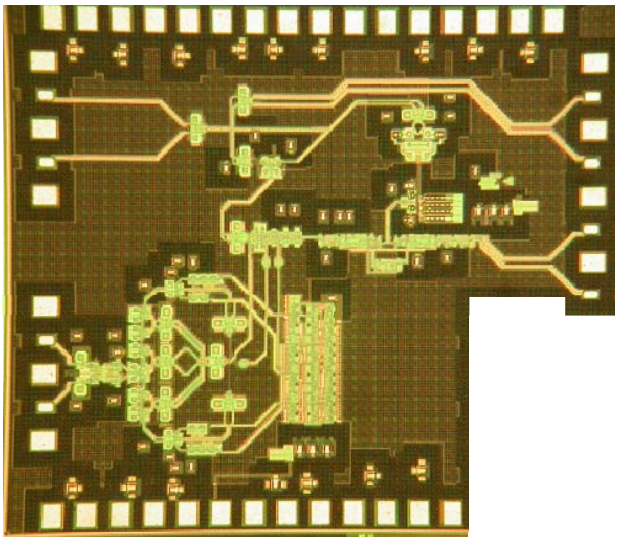

Fig. 9. 87-Gb/s stransceiver die photograph.The differential 87-Gb/s output is at the bottom left side of the die.

The die photo of the transmitter IC is shown in Fig. 9 and measures 1.5mm×1.8mm. It includes an on-chip 40-GHz clock multiplier unit (CMU) which is tunable from 38 to 42 GHz. Although the in-band PLL phase noise is between -80 dBc/Hz at 100-KHz offset and -95 dBc/Hz at the 3-dB bandwidth of 30 MHz, the CMU jitter is too high and the transmitter was tested using a lower noise, external 40-GHz clock. All measurements were conducted on-die with a temperature-controlled probe station. An Agilent 86100C DCA with 86107A 40-GHz precision timebase and 86118A 70-GHz remote sampling heads was employed in time domain measurements. Figs. 10 and 11 depict single-ended output eye diagrams with 300-mV per side at 80 Gb/s and 87Gb/s, respectively. Additionally as PRBS sequences are periodical, the sequence length can be determined by examining tone spacing in the output power spectrum, as seen in Fig. 12. The temperature dependence of the maximum operating data rate is shown in Fig. 13. The transmitter is functional up to 71Gb/s at 100°C and 92 Gb/s at 0°C.

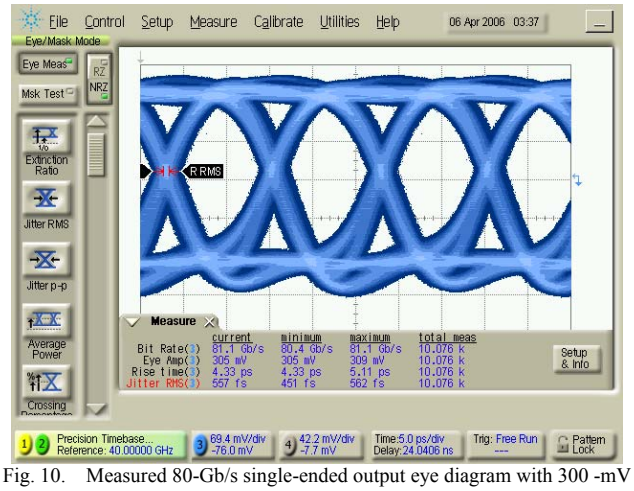

Fig. 10. Measured 80-Gb/s single-ended output eye diagram with 300 -mV swing per side.

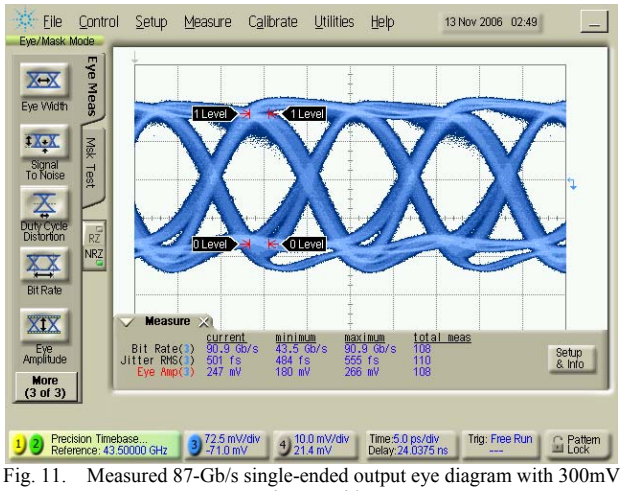

Fig. 11. Measured 87-Gb/s single-ended output eye diagram with 300mV swing per side.

The total power dissipation is 996 mW from a 2.5-V supply, and breaks down as follows: 372 mW for the 8:1 MUX, 172 mW for the output driver, 85 mW for the 16:1 frequency divider, 222 mW for the clock distribution, and 145mW for the on-chip 2^7-1 PRBS generator. If the 360 mW from the PLL is also considered, this work demonstrates that an entire 80-Gb/s transmitter can be realized with a power dissipation of about 1.4 W. Comparing with state-of-the-art CMOS results at the same lithography node [21], this work shows that by adding a SiGe HBT to a CMOS process one can realize a serial transmitter with double the data rate while dissipating half of the power.

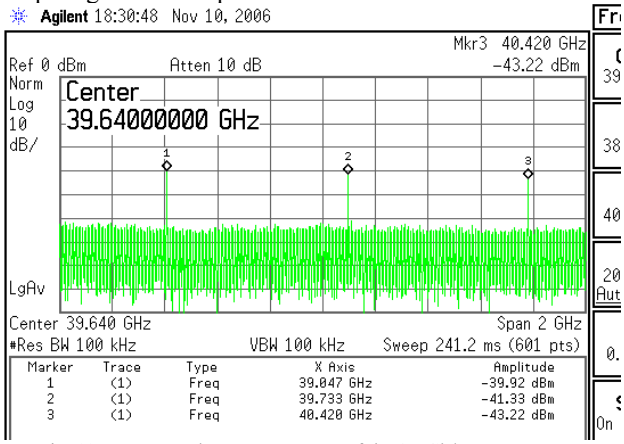

Fig. 12. Measured output spectrum of the 87-Gb/s output pattern demonstrating correct PRBS multiplexing.

IV. 100-GB/S FULL-RATE TRANSCEIVER BLOCKS

A. Static Frequency Dividers and Flip-Flops

Static frequency dividers with the highest reported self-oscillation frequency of 91.8 GHz for SiGe HBT, and 81 GHz for 65-nm GP CMOS implementations, were designed and fully characterized over process spread, power supply and temperature variation. The block diagram, shown in Fig.14 includes an on-chip transformer for single-ended to-differential conversion of the input signal at frequencies beyond 100 GHz [22]. The SiGe HBT latch, whose schematic is reproduced in Fig. 15, operates from a 2.5-V supply and is a modified version of the one in [24] where the current tail source has been removed from the differential pair to gain voltage headroom. Since a DC voltage of 70 mV falls across the internal emitter resistance of the SiGe HBTs, the absence of the current source, or of a resistor, in common mode does not seriously affect the operation of the divider over bias and temperature supply variation. At room temperature, the divider consumes only 28 mW per latch and operates correctly up to at least 105.4 GHz - the upper frequency limit of the signal source - with a sensitivity better than 0 dBm.

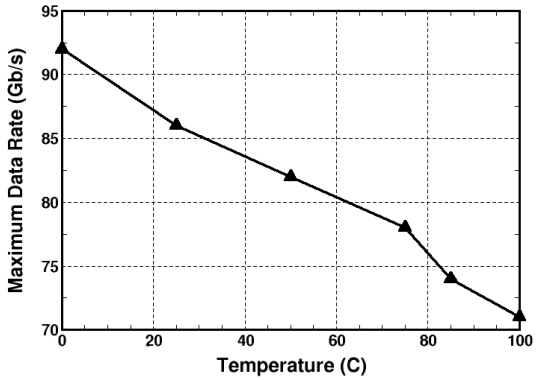

Fig. 13. Measured output data rate as a function of operating temperature.

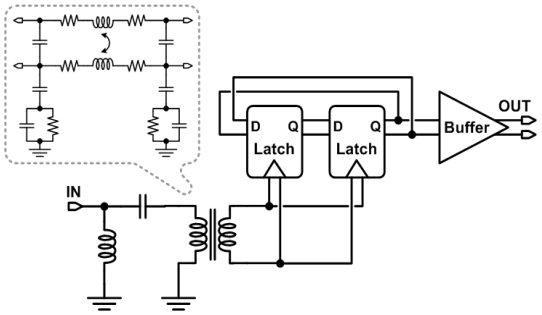

Fig. 14. Block diagram of static frequency divider test structures.

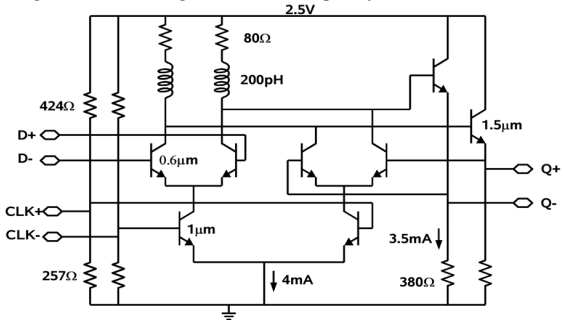

Fig. 15. 2.5V SiGe HBT latch schematic employed in the 105-GHz static frequency divider.

The 65-nm GP CMOS divider, whose die photo is shown in Fig. 16, employs the latch topology from Fig. 2 with 20% smaller latching pair. The transistors in the main differential pairs have a total gate width of 20 µm and are biased at 0.3-0.4 mA/µm when fully switched. Fig. 17 compares the

sensitivity curves of the 2.5-V SiGe HBT and 1.2-V CMOS dividers at room temperature with that of the divider reported in [22]. The CMOS divider operates from supplies as low as 1.0 V and divides correctly up to 90 GHz, dissipating a record 9.6 mW per latch. Operation at 100°C was verified up to 80GHz. The divided-by-two self-oscillation-frequency (SOF) was mapped across two thirds of a 12'' wafer showing a remarkably low spread of only 1.04 GHz (2.6%) with an average value of 39.6 GHz. The SOF of all 60 dividers that were tested is included in the wafer map of Fig. 18.

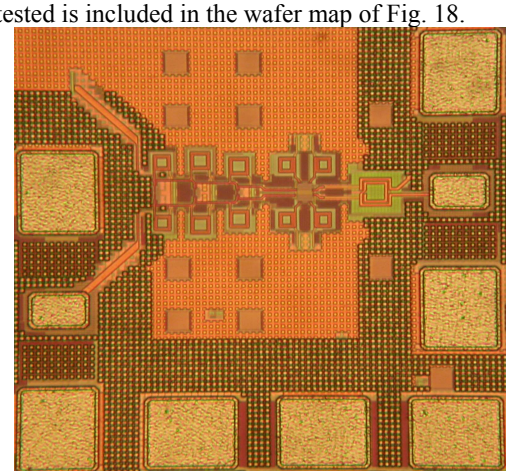

Fig. 16. 1.2V 90-GHz, 65nm GP CMOS static divider die photograph.

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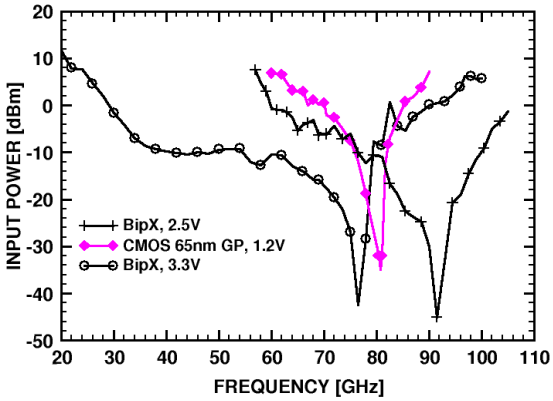

Fig. 17 Measured sensitivity of the SiGe HBT and CMOS static dividers.

B. Low Phase-Noise VCOs

Low-phase-noise Colpitts VCOs (Fig. 24) were implemented with SiGe HBTs [20] (Fig. 19) and 90-nm GP MOSFETs [23] for operation in the 77-GHz to 105-GHz range. The tank inductance (L_B) was chosen as the smallest realizable inductance with high Q, about 25pH for the HBT. In the W-band, the finite Q of the varactor (C_{VAR}) and of the base/gate inductance (L_B) adds substantial losses to the tank. Capacitor C_1 is important in minimizing the oscillator phase noise. Record phase noise values of -101.3 and -100.2 dBc/Hz, respectively, were measured at 1MHz offset from the 105GHz SiGe HBT VCO carrier and from the 79-GHz carrier of the CMOS VCO [23]. However, the output power is at least 18 dB higher for the SiGe HBT VCO, while its power consumption is only 4 times larger: 120 mW vs. 30 mW.

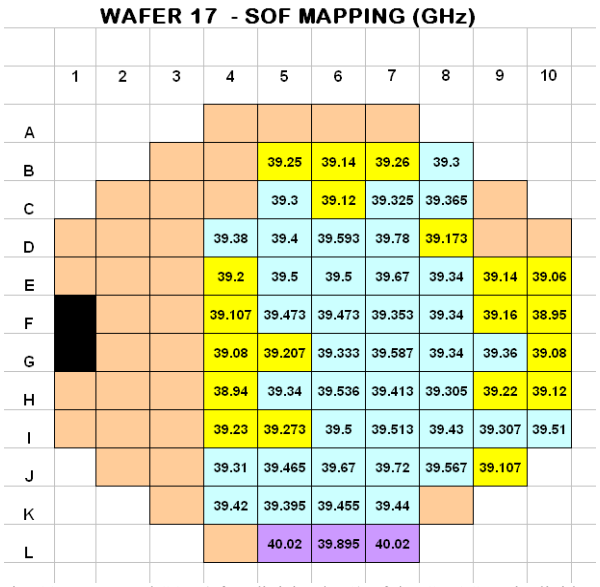

Fig. 18 Measured SOF (after division by 2) of the CMOS static dividers across a 12'' wafer.

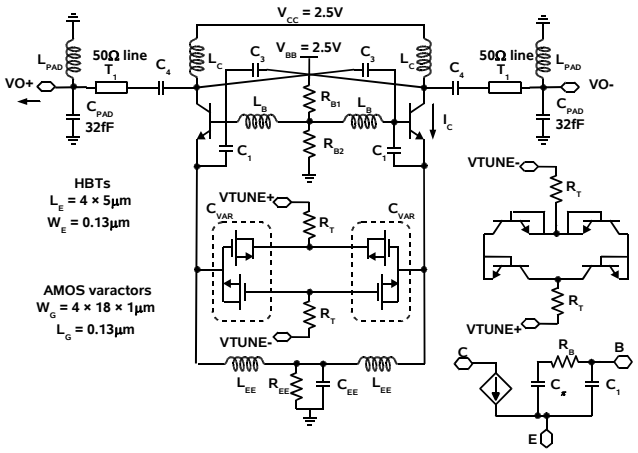

Fig. 19 105-GHz SiGe HBT Colpitts oscillator schematics.

The tuning range and output power of the 105-GHz SiGe HBT VCO with pn-junction varactors was measured over temperature up to 100 ^{0} C. As in the case of the 40-GHz SiGe HBT VCO, at a given control voltage, the frequency changes by less than 1%. The tuning range and its temperature stability are expected to improve further when the junction varactors are replaced by AMOS varactors in the BiCMOS version.

C. 100-GHz Clock Distribution Networks

It is now possible to build a 2.5-V clock distribution network at 100 GHz using HBT-HBT or MOS-HBT cascodes (Fig.20) in a SiGe BiCMOS process, and cascode inverters in a 65-nm CMOS process. As shown in Fig.21, the measured 3dB bandwidth of the clock buffers exceeds 15% with a gain of several dB at 100 GHz.

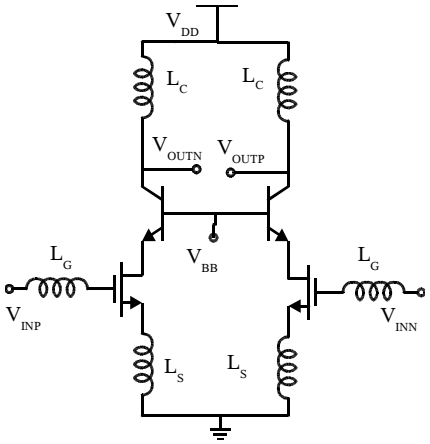

Fig. 20 80-100 GHz SiGe BiCMOS cascode buffer schematics.

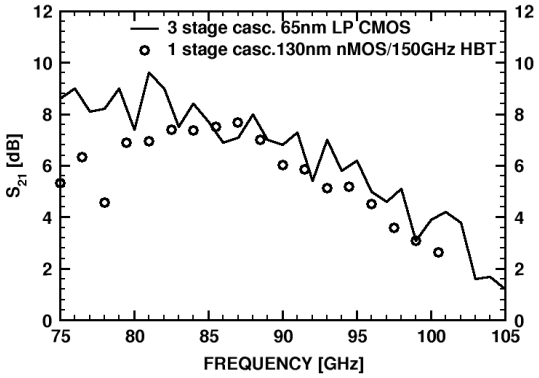

Fig. 21 80-100 GHz SiGe BiCMOS and 65nm CMOS cascode amplifier gain as a function of frequency.

V. Conclusion

A sub-2.5V serial 100-Gb/s transceiver with half-rate architectures is now viable in prototype SiGe BiCMOS technology. This transceiver can be developed using low-voltage MOS-HBT topologies, inductive peaking, and CML rather than ECL logic. The design and characterization of critical SiGe HBT and 65-nm CMOS blocks (VCO, static frequency divider and clock distribution) has also been conducted over process spread, supply voltage and temperature in an attempt to asses the feasibility of a full-rate serial transceiver architecture at 100 GHz. Full-rate, rather than half-rate architectures are currently employed in production 10-Gb/s and 40-Gb/s optical fiber systems. To date, a static frequency divider has only been demonstrated up to 97 GHz at 100 ^{0}C in SiGe, and up to 79 GHz at 100 ^{0}C in 65-nm GP CMOS technology, and appears to be the main roadblock, along with the 100-GHz flip-flop.

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