Methodology for Simultaneous Noise and Impedance Matching in W-band LNAs

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Outline

- Introduction
- Noise matching issues at mm-waves
- Mm-wave LNA design methodology
- 80-94 GHz CMOS LNA examples
- Summary

Motivation

80-100 GHz applications

- Automotive radar (SiGe BiCMOS)
- Active/passive imaging (SiGe BiCMOS, 65nm CMOS)

NF_{MIN} of nanoscale MOSFETs is very competitive at mm-waves

(P.Chevalier et al. CSICS-2006)

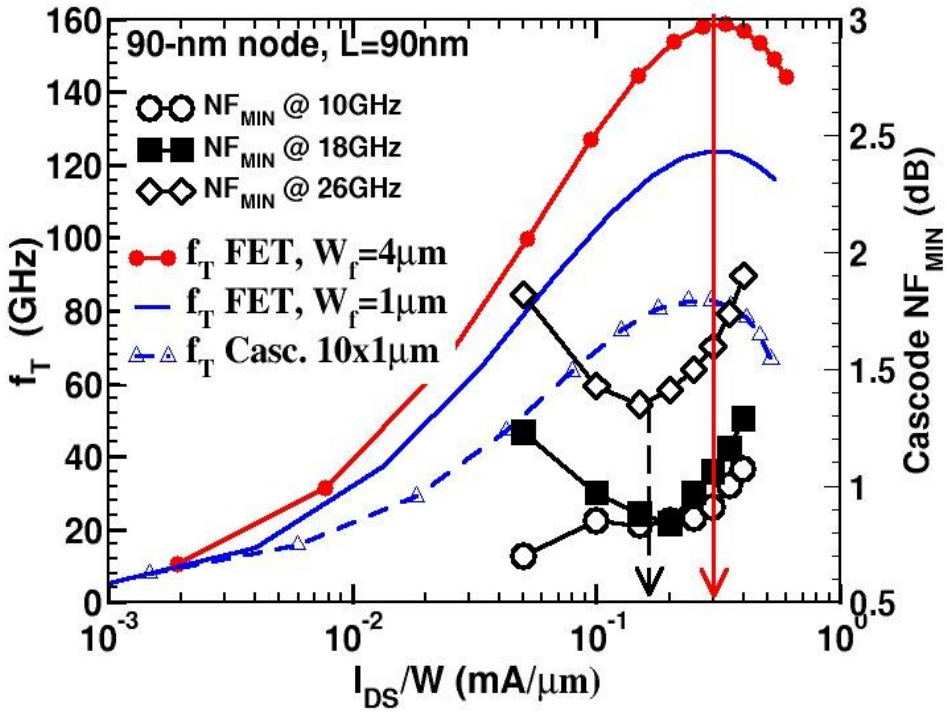
Issues

Pad capacitance and bondwire or flip-chip bump inductance

SiGe HBT and CMOS LNA Design Philosophy

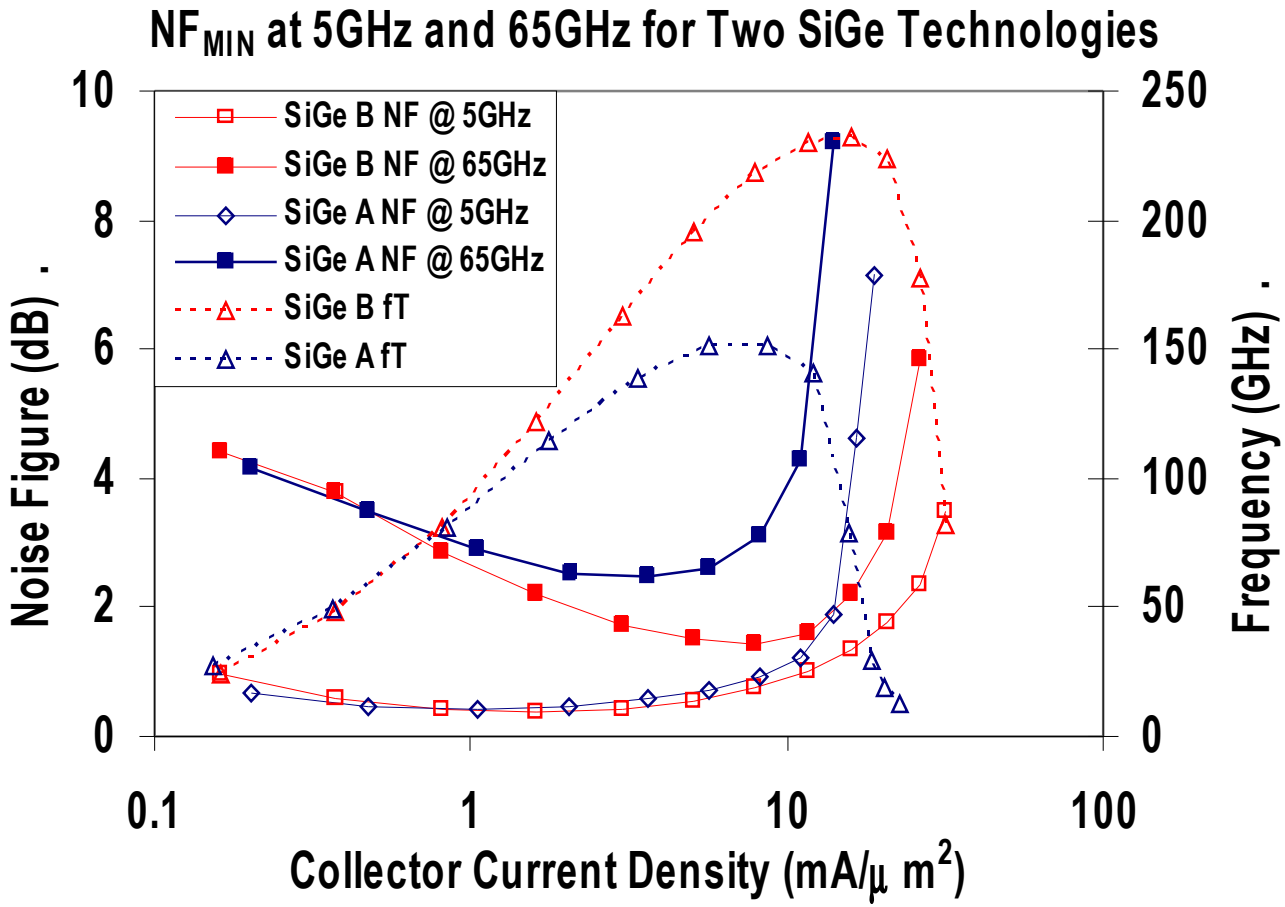
- Active device noise matching
  - Bias for minimum F_{MIN} $$\frac{\partial F_{MIN}(f, J = J_{OPT})}{\partial J} = 0$$
  - Find optimal W_f (I_E) for given frequency $$\frac{\partial F_{MIN}(W_f = W_{fopt})}{\partial W_f} = 0$$
  - size N_f or number of transistors connected in parallel for $Re\{Z_{sopt}\} = Z_0$
- Lossless feedback for input impedance matching Z_{IN} and $Im\{Z_{sopt}\}$
- Cascode with series-series inductive feedback is the preferred topology

Biasing MOSFET LNA Topology for Minimum Noise



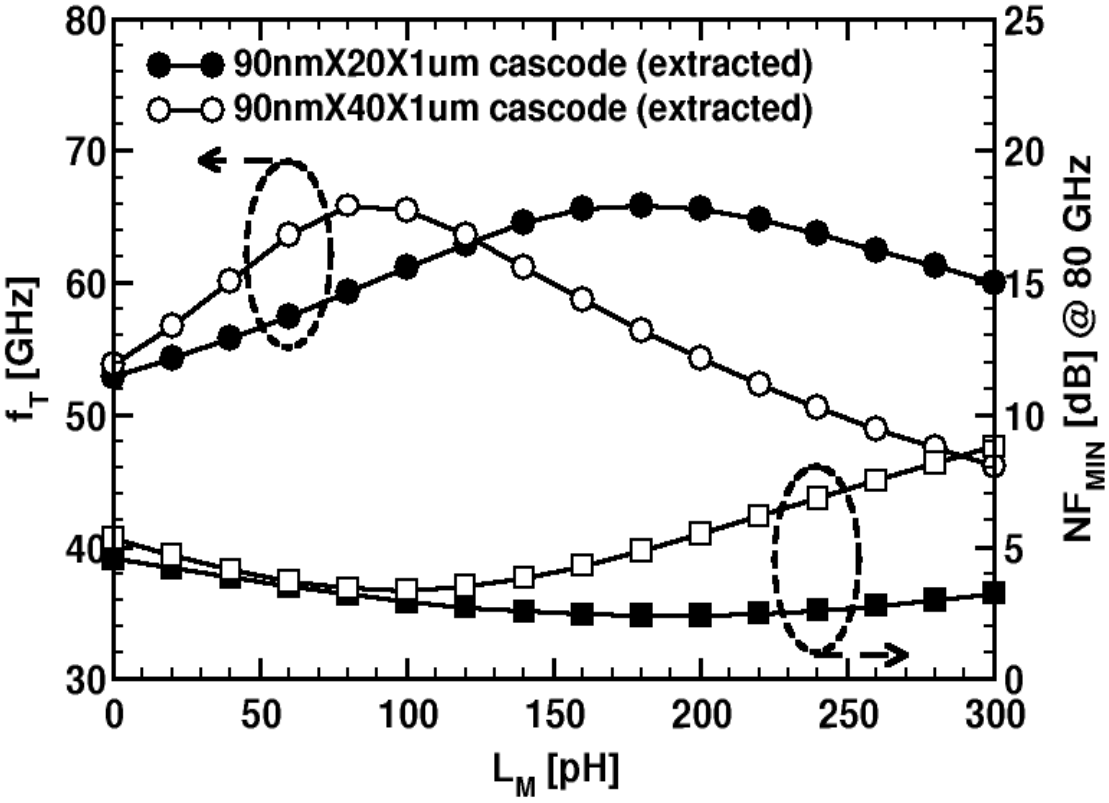
- MOSFET, cascode J_{OPT} = 0.15 mA/μm irrespective of *frequency*, W_f, and technology node

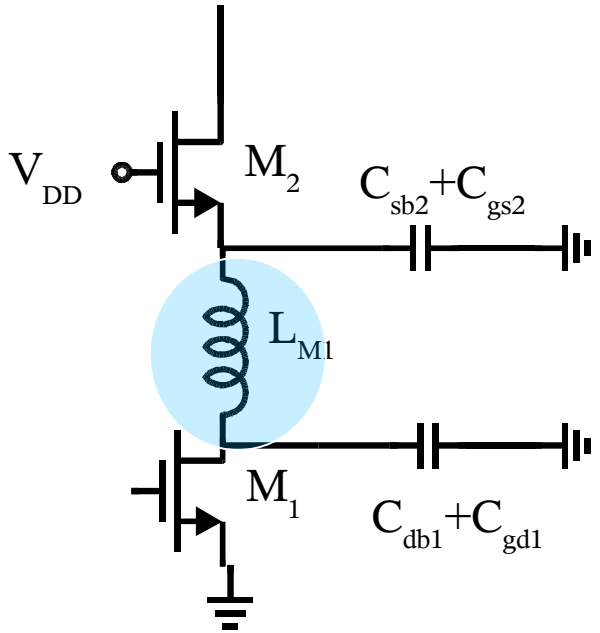
Biasing SiGe HBT LNA Topology for Minimum Noise



- J_{OPT} depends on topology, increases with frequency and in more advanced technology node

Refinements for mm-wave CMOS LNA design: f_T and NF_{MIN} of topology with L_M





L_{M1} scales as 1/W

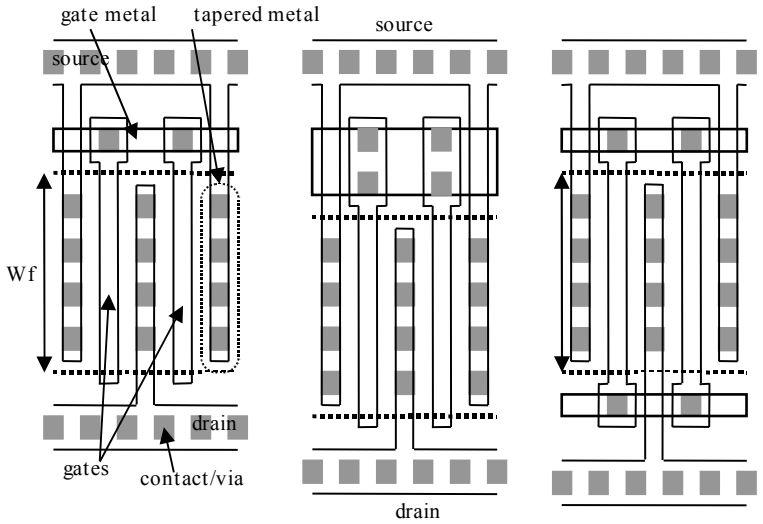
$$f_T(\text{cascode}) = \frac{g_{m1}}{2\pi(C_{gs1}+2C_{gd1})}$$

Both f_T and NF_{MIN} improve

Similar impact (15..20%) on bulk and SOI cascode

Selecting MOSFET W_f & Gate Contact Geometry

Compromise between gate parasitic capacitance and gate resistance

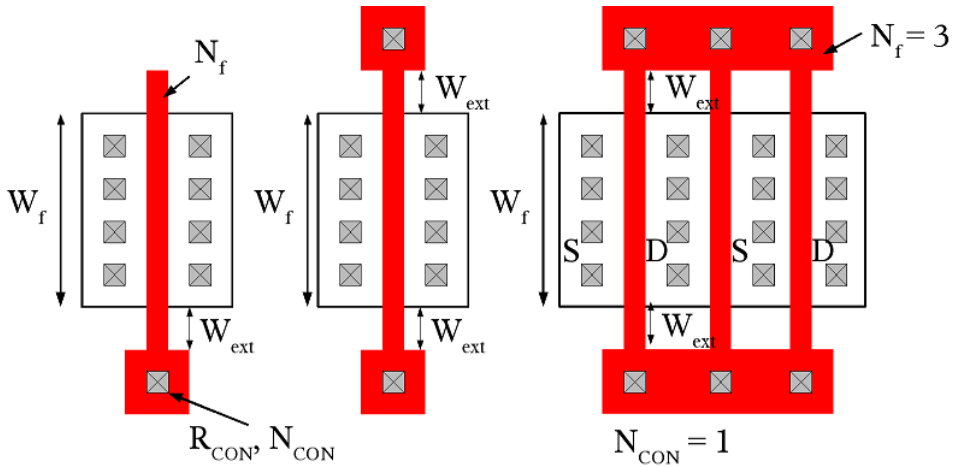


- gate contacted on one side

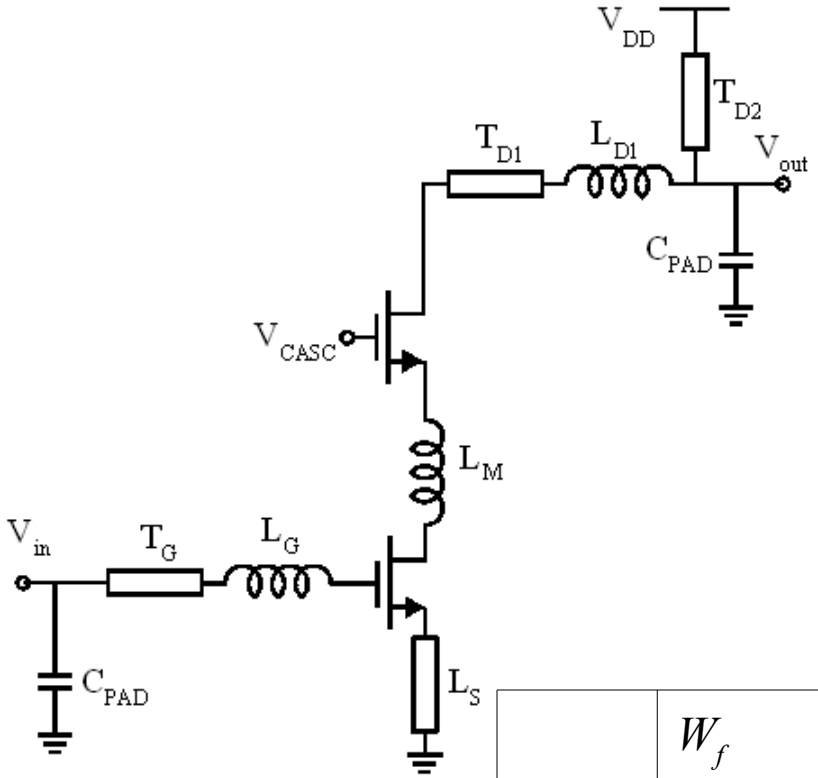
$$R_G = \frac{\frac{R_{CON}}{N_{CON}} + \frac{R_{sq}}{L}\left[W_{ext} + \frac{W_f}{3}\right]}{N_f}$$

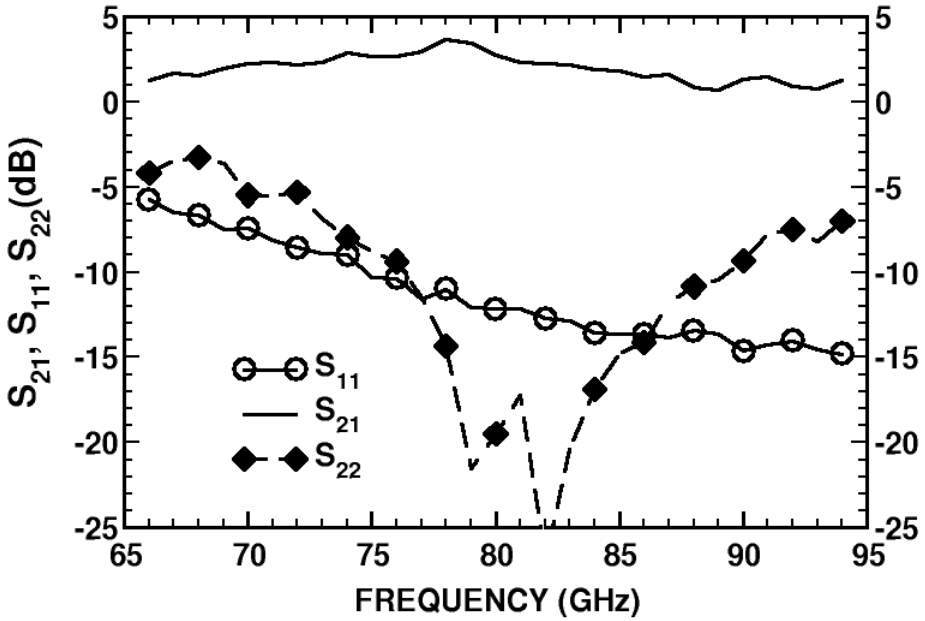
- gate contacted on both sides

$$R_G = \frac{\frac{R_{CON}}{N_{CON}} + \frac{R_{sq}}{L}\left[W_{ext} + \frac{W_f}{6}\right]}{2N_f}$$



Experiments in 90nm GP CMOS
77GHz 1-stage cascode with variable W_f gate geometry

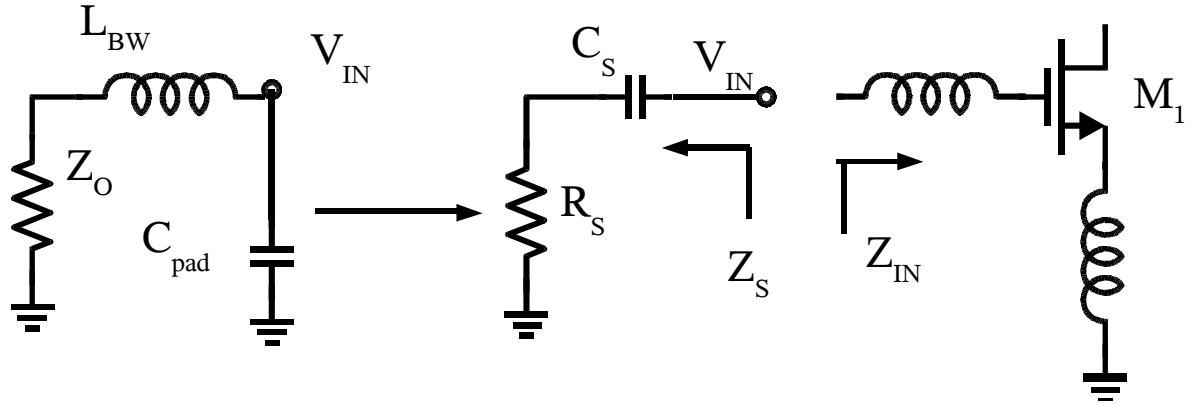




	W_f (μm)	W (μm)	*Gate Contact Ncon=1*	*S21 (dB) Sim. Meas.*	*NF (dB)*
A	1	36	single-sided	3.63 (2.1)	4.78
B	2	36	double-sided	4.36 (2.2)	4.88
C	1.5	36	single-sided	5.04 (3.7)	4.63

Refinements at mm-waves: source impedance

$$Z_{SOPT}(M_1) = R_S + j/\omega C_S$$



$$R_s = \frac{Z_0}{(1-\omega^2 L_{BW} C_{PAD}) + \omega^2 Z_0^2 C_{PAD}^2} \qquad X_s = j\omega \frac{[L_{BW}(1-\omega^2 L_{BW} C_{PAD}) - Z_0^2 C_{PAD}]}{(1-\omega^2 L_{BW} C_{PAD}) + \omega^2 Z_0^2 C_{PAD}^2}$$

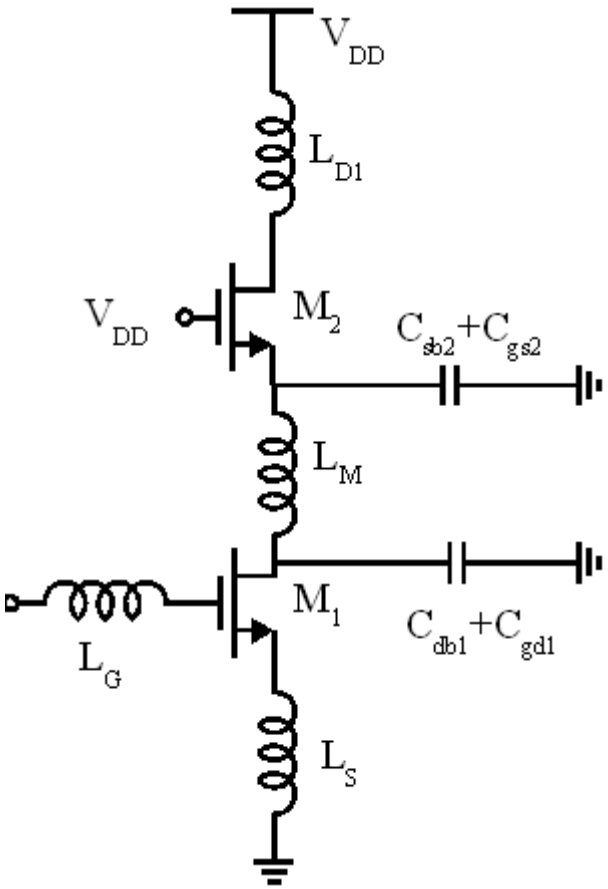
- Without bondwire

$$R_S = \frac{Z_0}{k} \qquad Z_S = \frac{Z_0}{k} - j\frac{\omega C_{PAD} Z_0^2}{k}$$

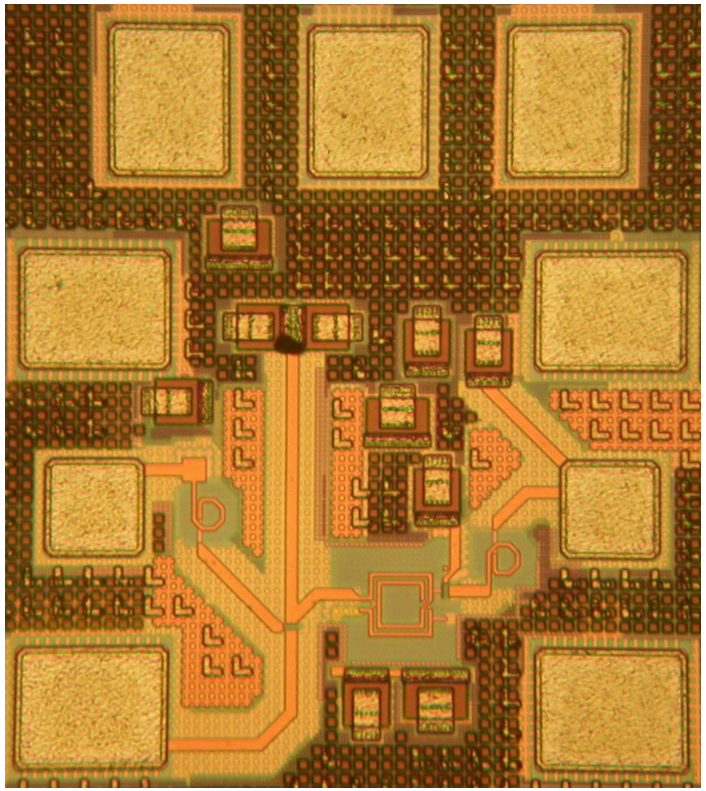
$$k = 1 + \omega^2 C_{PAD}^2 Z_0^2$$

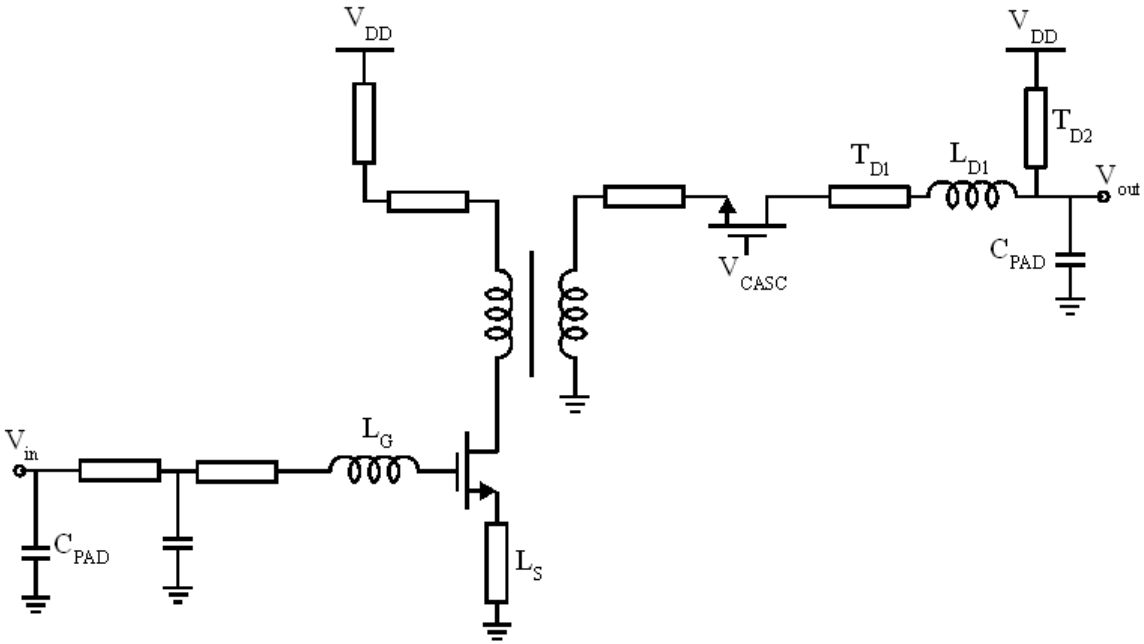
Proposed mm-Wave LNA Algorithmic Design Methodology

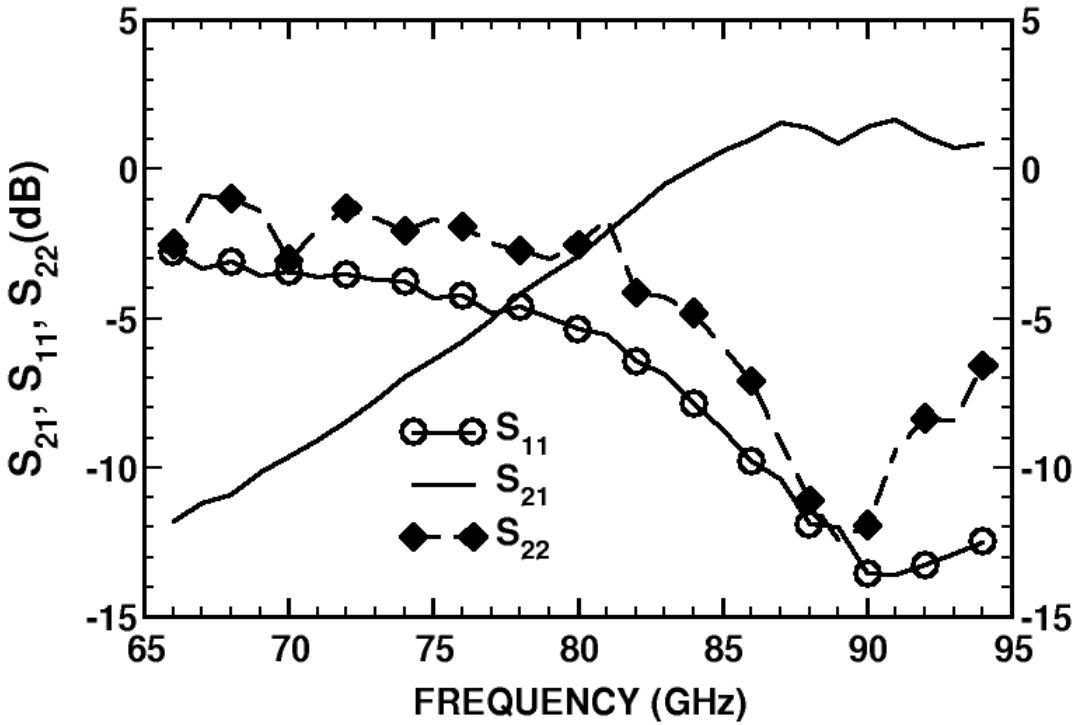
- $Z_S = R_S + jX_S$
- W_f and bias at J_{OPT}
- L_M to maximize f_T/NF_{MIN} of topology @ J_{OPT}
- Find optimal N_f such that $R_S = Re(Z_{SOPT})$ @ J_{OPT}
- Find $L_S = R_S/\omega_T$ such that $R_s = Re\{Z_{IN}\}$
- Find L_G such that $X_s = Imag\{Z_{IN}\} = Imag\{Z_{SOPT}\}$
- Output matching : L_{D1}, C_D



84-94 GHz xfmr-coupled CS-CG LNA in 90nm GP CMOS

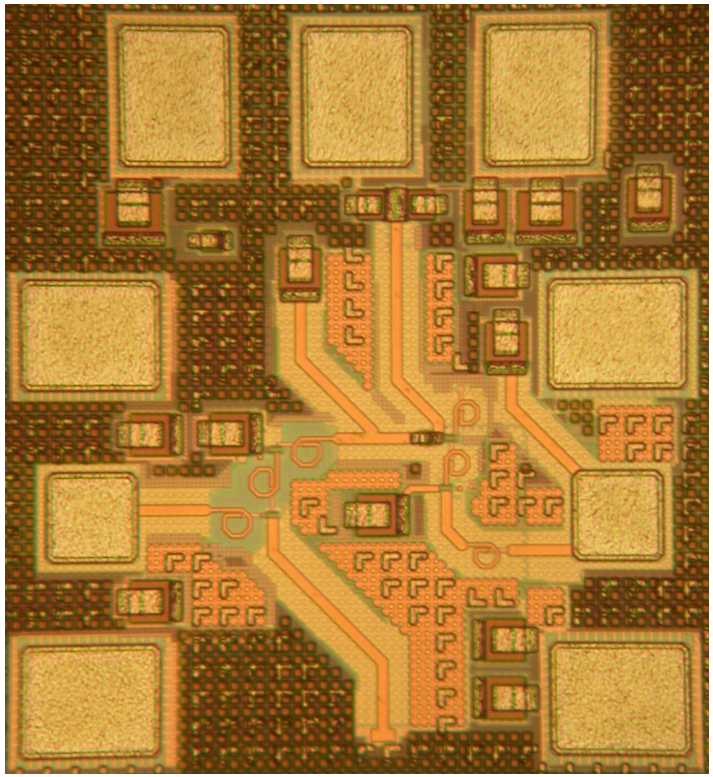


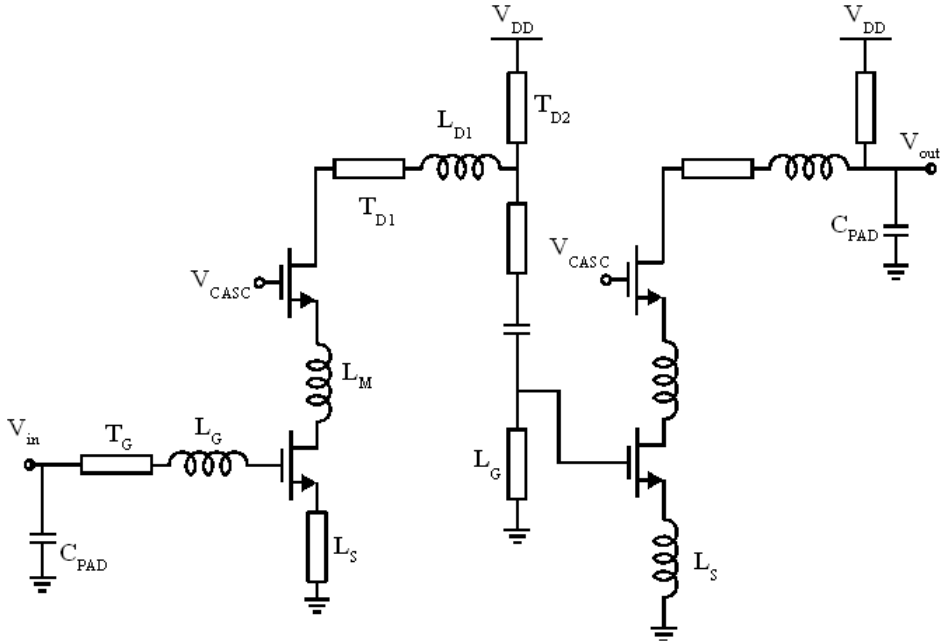


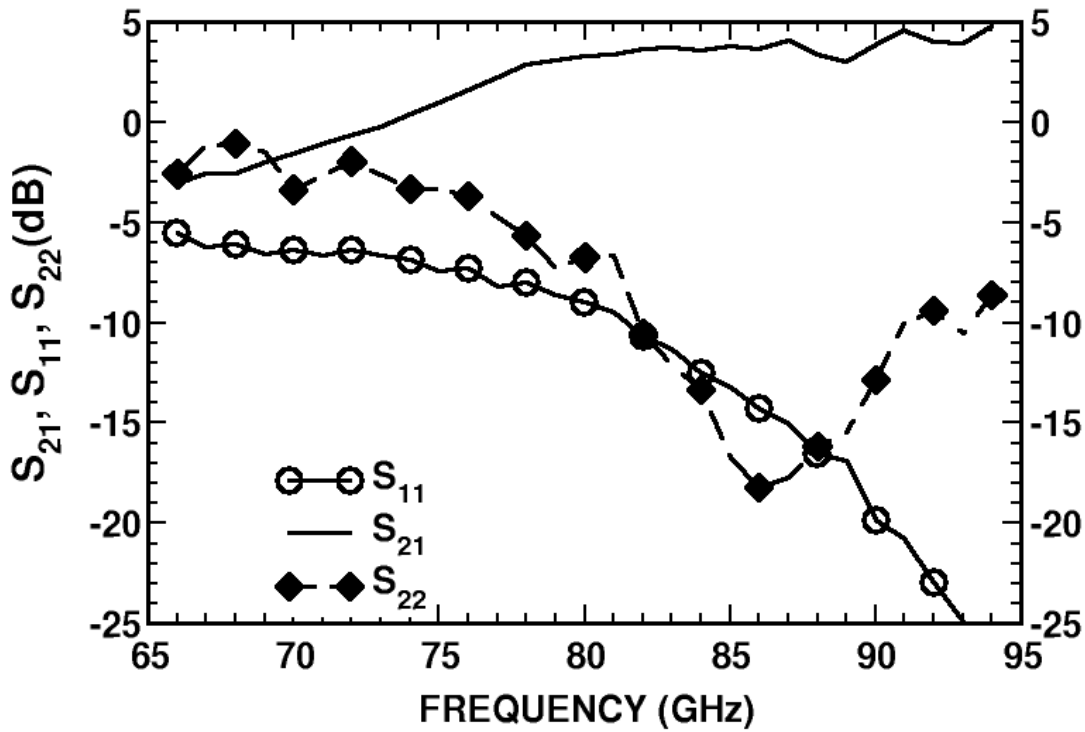


- Peak gain = 1.7 dB (91GHz)
- BW_{3dB}>10 GHz
- S_{11}, S_{22}<-10 dB, S_{12} <-30 dB
- 1.2 V supply, 23 mA
- 0.35mmx0.4mm

75-94 GHz 2-stage cascode LNA in 90nm GP CMOS

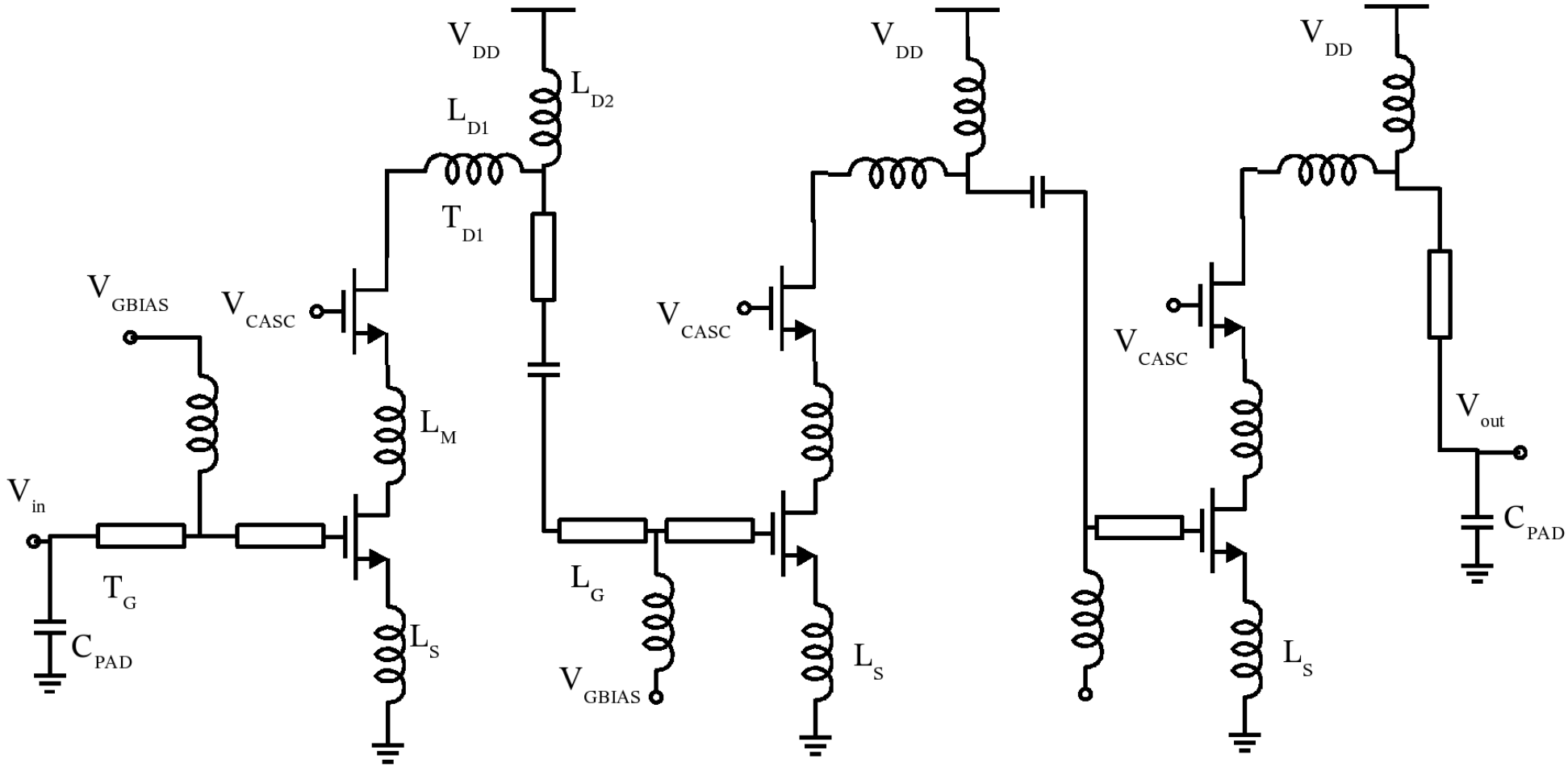




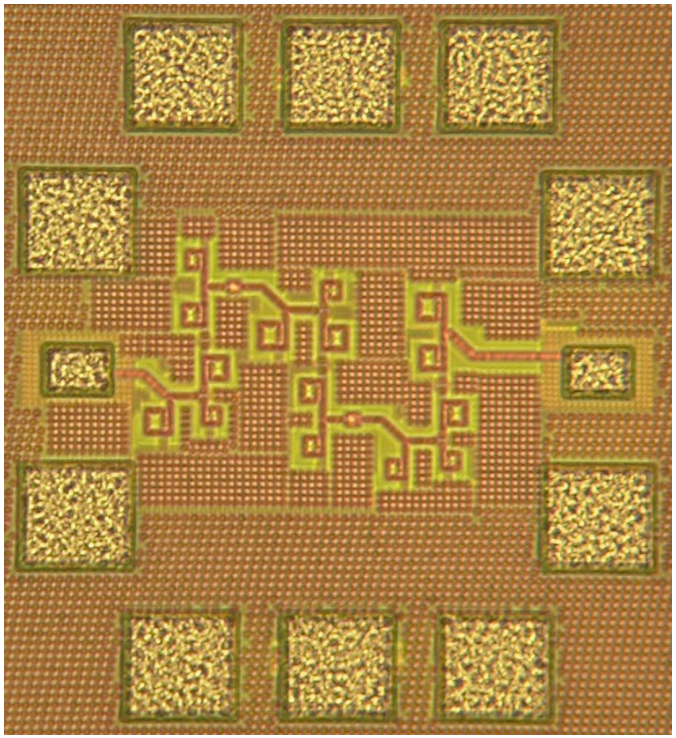


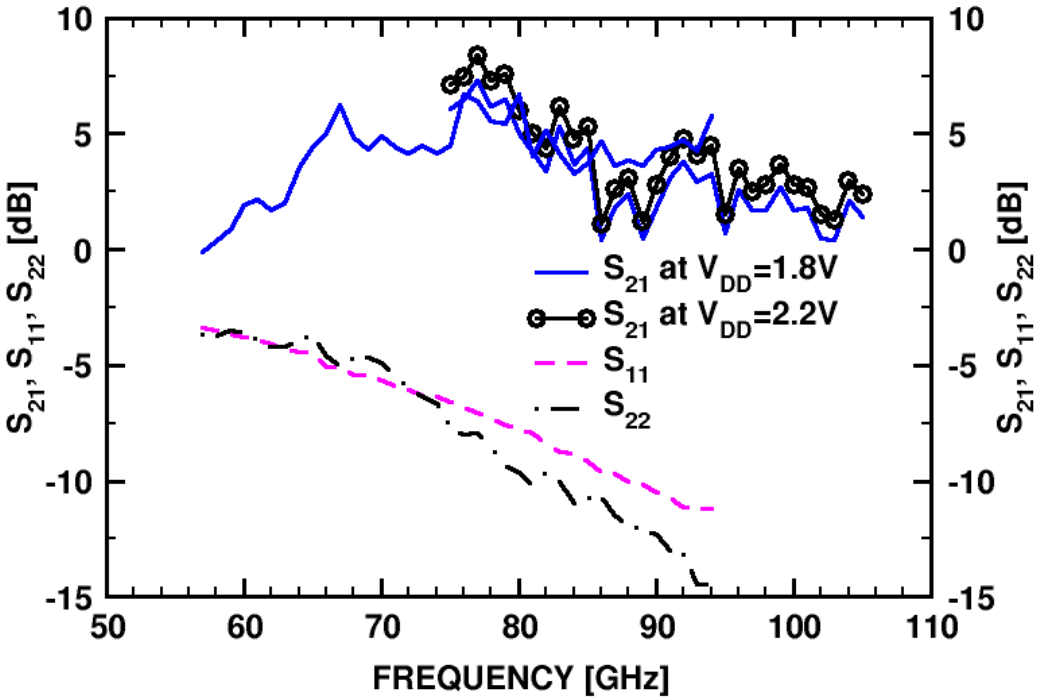
- Peak gain = 4.8 dB (94GHz)
- BW_{3dB}>20 GHz
- S_{11}, S_{22}<-10 dB, S_{12} <-30 dB
- 1.8 V supply, 16 mA
- 0.35mmx0.4mm

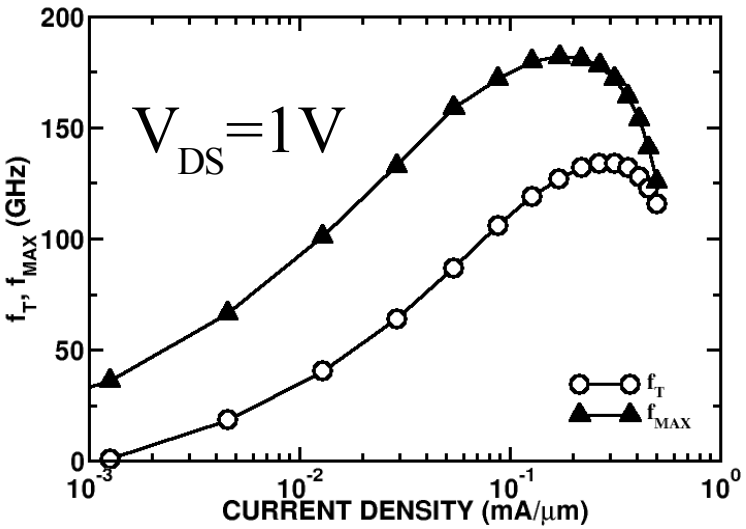
3-stage Cascode Amplifier Schematics in 65nm LP CMOS



Layout and Measured S-params







- f_T/f_{MAX} = 140/180 GHz (W_f=2μm)
- Peak gain = 8.5 dB (80 GHz)
- S_{11}, S_{22}<-8dB
- Isolation > 30 dB
- 0.4mmx0.4mm (including pads)

Conclusions

- Algorithmic LNA design methodology at mm-waves developed to account for
  - pad capacitance and bondwire inductance
  - Inductive broadbanding in MOS cascode
- First 80GHz and 94GHz CMOS amplifiers
- First transformer in CMOS at 94 GHz
- Low-VT GP 65nm CMOS technology is needed for 80-100 GHz LNAs
- At similar f_T, 80-GHz SiGe HBT LNAs have higher gain for similar power dissipation

Acknowledgments

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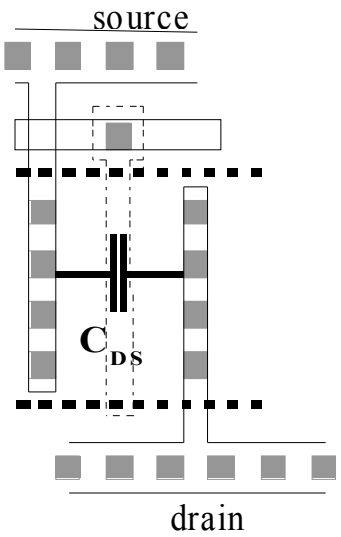
- OIT, CFI, ECTI for equipment

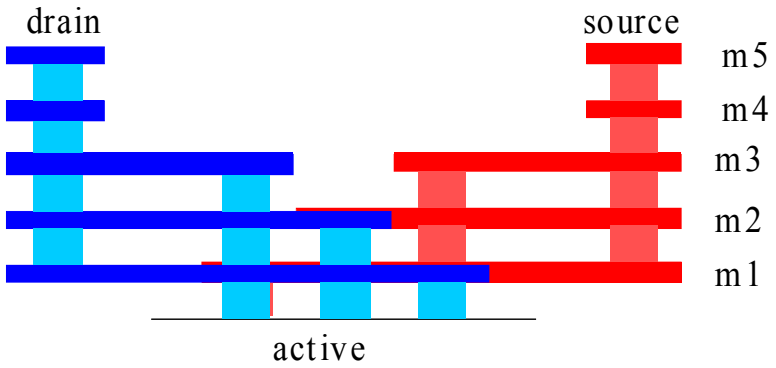
LNA Design Fundamentals

$$FoM_{LNA} = \frac{G \times IIP3 \times f}{(F-1)\times P} = \frac{OIP3 \times f}{(F-1)\times P}$$

- Device noise fundamentals:
  - $Re\{Z_{sopt}\}$ <> $Re\{Z_{IN}\}$ and $Im\{Z_{sopt}\}$ approx. $Im\{Z_{IN}\}$ (within 15%)
  - $Re\{Z_{sopt}\} = k\, f_T/(f g_m)$
  - F_{MIN} is invariant to number of gate fingers N_f, and number of transistors m connected in parallel, but depends on W_f.
- Reactive (lossless) feedback does not affect F_{MIN} and $Re\{Z_{sopt}\}$
- Power is dictated by noise impedance matching (by $V_{DD}*J_{OPT}/g'_m$)

Possible MOSFET Layouts





- gate resistance must be traded off with gate capacitance