

# CMOS SOCs at 100 GHz: System Architectures, Device Characterization, and IC Design Examples

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**Abstract**—This paper investigates the suitability of 90nm and 65nm GP and LP CMOS technology for SOC applications in the 60GHz to 100GHz range. Examples of system architectures and transceiver building blocks are provided which emphasize the need for aggressively scaled GP CMOS and low-VT transistors if CMOS is to compete with SiGe BiCMOS above 60 GHz. This requirement is in conflict with the 2005-ITRS proposal to use LP CMOS for RF applications.

## I. INTRODUCTION

Recent publications have explored the implementation of 60-94GHz LNAs, PAs and receivers in CMOS technology [1]-[5]. While reports of CMOS oscillators operating above 50 GHz are quite common, it is only in the 90nm node that their phase noise and tuning range have become competitive with those of SiGe BiCMOS VCOs [6]-[7]. The interest in CMOS for mm-wave SOCs has been kindled by the favorable impact that gate length scaling has on practically all transistor high-frequency figures of merit (FoMs), and by the hope that the expected lower wafer cost will unravel a wide range of new applications and consumer products. The latter include (i) 60GHz WPAN at 1.5 Gb/s and higher data rates, (ii) remote sensing and night vision cameras at 94 GHz, and (iii) low-exposure (i.e. low-power) short-range imaging for medical and security applications.

This paper will review the strengths and weaknesses of nanoscale CMOS technology for mm-wave SOCs, and will propose system architectures, circuit topologies, and design techniques that will facilitate their commercial deployment.

## II. SYSTEM DESIGN ISSUES

From the outset, it should be recognized that testing (even with on-chip self-test) and packaging, rather than the die, will dominate the cost of mm-wave SOCs. Given the higher product development cost in nanoscale CMOS relative to

coarser lithography SiGe BiCMOS technology with comparable or better transistor FoMs, applications and SOC architectures that demand the unique features of CMOS at mm-waves must be developed. What are those unique features? Clearly, the first is integration followed, arguably, by lower power dissipation and lower noise figure [8]. For applications where SIP is acceptable, or large output power and low  $1/f$  noise are critical, a SiGe BiCMOS solution, or a multi-chip SiGe BiCMOS and nanoscale CMOS combination remain the most economical.

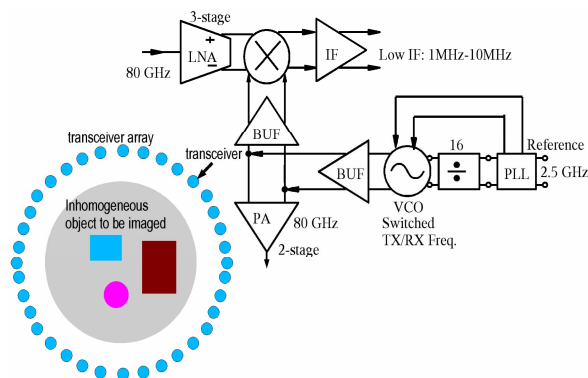


Figure 1. Pictorial view of an inverse-scattering-based imager system and transceiver block diagram with switched TX/RX frequency VCO.

Fig. 1 illustrates a possible mm-wave transceiver block diagram suitable for single-chip radio, automotive radar, and imaging applications. Using lumped inductors and transformers as tuning and matching elements, such a system can be realized in a silicon area smaller than  $2 \text{ mm}^2$  [4],[9]. It thus becomes feasible to integrate arrays of mm-wave transceivers and a large digital DSP core on a single die. Transceiver and receiver arrays are needed in imagers based on inverse scattering (Fig.1), and for remote sensing, respectively. To be practical, these SOCs must first overcome the cross-talk between adjacent transceivers, the leakage from

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the transmitter to the receiver, large  $1/f$  noise at sub-MHz offsets from the carrier, and increasing power dissipation, particularly in the VCO and PLL blocks. In the absence of adequate CMOS switches, and given the poor gain, isolation, and large area of antennas even at 100 GHz, a low-IF system architecture can be a viable solution. The VCO can be shared and its frequency is switched by a few MHz between transmit and receive modes. The antennas are best integrated in the package. To contain the power dissipation at acceptable levels, all mm-wave CMOS building blocks must be capable of operating from 1.2-1.5V supplies. The next section examines the adequacy of the general purpose (GP) and low power (LP) 90nm and 65nm CMOS technologies, and circuit topologies, to meet the low power dissipation challenge without compromising the high frequency FoMs.

### III. DEVICE AND CIRCUIT TOPOLOGY PERFORMANCE

The measured transconductance in the linear and saturation regions of n-MOSFETs fabricated in 90nm GP CMOS is plotted in Fig. 2a as a function of the inverse of the gate length. In both regions, the transconductance continues to increase as gate length decreases, clearly indicating that velocity saturation is not dominant. Fig. 2b confirms that even 65nm LP devices are not fully velocity-saturated. However, as a result of the thicker gate oxide and larger source/drain resistance, 65nm LP n-MOSFETs exhibit lower transconductance than 90nm GP devices at comparable physical gate length. A common misconception is that the “saturation” of the  $f_T$ - $V_{GS}$  characteristics of nanoscale n-MOSFETs seen in Fig. 3a is due to velocity saturation. In fact, it is primarily caused by vertical field mobility degradation [10]. Fig. 3b reveals that the peak  $f_T$  current density is independent of  $V_T$  and of the technology node. Most importantly, low-VT devices exhibit a wider range of gate voltages over which  $f_T$  and  $f_{MAX}$  remain practically constant, making them more robust to  $V_{GS}$  and power supply variation. Note also that in the GP process the high-VT device has a lower threshold voltage than the low-VT MOSFET in the LP process. As a consequence, and unintentionally, because of the comparable  $f_T$ , circuits fabricated in GP 90nm technology are expected to require a lower supply voltage and to dissipate less power than their 65nm LP versions operating in the same frequency range.

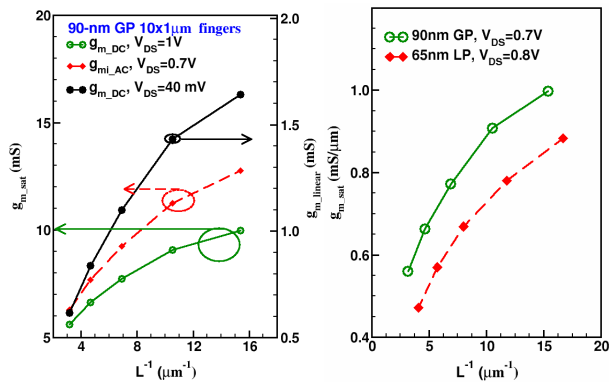


Figure 2. Measured transconductance in the triode and saturation regions vs. the inverse of the gate length for n-channel MOSFETs fabricated in 90nm GP and 65nm LP CMOS technologies.

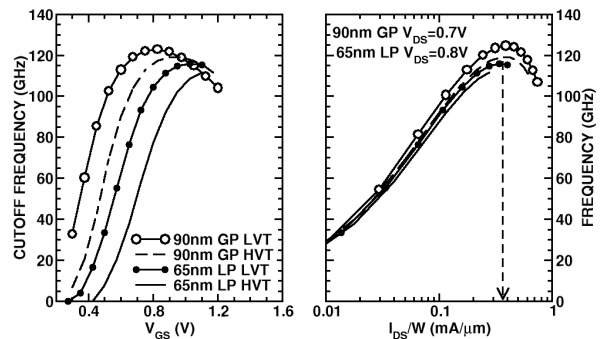


Figure 3. Measured  $f_T$  plotted vs. (a) gate voltage and (b) drain current density for 90nm GP and 65nm LP n-MOSFETs with 80 gate fingers, each with  $1\mu\text{m}$  finger width, and different threshold voltages.

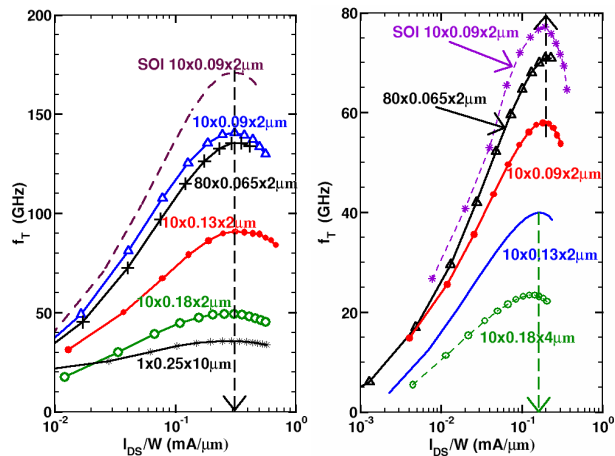


Figure 4. Measured  $f_T$  vs. drain current density for a) n-MOSFETs and b) p-MOSFETs fabricated in different bulk and SOI technology nodes.

When plotted vs. drain current density as in Fig. 4, GP MOSFETs from different foundries [10] exhibit remarkably similar high-frequency characteristics which scale almost ideally from one technology node to another [10]. Based on these measurements, one can conclude that biasing and sizing MOSFETs for linearity [3] or for low-noise mm-wave performance, remains largely unchanged across technology nodes [11]. Measured transistor (Fig. 4) and cascode (Fig. 5) data reveal that, despite improvement in the speed of the p-MOSFET due to strain, there is no increase in  $f_T$  between 90nm GP and 65nm LP n-MOSFETs. Finally, measurements shown in Fig. 5b confirm that the 65nm LP CMOS inverter is a viable topology for mm-wave circuits. While requiring similar supply voltage as the cascode, it features higher  $g_m/I_D$ , higher  $S_{21}$ , and comparable  $f_T$ .

Unlike their GHz-range analog and RF counterparts, mm-wave circuits and CML logic call for aggressively scaled GP devices with thin oxides and short gate length in order to achieve low noise, high gain, and fast switching. Because of the low input impedance of the MOSFET above 50 GHz, gate and subthreshold leakage pose little threat to circuits operating in this frequency range. Unfortunately but understandably, the 2005 ITRS has chosen LP rather than GP transistors for RF-CMOS processes [12].

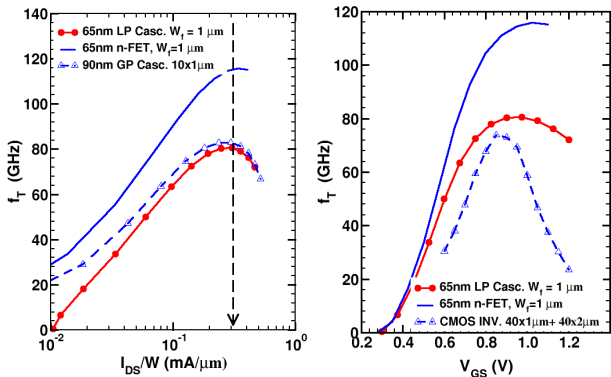


Figure 5. Measured  $f_T$  vs. drain current density for n-MOSFETs, cascodes and CMOS inverter fabricated in 90nm GP and 65nm LP CMOS technology. The  $V_{DD}$  of the CMOS inverter and cascode is 1.8V.

#### IV. CIRCUIT DESIGN EXAMPLES

##### A. 60GHz transceiver chipset in 90nm CMOS

A 60GHz WLAN chipset consisting of (i) a receiver with a 2-stage cascode LNA, double-balanced Gilbert cell mixer, LO buffer and IF amplifier [4], (ii) an upconverter featuring an LO buffer and a double-balanced mixer (Fig. 6), (iii) 3-stage common-source power amplifier [3], and (iv) a 55GHz VCO with 10% tuning range were implemented in a 90nm GP CMOS process using low-VT transistors, lumped inductors and transformers in a standard (except for the PA) back-end.

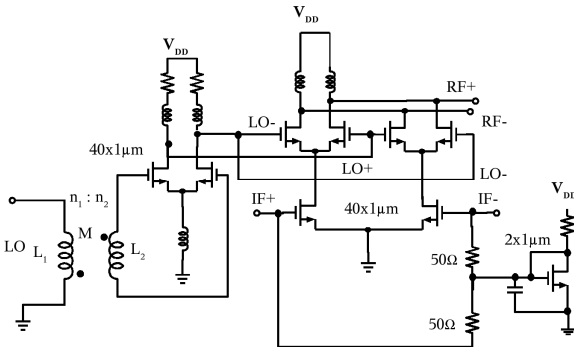


Figure 6. 60-GHz upconverter schematics.

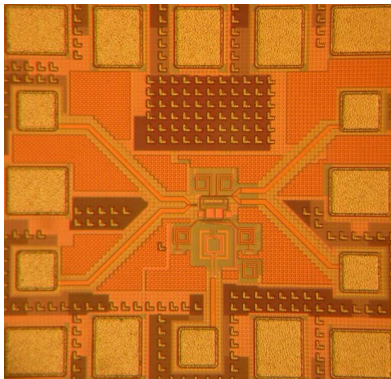


Figure 7. Die photo of 60GHz 90nm GP CMOS upconverter. LO port is at the bottom, IF on the left and RF output at the right.

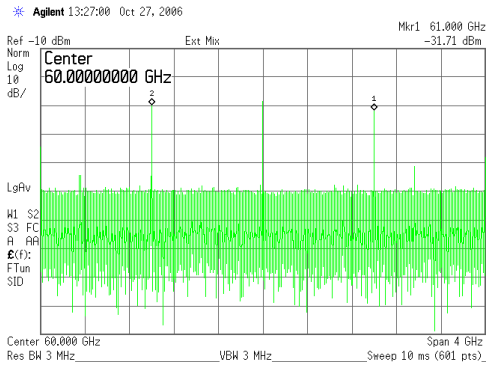


Figure 8. Measured 60GHz upconverter RF spectrum with 1GHz IF input. Setup and cable losses have not been de-embedded.

The receiver consumes 60 mW from 1.2V supply and has 15dB gain and a DSB noise figure of 5.5 dB [4]. The 600 $\mu$ m $\times$ 600 $\mu$ m die photo and the measured spectrum at the upconverter output are reproduced in Figs. 7 and 8, respectively. The upconverter gain varies between -4 and -7 dB for IF frequencies between 1 GHz and 5 GHz, and consumes 70 mW from a 1.5V supply. A 3-stage CS PA with a saturated output power of +9 dBm and a PAE of 7% was also demonstrated in a 90nm GP RF-CMOS process with thick copper top metal layer [3].

##### B. 80GHz VCOs

Colpitts VCOs centered at 77 GHz [7] and 83 GHz (Fig. 9) were also fabricated in 90nm GP CMOS. A record phase noise of -100.2 dBc/Hz was measured at 1MHz offset from the 79GHz carrier, as needed in imaging and automotive cruise control applications. Fig. 10 reproduces the measured tuning characteristics of the two VCOs which span 6 GHz and 5 GHz, respectively. The differential output power is in the -18dBm to -15dBm range, while the typical power consumption in the core is 30 mW from a 1.5V supply.

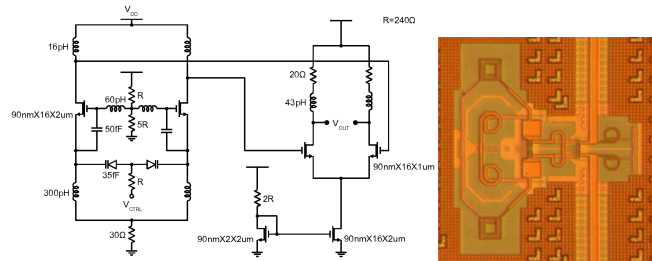


Figure 9. a) Schematics of 83GHz Colpitts VCO with output buffer and b) die photo detail showing tank and output buffer inductors.

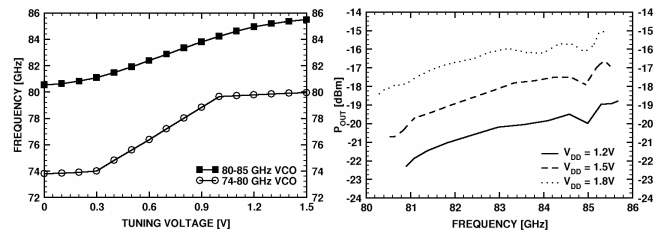


Figure 10. a) Measured 77GHz and 83GHz VCO tuning characteristics and b) output power vs. supply voltage variation for 83GHz VCO.

### C. 80-100 GHz amplifiers

A two-stage cascode amplifier with 4.8dB gain at 94 GHz was implemented in 90nm GP CMOS [5]. For comparison, Figs 11 and 12 show the schematics and die photo, respectively, of a 3-stage cascode amplifier, with 15 lumped inductors, which was fabricated in 65nm LP CMOS. Its measured and simulated S parameters, shown in Fig. 13, demonstrate a peak gain of 9 dB at 80 GHz when the amplifier is biased from a 2.2V supply. The large  $V_{DD}$  is imposed by the fact that the low-VT, 65nm LP n-MOSFET requires a  $V_{GS}$  of 0.9 V (similar to the  $V_{BE}$  of a SiGe HBT) at peak  $f_T$ . In contrast, the low-VT, GP 90nm LNAs can be powered from a 1.2V supply at 60 GHz [4] and from a 1.8V supply at 94 GHz [5].

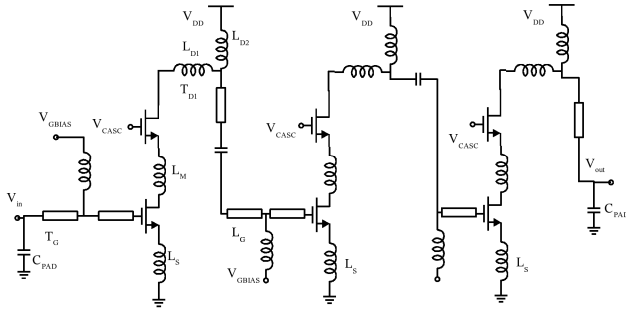


Figure 11. 80-GHz 3-stage amplifier schematics in 65nm LP CMOS.

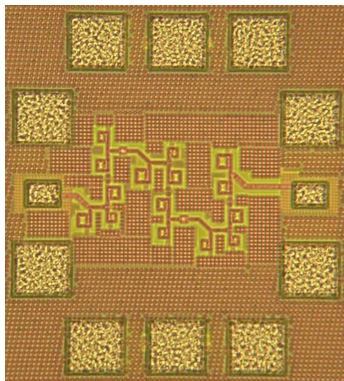


Figure 12. 80GHz 3-stage cascode amplifier die photo ( 0.4mmx0.4mm).

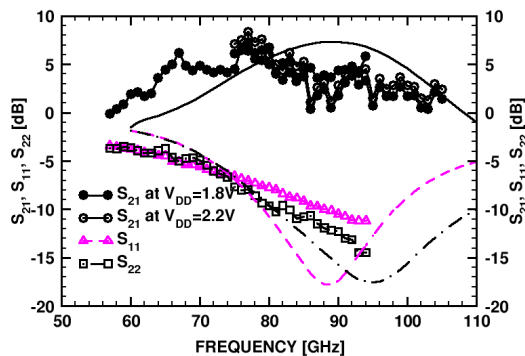


Figure 13. Measured (symbols) vs. simulated (lines) S parameters of 65nm LP 3-stage cascode amplifier.

### V. CONCLUSIONS

Nanoscale CMOS technology shows promise for mm-wave SOCs at 60 GHz, especially in low-noise/low-power receiver arrays. However, early mm-wave measurements of GP 90nm and LP 65nm MOSFETs, cascodes, CMOS inverters, and 80-100 GHz amplifiers provide an indication that the 2005 ITRS decision to select LP CMOS for RF applications is not beneficial for achieving large  $f_T$ ,  $f_{MAX}$  and low noise figure, as needed in 80-100 GHz ICs. On the contrary, if CMOS is to compete with SiGe BiCMOS technology for low-power, high performance, 100GHz SOCs, aggressively scaled GP technology, at the 65nm node and beyond, must be coupled with a thick metal back-end.

### ACKNOWLEDGMENT

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