CMOS SOCs at 100 GHz: System Architectures, Device Characterization, and IC Design Examples

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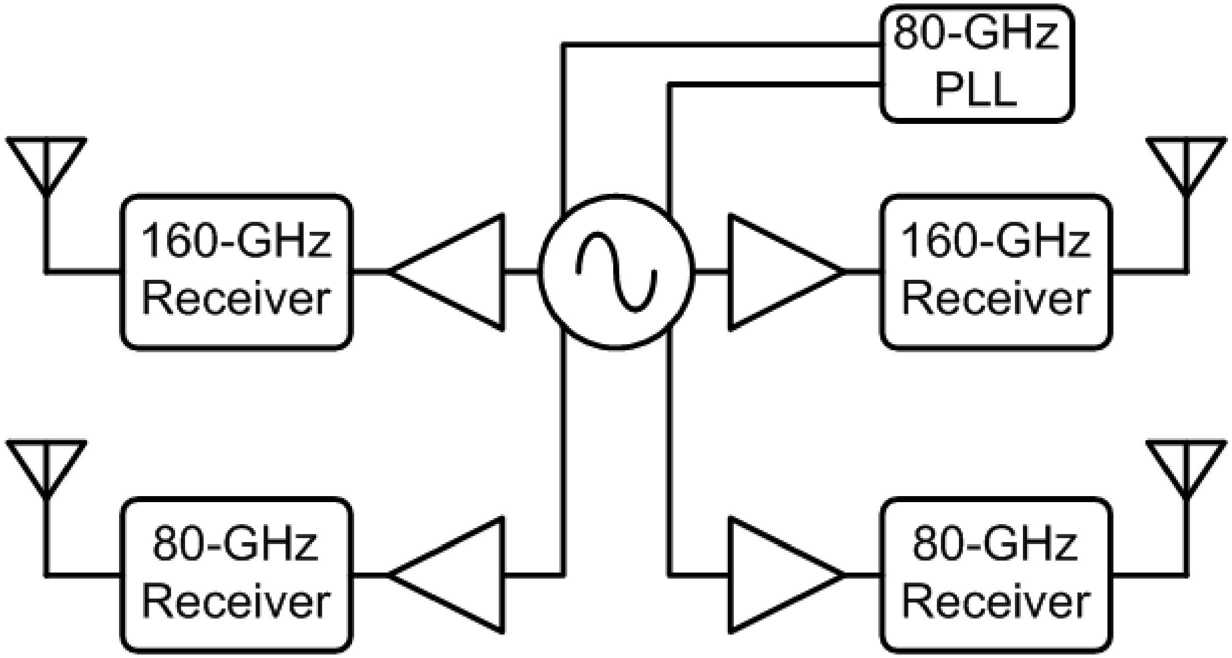
Outline

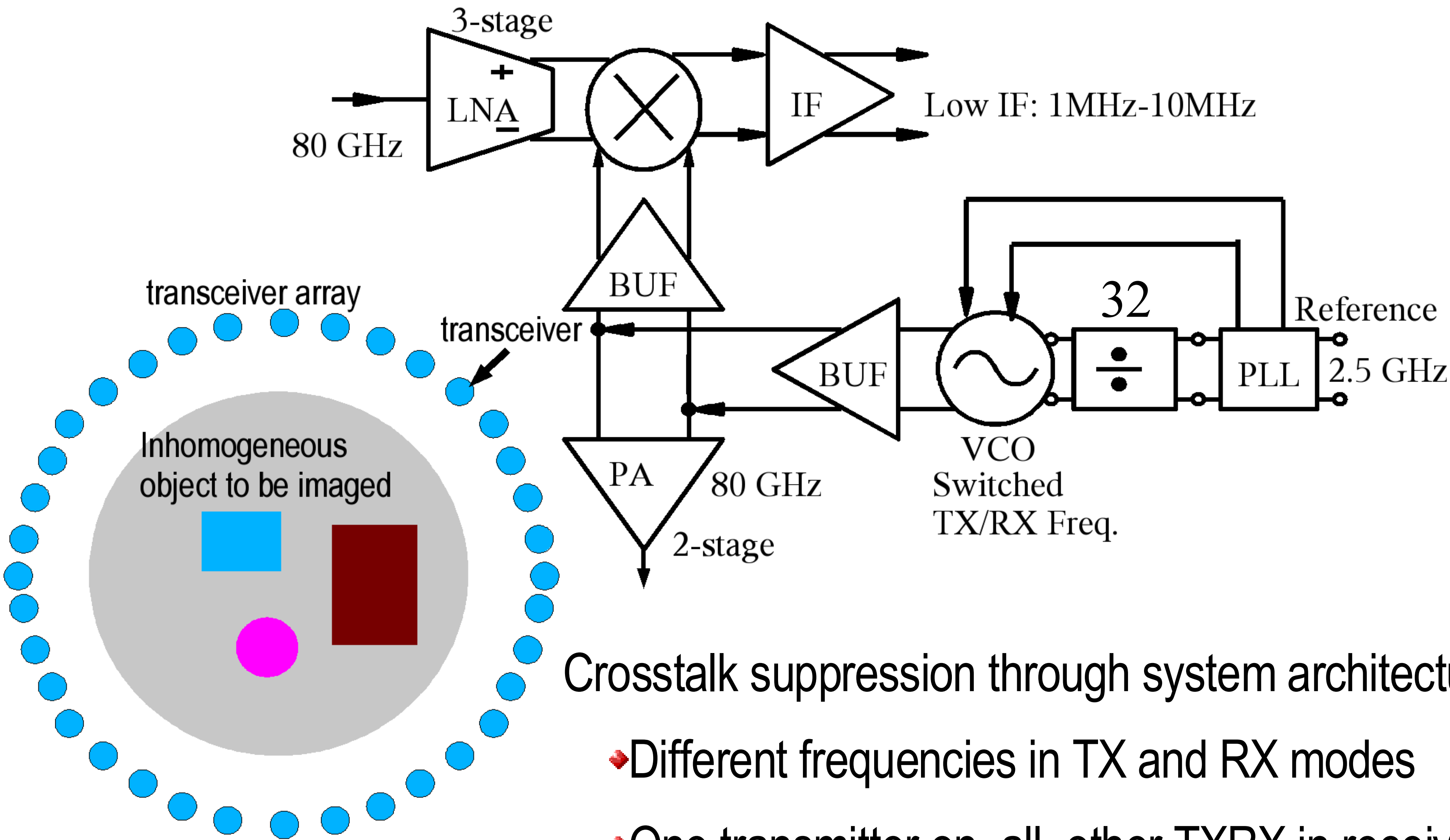
- Why?
- Measured 65nm MOSFETs: are they really that bad (for analog/RF)?
- 60-100 GHz circuits in 90nm and 65nm CMOS
- Summary

Remote sensing (passive imaging)
(E. Laskin et al. RFIC-2007)



- Multiphase/multi-frequency clock distribution
  - Quad signals @ 80 GHz. differential at 160 GHz.
- Save power by sharing PLL among

80GHz inverse scattering active imager



Crosstalk suppression through system architecture

- Different frequencies in TX and RX modes
- One transmitter on, all other TXRX in receive mode

Need very low power for array integration

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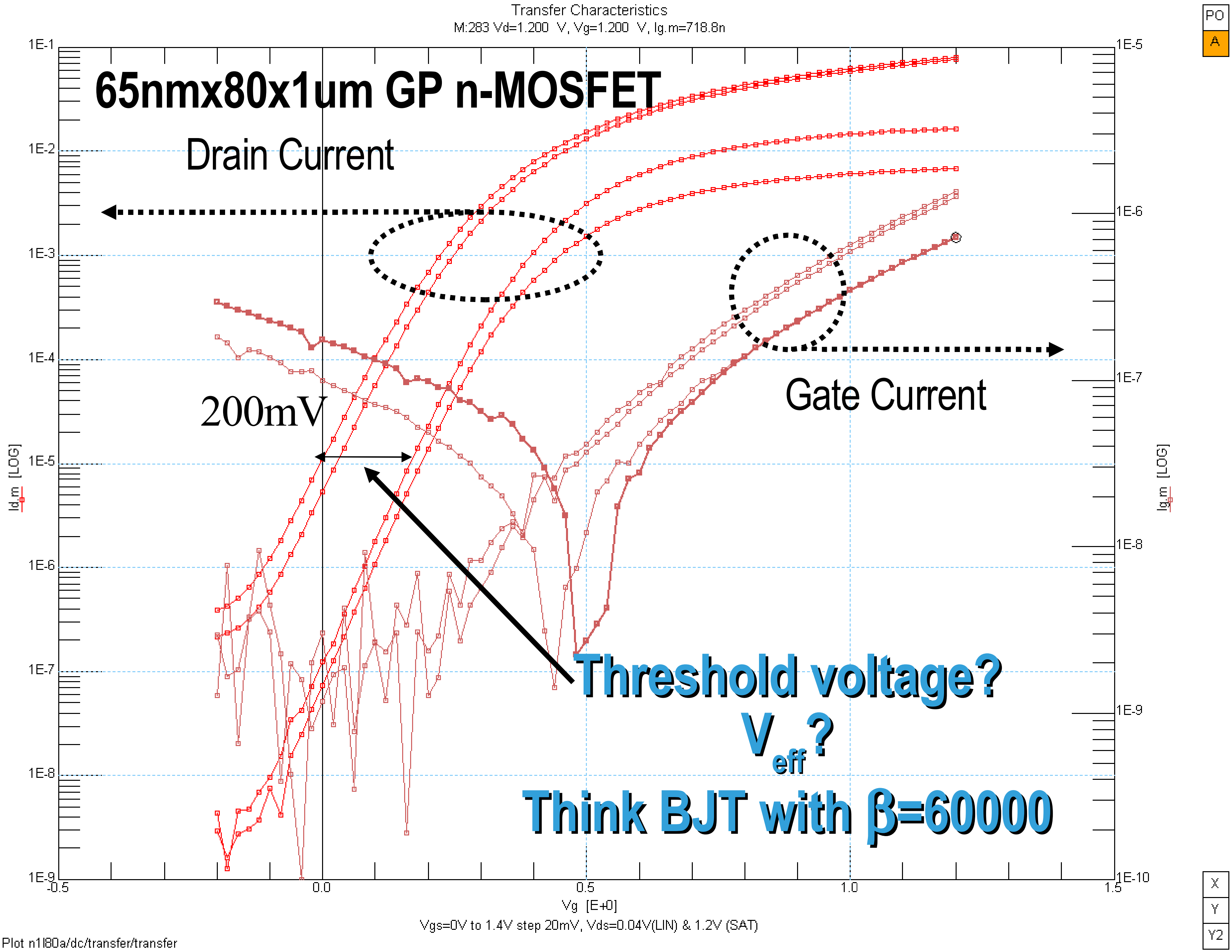
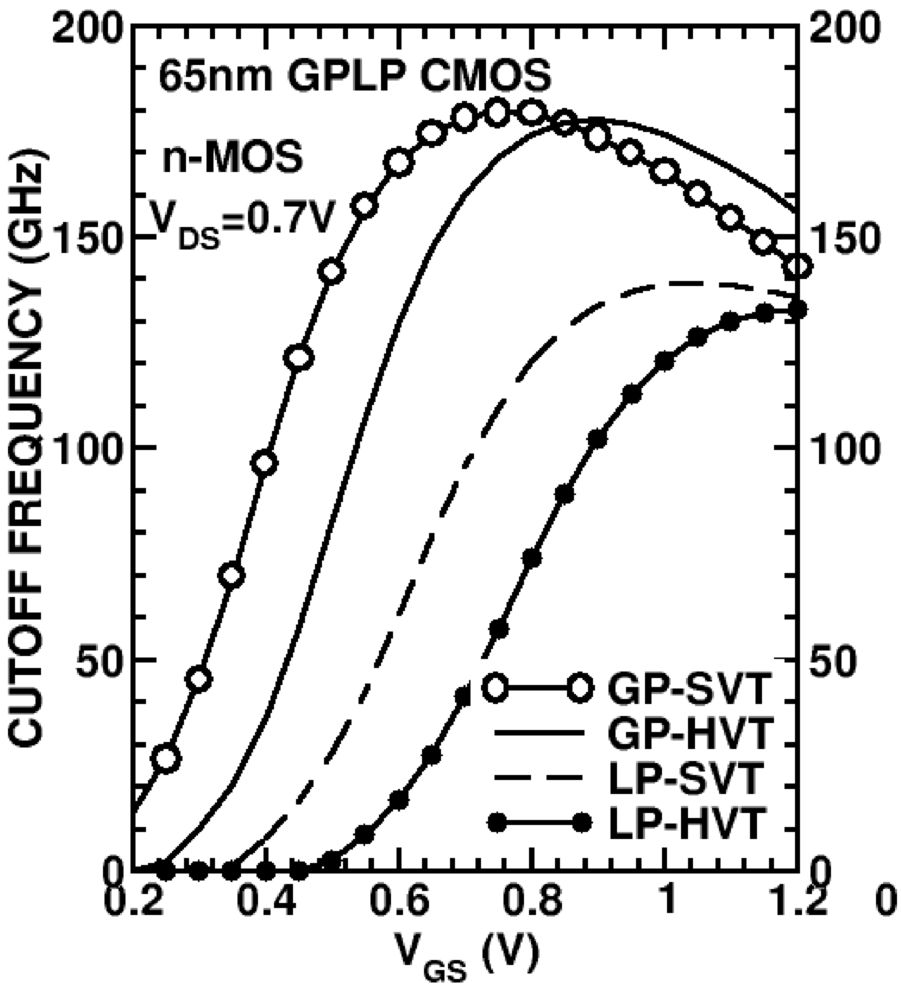
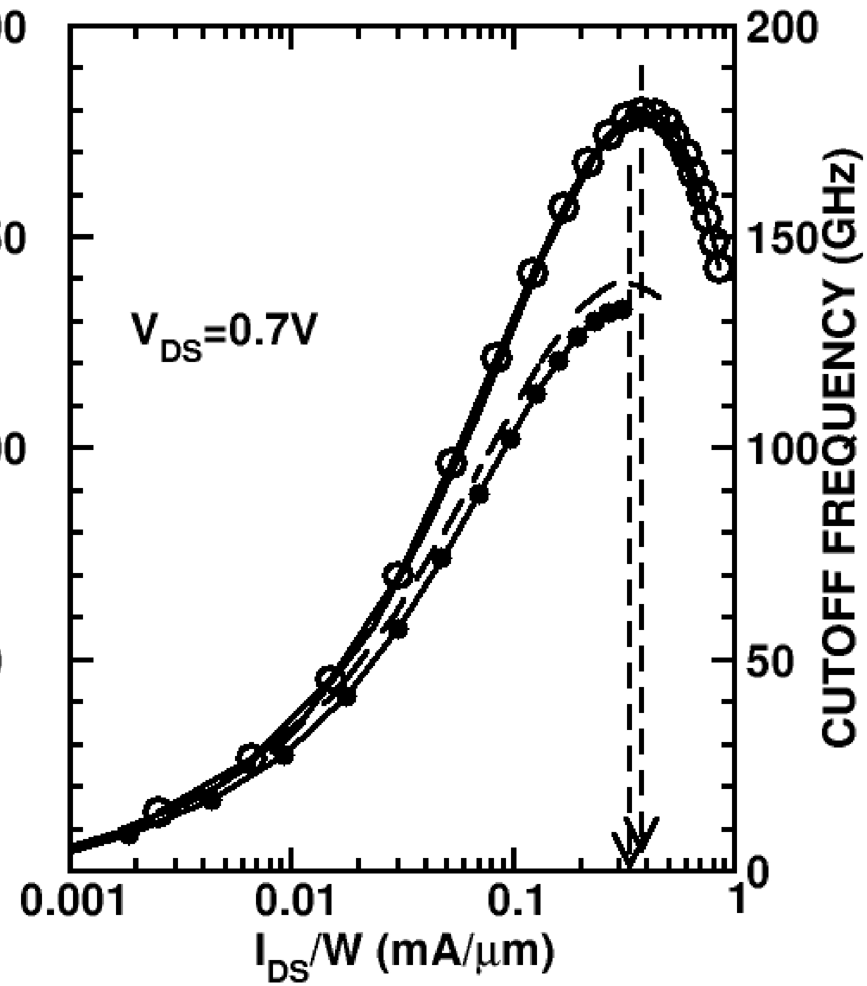


Transfer Characteristics
M:283 Vd=1.200 V, Vg=1.200 V, Ig.m=718.8n
65nmx80x1um GP n-MOSFET
Drain Current
Gate Current
200mV
Threshold voltage?
V_{eff}?
Think BJT with β=60000
Id.m [LOG]
Ig.m [LOG]
Vg [E+0]
Vgs=0V to 1.4V step 20mV, Vds=0.04V(LIN) & 1.2V (SAT)
Plot n1l80a/dc/transfer/transfer

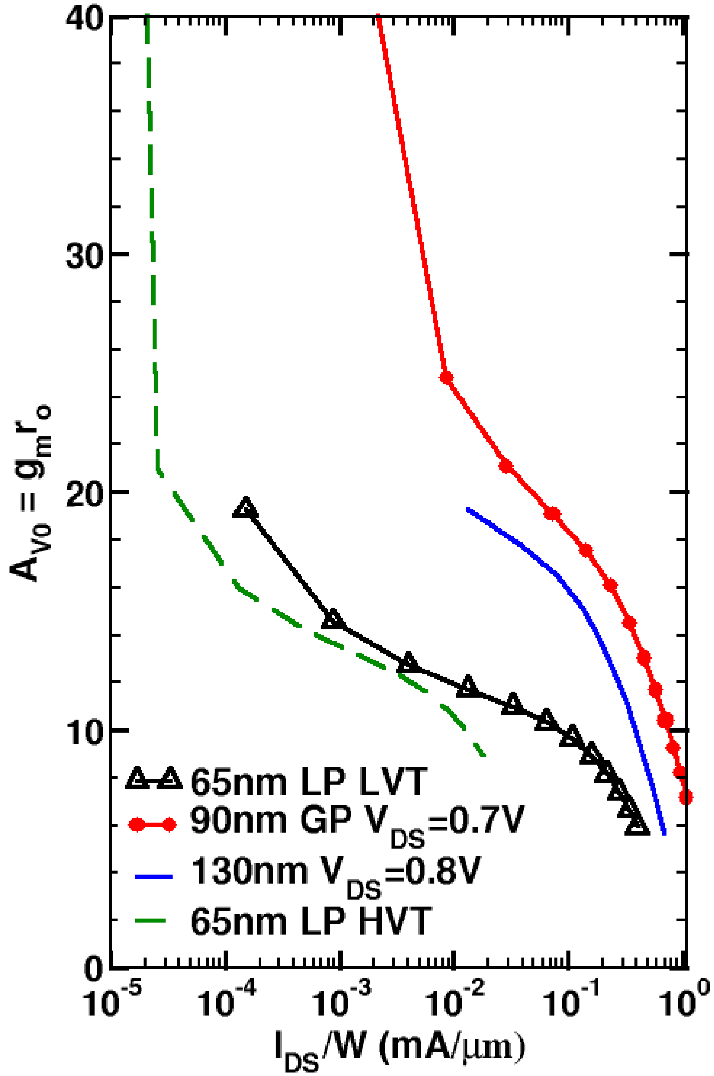
GP and LP 65nm CMOS

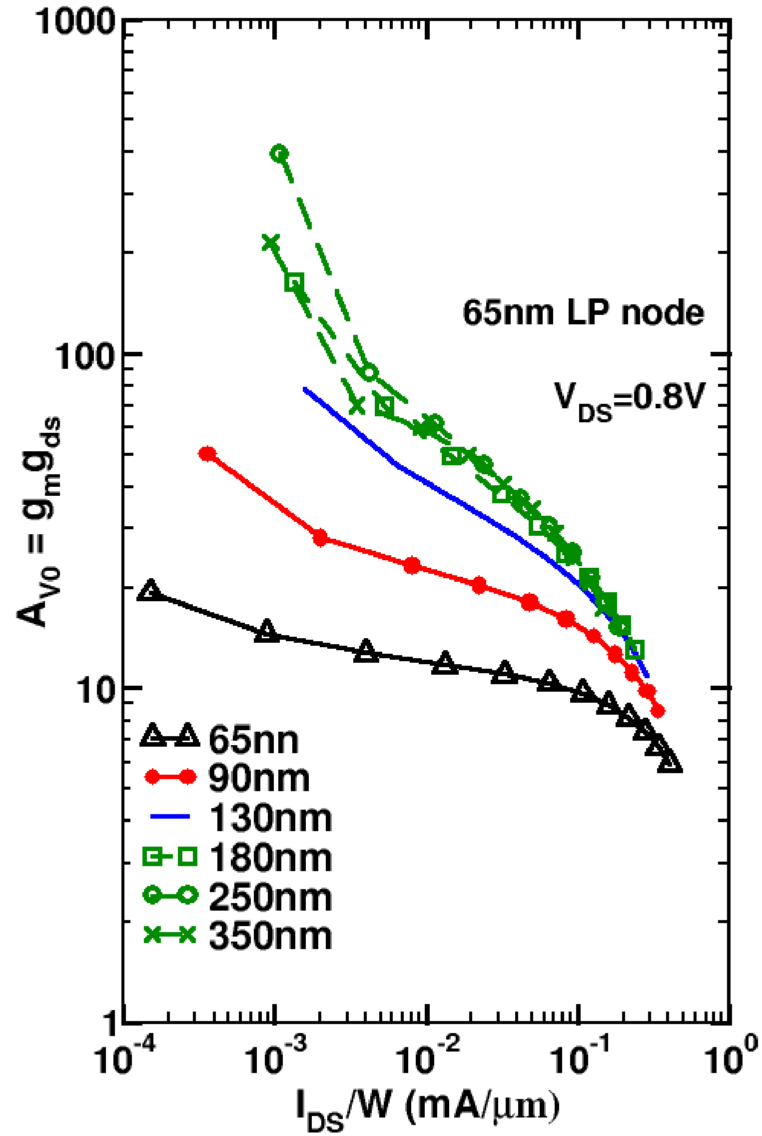




- GP 30% faster than LP and 300mV lower V_{GS} => lower power!
- Constant-current-density bias at 0.3-0.4mA/µm => robust to I_{DS} variation
- VT variation is large but mostly irrelevant

MOSFET DC gain scaling: think current density!





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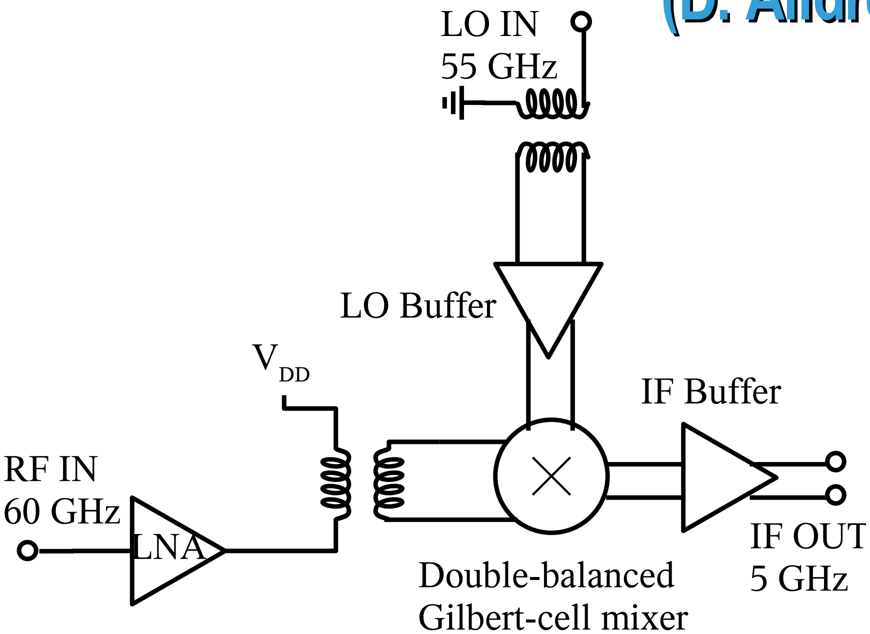
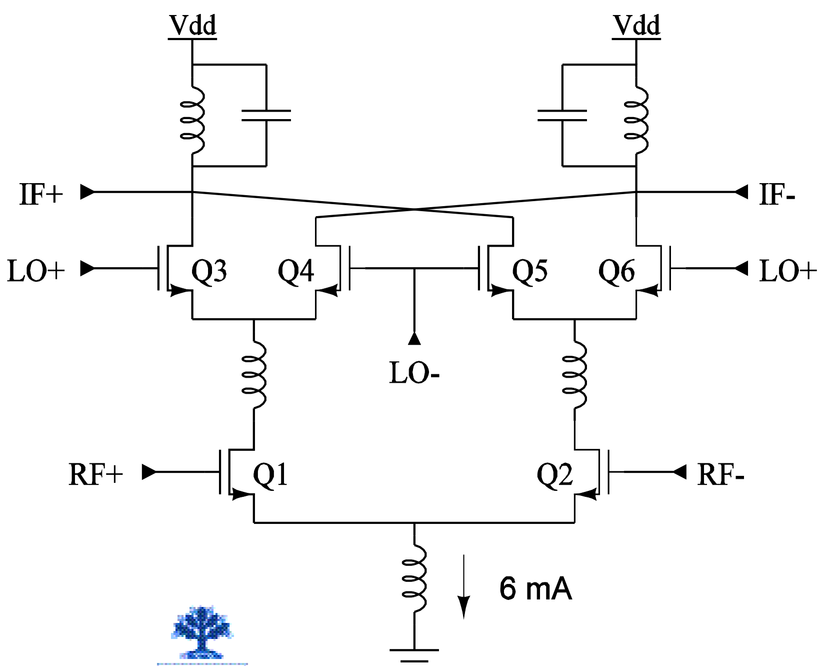
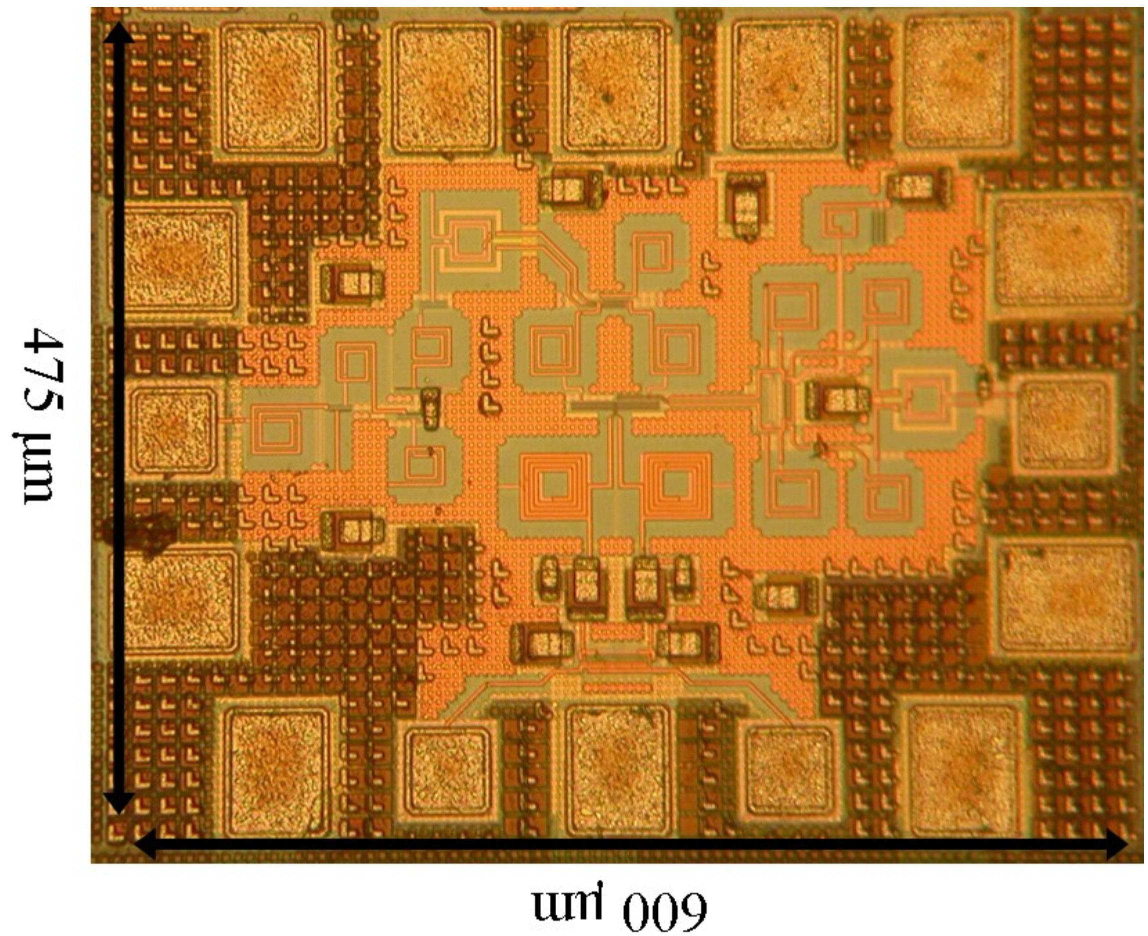
60GHz 90nm GP CMOS Receiver
(D. Alldred et al CSICS-2006)

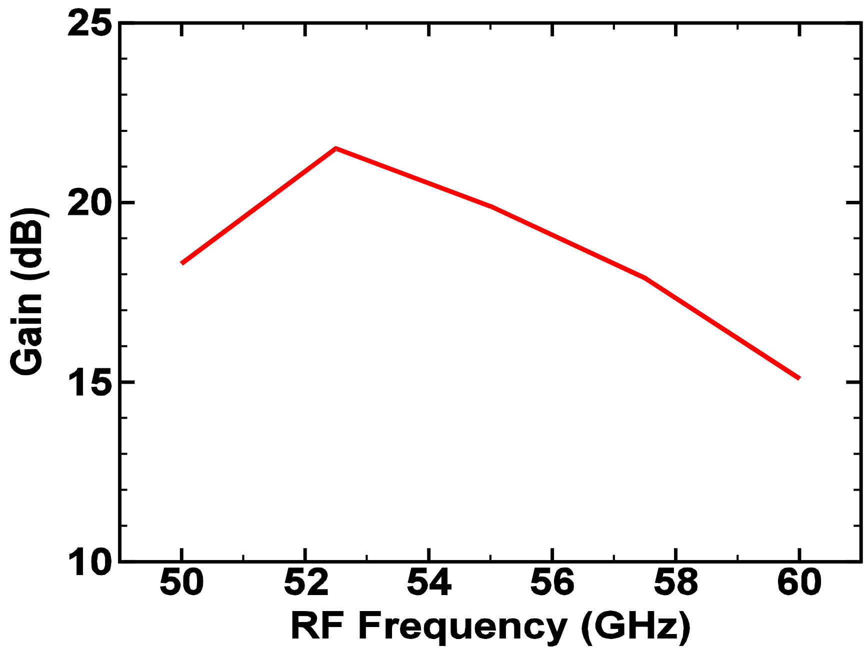
1.2V, 60mW, 20dB gain, NF = 5.5-7dB
IP_{1dB}=-21dBm, IF freq = 3.7-5.5GHz

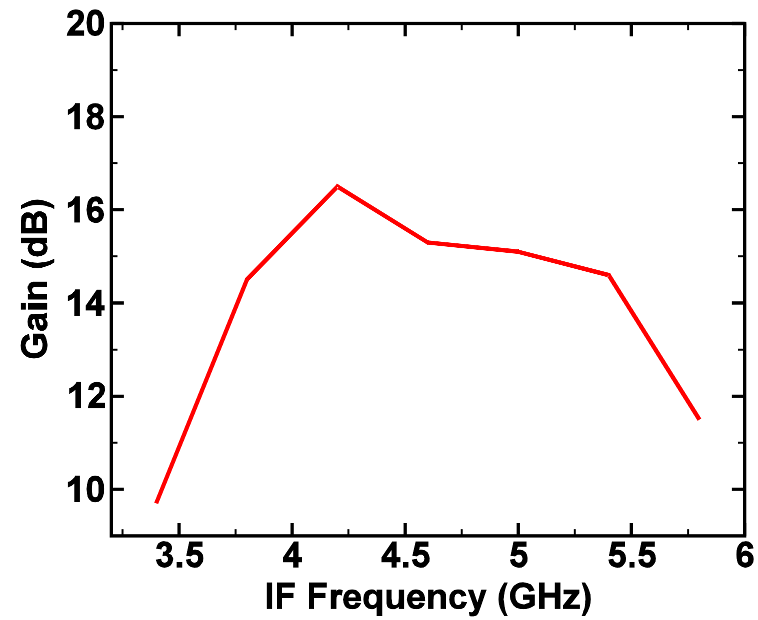


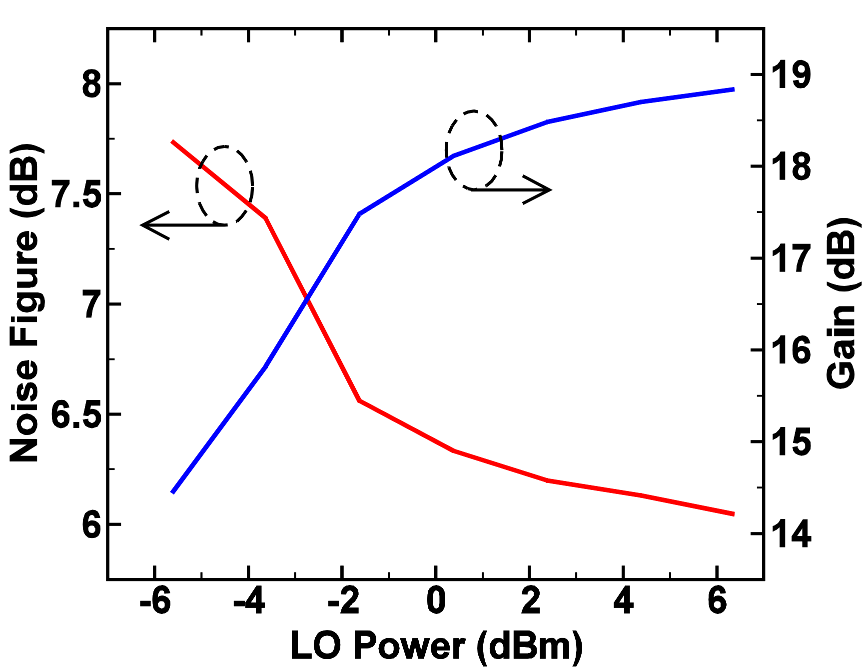


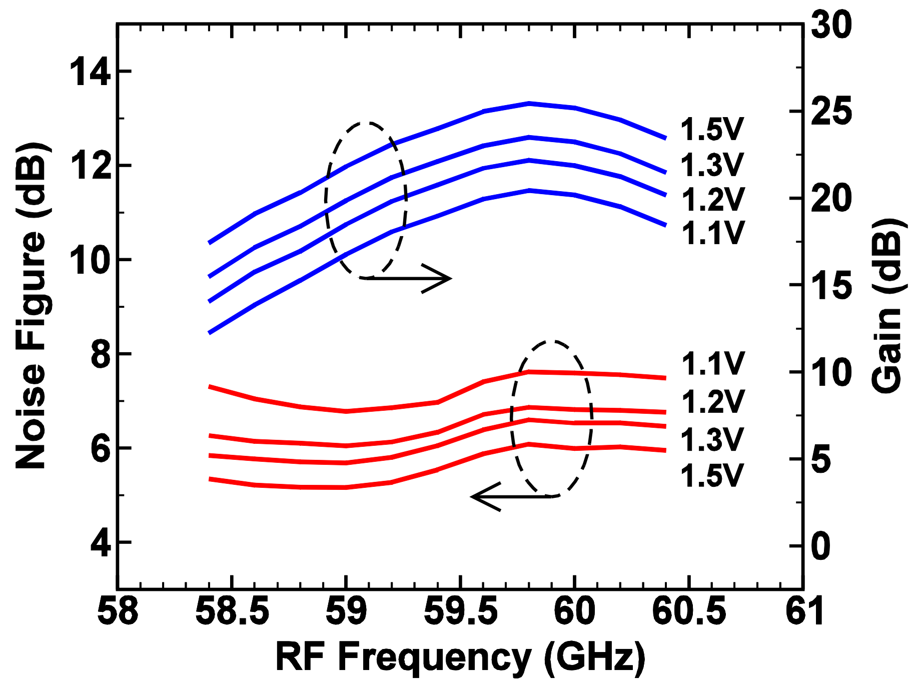


90nm CMOS Receiver Measurements

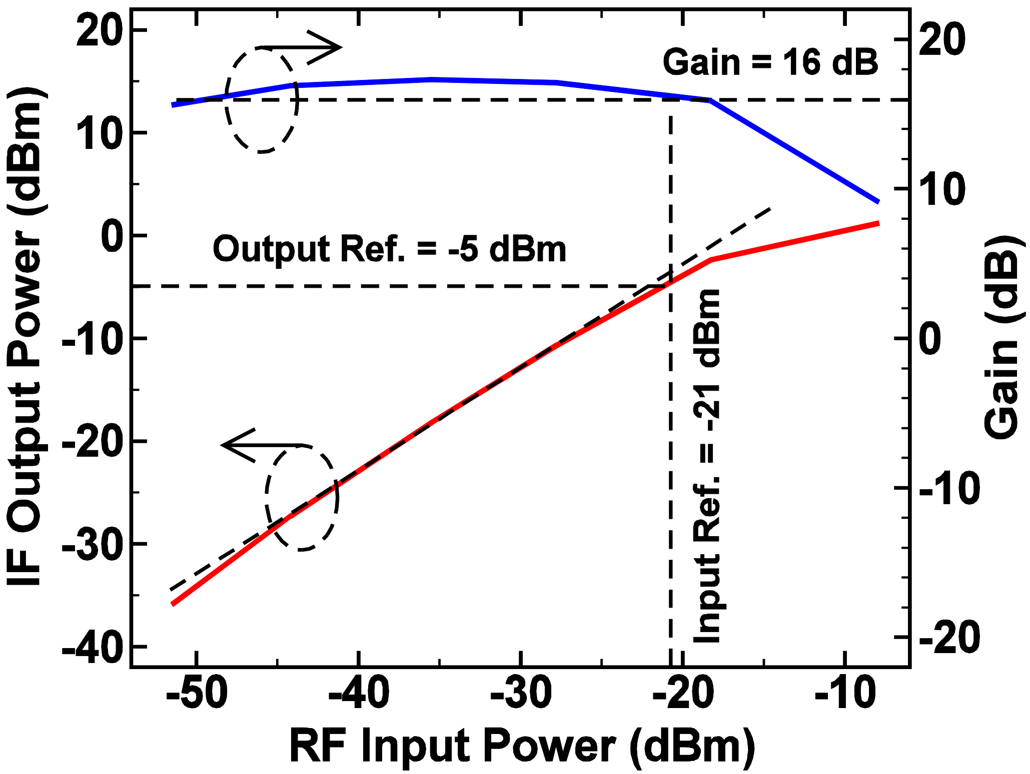


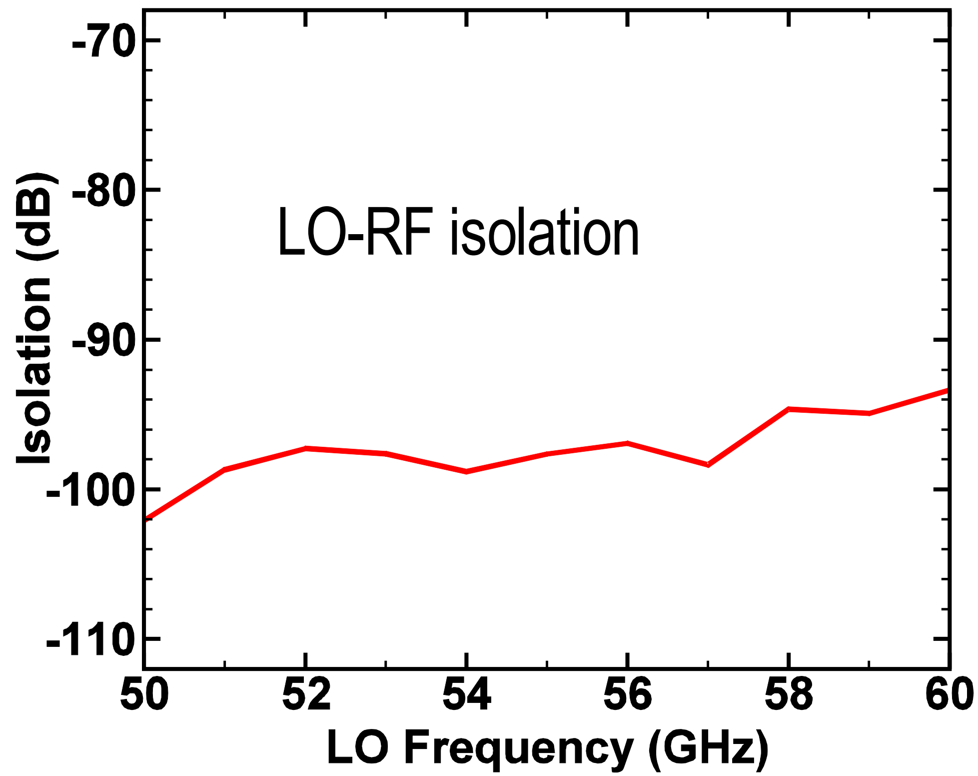




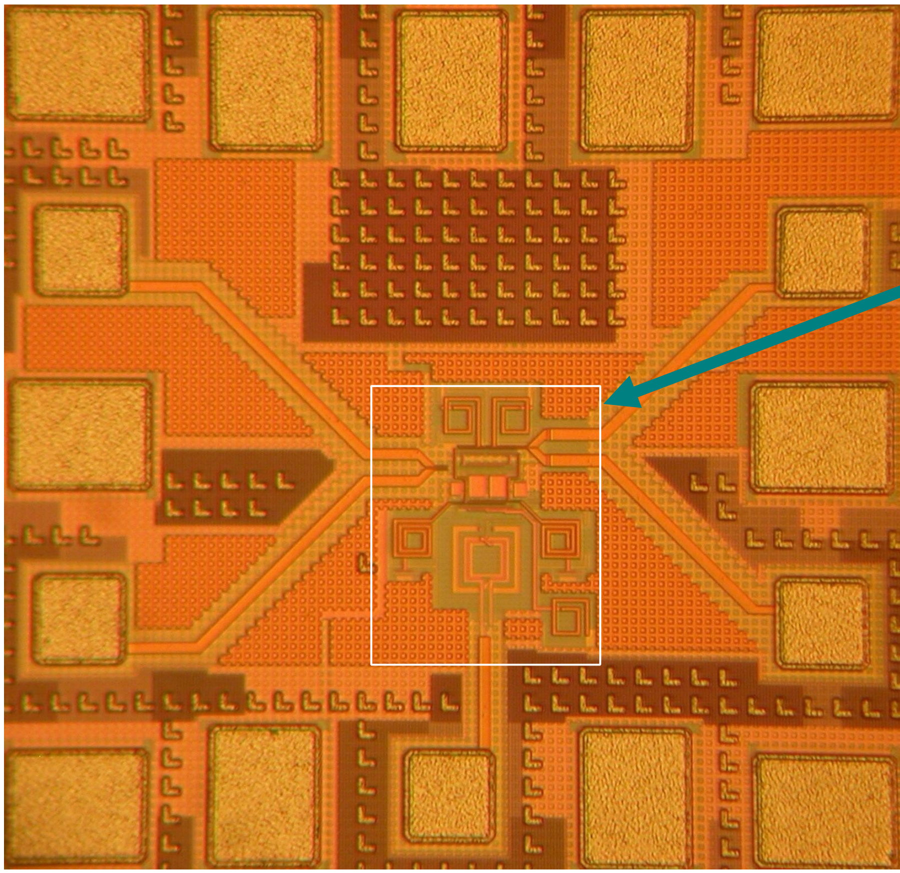


90nm CMOS Receiver Measurements (ii)





60GHz 90nm GP CMOS Upconverter

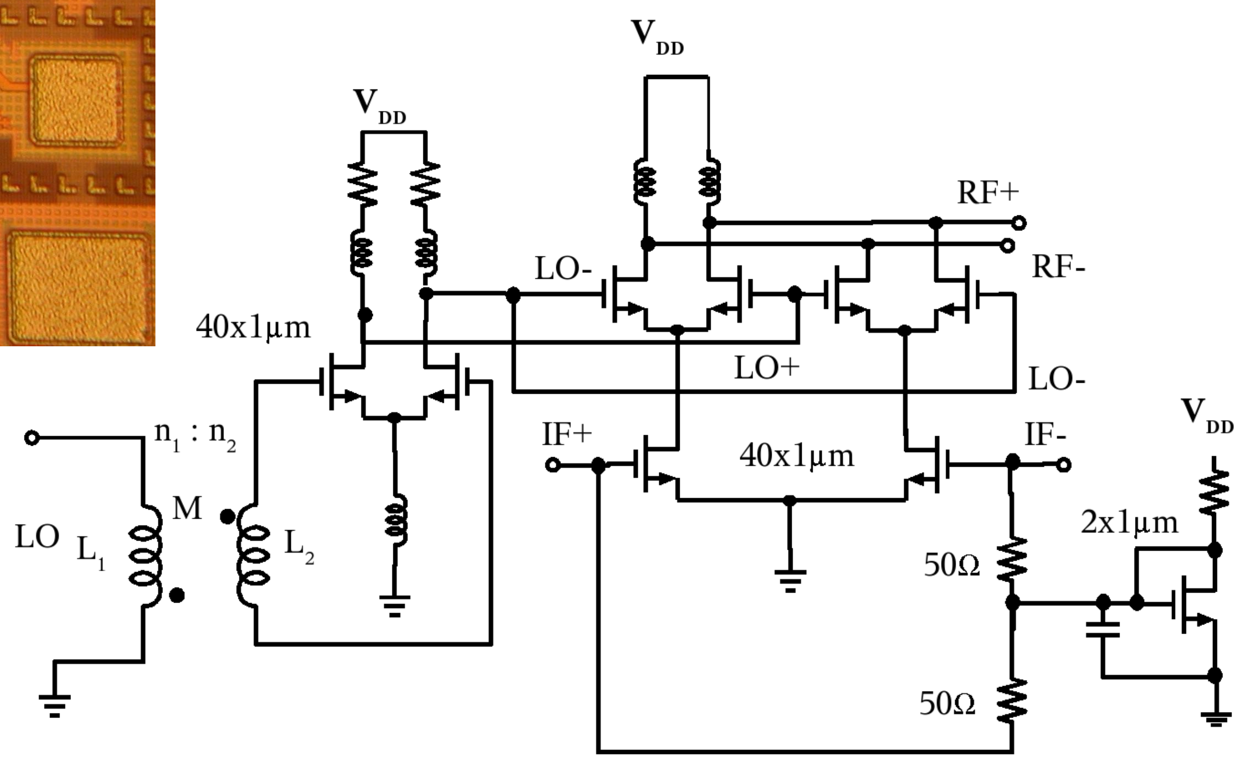


480µmx550µm, 1.5V, 70mW

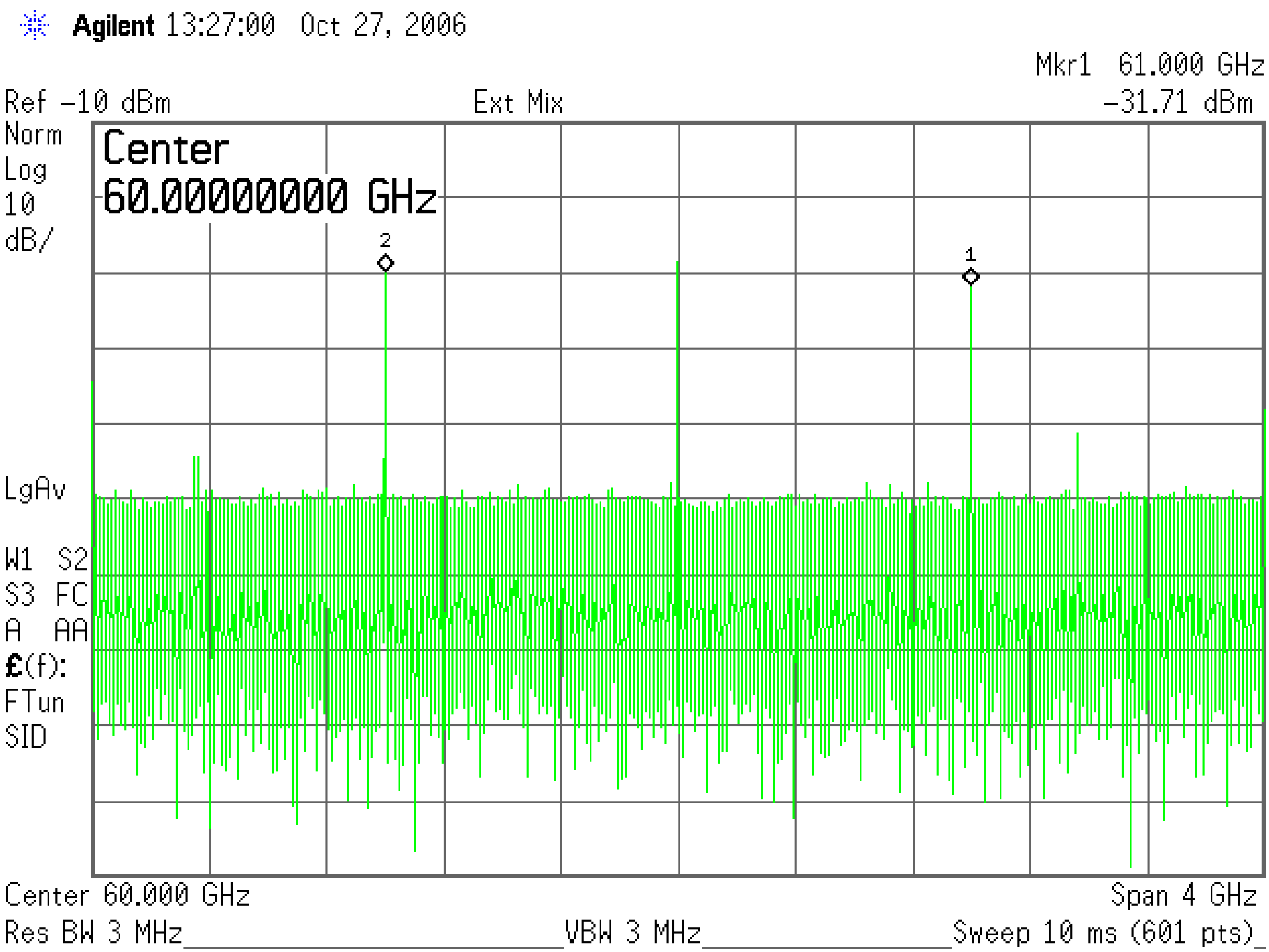
150µmx150µm core

-6dB gain, O_{1dB} = - 2dBm

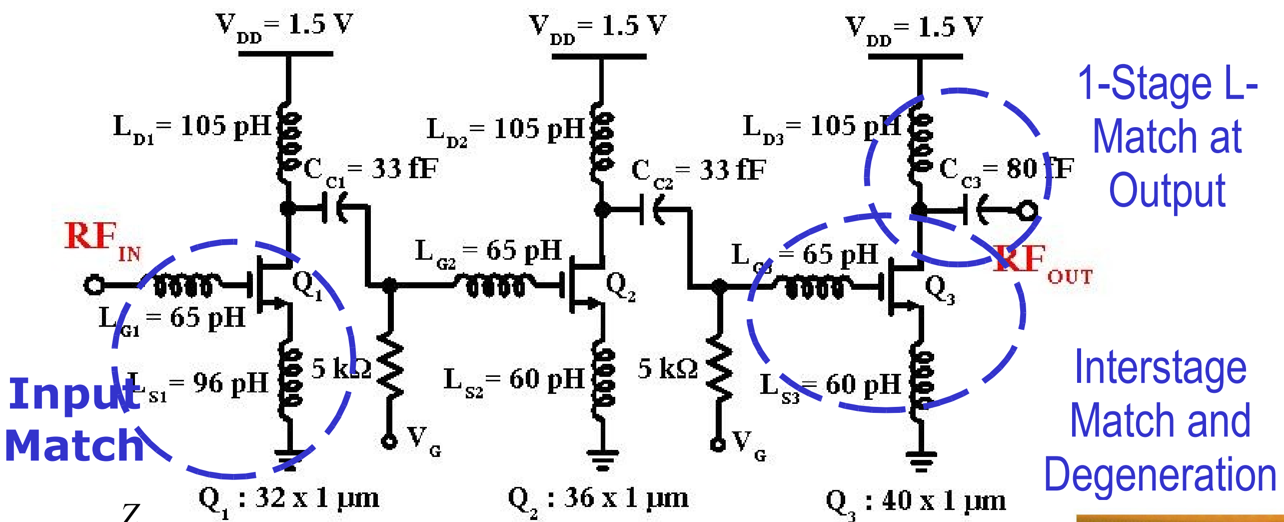
IF=DC-5 GHz, RF=55-60GHz



CMOS Upconverter RF Spectrum

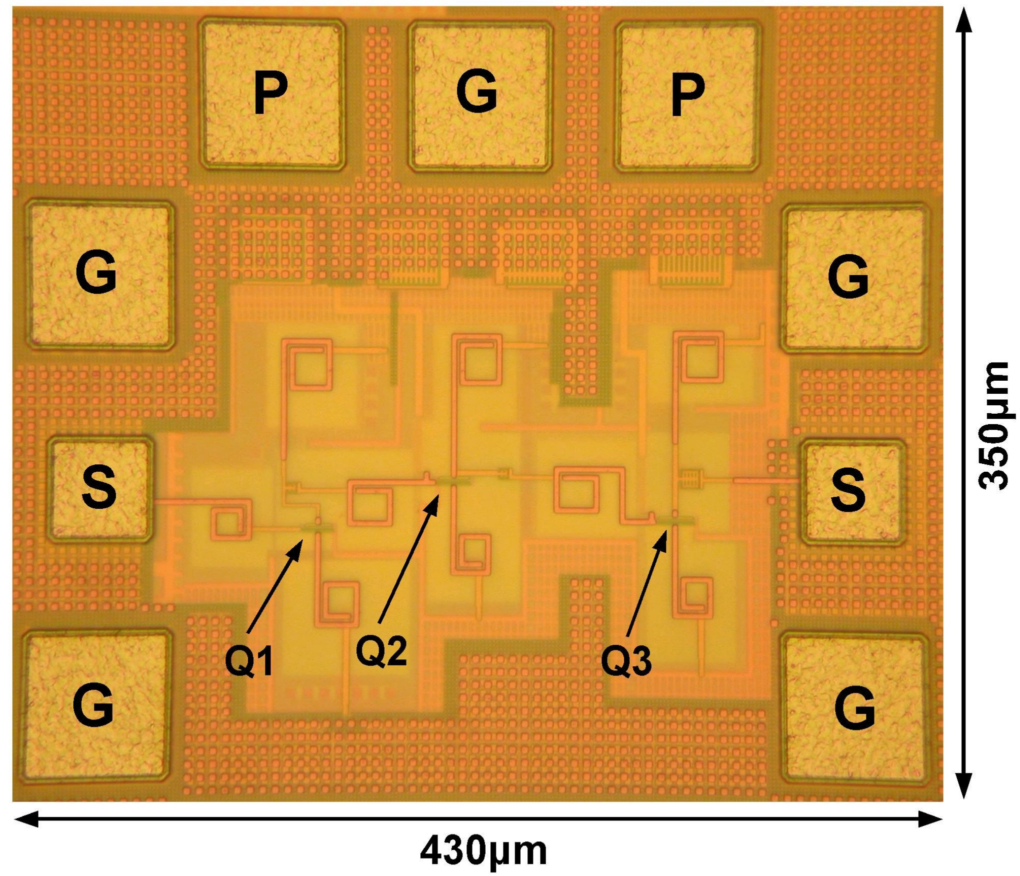


60GHz PA in 90-nm RFCMOS (T.Yao et al. RFIC-06)

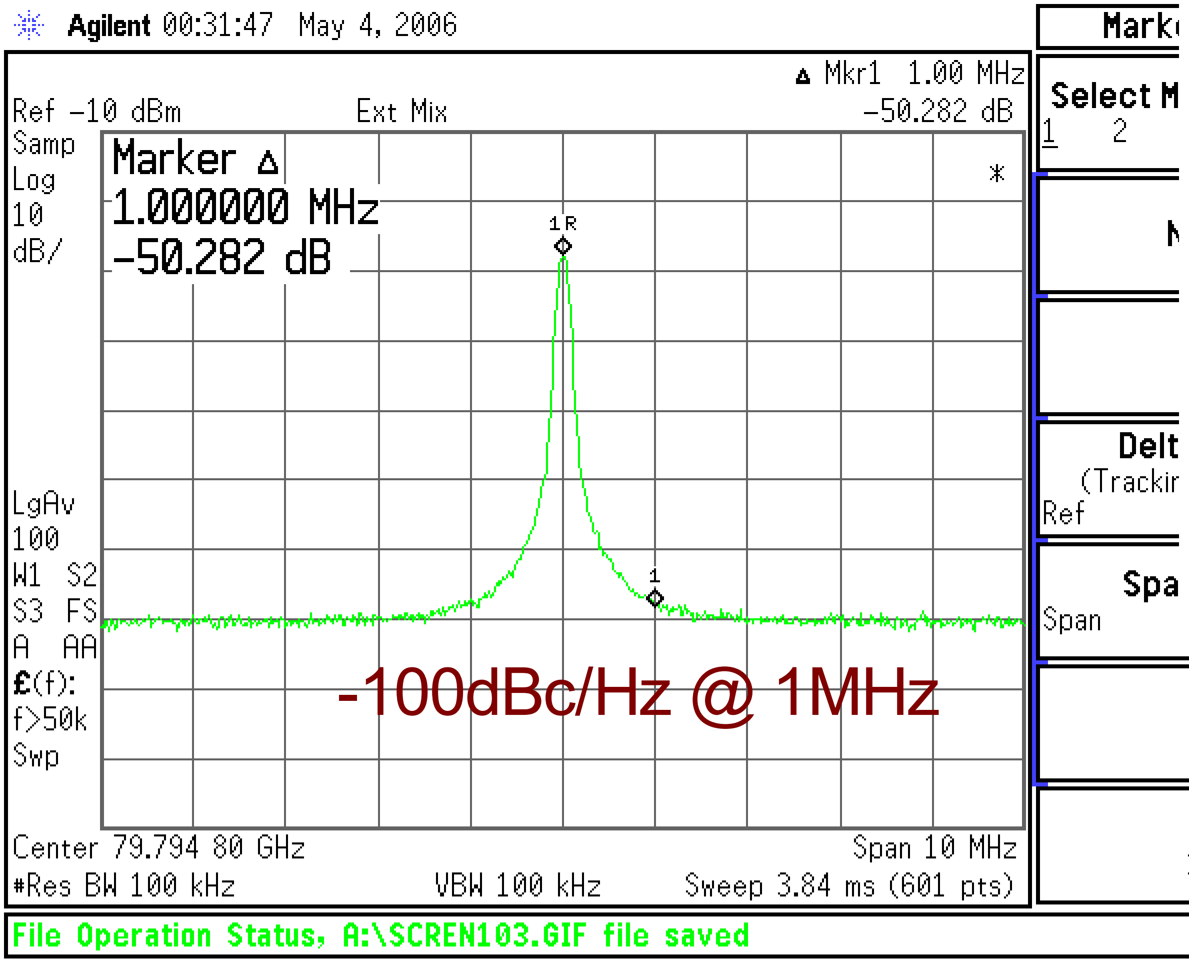


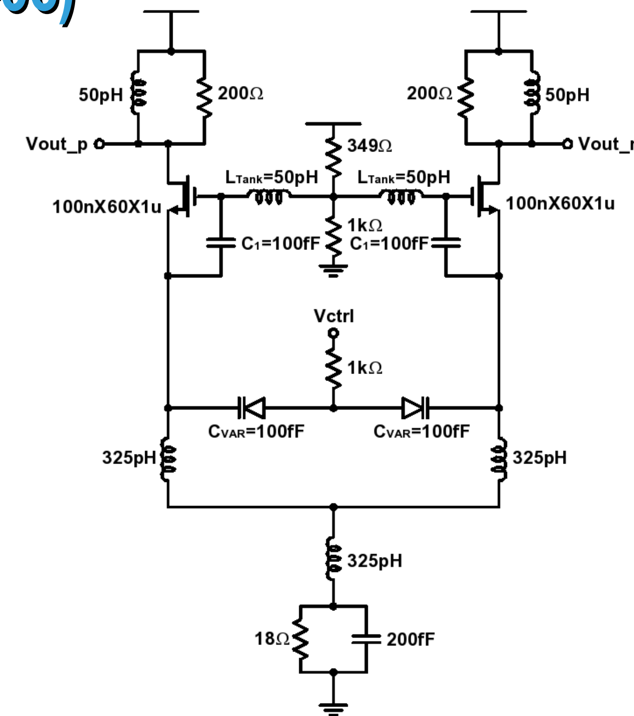
$$L_S = \frac{Z_o}{\omega_T}$$

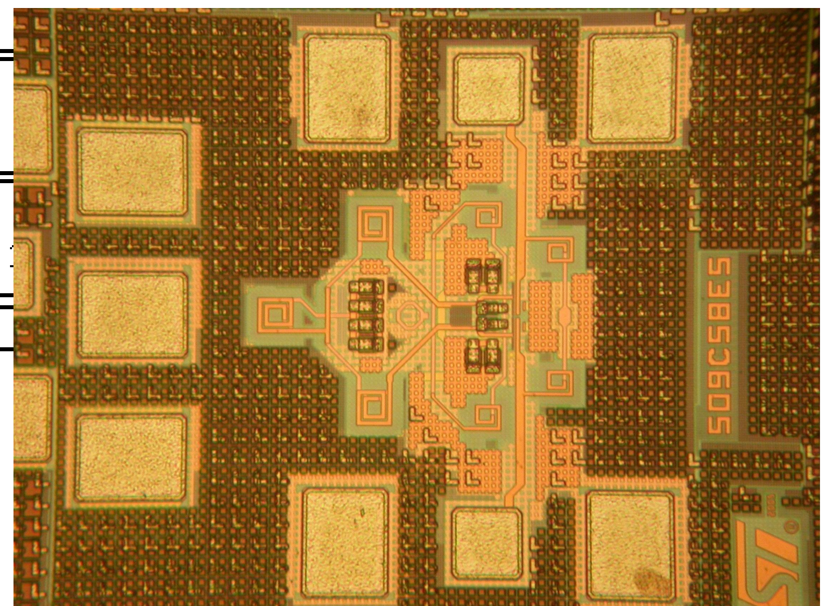
- G=5dB, O_{1dB}=6.4dBm, P_{sat}=9dBm
- PAE=7%
- 14dB gain version in 90nm digital GP CMOS also tested



77GHz Colpitts VCO in (digital) 90-nm GP CMOS
(K.Tang et al. CSICS-06)





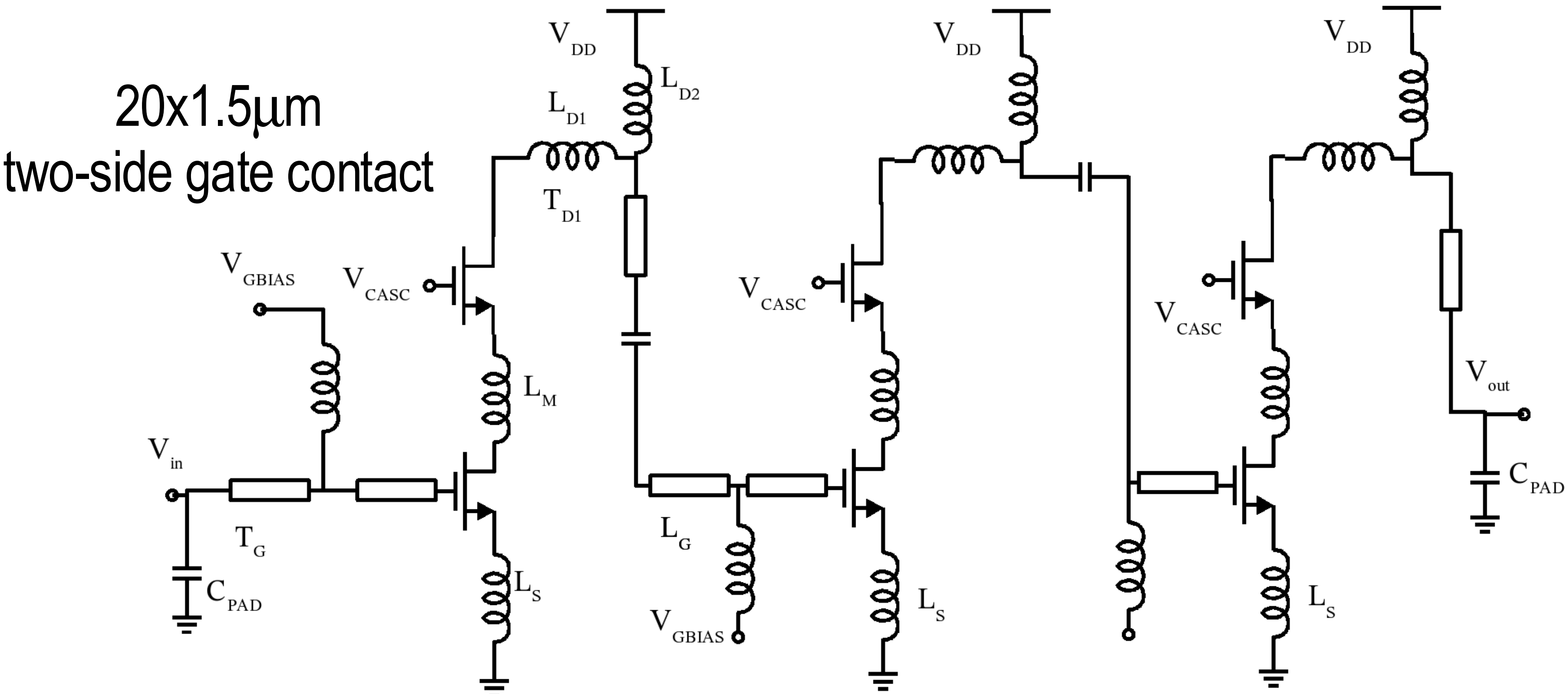


Biased as LNA, at 0.15mA/μm

Record phase noise for CMOS above 60 GHz

W-band 3-stage cascode LNA in 65nm LP RF-CMOS

S. Nicolson (CSICS 2006)

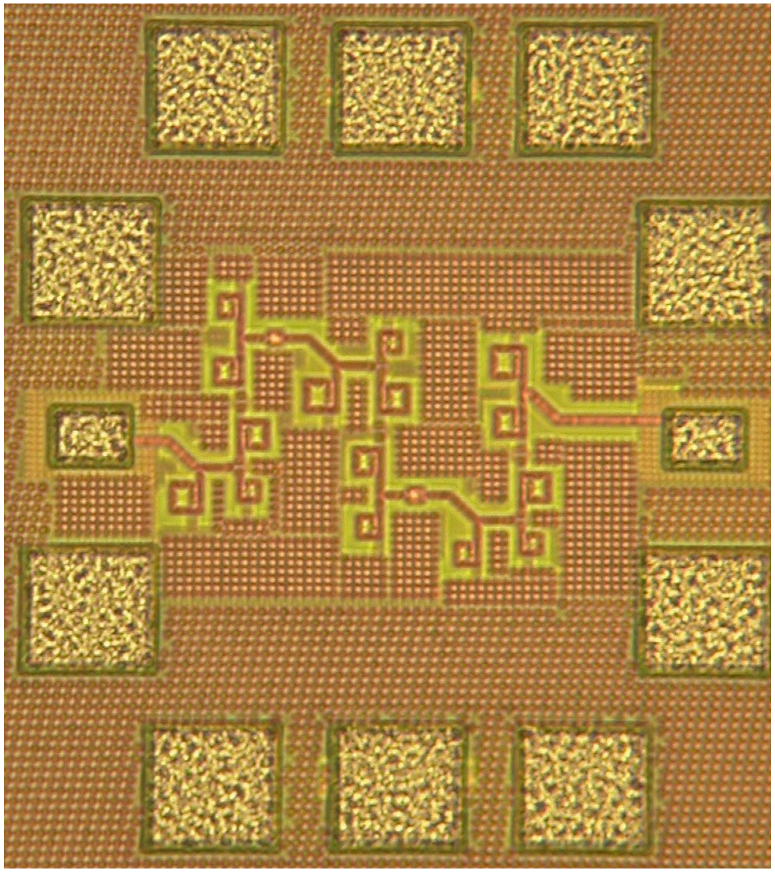


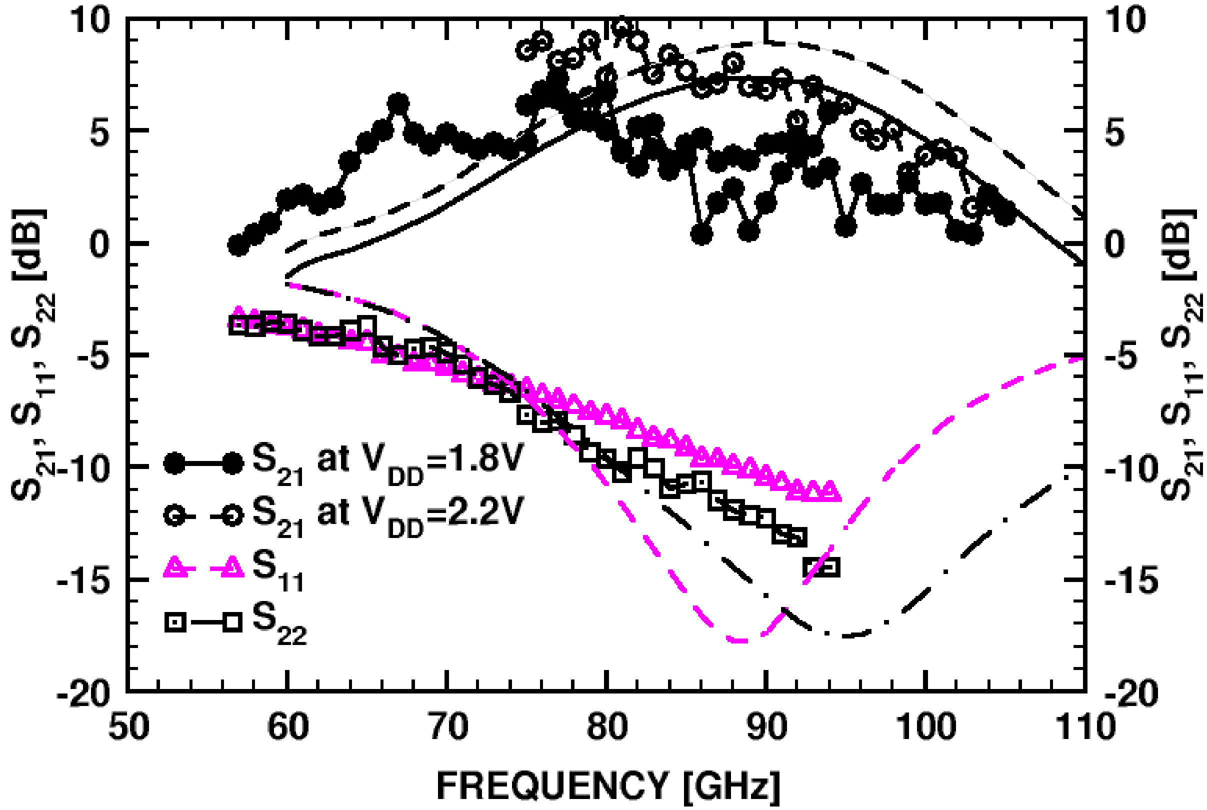
- Inductive broadbanding (L_M) -> also lowers NF_{50} (CS-CG topologies also fabricated)
- Pad capacitance included in design methodology at mm-waves

$$R_{in} = Z_0/[1+(\omega Z_0 C_{PAD})^2] = R_s + R_g + L_S\, \omega_T(casc)$$

$$R_{sopt} = Z_0/[1+(\omega Z_0 C_{PAD})^2] = R_s + R_g + f_T(casc)/(2fg_m)$$

Die photo and measured S-params

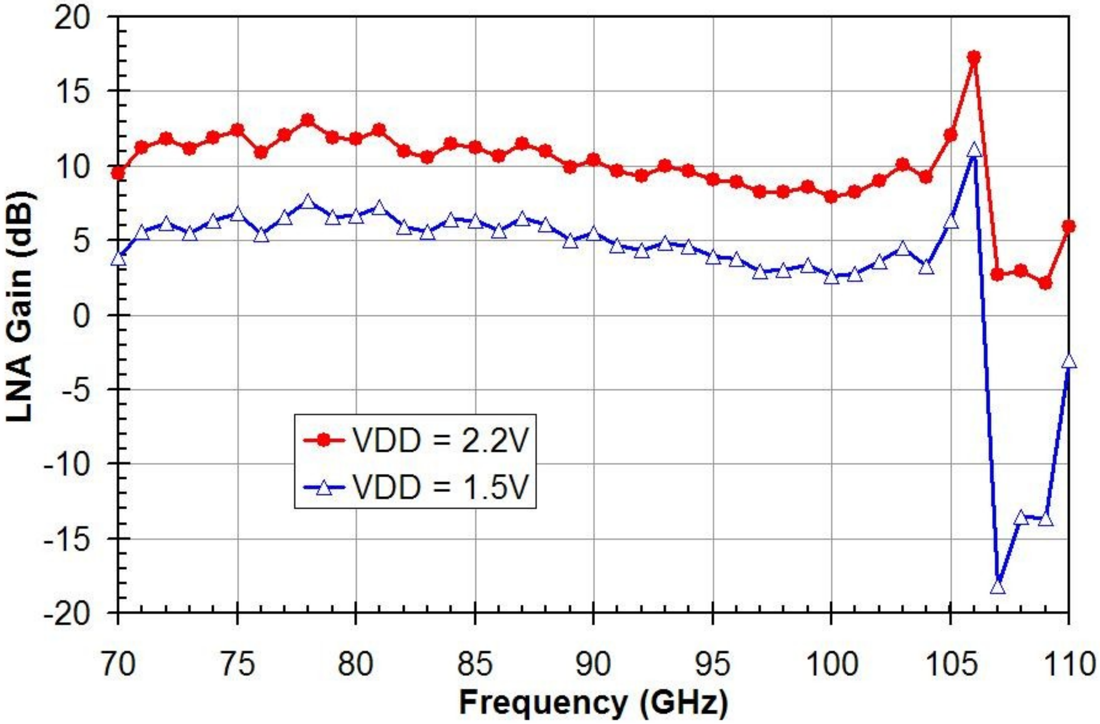




- 0.4mmx0.4mm including pads

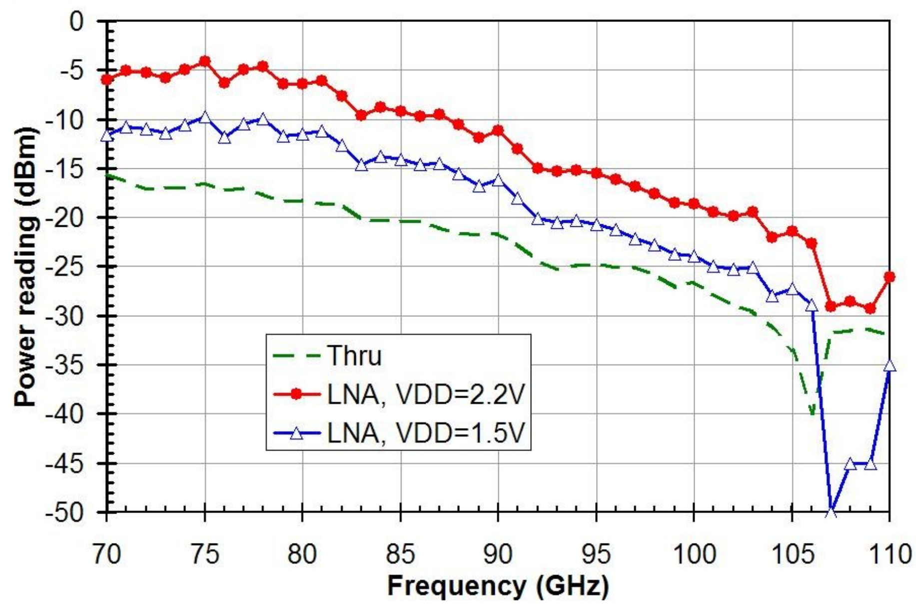
- Overdriven in non-linear mode
- S_{11}, S_{22} < -10 dB, S_{12} < -30 dB

LNA meas. with attenuator and power sensor



- Peak gain = 13 dB @ 77 GHz
- Gain > 0 dB up to 110 GHz
- 3dB bandwidth : 70-90 GHz

- Record for CMOS but...
- 10dB lower gain than 130nm SiGe HBT LNA (S. Nicolson et al, IMS-2007)
- 50GHz lower than highest frequency SiGe amplifier (E. Laskin et al, RFIC-07)



Summary

- CMOS for low-power SOCs up to 100 GHz
- GP rather than LP CMOS is needed
- 65nm CMOS DC gain is OK
- We can live with leakage at mm-waves
- CMOS design based on current density rather than V_T/V_{eff} => think HBT design
- 60-100 GHz state-of-the-art CMOS circuits in 90nm and 65nm CMOS
- Temperature and wafer mapping of 60GHz LNA, PA and 90GHz divider show manufacturability of 60-80 GHz radio in nanoscale CMOS
- SiGe HBT/BiCMOS still higher performance and lower cost than 65nm CMOS

Acknowledgments

- CITO, NSERC, NORTEL for funding
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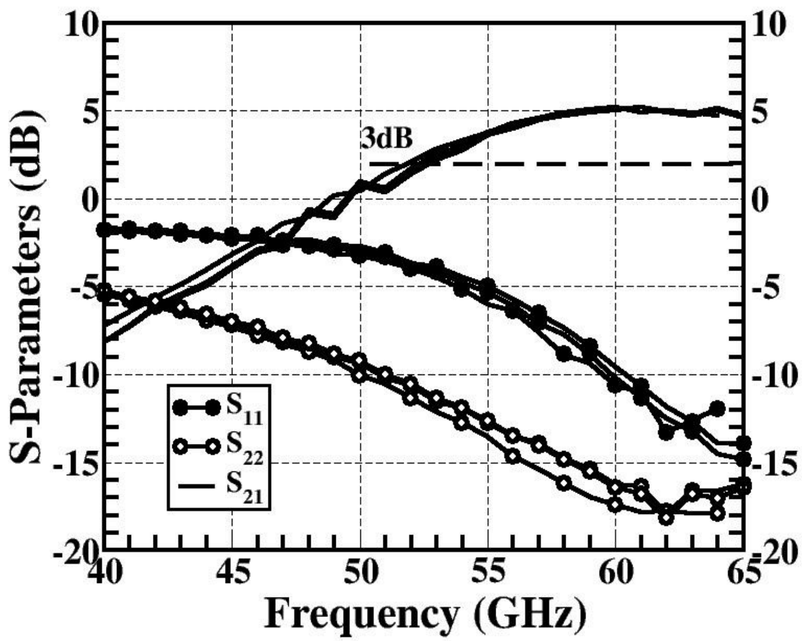
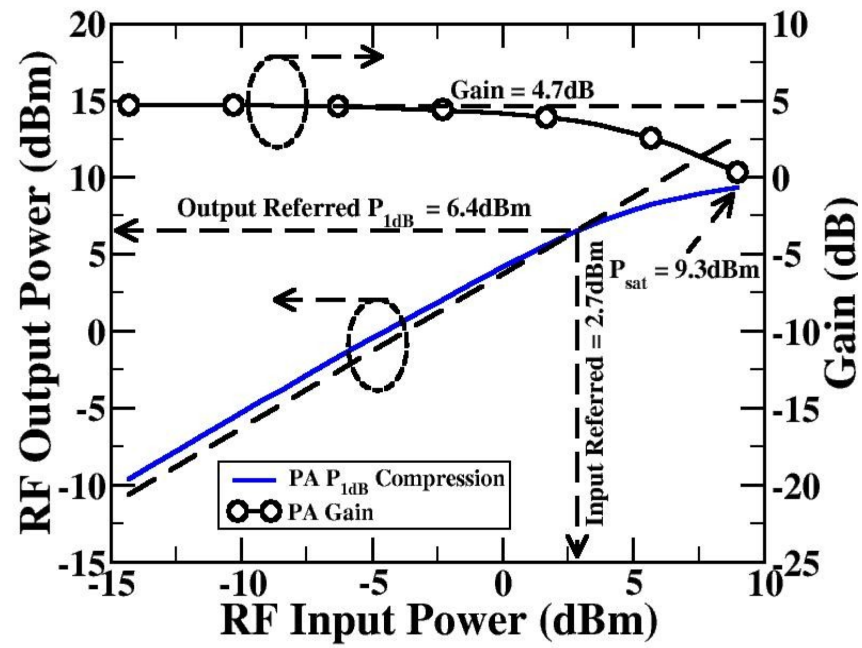
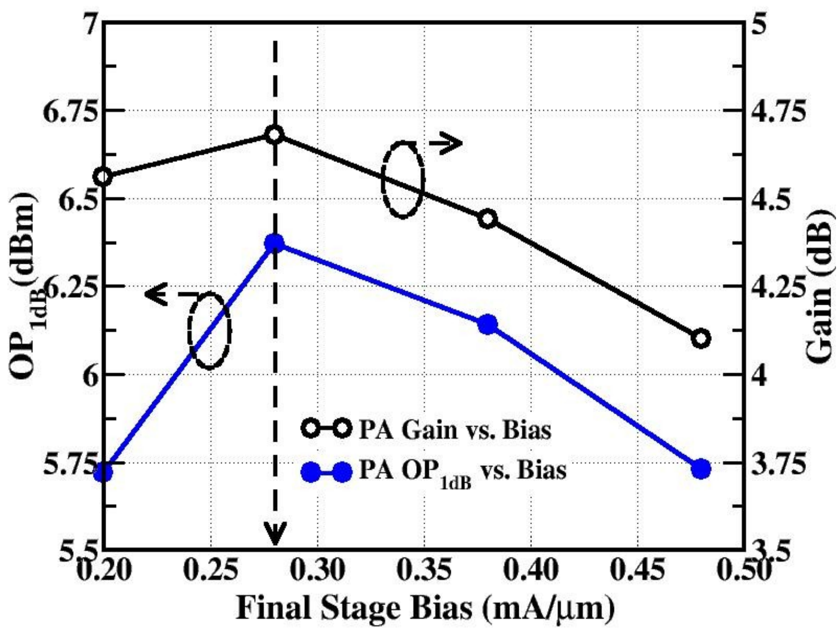
- Theo Chalvatzis and Katya Laskin for 90GHz LNA measurements
- Jaro Pristupa and CMC for CAD support
- OIT, CFI, ECTI for equipment

60GHz PA Measurements

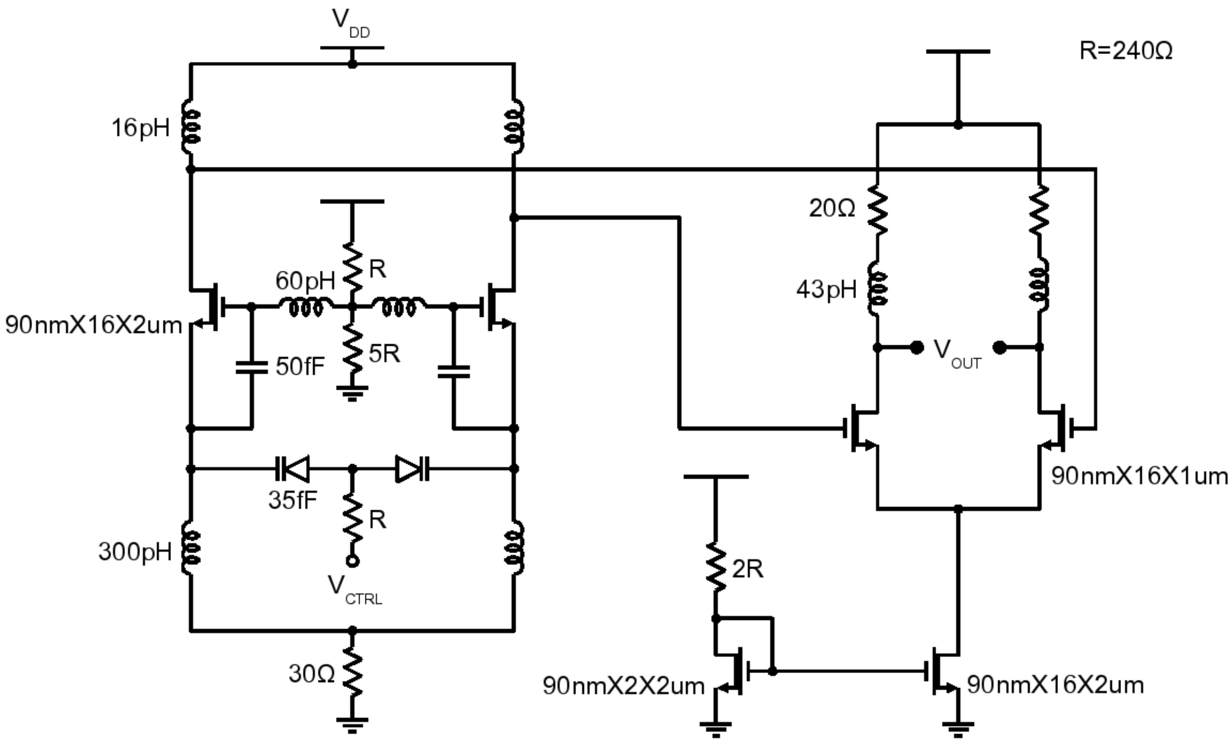


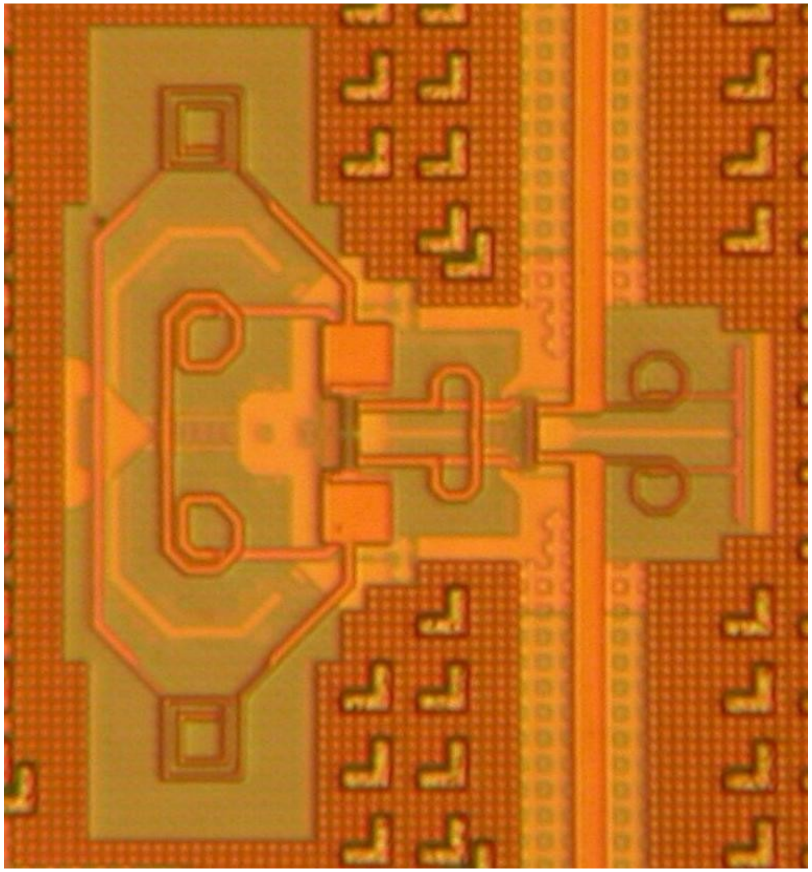




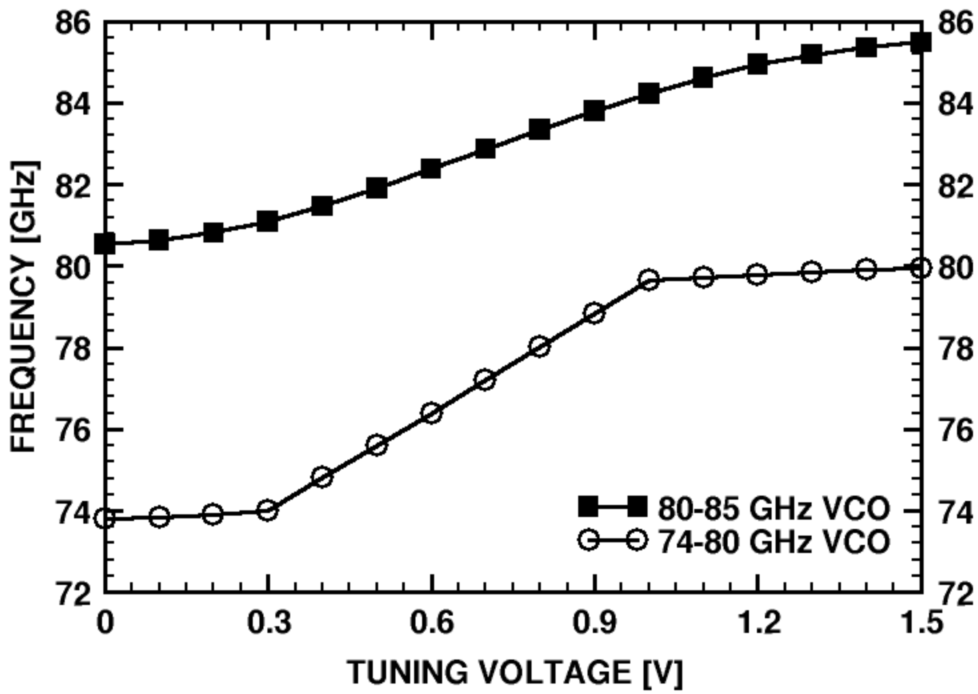
- Measured S-params on 3 dies
- Peak gain = 5.2dB (60GHz)
- 3-dB BW > 13GHz (52-65GHz)
- S_{22}, S_{11} both matched (60-65GHz)
- OP_{1dB} = 6.4dBm, P_{sat} = 9.3dBm
- Maximum linearity @ 0.28mA/µm

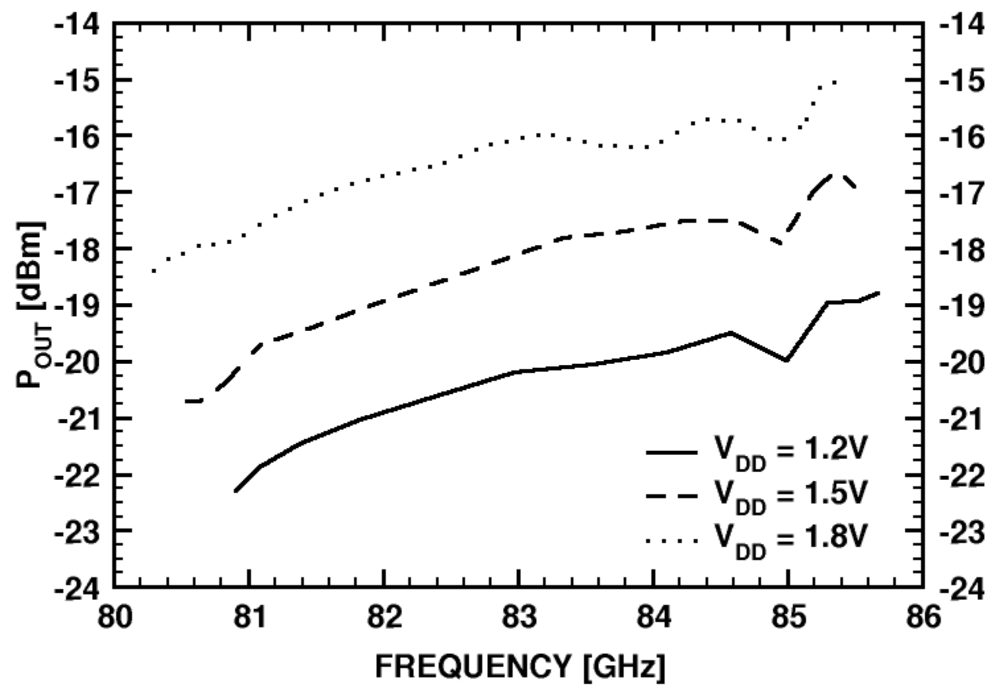
85-GHz Buffered Colpitts VCO 90-nm GP CMOS



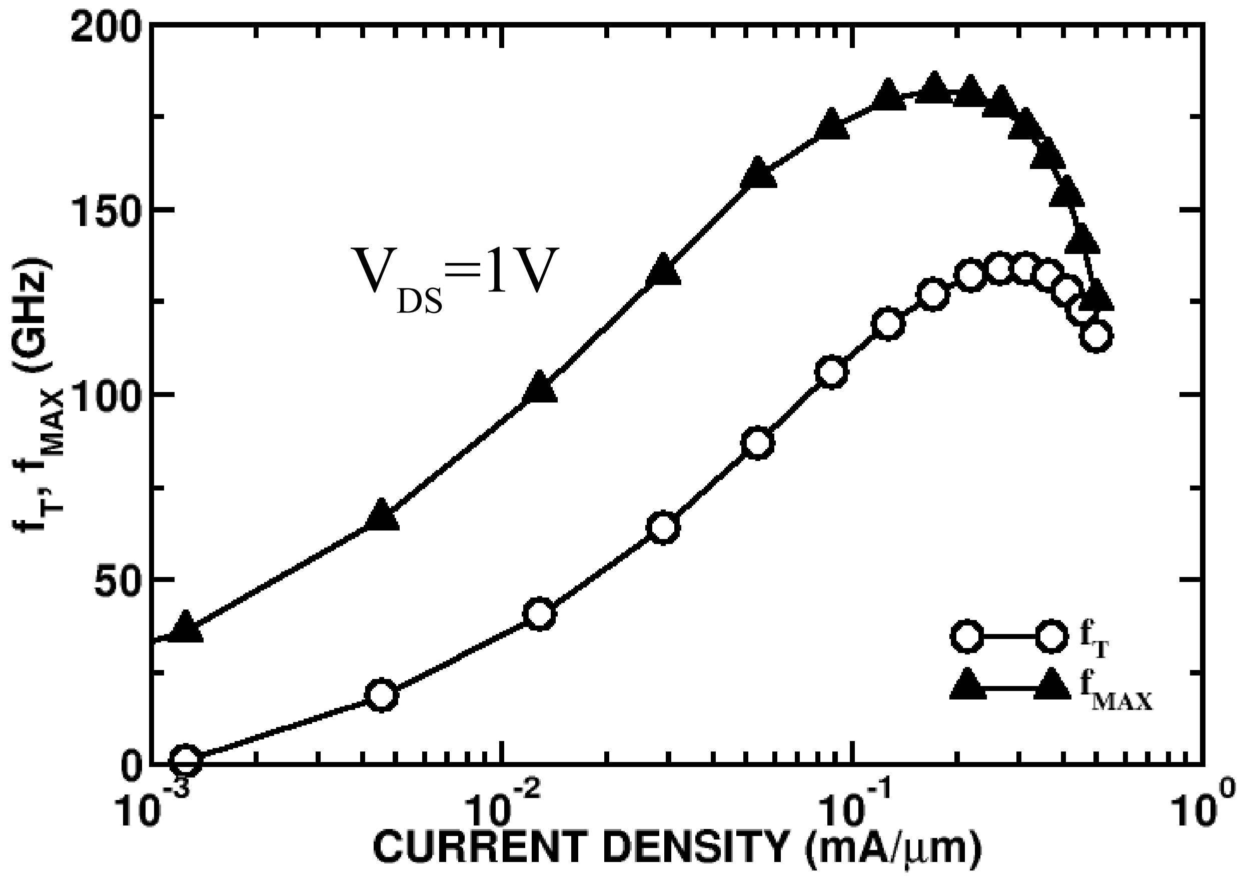


Measured tuning range and output power





Measured 65nm LP MOSFET performance



60-90 GHz Radio Systems

Classical radio architecture: simple and robust at mm-waves

Smaller die, lower cost, higher data rate than 2-10 GHz UWB radio

Crucial front-end blocks/issues:

- **Switch**
- **Divider √**
- **VC0 √**
- **PA √**
- **Isolation √**
- **On-chip mm-wave self-test**

Single-chip transceiver a MUST