Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio

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***Abstract*—Sixty-gigahertz power (PA) and low-noise (LNA) amplifiers have been implemented, based on algorithmic design methodologies for mm-wave CMOS amplifiers, in a 90-nm RF-CMOS process with thick 9-metal-layer Cu backend and transistor $f_{\rm T}/f_{\rm MAX}$ of 120 GHz/200 GHz. The PA, fabricated for the first time in CMOS at 60 GHz, operates from a 1.5-V supply with 5.2 dB power gain, a 3-dB bandwidth >13 GHz, a $P_{\rm 1dB}$ of +6.4 dBm with 7% PAE and a saturated output power of +9.3 dBm at 60 GHz. The LNA represents the first 90-nm CMOS implementation at 60 GHz and demonstrates improvements in noise, gain and power dissipation compared to earlier 60-GHz LNAs in 160-GHz SiGe HBT and 0.13-μm CMOS technologies. It features 14.6 dB gain, an IIP_3 of −6.8 dBm, and a noise figure lower than 5.5 dB, while drawing 16 mA from a 1.5-V supply. The use of spiral inductors for on-chip matching results in highly compact layouts, with the total PA and LNA die areas with pads measuring 0.35×0.43 mm^2 and 0.35×0.40 mm^2, respectively.**

***Index Terms*—Characteristic current densities, CMOS millimeter-wave integrated circuits, $f_{\rm MAX}$, $f_{\rm T}$, inductors, low-noise amplifier (LNA), millimeter-wave, noise figure, power amplifier (PA), receiver, transformers, V-band, 60 GHz.**

I. Introduction

RECENT interest in the 60-GHz band for high-density, short-range wireless links has led to significant progress in the development of integrated circuits for low-cost mm-wave radio systems [1]–[7], [32]. The large bandwidth available in this frequency range, with at least 3 GHz of overlap worldwide (59–62 GHz) in the U.S., Europe and Japan, is well-suited for applications such as WPANs and gigabit/s point-to-point links.

Although millimeter-wave radio front-end ICs have traditionally been the domain of III-V compound semiconductors such as GaAs and InP, an increasing number of 60-GHz building blocks and systems have been recently reported in advanced SiGe BiCMOS [1]–[4], [8], [32] and CMOS technologies [5]–[7] to meet the cost, size and power consumption needs of the consumer marketplace. CMOS is particularly attractive for its potential of integration with IF and baseband DSP functions, enabling true systems-on-chip. As CMOS technology is scaled into the nanometer range, the transistor $I_D - V_{\rm GS}$ characteristics in the saturation region become linear while the transconductance, minimum noise figure ($\rm NF_{MIN}$), $f_{\rm T}$, and $f_{\rm MAX}$ improve. Additionally, when biased at current densities between 0.15 mA/μm and 0.4 mA/μm, these figures of merit (FoMs) become almost insensitive to I_D and $V_{\rm GS}$ variation [9].

In this paper, the potential of 90-nm RF-CMOS for 60-GHz transceiver front-ends is explored in the implementation of two critical building blocks—the power amplifier (PA), demonstrated here for the first time at 60 GHz in CMOS, and the low-noise amplifier (LNA). The LNA is a CMOS replica of a noise- and impedance-matched, 2-stage cascode SiGe BiCMOS LNA [1]. It employs series inductors between the common source (CS) and common gate (CG) transistors for improvements in gain, noise and bandwidth. While earlier 60-GHz LNA implementations in 0.13-μm CMOS [6], [7] have shown the potential of mainstream CMOS technology for mm-wave circuits, this work proves the benefits of technology scaling and demonstrates FoMs comparable to those of SiGe-HBT LNAs [1], [2]. The power amplifier remains an important bottleneck in full transceiver integration, and the problems of low breakdown voltage and low power density are further exacerbated by the move to nanoscale CMOS for mm-wave operation. The 3-stage Class-A PA presented in this work takes advantage of the invariance of the maximum linearity bias current density across technology nodes and aids in evaluating the feasibility of a fully integrated CMOS transceiver at 60 GHz. By relying solely on inductors as on-chip matching elements, both amplifiers achieve smaller area as well as lower power consumption than previously published 60-GHz CMOS circuits.

The device level performance and modeling approach for nanoscale CMOS LNA and PA design are discussed in detail in Section II. The feasibility of implementing compact on-chip passives at mm-waves in CMOS is also illustrated through the examples of spiral inductors for on-chip impedance matching and a transformer for single-ended-to-differential conversion which was measured up to 94 GHz. A design methodology for mm-wave CMOS LNAs is presented in Section III. Section IV focuses on the 60-GHz PA design and finally, experimental results for both amplifiers are discussed in Section V.

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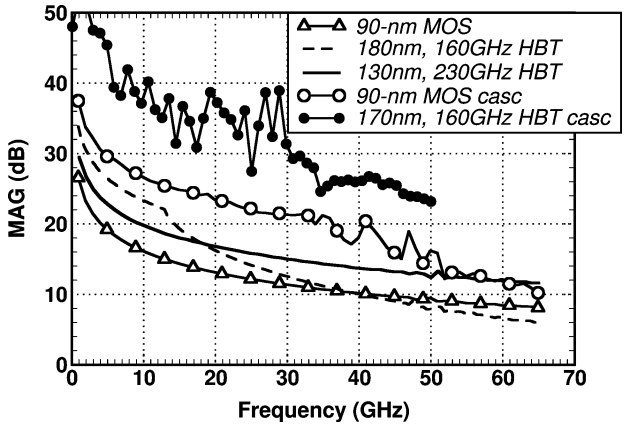

Fig. 1. Measured maximum available gain for cascode and single-transistor configurations in 90-nm CMOS and several SiGe BiCMOS technologies: $W_E = 0.18\ \mu$m, 160 GHz f_T/f_{MAX}; $W_E = 0.13\ \mu$m, 230/290 GHz f_T/f_{MAX}; and $W_E = 0.17\ \mu$m, 160 GHz f_T/f_{MAX}; the MOSFETs and HBTs were biased at $V_{DS} = 0.7$ V and $V_{CE} = 1.2$ V, respectively.

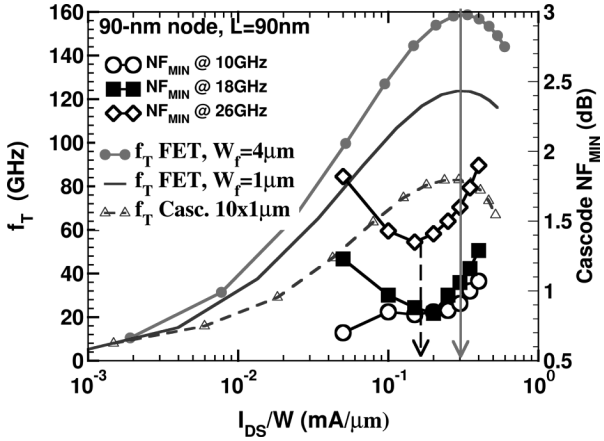

Fig. 2. Measured cascode f_T and NF_{MIN} as a function of drain current per unit gate width for 90-nm nMOSFETs and a 90-nm n-channel cascode.

II. 90-nm RF-CMOS Technology

A. Millimeter-Wave Transistor Performance and Modeling Approach

To evaluate the merits of nanoscale CMOS for mm-wave applications, we first examine the transistor performance in this frequency range and develop robust algorithmic and scalable design methodologies for amplifiers based on constant-current-density biasing. Fig. 1 shows that, while still a few dB lower than that of the most advanced 130-nm SiGe HBTs, the maximum available gain of 90-nm nMOSFETs is larger than 8 dB at 65 GHz. Furthermore, the application of constant-field scaling rules to every new generation of CMOS since the 0.5-μm node has resulted in constant peak f_T, f_{MAX} current densities of 0.3–0.35 mA/μm and 0.2 mA/μm, respectively [9]. This is in contrast to SiGe HBTs where the peak f_T, f_{MAX} current bias is technology dependent, and simplifies the porting of mm-wave CMOS circuits from one foundry to another. As shown in Fig. 2, the peak f_T current density remains constant for different finger widths and for both the CS and cascode configurations. The minimum noise figure bias of nMOSFETs is $J_{OPT} = 0.15$ mA/μm, irrespective of frequency and technology node [9]. This current density is very close to the peak f_{MAX} current density of 0.2 mA/μm and there is practically no degradation of power gain when the nMOSFET is biased for optimum noise. The characteristic current densities of MOSFETs do not change with threshold voltage, temperature, and gate length. While the peak f_T and peak f_{MAX} values decrease with increasing temperature and gate length (not with transistor V_T) [9], [10], by biasing the MOSFETs at the characteristic current density, the circuit performance is maximized for all temperatures, and for gate length and threshold voltage process spread. Any other biasing scheme would lead to wider circuit performance variation with temperature and process spread.

In the design of linear mm-wave PAs, examining the flatness of the f_{MAX} curve when plotted against V_{GS} or I_{DS} is an efficient method of linearity assessment, since f_{MAX} is directly extrapolated from power gain. As seen in Fig. 3(a), f_{MAX} changes by less than 11% (corresponding to the 1-dB compression point) for bias current density swings of up to 0.4 mA_{pp}/μm, irrespective of the technology node and, in the 90-nm node, for gate voltage swings of 0.45 V_{pp}. This property, in conjunction with a drain voltage swing larger than 2 V_{pp} as evident in the experimental output characteristics and load line shown in Fig. 4, can be applied to the design of highly linear power amplifiers. In PAs the optimal linearity bias is located at slightly higher currents than peak f_{MAX}, coinciding with the peak f_T current density of about 0.3 mA/μm, for maximum current and voltage swing before 1-dB compression. The impact of MOSFET scaling on PA linearity can be seen in Fig. 3(a) and (b). While the current swing remains constant across technology nodes Fig. 3(a), the maximum input voltage swing for 1-dB compression decreases with each generation of scaling Fig. 3(b). Hence, to achieve the same output power in a newer technology node, the device size and bias current must be increased to accommodate the drop in allowable voltage swing.

Finally, in addition to constant peak f_T/f_{MAX} bias current densities, the gate-source, gate-drain, and parasitic source/drain-bulk capacitance per unit gate width of p/nMOSFETs also remain largely unchanged across technology nodes [11] at approximately 1 fF/μm, 0.5 fF/μm, and 1.5 fF/μm, respectively. Similarly, the gate resistance can be easily calculated based on layout geometry, contact resistance and salicided gate poly resistance data. A transistor finger width of 1 μm leads to a good compromise between f_T degradation due to the gate-bulk overlap capacitance, C_{GBO}, and reduced gate resistance R_G, thereby increasing f_{MAX}. The gate resistance can be modeled as

$$R_G = \frac{R_{gsq}}{3}\frac{W_f}{N_f l_g} + \frac{R_{cont}}{N_{cont} N_f} + \frac{R_{gsq}}{N_f}\frac{l_{access}}{l_g} \qquad (1)$$

where R_{gsq} is the gate sheet resistance per-square, W_f is the finger width, N_f is the number of fingers, l_g is the gate length, l_{access} is the gate-contact-to-active distance, R_{cont} is the contact resistance and N_{cont} the number of contacts per gate finger. The gate length in this case refers to the physical gate length of 65 nm, which corresponds to the physical width of the polysilicon trace at the end of the fabrication process. In layout, the

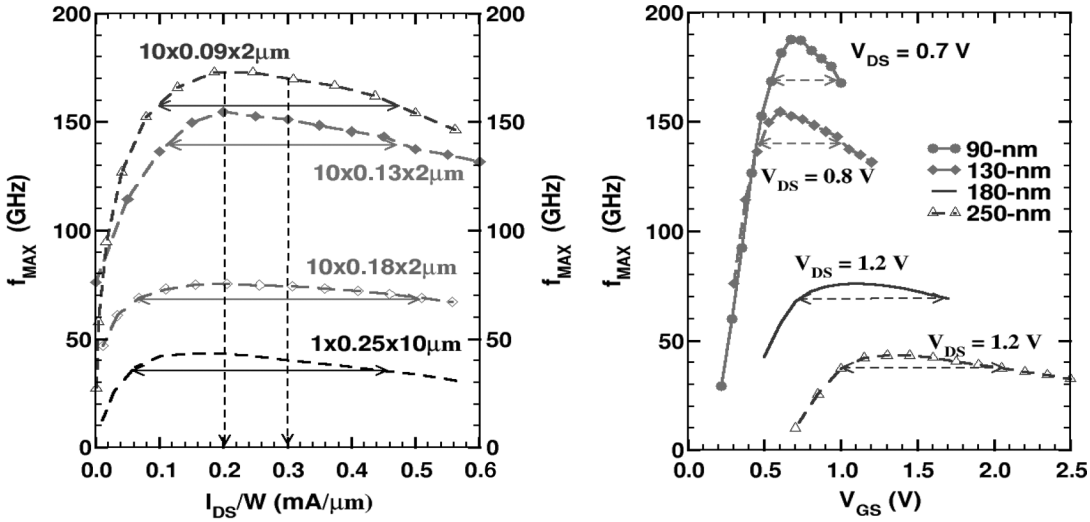

Fig. 3. (a) Measured f_{MAX} as a function of drain current per unit gate width for nMOSFETs across different technology nodes. (b) Measured f_{MAX} versus V_{GS} across different technology nodes.

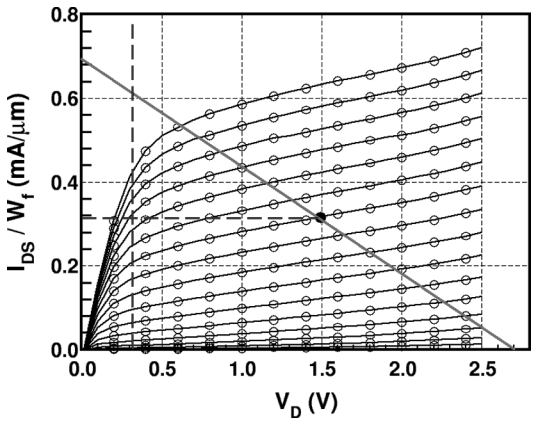

Fig. 4. Optimal load line for 90-nm common source nMOSFET stage on its measured *I–V* characteristic. The breakdown voltage is larger than 3 V.

gates are contacted on one side to avoid metal overlap between gate and drain, thereby minimizing C_{GD}. This results in a gate resistance of about 100 Ω per 1 μm gate finger and a source resistance R_S of (200–250) $\Omega * \mu$m. Since R_S and R_G appear together in the $\mathrm{NF}_{\mathrm{MIN}}$, R_{SOPT} and Z_{IN} expressions of the transistor, further reduction in gate resistance has minimal impact.

The intrinsic and extrinsic peak transconductance of 90-nm nMOSFETs biased in saturation are approximately $1.2\ \mathrm{mS}/\mu$m, and $1\ \mathrm{mS}/\mu$m, respectively. The measured noise parameters for a cascode stage biased at $0.15\ \mathrm{mA}/\mu$m are $R_n = 1880\,\Omega * \mu$m, $R_{\mathrm{SOPT}} = 1200\,\Omega * \mu$m (at 60 GHz) and $X_{\mathrm{SOPT}} = 50000\,\Omega *$ GHz $* \mu$m. These properties, along with the invariance of the f_{T}, f_{MAX} and $\mathrm{NF}_{\mathrm{MIN}}$ characteristic current densities across technology nodes, allow for simple hand design equations of tuned LNAs and PAs with better than 15% accuracy, even at 60 GHz and even in the absence of RF models. The designs of both amplifiers in this paper were conducted mostly by hand analysis based on measured data for the transistor and cascode stage f_{T}, f_{MAX} and $\mathrm{NF}_{\mathrm{MIN}}$, without RF MOSFET models and without parasitic extraction (local capacitance and resistance) from layout since they were unavailable at the time of design.

B. Millimeter-Wave Passives

A direct benefit of designing at mm-waves, and indeed also one of the important enabling factors, is the reduced size of on-chip passives. Significant area savings in the LNA and PA implementations result from the exclusive use of spiral inductors, rather than transmission lines, in the on-chip impedance matching networks. Although the inductors are small enough to be implemented as microstrip lines over metal-1 ground planes [12], test structure measurements have indicated that the spiral inductor implementation systematically leads to higher quality factor (Q) for a given inductance value and die area. All inductors are designed using the ASITIC software [13], whose accuracy at mm-waves has been repeatedly confirmed through previously fabricated inductor test structures in three different CMOS and SiGe BiCMOS technologies from three different foundries [1], [5], [12], [14]. Inductor $2-\pi$ models extracted from ASITIC simulations are used in the circuit schematics to capture the skin effect and substrate parasitics at high frequencies. The die photo of a 140-pH inductor fabricated in the top thick metal layer with 2 μm wide windings and spacing and occupying $29\ \mu\mathrm{m} \times 29\ \mu\mathrm{m}$ is reproduced in Fig. 5. The corresponding simulated and measured effective inductance and Q, larger than 20 at 60 GHz, are shown in Fig. 6. The Q measurements are noisier beyond 40 GHz because the network analyzer itself has lower dynamic range above 40 GHz. Moreover, since the inductance is small (140 pH), with low resistance (0.75 Ω at DC), comparable to that of the probe-to-pad contact and interconnect, and because the Q is high, the Q-f characteristics are more sensitive to measurement error. This problem is similar to that of measuring the f_{MAX} of small MOSFETs.

Single-ended-to-differential conversion is often required between a single-ended LNA output and the input of a double-balanced mixer [1], [5]. Transformers provide the most compact

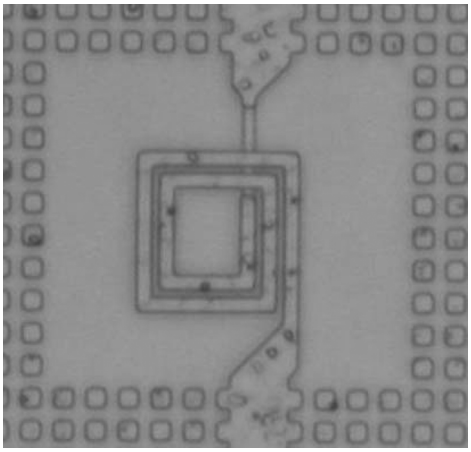

Fig. 5. Die micrograph of spiral $29\ \mu\text{m} \times 29\ \mu\text{m}$, 140-pH inductor with $2\ \mu\text{m}$ width and spacing implemented in the thick top metal of a 90-nm RF CMOS Cu backend with 9 metal layers.

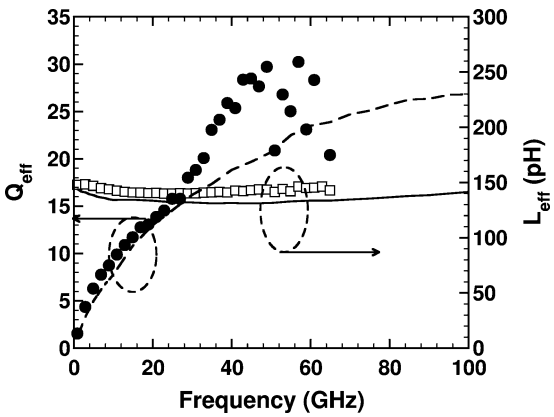

Fig. 6. Measured (symbols) and simulated (lines) inductance and quality factor for the 140-pH inductor. The inductor was simulated using ASITIC.

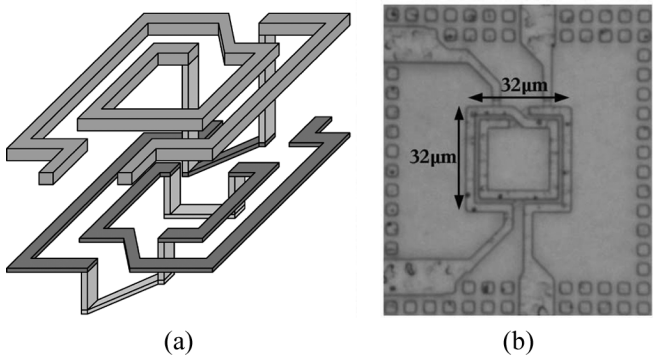

Fig. 7. (a) Design and (b) die micrograph of 1:1 vertically stacked $32\ \mu\text{m} \times 32\ \mu\text{m}$ transformer in 90-nm CMOS.

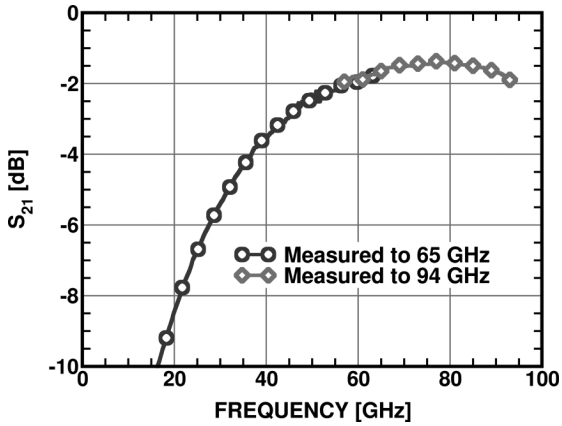

Fig. 8. Measured CMOS transformer S_{21}.

way for realizing single-ended to differential conversion up to at least 100 GHz [14], [15]. Taking advantage of the multi-level interconnect in the 90-nm RF-CMOS process, a 1:1 vertically stacked $32\times32\ \mu\text{m}^2$ transformer (Fig. 7) has also been designed and fabricated. Implementing the transformer in two adjacent metal layers ensures increased coil coupling and minimal area. The measured S_{21}, larger than -2 dB in the 60–94 GHz range (Fig. 8), is better than in an earlier implementation in a 180-nm SiGe BiCMOS process with a thick top Al layer [1].

III. 60-GHz LNA Design

A. Millimeter-Wave CMOS LNA Design Considerations and Methodology

The main design goals for the LNA are captured in the LNA FoM (2) as defined by the ITRS [16], which links the gain (G) and the noise factor (F) together with the linearity (IIP3):

$$\text{FoM}_{\text{LNA}} = \frac{G \times \text{IIP3} \times f}{(F-1) \times P} = \frac{\text{OIP3} \times f}{(F-1) \times P}\ [12]. \quad (2)$$

Achieving a good FoM for an LNA at mm-waves is nontrivial since operating the CMOS devices at frequencies close to the transistors' f_{T} values reduces their intrinsic gain and increases their noise factor. The necessity of employing nanoscale technologies to achieve the desired operation at mm-waves leads to reduced supply voltage and hence, limited headroom and linearity.

In the design of the LNA, we chose the cascode topology which, compared to the CG [7] or CS topologies, exhibits better isolation, improved bandwidth and higher gain even at mm-wave frequencies. The CMOS cascode topology can be simultaneously noise- and input-impedance matched. To improve the performance of a cascode LNA at mm-wave frequencies, a series inductor can be placed between the CS and CG transistors to tune out the middle pole of the cascode and to compensate for its lower f_{T}. As shown in the topology of Fig. 9, the series inductor L_M forms an artificial transmission line with the gate-source and source-bulk capacitances of transistor Q_2 and with the drain-bulk and gate-drain capacitances of transistor Q_1. The characteristic impedance of this line (Z_{o1}) is equal to the load impedance of Q_1 (3) as well as to the source input impedance of Q_2 (4).

$$Z_{o1} = \sqrt{\frac{L_{M1}}{C_{gs2} + C_{sb2}}} = Z_{Q1,\text{load}} \quad (3)$$

$$Z_{o1} = Z_{Q2,\text{in}} = \frac{1}{gm_2} + \frac{\omega L_{D1} Q}{1 + gm_2 ro_2}. \quad (4)$$

This technique has been successfully applied to low-GHz LNA designs [17] and high-speed HEMT-CML circuits [18]. It is

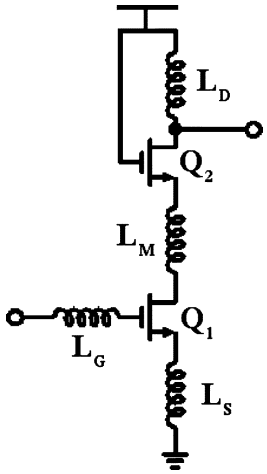

Fig. 9. LNA topology: cascode with middle inductor.

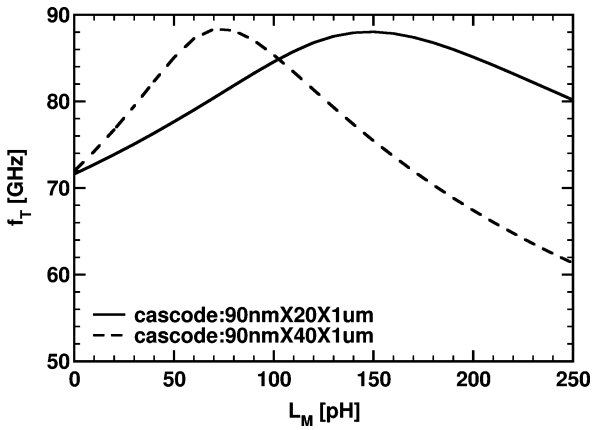

Fig. 10. Simulated $f_{\rm T}$ as a function of L_M for two different sizes of 90-nm nMOSFET cascode structures.

also proving to be useful now at mm-waves. Using (3) and (4) directly, without apriori knowledge of the load inductor L_{D1}, is problematic. Instead, it was found by simulation and experiment, that the optimal value of L_M can be obtained simply by simulating the $f_{\rm T}$ and $\rm NF_{MIN}$ of the entire cascode, with inductive broadbanding, as a function of L_M. As shown in plots of simulated $f_{\rm T}$ as a function of L_M for 2 different sizes of 90-nm nMOSFET cascode structures (Fig. 10), the $f_{\rm T}$ of the CMOS cascodes is increased by as much as 25% by adding L_M.

An algorithmic design methodology has been developed for a CMOS cascode LNA, based on active device matching, similar to the one applied to mm-wave SiGe-HBT LNAs [19]. After calculating the effective signal source resistance seen by the amplifier across its bond pad as in [22], the following seven design steps apply to the inductively-loaded cascode LNA shown in Fig. 9.

Step 1) Set the bias to the optimum $\rm NF_{MIN}$ current density ($J_{\rm OPT}$) to minimize the transistor noise figure. It is approximately 0.15 mA/μm, independent of the CMOS technology node or foundry [9].

Step 2) Choose an optimal W_f to maximize $f_{\rm MAX}$ and minimize $\rm NF_{MIN}$. For 90-nm CMOS, W_f is 1–2 μm.

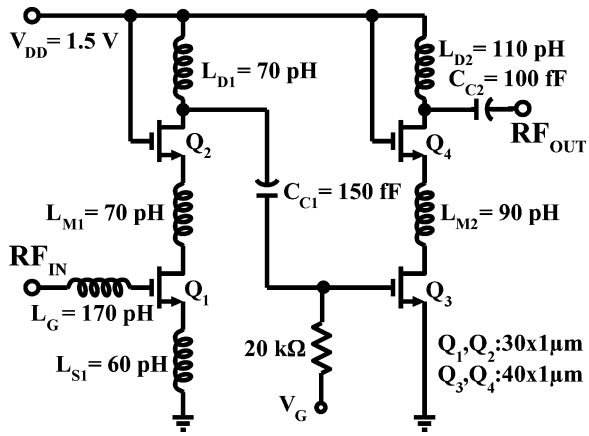

Fig. 11. Schematic of 60-GHz inductively-loaded LNA.

Step 3) Find the best L_M for the cascode biased at $J_{\rm OPT}$ by plotting the $f_{\rm T}$ of the cascode versus L_M (Fig. 10). Note that L_M scales with W^{-1} (N_f^{-1}).

Step 4) With all devices biased at $J_{\rm OPT}$, scale the number of fingers (N_f) and L_M to match the optimal noise impedance $R_{\rm SOPT}$, at the frequency of operation, to the source impedance.

Step 5) After layout and parasitic extraction, with $f_{\rm T}$ from Step 4 and according to (5), find $L_S = (Z_0 - R_S - R_G)/\omega_{\rm T}$ [20]. Note that adding L_S does not affect $R_{\rm SOPT}$ previously matched in Step 4 and that $\omega_{\rm T}$ corresponds to the cascode with L_M, not just to the transistor, and after extraction of layout parasitics.

$$Z_{\rm IN} = R_S + R_G + \omega_{\rm T} L_S + j\omega(L_S + L_G) - j\frac{\omega_{\rm T}}{\omega g_m} \quad (5)$$

where $\omega_{\rm T}$ and g_m already include the impact of R_S.

Step 6) Add L_G to tune out $\rm Im\{Z_{IN}\}$ and $\rm Im\{Z_{SOPT}\}$ according to (5).

Step 7) Add output matching network with inductive load to maximize gain [20].

Following this design methodology, it is possible to achieve the lowest noise performance in the given CMOS technology.

B. 60-GHz LNA Circuit Description

A 60-GHz LNA (Fig. 11) has been designed and fabricated in 90-nm RF-CMOS using the methodology described in Section III-A. It employs a 2-stage cascode topology with series inductors (L_{M1}, L_{M2}) between the CS and CG transistors in each stage. The input stage transistors are biased at 0.2 mA/μm for maximum gain and are sized such that the real part of the optimum noise impedance ($R_{\rm SOPT}$) is about 40 Ω, which accounts for the input pad capacitance as in [22]. This achieves a good compromise between noise impedance matching (requiring a device gate width of 24 μm), gain, linearity (requiring large device and current) and insensitivity to impedance mismatch and process variation, which calls for low R_n and minimized contribution of R_S and R_G to the overall

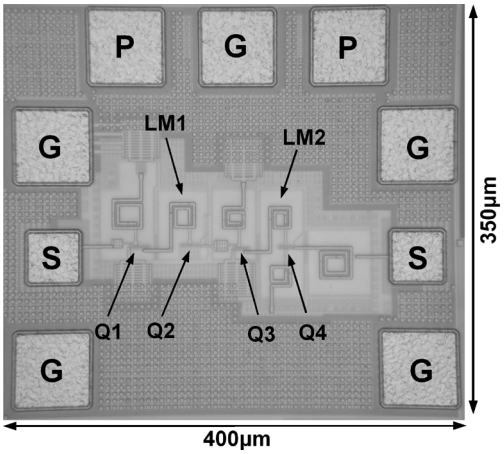

Fig. 12. Die micrograph of 60-GHz LNA ($350\ \mu\text{m} \times 400\ \mu\text{m}$).

input and noise impedance ($R_S + R_G < 10\ \Omega$). The second stage is biased at 0.25 mA/μm for improved linearity while source degeneration is omitted to achieve a higher gain.

Inductor L_S in the first stage was sized based on (5) and the value of f_{T} as obtained from Fig. 10. For the 30×90 nm $\times$ $1\ \mu$m cascode, $R_G = 3.3\ \Omega$ and $R_S = 200\ \Omega * \mu\text{m}/30\ \mu\text{m} = 6.7\ \Omega$. With an f_{T} of 87 GHz for the cascode with series inductor (Fig. 10), the inductor L_S was sized to be 60 pH for an input match to $\sim 40\ \Omega$.

The LNA layout consists of two sets of ground-signal-ground (GSG), $40\ \mu\text{m} \times 40\ \mu$m pads for the input and output signals, and a set of power-ground-power (PGP) pads for DC biasing. The 20-fF parasitic pad capacitance, obtained from previous test structure measurements, was accounted for in the design. Spiral inductors were implemented in the top metal layer to minimize substrate capacitance and maximize Q. ASITIC was used to simulate the Y-parameters as a function of frequency for all inductors and all interconnect. The interconnect is either directly added to the inductor before simulating in ASITIC the combined inductor with interconnect, or modeled separately with a $2-\pi$ equivalent circuit which is extracted from the simulated Y-parameters of the stand-alone interconnect.

The final LNA layout with pads measures only 0.35×0.4 mm^2 and is essentially pad-limited vertically. Four 2-pF MIM capacitors provide localized bias de-coupling. A large, slotted metal ground plane with ample substrate contacts was employed to reduce substrate resistance and ground inductance, while adhering to the metal density rules. The LNA chip micrograph is shown in Fig. 12.

C. Design Porting of Millimeter-Wave CMOS LNAs

The LNA design methodology presented here works very well across different foundries and technology nodes, since it is based on the current density biasing scheme at J_{OPT} which, together with the transistor capacitances per unity width, remains largely unchanged across foundries and technology nodes. As mentioned in Section II-B, even the passive inductor structures can be easily ported between foundries with minimal re-design given a similar backend metallization. As an illustration of the portability of this design methodology, the same LNA, without redesign, was transferred to another foundry and integrated into a 90-nm CMOS radio receiver operating at 60 GHz [5]. The same design methodology was also applied to a single-stage 60-GHz cascode LNA test structure fabricated in a different 90-nm CMOS process, which exhibited good agreement between measurement and simulation. Both the receiver and single-stage cascode LNA are discussed in more detail in Section V-A. An in-depth treatment of CMOS LNA scaling to different frequencies in the 12 GHz [23] to 94 GHz [22] range and porting to other technology nodes without re-design is presented elsewhere [23].

IV. 60-GHz PA Design

A. Millimeter-Wave Class-A PA Design Considerations and Methodology

Successful integration of the PA at 60 GHz relies on minimizing parasitic losses to maintain adequate gain (in light of the lower transistor MAG at mm-waves), designing with low voltage swings for low breakdown devices, and achieving sufficient linearity required for spectrally efficient, variable envelope modulation schemes proposed for 60-GHz applications.

The main design goals for the 60-GHz PA are captured in the PA FoM (6) as defined by the ITRS [16], which links the output power (P_{OUT}) with the gain (G) and power-added efficiency (PAE), while the f^2 term reflects the degradation in transistor gain and output power with increasing frequency:

$$\text{FoM}_{\text{PA}} = \text{P}_{\text{OUT}} \times G \times \text{PAE} \times f^2 [16] \tag{6}$$

Multi-stage PA topologies are essential to obtain adequate gain at mm-waves. This is especially true in the case of CMOS, where the $\sim$8 dB MAG of a 90 nm MOSFET is degraded by 3–4 dB due to the limited load impedance that can be realized at the drain output at high frequencies, and the losses in the matching networks. The optimal distribution of power gain and bias current (and hence $\text{P}_{1\text{dB}}$) between the stages of the PA can be obtained using the well-known expression for linearity in a cascaded system:

$$\frac{1}{OP1\text{dB}_{\text{cascade}}} = \frac{1}{OP1\text{dB}_3} + \frac{1}{OP1\text{dB}_2 \cdot G_3} + \frac{1}{OP1\text{dB}_1 \cdot G_2 \cdot G_3}. \tag{7}$$

The reduction in breakdown voltage with continued scaling dictates the need for larger bias currents to achieve the same output power as in earlier technology nodes. This, in conjunction with the constant-current-density biasing scheme, leads to larger device sizes and hence smaller output impedances (R_{OUT}), which complicates the output matching process. It gives III–V technologies and SiGe HBTs a clear advantage in PA design, since their higher breakdown voltage permits much lower bias currents and hence smaller devices, simplifying the matching to 50 Ω.

An algorithmic design methodology of a linear, Class-A PA at mm-waves can be developed based on load line theory [24] and constant-current-density biasing for optimal linearity. This is summarized in the six steps outlined below:

Step 1) Starting at the output stage, determine the maximum allowed voltage swing for the given technology. From load line theory, the optimal linearity and output power are obtained when the transistor (with inductive load) is biased such that the drain voltage swings equally between $V_{\mathrm{DS,sat}}$ and V_{MAX} (dictated by the device breakdown or reliability limit), centered at V_{DD}. Thus, the maximum voltage swing is $V_{\mathrm{swing}} = V_{\mathrm{MAX}} - V_{\mathrm{DS,sat}}$, where $V_{\mathrm{MAX}} = 2V_{\mathrm{DD}} - V_{\mathrm{DS,sat}}$.

Step 2) Set the bias current density to 0.3 mA/μm to maximize linearity.

Step 3) Determine the bias current that meets the $\mathrm{P_{1dB}}$ requirements, and from that find the transistor width. An expression for $\mathrm{P_{1dB}}$ can be derived from load line theory:

$$\mathrm{P_{max}} = \frac{I_{\mathrm{pk}} \times V_{\mathrm{pk}}}{2} = \frac{I_{DC} \times (V_{\mathrm{DD}} - V_{\mathrm{DS,sat}})}{2} \tag{8}$$

Using $I_{\mathrm{swing}} = (0.4\ \mathrm{mA_{pp}}/\mu\mathrm{m}) * W$, the maximum current swing before 1 dB compression, instead of $2 * I_{DC}$, we obtain the equivalent $\mathrm{P_{1dB}}$ equation, where $I_{\mathrm{pk}} = I_{\mathrm{swing}}/2$:

$$\mathrm{P_{1dB}} = \frac{I_{\mathrm{swing}} \times (V_{\mathrm{DD}} - V_{\mathrm{DS,sat}})}{4} \tag{9}$$

The value of $V_{\mathrm{DS,sat}}$ corresponding to the optimal linearity bias point of 0.3 mA/μm is about 0.3 V. From (9) $W = 4 * \mathrm{P_{1dB}}/[0.4\ \mathrm{mA_{pp}}/\mu\mathrm{m} * (V_{\mathrm{DD}} - V_{\mathrm{DS,sat}})]$ and $I_{DC} = W \times 0.3\ \mathrm{mA}/\mu\mathrm{m}$ (Fig. 3(a)).

Step 4) Add an output matching network for the last stage and (if necessary) inter-stage matching networks for intermediate stages to maximize power transfer. Add a degenerating inductor L_S to satisfy the input linearity condition as determined by the MAG of this stage and V_{swing}. Iterations may be needed since L_S also changes MAG.

Step 5) Repeat (1–4) for each preceding stage with the V_{swing} determined by V_{input} for the subsequent stage, to avoid gain compression.

Step 6) Design the first stage to be input-matched to 50 Ω. A cascode topology may be used in the first stage for higher gain.

B. 60-GHz PA Circuit Description

Based on the above technique, a 60-GHz PA has been designed and fabricated. It consists of three single-ended, common-source stages biased in Class A. Although the cascode topology has higher gain, larger output impedance and flat $I_{\mathrm{DS}} - V_{\mathrm{DS}}$ characteristic, the single-transistor CS configuration is advantageous for the PA implementation due to the lower supply voltage required, leading to higher efficiency and good linearity. The main drawback of the single transistor topology is the reduced reverse isolation, which complicates the input/output matching process.

The PA was designed for nominal 1.2-V operation and a saturated power of 7 dBm. With $V_{\mathrm{DS,sat}} = 0.3$ V, the voltage amplitude at the output is $V_{\mathrm{DD}} - V_{\mathrm{DS,sat}} = 0.9$ V. The required current in the final stage for 7 dBm (5 mW) output power is then 11 mA (8). This leads to an output transistor gate width of 11 mA/(0.28 mA/μm) = 39 μm, which was rounded off to 40 μm in the design. Since power gain at 60 GHz is directly linked to f_{MAX}, the gate voltage swing cannot exceed 0.45 $\mathrm{V_{pp}}$ for the transistor to operate below the 1 dB power compression, as shown in Fig. 3(b). With an output swing of $2 \times 0.9\ \mathrm{V} = 1.8\ \mathrm{V_{pp}}$ and a transistor MAG at 60 GHz of 8 dB, the gate voltage swing is $1.8\ \mathrm{V_{pp}}/2.5 = 0.7\ \mathrm{V_{pp}}$, exceeding the $\mathrm{P_{1dB}}$ limit of 0.45 $\mathrm{V_{pp}}$ at the gate. Hence, inductive degeneration is needed to prevent the G-S junction from becoming nonlinear. The first and second stages were designed in a similar manner given the required output voltage swing and MAG. The first stage is biased at the peak f_{MAX} bias of 0.2 mA/μm to maximize gain. The second and third stages are biased at the optimal linearity current density of 0.28 mA/μm. The transistor widths are 32 μm(Q_1), 36 μm(Q_2) and 40 μm(Q_3) (Fig. 13).

The input matching network consists of the inductor L_{S1}, which sets the real part of the input impedance to 50 Ω, and L_{G1} which cancels the imaginary part of Z_{IN}, at 60 GHz, as in an LNA. The gain of the first stage is rather low due to the large degeneration inductor needed to match the input to 50 Ω. A 1-stage L-network consisting of the load inductor L_{D3} and capacitor C_{C3} is employed at the output. Simplicity in the matching networks is critical in minimizing series parasitics, whose effects are more pronounced at 60 GHz. Inter-stage matching is used to maximize power transfer across the stages, and consists of the 1-stage L-networks (L_D, C_C) at the output of the first and second stages, and the gate (L_G) and source (L_S) inductors of the second and third stages, where the source inductors also improve linearity. The schematic of the PA is shown in Fig. 13.

Many of the layout techniques employed in the LNA for reducing substrate noise, supply de-coupling and area efficiency were also employed for the PA. All spiral inductors were designed to be smaller than required to account for the inductance of the interconnects, which were determined using ASITIC and included in the post-layout simulations. The die measures only $0.35 \times 0.43\ \mathrm{mm^2}$ and is also pad-limited vertically. The PA chip micrograph is shown in Fig. 14.

V. Circuit Measurements

The LNA and the PA were implemented in a 90-nm RF CMOS process with 9 Cu layers, the top two of which are thick. The f_{T} and f_{MAX} of 90-nm nMOSFETs with 1 μm wide fingers are 120 GHz and 200 GHz, respectively, at $V_{\mathrm{DS}} = 0.7$ V.

A. 60-GHz LNA Results

The simulated and measured S-parameters of 3 different LNA dies are shown in Fig. 15. All on-wafer S-parameter measurements up to 65 GHz were performed with a Wiltron 360B VNA and Cascade Microtech device probes. Calibrations to the probe

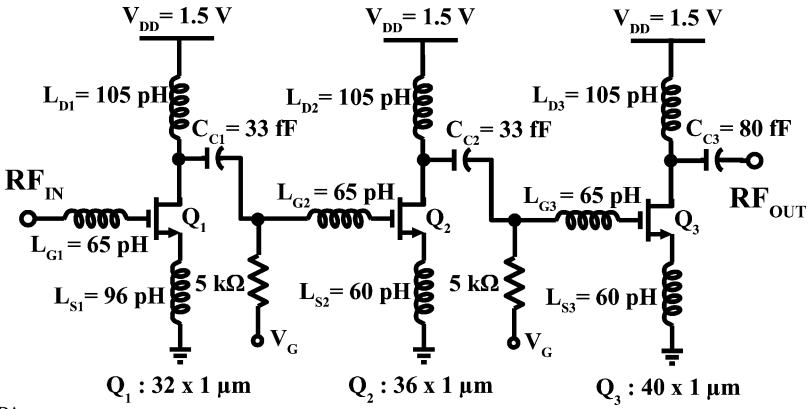

Fig. 13. Schematic of 60-GHz PA.

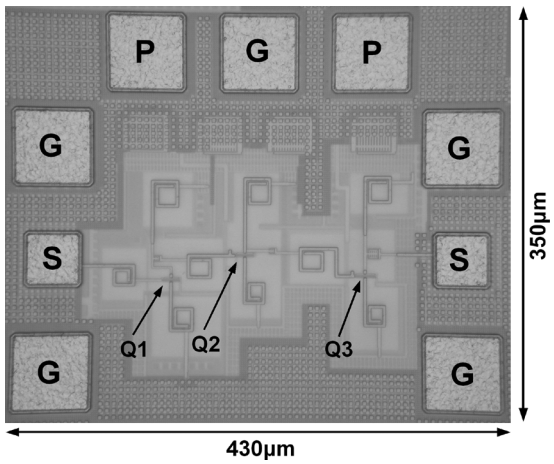

Fig. 14. Die micrograph of 60-GHz PA ($350\ \mu\text{m} \times 430\ \mu\text{m}$).

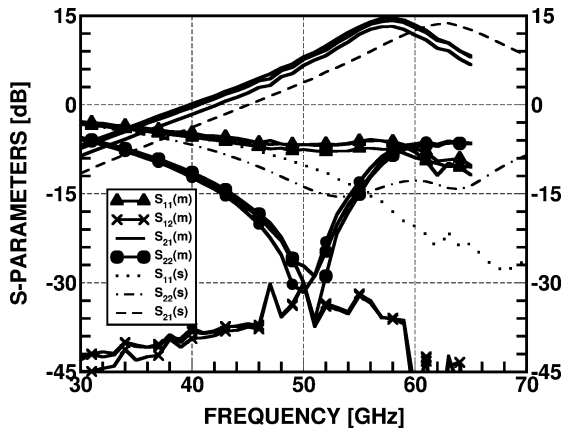

Fig. 15. Measured (m) and simulated (s) LNA S-parameters (measured across three different dies).

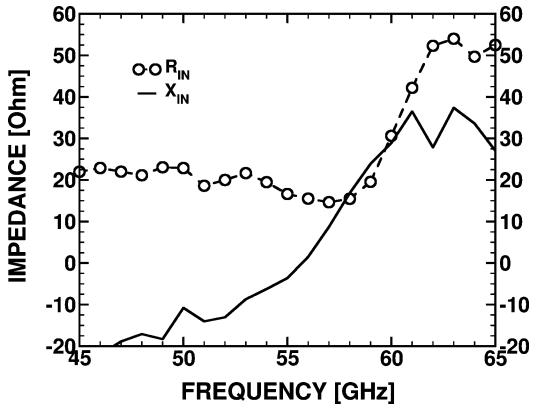

Fig. 16. Measured real and imaginary input impedance of LNA versus frequency.

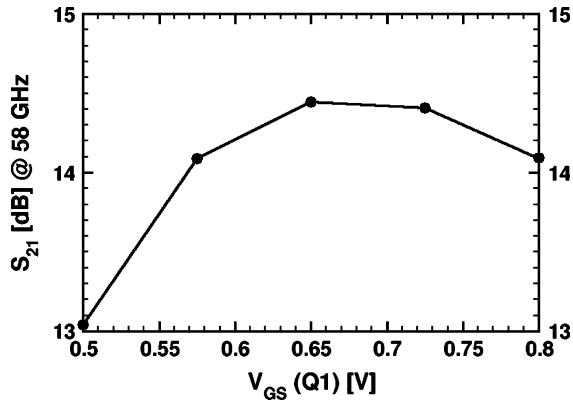

Fig. 17. Measured LNA S_{21} at 58 GHz as a function of V_{GS} of input transistor Q1.

tips were performed using the LRM (Line-Reflect-Match) algorithm, available in the WinCal software from Cascade Microtech. Since the pad capacitances were accounted for during design, they were not de-embedded from the measurements. The LNA achieves a measured peak gain of 14.6 dB at 58 GHz (within 7% of the target of 62.4 GHz) and an isolation of better than 32 dB. Both S_{11} and S_{22} are < -6 dB in the 50–65 GHz range. In simulation, the LNA has a peak gain of 14 dB centered at 62.4 GHz, while both S_{11} and S_{22} are < -10 dB in the 50–65 GHz range. The simulated isolation is also better than 50 dB.

The down-shift in the center frequency for S_{11} is mainly attributed to a lack of *RC* parasitic extraction tool. Thus, L_G was overestimated which, in turn, led to the input impedance resonance occurring at 56 GHz rather than at 61.5 GHz (Fig. 16). The input resistance is 50–55 Ω in the 62–65 GHz range. Because the output stage is a high-impedance, high-Q cascode, any parasitic capacitance associated with the MIM capacitor C_{C2} and with the interconnect has a big impact on S_{22}.

Plots of the LNA gain versus the gate bias of Q_1 and versus temperature are shown in Fig. 17 and Fig. 18, respectively. Robustness to V_{GS} variation is illustrated in Fig. 17, where the S_{21} of the entire LNA changes only by 0.3 dB from 14.1 dB to

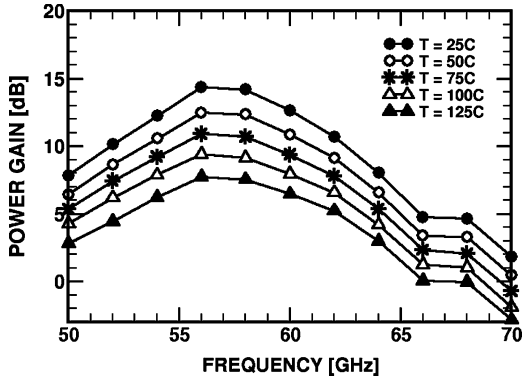

Fig. 18. Measured LNA power gain versus frequency over temperature.

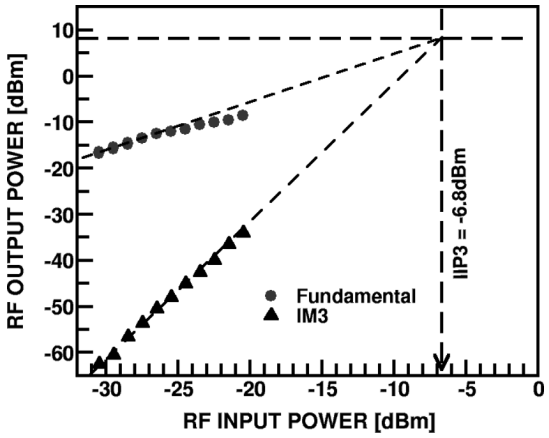

Fig. 19. Measured LNA $\mathrm{IIP_3}$ with 50-MHz tone spacing.

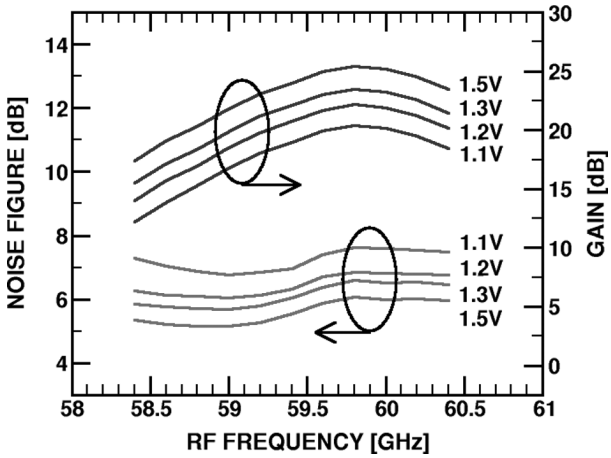

Fig. 20. Measured 60 GHz CMOS receiver gain and NF versus frequency, for different supply voltages.

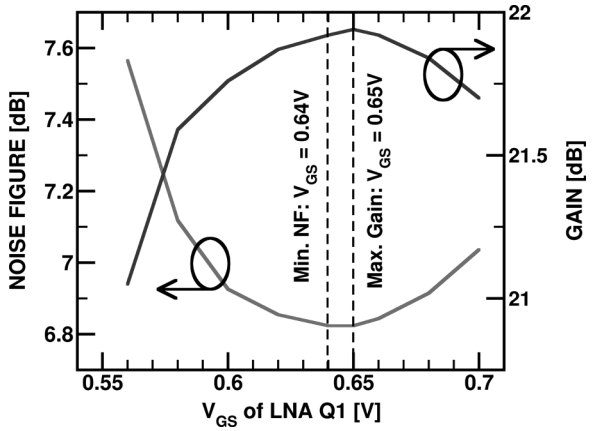

Fig. 21. Measured 60 GHz CMOS receiver NF and gain versus V_{GS} of LNA Q1.

14.4 dB when the gate voltage of the input MOSFET is changed from 0.575 mV to 0.8 V (corresponding to current densities of 0.1 mA/μm to 0.4 mA/μm). The measured $\mathrm{S_{21}}$ decreases by 3 dB between 25 °C and 75 °C, and by an additional 4 dB between 75 °C and 125 °C (Fig. 18). While this temperature dependence is twice as large as that measured on 80 GHz LNAs and PAs implemented in a 290-GHz SiGe HBT technology [25], it is comparable to that of published 60-GHz SiGe BiCMOS circuits [4], [32]. Linearity measurements show an output $\mathrm{P_{1dB}}$ of -0.5 dBm and an $\mathrm{IIP_3}$ of -6.8 dBm at 58 GHz, with a 50-MHz tone spacing used in the $\mathrm{IIP_3}$ measurement (Fig. 19).

The LNA noise figure could not be measured at 60 GHz due to lack of a down-convert mixer at this frequency. Instead, the noise parameters of a 90-nm nMOSFET cascode test structure were measured in the 10–26 GHz range using a Focus Microwaves system. The gate resistance was added to the digital transistor model to match both the measured noise figure of the transistor and of the cascode stage in the 10–26 GHz range, and the measured f_{MAX} of the transistor. The noise figure simulations for the cascode were found to be in good agreement with measurements in the 10–26 GHz range. After allowing for measurement scatter, the simulated 60-GHz $\mathrm{NF_{MIN}}$ of the cascode stage using this fitted model lies between 2.8 dB and 3.6 dB, while the simulated noise figure of the entire LNA is 4.5 dB at 60 GHz.

The simulated noise figure value is supported by the experimental demonstration of an integrated 60-GHz radio receiver implemented in a fully compatible 90-nm CMOS process with digital (rather than RF) back-end [5], employing the identical 2-stage cascode LNA. Transistor f_{T}, f_{MAX}, and noise parameter measurements up to 26 GHz, have been carried out for both processes, showing less than 0.1 dB differences in noise figure [23], [26] and less than 10% variation in f_{T} and f_{MAX}. The receiver also includes LO and IF buffers, and a double-balanced Gilbert cell mixer [5]. The double-sideband noise figure $\mathrm{NF_{DSB}}$ of the entire receiver was measured at 60 GHz as a function of LO power and bias supply voltage. For 1.5-V operation (as in the present LNA), the measured $\mathrm{NF_{DSB}}$ of the receiver is less than 5.5 dB in the LNA center frequency range of 58–59 GHz (Fig. 20). Thus, we can reasonably conclude that the LNA NF must also be $<$5.5 dB. More accurately, given that the LNA has a peak gain of 14.6 dB, and the mixer has a simulated $\mathrm{NF_{DSB}}$ of 14 dB, the NF of the LNA is lower than 5 dB. This figure is based on an analysis using the Friis formula for noise figure in a cascaded system.

Additionally, a plot of the measured receiver $\mathrm{NF_{DSB}}$ and gain versus the V_{GS} of transistor $\mathrm{Q_1}$ in the LNA (Fig. 21) confirms that the optimal NF occurs just below the maximum gain bias. The noise figure of the entire receiver changes by less than 0.1 dB around 6.5 dB, when the V_{GS} of the input transistor in the

TABLE I
90-nm LNA PERFORMANCE COMPARISON WITH STATE-OF-THE-ART USING THE LNA FoM IN UNITS OF GHz

LNA Technology	*f* [GHz]	*G* [dB]	*NF* [dB]	*IIP3* [dBm]	P_{DC} [mW]	*Area* [mm^2]	*FoM*
160/160 GHz f_T/f_{MAX} SiGe HBT [1]	65	14	10.5 (sim)	-6	34 (2.5V)	0.3 x 0.4	1.2
200/290 GHz f_T/f_{MAX} SiGe HBT [2]	61.5	15	4.5	-8.5	10.8 (1.8V)	0.6 x 0.9	13.8
90/130 GHz f_T/f_{MAX} 130 nm CMOS [6]	60	12	8.8	-0.5 (sim)	54 (1.5V)	1.3 x 1.0	2.1
120/200 GHz f_T/f_{MAX} 90 nm CMOS (this work)	**58**	**14.6**	**< 5.5 dB**	**-6.8**	**24 (1.5V)**	**0.35 x 0.4**	**5.7**

LNA changes from 0.6 to 0.68 V. Similarly, the down-conversion gain (21.8 dB) changes by less than 0.3 dB for the same gate voltage variation, indicating that NF and gain vary little with the gate voltage. Note that a higher $\mathrm{NF_{DSB}}$ was measured in this case due to a reduced supply voltage (1.2 V) and a lower LO power than for the best $\mathrm{NF_{DSB}}$ measurement at 1.5 V. In the latter case, the highest LO power produced the lowest receiver NF, which most closely reflects the LNA NF. The similarity between the LNA in the receiver and the present LNA can be seen by re-examining Fig. 17, where the LNA gain peaks exactly at $V_{\mathrm{GS}}(\mathrm{Q1}) = 0.65\ \mathrm{V}$, as in the receiver (Fig. 21). Finally, Table I shows a comparison of mm-wave LNAs in silicon using the FoM as defined by the ITRS [16]. The LNA presented in this paper achieves the highest FoM among all previous implementations in technologies with lower or comparable f_{T}, f_{MAX} performance.

To validate the accuracy of the proposed LNA design algorithm when extraction of layout parasitics *is* available and to illustrate its portability across foundries [22], Fig. 22 shows the measured and simulated S-parameters of a single-stage cascode LNA test structure fabricated in a 90-nm CMOS process from another foundry. This LNA was targeted at 60 GHz as part of an exercise in scaling circuits from 14 GHz to 28 GHz and to 60 GHz simply by scaling the gate width and bias currents of MOSFETs and the inductor values according to the ratio of the center frequency of the LNAs [22]. Simulations were conducted with digital MOSFET models to which R_G was added as an external element. The 60-GHz LNA test structure employs the same topology with tuning inductor L_M as in Fig. 9, and consumes 3 mA from a 1.5-V supply. The MOSFETs have $20 \times 1\ \mu$m gate width and are biased at $J_{\mathrm{OPT}} = 0.15\ \mathrm{mA}/\mu\mathrm{m}$. Inductors L_S, L_G, L_D, L_M are 55 pH, 190 pH, 140 pH and 190 pH, respectively. Measured $\mathrm{S_{11}}$ and $\mathrm{S_{22}}$ are simultaneously below -20 dB in the 56–60 GHz range. The input impedance match is broadband with the input return loss being better than -15 dB from 50 GHz to 65 GHz. While both LNAs were designed using the same algorithm as presented in Section III-A, the availability of an *RC* parasitic extraction tool in the design kit for this process resulted in a more accurate modeling of transistor and interconnect parasitics, leading to a better agreement between measurement and simulation (with extraction). Note that, as expected from (5), the input resistance match can be performed for a range of device widths. It is only the noise impedance that depends on the size of the input MOSFET.

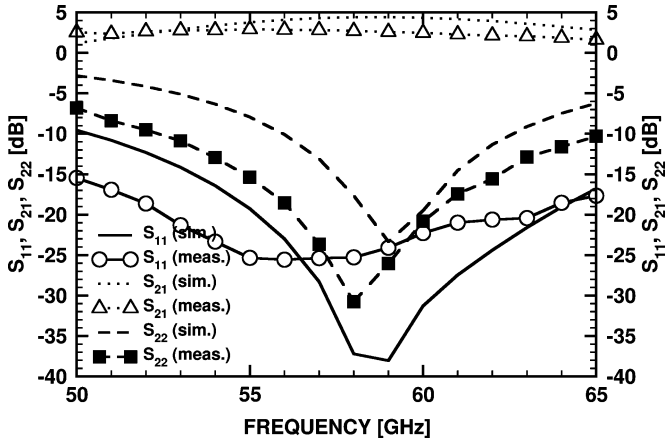

Fig. 22. (a) Measured and simulated S-parameters for a 60-GHz single-stage cascode LNA in a different 90-nm CMOS process.

B. 60-GHz PA Results

The simulated and measured PA gain and return loss are shown in Fig. 23(a). Measured S-parameters for three PA samples show good repeatability across dies. With a 1.5-V supply, the amplifier has a peak gain of 5.2 dB at 61 GHz, a 3-dB BW exceeding 13 GHz (52–65 GHz), with the upper frequency limit being imposed by the operating range of the VNA. Broadband matching is achieved at the output, with $\mathrm{S_{22}} < -10$ dB over the 51–65 GHz band, while $\mathrm{S_{11}}$ is < -10 dB in the 60–65 GHz range. The measured isolation $(\mathrm{S_{12}})$ is better than 30 dB in the entire measurement range Fig. 23(b). The 3 dB degradation between simulated and measured $\mathrm{S_{21}}$ at 60 GHz is mainly attributed to the lack of a parasitic *RC* extractor. While the inductors and all interconnect inductances were modeled using ASITIC and included in the post-layout simulation, the parasitic capacitance and via resistances on and around the transistors, and in the meshed ground plain, could not be extracted, and may contribute to the gain degradation. Unlike in the case of the LNA, the CS output stage in the PA provides a low-Q impedance, leading to a better agreement between measurements and simulation, despite a lack of parasitic extraction tool, with $\mathrm{X_{OUT}}$ resonating at exactly 62 GHz (Fig. 24).

Fig. 25 shows the large-signal performance of the PA, where an output $\mathrm{P_{1dB}}$ of $+6.4$ dBm and a saturated output power of $+9.3$ dBm were measured at 60 GHz, with a 1.5-V supply and total current of 26.5 mA. The measured output power agrees

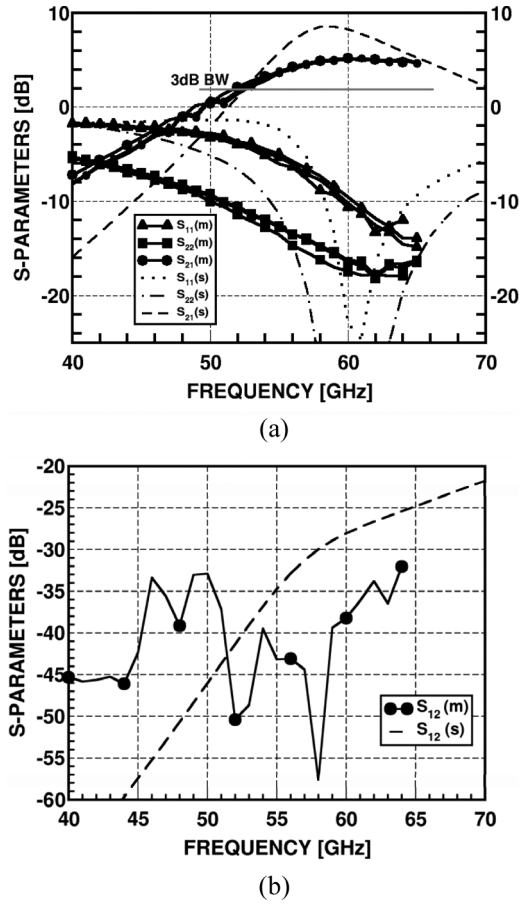

Fig. 23. (a) Measured (m) and simulated (s) PA S_{11}, S_{22}, S_{21} (measured across three different dice). (b) Measured and simulated PA S_{12}.

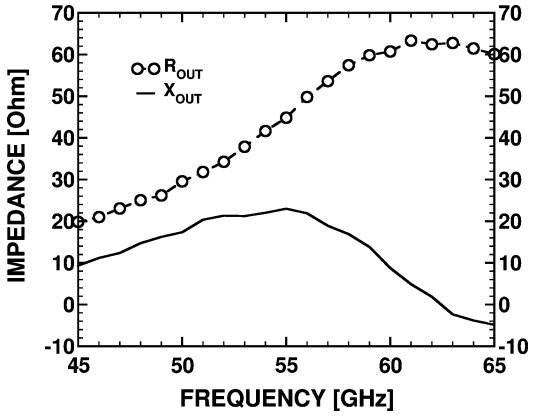

Fig. 24. Measured real and imaginary output impedance of PA versus frequency.

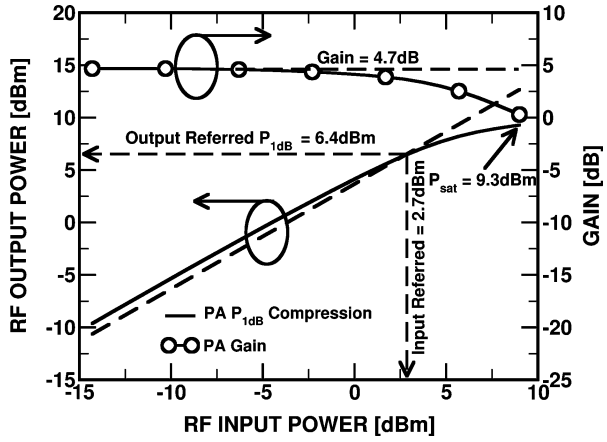

Fig. 25. Measured PA P_{1dB} at 60 GHz.

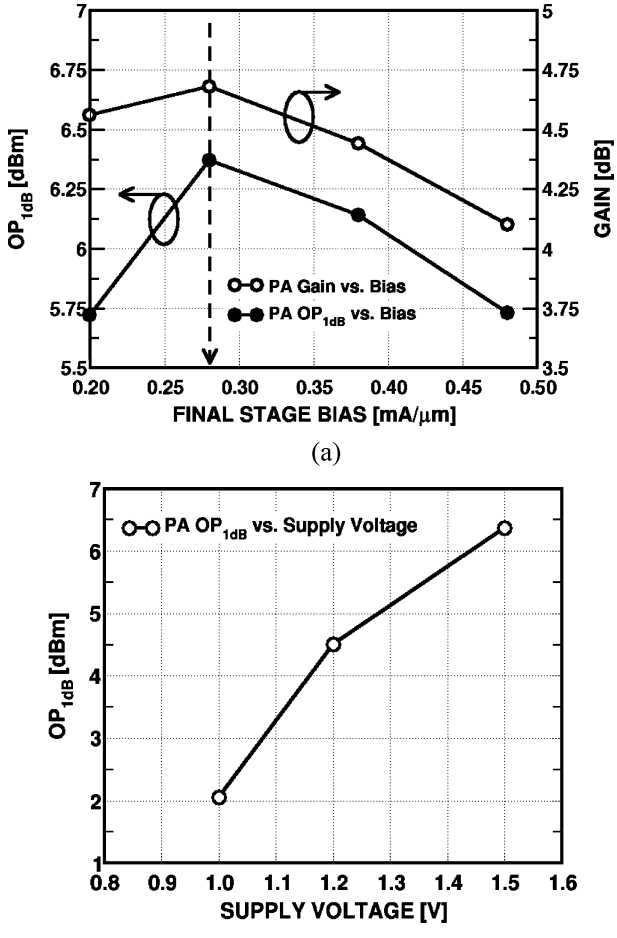

Fig. 26. (a) Measured PA P_{1dB}, gain versus final stage bias at 60 GHz. (b) Measured PA P_{1dB} versus supply at 60 GHz.

well with hand analysis, which predicts a P_{1dB} of 6.8 dBm for 1.5-V supply (8). The linearity and gain dependence on the bias current of the final stage are shown in Fig. 26(a), where the maximum gain and linearity occur when the final stage is biased at 0.28 mA/μm, close to the peak f_T bias (0.3 mA/μm). The output P_{1dB} varies almost linearly with the supply voltage, as shown in Fig. 26(b), indicating that the PA linearity is primarily limited by the supply voltage and by the V_{DS}-dependence of f_{MAX}, and not by the gate-source diode of the output transistor. A maximum PAE of 7.4% and a maximum drain efficiency of 21.4% were achieved. The gain, and hence PAE, can be further improved by replacing the first CS stage with a cascode stage, while maintaining the same power supply.

Table II provides a comparison of the PA in this work with previously reported mm-wave PAs in terms of the PA FoM, as defined in Section IV-A, using P_{sat} rather than OP_{1dB} to accommodate the data reported in literature. It can be seen that

TABLE II
90-nm PA PERFORMANCE COMPARISON WITH STATE-OF-THE-ART USING THE PA FOM IN UNITS OF [W • GHz]

PA Technology	*f* [GHz]	*G* [dB]	P_{sat} [dBm]	$P_{1dB,\,out}$ [dBm]	*PAE* [%]	*Area* [mm^2]	*Topology*	*FoM*
200/290 GHz f_T/f_{MAX} SiGe HBT [2]	60	10.8	16	11.2	4.3	2.1 x 0.8	2-stage CE (D)	74.3
200/240 GHz f_T/f_{MAX} SiGe HBT [27]	60	18	20	13.1	12.7	1.3 x 0.75	1-stage cascode (D)	2885
200/290GHz f_T/f_{MAX} SiGe HBT [28]	77	17	17.5	14.5	12.8	1.35 x 0.45	4-stage CE (S)	2137
200/290GHz f_T/f_{MAX} SiGe HBT [29]	77	6.1	12.5	11.6	3.5	2.1 x 0.75	2-stage CE (D)	9.1
65GHz f_{MAX} 0.18μm CMOS [30]	24	7	14.5	-	14.5	0.7 x 1.8	2-stage cascode (S)	11.7
84GHz f_{MAX} 0.18μm CMOS [31]	27	17	14	-	8.2	1.2 x 1.7	3-stage cascode (S)	74.7
84GHz f_{MAX} 0.18μm CMOS [31]	40	7	10.4	-	2.9	1.2 x 1.7	3-stage cascode (S)	2.6
120/200GHz f_T/f_{MAX} 90nm CMOS (this work)	**60**	**5.2**	**9.3**	**6.4**	**7.4**	**0.35 x 0.43**	**3-stage CS (S)**	**7.5**

this marks the highest frequency PA in CMOS reported to date, while also having the lowest area consumption due to the use of small form factor spiral inductors for on-chip matching. Its gain and $\mathrm{P_{sat}}$ are comparable to those of early 77 GHz SiGe [29] and 40 GHz CMOS PAs [31]. However, the CMOS PA performance remains markedly inferior to that of the most recent SiGe HBT PAs [25], [27], [28].

VI. CONCLUSION

A 60-GHz LNA and a 60-GHz PA have been demonstrated in 90-nm RF-CMOS. Algorithmic design methodologies were developed for mm-wave CMOS LNAs and PAs, based on constant-current-density-biasing. These amplifiers exploit the invariance of the optimum linearity, minimum $\mathrm{NF_{MIN}}$, and peak f_{MAX} current densities across technology nodes. The 2-stage cascode LNA represents the first 60-GHz LNA in the 90-nm node, and exhibits significant improvements in noise, gain and power consumption compared to existing mm-wave LNAs implemented in SiGe BiCMOS and CMOS processes with comparable f_{T}, f_{MAX}. Further performance enhancements are enabled by the addition of broadbanding inductors in each cascode stage, which form artificial transmission lines that boost the gain while lowering the noise figure. The successful integration of the LNA in a 60-GHz 90-nm CMOS receiver fabricated in a process from a different foundry, and the application of the design algorithm to a single-stage 60-GHz 90-nm CMOS LNA, also from another foundry, provide evidence to its design portability. The 3-stage common source PA represents the first 60-GHz CMOS implementation and demonstrates the potential of nanoscale CMOS for high-linearity applications. Both amplifiers have shown that trusted topologies based on lumped inductors and design methodologies from lower frequencies can be successfully extended to mm-waves.

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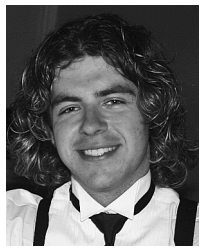

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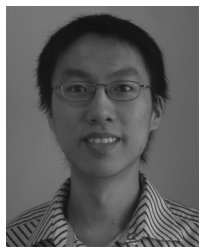

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