A Low-Noise 40-GS/s Continuous-Time Bandpass $\Delta\Sigma$ ADC Centered at 2 GHz for Direct Sampling Receivers

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***Abstract*—This paper presents a 40-GS/s continuous-time bandpass $\Delta\Sigma$ analog-to-digital converter centered at 2 GHz for wireless base station applications. The ADC consists of a fourth-order loop with multiple feedback and is designed entirely in the s-domain. The circuit achieves an SNDR of 55 dB and 52 dB over bandwidths of 60 MHz and 120 MHz, respectively, and an SFDR of 61 dB with a single-ended IIP3 of $+4$ dBm. The center frequency is tunable from 1.8 to 2 GHz. It employs a G_m–$LC_{\rm VAR}$ filter based on a MOS-HBT cascode transconductor with an $\rm NF_{MIN}$ of 2.29 dB. The entire circuit is implemented in a 130-nm SiGe BiCMOS technology with 150-GHz f_T SiGe HBT and dissipates 1.6 W from a 2.5-V supply.**

***Index Terms*—Analog-to-digital converter, continuous-time, delta-sigma, direct RF sampling, SiGe BiCMOS.**

I. Introduction

ADVANCES in silicon technologies have led to transistors having f_T and $f_{\rm MAX}$ in excess of 150 GHz. With these devices, it becomes feasible to directly digitize the RF carrier. The main benefit of a direct sampling receiver is the flexibility it provides to process the entire system bandwidth in the digital domain, while replacing most of the analog circuitry used for downconversion and filtering. Channel selection can be performed by digital filters, which are relatively easy to implement in sub-100-nm technologies. This trend is captured in the radio receiver architecture shown in Fig. 1, with the digital receiver directly following the antenna and duplexer. This topology achieves direct digitization without using subsampling mixing [1], [2], which is known to increase the receiver noise figure (NF) [3], and without analog downconversion [4]. In comparison to Fig. 1, the receivers of [1], [2], and [4] support only a single radio channel.

This paper describes a direct digitizer for 2-GHz radio systems implemented as a continuous-time $\Delta\Sigma$ ADC. Since the power supply voltage follows the ever-decreasing breakdown voltage of transistors in advanced technology nodes, one must take advantage of the faster response of transistors and compensate for the reduced signal amplitude by exploiting timing information. $\Delta\Sigma$ modulators ($\Delta\Sigma$M) are an attractive solution for direct sampling receivers, because they trade off resolution in amplitude for resolution in time, while having high resolution, low power and low complexity compared to other ADC types. They can potentially replace the analog blocks (excepting the VCO/PLL) of a wireless receiver, including the low-noise amplifier (LNA), and directly digitize the RF signal. Continuous-time bandpass $\Delta\Sigma$ ADCs centered between 0.8 to 1 GHz were reported in the 1990s, but insufficient transistor speeds resulted in inadequate circuit performance [5]–[7]. Unlike all previous $\Delta\Sigma$ ADCs, the proposed architecture incorporates the LNA in its main path, as the input stage of the loop filter. Compared to other bandpass ADC designs with GHz clocks [5]–[9] and operating from 3.3 V or higher supplies, this work employs a new, highly linear and low-noise MOS-HBT cascode filter topology, which is powered from a 2.5-V supply. To process the entire system bandwidth and have sufficient resolution, as required in a base station receiver, a large oversampling ratio (OSR) is needed. Although a bandpass $\Delta\Sigma$M clocked at 42.6 GHz has been demonstrated in [10], the circuit was implemented in a superconductive technology with Josephson junctions. The 40-GHz clock frequency in the present paper is two times larger than in any previously reported semiconductor $\Delta\Sigma$ ADCs, marking the first use of mm-wave clocks in silicon $\Delta\Sigma$M.

This paper is organized as follows. Section II presents the system level design methodology of the loop in s-domain. Circuit design is discussed in Section III, where the filter, DACs, quantizer and clock distribution topologies are analyzed. At the core of all circuits is the MOS-HBT cascode topology, which provides the best linearity, and the best frequency response in both the analog and digital parts of the chip. Finally, measurement results of a loop filter break-out and of the entire ADC are

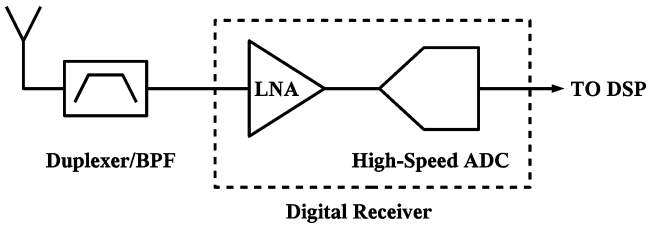

Fig. 1. Top level architecture of a digital receiver.

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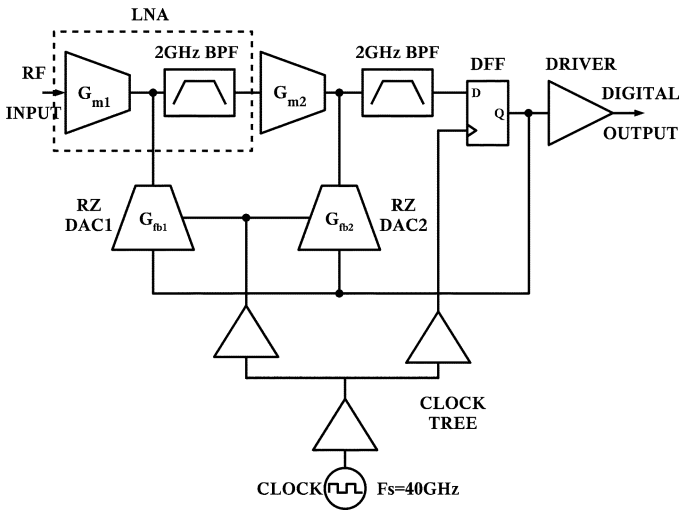

Fig. 2. System-level ADC block diagram.

summarized in Sections III and IV, respectively, along with a comparison to state-of-the-art GHz-sampling $\Delta\Sigma$ ADCs.

II. System-Level Design

Fig. 2 shows the system-level architecture of the $\Delta\Sigma$ ADC. It is based on a classical feedback topology with two resonators and two feedback paths. The bandpass loop filter consists of two G_m–LC stages. A master–slave–master D-type flip-flop with 5-ps rise and fall times [11] is used as comparator and quantizer. The single-bit quantizer is clocked at 40 GHz to create a large OSR such that the ADC can convert the full system bandwidth. Choosing a large OSR can also give an insight into the impact of clock jitter and loop delay to multi-GHz $\Delta\Sigma$M. Feedback is applied through two current steering return-to-zero (RZ) DACs. While the master–slave–master topology compensates for metastability, it introduces an additional half-clock cycle delay in comparison to a simple master–slave implementation. The tail currents of the feedback DACs were adjusted to ensure that the ADC is stable in the presence of excess loop delay [5]. A second technique that helps mitigate the impact of the delay is the choice of a RZ instead of non-return-to-zero (NRZ) pulse. A loop with RZ pulses can tolerate delays of up to half a clock cycle without signal-to-noise-and-distortion ratio (SNDR) degradation. This becomes important as clock frequencies exceed 1/5 of the transistor f_T [5]. Since the output digital stream has 40-Gb/s content, a 50-Ω driver with 50-GHz bandwidth [11] is employed to drive the signal off chip.

In continuous-time $\Delta\Sigma$M, the closed loop stability is traditionally analyzed in the z-domain. The coexistence of analog (loop filter) and digital (quantizer, DACs) components makes the design of such a circuit cumbersome in the s-domain. Typically, the design process starts from a discrete-time transfer function that satisfies the requirements in OSR, SNDR, and spurious-free dynamic range (SFDR). The loop filter is then transformed to its equivalent in the Laplace domain. In bandpass ADCs, the G_m–LC filter is the most popular approach when the center frequency is in the RF range. Such a circuit, however, cannot implement the z-to-s domain equivalence due to the inherent absence of a low-pass term in the transfer function of the bandpass filter. Historically, this problem has been addressed in two ways. The first approach [12] uses an optimization algorithm that tries to match the impulse response of the z and s-domain filters. Another approach [13] employs a modified quantizer that has half a clock cycle delay. The resulting loop filter can be made equivalent to its z-domain counterpart, due to the extra degrees of freedom inserted into the system by the two DAC pulses. This scheme, however, poses circuit implementation difficulties when the clock is in the GHz range. At mm-wave sampling speeds, it is difficult to maintain the phase delay between the two parallel DAC pulses.

A new method that bypasses the z-domain analysis is proposed here. The loop filter is directly designed in the s-domain using established analog filter design techniques. Stability is verified by employing a linear approximation of the quantizer. The design procedure begins with the derivation of the loop filter transfer function. The loop filter can be chosen to have a flat response in the passband and its transfer function can be derived either from a low-pass prototype [14], or directly in bandpass mode. The filter is centered at 2 GHz and covers the entire 60-MHz bandwidth of the CDMA system. The transfer function of a $G_m - LC$ filter with quality factor Q, center frequency ω_o, and gain constant A is

$$H(s) = \frac{A\omega_o s}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}. \tag{1}$$

Ideally, the two poles of each resonator should be placed close to the $j\omega$ axis to achieve large suppression of quantization noise. The ADC closed-loop transfer function with two resonators and two feedback DACs is described by (2), shown at the bottom of the page, where G_{m1}, G_{m2} are the transconductances of the bandpass filters and G_{fb1}, G_{fb2} are the transconductances of the DACs. For simplicity it has been assumed that the two stages are tuned to the same center frequency. The transfer function of the filter path is described by

$$H^2(s) = \frac{G_{m1}G_{m2}}{C^2}\frac{s^2}{\left(s^2 + \frac{\omega_o}{Q}s + \omega_o^2\right)^2} \tag{3}$$

$$G(s) = \frac{H^2(s)D(s)}{1 + \frac{H^2(s)D(s)}{s}\left[\frac{G_{fb2}C}{G_{m1}G_{m2}}s^2 + \left(\frac{G_{fb1}}{G_{m1}} + \frac{G_{fb2}C\omega_o/Q}{G_{m1}G_{m2}}\right)s + \frac{G_{fb2}C\omega_o^2}{G_{m1}G_{m2}}\right]} \tag{2}$$

and the RZ DAC transfer function is expressed as

$$D(s) = \frac{1 - e^{-sT_s/2}}{s}. \tag{4}$$

The two pairs of poles from (3) are located at

$$s_{1,2} = -\frac{\omega_o}{2Q} \pm j\omega_o\sqrt{1 - \frac{1}{4Q^2}}. \tag{5}$$

If the effect of the quantizer is ignored ($D(s) = 1$), the root locus method for stability analysis shows that the loop is unconditionally stable (i.e., poles do not enter the right half-plane). However, the quantizer must be taken into consideration in the design, because it introduces a variable gain element K in the loop. For small input signals, the system gain can increase and lead to the generation of limit cycles [15]. Equation (2) cannot be solved analytically for the evaluation of stability, due to the exponential term of the DAC transfer function. To overcome this issue, one solution is to estimate the poles and zeros numerically, as shown in [15], but this adds complexity to the design procedure. Instead, we can employ a rational function to approximate the quantizer/DAC transfer function $D(s)$. By using the Padé approximation [16], a linear system with delay τ_d can be expressed as

$$e^{-\tau_d s} \approx \frac{1 - \tau_d s/2 + (\tau_d s)^2/12}{1 + \tau_d s/2 + (\tau_d s)^2/12}. \tag{6}$$

The first-order approximation of the quantizer followed by a delay element is

$$D(s) \cdot e^{-\tau_d s} \approx \frac{T_s/2}{\left(1 + \frac{\tau_d}{2}s\right)\left(1 + \frac{\tau_d + T_S/2}{2}s\right)} \tag{7}$$

which describes mathematically the combination of the flip-flop and DAC, including the excess loop delay. The root locus of the modulator can now be plotted since the quantizer is approximated by a rational expression. Part of the root locus plot around the filter poles is reproduced in Fig. 3. The filter poles move from the values defined in (5) when the loop is open, and $K = 0$ (no feedback) to the position of zeros for an infinite gain in the loop as $K \to \infty$ (zero input signal to the modulator). As the gain in the loop increases due to the presence of the quantizer, one pair of the filter poles moves toward the $j\omega$-axis. For certain gain values, the loop can become unstable. This occurs when the poles enter the right half-plane for a gain of $K_{\max} = 4.3 \cdot 10^4$. In order to ensure stability of the system for low input signals, the total gain introduced by the quantizer must be smaller than $K_{\max}$. If the loop gain for small input signals is comparable to the maximum allowable gain, the feedback transconductances G_{fb} must be adjusted to reduce the closed loop gain.

The design methodology for the continuous-time bandpass ADC can be summarized in the following steps.

1) Design a bandpass filter in s-domain.
2) Map filter transfer function to circuit parameters (G_m, L, C, Q).
3) Check for stability with root locus method.
4) Adjust G_{fb} to account for excess loop delay.

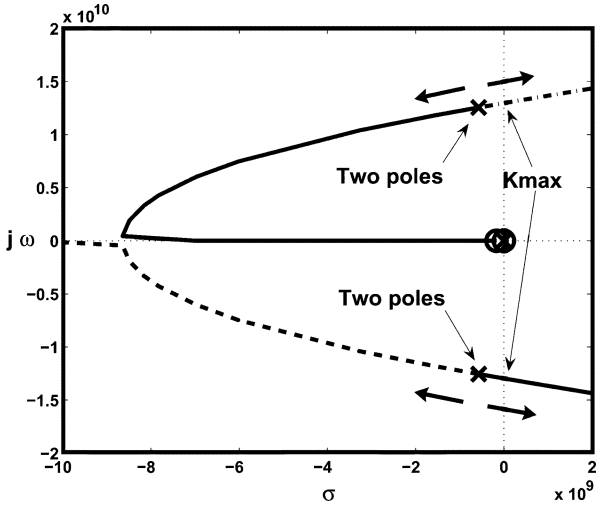

Fig. 3. Root locus of fourth-order bandpass ΔΣ ADC.

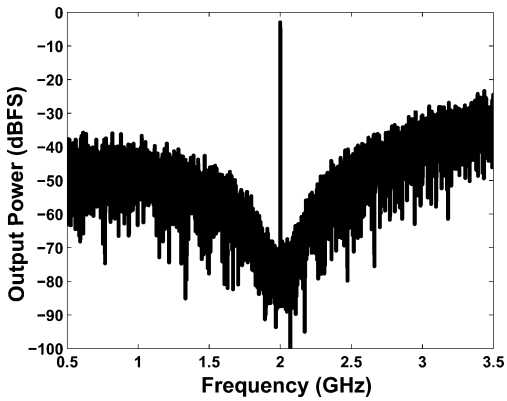

Fig. 4. System-level simulation of ΔΣ ADC ($N_{\mathrm{FFT}} = 65536$).

Following the derivation of the loop parameters, the system level model must be verified in a behavioral simulation. The fourth-order ΔΣM model was simulated in Matlab Simulink in order to capture the real effect of the quantizer. The final ADC parameters were $G_{m1} = 22$ mS, $G_{m2} = 10$ mS, $G_{fb1} = 50$ mS and $G_{fb2} = 150$ mS. The ADC achieves an SNDR $= 57$ dB over 60 MHz at 2 GHz (Fig. 4) and is able to recover its ΔΣ noise shaping after being overloaded with a full-scale (FS) input signal.

III. Circuit Design

A. Loop Filter

The circuit schematic of the fourth-order loop filter is shown in Fig. 5. The first stage serves as both the input transconductor G_{m1} and the receiver LNA. The filter tank consists of an LC–C_{VAR} combination, with $L_C = 3.8$ nH (differential) and $C_C = 2.3$ pF, such that

$$\omega_o = \frac{1}{\sqrt{(L_C/2)(C_C + C_{\mathrm{VAR}})}}. \tag{8}$$

The varactor was added to provide a means of adjusting the center frequency. Its capacitance C_{VAR} varies between 0.4 and 0.8 pF. It is significantly smaller than C_C in order to maintain a

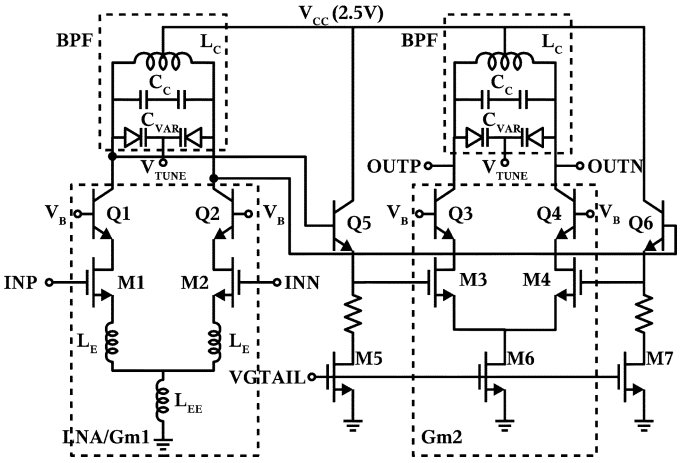

Fig. 5. Circuit schematic of 2-stage loop filter.

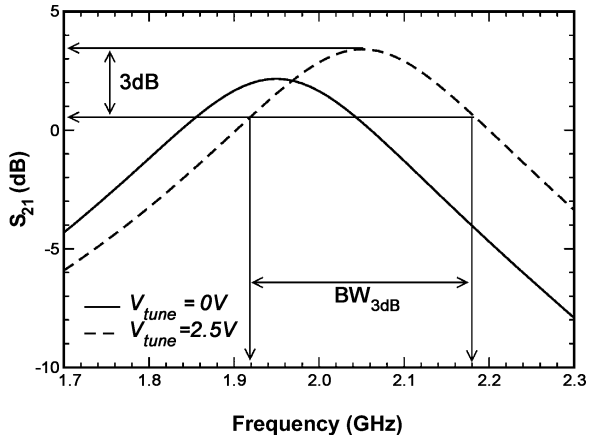

Fig. 6. Measured S_{21} of the filter test structure.

high quality factor Q while still providing more than 10% tunability at 2 GHz. The varactor control voltage $V_{\rm TUNE}$ is applied from an external power supply.

The combination of nMOSFET and HBT transistors in the cascode amplifier provides maximum linearity and isolation allowing for lower power supply than is otherwise possible with an HBT-only implementation. Since the design goal for the filter is linearity rather than gain, we take advantage of the excellent linearity of nMOSFETs when biased at the peak-g_m current density of 0.4 mA/μm. Under peak-g_m bias, the 130-nm nMOSFET exhibits 0.45 $V_{\rm pp}$ linear swing at its gate for 1-dB compression of g_m and does not require inductive or resistive source degeneration for improved linearity. The NF is only slightly degraded from its minimum value at 0.15 mA/μm [17]. A degenerated HBT-HBT cascode would increase the NF of the circuit for the same linearity. Furthermore, the linearity is improved over that of a MOS-MOS cascode by the higher output voltage swing and output resistance of the HBT in the MOS-HBT cascode. The degeneration inductor L_E is used to make the real part of the input impedance equal to 50 Ω, as in an LNA. The MOS-HBT cascode has an f_T of 80 GHz.

$$\Re(Z_{\rm in}) = \omega_T \cdot L_E$$
$$L_E = \frac{50\ \Omega}{2\pi 80\ \text{GHz}} = 100\ \text{pH}. \tag{9}$$

The common mode inductor L_{EE} suppresses the even order harmonics of the first transconductor with minimal noise contribution. A current source or a resistor could provide common mode rejection but at the expense of increased noise. Both filter stages are biased at the peak-g_m current density. The resistors at the drains of M5/M7 lower the $V_{\rm DS}$ across these transistors below 1.2 V.

Assuming a NF of 2 dB across a signal bandwidth of 60 MHz and an SNR $= E_b/N_o = 14$ dB for voice/data signals, the receiver sensitivity at room temperature without accounting for quantization noise is

$$P_S = -174\ \text{dBm/Hz} + \text{NF} + 10log_{10}BW + \text{SNR}$$
$$= -80.2\ \text{dBm}. \tag{10}$$

Based on the measured sensitivity of the flip-flop at 40 Gb/s [11], the minimum signal required at the input of the quantizer is 10 $\text{mV}_{\rm pp}$ per side. The LNA/filter must therefore amplify the minimum input signal up to at least 10 $\text{mV}_{\rm pp}$ at the first stage of the quantizer. The voltage gain of the two-stage filter must be larger than

$$A_V = \frac{V_{\rm out}}{V_{\rm in}} = \frac{5\ \text{mV}}{30.9\ \mu\text{V}} = 162. \tag{11}$$

Each *LC* filter tank has a Q of 11 and can be represented at resonance as a parallel *RLC* network with $R_P = Q\omega_o L = 262\ \Omega$, resulting in a voltage gain of the first stage $V_{\rm out}/V_{\rm in} = -g_m R_P = -6\ \text{V/V}$. The total gain of both stages is about 36. To reach the required $A_V = 162$, the filter Q must be further improved by a factor of 2. Therefore, we can conclude that the sensitivity of the present design is limited by the Q of the filters.

The linearity of the ADC is also determined by the voltage swing at the output of each amplifier stage. The maximum voltage swing at the collectors of Q1-Q2 should not drive the HBTs into saturation. Assuming a bias current I_C and $V_{CE,\rm SAT} = 0.3$ V, the maximum swing is

$$\Delta V_{\max} = \min\left\{I_C R_p, V_{CC} - (V_B - V_{BE} + V_{CE,\rm SAT})\right\} \tag{12}$$

or 2.6 $\text{V}_{\rm pp}$. For a single-ended gain of 6 and 2.6 V swing, the maximum allowable input signal is $V_{\rm in,max} = 0.44\ \text{V}_{\rm pp}$, corresponding to an input power of -3 dBm. This value is approximately equal to the receiver $P_{\rm 1dB}$, as will be shown in Section IV.

Single-ended S-parameter, NF and differential $P_{\rm 1dB}$ and IP3 measurements were performed on wafer on a separate filter test structure, identical to the one used in the ADC. Fig. 6 illustrates the tunability of the filter for two varactor control voltages $V_{\rm TUNE} = 0$ and 2.5 V. The minimum value of the measured $\text{NF}_{\rm MIN}$ is 2.29 dB at 2 GHz (Fig. 7). As can be seen in Fig. 8, the maximum value of the differential $P_{\rm 1dB,out}$ is 0.5 dBm and occurs at 0.4 mA/μm current density, which coincides with the flat region of the transistor $g_m - I_{\rm DS}$ transfer characteristic. The differential IIP3 and OIP3 of the filter are -0.5 dBm and 9 dBm, respectively, as can be found in Fig. 9. It should be noted that when used in the ADC, the filter linearity is higher than that of the test structure because of the feedback network.

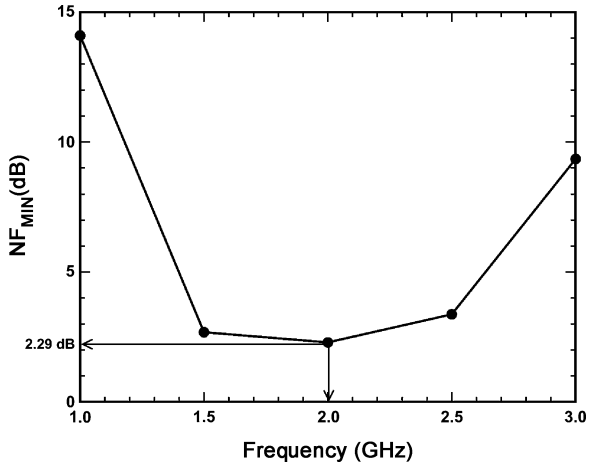

Fig. 7. Measured $\mathrm{NF_{MIN}}$ of the filter test structure.

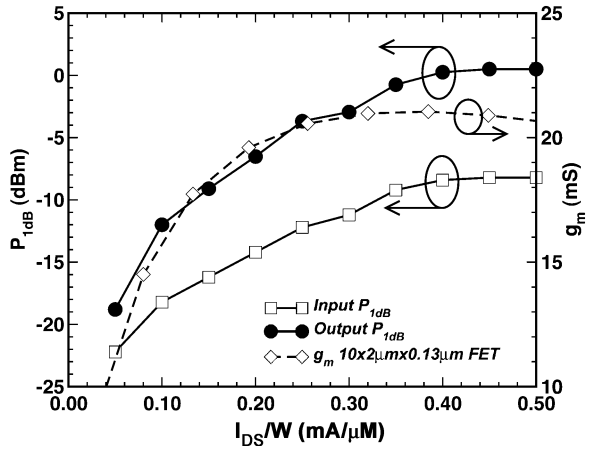

Fig. 8. Measured filter linearity and g_m of nMOSFET versus current density.

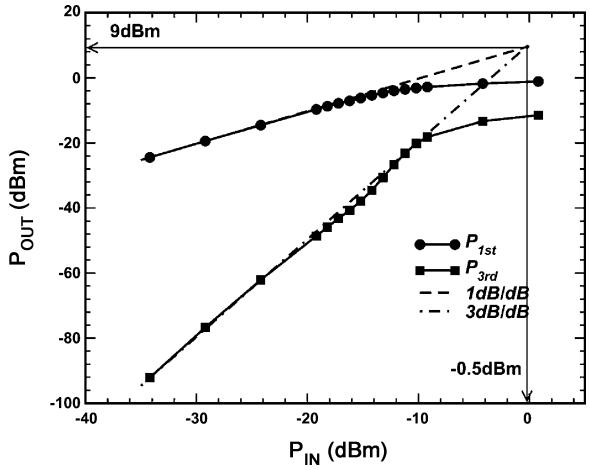

Fig. 9. Measured IP3 of the filter test structure.

B. Feedback DACs and Quantizer

Fig. 10 shows the DAC topology, similar to the one in [18] but implemented with MOS-HBT cascodes which allows it to operate from 2.5 V with improved frequency response. When both

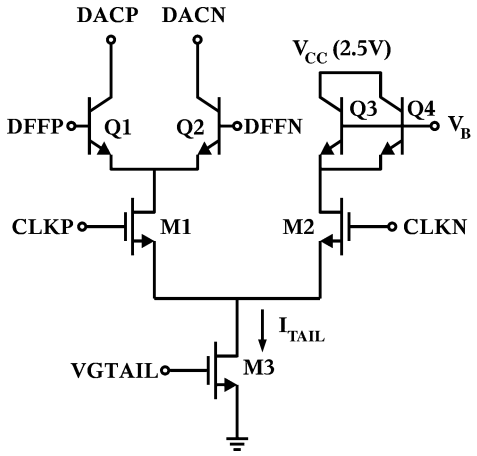

Fig. 10. Circuit schematic of RZ DAC.

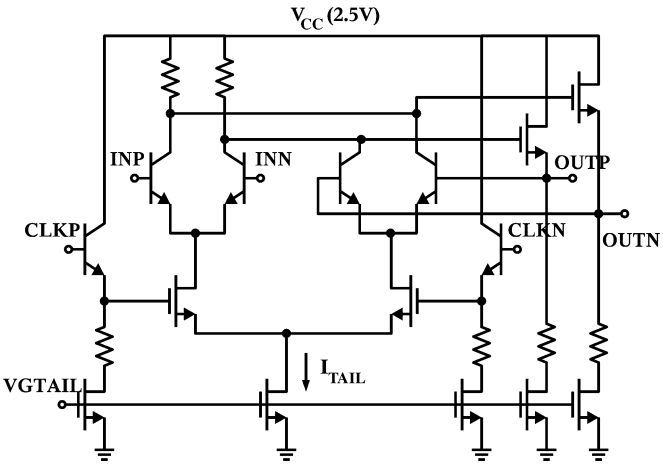

Fig. 11. Circuit schematic of latch.

M1 and one of Q1-Q2 turn on, I_{TAIL} flows though the nodes DACP or DACN and is subtracted from the feedback node, which is the collector of the MOS-HBT amplifier in the filter. The clock signal switches the differential pair M1-M2 and generates the RZ current waveform. The presence of HBTs Q1-Q2 provides a large g_m/I_{TAIL} ratio and reduces the voltage swing that is required at the quantizer output to fully switch the DACs. Transistors Q3-Q4 act as dummy loads to ensure the symmetry of the waveform.

The schematic of the latch used in the master–slave–master flip-flop is illustrated in Fig. 11. It is based on the same MOS-HBT cascode and has similar speed from a lower power supply [11] when compared to an HBT-only implementation. The HBTs provide large gain on the data path to reduce the effect of quantizer metastability. To fully switch the DACs and output driver, the voltage swing at the quantizer output must be higher than 300 $\mathrm{mV_{pp}}$. If the master–slave–master latches do not have adequate output swing, the DACs in the feedback loop of the ADC will not operate correctly. For a minimum input data swing of 10 $\mathrm{mV_{pp}}$, this requires a voltage gain of 30, which can only be realized by cascading at least three latches in a master–slave–master configuration.

For an $I_{\rm TAIL}$ of 14 mA and a load resistance R_L of 35 Ω, the data path gain of the latch (from the data input to the source follower) is

$$\text{Gain} = -g_m R_L = -\frac{I_{\rm TAIL}/2}{V_T} R_L = -10\ \text{V/V}. \qquad (13)$$

This value ignores the effect of the parasitic emitter resistance R_E, typically 3.5 Ω for a 8 μm × 0.17 μm HBT. The effective transconductance then becomes

$$g_{m,\text{eff}} = \frac{g_m}{1 + g_m R_E} \qquad (14)$$

and considering the 0.8 V/V gain in the source follower, the gain of the latch reduces to about 4. The HBT differential pair produces a voltage swing of 14 mA × 35 Ω = 490 $\text{mV}_{\rm pp}$, which is further attenuated to 400 $\text{mV}_{\rm pp}$ by the source follower pair. For this reason a master–slave–master flip-flop is employed with a total voltage gain of $4^3 = 64$. If a master–slave flip-flop had been employed, the gain would have been only 16 and the voltage swing before the driver and DACs would have been only 160 $\text{mV}_{\rm pp}$, which is inadequate to fully switch a bipolar differential pair with some emitter degeneration. This analysis gives a worst-case estimate of the signal gain in the latch. It assumes that the clock differential pair is switched to one side and the latch operates as an amplifier. In reality, the gain can be higher due to the finite regeneration inside the latch. As shown in [11], the flip-flop produces a high swing output for low input signals up to 45 Gb/s. From time domain simulations of the latch at 40 GHz, the large signal gain is 5.9 V/V and the regeneration time is 5.1 ps.

C. Clock Distribution Network and Output Driver

The external clock signal is distributed to the three latches and two DACs by a broadband clock tree. As depicted in Fig. 12, the clock network comprises a chain of MOS-HBT cascode inverters with series and shunt inductive peaking to extend its bandwidth beyond 40 GHz. The number of stages is determined by the load that the clock tree drives. Due to the existence of delay around the loop and accounting for the subsequent adjustment of the tail currents in the feedback DACs, the flip-flop fanout was increased to ensure that the DACs and output driver switch completely. The resulting total tail currents in the flip-flop and DACs are 62 mA and 60 mA, respectively. Fig. 12 shows the current consumption of each MOS-HBT inverter, including the emitter-follower differential pair, for a scaling factor of about 1.5 between successive stages.

The clock distribution network operates as a chain of CML inverters each with a gain of 1.5. The minimum voltage swing to switch the 130-nm MOS differential pair biased for maximum switching speed is 400 $\text{mV}_{\rm pp}$ [17]. For a tail current of 3 mA, the MOS-HBT inverter (Fig. 12) has a swing $\Delta V = 1.5 \times 400\ \text{mV}_{\rm pp} = 600\ \text{mV}_{\rm pp}$ and a load resistance $R = \Delta V / I_{\rm TAIL} = 200\ \Omega$. The cascode is biased at peak-f_T current density when the entire $I_{\rm TAIL}$ is steered through one side. The bandwidth of the MOS-HBT inverter can be estimated if the total capacitance C_T at the collector node of Q_1 is known.

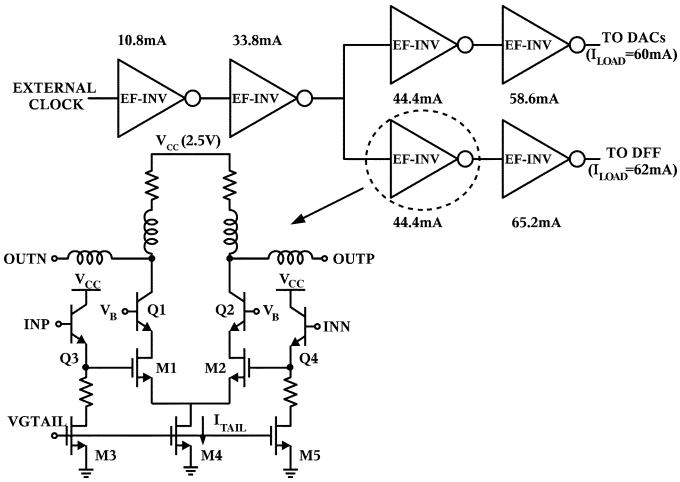

Fig. 12. Block diagram of clock distribution tree and schematic of emitter-follower MOS-HBT inverter.

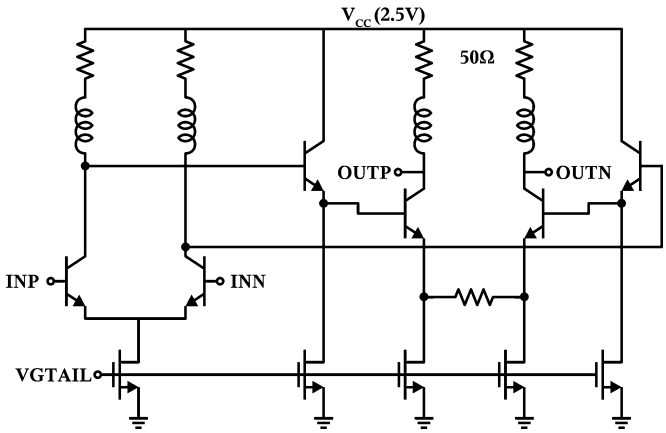

Fig. 13. Circuit schematic of 50-Ω output driver.

For the MOS-HBT inverter of Fig. 12 with 10 μm × 0.13 μm MOSFETs, 1.5 μm × 0.17 μm HBT in the cascode and 2.9 μm × 0.17 μm HBT in the emitter-follower, C_T can be estimated as

$$C_T = C_{\mu,Q1} + C_{CS,Q1} + C_L = 32.5\ \text{fF} \qquad (15)$$

where C_L is the capacitive load of the next stage

$$C_L = C_{\mu,Q3} + \frac{C_{\pi,Q3} C_{\rm MOS}}{C_{\pi,Q3} + C_{\rm MOS}} \qquad (16)$$

and

$$C_{\rm MOS} = C_{gs,M1} + C_{gd,M1} + C_{gd,M3} + C_{db,M3} = 38\ \text{fF}. \qquad (17)$$

The 3-dB bandwidth $BW_{3\ \text{dB}}$ is 24.5 GHz. With the use of inductive peaking ($L = 420$ pH), the bandwidth is extended to 39.2 GHz.

The output buffer that drives the ΔΣ bitstream to the external 50-Ω loads consists of two bipolar inverter stages with inductive peaking [11]. As shown in Fig. 13, the second inverter employs an emitter degeneration resistance in order to improve the bandwidth and reduce the impact of distortion in the last stage that drives the signal off chip.

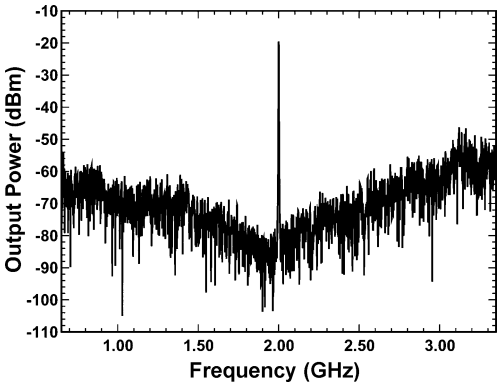

Fig. 14. Simulated ADC spectrum ($N_{\mathrm{FFT}} = 32768$).

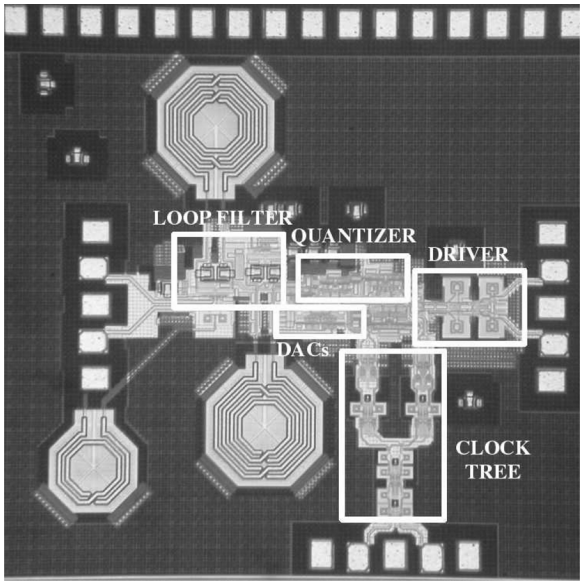

Fig. 15. Chip microphotograph.

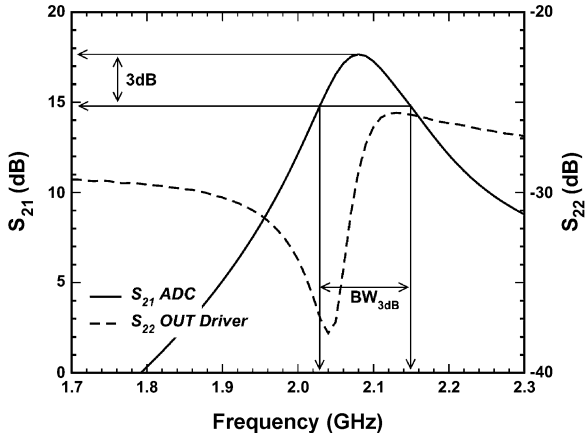

Fig. 16. Measured ADC single-ended S-parameters.

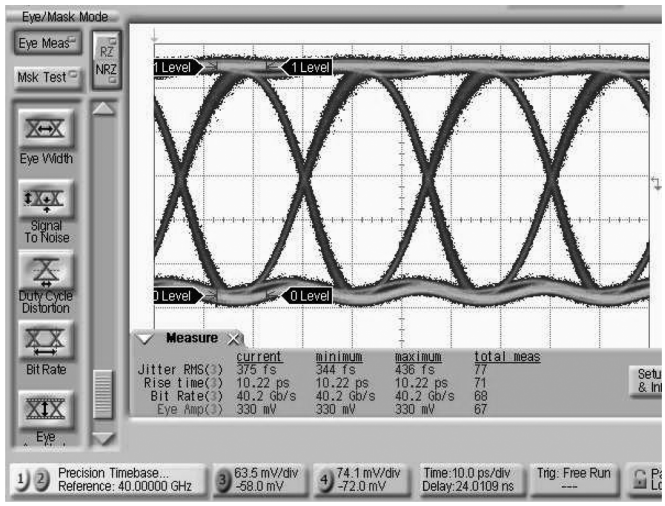

Fig. 17. Measured output eye diagram at 40 Gb/s.

D. Closed-Loop Circuit Simulation

The closed-loop simulation at the transistor level of the entire circuit, after parasitic extraction is illustrated in Fig. 14. The circuit must be simulated over a large number of clock cycles to accurately predict the quantization noise levels [8], but the required time and amount of generated data makes such a simulation prohibitive at 40-GHz sampling rates. The simulation period for 32768 samples is 0.82 μs. The spectrum at the output of the driver is plotted for an input power of -10 dBm and 32768 FFT points. The simulated SNDR of 51 dB is calculated over a bandwidth of 60 MHz.

IV. ADC Measurement Results

The circuit was implemented in a 130-nm SiGe BiCMOS process and occupies 1.52×1.58 mm^2. The chip microphotograph is shown in Fig. 15. S-parameter, eye diagram and power spectrum measurements of the ADC were performed on wafer using 65-GHz GGB probes. Fig. 16 illustrates the measured S_{21} and S_{22} in the passband of the ADC without applying a clock signal to the circuit. Instead, a DC signal was applied at the clock input of the circuit to switch the latches to one side and put them in transparent mode. The filter Q is 17.5 and the 3-dB bandwidth is 120 MHz. Large signal measurements were conducted by directly connecting one differential output of the circuit to a 50-GHz Agilent E4448A spectrum analyzer (PSA) and the other output to an Agilent Infiniium DCA-86100C oscilloscope with 70-GHz remote heads. The clock signal was provided from a low phase noise Agilent E8257D PSG signal source and the RF input signals were obtained from Agilent E4422B and 83650B signal sources.

The 40-Gb/s output eye diagram is reproduced in Fig. 17 for a 2-GHz input, when the feedback loop is turned off and the analog input is sampled by the quantizer at 40 GS/s. The eye jitter is less than 0.375 ps rms, indicating that it does not limit the ADC resolution. For the measured jitter value $\sigma_t = 0.375$ ps, OSR $= 333$, and $f_o = 2$ GHz, the SNR limit due to jitter can be estimated as [19]

$$\mathrm{SNR} = 20log_{10}\frac{\sqrt{\mathrm{OSR}}}{2\pi f_o \sigma_t} = 71.76\ \mathrm{dB} \tag{18}$$

proving that the dominant source of in-band noise is quantization noise and that the ADC is not close to the theoretical jitter limit [20]. Similar jitter performance can be achieved with a recently reported 40-GHz VCO/PLL [21] fabricated in the same

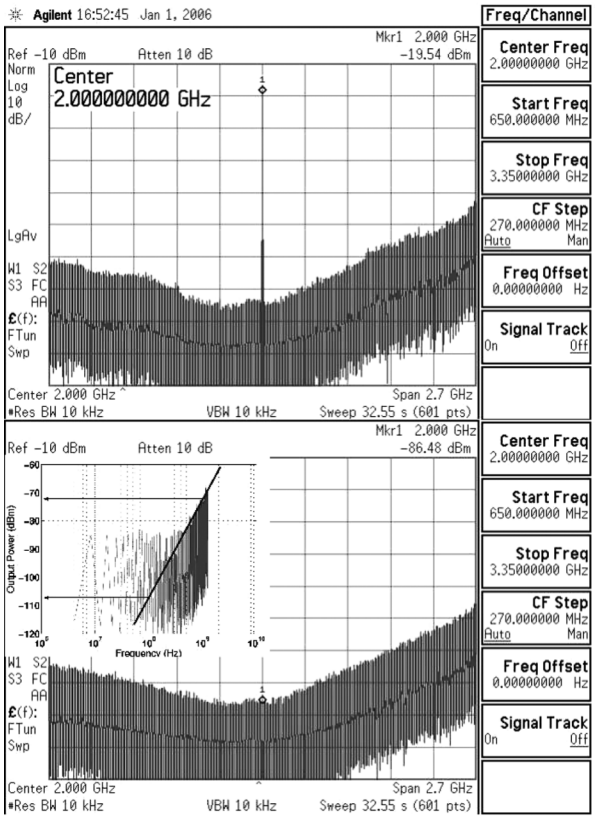

Fig. 18. Measured ADC output spectrum with and without a 2-GHz input sinusoid.

SiGe BiCMOS technology and having -105 dBc/Hz of phase noise at 1 MHz offset from the clock frequency.

Fig. 18 shows the measured $\Delta\Sigma$ ADC output spectrum with and without an input sinusoidal signal at 2 GHz. Losses in the test setup have not been de-embedded. The loop remains stable in the absence of the input signal and maintains its noise shaping, despite the finite Q of the resonators. The noise shaping in the lower part of the spectrum is >35 dB/decade, as displayed in the inset. The theoretical noise shaping of a fourth-order bandpass loop is 40 dB/decade. The inset is obtained by shifting the spectrum to 0 GHz, flipping it along the vertical axis and plotting on a log scale.

The SNDR was found from the measured power spectrum by integrating the noise around the input signal over the bandwidth of interest using the built-in integration function of the PSA. To accurately measure the SNDR, the resolution bandwidth of the PSA was lowered until the noise floor remained constant. The noise floor obtained in this manner represents the quantization noise from the ADC. The noise at the ADC output integrated over 10 MHz band centered at 2 GHz is -73 dBm, as depicted in Fig. 19 (top trace). When the feedback is turned off, the circuit and thermal noise contributions are below the -83 dBm (-153 dBm/Hz) sensitivity of the spectrum analyzer (Fig. 19, bottom trace), indicating that quantization noise is the main limitation in the circuit. The output versus input power transfer characteristic at 2-GHz is reproduced in Fig. 20. The single-ended SNDR is plotted as a function of input power for 10-MHz, 60-MHz, and 120-MHz bandwidths in Fig. 21. The

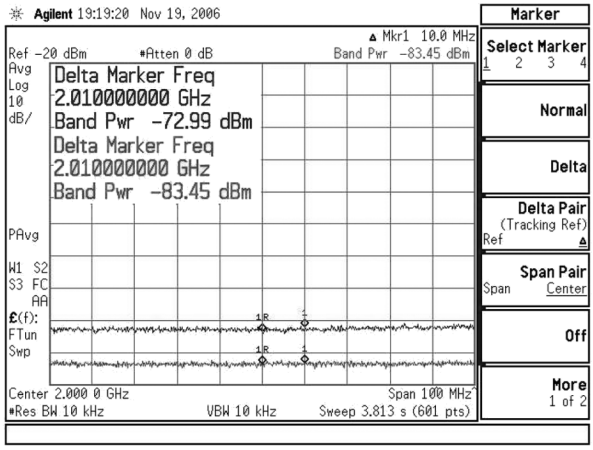

Fig. 19. Measured noise floor at the ADC output (top trace). The noise floor of the ADC drops from -73 dBm to -83.45 dBm (bottom trace) when the feedback is off, indicating that quantization noise is limiting the ADC.

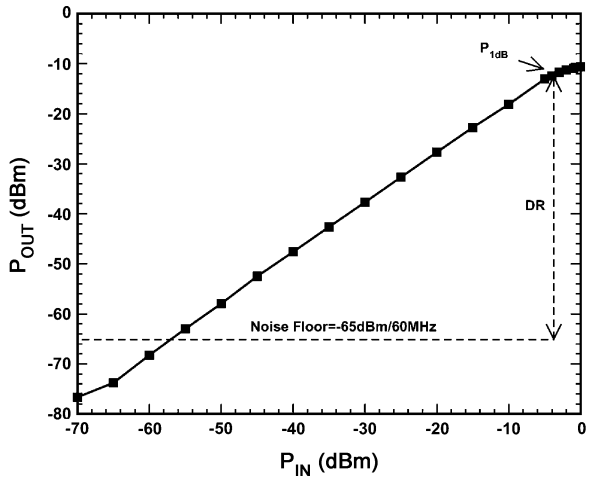

Fig. 20. Measured output versus input power of the ADC for a 2-GHz single-tone input.

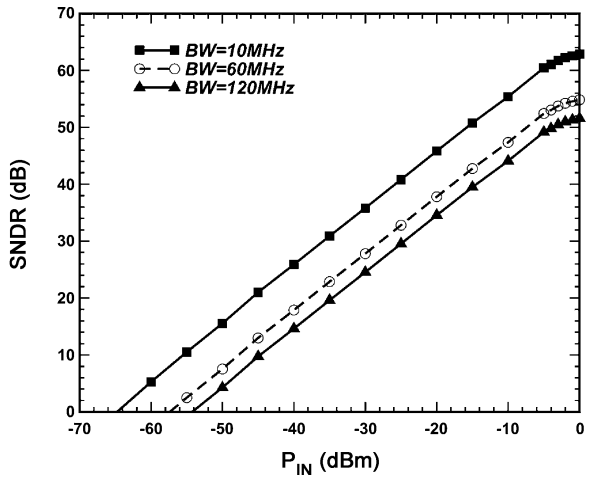

Fig. 21. Measured dynamic range for a 2-GHz single tone input.

ADC achieves SNDR values of 63 dB, 55 dB, and 52 dB over 10 MHz, 60 MHz, and 120 MHz, respectively, for a single tone at 2 GHz. The measured peak SNDR as a function of bandwidth can be found in Fig. 22. The simulated SNDR (Fig. 14) has 32768 samples, corresponding to an FFT bin of 1.22 MHz,

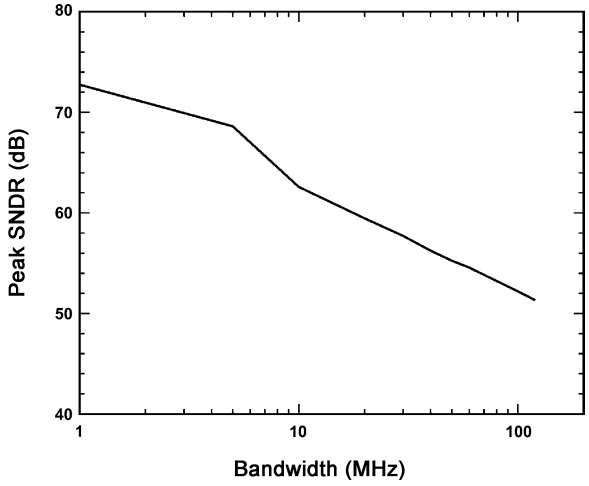

Fig. 22. Measured peak SNDR versus bandwidth for a 2-GHz single tone input.

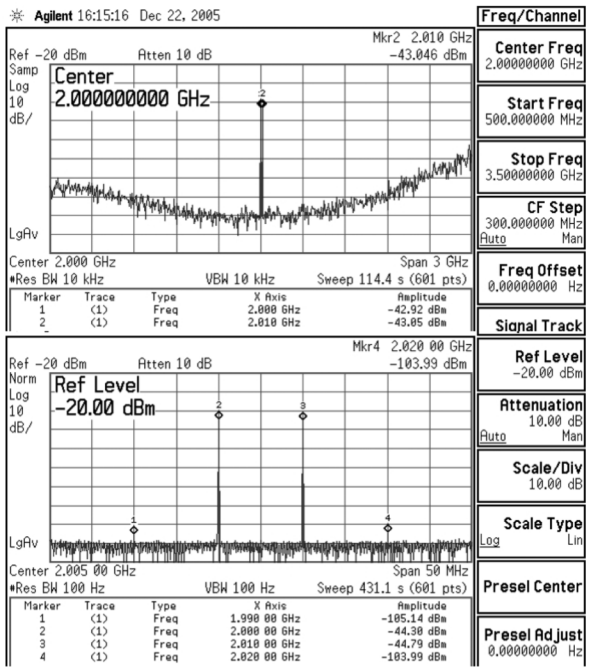

Fig. 23. Measured ADC two-tone spectra at 2 GHz with $P_{\rm IN} = -30$ dBm.

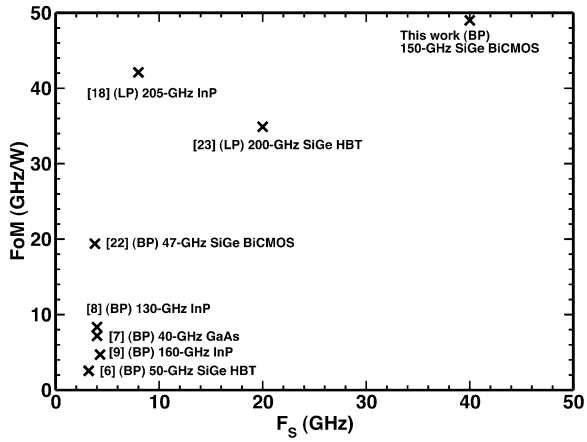

Fig. 24. Comparison of mm-wave ΔΣ ADCs.

TABLE I
PERFORMANCE SUMMARY OF ΔΣ ADC

Technology	130-nm SiGe BiCMOS
Chip Area	1.52×1.58 mm^2
Power Supply	2.5 V
Center Frequency	2 GHz
Clock Rate	40 GHz
OSR	333
SNDR	55 dB / 60 MHz 52 dB / 120 MHz
SFDR	61 dB
IIP3	+4 dBm
DR	53 dB
Power Consumption	1.6 W
Filter	115 mW
Quantizer	512.5 mW
DACs	237.5 mW
Clock Tree	645 mW
Driver	94 mW
FoM	49 GHz/W

100 times larger than the PSA resolution bandwidth. As can be seen in Fig. 19, the ADC passband has an approximately flat noise distribution. The SNDR can be further improved by adding cross-coupled negative resistance cells across the filter tanks to increase their Q [5]. However, this option should be carefully analyzed as high-Q circuits suffer from low linearity, high noise, and instability.

The single-ended IIP3 $= +4$ dBm, $P_{\rm 1dB} = -4$ dBm, and $\rm SFDR = 61$ dB of the entire ADC were obtained from two-tone measurements with 10-MHz spacing, as shown in Fig. 23. The ADC linearity is better than that of the filter test structure discussed in Section III-A due to the application of feedback. From the measured $P_{\rm 1dB}$ value and noise floor of Fig. 20, the dynamic range (DR) of the receiver over 60 MHz, is 53 dB.

The circuit dissipates 1.6 W from a 2.5-V power supply. Table I summarizes the performance of the ADC. Almost half of the power (0.74 W) is consumed by the clock path and output driver with the rest being dissipated by the filter, DACs, and quantizer. In comparison to recently-published ADCs (Fig. 24), this ADC achieves the best figure of merit (FoM) [20]

$$\text{FoM} = \frac{2^{\rm ENOB} \times 2BW}{P_{\rm DC}} \tag{19}$$

among the bandpass designs [6]–[9], [22] and comparable performance to the low-pass ADCs of [18] and [23], which were implemented in 200-GHz f_T InP and SiGe HBT technologies, respectively. Although the output stream of the ADC must be decimated to lower rates, a low-power 40-Gb/s decimation filter consisting of a DEMUX and digital filters can be realized in SiGe BiCMOS with only 10 mW per latch [21] at 2.5 V. The power dissipation of a 1:2 DEMUX consisting of three latches would be 30 mW. The FoM would not be significantly degraded by the decimation stage.

V. CONCLUSION

A fourth-order continuous-time bandpass ΔΣ ADC, clocked at 40 GHz and centered at 2 GHz has been demonstrated. The loop filter employs two G_m–LC stages with MOS-HBT cascode transconductors for high linearity, low noise, and lower

supply voltage when compared with an all-HBT implementation. The ADC achieves an SNDR of 52 dB over a 120-MHz bandwidth with an ENOB of 8.5 and tunable center frequency between 1.8 and 2 GHz. The SFDR is 61 dB and the FoM is 49 GHz/W. These results demonstrate for the first time that mm-wave sampling can be applied to bandpass $\Delta\Sigma$ ADCs implemented in silicon. The simplicity of the design also makes it scalable to other standards between 2.4 and 6 GHz, such as WLAN, WiMAX and possibly 12-GHz DBS with minimum modifications in the loop filter. Tunable transconductance cells and resonators would give the ADC the flexibility to adjust to the desired standard, thus realizing a true software-defined radio receiver.

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