# Si-based Inductors and Transformers for 30-100 GHz Applications

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***Abstract*** **– Silicon planar and 3-D inductors and transformers were designed and characterized on wafer up to 100 GHz. Self-resonance frequencies (SRF) beyond 100 GHz were obtained, demonstrating for the first time that spiral structures are suitable for applications such as 60-GHz WLAN or 77-GHz automotive RADAR. Minimizing area over substrate is critical to achieving high SRF. A stacked transformer is reported with $S_{21}$ of -2.5 dB at 50 GHz, and which offers improved performance and less area (30μm x 30μm) than planar transformers or microstrip couplers.**

***Index Terms*** **– Inductors, stacked inductors, transformers, millimeter wave, self-resonance frequency**

## I. Introduction

Monolithic spiral inductors and transformers have become very popular in silicon-based RFICs. However, their application in millimeter wave circuits has not been investigated. While silicon is still an emerging technology for this frequency range, VCO and LNA designs reported to date [e.g. 1, 2] employ transmission-line resonators which suffer from larger area than spiral structures. Mutual inductance in spiral coils allows for larger inductance in less area than transmission-line structures. Furthermore, increasing number of metal layers in (Bi)CMOS technologies facilitates the design of 3-D inductors and transformers reminiscent of discrete components found at lower frequencies. In this paper we present spiral inductors and transformers suitable for mm-wave applications such as 60-GHz radio, 77-GHz automotive RADAR, and broadband serial communications above 40 Gb/s.

## II. Inductors

### A. Millimeter-wave Design Considerations

For silicon-based inductors in the mm-wave regime, the dominant mechanism for degradation in quality factor is losses in the silicon substrate [3]. To minimize these losses, inductor footprint is made as small as possible. This involves reducing outer diameter as well as metal line width. While inductor design at radio frequencies emphasizes the use of wide metal lines to reduce series resistances, this approach increases capacitance to substrate and degrades both Q and self-resonance frequency (SRF). In our designs, DC electromigration effects set the lower limit on line width. Turn-to-turn spacing is made roughly equal to the dielectric thickness to substrate to lessen the impact of interwinding capacitances. Wide metal spacing also diminishes the frequency dependence of the inductance set forth by the proximity effect [4].

### B. Planar Inductors

Based on the discussion in the previous section, a family of square and symmetric [5] planar inductors was designed using ASITIC [6] and implemented in a six-layer copper CMOS backend [7]. Inductance values are in the range of 100-300 pH with outer diameters between 30-50 μm. Inductors were measured up to 100 GHz in Crolles, France, and up to 50 GHz in Ottawa, Canada. Excellent agreement is seen in measured effective inductance ($L_{EFF} = \mathrm{Im}\{Y_{11}^{-1}\}/\omega$) from both systems. In all cases, measured inductance was within ~5% of the design value, as summarized in Table 1. To the authors' best knowledge, this marks the first verification of ASITIC in the mm-wave regime. Slight dips in $L_{EFF}$ are seen close to 90 GHz in all cases, which underscore the difficulty in measuring and de-embedding such small inductance values at very high frequencies. Measurements indicate that the SRF is well beyond 100 GHz in all cases.

### C. Stacked Inductors

Further reduction in area is achieved using 3-D (or stacked) inductors [8]. These structures benefit from

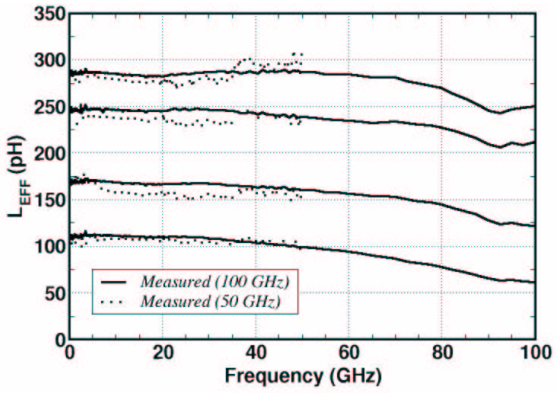


Fig. 1. $L_{EFF}$ for planar mm-wave inductors measured using 50-GHz and 100-GHz network analyzer systems.

TABLE 1
DESIGNED VS. MEASURED INDUCTOR PERFORMANCE

| DUT | $L_{EFF}$ @ 40 GHz (Measured) | $L_{EFF}$ @ 40 GHz (ASITIC) | SRF (ASITIC) |
|---|---|---|---|
| D1 | 290 pH | 270 pH | 159 GHz |
| D2 | 168 pH | 156 pH | 221 GHz |
| D3 | 239 pH | 241 pH | 170 GHz |
| D4 | 115 pH | 101 pH | 334 GHz |

strong mutual coupling between vertically adjacent metal layers, and can generate the same inductance in less area as compared with planar inductors. Stacked inductors implemented in two or three metal layers were designed with inductance values between 200 and 600 pH and with outer diameters ranging from 20 µm to 40 µm. $L_{EFF}$ extracted from measured 50-GHz data is presented in Fig 2.

Effective inductances for a planar and for a stacked inductor with respective outer diameters of 36 µm and 18 µm are shown in Fig 3. In both cases, self-resonance is well beyond the measurement capability. Results indicate that comparable inductance (~220 pH) in the mm-wave regime can be obtained using stacked inductors with significant area reduction over planar inductors. A die photo of the 220-pH stacked inductor, with two turns in metal 6 and two turns in metal 5, is presented in Fig. 4.

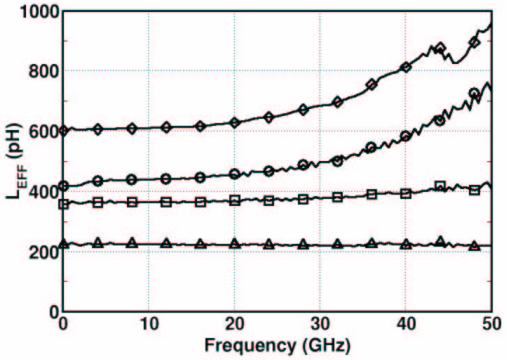


Fig. 2. Measured $L_{EFF}$ of mm-wave stacked inductors.

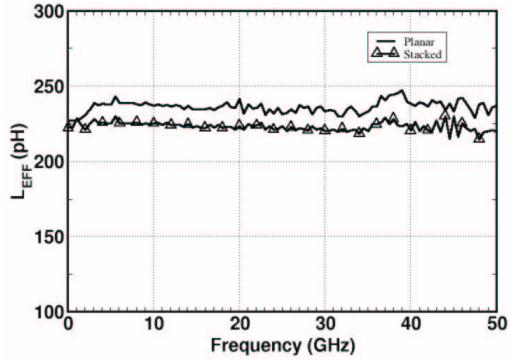


Fig. 3. Measured $L_{EFF}$ for 220-pH planar and stacked inductors.

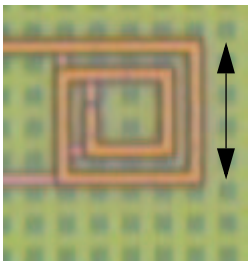


Fig. 4. Die photo of 220-pH 2-metal stacked inductor.

In order to understand whether dielectric thickness or inductor footprint are more important in determining SRF and Q, two stacked inductors of similar inductance were designed, the first using the top two metal layers with an outer diameter of 30 µm and the second using the top three metals with a 21 µm diameter. Clearly, smaller inductor footprint results in an improved SRF, as seen in the measured $L_{EFF}$ of Fig 5. The nearly 50% reduction in total area with more metal layers yields higher SRF, even though the bottom metal layer is slightly closer to the substrate. Despite additional via resistance, the three-metal inductor has similar Q due to reduced substrate loss.

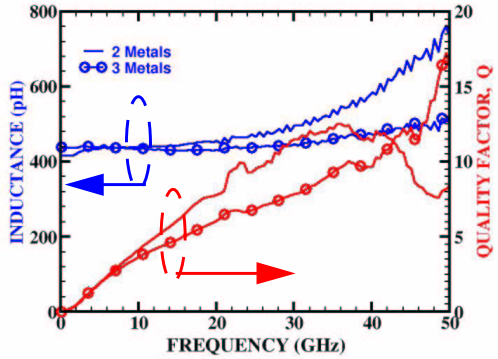


Fig. 5. Measured $L_{EFF}$ and Q of 420-pH stacked inductors implemented in two and three metal layers.

### *D. Impact of CMP Integrity Fill*

In sub-0.18 µm technologies with multi-metal backend, dummy metal fill patterns (as seen in the die photo in Fig. 6) are required to preserve chemical mechanical planarization (CMP) integrity. While these structures are usually automatically generated by CAD tools, the layout designer can often specify an exclusion region to prevent dummy fill from being generated near inductors. Test structures were designed to assess the impact of varying the spacing between the dummy fill and a 160-pH square inductor. Less than 5-pH variation, well within the measurement accuracy, is observed (Fig 7) as the distance from inductor edge to fill pattern is changed. Reducing fill spacing eases layout requirements for circuits employing inductors in state-of-the-art silicon technologies.

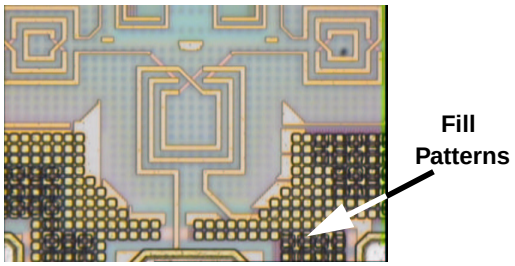


Fig. 6. CMP fill patterns near mm-wave inductors and transformer.

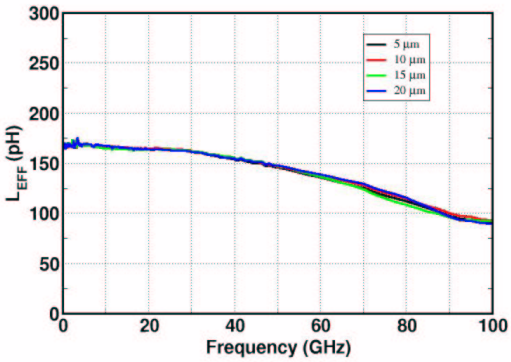


Fig. 7. Effect of fill pattern proximity on measured $L_{EFF}$.

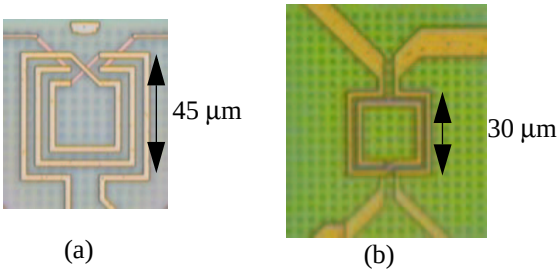


Fig. 8. Die photos of mm-wave transformers (a) planar and (b) stacked.

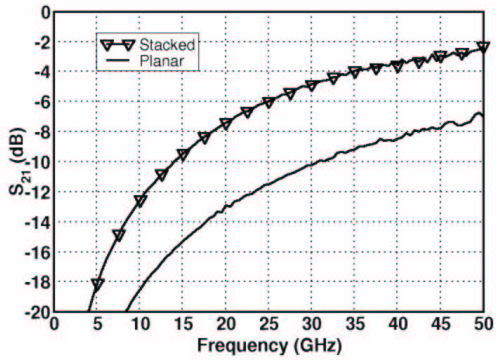


Fig. 9. Comparison of stacked and planar mm-wave transformers.

## III. MM-Wave Transformers

High-speed CML or ECL digital circuits require differential clocks, but only single-ended signal generators are available above 40 GHz. Single-ended-to-differential conversion can be achieved at low frequencies via a differential pair with the unused input terminated off-chip. At mm-wave frequencies, poor common-mode rejection renders this approach ineffective, as the differential outputs exhibit amplitude mismatch and phase misalignment. Other approaches have relied on a rat-race coupler, which occupies an area of 250 x 800 µm for single-ended-to-differential conversion at 80 GHz [9]. An on-chip transformer is ideal for single-ended-to-differential conversion, but so far has not been considered in the mm-wave regime.

Two transformer structures are investigated for mm-wave applications. The first, a planar transformer, employs symmetrical inductors for the primary and secondary as seen in the die photo of Fig 8a. Both windings are formed in metal 6 with metal 5 used for crossover. To ensure adequate SRF in the primary and secondary, the design follows guidelines set forth in Section II. This transformer, with an outer diameter of 45 µm, has been utilized to generate differential 43-GHz clocks from a single-ended signal source in a 43-Gb/s decision circuit [10].

A second transformer was implemented by vertically stacking two symmetrical inductors, each with two turns. The primary is formed in metal 6 with metal 5 crossovers, while the secondary is formed in metal 4 with metal 3 crossovers. The outer diameter of the stacked transformer (Fig. 8b) is 30 µm, which minimizes losses to the substrate. The vertical structure offers high coupling (k=0.7) and is much more area-efficient than the rat-race coupler in [9], making it well-suited for deep submicron silicon technologies. Fig. 9 compares the measured input-output coupling, $S_{21}$, in both the stacked and planar structures. The stacked structure exhibits -2.5 dB coupling at 50 GHz, and has approximately 5-dB better coupling than the planar transformer across the measured frequency range.

## IV. Modeling

Inductor model parameters for a double-Π equivalent circuit (Fig 10) are obtained by direct extraction from ASITIC simulations, or from measurements, as follows. Oxide capacitances and substrate resistances are extracted from low-frequency (0.5 GHz) simulations. Substrate capacitances are determined from the dielectric relaxation time of the substrate, such that $R_{SUB}C_{SUB} = \rho_{SUB}\varepsilon_{SI}$. Inductance and the frequency-dependent resistance network are then extracted from $y_{12}$ simulations.

The inductor model is applicable to both planar and stacked mm-wave inductors. Models were extracted from simulated data up to 100-GHz and are compared with 100-GHz measurements in Fig. 11. While the ASITIC-based models concur with measured data at lower frequencies,

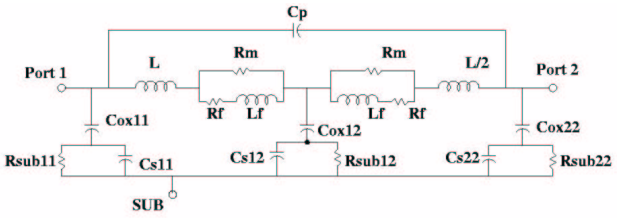


Fig. 10. Double-Π inductor model.

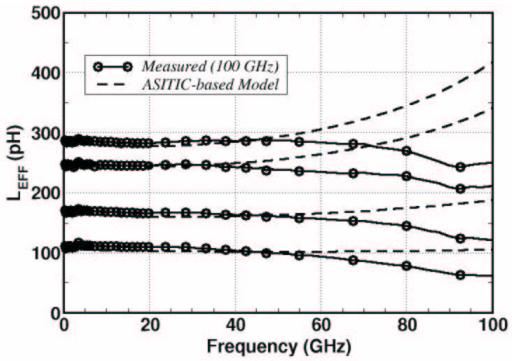


Fig. 11. Measured and ASITIC-modeled $L_{EFF}$ to 100 GHz.

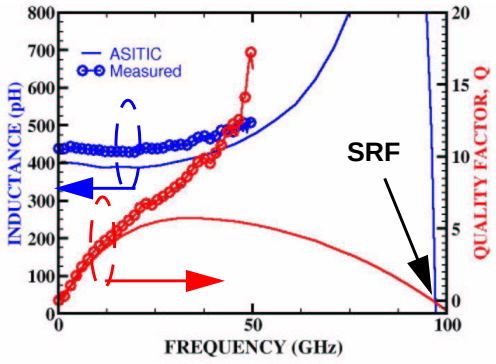


Fig. 12. Measured and modeled $L_{EFF}$ and Q for 3-metal 400pH.

discrepancies are noticed above 50 GHz. ASITIC predictions and measurements of the ~400-pH 3-metal stacked inductor introduced in Section III are compared in Fig. 12. Excellent agreement is observed between the simulated $L_{EFF}$ and that predicted from measurements up to 50 GHz, although measured Q values deviate from simulations at high frequencies. Further investigations focusing on de-embedding techniques and measurement error above 40 GHz are needed to conclude whether measurements or simulations are responsible for disparities.

## V. Conclusion

For the first time, spiral inductors realized in silicon technologies have been demonstrated and characterized up to 100 GHz. Reducing the total inductor area over substrate is paramount in achieving high SRF. Inductors have Q's in the 10-20 range, adequate for mm-wave VCOs, LNAs, or inductive peaking in broadband circuits, while consuming less die area than microstrip lines previously found in silicon-based mm-wave designs [1, 2]. A mm-wave transformer structure has been presented based on stacked symmetrical inductors. This transformer is well-suited as a single-ended-to-differential converter above 50 GHz, and occupies 200 times less area than previously reported mm-wave single-ended-to-differential converters in integrated circuit technologies [9]. The inductors and transformers presented in this work are adequate for several mm-wave applications, including 40-GHz fixed access radios, 60-GHz WLAN, 77-GHz automotive RADAR, and broadband serial communication systems above 40 Gb/s.

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## References

[1] H. Li and H.-M. Rein, "Millimeter-wave VCOs with wide tuning range and low phase noise, fully integrated in a SiGe bipolar production technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 184-191, Feb. 2003.

[2] S. Reynolds et al, "60 GHz transceiver circuits in SiGe bipolar technology," *ISSCC Dig. Tech. Papers*, pp. 442-443, Feb. 2004.

[3] S.P. Voinigescu et al, "Process- and geometry-scalable bipolar transistor and transmission line models for Si and SiGe MMICs in the 5-22GHz range," *IEDM Tech. Digest*, pp. 11.7.1-11.7.4, Dec. 1998.

[4] Y. Cao et al, "Frequency-independent equivalent-circuit model for on-chip spiral inductors," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 419-426, March 2003.

[5] M. Danesh et al, "A Q-factor enhancement technique for MMIC inductors," *Proc. IEEE RFIC Symp*, pp. 217-220, Apr. 1998.

[6] A. Niknejad, ASITIC, http://rfic.eecs.berkeley.edu/~niknejad/asitic.html

[7] M. Laurens et al, "A 150 GHz $f_T/f_{MAX}$ 0.13 µm SiGe:C BiCMOS technology, *Proc. IEEE BCTM*, Sept. 2003.

[8] R.B. Merril et al, "Optimization of high-Q inductors for multilevel metal CMOS," *Proc. IEDM*, pp. 38.7.1-38.7.4, Dec. 1995.

[9] T. Suzuki et al, "A 80-Gbit/s D-type flip-flop circuit using InP HEMT technology," *IEEE GaAs IC Symp. Tech. Dig.*, pp. 165-168, Nov. 2003.

[10] T.O. Dickson, R.Beerkens, and S.P.Voinigescu, "A 2.5-V, 40-Gb/s decision circuit using SiGe BiCMOS logic," accepted for publication in *Symp. on VLSI Circuits*, June 2004