# Low-Power Circuits for a 2.5-V, 10.7-to-86-Gb/s Serial Transmitter in 130-nm SiGe BiCMOS

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***Abstract*—Low-power building blocks for a serial transmitter operating up to 86 Gb/s are designed and implemented in a 130-nm SiGe BiCMOS technology with 150-GHz $f_T$ SiGe HBT. Design techniques are presented which aim to minimize high-speed building block power consumption. They include lowering the supply voltage by employing a true BiCMOS high-speed logic family, as well as reducing current consumption by trading off tail currents for inductive peaking. A serial transmitter testchip consuming under 1 W is fabricated and operation is verified up to 86 Gb/s at room temperature (92 Gb/s and 71 Gb/s at 0 °C and 100 °C, respectively). The circuit operates from a 2.5-V supply voltage, which is the lowest supply voltage for circuits at this data rate in silicon technologies reported to date.**

***Index Terms*—BiCMOS, CML, Colpitts VCO, inductors, multiplexer, serial transmitter, SiGe HBT, 100 G Ethernet.**

## I. Introduction

THE volume of data transported over networks continues to increase, fueled by demands for faster transmission of bandwidth-intensive applications such as high-definition video broadcasts. Next-generation serial communication systems are expected to have data rates in the 80–100-Gb/s range, as evidenced by recent calls for 100-Gb/s Ethernet (100 GE). As a result, high-speed building blocks such as multiplexers, demultiplexers, and clock and data recovery circuits have been reported in the literature operating at data rates of at least 80 Gb/s and implemented primarily in SiGe HBT or InP HBT technologies [1]–[3]. To achieve such high data rates with time-division multiplexing techniques, building block power consumption is often considerably high. For example, 4:1 multiplexers operating above 100 Gb/s dissipate at least 1.4 W even in HBT technologies with transistor cutoff frequencies exceeding 200 GHz [1]. Such numbers do not bode well for the integration of a single-chip 100 GE serializer-deserializer (SERDES). Moreover, a state-of-the-art 10 GE SERDES in 130-nm CMOS consumes only 800 mW [4], indicating that a more power-efficient 100 GE solution could be realized by operating ten 10 GE channels in parallel. However, the latter solution increases system complexity. If single-chip 100 GE SERDES are to be feasible, power consumption must be lowered in HBT-based transceivers.

This paper presents low voltage, low power design techniques for high speed wireline building blocks. Power dissipation is minimized by employing a low 2.5-V supply voltage, while using inductive peaking to lower bias currents in high-speed building blocks. As a test vehicle to show how record-breaking performance can be achieved with low power consumption, a 2.5-V, 10.7-to-86-Gb/s serial transmitter is designed in a 130-nm SiGe BiCMOS technology with HBT $f_T = 150$ GHz.

The paper is organized as follows. Section II presents low-power design methods for high-speed digital building blocks. These concepts are then applied to the design of critical building blocks for an 86-Gb/s serial transmitter in Section III. Key building blocks, including high-speed BiCMOS CML gates clocked at 43 GHz, an 86-Gb/s output driver with adjustable amplitude control, and a bipolar Colpitts oscillator are discussed. Experimental verification of the test chip is presented in Section IV. Finally, Section V concludes the paper.

## II. Low-Power High-Speed Design Methodology

In order to reduce power consumption in high-speed digital building blocks, one must combat the problem on two fronts. First, the supply voltage must be lowered. This has been problematic in SiGe bipolar designs due to the high $V_{\rm BE}$ of the HBT, leading to power supplies of 3.3 V or 5 V irrespective of technology node. In CMOS technologies constant-field scaling has allowed for a continued reduction in supply voltage with each new technology, leading to 1-V power supplies in 90-nm technologies. It has been demonstrated that one can derive a logic family that employs both n-channel MOSFETs and SiGe HBTs in a BiCMOS technology. A BiCMOS inverter from this logic family is illustrated in Fig. 1(a), which maintains the high intrinsic slew rate of the SiGe HBT while employing MOSFETs on lower-level transistors to benefit from their low input time constant [5]. At the 130-nm technology node and below, the $V_{\rm GS}$ of the nMOS ($\sim$750 mV) is lower than the $V_{\rm BE}$ of the SiGe HBT ($\sim$900 mV) when both devices are biased at their peak $f_T$ (Fig. 2). Unlike previous attempts to replace HBTs with n-MOSFETs for low-voltage operation of CML/ECL digital gates at the 0.8-$\mu$m technology node [6] (where the MOSFET $V_{\rm GS}$ at peak-$f_T$ is at least 3 V), it is now possible to do so while still getting the best high-speed performance from the n-channel device. The resulting 2.5-V power supply of this logic family represents a 24% reduction in power consumption as compared with 3.3-V bipolar current-mode logic blocks without compromising speed. Moreover, it has been shown

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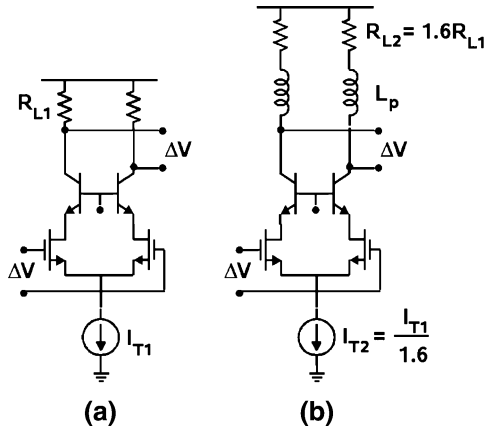


Fig. 1. BiCMOS CML inverters (a) without and (b) with inductive peaking. The inverter in (b) achieves roughly the same 3 dB bandwidth as that in (a) but with lower bias current.

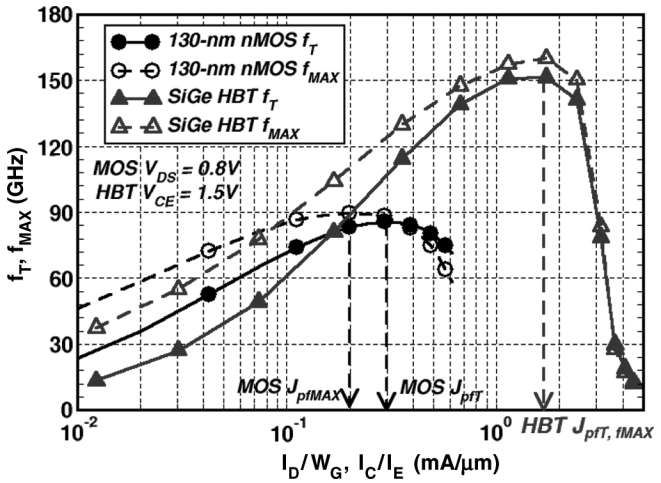


Fig. 2. Measured $f_T$ and $f_{\rm MAX}$ versus current density for 130-nm n-channel MOSFETs (finger width $= 2\ \mu$m) and SiGe HBTs.

that by removing current tail transistors from the BiCMOS logic topology, the supply voltage can be further lowered to 1.8 V. Early evidence suggests that the combination of 130-nm MOSFETs with 230-GHz $f_T$ HBTs from a 1.8-V supply will result in a lower-power 80-Gb/s latch than one implemented in 65-nm LP CMOS operating from 1.2 V [7]. Such results not only testify to the potential of BiCMOS logic for low-power serial transceiver design, but also demonstrate that it may be a more economical solution than moving to highly-scaled CMOS technologies.

It is important to distinguish the BiCMOS logic family from other low-voltage topologies that rely on the parallel switching of bipolar transistors to reduce device stacking [8]. These topologies require double the number of tail current sources, but since the supply voltage is not reduced by half, the power dissipation per building block actually increases. This distinction points to a second goal in reducing power dissipation, which is to minimize the bias current in each building block. To first order, the bandwidth of the resistively loaded BiCMOS inverter in Fig. 1(a) is set by the time constant at the output node.

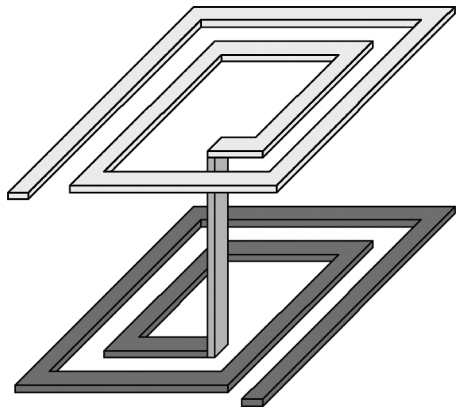

Fig. 3. Conceptual illustration of a stacked (or 3-D) spiral inductor implemented in two metal layers.

$$BW_{\rm 3dB} \approx \frac{1}{2\pi \times R_{L1} \times C_L} = \frac{I_{T1}}{2\pi \times \Delta V \times C_L}. \quad (1)$$

Here, $C_L$ represents the total capacitance at the output node. It is well known that for a fixed resistance, one can add inductive peaking and improve bandwidth by as much as 60%. Alternatively, one can design for lower bandwidth with larger load resistances, and then apply inductive peaking to reach the desired 3 dB bandwidth. The bandwidth of the BiCMOS cascade inverter with inductive peaking in Fig. 1(b) becomes

$$\begin{aligned} BW_{\rm 3dB,peaked} &\approx 1.6 \times \frac{1}{2\pi \times R_{L2} \times C_L} \\ &= 1.6 \times \frac{I_{T2}}{2\pi \times \Delta V \times C_L}. \end{aligned} \quad (2)$$

Setting the bandwidths of (1) and (2) to be equal and noting that the logic swing $\Delta V$ remains constant, one can see that the bias current after peaking is about 37% lower than the design without peaking. It should be pointed out that as the tail current is decreased, the emitter length of the HBTs and gate widths of the MOSFETs are also reduced to maintain the current density and $f_T$. In a BiCMOS implementation with a 2.5-V supply, the total power consumption after applying inductive peaking is slightly less than half that of a 3.3-V bipolar design without inductive peaking.

One perceived drawback of this approach is the area occupied by the inductors. This can be mitigated by using the multiple metal layers available in CMOS or BiCMOS technologies and creating stacked (or 3-D) structures to obtain a larger inductance for a given area, as shown in Fig. 3 [9]. It is important to note that like MOSFETs, spiral inductors also follow scaling laws. One can estimate the inductance $L$ of a 3-D spiral constructed from $m$ metal layers based on the number of turns $n$, outer diameter $d$, and average diameter $d_{\rm avg}$ [10], [11]:

$$L \approx \frac{6\mu_0 m^2 n^2 d_{\rm avg}^2}{11d - 7d_{\rm avg}}. \quad (3)$$

From (3), it is observed that if the diameter is scaled by a factor $S$, the inductance also reduces by the same factor.

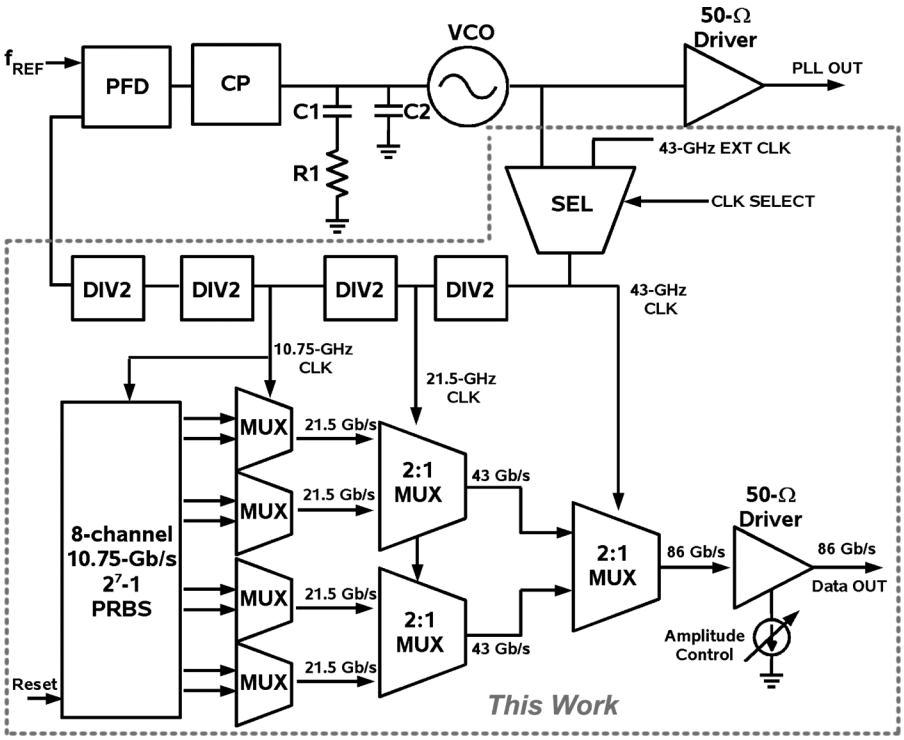


Fig. 4. Block diagram of the 80-Gb/s transmitter IC testchip.

$$\frac{L}{S} \approx \frac{6\mu_0 m^2 n^2 \left(d_{\text{avg}}/S\right)^2}{(1/S)\,(11d - 7d_{\text{avg}})}. \tag{4}$$

Moreover, the oxide capacitance from the bottom metal layer to the substrate is a function of the total metal line length in one layer $(l)$, the trace width $(W)$, and the distance from the bottom metal layer to the substrate $(h)$. If the length and width are scaled by the same factor $S$, the inductor area is reduced by a factor of $S^2$, as is the total parasitic capacitance to ground.

$$C_{\text{OX}} \approx lW\frac{\varepsilon_{\text{OX}}}{h} \Rightarrow \frac{C_{\text{OX}}}{S^2} \approx \frac{lW}{S^2}\frac{\varepsilon_{\text{OX}}}{h}. \tag{5}$$

This suggests that it is reasonable to integrate a large number of inductors on a single chip, particularly at high frequencies where the required inductance value is not large. In the design to be presented in Section III, stacked inductors can be realized with outer diameters of between 10 $\mu$m and 20 $\mu$m. Interestingly, this is on the same order as the gate widths of the MOSFETs employed in 80-Gb/s logic circuits. The inductor quality factor is not of particular importance in shunt-peaking applications, as it can be absorbed in the resistive load. However for completeness is it instructive to see how $Q$ scales with the inductor size. The DC resistance in a single metal layer can be determined by introducing the metal thickness $t$ and sheet resistance $\rho$.

$$R_{\text{DC}} \approx \frac{\rho l}{Wt} \Rightarrow R_{\text{DC}} \approx \frac{\rho\,(l/S)}{(W/S)\,t}. \tag{6}$$

While $l$ and $W$ are both reduced by $S$[1], the metal thickness and sheet resistance cannot be changed and the total series resistance remains constant. The same is true at high frequencies when the skin depth $\delta$ of the conductor is considered.

$$R_{\text{AC}} \approx \frac{\rho l}{W\delta\left[1-\exp\left(-t/\delta\right)\right]} \quad \Rightarrow$$

$$R_{\text{AC}} \approx \frac{\rho\,(l/S)}{(W/S)\,\delta\left[1-\exp\left(-t/\delta\right)\right]}. \tag{7}$$

Because of this, the peak quality factor of the scaled inductor is unchanged, but the frequency at which the $Q$ peaks is higher roughly by a factor of $S$. Consequently spiral structures are as suitable for use at mm-wave frequencies above 30 GHz as they were for RF applications at 2 GHz.

## III. 80-Gb/s Serial Transmitter Design

Using the low-power design techniques presented in Section II, an 80-Gb/s serial transmitter testchip was designed in a 130-nm SiGe BiCMOS technology with 150-GHz $f_T$ HBTs. The block diagram of the transmitter is shown in Fig. 4. It consists of an 86-Gb/s 8:1 multiplexer (MUX), an 86-Gb/s output driver with adjustable amplitude control, and a 43-GHz 16:1 frequency divider. Additionally, a low-power 10.7-Gb/s $2^7-1$ PRBS generator is also included for built-in self-test [12]. For testing purposes, the eight inputs to the MUX were aligned such that the 86-Gb/s output would also be pseudo-random.

The 8:1 MUX is implemented by connecting several 2:1 multiplexers in a tree architecture. A block diagram of the

[1]A lower limit on the trace width $W$ is usually determined by the current through the inductor and electromigration reliability rules for the technology.

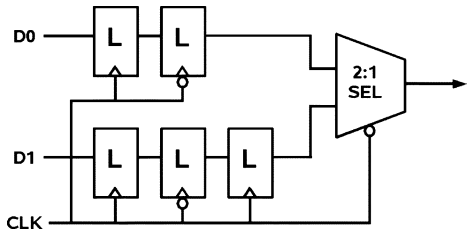


Fig. 5. 2:1 MUX implementation with five latches and a selector.

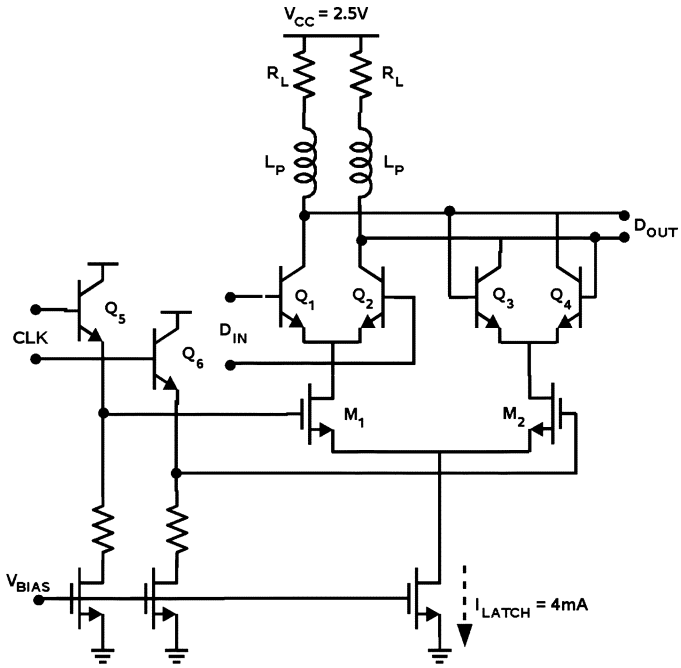


Fig. 6. 20-mW 43-Gb/s BiCMOS latch.

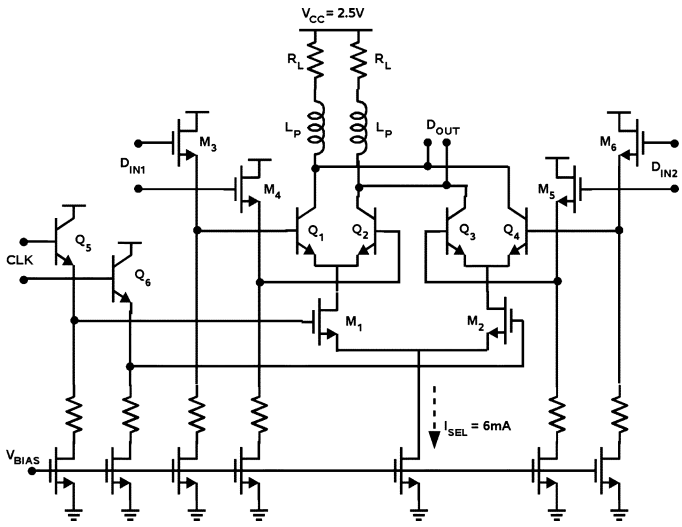


Fig. 7. 60-mW, 86-Gb/s BiCMOS selector.

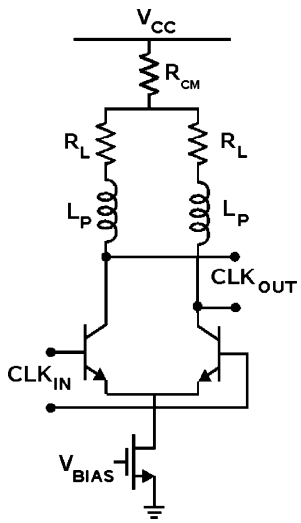


Fig. 8. 43-GHz clock buffer. A common-mode resistor is employed to avoid operating nFETs $\mathrm{M}_1/\mathrm{M}_2$ from Fig. 6 in the triode region.

final 2:1 multiplexer is shown in Fig. 5 and consists of five 43-GHz latches which align the data going into the 86-Gb/s selector. Note that the lower speed 2:1 multiplexers employ the same five-latch architecture. The BiCMOS implementation of a 43-GHz latch using the low-power techniques outlined in Section II is illustrated in Fig. 6. Compared with our previous latch designs [5], the level-shifting followers in the latch regenerative path have been removed for further power savings. The power consumption of the 43-GHz latch is 20 mW, which is believed to be the lowest for any silicon-based latch operating at this speed, and equals that of the lowest power InP HBT latch [13].

The schematic of the BiCMOS 86-Gb/s selector is shown in Fig. 7. A combination of MOS source followers and HBT emitter followers are employed on the data and clock paths, respectively. The latter have higher bandwidth, making them more suitable for use on the 43-GHz clock path. Headroom considerations prevent the use of HBT followers on the input data paths if the circuit is to operate from 2.5 V. Instead, MOS source followers are employed on the 43-Gb/s input data paths. It is interesting to note that the combination of MOS and HBT devices on high-speed paths gives rise to important DC biasing considerations. Of primary concern is the $V_{\mathrm{DS}}$ of transistors $\mathrm{M}_1$ and $\mathrm{M}_2$ in the selector. If the data and clock signals at the input to the source followers have the same common mode level, it can be seen that the $V_{\mathrm{DS}}$ of both $\mathrm{M}_1$ and $\mathrm{M}_2$ at the quiescent point is nearly zero. This results in a significant degradation in the $f_T$ of the MOSFETs and prevents the devices from switching at the required 43-GHz clock rate. To avoid this situation, a common-mode resistor is inserted in the clock buffer as seen in Fig. 8. The voltage drop across this resistor sets the $V_{\mathrm{DS}}$ of $\mathrm{M}_1$ and $\mathrm{M}_2$ to ensure sufficient $f_T$ for 43-GHz operation.

The 86-Gb/s selector is followed by a 50-$\Omega$ output driver with adjustable amplitude control whose schematic is presented in Fig. 9. The final stage of the driver consists of a BiCMOS cascode differential pair, which combines the excellent input linearity of the n-channel MOSFET with the output linearity of a bipolar transistor. A key advantage of this implementation is that unlike bipolar transistors, the transconductance and input capacitance of an n-channel MOSFET biased near its peak-$f_T$ current density of 0.3 mA/$\mu$m remain fairly constant as a function of the bias current [14]. Consequently as the tail current in the differential pair is varied to adjust the output swing, little degradation

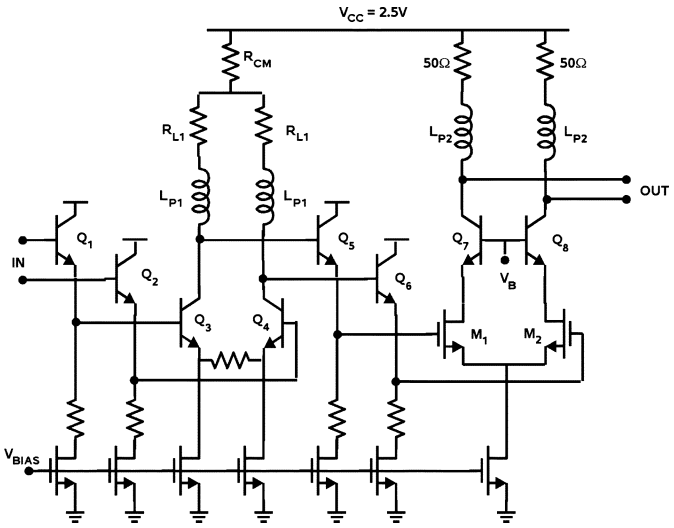


Fig. 9. 86-Gb/s 50-Ω BiCMOS output driver with adjustable amplitude control.

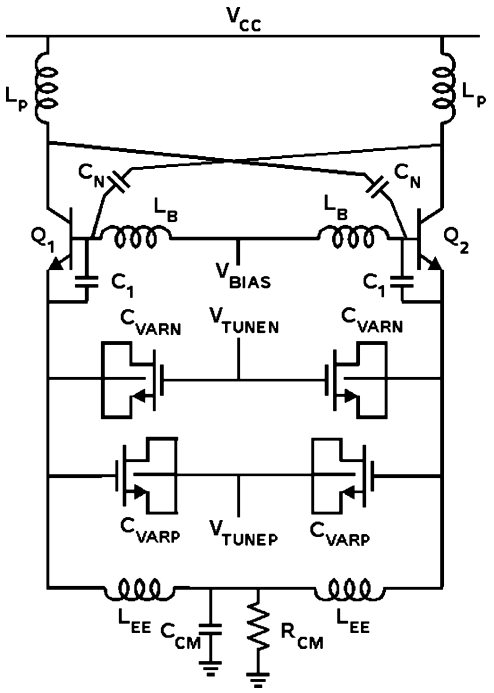


Fig. 10. 40-GHz Colpitts common-collector oscillator with $C_{\rm BC}$ neutralization.

in the quality of the output eye diagram is observed. Measured $S$-parameters of a breakout of this driver were presented previously [14], which show that the output match is unaffected by the change of bias current. Intentional gain peaking at higher frequencies is introduced to compensate for losses in the cables and probes anticipated in the measurement setup. Note that the 130-nm nMOSFETs with $f_T = 85$-GHz switch at the full rate of 86 Gb/s, the fastest for any MOSFET digital circuit reported to date. More details on the output driver design are presented in a prior publication [14].

At data rates above 40 Gb/s, low noise clock generation becomes ever more critical to minimize jitter in transmitted data.

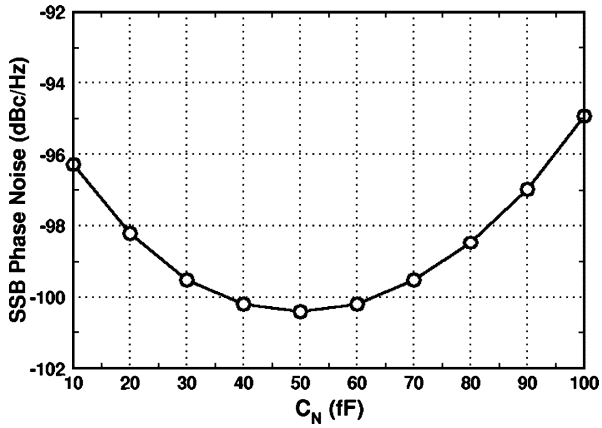


Fig. 11. Effect of neutralization capacitor $C_{\rm N}$ on simulated phase noise at a 1-MHz offset from the 40-GHz center frequency. The phase noise is minimized when $C_{\rm N}$ equals $C_{\rm BC}$ of the tank transistors.

This underscores the need for low phase noise VCOs. While the use of cross-coupled VCOs is widespread, it is important to realize that the output directly loads the *LC* tank and leads to lower tuning range and higher phase noise. On the other hand, the Colpitts common-collector VCO topology does not suffer from such limitations. A schematic of a bipolar Colpitts oscillator is illustrated in Fig. 10. The tank is formed around the base-emitter of the SiGe HBTs, with the capacitance in the emitter providing sufficient negative resistance to sustain oscillations. The output is taken from the collector resulting in improved isolation, and inductor $L_P$ allows for large output voltage swing without raising headroom concerns. Inductor $L_{EE}$ filters noise from the tail resistor to further improve phase noise [15]. Differential tuning is achieved through the use of accumulation-mode nMOS varactors, as can be seen in the schematic. It is noted that the base-to-collector capacitance loads the tank and degrades the oscillator tuning range. To compensate for $C_{\rm BC}$, cross-coupled neutralization capacitors are introduced [16]. Unlike similar VCOs which combine the Colpitts and cross-coupled topologies [17], it is important to note that these capacitors do not impact the oscillation frequency. It can be shown that the oscillation frequency is given by

$$f_{\rm osc} = \frac{1}{2\pi\sqrt{L_B C_{\rm EFF}}} \tag{8}$$

where the effective tank capacitance is

$$C_{\rm EFF} \approx C_{\rm BC} - C_{\rm N} + \frac{(C_1 + C_{\rm BE})(C_{\rm VARP} + C_{\rm VARN})}{C_1 + C_{\rm BE} + C_{\rm VARP} + C_{\rm VARN}}. \tag{9}$$

Clearly for $C_{\rm N}$ equal to $C_{\rm BC}$, the impact of the base-to-collector capacitance is cancelled. Interestingly, simulations in Fig. 11 show that the phase noise of the 40-GHz VCO is minimized for $C_{\rm N} = C_{\rm BC}$.

## IV. Experimental Results

The transmitter IC and associated test structures were fabricated in a 130-nm SiGe BiCMOS technology with SiGe HBT $f_T$ of 150 GHz [18]. A separate VCO test structure was also fabricated and measured on-die using an Agilent E4448A power spectrum analyzer and E4419B power meter

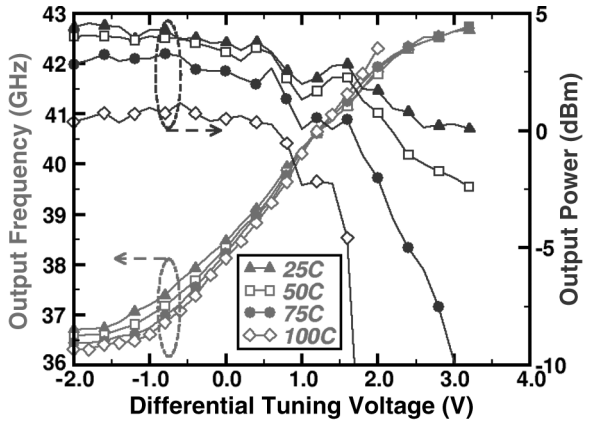


Fig. 12. Measured tuning characteristics and output power of the 40-GHz Colpitts oscillator with differential tuning.

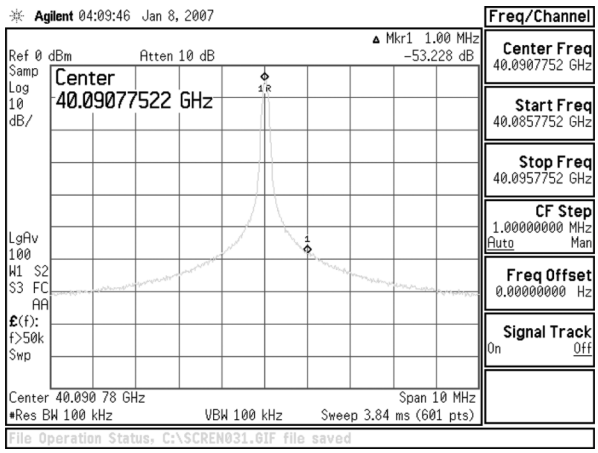


Fig. 13. Measured 40-GHz VCO spectrum showing a phase noise of −103 dBc/Hz at a 1-MHz offset.

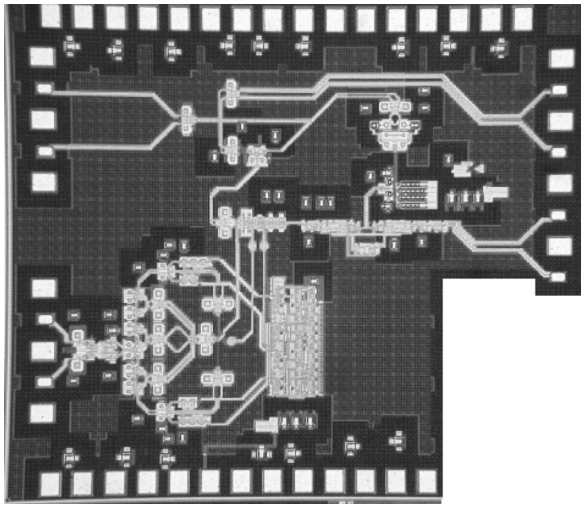

Fig. 14. Die photo of the 86-Gb/s transmitter testchip.

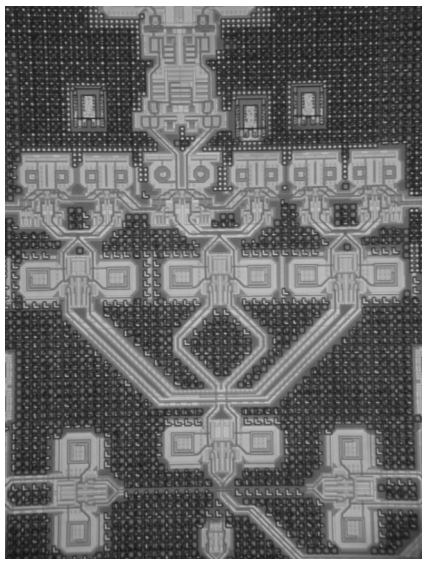

Fig. 15. High-resolution die photo showing layout details of the 43-GHz clock distribution to the final 2:1 MUX.

with DC-to-50-GHz power sensor. The VCO tuning range and output power are depicted in Fig. 12, showing that the VCO is tunable from 36.7–42.7 GHz (15.1%) at room temperature. The oscillation frequency remains remarkably constant over temperatures from 25 °C to 100 °C, which is a direct result of employing a tank which does not rely on base-to-emitter capacitances to set the oscillation frequency. MOS varactors are used instead of p-n varactors. Additionally, capacitor $C_1$ is dominated by a MIM capacitor instead of the $C_{\rm BE}$ of the tank transistor. The measured phase noise is about −103 dBc/Hz at a 1-MHz offset as seen in Fig. 13. It is pointed out that the measured phase noise is lower than the value simulated in Fig. 11, a fact that is not uncommon in high-frequency HBT VCOs [19] and is attributed to the lack of correlation between the base and collector noise current sources in existing BJT/HBT models [20]. The differential VCO consumes 20 mA from a 2.5-V supply.

The die photo of the transmitter IC is shown in Fig. 14 and measures 1.5 mm × 1.8 mm. In half-rate serial transmitter architectures where full-rate retiming is not employed, layout of the clock distribution network is critical to minimize clock skew and avoid duty cycle distortion in the output eye diagram. As seen in the close-up die photo in Fig. 15, all line lengths in the 43-GHz clock path leading to the final 2:1 MUX are closely matched to avoid systematic skew. The transmitter includes an on-chip 40-GHz clock multiplier unit (CMU) which is tunable from 38 to 42 GHz. Due to larger-than-expected PLL noise, the CMU jitter is too high and the transmitter was tested using an external 40-GHz clock. All measurements were performed on-die with a temperature-controlled probe station. Time domain measurements were performed with an Agilent 86100C sampling oscilloscope with 86107A 40-GHz precision timebase and 86118A 70-GHz remote sampling heads. Figs. 16 and 17 depict 80-Gb/s single-ended output eye diagrams with 300 mV and 100 mV per side, respectively, demonstrating a 3:1 variation in output amplitude without degrading the eye quality. Two methods were employed to verify correct multiplexing of the input PRBS sequence. First, the output sequence was captured on the oscilloscope and compared with the ideal $2^7-1$ sequence, as seen in Fig. 18. Additionally, as PRBS sequences are periodic, the sequence length can be determined by examining tone spacing in

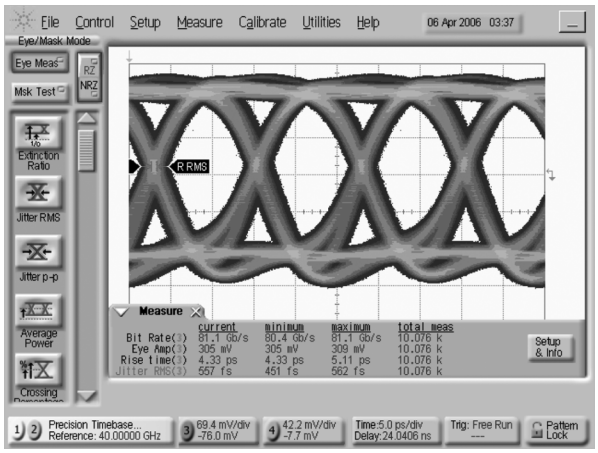


Fig. 16. Measured 80-Gb/s single-ended output eye diagram with 300-mV swing per side.

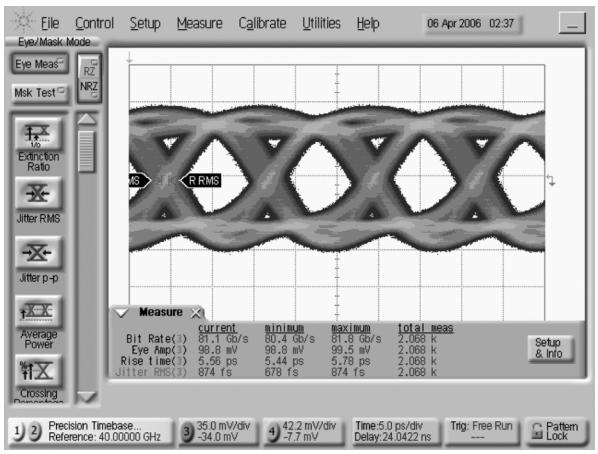


Fig. 17. Measured 80-Gb/s single-ended output eye diagram with 100-mV swing per side.

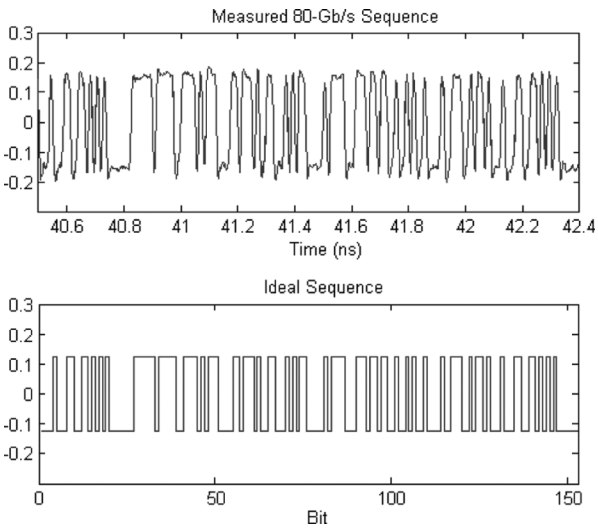


Fig. 18. Measured 80-Gb/s $2^7-1$ output bit sequence and ideal output sequence.

the output power spectrum as seen in Fig. 19. Operation with the external clocking was verified at room temperature over a continuous range of data rates from 5 Gb/s up to 86 Gb/s (Fig. 20),

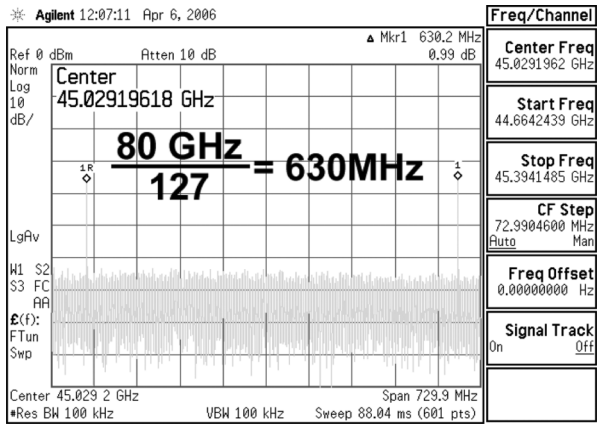


Fig. 19. Measured output spectrum of the 80-Gb/s output pattern demonstrating correct PRBS multiplexing.

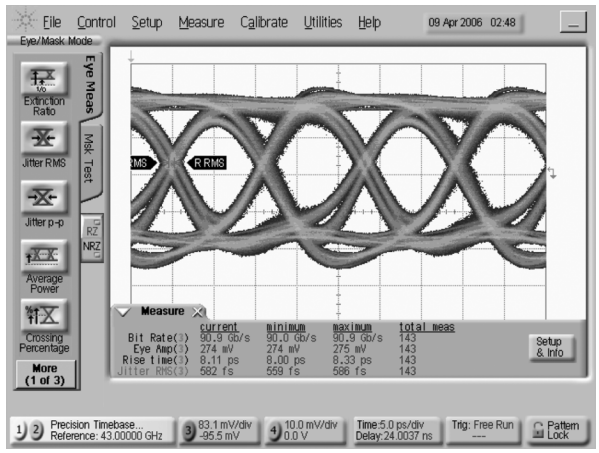


Fig. 20. Measured output eye diagram at the maximum room temperature output data rate of 86 Gb/s.

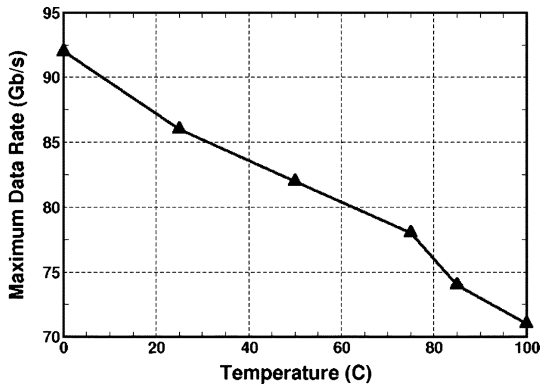


Fig. 21. Maximum output data rate as a function of operating temperature.

although the circuit is expected to operate at even lower data rates. The temperature dependence on the maximum operating data rate is shown in Fig. 21. The transmitter is functional up to 71 Gb/s at 100 °C and 92 Gb/s at 0 °C, as seen in Fig. 22.

The total power dissipation is 996 mW from a 2.5-V supply, and breaks down as follows: 372 mW for the 8:1 MUX, 172 mW for the output driver, 85 mW for the 16:1 frequency divider, 222 mW for the clock distribution, and 145 mW for the on-chip $2^7-1$ PRBS generator. If the 360 mW from the PLL is also

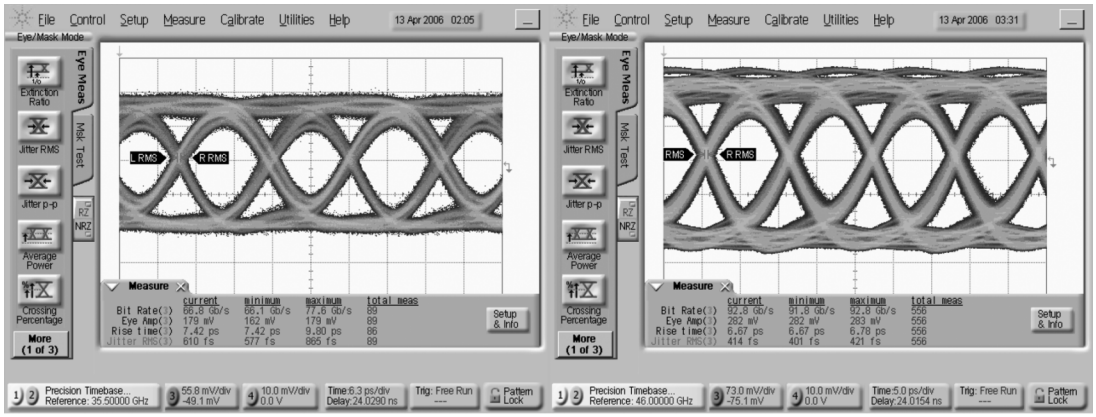


Fig. 22. Measured output eye diagrams over temperature variations. (a) 71 Gb/s at 100 °C. (b) 92 Gb/s at 0 °C.

TABLE I
COMPARISON OF HIGH-SPEED TRANSMITTER POWER DISSIPATION IN VARIOUS TECHNOLOGIES

| Technology | $f_T/f_{MAX}$ | Data rate | Supply Voltage | $P_{DISS}$ | Ref. |
|---|---|---|---|---|---|
| 130-nm CMOS | ~85/90 GHz | 40 (half-rate) | 1.5 V | 2.7 W | [21] |
| InP HBT | 150/150 GHz | 43 (full-rate) | -3.6/-5.2 V | 3.6 W | [22] |
| 180-nm SiGe BiCMOS | HBT: 120/100 GHz | 43 (half-rate) | -3.6 V | 1.6 W | [23] |
| 180-nm SiGe BiCMOS | HBT: 120/100 GHz | 43 (full-rate) | -3.6 V | 2.3 W | [23] |
| 130-nm SiGe BiCMOS | MOS: 85/90 GHz HBT: 150/160 GHz | 86 (half-rate) | 2.5 V | 1.4 W | This Work |

considered, this work demonstrates that an entire 80-Gb/s transmitter can be realized with a power dissipation of about 1.4 W. A comparison with other high-speed transmitters in various semiconductor technologies [21]–[23] is presented in Table I. The 80-Gb/s transmitter in this work achieves lower power dissipation than any 40-Gb/s transmitter reported to date. Comparing with state-of-the-art CMOS results at the same lithography node [21], this work shows that by adding a SiGe HBT to a CMOS process one can achieve a serial transmitter with double the data rate while dissipating half of the power.

## V. CONCLUSION

Low-power design techniques for high-speed building blocks have been presented, allowing for record-breaking performance with low power consumption. Power dissipation is minimized at the building block level by using a low supply voltage and by trading off bias current for inductive peaking. In addition, a methodology for scaling spiral inductors to higher frequencies has been presented, paving the way for their use in millimeter-wave applications. To demonstrate these low power techniques, all of the critical high-speed building blocks for an 86-Gb/s serial transmitter have been designed and verified. Novel 43-GHz BiCMOS latches and 86-Gb/s BiCMOS selectors and output drivers, all operating from 2.5 V, have been presented. To the authors' best knowledge, this marks the lowest supply voltage for circuits at such high data rates in silicon-based technologies. The 130-nm n-channel MOSFETs employed in the 86-Gb/s output driver achieve record-breaking switching speed for MOSFETs, even outperforming recent results in 90-nm and 65-nm LP CMOS technologies [24], [25]. The low power consumption achieved in this work suggests that an entire serial transmitter with CMU operating at 80 Gb/s and dissipating 1.4 W is feasible. Finally by applying the presented design techniques in more advanced SiGe BiCMOS technologies with cutoff frequencies in excess of 200 GHz [26], low-power single-chip transceivers for 100 G Ethernet can be realized.

## ACKNOWLEDGMENT

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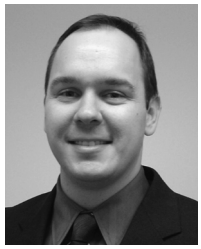

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