# A 2.5-V, 40-Gb/s Decision Circuit Using SiGe BiCMOS Logic

Timothy O. Dickson[1], Rudy Beerkens[2], and Sorin P. Voinigescu[1]

[1]Department of Electrical and Computer Engineering, University of Toronto, Canada

[2]STMicroelectonics, Ottawa, Canada

Email: tod@eecg.toronto.edu

**Abstract**

A 40-Gb/s decision circuit is reported which operates from a 2.5-V supply. It includes a flip-flop, a broadband transimpedance preamplifier, a tuned 40-GHz clock buffer, and a 50-Ω output driver. The flip-flop features a novel BiCMOS CML logic topology, which allows for lower supply voltages as compared with pure bipolar implementations without compromising speed. A mm-wave transformer is used to perform single-ended-to-differential conversion along the 40-GHz clock path.

## Introduction

SiGe bipolar technology has become a popular choice for broadband circuits due to the high $f_T$ of the SiGe HBT and the reliability of the mature silicon-based processing technology. However, the high $V_{BE}$ of the SiGe HBT hinders low-voltage operation. In this paper, a novel BiCMOS logic family is presented that reduces supply voltages through effective use of n-MOSFETs in the high-speed data and clock paths. The family is based on a BiCMOS cascode topology, which is demonstrated to outperform all other cascode configurations available in a SiGe BiCMOS technology. A 40-Gb/s D flip-flop (DFF) is reported from the lowest-supply voltage (2.5V) of any silicon-based flip-flop at this speed.

## MM-Wave BiCMOS Cascode Topologies

Recently, record-breaking high-speed building blocks have been demonstrated in SiGe bipolar technologies [1, 2]. While the performance rivals that found in III-V technologies, the power consumption in these circuits hinders high levels of integration required for single-chip transceivers. The main obstacle in reducing power consumption remains the $V_{BE}$ of the SiGe HBT, which is close to 1V when biased at peak-$f_T$ current densities. Cascades of emitter-followers and bipolar differential pairs, common to high-speed building blocks, limit voltage headroom and can result in supply voltages of 3.3V for ECL [2] and 5V or higher in $E^2CL$ designs [1]. Additionally, modern ECL building block performance is limited by RC delays rather than the forward transit time. The single-largest contribution to gate delay is from the $R_BC_{BC}$ time constant [3]. For a given technology, this product cannot be reduced through layout techniques since any increase in total emitter length to minimize base resistance results in a commensurate rise in base-collector capacitance.

Incorporation of n-MOSFETs into high-speed bipolar topologies can simultaneously alleviate both the supply voltage and input time constant limitations. High-speed digital building blocks such as flip-flops and multiplexers are based on cascode topologies similar to Gilbert cells. The four types of cascode topologies available in a BiCMOS process are illustrated in Fig. 1. In a 0.13-µm technology, the $V_{GS}$ of a standard-threshold n-MOSFET is about 700mV when biased at peak $f_T$. This gives a 200-250mV savings in voltage headroom for each HBT replaced by a standard $V_T$ n-MOSFET. Of greater importance in high-speed digital design is the fact that the input time constant, $R_GC_{GD}$, can be minimized through layout. The gate resistance of a multi-finger n-MOSFET contacted on one side of the gate can be estimated as

$$R_{gate} \approx \frac{1}{3}\frac{\rho_{poly} W_f}{N_f L} + \frac{R_{cont}}{N_{cont} N_f} \qquad (1)$$

where $W_f$ is the MOS gate finger width, $N_f$ is the number of fingers, L is the polysilicon gate length, $\rho_{poly}$ is the silicided polysilicon sheet resistance, $R_{cont}$ is the polysilicon-to-metal1 contact resistance, and $N_{cont}$ is the number of contacts per gate finger. For a given total gate width, gate resistance can be reduced by increasing $N_f$ without increasing $C_{GD}$ since the total gate-drain periphery is unchanged. This yields a lower input time constant over the SiGe HBT. Even for the lowest reported base resistance of 100Ωµm [3] and for typical gate polysilicon sheet resistances of 5Ω per square, the $R_GC_{GD}$ time constant is at least one order of magnitude lower than the $R_BC_{BC}$ time constant.

To validate these findings, test structures were fabricated in a 0.13-µm SiGe BiCMOS technology, with peak-$f_T$ values of 90GHz at 0.25mA/µm and 160GHz at 1.4mA/µm for the n-MOSFET and SiGe HBT, respectively [4]. The MOS and HBT devices were sized for peak-$f_T$ at a bias of 6 mA. Measured $S_{21}$

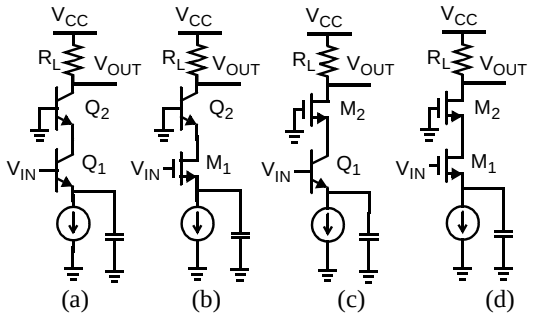


Fig. 1 Cascode structures: (a) HBT (b) MOS-HBT (c)HBT-MOS (d)MOS

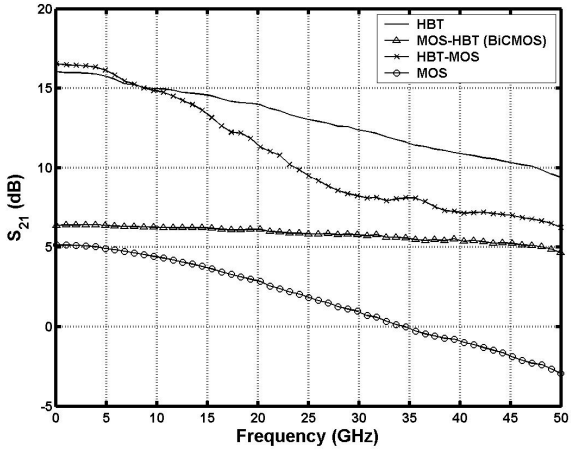


Fig. 2 Measured $S_{21}$ of cascode topologies

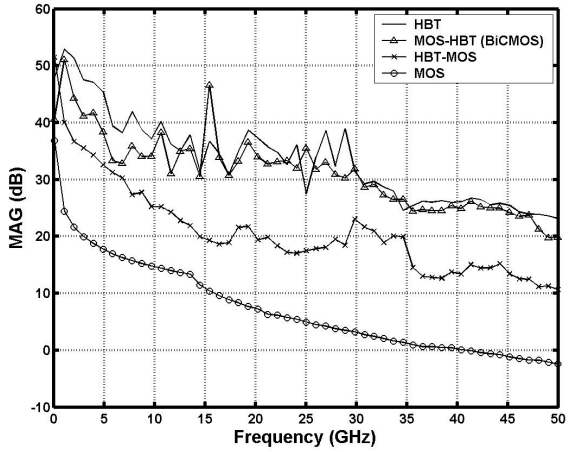


Fig. 3 Maximum available gain (MAG) of cascode topologies

of these structures is shown in Fig. 2, along with the maximum available gain (MAG) extracted from measured S-parameters up to 50 GHz, in Fig. 3. The MOS-HBT topology, hence referred to as the BiCMOS cascode, has a 3-dB bandwidth beyond 50GHz and by far outperforms the other cascode structures. The BiCMOS cascode bandwidth is over twice that of the pure HBT cascode while having comparable MAG up to 50 GHz. Open-circuit time constant analysis shows that the improved bandwidth is due to both the low gate resistance at the input of the amplifier and the low collector-to-substrate capacitance ($C_{CS}$) of the SiGe HBT. The latter is considerably less than the drain-bulk capacitance of the MOSFET for the same tail current. In the HBT-MOS and MOS cascodes, the intermediate time-constant at the source of M2 is comparable to the input and output time constants, and leads to severe degradation of stability and bandwidth. While it is textbook knowledge that the BiCMOS cascode improves op amp stability [5], this work is, to the authors' best knowledge, the first to exploit the benefits of lower gate resistance to improve bandwidth. Its high bandwidth and MAG makes the BiCMOS cascode well-suited for numerous (mm-wave) applications, including low-noise amplifiers, voltage-controlled oscillators, folded-cascode op amps, and low-voltage high-speed logic. The latter will be discussed immediately.

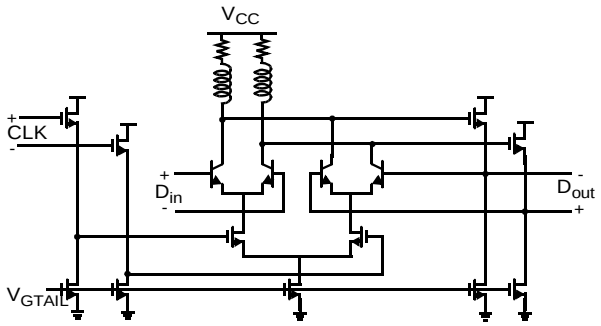


Fig. 4 BiCMOS D-latch

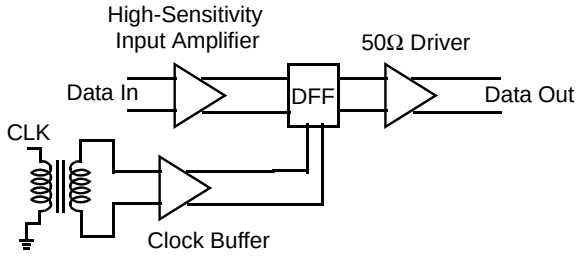


Fig. 5 Decision Circuit Block Diagram

### Proposed BiCMOS Logic

A BiCMOS high-speed logic family is now derived from the BiCMOS cascode discussed in the previous section, and is illustrated in the latch of Fig. 4. Departing from previous conventions in bipolar ECL/CML design, the highest frequency signal is applied to the input of the lower $f_T$ device, the n-MOS differential pair. The lower input time constant at this node is more important in achieving high bandwidth than the transistor $f_T$. While the latch is used as an example, this logic family can more generally be applied to other high-speed building blocks such as multiplexers, where the highest frequency input is the full-rate clock. SiGe HBTs are used for the upper-level data inputs. In digital applications where the output is slew-rate limited, the low $C_{CS}$ of the SiGe HBT results in fast rise and fall times. MOS source followers are used instead of emitter followers to further reduce supply voltage. Low-threshold n-MOSFETs would further reduce the supply voltage to 1.8V. With a 2.5-V supply, sufficient headroom is available for emitter followers along the clock path to extend frequency response beyond 50GHz, but source followers would be required from a 1.8-V supply.

### 40-Gb/s Decision Circuit

The 40-Gb/s decision circuit, consisting of a high-sensitivity input stage, 50Ω output driver, clock buffer, and BiCMOS DFF, is shown in Fig. 5. The DFF is implemented by placing two BiCMOS D-latches of Fig. 4 in a master-slave configuration. The input stage, shown in Fig. 6, is based on a transimpedance feedback amplifier which, while typically employed as a current-to-voltage amplifier, has only recently been considered for use as a voltage preamplifier [6]. Transimpedance feedback lowers the optimal noise impedance, which improves sensitivity in a 50-Ω environment. Appropri-

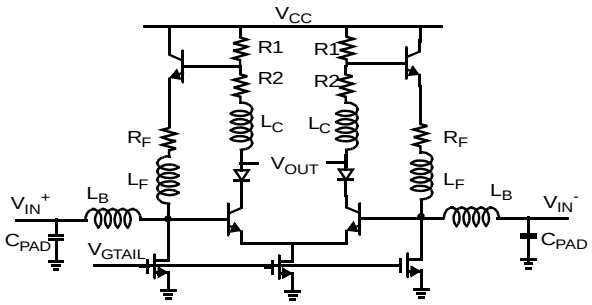


Fig. 6 Transimpedance voltage preamplifier

ate choice of loop gain (A) and feedback resistor ($R_F$) results in a broadband 50–Ω input match given by

$$R_{in} = \frac{R_F}{1 + A} \qquad (2)$$

The 40-fF pad capacitance is tuned out through the use of an input inductor $L_B$, while a feedback inductor $L_F$ reduces the high-frequency noise contribution of $R_F$. Finally, $L_C$ peaks the output node to ensure proper spacing of the open-loop poles for maximally-flat frequency response. The outputs are taken from the collectors of the common-emitter stages to improve gain, and the split resistor load R1 and R2 alleviates headroom concerns. The ratio of R2 to R1 is set to unity for maximum bandwidth [7]. A bipolar differential pair stage follows the TIA stage for additional gain.

The 40-GHz clock is the highest-frequency signal in the decision circuit, making design of a clock buffer challenging. The difficulty is compounded by the inavailability of differential mm-wave signal sources needed for CML applications. Previous designs in the mm-wave regime have either relied on expensive off-chip techniques [1] or area-intensive on-chip rat-race couplers [8] to perform single-ended-to-differential conversions. In this work, the first silicon-based mm-wave monolithic transformer is used to generate differential clock signals from a single-ended signal source. The transformer consists of two coupled symmetric inductors and occupies an area of 45μm x 45μm, which is about $1/100^{th}$ of the area of the 80-GHz rat race coupler [8]. The schematic of the clock buffer is shown in Fig. 7. Two tuned stages are cascaded for additional gain to compensate for limited signal source power and losses in the cabling and transformer. The series addition of small resistors intentionally degrades inductor Q and improves bandwidth of the otherwise narrowband topology. From previous discussions, the BiCMOS cascode is best-suited as an amplifier in this frequency range.

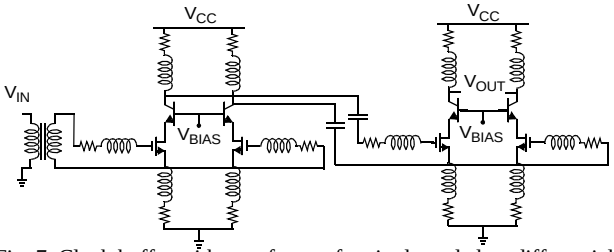


Fig. 7 Clock buffer with transformer for single-ended-to-differential conversion (biasing omitted for clarity)

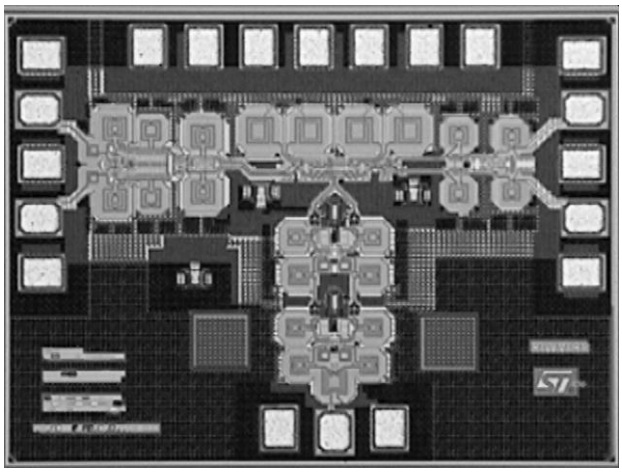

Fig. 8 40-Gb/s decision circuit die photograph

**Experimental Results**

The 40-Gb/s decision circuit was implemented in the 0.13-μm SiGe BiCMOS process mentioned earlier. The chip microphotograph is shown in Fig. 8, and occupies an area of 1.0mm x 0.8mm. The chip contains 24 mm-wave inductors and one transformer (a record for mm-wave silicon circuits), each occupying less than 45μm x 45μm. The circuit consumes 347mW from a nominal 2.5-V supply, and is functional at supply voltages as low as 2.2V. The DFF, input preamplifier, clock buffer, and output driver nominally consume 117mW, 70mW, 68mW, and 92mW, respectively for an output swing of $400mV_{P-P}$ per side. The flip-flop was also measured to operate at half-power (58mW) with less than 5% degradation in speed. Fig. 9 shows single-ended S-parameters measured to 50 GHz for a separate test structure consisting of the broadband input stage and the 50-Ω output driver. The 3-dB bandwidth is over 50 GHz, and input and output return losses are less than -10 dB up to 50 GHz.

Eye diagrams for the 40-Gb/s decision circuit were measured on-wafer. For initial testing, a 12.5-Gb/s $2^{31}$-1 pseudo-random data stream was applied to one of the differential inputs with the other input terminated in 50Ω. A 37.5-GHz clock signal was used so as to achieve synchronization with one of the harmonics of the clock provided by the 12.5-Gb/s

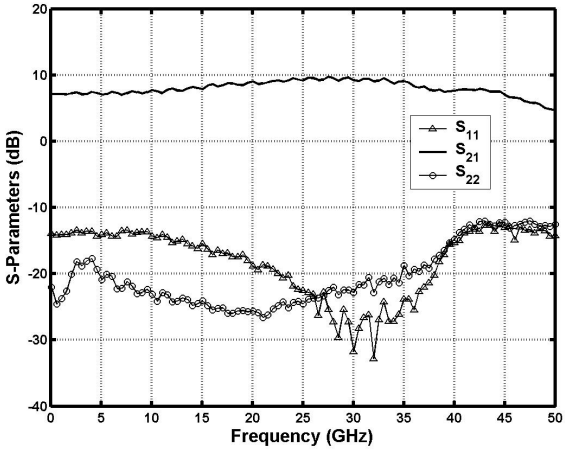


Fig. 9 Measured S-parameters of input amplifier and output driver

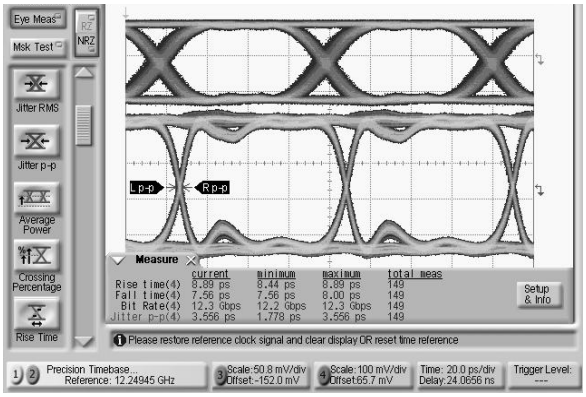


Fig. 10 Input (top) and output 12.5-Gb/s eye diagrams with 37.5-GHz clock signal.

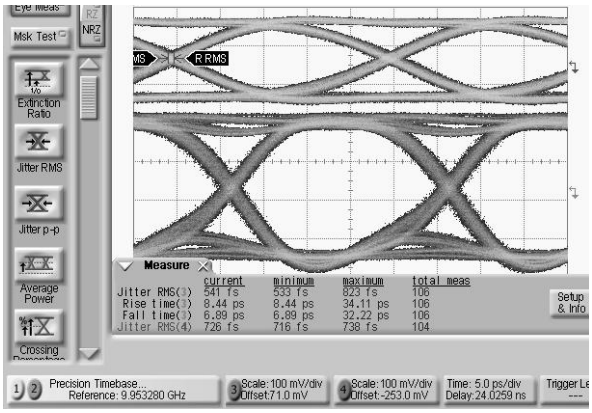


Fig. 11 Input (top) and output 40-Gb/s eye diagrams

Agilent BERT. The retiming function of the circuit is clearly demonstrated in Fig. 10 where the jitter and rise/fall times of the output data are reduced more than two times in comparison with those of the input data. Operation up to 43-Gb/s was verified by applying a $2^{31}$-1 PRBS pattern and 40-GHz clock from an Anritsu 43.5-GB/s MUX and pattern generator to the data and clock inputs, respectively. Again, reduction in the jitter and rise/fall times of the output signal is observed as seen in the 40-Gb/s eye diagrams of Fig. 11. By adjusting the tail current of the DFF latches, the rise and fall times can be varied between 6.5 ps and 9 ps, adequate for 50-Gb/s operation [9]. Also, the quality of the output eye diagram is maintained when the output swing is changed from $150mV_{P-P}$ to $400mV_{P-P}$ per side. Maximum output swing is still observed with a 40-mV signal applied to one input with the other input terminated in 50Ω, indicating high-sensitivity due to the transimpedance input stage.

## Conclusions

A novel BiCMOS logic family has been proposed that reduces the supply voltage from 3.3V to 2.5V while maintaining the speed of pure SiGe HBT ECL circuits. It benefits from the low input time constant of the n-MOSFET and the low output capacitance of the SiGe HBT. A 40-GHz retiming flip-flop which consumes 58mW from a 2.5V supply was implemented using this logic family in a 0.13-µm SiGe BiCMOS process. To the authors' best knowledge, full-rate retiming at 40-Gb/s has only been demonstrated in SiGe BiCMOS circuits from a supply voltage of -5.2V [10]. CMOS CML circuits with 25-GHz clocks have recently been reported in 90-nm CMOS [11], suggesting that 40-Gb/s full-rate retiming in CMOS may not be feasible until the 65-nm technology node. These results indicate that the proposed BiCMOS logic topology is two generations ahead of pure CMOS while at the same time operating from less than half the supply voltage of ECL SiGe HBT implementations.

## Acknowledgments

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