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Curriculum Vitae of

Amir H. ASHOURI

Personal Data

DOB: 1985 - Tehran, IRAN
Status: Permanent Resident (PR) of Canada
PEO: P.Eng. License No. 100511802
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Education

- **January 2017 – July 2019 (2.5 Years -- Expected)**
  Postdoctoral Fellow in Computer Engineering
  University of Toronto (http://www.utoronto.ca)
  Advisor: Tarek Abdelrahman
- **January 2013 – *December 2016 (4 Years)***
  Ph.D. in Computer Science and Engineering
  Politecnico di Milano (http://www.polimi.it)
  Final Thesis: Compiler Autotuning using Machine Learning Techniques
  (https://www.politesi.polimi.it/handle/10589/129561)(**Grade**: Cum laude – w/ honors)
  Advisors: Cristina Silvano, Gianluca Palermo and John Cavazos
- **September 2010 – December 2012 (2 Years)**
  M.Sc. in Computer Engineering
  Politecnico di Milano (http://www.polimi.it)
  Final Thesis: Design Space Exploration Methodology For Compiler Parameters in VLIW Processors
  (https://www.politesi.polimi.it/handle/10589/72083) (**Grade**: 109/110 – A+)
- **January 2005 – Oct 2009 (4.5 years)**
  B.Sc. in Information Technology Engineering
  Iran University of Science and Technology (http://www.iust.ac.ir)

Teaching Experience

- (Mar 2014– July 2016) Teaching Assistant (3 Years), "*Advance Computer Architecture*", Politecnico di Milano - (http://home.deib.polimi.it/ashouri/Courses.html)

- (Mar 2014- April 2014) Invited Seminars, "*Compilers Code Optimizations and Transformation*", Politecnico di Milano - (http://home.deib.polimi.it/ashouri/courses/compiler2014.html)

Research Interests

- Automatic Tuning
- Machine Learning Applications
- Accelerating Deep Learning Applications
- Computer Architecture

Selected Publications *(Full list is available on my Google Scholar profile)*

• **[J3] A. H. Ashouri**, W. Killian, J. Cavazos, G. Palermo, and C. Silvano. "*A Survey on Compiler Autotuning using Machine Learning*" ***ACM Transactions on Computing Survey (CSUR)*** (2018) – Accepted

• **[C4]** C. Silvano, G. Palermo, G. Agosta, **A. H. Ashouri**, D. Gadioli, et al., "*Autotuning and Adaptivity in Energy Efficient HPC Systems: The ANTAREX toolbox*", **ACM Computing Frontiers** *(***CF), 2018**

• **[C3]** D. Gadioli, R. Nobre, P. Pinto, E. Vitali, **A. H. Ashouri**, G. Palermo, J. Cardoso, C. Silvano, "*SOCRATES—A seamless online compiler and system runtime autotuning framework for energy-aware applications*", **IEEE/ACM Design, Automation & Test in Europe Conference & Exhibition** *(***DATE), 2018**

• **[BOOK] A. H. Ashouri**, J. Cavazos, G. Palermo, and C. Silvano. "*Automatic Tuning of Compilers using Machine Learning Techniques*" ***SpringerBriefs 2018*** (ISBN 978-3-319-71489-9). (6 chapters)

• **[J2] A. H. Ashouri**, A. Bignoli, G. Palermo, C. Silvano, S. Kulkarni and J. Cavazos. "*MiCOMP: Mitigating The Compiler Phase-ordering Problem using Optimization Sub-sequences and Machine Learning*" ***ACM Transactions on Architecture and Code Optimization (TACO)*** 14, no.3 (2017): 29.

• **[J1] A. H. Ashouri**, G. Mariani, G. Palermo, E.J. Park, J. Cavazos, and C. Silvano. "*COBAYN: Compiler Autotuning Framework Using Bayesian Networks*" ***ACM Transactions on Architecture and Code Optimization (TACO)*** 13, no. 2 (2016): 21.

• **[W1] A. H. Ashouri**, A. Bignoli, G. Palermo, C. Silvano, "*Predictive Modeling Methodology for Compiler Phase-ordering*", **ACM Workshop of *PARMA-DITAM co-located with HiPEAC Conference***, 2016

• **[C2] A. H. Ashouri**, G. Mariani, G. Palermo and C. Silvano, "*A Bayesian Network Approach for Compiler Auto-tuning for Embedded Processsors*", **IEEE 12th Symposium on Embedded Systems for Real-time Multimedia** *(**ESTIMedia**),* 2014

• **[C1] A. H. Ashouri**, S. Xydis, V. Zaccaria, G. Palermo and C. Silvano, "*A Framework for Compiler-level Statistical Analysis over Customized VLIW architecture*", 21st **IFIP/IEEE International Conference on Very Large Scale Integration (*VLSI-SoC*)**, October 2013, 2013

Research Experience

At University of Toronto (Canada) (Advisor: *Tarek Abdelrahman*) – (http://www.eecg.toronto.edu/~tsa/)

• (Jan 2017-) Conducting research on optimizing deep learning inference task for mobile and embedded devices in partnership with Qualcomm Canada Inc.

• (July 2017-) Conducting research on Sparsification techniques for CNNs

At High Performance Computing and Compiler lab (Supervisor: *John Cavazos*) – University of Delaware (USA) (http://www.eecis.udel.edu/~cavazos/)

• (Dec 2014- March 2016) Collaborating research on compiler optimization for multi/many core systems, targeting power consumption and performance utilizing LLVM-OpenMP, Intel-ICC, etc.

• (Sep 2014- March 2016) Conducting research on compiler optimization using different fine-grain kernel characterizations and utilizing machine learning for compiler auto-tuning utilizing GCC, GCC-ARM

At System Architecture Group (Advisors: *Cristina Silvano*, *Gianluca Palermo*)- Politecnico di Milano (Italy) (http://sagroup.elet.polimi.it/)

- (Sep 2015- Dec 2016) collaborating research on ***ANTAREX*** European Funded High-performance Computing Project (www.antarex-project.eu) on Compiler Phase-ordering and Application Autotuning

- (Jan 2011- July 2015) conducting research on compiler optimization, using machine learning, Design Space Exploration and Static-Dynamic analysis and building tool-chains targeting embedded domain architectures (ARM, VLIW) utilizing compilers such as LLVM, GCC and VEX

Awards and Grants

- (June 2017 - 2019) ***Mitacs Elevate*** Postdoctoral Fellowship: In collaboration with Qualcomm Inc. Canada

- (July 2017- Feb 2018) **HiPEAC** (*European Network of Excellence on High Performance and Embedded Architecture and Compilers*) (http://www.hipeac.net): ***Winner*** of Postdoctoral grant for proposal on *using deep learning to autotune GPU applications*.

- (April 2017) Best IEEE (Italy-section) ***PhD Thesis Award*** of 2016 (http://www.computersociety.it/ieee-computer-society-italy-section-chapter-2016-phd-thesis-award/)

- (March 2016) Microsoft Student Research Competition (**SRC**): Travel grant to ACM/IEEE CGO 2016, Spain

- (July 2014- Feb 2015) **HiPEAC** (*European Network of Excellence on High Performance and Embedded Architecture and Compilers*) (http://www.hipeac.net): ***Winner*** of PhD grant for proposal on *using machine learning for compiler phase ordering*.

- (Dec 2012- Dec 2015): **PhD Fellowship** by Ministry of Science and Technology in Italy

Volunteerism and Service

- (June 2018) Reviewer at *ACM TACO* (Transactions on Architecture and Code Optimization)
- (Jan 2018-) Co-chair of Technical Committee–Professional Engineering Ontario (PEO) – West Toronto Chapter
- Reviewer at *JCST* (Springer Journal of Computer Science and Technology)
- Reviewer at *JPDC* (Elsevier Journal of Parallel and Distributed Computing)
- Subreviewer at *PACT* 2018, *ICTAI* 2016, *DSD* 2017, *ASAP* 2016-17
- Artifact Evaluation Committee at IEEE/ACM *CGO* 2018 (https://cgo18ae.hotcrp.com/users?t=pc)
- Student Volunteer at *HiPEAC 2016*, *Computing Frontiers 2016*, *Supercomputing (SC) 2015*, *FPL 2015*
- Web chair *and* poster-submissions *chair* at *DATE 2016* 1st workshop on RESource Awareness and Application Auto-tuning in Adaptive and heterogeNeous compuTing (***Res4Ant***) (http://res4ant.deib.polimi.it/)