SSCS-South Brazil Chapter Chair Wilhemus Van Noije (left) with SSCS DL Payam Heydari at SEMANITEC 2014.

Prof. Payam Heydari presenting one of SEMINATEC 2014's six seminars, which were also offered by DLs from the IEEE EDS and IMEC, Belgium.

super-pixels was introduced and the design and implementation of a nine-element fully integrated imaging array receiver with on-chip antennas based on this concept.

In addition to the scientific lectures, five semiconductor companies were invited to give half-hour presentations describing their activities and demands of academia and industry for research and human resources in the region. Invited speakers from industry were Dr. Cristiano Krug from CEITEC Federal Research Center, Cleber Figueira from Smart Modular Technologies, Vera Bier from Sansung, Mauricio Kobayashi from Agilent Technologies, and Dr. Eric Fabris from IC Brazil.

In a poster session, 40 technical papers were presented and discussed. The event closed with a panel discussion session about the interaction between universities and industry, in which some of the six SEMINATEC DLs were invited talk about their experiences in this area.

More information about SEMINATEC 2014 is available at http://www.psi.poli.usp.br/seminatec2014.

—Wilhelmus Van Noije,
Chapter Chair

CORRECTION TO "LOOKING INTO A NODE"

There was an error in the Spring 2014 "Circuit Intuitions" column, "Looking into a Node" [1]. In Figure 3 of the article (the corrected figure is shown at right), we were interested in finding v_{d1} and v_{out} in a cascade configuration. We did this by first finding an expression for v_{d1}. In the original article, the final expression for v_{d1} has an extra r_{o1} factor, which is now corrected here. The correct expression for v_{d1} is $v_{d1} = -g_m v_{in}(r_{o1} \parallel R_{eq2})$. The reader notes that this final expression is intuitively obvious as it contains the product of the short-circuit current at v_{d1} and the total resistance looking into v_{d1}.

—Ali Sheikholeslami

Reference

[1] A. Sheikholeslami, "Looking into a Node," *IEEE Solid-State Circuits Mag.*, vol 6, no. 2, pp. 8–10, 2014.

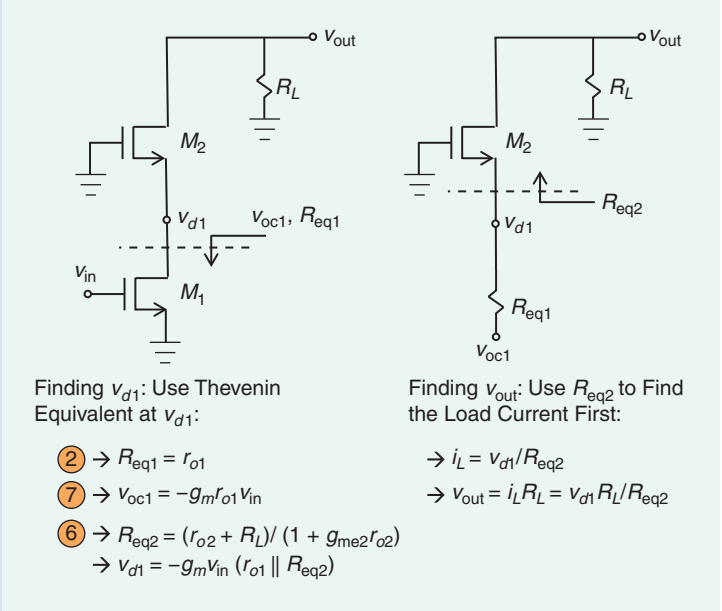

FIGURE 3: Finding v_{d1} and v_{out} in a cascode configuration using library elements.

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