A Blind ADC-Based CDR with Digital Data Interpolation and Adaptive CTLE and DFE

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***Abstract* — This paper proposes replacing the analog phase interpolator in a phase-tracking ADC-based receiver with a digital data interpolator following the ADC. This allows for a blind ADC-based receiver that has a simpler adaptive DFE compared to previous implementations. Our measurements from a 65nm CMOS testchip confirm 7Gb/s operation for a 17dB channel loss.**

***Index Terms* — Adaptation, zero-forcing DFE, linear equalizer, data interpolator, blind ADC-based CDR.**

I. Introduction

ADC-based receivers perform data recovery and equalization in digital domain, eliminating the need for most of the analog front end. In a phase-tracking ADC-based receiver (Fig. 1a), the clock is recovered by phase interpolation (PI) between CK_0 and CK_{90} in the analog domain. As such, the recovered clock is expected to sample the received data in the center of the eye, but is limited by the phase interpolator nonlinearity.

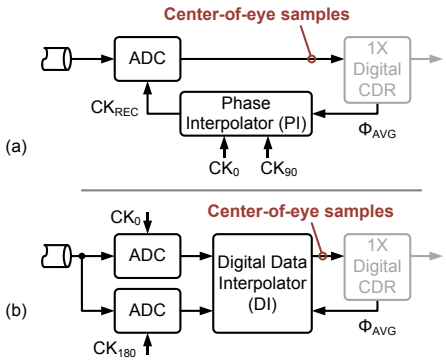

Fig. 1. Comparison of (a) PI-based receiver [1] and (b) proposed DI-based receiver

In contrast, we propose replacing the analog phase interpolator with a simpler digital data interpolator (DI in Fig. 1b). In the proposed receiver, the received signal is sampled twice per UI (once by each of CK_0 and CK_{180}) producing two digital blind samples. These samples are then interpolated in digital domain to estimate the binary data corresponding to the center of the eye. The two systems are functionally equivalent although the proposed system is easier to design and is immune to process, temperature, and voltage variations. The proposed system is also much simpler compared to the one in [2] where an analog data interpolator is used prior to the comparators.

Previously reported 2x blind ADC-based receivers [3,4] equalize the blind samples prior to the data decision. This necessitates storing multiple coefficients for each DFE tap and, therefore, complicates the DFE design and its adaptation. In contrast, the DI simplifies the 2-tap adaptive DFE in the proposed receiver to one coefficient per tap.

II. Proposed Receiver Architecture

Fig. 2 shows our proposed ADC-based receiver system. The main blocks are a continuous-time linear equalizer (CTLE), an 8-way time-interleaved 3-bit flash ADC, CTLE controller, and a digital CDR with an adaptive zero-forcing (ZF) DFE. The linear equalizer is implemented in the analog domain so as not to amplify ADC quantization noise. Each of the 8 interleaved ADCs samples the 7Gbps received signal at 1.75GS/s for an aggregate sampling rate of 14GS/s. The ADC includes automatic offset calibration to improve performance. The 3-bit samples are demuxed into 32 parallel samples at 437.5MHz and passed to the digital blocks. The CTLE controller uses the blind samples to adjust the linear equalization. The use of blind samples allows the CTLE control loop to operate independently of the downstream CDR. The CDR operates at baud rate and is similar to the one described in [5] with modifications to accommodate the adaptive DFE.

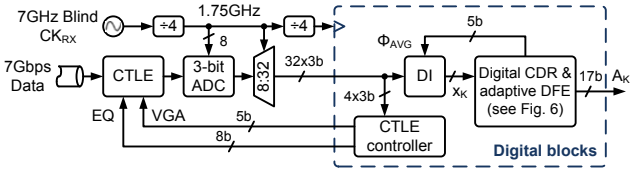

Fig. 2. System block diagram of proposed receiver with an 8-way interleaved 3-bit ADC, CTLE, CDR, and adaptive DFE

The DI interfaces the 2x oversampling ADC with the 1x (baud-rate) CDR by interpolating one data sample from each pair of adjacent blind samples as a function of Φ_{AVG}. The CDR tracks the desired sampling location at the

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center of the eye and provides Φ_{AVG} in a feedback loop to the DI. If a frequency offset exists between the data signal and the blind clock (CK_{RX}), the DI will skip or insert an extra interpolated sample when Φ_{AVG} rolls over. The 1x CDR architecture reduces power by eliminating the interpolation and equalization of edge samples. The use of 2x ADC sampling reduces interpolation error, which, in turn, allows us to reduce the ADC resolution to 3 bits.

A. Adaptive CTLE

The CTLE consists of 4 stages – two with RC source degeneration for high-frequency boost and two with R-only source degeneration for gain control. The CTLE taps, EQ and VGA, are digital signals between 0 to 7 and 0 to 4, respectively. When EQ is set to its maximum (7), the CTLE can equalize 12dB of channel loss at 3.5GHz.

Fig. 3 shows the CTLE controller. During operation, it sweeps through all EQ and VGA settings and measures the quality of the eye by accumulating a cost function over 3,584 samples. The cost function is modified from the common-modulus algorithm (CMA) [6] by approximating the squared operations with absolute values. The decision block picks the final EQ and VGA settings with the lowest cost function.

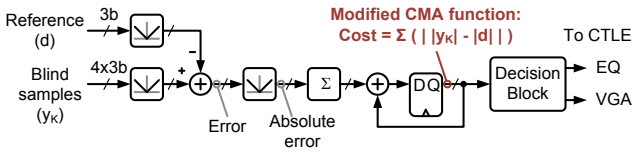


Fig. 3. CTLE controller

B. Adaptive DFE

Least-mean squared (LMS) controllers are commonly used to adapt DFE coefficients [1,3,7,8]. Fig. 4 shows a conventional LMS controller that correlates the error at the output of the DFE summer (e_K) with the recovered bits (A_K) and sends the correlation terms back to the DFE coefficients via the feedback path. The gain, g, must be carefully chosen so that the control loop is stable.

In the proposed work, we use information from a Mueller-Muller PD (MMPD) to adapt the DFE coefficients. It is shown in [9] that the ISI values of a pulse response can be derived from the samples of the received signal and the recovered data (see Fig. 5a). An MMPD provides information to the phase recovery loop, for example, by subtracting two taps (h_{-1}-h_1) [9] or by comparing a tap with a reference (h_0=0) [1]. We will use the same information to drive the DFE coefficients.

Fig. 5b shows the proposed ZF DFE. The sampled received signal (x_K) is correlated with previously recovered data (A_{K-1} to A_{K-N}). The low-pass filters (LPF) approximate the expected value operations and the LPF outputs drive the coefficients of an N-tap DFE summer. The sampled signal, x_K, forms a feed-forward path into the proposed DFE controller. If the bit error rate is assumed to be very small, then the A_K's are essentially equal to the transmitted bits (i.e. they are not affected by the loop dynamics). As a result, the system will have no feedback and, as such, is unconditionally stable. The proposed ZF DFE can be designed with faster convergence than a conventional LMS DFE and is easily scaled as N increases. The LMS DFE in [3] converges in 80µs; the proposed ZF DFE converges in 5µs.

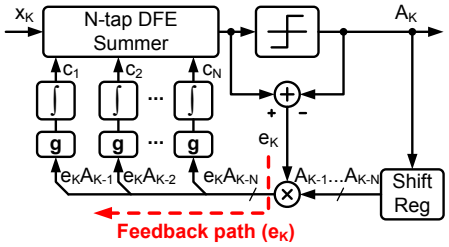


Fig. 4. Conventional least-mean-squared (LMS) DFE [7]

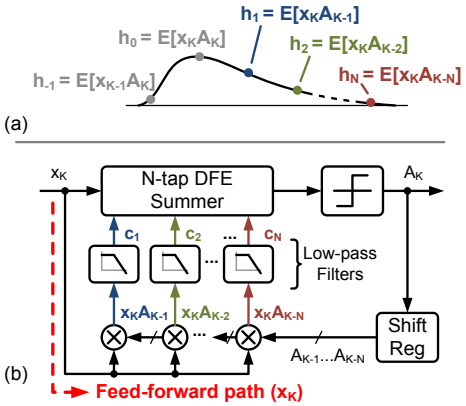


Fig. 5. (a) Pulse response example and (b) proposed adaptive zero-forcing (ZF) DFE

C. System Implementation

Fig. 6 shows the digital CDR and adaptive DFE. The data interpolator, MMPD, and loop filter form phase-tracking loop at the top. The MMPD compares the pre-tap cursor with first post-tap cursor (h_{-1}-h_1). In order to accommodate a wider variety of channels, we added a manually adjustable offset P at the input of the loop filter. At steady state, the CDR locks such that:

$$h_1 = h_{-1} + \frac{P}{K_{DIV} K_{SUM}} \qquad (2)$$

The offset, P, helps the CDR lock to data signals where h_1 is larger than h_{-1} in order to sample the main tap, h_0, at the peak of the pulse response (e.g. Fig. 5a). In this work, we adjust P through test registers by observing the main tap through the ISI monitor output, c_M (described below).

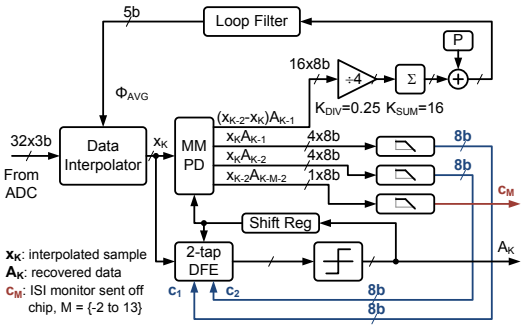


Fig. 6. Baud-rate CDR with adaptive 2-tap ZF DFE

The MMPD block provides three other correlation terms (x_KA_{K-1}, x_KA_{K-2}, and $x_{K-2}A_{K-M-2}$). The first two are used to estimate the first and second DFE taps (c_1 and c_2) as described in the previous section. The LPF blocks are first-order digital filters shown in Fig. 7. The third correlation term provides c_M as an ISI monitor. The integer M, in A_{K-M-2}, can be configured between values of -2 to 13 in order to observe 16 ISI taps.

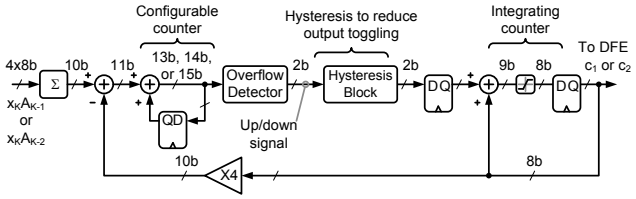
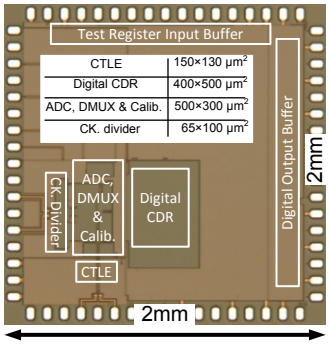


Fig. 7. Low-pass filter used in adaptive ZF DFE

In addition, the MMPD-based architecture in Fig. 6 provides an advantage by decoupling the phase-tracking loop from the DFE adaptation loop. In an Alexander PD-based phase-tracking CDR [8], the PD detects the signal edges at the DFE summer output. Hence, a change in DFE coefficients can shift Φ_{AVG}. At the same time, Φ_{AVG} determines the sampling point, which affects the DFE coefficients. To prevent instability, the DFE adaptation is implemented with much lower bandwidth than the phase-tracking loop – at the expense of increasing the CDR's start-up time. In the proposed CDR, the MMPD locks to the pre-DFE eye. Thus, the DFE does not affect the phase-tracking loop in Fig. 6. Consequently, the DFE adaptation in an MMPD-based architecture can be faster compared to DFE adaptation in an Alexander PD-based architecture.



CTLE	22.7mW
ADC+Demux+ Calib.+Ck.Div.	50.3mW
Digital CDR	32.3mW
Total Power	**105.3mW**
Data Rate	7Gbps
Power FoM	**15mW/Gbps**

Fig. 8. Chip micrograph and power consumption

III. Experimental Results

Fig. 8 shows the chip micrograph of the proposed receiver and its power breakdown. It is fabricated in a 65nm CMOS process and consumes 105.3mW at 7Gbps.

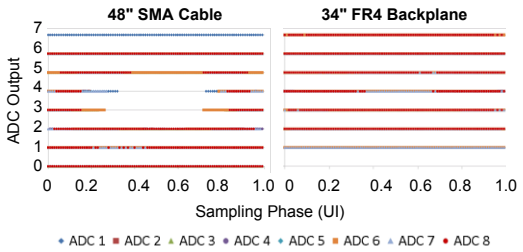


Fig. 9. Measured 3-bit ADC output eye after CTLE adaptation and before DFE

To test the chip, we used a 48" SMA cable and a 34" FR4 backplane (whose attenuations are 1dB and 17dB, respectively, at 3.5GHz). For each channel, we performed the measurements by first asserting the reset signals to the CDR and DFE blocks until the CTLE controller settles on the final tap values (EQ=1, VGA=0 for SMA cable, and EQ=6, VGA=1 for 34" FR4). Fig. 9 shows combined eye diagrams that include the outputs of the 8 interleaved ADCs after the CTLE adaptation. After the CTLE converges, we release the CDR and DFE reset signals simultaneously to achieve phase lock and DFE tap convergence. Figs. 10 and 11 show the adaptation curves of c_1 and c_2 and the eye diagrams at the output of the DFE summer, respectively. The DFE converges within 1 LSB of the final tap values within 5μs.

Fig. 12 shows that c_1 and c_2 converge to near their optimal values (i.e. to the values corresponding to the maximum vertical and horizontal eye openings). Fig. 13 shows the measured jitter tolerance curve. Table I compares the proposed design with previous ADC-based receivers.

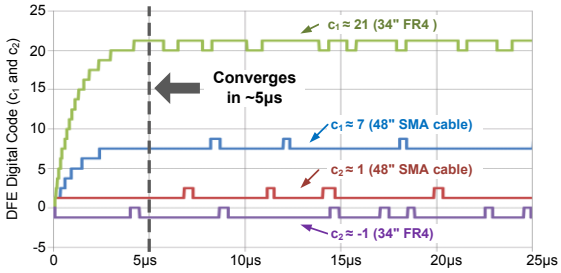


Fig. 10. Measured DFE adaptation curves

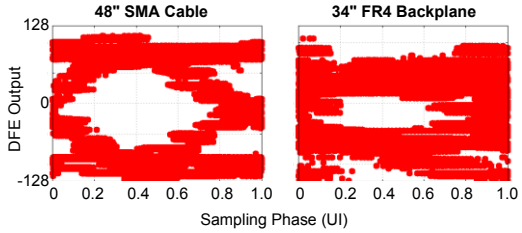


Fig. 11. Measured eye diagrams after the DFE

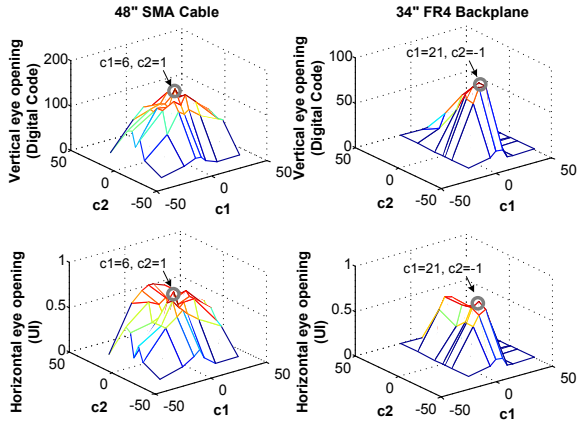


Fig. 12. Vertical and horizontal eye openings at DFE output while sweeping across c_1 and c_2 coefficients

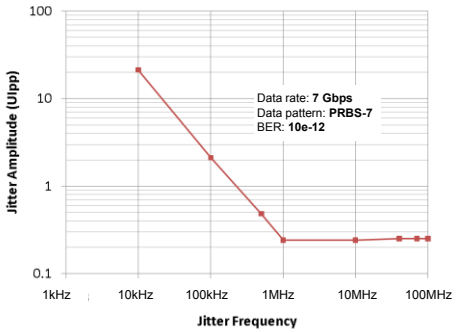


Fig. 13. Measured jitter tolerance

TABLE I
COMPARISON OF ADC-BASED RECEIVERS

	[1]	[3]	[5]	[6]	[10]	This work
CDR Type	Phase-tracking	Blind	Blind	Blind	Blind	Blind
Data Rate (Gbps)	12.5	5	10	5	5	7
Technology	65nm	65nm	65nm	65nm	65nm	65nm
Power (mW/Gbps)	26.4*	38.4**	30.6**	56*	19**	15**
Ch. Loss (dB)	24	13.3	2	15	6	17
DFE?	Y	Y	N	N	Y	Y
Adaptive DFE?	Y	Y	N	N	N	Y
DFE Convergence Time	N/A***	80us	N/A	N/A	N/A	5us
Linear EQ?	Y	N	N	Y	N	Y
Adaptive Linear EQ?	N	N	N	Y	N	Y

* Includes TX and RX **Includes RX only ***Not reported

IV. CONCLUSION

We have presented a blind ADC-based receiver with a 2x oversampling 3-bit ADC, digital DI, baud-rate CDR, adaptive CTLE, and zero-forcing DFE with feed-forward adaptation. The proposed design, fabricated in 65nm CMOS, equalizes up to 17dB of channel loss at 7Gbps.

ACKNOWLEDGEMENT

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