Transient Modeling of Ferroelectric Capacitors for Semiconductor Memories

Ali Sheikholeslami and P. Glenn Gulak
Department of Electrical and Computer Engineering
University of Toronto, Toronto, Canada

Present ferroelectric (FE) capacitor models mostly rely on hysteresis loop characteristics of FE materials. Our experimental results show that this approach overestimates the remanent and saturation polarizations available for nonvolatile semiconductor memories by more than 50%. A behavioral transient model based on pulse measurement results is proposed and implemented as an HSPICE macro-model. The model mainly consists of two nonlinear capacitors, corresponding to the two different polarization states of an FE capacitor.

1. INTRODUCTION

Ferroelectric (FE) capacitors have long been recognized as suitable storage elements for nonvolatile memory cells [1]. Low density FRAMS (such as 2k×8b) are now commercially available and compete with both EEPROMs and battery-backed SRAMs [2]. Higher density FRAMs (such as 32k×8b, 100ns access time) have been successfully designed and tested [3], and the search continues to provide higher density FRAMs with faster read/write time and higher reliability. Meanwhile, FE circuit simulation and optimization are hindered by a lack of accurate CAD circuit models. As a result, current design methods are primitive, and FE circuits are usually designed and margined independently of the actual transient characteristics of the FE capacitor. In fact, the best modeling techniques used presently in memory circuit simulation for this technology only provide for static DC modeling; few transient models have yet been proposed [4].

The complex behavior of an FE capacitor in response to arbitrary voltage patterns is perhaps the main difficulty towards universal modeling of this element. From the circuit point of view, the FE capacitor is a nonlinear element with memory and, hence, has the complexity of both. A nonlinear *but memoryless* capacitor can be modeled behaviorally by a piecewise linear curve in the Q-V plane (charge vs. applied voltage). A nonlinear *with memory* capacitor, on the other hand, is modeled by several piecewise linear curves. Each curve represents a nonlinear capacitor corresponding to a state of the capacitor memory. It is evident, therefore, that the larger the memory depth (the number of memory states), the more complex the model.

For an FE capacitor, the number of states can be very large if a general model is intended. However, only a few states need to be considered if modeling is employed for conventional memory applications such as a 1T-1C FRAM cell (Fig. 1a).

A two-state transition diagram (Fig. 1c) forms the basis of our proposed model. Accordingly, it consists of two distinct parts, corresponding to two distinct states, and an algorithm that dictates switching from one state to another depending on the input pulse polarity. In Section 2 of this paper, we present our experimental results that lead to the construction of each part. Next, in Section 3, we propose the model by incorporating the experimental results into the state transition diagram. As we will see in the same section, such a model easily lends itself to an HSPICE macro-model implementation. Finally, some simulation results will be presented.

2. RESULTS AND DISCUSSIONS

We have used FE capacitor samples from two different vendors, which we refer to as C_A and C_B throughout this paper. C_A is $80 \times 80\ \mu m^2$ while C_B is $100 \times 100\ \mu m^2$ in size. An initial negative pulse brings the capacitor to its negative state (refer to Fig. 1b). After a few seconds, two positive pulses are applied. The first positive pulse stimulates both the switching and the nonswitching current to flow through the capacitor. The second positive pulse only stimulates the nonswitching current [5].

The experiment is repeated 20 times (for 20 different pulse amplitudes uniformly distributed between zero volts and the full supply voltage (10V).

The integral of the transient current is equal to the

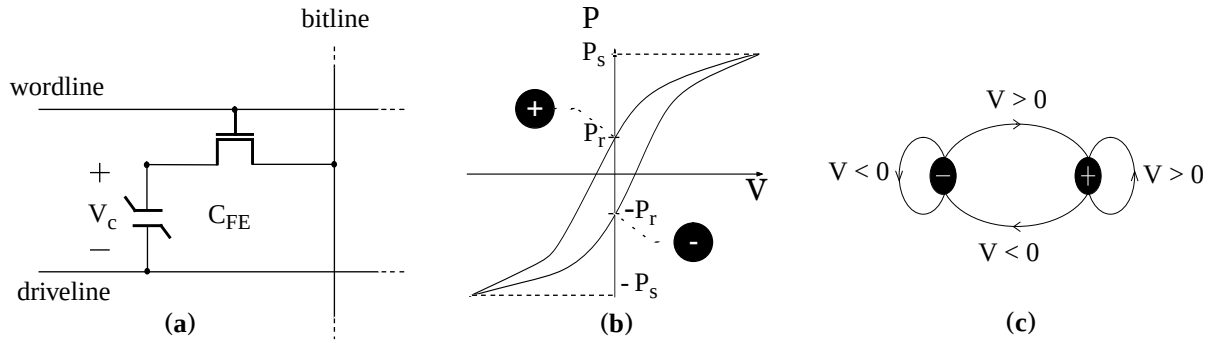

Fig. 1. (**a**) A 1T-1C FRAM Cell, (**b**) Hysteresis Loop employed as a polarization state diagram, (**c**) State Transition Diagram for a two-state capacitor model

incremental charge on the capacitor. This integral corresponds to the P_s+P_r (P_s-P_r) of the hysteresis loop for the first (second) transient current. These parameters are extracted as functions of the pulse amplitude and compared with their corresponding values derived from hysteresis loop measurement in Fig. 2. Part (a) of the figure compares P_s+P_r and P_s-P_r for C_A as derived from pulse measurements (dashed curves) with their counterparts derived from hysteresis loop measurements (solid curves). Part (b) of the figure illustrates similar parameters for C_B.

The hysteresis loop characteristic overestimates P_s+P_r by 85% and 104% for C_A and C_B, respectively. This overestimation is caused by the longer period of the applied signal (1ms instead of 100ns) as well as its periodicity.

2.1 Switching Time

The switching speed of a ferroelectric capacitor from one polarization state to another is a figure of merit for the capacitor in nonvolatile memory applications. This speed is normally characterized by the switching time of the capacitor. In this section, we investigate practical limitations in the measurement of this parameter.

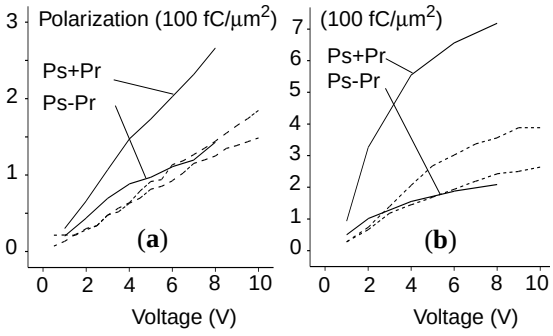

Fig. 2. Hysteresis loop based polarizations (solid curves) versus the transient based polarizations (dashed curves) for (**a**) C_A and (**b**) C_B .

Switching time is defined as the time required for a constant applied voltage to switch the polarization state of the capacitor. In practice, switching time is difficult to measure, since it is much smaller than both the RC time constant of the measurement circuit and the rise time of the applied pulse. In fact, by the time the voltage across the capacitor is constant, the switching has already been completed. Therefore, it remains ambiguous as to what fraction of this time is due to the intrinsic switching time and what fraction is due to the pulse rise time and the RC time constant. A study by Larsen et. al. [6] demonstrates the switching time as a function of the capacitor area. As the area of the capacitor decreases (equivalent to reducing the RC time constant of the circuit), the measured switching time decreases. If this function is extrapolated to where the capacitor area is zero, a switching time of 1.8ns can be predicted. This value is exactly equal to the rise time of the applied pulse. Therefore, the switching time measurement is now restricted by the pulse rise time, which is an instrument limitation. The ideal switching time (not restricted by the RC time constant and the instrument limitation) is expected to be around 100ps [7]. This time is at least one order of magnitude less than the typical RC time constant of a 1T-1C memory cell (refer to Fig. 1). In 0.8 micron CMOS technology, for example, such time constants are around 10ns, assuming a 1pF bitline capacitance and 2:1 ratio for the bitline to the cell capacitance [8].

Based on the above arguments, we neglect the switching time in comparison with the RC time constant of the cell. Assuming zero switching time greatly simplifies the transient analysis of the ferroelectric capacitor. It also reduces the measurement complexity that otherwise is required. We present this analysis in the next section where we will introduce our proposed model.

3. ZERO SWITCHING-TIME TRANSIENT (ZSTT) MODEL

Zero switching-time implies that the charge increment on the FE capacitor will reach its final value instantaneously. Therefore, the charge increment is only a function of the applied voltage and the initial state of the capacitor, not a function of time. In other words:

$$\Delta Q = \Delta Q(V, Q_{init}) \quad (1)$$

where V and Q_{init} represent the applied voltage and the initial polarization charge on the capacitor, respectively. Since there are only two initial states that are important to a memory cell (i.e. digital 0 and 1), the above equation can be broken into two parts, each corresponding to one initial state. In other words:

$$\Delta Q = \begin{cases} \Delta Q_0(V) & \text{for digital 0 state} \\ \Delta Q_1(V) & \text{for digital 1 state} \end{cases} \quad (2)$$

Each part of Equation 2 represents, in general, a nonlinear function of voltage that must be determined. Let us first determine ΔQ_0. A digital zero state corresponds to the positive polarization state of the capacitor. A positive voltage, in this case, results in a polarization increment of P_s-P_r whereas a negative voltage results in a charge decrement of P_s+P_r . Both of these parameters are functions of the applied voltage, and determined experimentally. Noting that a charge increment is equivalent to a polarization increment multiplied by the capacitor area, we have:

$$\Delta Q_0(V) = A\{P_s(V) - \mathrm{sgn}(V)P_r(V)\} \quad (3)$$

where A represents the capacitor area and sgn(V) represents the signum function that is equal to -1 for negative values and +1 for positive values of V. A similar argument for the digital 1 state results in:

$$\Delta Q_1(V) = A\{P_s(V) + \mathrm{sgn}(V)P_r(V)\} \quad (4)$$

Equations 3 and 4 form the basis of the ZSTT Model. The accuracy of these equations depends on the accuracy of the two functions P_s(V) and P_r(V), that are determined by curve fitting to the experimental data. Therefore, their accuracy depends on the number of data points as well as the measurement accuracy. When there is a sufficient number of data points, measurement accuracy is the limiting factor in the overall accuracy.

The experimental results for C_A and C_B presented in the last section can be directly substituted into Equations 3 and 4 to determine ΔQ_0 and ΔQ_1 for each capacitor. Since 20 data points are used between 0 and 10 V, such a direct substitution results in a piecewise linear function with 37 breakpoints between -10 and 10 V. However, simple inspection of Fig. 2 reveals that P_s+P_r and P_s-P_r for C_A (C_B) can be approximated by 2 (6) straight lines if a 5% error is tolerable. As a result of this approximation, ΔQ_0 and ΔQ_1 have only 1 (5) break points in the full domain of ΔQ_0 and ΔQ_1 .

The piecewise linear approximation of ΔQ_0(V) and ΔQ_1(V) results in two piecewise linear capacitors that can be implemented in most circuit simulators. We present an HSPICE implementation of the model in the following.

3.1 Model Implementation

A circuit representation of the ZSTT Model is shown in Fig. 3. $C_0(V_0)$ and $C_1(V_1)$ represent the two nonlinear capacitors corresponding to the two binary states of the FE capacitor. For binary state 0, switches S_{01} and S_{12} are closed while switches S_{11} and S_{02} are open. In this case, the equivalent capacitance looking into the input terminals is $C_0(V_0)$. Meanwhile, a voltage controlled voltage source, which is equal to V_i , is connected to $C_1(V_1)$ to initialize this capacitor for the opposite binary state. For binary state 1, the states of the switches are the reverse: switches S_{11} and S_{02} are closed while switches S_{01} and S_{12} are open. Therefore, the capacitance looking into the input terminals is $C_1(V_1)$, and the controlled source is connected to $C_0(V_0)$ for the similar reason mentioned above.

The ZSTT Model can be easily implemented as an HSPICE macro-model if the two nonlinear capacitors in Fig. 3 are replaced by their piecewise linear approximations. The switches can be replaced

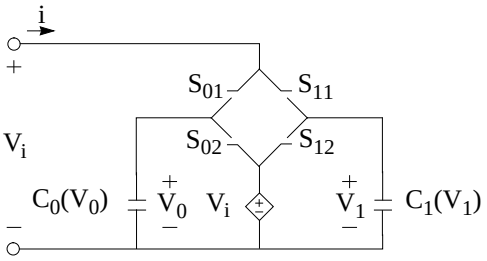

Fig. 3. An implementation of the ZSTT Model.

by voltage-controlled resistors (VCRs) that exhibit high and low resistances for the open and closed states of the switches, respectively.

4. SIMULATION RESULTS

The ZSTT Model can be used to simulate the electrical behavior of an integrated FE capacitor in any of the standard memory configurations. In this section, we present an example of such a simulation. In particular, we use this model in conjunction with the 1T-1C FE memory cell (Fig. 1a) to simulate an FRAM read operation.

A typical decision made during the course of any FRAM design is the selection of an appropriate capacitor area given certain design parameters. A transient simulation of a read operation is useful in making this selection. We wish to determine (for C_A and C_B) the area that results in an identical 100 mV differential signal on a 1-pF bitline.

The dielectric thickness, for both C_A and C_B, is optimized for 10 V supply operation. However, it is expected that the capacitors would behave similarly if the thickness was decreased for 5 V supply operation. Therefore, we assume that the horizontal axes in Fig. 2 can be scaled down to 5 V without changing the polarization parameters.

As shown in Fig. 4, the wordline (WL) and driveline (DL) in both designs are driven by identical pulses, having 1ns rise time. The capacitor sizes are then optimized, an incremental process requiring several simulation runs, to obtain the same differential voltage (100mV) on the bitline for the digital 1 and 0 stored data. The scaled sizes are predicted to be 11 μm^2 and 5 μm^2 for C_A and C_B, respectively. Therefore, an area saving of 54% is expected by using vendor B capacitors. Fig. 4 illustrates the final simulation results.

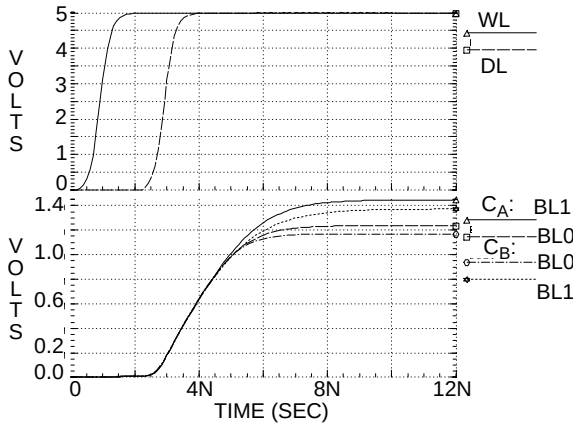

Fig. 4. HSPICE simulation results for the read operation of a 1pF-bitline FRAM using optimized sizes of C_A and C_B

5. SUMMARY

The switching time of the FE capacitor can be neglected in comparison with the RC time constant of a memory cell. Based on this argument and pulse measurement results, a new transient model was proposed and implemented as an HSPICE macro-model. The model was used to optimize the capacitor sizes for a read operation in a 1T-1C FRAM design.

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