A Multiple-Valued Ferroelectric Content-Addressable Memory

Ali Sheikholeslami, P. Glenn Gulak, and Takahiro Hanyu

Abstract

A novel architecture for a Multiple-Valued Ferroelectric Content-Addressable Memory (FCAM) is proposed. An FCAM employs ferroelectric capacitors as storage elements to provide a nonvolatile content-addressable memory. A 2-bit search operation is performed by a simultaneous access to a 4-level polarization, hence reducing the total number of search operations to half. Four FCAM structures are discussed in terms of their speed, area, and implementation feasibility.

1. Introduction

Content-Addressable Memories (CAMs) are used in several applications ranging from look-up tables to artificial neural networks. Many of these CAMs are designed with dynamic circuits to achieve a higher density than that of SRAM-based CAMs. However, dynamic CAMs need a stand-by power supply as well as periodic refreshing of their contents even during periods when the CAM is not being searched. A nonvolatile CAM, proposed by T. Hanyu et al. [1], uses floating-gate MOS devices to eliminate the stand-by-power-supply problem but does not support real-time programming, which may constrain the CAM-based application.

A ferroelectric (FE) capacitor can be used to store binary data, and hold the data without refreshing and stand-by power. Also, a data write into an FE capacitor takes the same amount of time as a data read. Two structures are proposed in this paper that exploit the above properties of FE capacitors to implement a nonvolatile binary CAM that supports real-time programming. Moreover, two bits of data are combined in a unified cell and accessed simultaneously to produce a 4-level polarization. Using this technique, a new multiple-valued FCAM is proposed that combines a higher speed per bit with the advantages of a binary FCAM.

Ali Sheikholeslami and P. Glenn Gulak are with the Department of Electrical and Computer Engineering, University of Toronto, Ontario, Canada, M5S 1A4. Phone (416) 978-1652, Fax: (416) 971-2286. Takahiro Hanyu is with the Department of Computer and Mathematical Sciences, Graduate School of Information Sciences, Tohoku University, Sendai 980-77, Japan. Phone (+81) 22-217-7154, Fax: (+81) 22-263-9401. **This work was supported by Nortel and the Natural Sciences and Engineering Research Council of Canada.**

1.1 Ferroelectric Capacitor

An FE capacitor is physically distinguished from a regular capacitor by substituting the dielectric with an FE material. Two important characteristics of this material are its high permittivity and its bistability. Higher permittivity of the capacitor allows its integration in much smaller area than a regular capacitor. For example, the permittivity of PZT, a typical FE material, is at least one order of magnitude larger than the silicon dioxide employed in typical ASIC processes. As a result, the size of the FE capacitor would be about the size of a source or drain contact, say 2μm by 2μm. In addition, the FE capacitors can be fabricated directly on top of the access transistors. The size of the memory cell is therefore constrained by the size of the access transistor.

An FE capacitor is capable of storing one bit of data in the form of electric polarization [2]. Figure 1 shows our notation for an FE capacitor along with its so-called hysteresis loop characteristic. When the voltage across the capacitor is 0, the capacitor remains in either a negative polarization state (corresponding to a digital state 1) or a positive polarization state (corresponding to a digital state 0). Assuming the capacitor is in state 1, a positive pulse will bring it to state 0, while a negative pulse will not affect its state. Similarly, a negative pulse can flip the state of an FE capacitor whose initial state is a 0.

An FE capacitor constitutes the core of an FE memory cell. Figure 2 shows a binary memory cell utilizing one FE capacitor and one access transistor (hence called 1T-1F

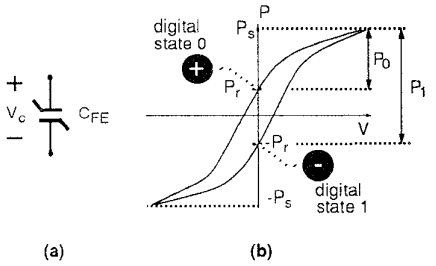


Figure 1. (a) A ferroelectric capacitor (b) Hysteresis loop employed as a polarization state diagram

0-8186-7392-3/96 $05.00 © 1996 IEEE

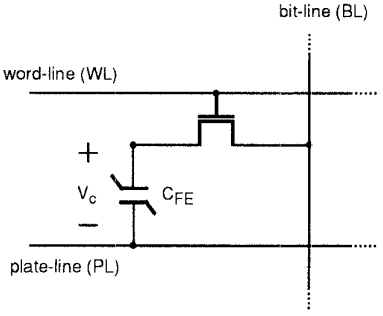


Figure 2. A conventional 1T - 1F binary FRAM cell

memory cell). The cell is activated through the word-line (WL), and written or read through the bit-line (BL) and plate-line (PL). In writing a binary digit 0 to the cell, a positive voltage (normally the full power supply, V_{DD}) is applied to BL while PL is grounded and WL is asserted. In writing a binary digit 1, a positive voltage is applied to PL while BL is grounded and WL is asserted.

Reading the stored data consists of a sequence of precharging BL, asserting WL, pulsing PL, and sensing the voltage developed on BL by a sense amplifier. Since the reading procedure is destructive, the sensed data must be written back to the memory cell. This will be automatically done after the data is latched in the sense amplifier by restoring PL back to ground level.

Multilevel storage of data in a single FE capacitor faces some difficulties, as the present FE materials and technologies do not support a reliable storage of multilevel polarizations. However, it is possible to store multibit information using more than one capacitor in each cell. One example of such a strategy is shown in Figure 3, where two FE capacitors are used to store 2 bits of information. The area of C_{FE2} is twice the area of C_{FE1}. Therefore, four voltage levels can be distinguished on BL if both access transistors M_1 and M_2 are turned ON, and PL_1 and PL_2 are pulsed high simultaneously. The lowest and highest voltage levels are sensed on BL when both C_{FE1} and C_{FE2} are holding a digital state 0 or 1, respectively. The second lowest voltage level corresponds to a 1 on C_{FE1} and a 0 on C_{FE2} , and the second highest voltage level corresponds to a 0 on C_{FE1} and a 1 on C_{FE2}.

The 2-bit cell of Figure 3 is combined later with a multilevel CAM cell to propose a novel multiple-valued FCAM.

1.2 Content-Addressable Memory

A CAM searches for data by content rather than by address. Thus, a CAM is distinguished from a conventional address-based RAM which searches for a data at a

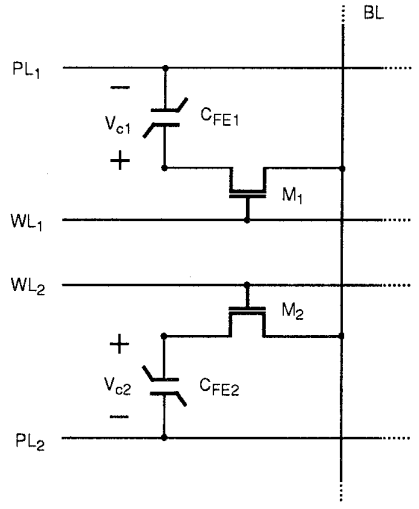


Figure 3. A 2-bit binary FRAM cell

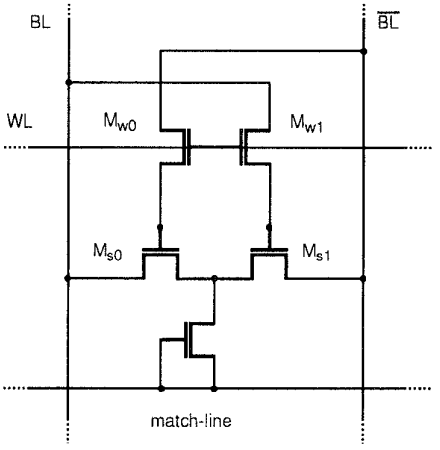


Figure 4. A conventional binary dynamic CAM cell [3]

particular address. One application of CAMs is in an electronic spelling checker, where it is merely searched to locate a word with a specific spelling. If there is at least one word with the same spelling as the input word, the search has been successful.

A binary CAM cell, referred to as a conventional dynamic-type CAM cell, is shown in Figure 4 [3]. The binary data is stored on the gates of two storage transistors M_{s0} and M_{s1} via two access transistors M_{w0} and M_{w1}, respectively. Due to substrate leakage, the stored data must be refreshed on a regular basis (and hence the word dynamic-type). If WL is disabled, the digital state of the match-line will be determined by the exclusive-nor of the

stored data and the reference data (BL data). Therefore, a mismatch pulls down the match-line to ground level while a match will leave the match-line in its precharged high level.

Several cells can be laid out in a row with a common match-line to implement a word. The match-line, in this case, is pulled low if any stored bit does not match its corresponding reference bit.

Aside from equality search in CAMs, there are Greater-Than (GT) and Less-Than (LT) searches that prove useful in some applications [4]. A GT search for an n-bit word can be accomplished in a bit-serial approach using n sequential steps.

1.3 Multiple-Valued CAM cell

T. Hanyu et al. [1] have proposed an indirect approach for multiple-valued data search. Each search consists of two logic value conversions and a threshold operation. The proposed multiple-valued CAM cell for one digit is shown in Figure 5. The capacitor in the cell is used for both storing the multiple-valued data and summing up the stored data with the multiple-valued single-digit input data. The transistor performs the threshold operation by pulling the match-line down if the sum is greater than its threshold and leaving it unchanged if the sum is equal to or less than the threshold. The proposed cell has an apparent advantage over the conventional dynamic cell in terms of area. We will integrate this cell with the multibit FE memory cell described earlier to propose a novel multiple-valued, nonvolatile FCAM cell.

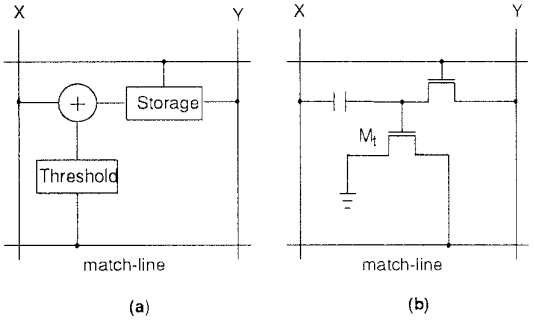
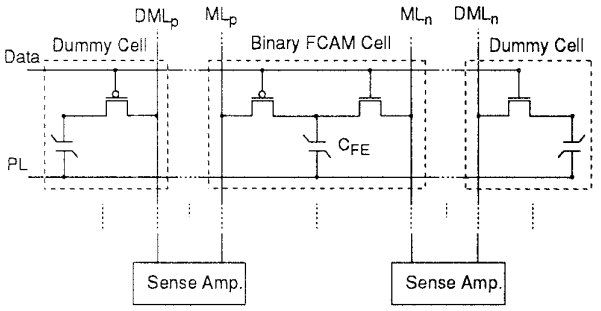


Figure 5. (a) A block diagram and (b) a circuit diagram of a 2T-1C multiple-valued CAM cell [1]

2. Proposed Binary FCAM

There are several architectures for data access and comparison in a CAM [5]. In a word-serial, bit-parallel architecture, the words are compared, one by one, against the reference word. On the other hand, a bit-serial, word-parallel architecture compares one-bit of each word in a CAM against the corresponding bit of the reference word.



Reference Data	Stored Data	(MLp, ML_n)	Conclusion
0	0	(0, 1)	ref. data = sto. data
0	1	(1, 1)	ref. data < sto. data
1	0	(0, 0)	ref. data > sto. data
1	1	(0, 1)	ref. data = sto. data

Figure 6. A complementary 2T-1F binary FCAM cell

Assuming a CAM with w n-bit words, a search operation using word-serial, bit-parallel architecture requires w clock cycles while a bit-serial, word-parallel architecture requires n clock cycles. If $n << w$, a bit-serial, word-parallel architecture is advantageous in terms of search speed. In the rest of this paper, we focus on bit-serial, word-parallel architecture.

A proposed binary FCAM is shown in Figure 6. The FCAM cell resembles that of the FRAM, except for an additional PMOS transistor and different labeling of lines. WL and BL in an FRAM are replaced by the Data-Line (DL) and the Match-Line (ML) in an FCAM, respectively. All PMOS transistors in the same column are connected to ML_p, and all the NMOS transistors are connected to ML_n. There exist also two dummy cells per row of the FCAM, that are connected to two dummy match-lines (DML_n and DML_p). Binary data is written into an FCAM cell in a way similar to a write in an FRAM. A comparison between the stored data and the reference data is made by first writing a 1 and then a 0 into the dummy cells connected to the DML_n and the DML_p, respectively, then precharging the match-lines, bringing DL to the logic value of the reference data, pulsing PL, and enabling the sense amplifiers.

The precharging levels for ML_n and ML_p are different from that of DML_n and DML_p, respectively. ML_n and ML_p are precharged to $(V_{DD}/2 - \Delta V)$ and $(V_{DD} + \Delta V)$, respectively, whereas the DML_n and DWL_p are both precharged to $V_{DD}/2$. In a step sensing scheme [6], ΔV is

given by the following equation:

$$\Delta V = (\Delta V_1 - \Delta V_0)/2 \qquad \text{(eq. 1)}$$

where ΔV_0 and ΔV_1 are the voltage increments on the match-line when the stored data is a 0 and a 1, respectively.

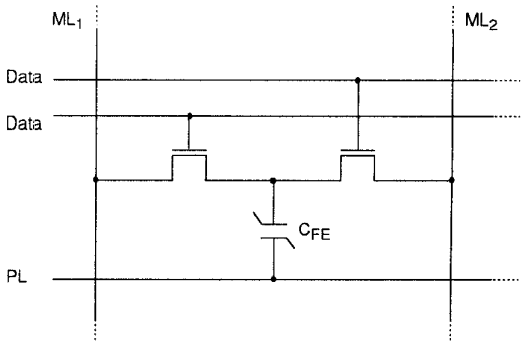
If the reference data is a 1, the voltage on ML_n will increase by either ΔV_0 or ΔV_1, depending on the stored data, while ML_p remains unchanged. Upon enabling the sense amplifier, ML_n will latch to a 1, for the stored data 1, or to a 0, for the stored data 0, while the ML_p will latch to a 0. These results are summarized in a table in Figure 6 along with similar results for the case where the reference data is a 0. The last column of this table shows how a decision can be made by knowing the logic levels of ML_p and ML_n. An exclusive OR (not shown in the figure) of the final logic values of ML_n and ML_p provides the equality signal, an AND gate provides the result of an LT search, and a NOR gate provides the result of a GT search.

The FCAM cell as presented in Figure 6 has several advantages over a conventional binary CAM cell. First, it is nonvolatile, as the FE capacitor can hold its stored data without an applied voltage. Second, it uses a single power supply for both writing into a cell and relational search. Third, the occupied area of the proposed cell is mainly due to the two access transistors—the FE capacitor is normally mounted on top of the transistors—and is smaller than that of the conventional dynamic cell.

The FCAM cell of Figure 6 has a drawback: if the number of cells per row is increased beyond a certain limit and hence increasing the parasitic capacitance on PL, a data comparison in one row can affect the stored data in other rows. This is because one of the two access transistors in each cell is always ON, hence connecting its corresponding FE capacitor to a match-line. The FE capacitor is in series with the parasitic capacitance on PL, providing a capacitor divider that divides the voltage on the match-line in favor of the FE capacitor if the PL capacitance is large enough. In order to avoid this problem, an alternative design is proposed in Figure 7, where the PMOS transistor is replaced with an NMOS one, and the two access transistors are controlled via different data-lines (DL and $\overline{DL}$). When the access is made to a specific row of the array, both DL and $\overline{DL}$ of all other rows can be set low and, therefore, disconnecting the unaccessed FE capacitors from the match-lines. This cell has also an area advantage due to using NMOS transistors only.

3. Proposed Multiple-Valued FCAM

A comparison of FRAM with Flash memory, presently



Reference Data	Stored Data	(ML_1, ML_2)	Conclusion
0	0	(0, 1)	ref. data = sto. data
0	1	(1, 1)	ref. data < sto. data
1	0	(0, 0)	ref. data > sto. data
1	1	(0, 1)	ref. data = sto. data

Figure 7. A 2T-1F binary FCAM cell

the most common type of nonvolatile memory, reveals that an FRAM is much faster in writing data into the memory. One trend in nonvolatile memories that has appeared recently [7] is the emergence of commercial multiple-valued Flash memories. FE memories must follow suit in order to compete in terms of storage density and speed per bit. In this section, we propose two types of multiple-valued FE memory circuits for building nonvolatile CAMs.

Figures 8 and 9 illustrate two proposed structures for a multiple-valued FCAM along with their corresponding timing diagrams for a multiple-valued threshold operation. Any relational search operation, such as the GT, LT, or equality search, can be performed by a combination of two multiple-valued threshold operations [1].

Multiple-valued data is stored in the form of multibit data in a multibit FRAM cell. A 2-bit FRAM cell is employed in Figure 8 to store two bits of information. Also, there is a 2-bit register per column that allows a momentary storage of the sensed data during the threshold operation.

Referring to the timing diagram of Figure 8, a threshold operation begins with a sequential read of the 2-bit stored data by sequentially pulsing WL_1 and PL_1, and then WL_2 and PL_2. Each read includes an automatic write-back, as mentioned in the introduction, as well as a momentary write into the 2-bit register. Next, the two FE capacitors are accessed simultaneously to dump their charge on BL by pulsing PL_1 and PL_2. This will cause a voltage increment on BL that can take any of the four possible levels depending

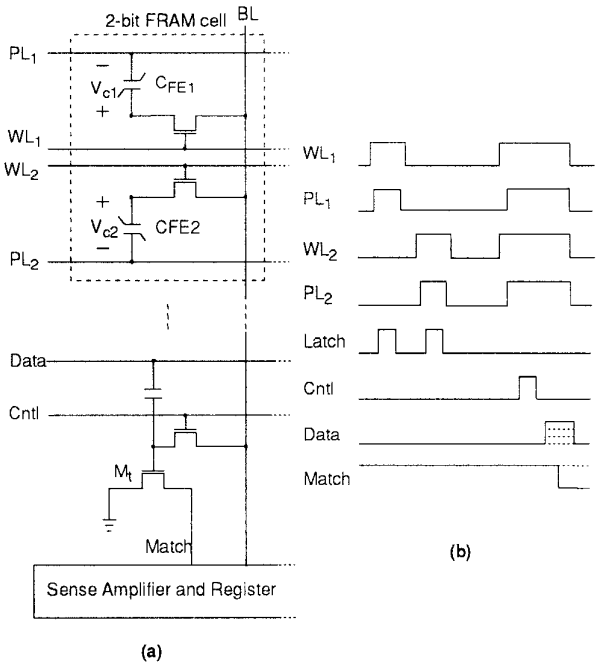


Figure 8. (a) A sequential-access structure for a multiple-valued FCAM (b) The timing diagram for a multiple-valued threshold operation

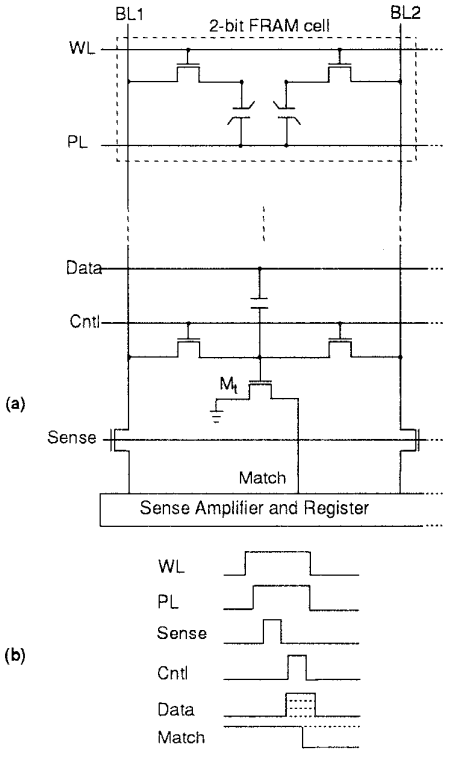


Figure 9. (a) A parallel-access structure for a multiple-valued FCAM cell (b) The timing diagram for a multiple-valued threshold operation

on the stored data. By pulsing the control signal (Cntl), the multilevel voltage will appear on the gate of transistor M_t. The multilevel reference data (or its converted version) is then added to the gate of M_t via the capacitor coupling. This sum will turn M_t ON or OFF depending on whether the sum is greater or less than the transistor threshold, respectively. The threshold operation is completed by writing back the contents of the 2-bit register to the 2-bit FRAM cell (not shown in the timing diagram).

The timing diagram of Figure 8 suggests that a total of at least 4 access times are required to complete a threshold operation; two separate reads, one simultaneous read, and a write-back. This speed can be greatly enhanced by a parallel read as proposed in Figure 9. The two FE binary cells in this figure share the same WL, instead of the same BL. C_{FE1} sends its data to BL_1 while, simultaneously, C_{FE2} sends its data to BL_2. Also, the sensing procedure and the data storage for the final write-back can be performed in parallel with the summing operation by disconnecting the sense amplifiers from the bit-lines after enough charge is developed on the bit-lines. As a result, the threshold operation requires 2 access times less than that of the proposed structure in Figure 8. The reduction of 2 access times in completing a threshold operation does not come for free; the four voltage levels are reduced to half of their counterparts in Figure 9. This is due to doubling the total bit-line capacitance, that is the sum of the capacitances of BL_1 and BL_2.

Table 1 compares different CAM types discussed in this paper. In summary, the sequential-access architecture requires a simpler sense amplifier design while the parallel-access architecture enjoys a higher speed-per-bit performance.

4. Discussion and Conclusions

Several structures were proposed for multiple-valued, nonvolatile FCAMs. A parallel-access structure for a multiple-valued FCAM provides a faster search time than its binary counterpart, while a sequential-access structure provides a higher charge level for sensing.

A 4-valued FCAM can be extended to an 8-valued FCAM by substituting the 2-bit FRAM cell in Figure 8 or 9 with a 3-bit FRAM cell and modifying the peripheral circuitry accordingly. Since the size of the additional FE capacitor must be four times the size of the minimum-size FE capacitor, the challenge in this extension will be that of optimizing the BL capacitance for a reliable sensing of three

Table 1: An approximate evaluation of the relative advantage of each CAM type

CAM	Type	Non-volatile	Real-time Programm-ability	Bit-density	Speed/bit	Sense Amp. Simplicity
Dynamic [3]	Binary	No	Yes	+	+	+++
2T-1C [1]	Multiple-valued	No	No	++	+	++
Comp. 2T-1F [this work]	Binary	Yes	Yes	+	+	++
2T-1F [this work]	Binary	Yes	Yes	+	+	++
Sequential-access [this work]	Multiple-valued	Yes	Yes	+	+	++
Parallel-access [this work]	Multiple-valued	Yes	Yes	+	++	+

FE capacitors with a 1:2:4 ratio.

Recall that the size of an FE memory cell is constrained by the access transistor area, not the FE capacitor area. Therefore, an improvement in the density of the sequential-access multiple-valued FCAM is achievable by eliminating one of the access transistors in the 2-bit FRAM cell, that is, by sharing one access transistor for the two FE capacitors. Depending on the actual ratio of the FE capacitor to the access transistor area, eliminating an access transistor from a 4-valued cell can be equivalent to halving the cell-array area. This requires more accurate timing and design margining to avoid possible cross-talk between the two FE capacitors of a cell, or among the unaccessed FE capacitors of different cells sharing the same plate-line.

An improvement in the access time can be achieved by incorporating a non-driven cell plate-line write/read scheme [8] in the FRAM cell.

5. References

[1] T. Hanyu, S. Aragaki, and T. Higuchi, "Functionally separated, multiple-valued content-addressable memory and its applications", *IEE Proc.-Circuits Devices Syst.*, Vol. 142, No. 3, pp. 165-172, June 1995.

[2] A. Sheikholeslami and P. G. Gulak, "Transient modeling of ferroelectric capacitors for semiconductor memories", *Microelectronic Engineering*, Vol. 29, pp. 141-144, 1995.

[3] J. P. Wade and C. G. Sodini, "A ternary content search engine", *IEEE Trans. on Comput.*, Vol. C-35, No. 5, pp. 456-461, May 1989.

[4] M. Hariyama and M. Kameyama, "A collision detection processor for intelligent vehicles", *IEICE Trans. Electron.*, Vol. E76-C, No. 12, pp. 1804-1811, Dec. 1993.

[5] K. J. Schultz and P. G. Gulak, "Architectures for large-capacity CAMs", *INTEGRATION*, the VLSI journal, Vol. 18, No. 2 & 3, pp. 151-171, June 1995.

[6] S. W. Wood, "Ferroelectric Memory Design", *M.A.Sc. thesis*, University of Toronto, 1992.

[7] T. S. Jung, et al., "A 3.3V 128Mb Multi-Level NAND Flash Memory for Mass Storage Applications", *ISSCC Dig. Tech Papers*, pp. 32-33, 1996.

[8] H. Koike, et al., "A 60-ns 1-Mb nonvolatile ferroelectric memory with non-driven cell plate line write/read Scheme", *ISSCC Dig. Tech Papers*, pp. 368-369, 1996.