14.1 Negative-Resistance Read and Write Schemes for STT-MRAM in 0.13µm CMOS

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Spin-torque-transfer (STT) magnetoresistive random-access memory (MRAM) [1-3], a successor to field-induced magnetic switching MRAM [4,5], is an emerging non-volatile memory technology that is CMOS-compatible, scalable, and allows for high-speed access. However, two circuit-level challenges remain for STT-MRAM: potentially destructive read access due to device variation and a high-power write access. This paper presents two STT-MRAM access schemes: a negative-resistance read scheme (NRRS) that guarantees non-destructive read by design, and a negative-resistance write scheme (NRWS) that, on average, reduces the write power consumption by 10.5%. A fabricated and measured test-chip in 0.13µm CMOS confirms both properties.

A simplified block-diagram of the STT-MRAM is shown in Fig. 14.1.1. The memory consists of storage cells and reference cells. A negative-resistance read/write scheme is used to access the storage cells. Two reference cells (per row) provide an on-chip reference for the read scheme. Due to area and I/O constraints, we access the 16kb array serially through shift registers. The cell, shown in the top inset, consists of a magnetic tunnel junction (MTJ) in series with an access transistor: 1T1MTJ topology [1,2]. The bottom inset shows a cross-section of the MTJ: an oxide barrier (MgO) between a fixed and a free magnetic layer (CoFeB) [3]. Depending on the magnetic orientation of the free layer with respect to the fixed layer, the MTJ (R_{MTJ}) can be in one of two states, a parallel (P) low-resistance (R_P) or an anti-parallel (AP) high-resistance (R_{AP}) state, which encode the stored data bit.

To read from a cell, the conventional scheme [1,2,4], shown in Fig. 14.1.2, supplies a constant current (I_{READ}) to the MTJ and detects the value of R_{MTJ} (R_P or R_{AP}) by monitoring the voltage across it (V_{MTJ}). A cell can also be read using a constant voltage source, in which case I_{MTJ} is measured. I_{READ} is chosen to maximize the sense voltage, which comes at the cost of reducing the non-destructive read margin due to I_{READ} approaching the MTJ switching current, I_{C-}, indicated in the current-based R_{MTJ} hysteresis loop. Due to device variation, I_{C-} might deviate from its nominal value to be smaller than I_{REF} in magnitude, which would cause destructive reads. To avoid this trade-off between the sense voltage and the read margin, and to guarantee a non-destructive read, we shunt the MTJ with a negative resistance (–R) that dynamically allocates current to the MTJ depending on its state (bottom of Fig. 14.1.2). We choose –R such that $-R||R_{AP}$ is negative, while $-R||R_P$ is positive. A negative net resistance in parallel with the sense-line (SL) capacitance, C_{SL}, makes an unstable system, while a positive net resistance makes a stable system. A small initial voltage, V_{init}, causes V_{MTJ} to exponentially grow to V_{DD} in the unstable system, and decay to ground in the stable system, thus sensing the MTJ state and reading the stored bit. To illustrate the non-destructive nature of NRRS, we annotate the developing V_{MTJ} with successive dots on the voltage-based R_{MTJ} hysteresis loop. We choose the orientation of the MTJ such that in the unstable system (shaded dots) V_{MTJ} moves to the left along the hysteresis loop, while in the stable system (clear dots) V_{MTJ} moves to the right. Since V_{init} can be arbitrarily small, we set it well below V_{C-}, ensuring a non-destructive read regardless of device variation.

Figure 14.1.3 presents the circuit implementation of the NRRS. To read from the storage cell, we first connect the BL to GND and then enable the WL, which connects the cell to the –R read circuit. A sense amplifier monitors the voltage developing on the sense node, S, and compares it against an inverter threshold, V_{TH}, to output the read result. The –R circuit [6] generates a current proportional to the voltage at S with a transconductor M_G, and then reflects this current back into S with a current mirror M_{P1}-M_{P2}, thus appearing as a negative resistance at node S. We bias the –R circuit such that it forms a meta-stable system when connected to $R_P||R_{AP}$, which is the equilibrium point between a stable R_P and an unstable R_{AP} case. We add a bias current to the current mirror using M_B, which is controlled by a replica bias scheme. This bias scheme consists of two reference cells per row, a scaled –R/2 replica circuit and an amplifier in negative feedback. The two reference cells in parallel, one in P and one in AP state ($R_P||R_{AP}$), connect to a –R/2 replica circuit, which is two –R's in parallel. The amplifier forces the voltage at the reference sense node, S_{REF}, to V_{TH} by driving the gate of M_{BREF} in the negative feedback loop, as well as the gate of M_B. As a result of this biasing, the SA effectively compares the voltage at S with the voltage at S_{REF}, which corresponds to comparing R_{MTJ} in the storage cell with the reference resistance $R_P||R_{AP}$, maximizing the sense margin. Transistor M_C is used in a cascode configuration to increase the R_P to R_{AP} difference seen by the read circuit.

To write into a cell, the conventional scheme applies a current to the cell that is larger than the critical switching current. The negative resistance saves power during write by moderating the current though the MTJ, I_{MTJ}, as its resistance drops from high R_{AP} to low R_P, i.e. writing a '0'. In contrast to the read scheme, the write scheme uses the reversed orientation of the MTJ with respect to the –R circuit, as we show in Fig. 14.1.4. While writing a '0', the –R driver reflects current into BL that is proportional to R_{MTJ}. Once the write is complete, and R_{MTJ} reaches the low R_P value, the driver reduces the reflected current thus saving power. We show this using the current-based R_{MTJ} hysteresis loop. If a cell stores a '1' (shaded circles), the driver exponentially increases I_{MTJ} as in an unstable system, until I_{MTJ} reaches I_{C+} and the MTJ switches its state. Then, I_{MTJ} exponentially decays as in a stable system, saving power. If a cell stores a '0' (clear circles), I_{MTJ} decays right away. An externally controllable V_B allows us to trade-off write-0 access time against amount of current saved. To write a '1', we use a conventional push-pull topology, since the R_{MTJ} increases to a high R_{AP} value, which naturally moderates I_{MTJ}.

In Fig. 14.1.5 we present the measured read access time (t_R) of the NRRS. The simplified schematic of the measurement setup consists of the storage cell, the NRRS, a static buffer, and a shift-register flip-flop. We define t_R as the time from the onset of column select (CS) to the onset of the shift-register clock (CLK). We varied t_R from 1 to 15ns, and measured the yield of successful reads for all cells in the array. The read-access-time yield plot shown in Fig. 14.1.5 indicates that for $t_R \geq 8$ns, the yield levels off, which confirms that the NRRS has a minimum t_R of 8ns. Read time yield varies below 8ns, as the feedback loop around the reference negative resistance requires a finite nonzero time to stabilize to a final value.

Figure 14.1.6 compares the measured write power consumption and write access time of the NRWS and conventional schemes. The bar graph compares the power of NRWS and conventional write scheme for four write patterns. A repeating 0 pattern results in the highest savings of 58.5%, while typical data pattern results in a 10.5% saving. We measured the write access time by measuring its yield, similar to the read access time. The measured minimum access time, shown in Fig. 14.1.6, is 9ns for write-0 and 10ns for write-1 cases. Our measurements indicate that, compared to the conventional scheme, NRWS saves write power without compromising the write access time.

We implemented the test-chip, shown in Fig. 14.1.7, in Fujitsu's 1-poly 8-metal 0.13µm CMOS process with MTJ layers present between metals 7 and 8, as illustrated in the TEM images. We implemented the proposed and conventional schemes in the same test-chip in a 16kb array. The table in Fig. 14.1.7 compares our test-chip's performance with the most recent STT-MRAM implementation [1].

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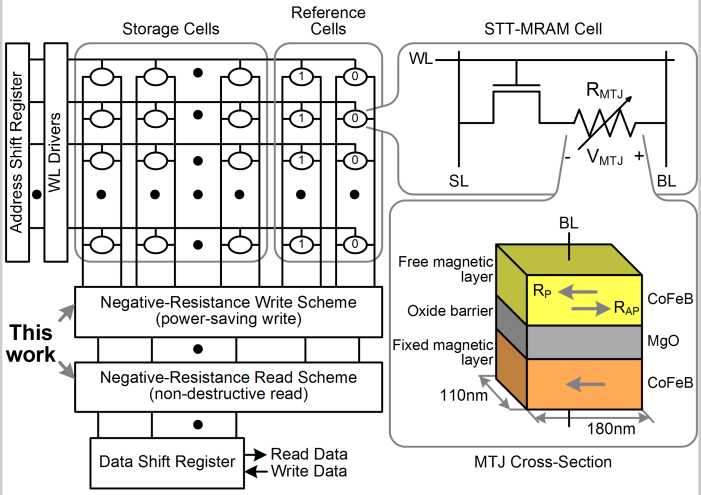
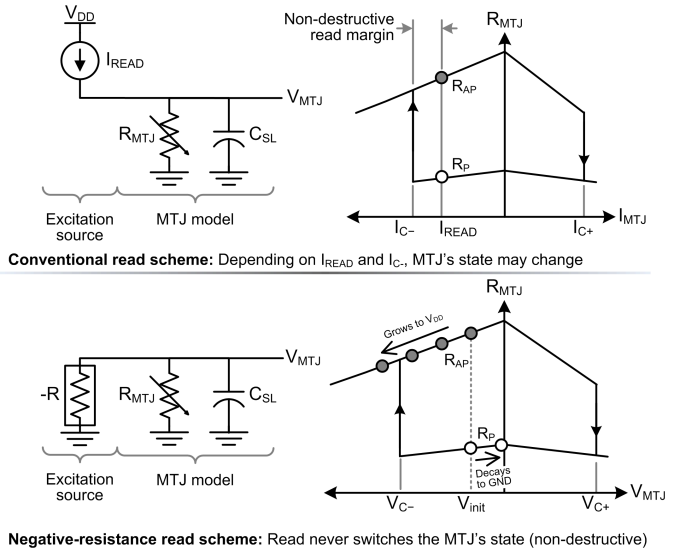


Figure 14.1.1: Simplified block diagram of STT-MRAM array.



Conventional read scheme: Depending on I_{READ} and I_{C-}, MTJ's state may change

Negative-resistance read scheme: Read never switches the MTJ's state (non-destructive)

Figure 14.1.2: Conventional and negative-resistance read schemes.

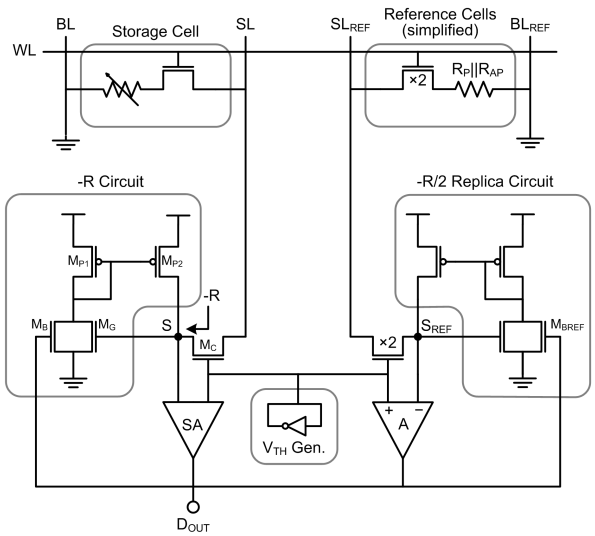


Figure 14.1.3: Negative-resistance read scheme (NRRS) implementation.

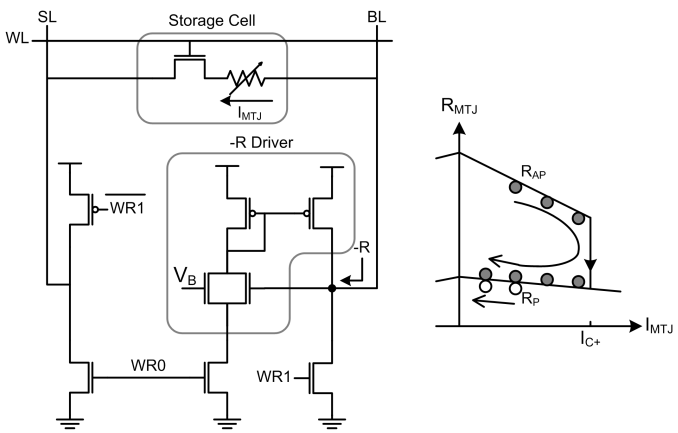


Figure 14.1.4: Negative-resistance write scheme (NRWS) implementation.

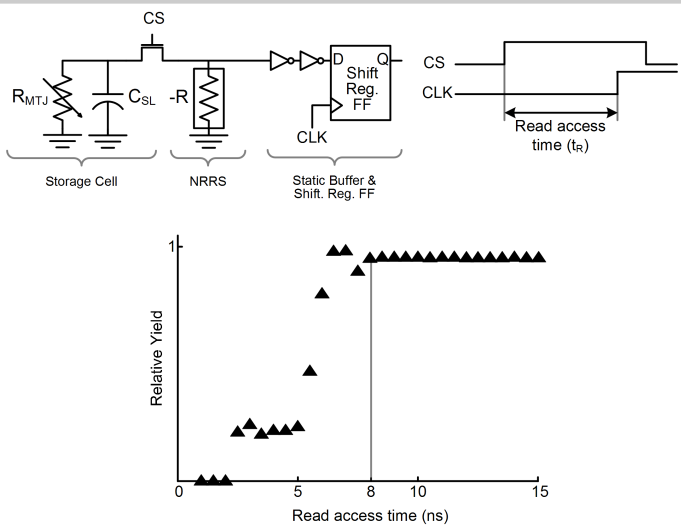


Figure 14.1.5: Measurement setup and measured NRRS read access time.

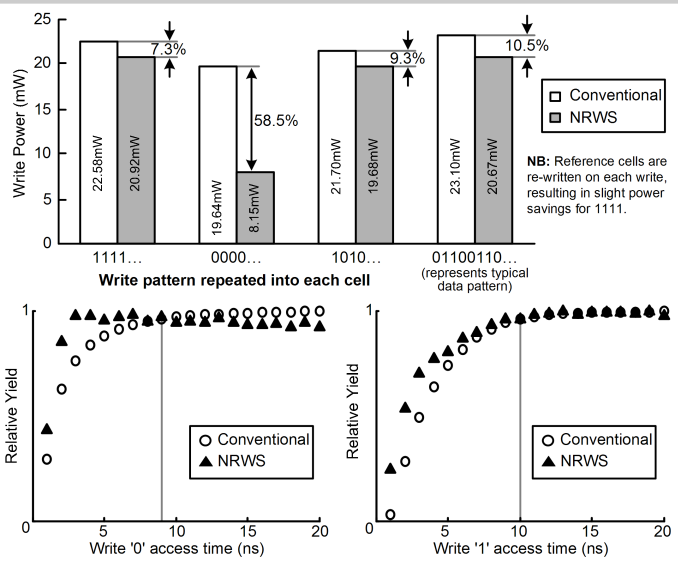
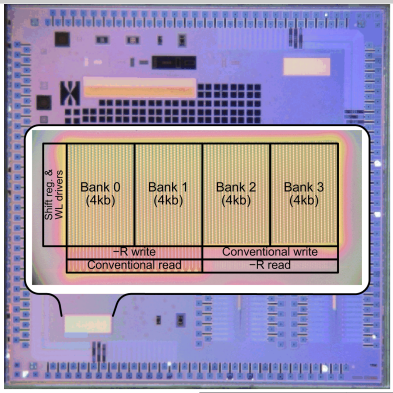
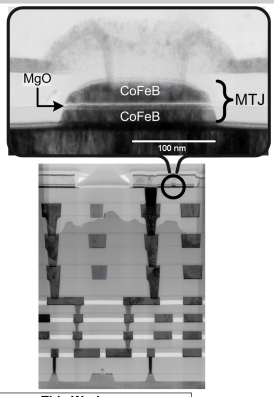


Figure 14.1.6: Measured write power consumption and access time.





		ISSCC 2007 [1]	This Work
Process		0.2µm CMOS (1P, 4M)	0.13µm CMOS (1P, 8M)
Read time		40ns	**8ns**
Write	time	100ns	**9/10ns**
	current	0.2mA	0.40 / 0.87mA
Capacity		2Mb	16kb
Memory Cell Sizes		1.6 x 1.6µm^2	3.25 x 1.7µm^2
Power Supply		1.8V	1.2V:read and logic/3.3V:memory core

Figure 14.1.7: Die photograph, TEM cross section, and comparison to previous work.

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