6.7 A 28Gb/s Digital CDR with Adaptive Loop Gain for Optimum Jitter Tolerance

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As we move to higher data rates, the performance of clock and data recovery (CDR) circuits becomes increasingly important in maintaining low bit error rates (BER) in wireline links. Digital CDRs are popular in part for their robustness, but their use of bang-bang phase detectors (BB-PD) makes their performance sensitive to changes in jitter caused by PVT variations, crosstalk or power supply noise. This is because the gain of a BB-PD depends on the CDR input jitter, causing the loop gain of the CDR to change if the jitter magnitude or spectrum varies. This problem is illustrated in Fig. 6.7.1 where small jitter leads to excessive loop gain and hence to an underdamped behaviour in the CDR jitter tolerance (JTOL), while large jitter leads to insufficient loop gain and hence to low overall JTOL. To prevent this, we propose a CDR with an adaptive loop gain, K_G, as shown in Fig. 6.7.1.

To control the loop gain, prior works adapt the CDR loop filter (LF) based on the jitter bandwidth, as estimated by filtering [1] or detecting patterns in the PD output [2,3]. Both approaches assume that the best-case jitter spectrum is known a priori, which is not always true. In contrast, in this work, we increase K_G and therefore the CDR loop bandwidth to suppress the most jitter and minimize BER while preventing the CDR from becoming underdamped. We ensure this by monitoring the autocorrelation function *(R(n))* of the PD output as we explain next.

Figure 6.7.2 shows the proposed adaptation concept. We increase K_G while monitoring the autocorrelation function of the lowpass-filtered PD output to determine when K_G reaches the desired value. If K_G is increased too much, ringing occurs in *R(n)*, causing *R(n)* to dip at a particular value of n we call n_{peak}. This is consistent with the peaking observed in the spectrum of the jitter between data and clock as shown in the same figure. Since any ringing causes $R(n_{peak})$ to fall below zero, the proposed CDR increases K_G if $R(n_{peak})>0$ and decreases it otherwise. This maximizes the bandwidth while avoiding underdamped behaviour. The lowpass filter (LPF) suppresses white or broadband random jitter such as jitter caused by intersymbol interference (ISI), providing better observability of CDR behaviour. Without the LPF, *R(n)* could be dominated by a delta-function (the autocorrelation function of white noise), obscuring ringing caused by an underdamped CDR.

The task remains of finding n_{peak}, which corresponds to half of the CDR oscillation period if it is highly underdamped. We determine n_{peak} adaptively by initially setting K_G to its highest value and observing the period of the CDR's damped oscillation. Using the fact that $R(n_{peak}/2)\approx 0$, the feedback loop shown in Fig. 6.7.3 is able to find n_{peak}. The result is stored as $n_{peak,REF}$, and used for the rest of adaptation.

Recent works also use *R(n)* to adapt PLLs [4,5] and CDRs [6] but by not filtering the PD output, lose observability of CDR behaviour if broadband (e.g. ISI) jitter is present. These works derive conditions on *R(n)* which minimize jitter. If however, parameters such as the CDR latency or input jitter profile differ from what was assumed in the derivations, or sinusoidal jitter (SJ) is added, the results no longer apply. In contrast, this work adapts n_{peak} based on measurements and does not rely on any simulated or calculated parameters. It also does not assume a particular jitter profile and can therefore be applied to a variety of CDR topologies and jitter profiles, including SJ, as we discuss later.

The proposed adaptation, shown in Fig. 6.7.3, is implemented in a half-rate 28Gb/s phase interpolator (PI)-based CDR and fabricated in 28nm CMOS. The analog frontend includes a continuous time linear equalizer (CTLE) with active feedback and an inverter-based second stage driving six half-rate samplers including an eye-monitor used for diagnostics. An injection-locked oscillator (ILO) locked to an external reference clock generates quadrature clocks for the 7b CMOS inverter-based PIs. The demuxed data is sent to PD logic in the digital core.

After majority voting (MV), which comprises a moving average followed by a slicer, the PD outputs are scaled by K_G before entering the LF. Since the inputs to the adaptation block and LF are binary, the implementations of these blocks are greatly simplified. The wide bandwidth of the first MV stage preserves any ringing that needs to be observed to adapt n_{peak}. The *R(n)* measurement block input is then further filtered by an MV stage with a programmable bandwidth.

The top two plots of Fig. 6.7.4 show the measured adaptation of n_{peak} and corresponding *R(n)* curve, while K_G is at its highest setting. The results confirm that the adapted n_{peak} value closely matches the minimum location of *R(n)*. The bottom plots show the measured adaptation of K_G (after n_{peak} had already been determined). After adaptation, the JTOL of the CDR is superior compared to when K_G is too high or too low and as discussed next, high-frequency jitter tolerance is optimized.

Figure 6.7.5 shows the test setup used to assess the performance of the algorithm. Given the CDR loop bandwidth of approximately 10MHz, we plot the lowest out-of-band JTOL measured from 10MHz to 100MHz (for BER<10^{-12} and PRBS31 data), as a function of K_G. The results in Fig. 6.7.5 show that K_G adapts to within one code of the highest JTOL for two test cases. In Case 1, the reference clock has a 100ppm frequency offset and is phase-modulated to give a phase noise characteristic like that of a PLL. In Case 2, the clock has a 50ppm frequency offset and is FM-modulated to mimic the phase noise of a free-running oscillator. Figure 6.7.5 also shows the reference clock phase noise measured in each case. In these measurements, K_G is adapted prior to applying SJ and held at the adapted value $(K_{G,REF})$ during JTOL tests. Having obtained values for $K_{G,REF}$ and $n_{peak,REF}$, additional logic can also be enabled allowing K_G to adapt dynamically to better suppress any SJ seen by the CDR. We explain this next.

If SJ becomes dominant, ringing will be detected in *R(n)* even if the CDR remains well-damped. If ringing is detected, the additional adaptation logic continuously monitors the output of the n_{peak} adaptation block to estimate the SJ period by measuring the period of the ringing. By comparing n_{peak} to $n_{peak,REF}$, the logic decides if the detected SJ is within the tracking bandwidth of the CDR. If it is, K_G increases to better suppress the jitter. If the jitter is out-of-band or no peaking is detected at all, K_G reduces back to $K_{G,REF}$ obtained previously.

To demonstrate the effectiveness of this feature, Fig. 6.7.6 plots the highest SJ amplitude for which the CDR can maintain BER<10^{-12}, measured for the two test cases described earlier. The results of fixed adaptation (where K_G stays at $K_{G,REF}$ after adaptation) are compared to the dynamic case where K_G continuously adapts to the input jitter. Both results are compared to the best possible result, where K_G is manually tuned at each frequency. While fixed adaptation optimizes the ability of the CDR to tolerate high frequency SJ, enabling dynamic operation further improves tracking of in-band jitter, nearly matching the performance achieved if K_G is manually tuned. The entire CDR consumes 106.6mW, of which the eye-monitor consumes about 12%. Figure 6.7.7 shows the die photo, area and power breakdown of the design.

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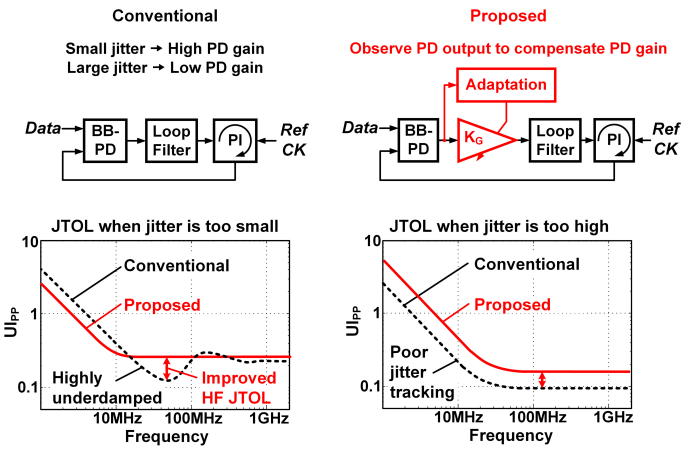


Figure 6.7.1: Conventional bang-bang CDR and proposed adaptive loop gain CDR showing the impact of adaptation on jitter tolerance.

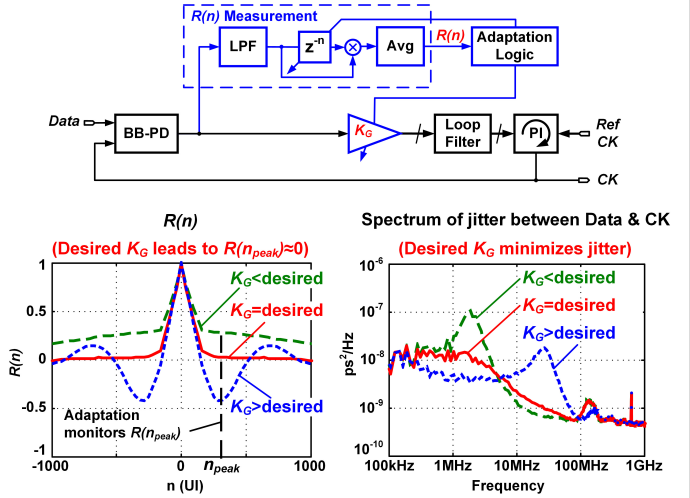


Figure 6.7.2: Basic concept of the proposed adaptation showing the relationship between *R(n)* and the spectrum of the jitter as K_G is varied. Jitter is minimized when $R(n_{peak})$ is approximately zero.

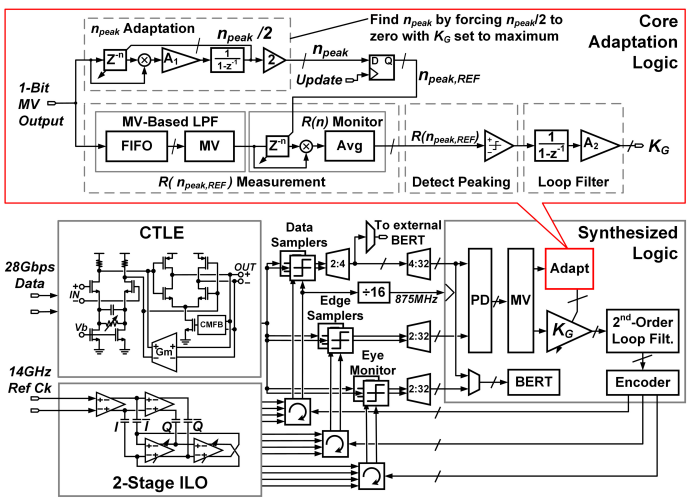


Figure 6.7.3: Block diagram of proposed adaptive loop gain CDR showing core adaptation logic.

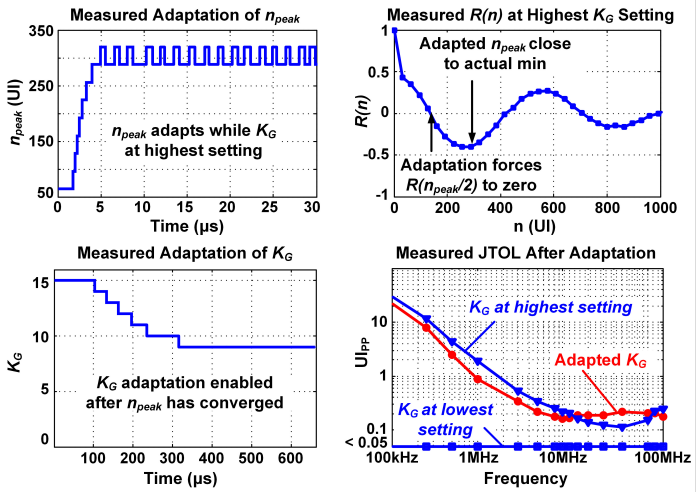


Figure 6.7.4: Measured adaptation curves for n_{peak} and K_G; measured *R(n)* at maximum K_G and measured jitter tolerance (for PRBS31 and BER<10^{-12}) following adaptation.

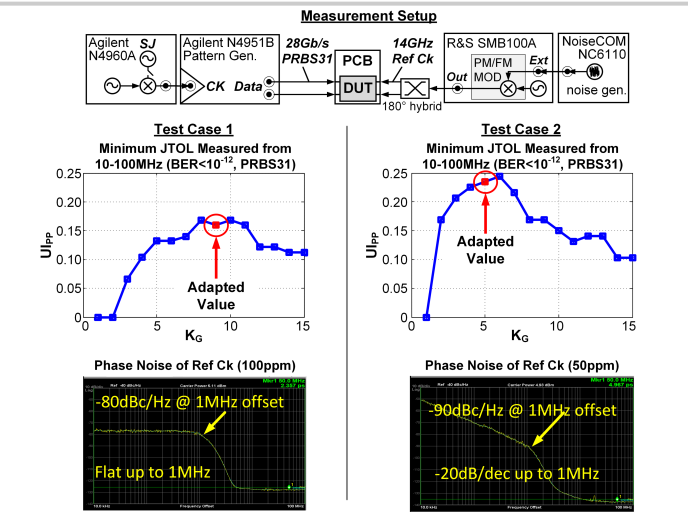


Figure 6.7.5: Measurement setup and results for minimum high-frequency jitter tolerance (between 10-100MHz) vs. CDR loop gain (K_G) and phase noise of Ref Ck for two test cases.

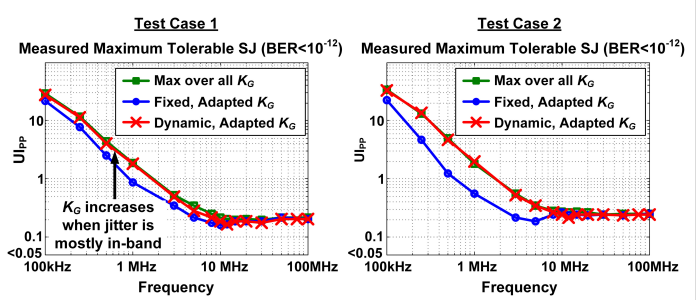
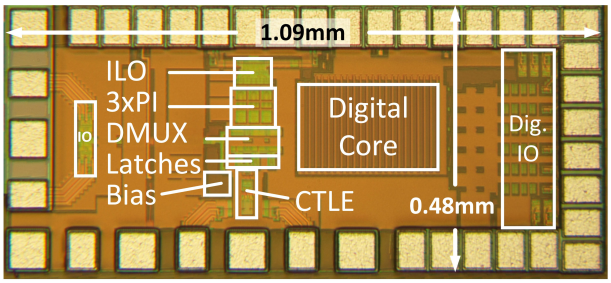
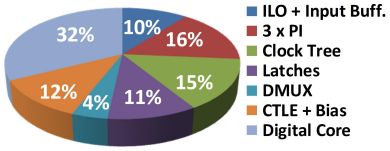


Figure 6.7.6: Maximum SJ the CDR can tolerate, comparing max over all K_G settings to fixed adaptation (K_G is fixed after adapting) and dynamic adaptation (K_G dynamically adapts to input jitter). Test cases are the same as those in Fig. 6.7.5.



Power Breakdown†



Total Measured Analog Power : 72mW
Total Measured Digital Power : 34.6mW
†*Breakdown estimated based on simulation*

Area Breakdown

Block	Area (µm x µm)
ILO + Input Buff.	84 x 50
3 x PI	80 x 80
DMUX	110 x 52
Latches	84 x 25
CTLE	64 x 80
Bias	45 x 50
Digital Core	274 x 175

Figure 6.7.7: Die photo with power and area breakdowns.

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