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Negative Resistance

Welcome to "Circuit Intuitions!" This is the third article in a series in this magazine. As the title suggests, each article provides insights and intuitions into circuit design and analysis. These articles are aimed at undergraduate students but may serve the interests of other readers as well. I would appreciate your comments and feedback, as well as your requests and suggestions for future articles in this series. Please e-mail me at ali@ece.utoronto.ca.

The past two articles in this series introduced a number of small circuit blocks or "library elements" to analyze larger circuits. We use these library elements in this article to analyze the implementation of *negative resistance*. But let us first define what a negative resistance is and why it is useful.

In a one-port circuit, as shown in Figure 1, an increase in the port voltage typically results in an increase in the port current. Equivalently, we can say a positive small-signal voltage results in a positive small-signal current. Since the ratio of the small-signal voltage to the small-signal current is defined as the small-signal resistance, this resistance is positive for the case mentioned. However, there are circuits that exhibit negative resistance, also represented in Figure 1, where applying a positive small-signal voltage results in a negative small-signal current. Assuming we can build such a circuit and connect it either in series or in parallel with a positive resistor of the same magnitude, we can essentially create a circuit element with zero loss (power dissipation) for the signal. In the case of series combination, we will end up with zero resistance (short circuit), and, in the case of parallel combination, we will end up with infinite resistance (open circuit), with both consuming zero signal power. Since the positive resistance consumes signal power, the negative resistance must produce signal power to compensate. As we will see later, however, we need to burn dc power for this to happen.

What would be the use of this negative resistance? We provide two examples.

- In a typical RC circuit, shown in Figure 2, an initial voltage on the capacitor will *decay* exponentially to zero over time. If R is negative, however, the initial voltage will *grow* exponentially until it is limited by other components in the circuit. This is indeed how we design regenerative amplifiers, latches, and flip-flops.
- Consider building an LC oscillator by a parallel combination of an inductor (L) and a capacitor (C), referred to as an LC tank [see Figure 3(a)]. If the L and the C are ideal (i.e., lossless), then the total energy stored in the L (in the form of $LI^2/2$) and the C (in the form of $CV^2/2$) will remain constant over time. The stored energy swings back and forth between the capacitor and the inductor but is never lost simply because there is no loss mechanism (resistive element) in the tank. In reality, however, one cannot find a lossless inductor or a

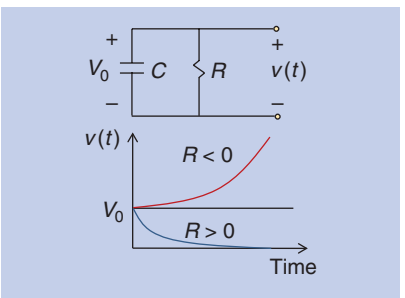

FIGURE 2: The voltage across a capacitor decays to zero for a positive resistance but grows exponentially for a negative resistance.

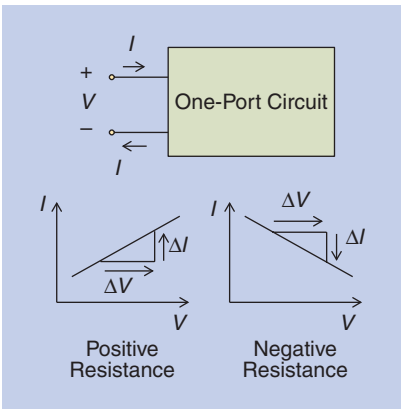

FIGURE 1: A one-port circuit has a positive (negative) resistance when an increment in the port voltage results in an increment (decrement) in the port current.

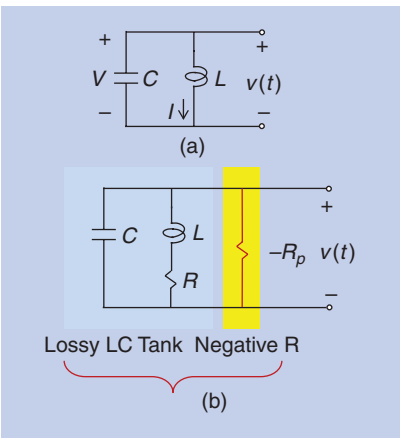

FIGURE 3: A negative resistance (–Rp) in parallel with a lossy LC tank effectively creates a lossless LC tank.

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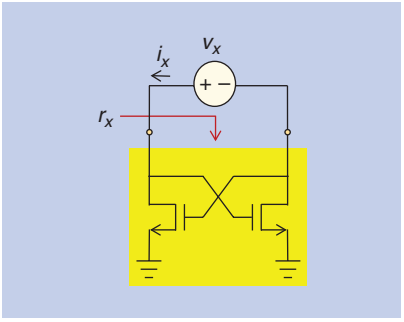

FIGURE 4: A cross-couple NMOS pair exhibits a small-signal negative resistance. r_x is found in Figure 5.

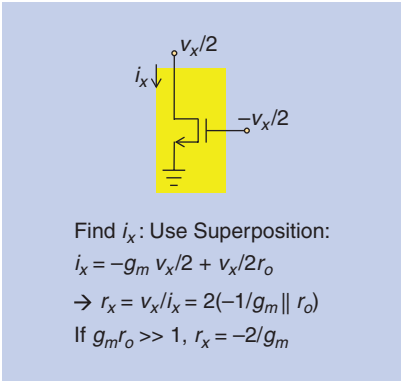

FIGURE 5: The half circuit for derivation of negative resistance in Figure 4.

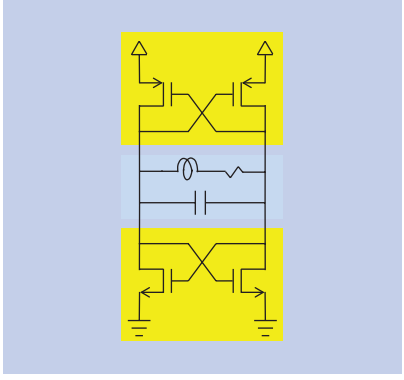

FIGURE 6: A negative-resistance LC oscillator consists of a lossy LC tank in parallel with two negative resistances.

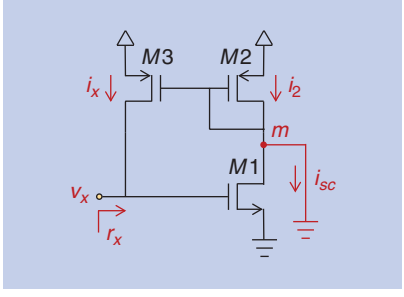

FIGURE 7: The input voltage is converted to current, then mirrored back to the input to create a negative resistance.

lossless capacitor. Figure 3(b) shows a lossy inductor with a series resistance in the tank.

This series resistance consumes the initial energy stored in the tank until it diminishes to zero. If an LC oscillator is to sustain its oscillation indefinitely, then we must compensate for the energy lost in the series resistor. This can be done with the inclusion of a negative resistance in parallel with the LC tank, as shown in Figure 3. We now look at two simple implementations of negative resistance.

Figure 4 shows a simple implementation of a negative resistance that consists of two cross-coupled NMOS transistors (biasing not shown). To understand how this circuit exhibits a negative resistance, let us apply a small-signal voltage source v_x to this circuit as shown. Since the circuit is fully symmetric, it can be broken into two half circuits, like the one shown in Figure 5. One can easily verify that the resistance of the half circuit is $-1/g_m \| r_o$, and hence the resistance of the full circuit is $2(-1/g_m \| r_o)$. Since $g_m r_o > 1$, the resulting resistance is always negative. If we assume $g_m r_o >> 1$, the equivalent resistance becomes $-2/g_m$.

This circuit is at the heart of what is known as a *negative-resistance LC oscillator*, shown in Figure 6. The two cross-coupled pairs (PMOS and NMOS) produce two negative resistances that are placed in parallel with the lossy LC tank in the middle, effectively producing a lossless LC tank. In addition, the two pairs provide dc bias currents for each other. The bias currents, drawn from the dc power supply, provide the signal power produced by the two negative resistances. Interested readers are referred to [1] for a more detailed discussion on this design.

It is interesting to see what happens to the negative resistance shown in Figure 4 if we add a source-degeneration resistor in series with the cross-coupled NMOS transistors. The reader is encouraged to discover this on his/her own after reviewing the equivalent circuit for a source-degenerated NMOS transistor discussed in the previous article in this series.

The circuit shown in Figure 4 is only one way to produce negative resistance. Another approach is shown in Figure 7 (biasing not shown). Here the input voltage is first converted into a current using an NMOS transistor (M1), and the resulting current is mirrored (by M2 and M3) to provide a small-signal current back to the input. To estimate the resulting negative resistance in this configuration, observe that the short-circuit current at m node is $g_{m1} v_x$. This current is then divided between the resistance looking up (at the drain of M2) and down (at the drain of M1). Using the library elements introduced in the Spring 2014 column, we can write the following expression for the current being mirrored:

$$i_2 = g_{m1} v_x \frac{g_{m2} + 1/r_{o2}}{g_{m2} + 1/r_o},$$

where r_o refers to $r_{o1} \| r_{o2}$. Since this current is mirrored to the left side, the resulting negative resistance will be

$$r_x = \left(\frac{-1}{g_{m1}} \frac{g_{m2} + 1/r_o}{g_{m2} + 1/r_{o2}}\right) \| r_{o3}.$$

Since the first term in the parallel combination is usually much smaller than the second term (r_{o3}), one can see that the magnitude of r_x is only slightly larger than $1/g_{m1}$.

To conclude, a negative resistance is used in regenerative amplifiers, latches, and LC oscillators. A negative resistance can be implemented simply as a pair of cross-coupled NMOS or PMOS transistors, or it can be implemented using a transconductance and a current mirror.

References

[1] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2004, pp. 641–645.

For Thevenin and Norton equivalent circuits, refer to R. E. Thomas et al., *The Analysis and Design of Linear Circuits*, 7th ed. New York: Wiley, 2012, pp. 109–122.

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