An Adaptive Reference Generation Scheme for 1T1C FeRAMs

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Abstract
A reference time, instead of a reference voltage, is generated used to compare stored "0" and "1" in a race of bitlines towards reaching a threshold voltage in a 1T1C FeRAM. The reference time is adaptive, tracking process variations, aging, and fatigue of ferroelectric capacitors. This scheme is implemented in a 256x128-bit testchip in a 0.35 μm ferroelectric process and achieves a 40ns access time at 3V.

Introduction
FeRAMs can be implemented using a one-transistor one-capacitor (1T1C) cell structure to improve density, however, a reference scheme is required for reading [1]. A constant reference voltage such as one reported in [2] does not track fatigue and aging properties of ferroelectric capacitors, rendering the scheme inefficient for frequent read/write applications. In contrast, an adaptive reference scheme proposed in this paper tracks fatigue, aging, and process variations, such that equal sensing margins are maintained over time and across chip for stored "0" and "1".

A conventional read scheme detects the stored data by comparing the bitline voltage to a reference voltage (V_{ref}) using a sense amplifier (SA), as shown in Figure 1a. Our proposed scheme, shown in Figure 1b, detects the stored data by comparing the time of the rising edge of the sense amplifier output to the time of the rising edge of the reference signal (SA_{ref}). An SA output reading a "0" (SA_0) rises at time T_0, while an SA output reading a "1" (SA_1) rises at time T_1. The comparison occurs by latching the SA outputs at reference time (T_{ref}), halfway between T_0 and T_1. This time-domain scheme lends itself easily to adaptive implementation as we will see next.

Adaptive Reference Generation
Figure 2 shows the block diagram of the proposed scheme. During read, the plateline (PL) is held low while the bitlines (BL) are charged up using constant current sources (CS). The BLs connected to stored "0" are charged up faster compared to the bitlines connected to stored "1", due to smaller capacitance of the ferroelectric capacitor (C_{FE}) in state "0" [3]. A BL with stored "0" reaches the SA threshold voltage (SA_{th}) at T_0 causing SA_0 to rise, while a BL with stored "1" reaches the same threshold at T_1 causing SA_1 to rise. As a result, SA_0 rises prior to SA_1. These two signals are used to adaptively generate SA_{ref} with a rising edge at $T_{ref} = (T_1 + T_0)/2$ to maximize the sensing margins (Figure 1b). SA_{ref} is then used as a control signal to latch the SA outputs at T_{ref}. The last bit, n, of each row is stored differentially [4] to ensure the reference generator has both SA_0 and SA_1 to produce SA_{ref}.

The circuit diagram of one column is shown in Figure 3. A differential amplifier compares the BL voltage to SA_{th}, producing the SA output signal. The latch stores the value of the SA output at T_{ref}. Once SA_{ref} occurs, the result of the read is available at Data node of the latch, and writeback can begin. Since Data node is isolated from the BLs, the data can be read before the BLs reach their final voltages, hence reducing access time compared to conventional scheme [2].

To guarantee $T_{ref} = (T_1 + T_0)/2$, two identical adjustable delay elements are connected in series and adaptively tuned by a delay comparator to match the time difference $T_1 - T_0$, as shown in Figure 4. As a result, a single delay element provides a rising edge midway between T_0 and T_1. The adjustable delay element, shown in Figure 5, delays SA_0 by attaching binary weighted capacitors to the control node, and buffers the result to all the latches. The binary weighted capacitors are controlled by the signals B0, B1, B2, which are generated by the delay comparator. The second adjustable delay element uses SA_{ref} as the input and uses the same control signals to produce $SA_{0\text{-}2\Delta}$. The delay comparator, shown in Figure 6, determines which rising edge occurs first ($SA_{0\text{-}2\Delta}$ or SA_1), accordingly sending an up/down signal to the counter to increase or decrease the delay control signals until $SA_{0\text{-}2\Delta}$ and SA_1 are matched.

Simulation Results
Figure 7 shows simulation results of one read cycle for the proposed scheme. PL is held low while the BL voltages rise by the activated CSC. The rise time difference is captured by the comparison of the BL voltage against SA_{th}, producing either SA_0 or SA_1. The results are latched by SA_{ref}. The total access time of this scheme is 40ns with only 15ns in actual sensing. The proposed scheme achieves a 20% reduction in access time compared to previous work [3]. Figure 8 shows the circuit adaptively reduces the delay of $SA_{0\text{-}2\Delta}$ until it is matched to SA_1. Extensive simulations for process variations and operating conditions verify the robustness of the proposed scheme. Further verification to be provided by test results.

Conclusion
An adaptive reference time is generated for a 256x128-bit 1T1C FeRAM testchip, with layout shown in Figure 9. Simulation results confirm the reference time tracks fatigue and process variations. The proposed scheme achieves an access time of 40 ns at 3 V supply. Measurement results will be presented during the symposium.

Acknowledgments
The authors thank Shoichiro Kawashima and Toru Endo of Fujitsu Labs, Japan, for their valuable comments, and Yadollah Eslami, Joyce Wong, and Igor Arsovski of the University of Toronto for their feedback and help on this work. Authors also thank Fujitsu Labs of Japan and NSERC of Canada for their generous funding.

References
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[3] Y. Eslami et al., "A differential-capacitance read scheme for FeRAMs," Symp. VLSI Circuits, pp. 298-301, June 2002
[4] T. Endo and S. Kawashima "Semiconductor Integrated Circuit Device" US Patent, Pub. No. US 2002/0060930, May 23, 2002

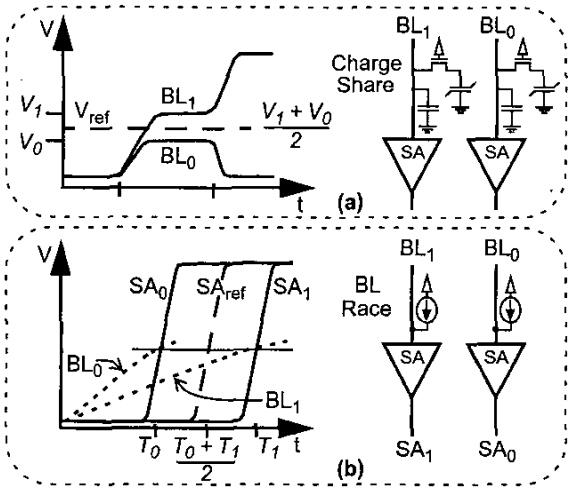

Figure 1: (a) Conventional read scheme using V_{ref}
(b) proposed scheme using T_{ref} halfway between T_0 and T_1

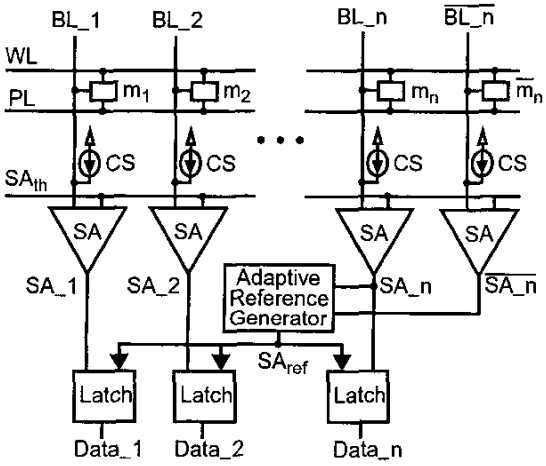

Figure 2: Block diagram of adaptive reference scheme

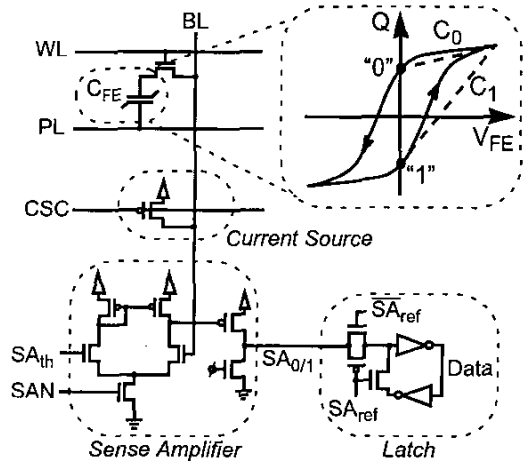

Figure 3: Column circuit - current source (CS) charges BL with constant current, sense amplifier (SA) compares V_{BL} to SA_{th} and latches data at T_{ref}

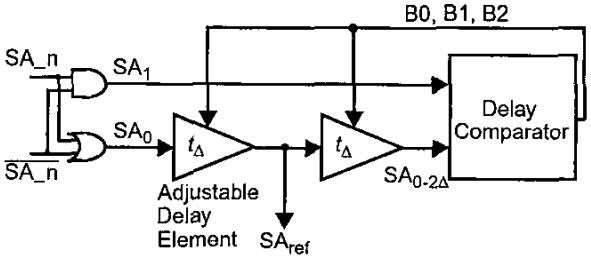

Figure 4: Adaptive Reference generator adaptively controls delay to ensure $T_0+T_{2\Delta}=T_1$ and hence $T_{ref}=(T_1+T_0)/2$

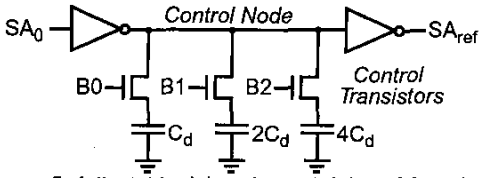

Figure 5: Adjustable delay element delays SA_0 using binary weighted capacitors to generate SA_{ref}

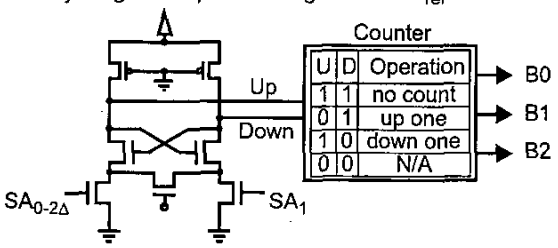

Figure 6: Delay comparator compares $SA_{0-2\Delta}$ against SA_1 to determine if $SA_{0-2\Delta}$ needs more/less delay to match SA_1

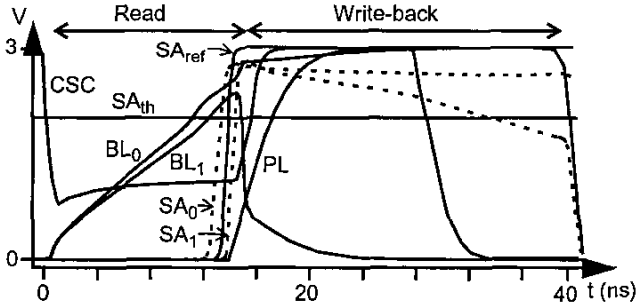

Figure 7: Read Simulation - stored data is detected by time difference between SA_0, SA_{ref} and SA_1

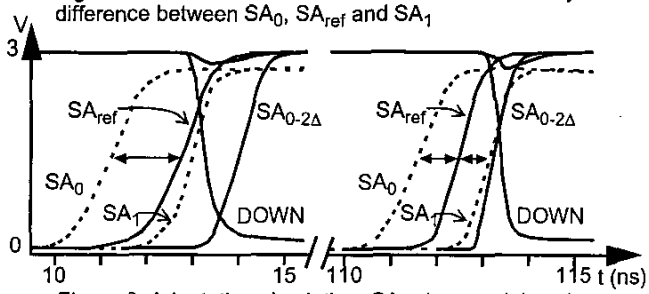

Figure 8: Adaptation simulation: SA_{ref} is over-delayed in first cycle, signalling DOWN to counter to bring SA_{ref} closer to midpoint in the following cycle

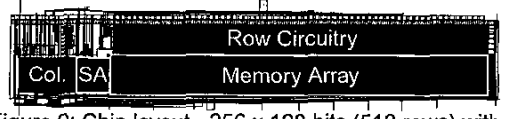

Figure 9: Chip layout - 256 x 128 bits (512 rows) with a read access time of 40 ns at 3 V