

CMOS Implementation of a Current Conveyor-Based Field-Programmable Analog Array

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Abstract

To date, all published CMOS field-programmable analog array (FPAA) designs have operated under 1MHz bandwidths. This paper develops circuit methods allowing the development of a CMOS FPAA operating at greater than 1MHz frequencies. For this purpose the second-generation current conveyor (CCII) is used. IC test results of a 0.8 μ m CMOS chip containing four configurable analog blocks based on the CCII, as well as an interconnection network based on transmission gates, are presented. The test results show that bandwidths exceed 10MHz. The four CABs and interconnect occupy a core area of 1551.8 \times 741.2 μ m².

1. Introduction

Recent trends in hardware design have seen a marked increase in the use of programmable devices such as PALs, CPLDs, FPGAs [1], and more recently field-programmable analog arrays (FPAA) [2]. Programmable devices reduce the time and cost of hardware prototyping.

Several commercial FPAA designs have now been released, operating in both the continuous-time and discrete-time domains [3]. Many university-based FPAA designs have also been proposed. Until now, FPAA designs, both continuous-time and discrete-time, have been operational amplifier-based and have operated at audio frequencies (100kHz bandwidths). Another frequency range where FPAA designs could find a niche is the video frequency range. The NTSC video frequency range extends to 4.5MHz, and cable television channels are allocated 6MHz slots. Thus an FPAA that operates up to 10MHz may be of use in certain video applications.

In order to increase bandwidths of CMOS FPAA designs to video frequencies, new architectures where the bandwidth is not limited by the frequency response of a simple operational amplifier, should be explored. Current conveyors [4] have shown promise as a replacement.

This paper deals with the design of CMOS FPAA designs operating in the video frequency range (10MHz). For

this purpose the second generation current conveyor is used in the FPAA design. Design and test of an architecture for an FPAA chip are shown in this work.

2. Current Conveyor Theory

A current conveyor [4] is a building block similar to an operational amplifier and which, when used in conjunction with other components such as resistors, capacitors and diodes, can implement several useful analog sub-systems such as amplifiers, integrators, and rectifiers.

The second generation current conveyor is a three terminal device. Its symbol is shown in figure 1.

The Y node is an infinite impedance node, with no current flowing into it; in practice the input impedance is finite and must be taken into consideration in the circuit design. When a voltage is applied at node Y, that voltage is replicated at node X. This is similar to the virtual short on an op-amp; however there is no need for negative feedback to achieve it. Also, when a current is injected into node X, that same current gets copied into node Z. The notation CCII+ denotes a positive Z output current conveyor. Continuous-time analog functions can be realized by hooking up other elements to the various terminals of the CCII.

The following subsections make an argument in favour of the current conveyor as an alternative to the simple op-amp.

2.1 Area Requirement

A standard simple op-amp uses 10 transistors, a compensation capacitor, and a bias stage. A common version of the current conveyor uses 12 transistors and a bias stage. These two are comparable in area requirements. An op-amp designed for higher frequency operation could use the same number of transistors, but would have a higher power consumption.

2.2 Compensation

An operational amplifier-based sub-system usually requires negative feedback. However, where the open-loop response A(s) of an uncompensated op-amp is

greater than unity in magnitude, and the phase shift nears 180°, there can be instability. For this reason, a compensation capacitor is used to reduce the unity-gain frequency of the op-amp to a point with larger phase margin, thus ensuring stable operation. This procedure results in an op-amp incapable of producing significant gains at high frequencies.

However, current conveyor-based building blocks do not use feedback. Stability is ensured since the gains in current and voltage from one node to another are unity. There is thus no need to compensate a current conveyor. A current conveyor-based design may thus be able to operate at higher frequencies than its op-amp-based counterpart, and still produce significant gains at a savings in silicon area.

2.3 Constant Bandwidth

Another advantage of using current conveyors rather than op-amps is that current conveyor-based amplifiers have a constant bandwidth, independent of gain. This is in contrast to op-amp-based amplifiers, which have a constant gain-bandwidth product.

2.4 Previous Work

Prémont et al [5] have proposed a current conveyor-based FPAA design. The Configurable Analog Block (CAB) contains two current conveyors arranged in a feedback loop. The feedback arrangement allows the implementation of gyrators, which realize a second-order filtering function.

The current conveyors are configured so as to be able to be switched off, electrically disconnecting their inputs and outputs. The architecture of the FPAA is to have locally interconnected CABs. A significant waste of silicon area can occur with the two current conveyor CAB since quite often only one of the two current conveyors is used and the other one must be turned off.

3. A Simple CCII-Based FPAA

The CAB is the principal functional block in an FPAA. Some desirable functions for a CAB include amplification, integration, and differentiation, multiplication, addition, subtraction, log, anti-log and comparison. Figure 2 shows a potential current conveyor-based implementation of a CAB capable of implementing first-order filtering functions as well as amplification; the log and anti-log functions could potentially be added by having switchable diodes on the X and Z nodes. The CAB includes a current conveyor, two transconductors, two programmable capacitors, and a buffer. The transconductors realize programmable resistors.

The response of the CAB is described by equation 1.

$$\frac{V_{out}}{V_{in}} = \frac{R_Z(1 + sR_X C_X)}{R_X(1 + sR_Z C_Z)} \quad (1)$$

By disconnecting C_X and C_Z , we obtain the response of an amplifier. Similarly, by disconnecting C_X and R_Z , we obtain the response of an integrator. As well, a lossy integrator function is obtained by disconnecting C_X .

In the prototype implementation, the current conveyor is based on the Oliaei-Loumeau CMOS design [6]. This implementation of the CCII (schematic shown in Figure 3) has been chosen for its low impedance on the X node, crucial in order to eventually implement a fast comparator. The variable resistors are implemented using CMOS double pair transconductors [7]; this transconductor is configurable as a grounded, programmable resistor. The variable capacitors are implemented using programmable capacitor arrays (PCA), which produce discrete capacitor values. The unity gain buffer is based on an operational amplifier in a unity-gain feedback configuration.

Transistors M10 to M13 instantiate current sources, biased by V_{n1} and V_{p1} . The source-to-source current mirrors M1/M2 and M3/M4 ensure that the voltage at node Y is replicated at node X; each current mirrors' gate-to-source voltages must be equal in order to get equal currents through both branches of the current mirrors (a condition forced by the current sources). The two class-AB output stages M6/M7 and M8/M9 ensure that equal currents flow out of the X and Z nodes; the currents flowing through M2 and M4 are equal. M2 and M4 instantiate grounded-gate amplifiers which lower voltage variations on the X node, resulting in lower X impedance.

The transconductor chosen for this design is based on a CMOS double pair [7], and is shown in figure 4. Advantages of the CMOS double pair transconductor include its ability to be used to implement a grounded resistor, and the absence of mismatch problems between NMOS and PMOS transistors. Problems do exist, however, in terms of linearity and mismatch between the NMOS threshold voltages due to the body effect. The equivalent resistance is given by equation 2.

$$R_{eq} = \frac{V_{in}}{I_{in}} = \frac{1}{4K_{eq}(V_{G1} - V_{Teq})} \quad (2)$$

A CMOS test chip, designed in double poly, triple metal 0.8µm CMOS, was fabricated. The chip contains four current conveyor-based CABs and a transmission gate-based interconnection network. Figure 5 shows a block

diagram of the chip. Each circle represents a transmission gate connecting the two crossing wires. The X input on each CAB is connected to the X node on that CAB's current conveyor; this is done so as to implement adders and subtractors. The current conveyors are organized in a bipartite architecture, with connection between CCIs of different groups.

4. Test Chip Results

Figure 6 shows a die photo of the chip. Dimensions of the chip are $3.5\text{mm} \times 1.5\text{mm}$.

An amplifier is configured by turning on the transconductors on the X and output nodes. Figure 7 shows the steady state response of an input sine wave at 500kHz, at high gain. Figure 8 shows the frequency response of the amplifier at a gain of 14dB. The 3dB points for various gains were measured at 11 to 13MHz and are in agreement with current conveyor theory which states that bandwidth should be constant. Gains vary from 2 to 14dB. The total harmonic distortion was measured at 2.89% (30.8dB) for a 10kHz 0.5V_{pp} input sine wave (the input wave had a THD of 0.92%). Output noise of the amplifier for a bandwidth of 12MHz was measured as 11.52mV_{rms}, resulting in a signal-to-noise ratio of 38.8dB for a 1V output. Power dissipation for the test chip in the amplifier configuration is 162mW for 5V operation. This compares well with simulation results of 165.3mW; simulations also show that the power dissipation of each current conveyor is 4.9mW. Most of the power dissipation is lost in the chip's output buffers, which each consume 28mW (included in the 162mW).

Tests were also performed for integrators, differentiators, and adders, all of which were functional. Test results are summarized in table 1.

5. Conclusions

Current field-programmable analog array designs operate at 100kHz frequencies. However, video bandwidths are in the order of 10MHz. In this paper the circuitry necessary for the development of field-programmable analog arrays operating at video frequencies, has been presented. Current conveyors were seen as being a viable option in achieving a video frequency FPAA.

Section 3 presented the design and implementation of a simple FPAA designed to operate at video bandwidths, using current conveyors. A test chip was fabricated in a 0.8 μm CMOS process. Test results demonstrated bandwidths of over 10MHz for a current conveyor-

based amplifier, as well as functionality of an integrator, differentiator, and adder. These developments are seen as a first step towards the development of a complete current conveyor-based FPAA.

6. Future Work

Among future areas of research will be FPAAs with even higher bandwidths and improved performance specifications, field-programmable mixed-signal arrays, CAD tools dedicated to FPAAs, on-chip programming memories, and low power-supply FPAAs, and well as s.

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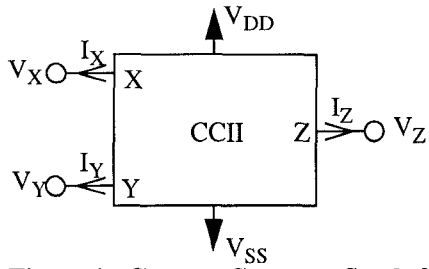


Figure 1: Current Conveyor Symbol

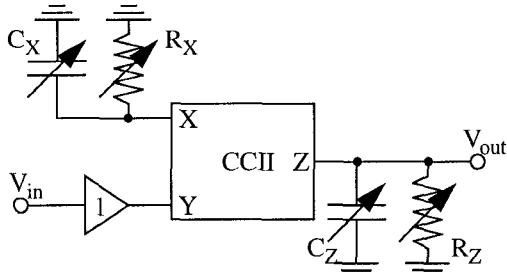


Figure 2: CCII-Based CAB

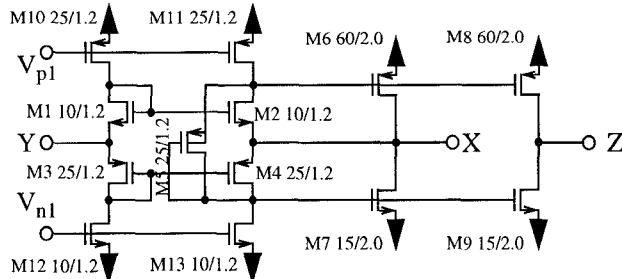


Figure 3: Current Conveyor Schematic

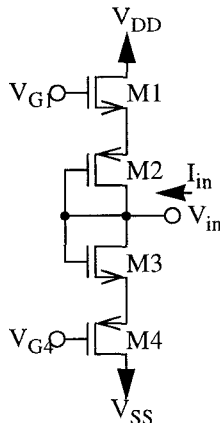


Figure 4: Transconductor Schematic

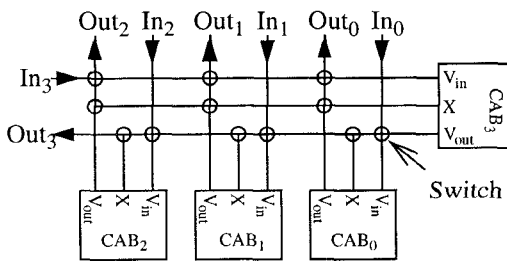


Figure 5: Test Chip Block Diagram

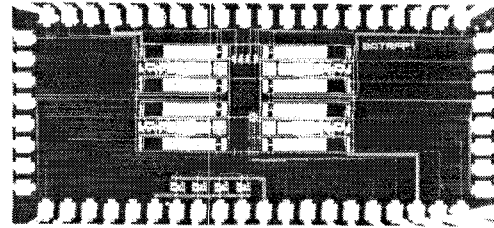


Figure 6: Chip Die Photo

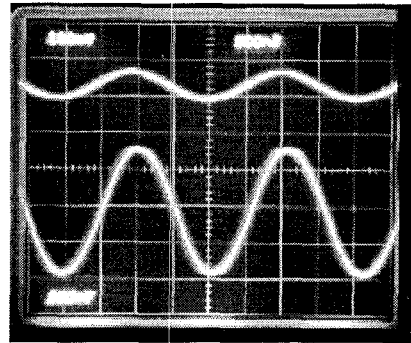


Figure 7: Amplifier Response at High Gain

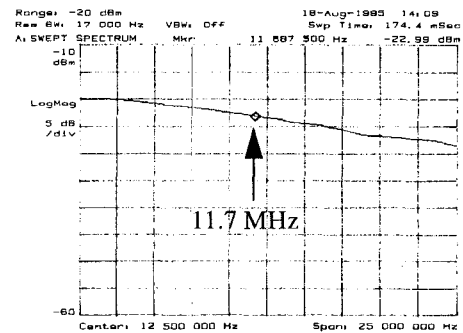


Figure 8: Amplifier Frequency Response

Parameter	Result
Power Supply	5V
Power	162mW
f_{-3dB}	11MHz
Maximum Gain	14dB
THD	2.89%
SNR (1V Output, 12MHz BW)	38.8dB

Table 1: Summary of Test Results