

Towards a Current Conveyor-Based Field-Programmable Analog Array

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Abstract

This paper presents the design of a CMOS field-programmable analog array using second-generation current conveyors. An FPAA containing 4 configurable analog blocks and designed in a $0.8 \mu\text{m}$ CMOS process, has been submitted for fabrication. Simulation results show expected bandwidths of 10 MHz. Core area for the FPAA IC is $1551.8 \times 741.2 \mu\text{m}^2$.

1. Introduction

Recently, several new university and industry-based field-programmable analog array (FPAA) ICs have been announced. An FPAA is an integrated circuit containing user-programmable analog circuitry and interconnect. An FPAA designer specifies a description of an analog design in a CAD tool which then maps the circuit onto the given FPAA architecture. That mapping is then loaded into memory on the FPAA IC, so as to instantiate the user's circuit. Reprogramming of the FPAA can be done in a matter of hours instead of months. FPAAs, like FPGAs, are useful when designing small numbers of circuits, where the expense of developing a custom ASIC would be too large.

Current FPAA designs include two continuous-time designs done by Lee and Gulak [1][2], one of which is based on operational amplifiers and MOS transconductors, and which operates at 100 kHz bandwidths. Industrial designs include the CMOS switched capacitor designs by IMP Inc. [3] and Pilkington Microelectronics [4]; these industrial designs also operate at 100 kHz frequencies. Zetex Semiconductors has recently introduced a continuous-time FPAA based on bipolar technology operating at 4 MHz bandwidths [5].

Work is currently underway to develop CMOS FPAAs which will operate at 10 MHz bandwidths. Our approach, as well as that in [6], is based on the second generation current conveyor (CCII) [7]. Current conveyors are explained in section 2. Section 3 describes our CCII-based FPAA design. Section 4 concludes this paper.

2. Current Conveyor-Based FPAA

The CCII, depicted in figure 1, is a three terminal building block which, like an operational amplifier, can be used to construct various useful analog functions.

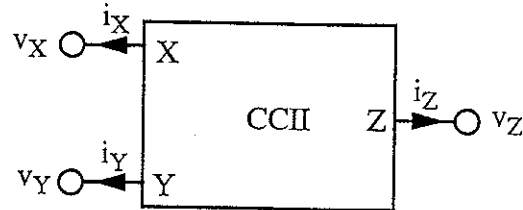


Figure 1: Current Conveyor Diagram

Its response is given by:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm\beta & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

Normally $\beta = +1$, in which case the notation CCII+ is used.

A CCII-based amplifier is shown in figure 2.

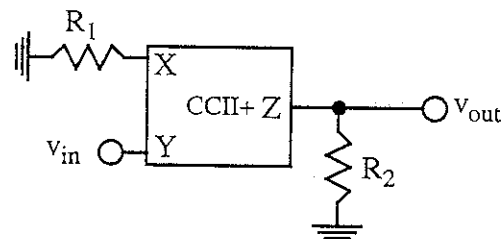


Figure 2: CCII-Based Amplifier

Here, an input voltage v_{in} applied at node Y will be replicated at node X. This will produce a current i_X equal to v_{in}/R_1 , coming out of node X. That same current will get copied out of node Z, and will flow into resistor R_2 , producing an output voltage v_{out} equal to $v_{in}(R_2/R_1)$. Other useful analog functions such as integrators, adders and rectifiers, can also be implemented using current conveyors, resistors,

capacitors and diodes.

3. CCII-Based FPAA

The configurable analog block (CAB) is the basic building block for a FPAA. Desirable functions for a CAB include amplification, integration, and differentiation. Figure 3 shows a current conveyor-based implementation of a CAB capable of implementing the aforementioned functions.

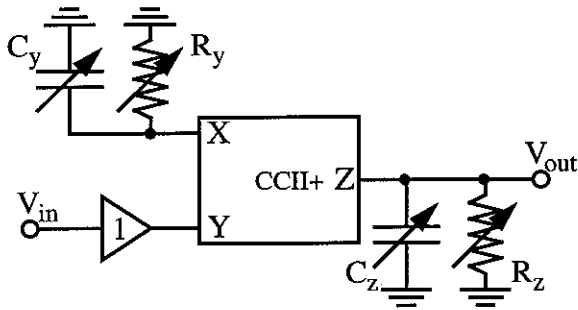


Figure 3: Configurable Analog Block

The variable capacitors are implemented using programmable capacitor arrays, and the variable resistors are implemented using CMOS double pair transconductors [8].

A chip containing four CABs based on the CCII, and an interconnection network based on transmission gates, is currently being fabricated in the 0.8 μm CMOS process available through CMC. Figure 4 shows a schematic diagram of the chip, with the CABs and interconnect.

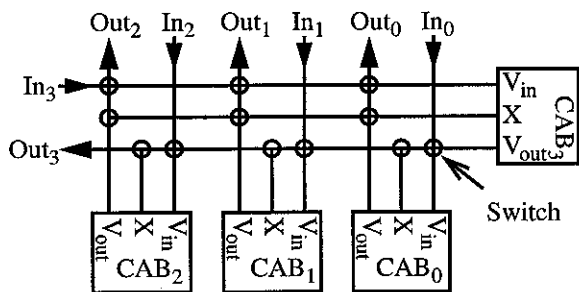


Figure 4: CCII-Based FPAA Schematic

The core area is 1551.8 x 741.2 μm^2 . Simulation results for an amplifier, depicted in figure 5, show that we can expect 10 MHz bandwidths from this FPAA.

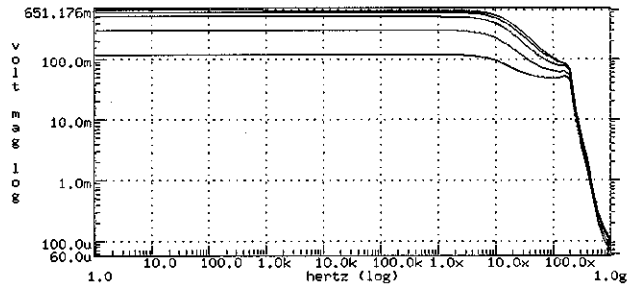


Figure 5: Amplifier Hspice Simulation

4. Conclusion

This paper has presented the design of a field-programmable analog array implemented using current conveyors and submitted for fabrication in a 0.8 μm CMOS process.

Given recent growths in the area of mixed-signal ICs, it is expected that we will soon see increasing demand for field-programmable mixed-signal arrays (FPMA). An FPMA is an IC that contains both an FPAA and an FPGA, linked together by the use of configurable converter blocks.

Up to date information about FPAAs and FPMAs can be obtained from our web site at the following address: <http://www.eecg.toronto.edu/~vgaudet/fpaa.html>.

Bibliography

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