

# A SHUFFLE EXCHANGE IMPLEMENTATION OF VITERBI'S ALGORITHM USING CMOS VLSI

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## ABSTRACT

Viterbi's algorithm can be used in a communications receiver to decode convolutional codes, or decode signals distorted by inter-symbol interference and noise. A completed design is presented which embeds a Shuffle Exchange layout of Viterbi's algorithm in CMOS VLSI technology. Considerations for expanding the design are also presented.

## INTRODUCTION

This paper describes a VLSI design methodology for implementing Viterbi's Algorithm. The resulting layout is practical with present technology, and flexible in terms of future design expansion and changes.

Viterbi's algorithm is useful for solving both inter-symbol interference (ISI) and convolutional decoding problems. Since the solutions for both problems are almost identical, ISI will be discussed.

For a finite bandwidth communications channel, inter-symbol interference becomes the dominant channel characteristic as a system is pushed closer to its theoretical capacity. ISI occurs when each channel output bit is affected by the current input, and the previous  $Q$  inputs. ( $Q$  is called memory length or constraint length.) The channel can be modelled as a finite state machine, with the current input determining the state transition.

Viterbi's algorithm combats ISI by taking into account the previously received symbols when determining the currently received symbol. The algorithm is a graph search procedure applicable to trellises, and determines a path through the trellis states least likely to contain an error. Figure 1 shows the trellis for a binary channel with memory length of 2 bits. As an example, if the 2 previously transmitted bits were (0,0), the channel would be in state 0. Receiving a 0 would cause a transition into the 0 state, while receiving a 1 would cause a transition into state 1, as the 2 most recent bits would be (0,1) at the next bit interval.

For a binary channel, each state has 2 possible transitions. A model of the expected channel characteristics is used to compare the received signal value with that expected ideally for each state transition. The measure of this match with the ideal is called the transition metric for that transition. The state metric is the sum of all transition metrics used to get to that state since time zero, using the path with the lowest sum. Figure 1 shows how the transition metrics are added to the state metrics, and the lowest sum chosen for each state.

The graph search mentioned above can be conveniently implemented as a shuffle exchange (SE) layout, [1] which is area efficient and has high throughput. It uses  $2^Q$  processors for a binary channel, where  $Q$  is the memory length. Each processor corresponds to a state, and concurrently calculates and selects both transition metrics for that state. Thus, the receiver hardware shown in figure 2 must perform 3 basic operations: a) add the transition metrics to the sum of the previous metrics, b) compare

the metric sums, and c) select the lowest sum and record its corresponding state history. These three operations constitute an ACS (add-compare-select) processor.

## LAYOUT CONSIDERATIONS

In searching for general guidelines for laying out a SE Viterbi Receiver in VLSI, several physical constraints which are not addressed in VLSI layout theory must be kept in mind.

Available chip area is always a constraint. One is forced either to construct a receiver of a low enough resolution or constraint length to fit on a single chip, thereby increasing the error rate of the receiver, or else the problem must be partitioned to fit onto multiple chips.

If a multi chip configuration is chosen, one must immediately deal with time penalties inherent in crossing package boundaries. Because the ACS operation occurs simultaneously in all processors, if even one metric must cross a chip boundary, the ACS operation must synchronize with the slowest transfer. Likewise, the processing speed is limited by the slowest survivor sequence transfer. If multiplexing becomes necessary, the I/O speed can be severely limited.

One can observe from figure 3 that processors are grouped into loops called necklaces and connected in pairs called edges. Because the number of pins on a package is limited, it is important to partition the SE graph where connections outside each package are minimized. One may either package 2 edge processors together, or all or part of a necklace. Both solutions produce a low I/O partitioning of the trellis. As technology improves, and the ratio of chip size to processor area becomes larger, the factor governing how many processors can be placed on each chip will likely be the number of contacts each processor requires with the outside world.

Finally, one may reduce the amount of I/O per chip by separating the two functions of metric handling, and survivor sequence routing. By exporting the metric selection signal for each processor, one may construct the survivor sequence multiplexors and latches on a separate chip. In fact, a rough layout indicates that 5 micron technology could support a 16 processor survivor sequence circuit with 7 to 10 bit registers. Unfortunately, for 64 or more processors, either the select pins will require multiplexing, or the survivor sequence chip will also need to be partitioned, again causing I/O problems in this type of scheme.

To gain insight into the limitations discussed above, a test chip was designed. The current chip uses short constraint length and low resolution for a single chip solution. Future work will involve partitioning the problem between several chips.

## THE TEST CHIP

A single chip Viterbi Receiver was designed from logic cells in the CMOS library compiled by the University of Manitoba VLSI Design group. The layout was done using ELECTRIC running on a Metheus design work-station, and was submitted to the Canadian Microelectronics Corporation for fabrication in a 5 micron process with single metal and polysilicon layers.

The receiver corresponds to the trellis in figure 1. The 4800 by 4800 micron die allowed each of the 4 processors to use 4 bit resolution of the transition metrics, and 6 bit representation of the state metric sums. The metrics are generated off chip to save the space that the lookup ROM would require. The resulting layout is shown in figure 4.

The hardware converts each quantized channel symbol into two 4 bit transition metrics for each processor using 8 external lookup ROMs. Two ripple carry adders in each processor add the corresponding transition metrics and state metrics at the inputs and generate 6 bit sums. A comparator chooses the lesser of the two sums, retaining only that sum along with its state history. The normalization circuit subtracts 16 from all the

sums (this involves only the upper 2 bits) once the lowest sum exceeds 15. Software simulation confirms that using 2 extra bits in the sums with normalizing avoids overflow. The state histories, or survivor sequences, are truncated to the most recent 6 transitions. Simulation has shown that this produces negligible decision degradation. The oldest survivor sequence bit of one of the processors is taken to be the decoded output after each symbol interval and the next input is then processed.

The receiver decodes one symbol per clock cycle. On the rising edge of the clock, previous metric sums become available at the latch outputs, and the ACS operation ripples through. The selection is made, and on the negative clock transition, the selected survivor sequences are latched. On the next positive transition, the sums are latched, and the process repeats.

Because each processor receives two 4 bit metrics from off-chip, two 6 bit metric sums and two 6 bit survivor sequences from other processors, and generates 6 bit wide sums and survivor sequences, a large portion of the layout is devoted to wiring.

## CONCLUSIONS

Using 5 micron technology, it has been shown that a binary Shuffle Exchange Viterbi Receiver can be constructed for a constraint length of 2. The design can decode 1 symbol every clock cycle, paced to the speed of an ACS operation. With proper problem partitioning, receivers with larger constraint lengths can be constructed.

## REFERENCES

- [1] Gulak, P.G., "VLSI Structures for Digital Communication Receivers", Ph.D. Dissertation, Department of Electrical Engineering, University of Manitoba, 139 pages, 1984.

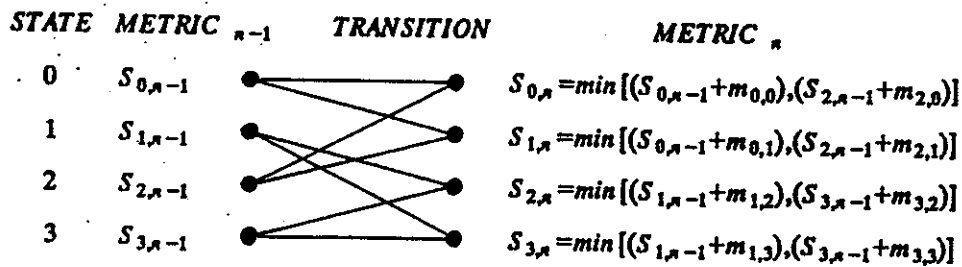


FIGURE 1 Viterbi Trellis for Binary Channel  $Q=2$

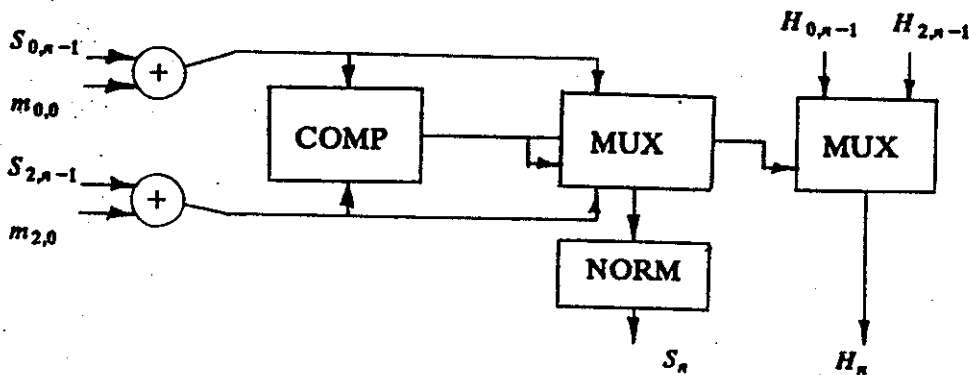


FIGURE 2

ACS Unit for State 0

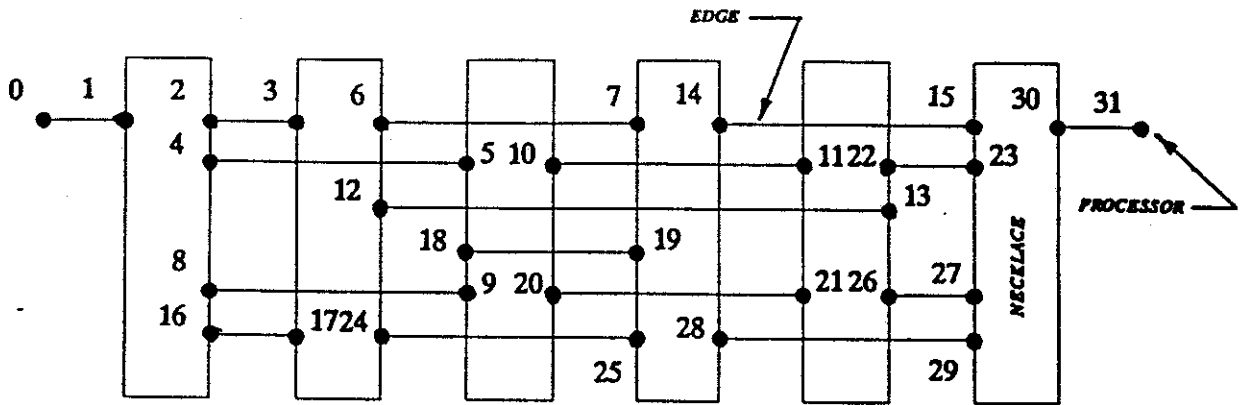


FIGURE 3 SE Graph of a Binary Viterbi Receiver for  $Q=5$

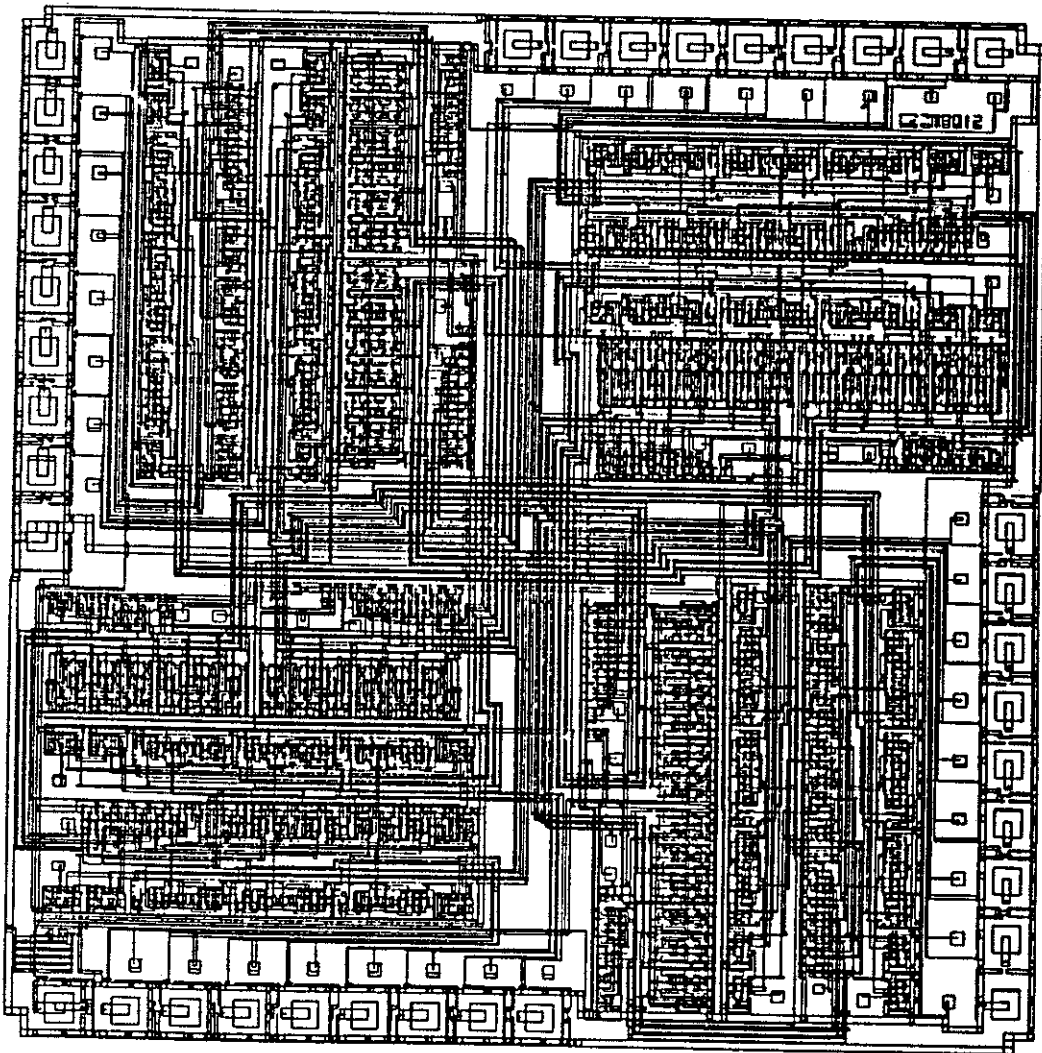


FIGURE 4 SE Viterbi Receiver Test Chip