High Speed DRAMs for ASIC Memory Applications

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Abstract

The design and implementation of a high speed Dynamic RAM memory with limited telescoping capability in CMOS3 is presented. The RAM components are designed for easy inclusion in custom designs as standard cells. The DRAM uses a high speed $1/3-V_{DD}$ sensing scheme and a 3 Volt power supply. Circuit design improvements such as isolation during sensing and simplified reference voltage generation are presented. Equations for hand analysis and design are presented. Eight test cells have been fabricated and tested. These cells show an access time of 40ns and a cycle time of 100ns with a 2pF load providing a maximum speed of 10MHz.

1 Introduction

Dynamic Random Access memories have been the dominant component family in a wide and varied range of integrated circuit products. Significant and almost continuous advancements in process technology and circuit design have provided for new and faster DRAMs every year for the past decade. While these advancements have benefitted large scale memories, their use in small scale applications has not been widely exploited.

The purpose of this work is to explore circuit design techniques that will be useful in designing relatively high speed DRAMs on a much smaller scale. The aim is to provide the designer with a means of quickly constructing small, high speed dynamic register files. For this reason, the proposed design must be modular and have a limited telescoping capability.

This paper proposes just such a small scale DRAM based on a $1/3-V_{DD}$ sensing scheme [1] and a 3 Volt power supply. The lower power supply was chosen to maintain compatibility with future sub-micron processes and for device reliability considerations. Section II presents simple equations for hand analysis and design of DRAMs. Section III presents the cell circuit designs, the advantages of the $1/3-V_{DD}$ sensing
scheme and design of a complementary cross-coupled sense amplifier. Section IV presents circuit timing and proposed circuits for self-timing the DRAM. Test results and conclusions are presented in Section V.

2 Design Equations and Tradeoffs

A simple, first order model of a DRAM, useful for hand analysis is shown in Figure 1. From charge sharing theory [2], the resultant bitline voltage upon closure of the switch SW1 is:

$$ V_R = \frac{Q_T}{C_T} = \frac{C_{BL}V_{BL} + C_SV_{S1}}{C_{BL} + C_S} $$

(1)

We are interested in the change in bitline voltage after switch closure since this is the signal which must be amplified. The change in bitline voltage can be expressed as:

$$ \Delta V = V_R - V_{BL} = \frac{V_{S1} - V_{BL}}{1 + C_{BL}/C_S} $$

(2)

where $V_{S1}$ is the stored voltage level representing a one, $V_{BL}$ is the bitline precharge voltage, $C_{BL}$ is the total bitline capacitance, and $C_S$ is the cell capacitance. $\Delta V$ is a significant quantity known as the signal development or sense signal.

Equation 2 identifies important design tradeoffs in the cell design. In order to minimize area, we must keep $C_S$ as small as possible. This is limited by the size of the $C_{BL}$ which causes attenuation of the sense signal. $C_{BL}$ can easily be on the order of picofarads and must be kept to a minimum, hence it practically determines the size of the transistor used as the transfer gate. At low power supply voltages, $V_{S1}$ becomes increasingly important due to the body effect of the transfer gate. In CMOS3 the body effect raises the nominal NMOS threshold to 1.5V for a 3V substrate bias. This represents half the signal swing and decreases the amount of charge we can store on the cell. This in turn makes the sense signal smaller and hence the entire cell design is more critical.

A Figure of merit can be defined to evaluate cell designs. The Charge Transfer Ratio $T$ [3] is defined as:

$$ T = \frac{1}{1 + nC_{BL}/C_S} \leq 1 $$

(3)

5.3.2
where \( n \) is the number of cells on the bitline. It can be thought of as the fraction of the maximum possible sense signal\(^1\) that actually appears on the bitline. Obviously higher values of \( T \) are more desirable and it is generally in the range of 5\% to 25\%.

## 3 Cell Design

The \( 1/3-V_{DD} \) sensing circuit is shown in figure 2. Transistors M6-M9 form a complementary sense amplifier consisting of cross-coupled NMOS and PMOS pairs. \( \phi_S \) and \( \phi_{SP} \) are complementary latching clocks. The NMOS transistors M1-M3 are used to precharge and equalize the bitlines and are controlled by clock \( \phi_{pr} \). Transistors M1 and M2 switch the 1-Volt precharge voltage supply onto the bitlines. Transistors M12 and M13 isolate the sense amplifier from the large capacitance of the bitline during sensing. Isolation is controlled via clock \( \phi_{iso} \). Transistors M4 and M5 switch the cell and dummy cell onto their respective bitlines when required.

At the end of the previous active cycle, the bitline BL and its complement \( \overline{BL} \) are at \( V_{DD} \) and GND respectively. The bitlines are then precharged and a 1 Volt reference level is stored in the dummy cell by asserting \( \phi_{pr} \) and DWL. Once precharge has been achieved, the DWL will be dropped, but \( \phi_{pr} \) will stay asserted until a read or write is requested. If a read is requested, WL and DWL are asserted, causing two simultaneous charge transfers from the storage capacitors to the bitlines. After sufficient differential signal has been developed between the bitlines \( \phi_{iso} \) is applied to

\[^1\]V_{S1} - V_{BL} \text{ is the maximum, occurring when } C_S = \infty. \]
isolate the sense amplifiers and $\phi_s$, $\overline{\phi_{so}}$ are turned on to amplify and latch the state of the bitlines. After latching has occurred, $\overline{\phi_{iso}}$ is raised allowing cell rewrite to occur.

The reference generation scheme has been simplified due to the fact that the precharge voltage is sufficient to be used as a reference. This eliminates one dummy cell, an equalization transistor and a reference generation phase from the conventional scheme (see [1]).

The sense amplifiers (M6-M9) are a complementary pair of clocked differential amplifiers. The amplifiers are cross-coupled to provide positive feedback to latch the sense voltage on the bitlines. Speed optimization was performed by spice simulations. It was found that common speed optimization techniques such as dual-slope sensing [4][5] were not beneficial and hence the sense amplifiers are controlled by simultaneous complementary clocks. One speed up technique developed was that of isolation of the bitlines from the large bitline capacitance during sensing. This provides a significant speed increase in sense amplifier latching.

Performance Comparison Table 1 compares parameters relating to the performance of the $1/3-V_{DD}$ sensing scheme relative to the $1/2-V_{DD}$ sensing scheme. Signal development time is defined as the time interval between the start of wordline assertion and the time when the differential signal between BL and $\overline{BL}$ reaches 100 mV. The table is developed assuming a one is stored. If a zero is stored, charge transfer starts as soon as the wordline is raised above $V_{TN}$ of the pass transistor. Hence in an NMOS array, signal development is always faster when reading a zero than when reading a one.

From the table, the advantage of the $1/3-V_{DD}$ scheme can be seen. Since the bitline capacitance is much larger than the storage capacitance, bitline voltage change will be less than the storage cell voltage change during charge transfer. Thus it is desirable for the source of the transfer gate to be the bitline, since the overdrive on the gate would remain for a longer period of time, hence keeping the transfer gate at higher current levels during readout. Examining the table we see that in the $1/2-V_{DD}$ case, there is no charge transfer from the cell and the dummy cell determines the final state of the bitlines. Furthermore, the dummy cell also loses its overdrive faster since it has the cell as its source making readout slower. In the $1/3-V_{DD}$ scheme, the situation is much better. The dummy cell contributes no charge to signal development, serving only as a reference. The storage cell develops all the sense signal and has the bitline as its source, thus its overdrive remains at a higher level for a longer time and the maximum available overdrive on the cell is larger.

4 Circuit Timing

An asynchronous self-timed approach is taken for the timing of the DRAM circuit. Two of the most critical timing circuits are discussed. During precharge the dummy

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$^2$The opposite is true for a PMOS array
<table>
<thead>
<tr>
<th>Storage Cell</th>
<th>Sensing Scheme</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Stored</td>
<td>1.5V</td>
</tr>
<tr>
<td>Source (Transfer Gate)</td>
<td>BL</td>
</tr>
<tr>
<td>WL Turn-on</td>
<td>3.0V</td>
</tr>
<tr>
<td>Max. Overdrive</td>
<td>0.0V</td>
</tr>
<tr>
<td>Dummy Cell</td>
<td>Voltage Stored</td>
</tr>
<tr>
<td>Source (Transfer Gate)</td>
<td>Dummy Cell</td>
</tr>
<tr>
<td>DWL Turn-on</td>
<td>2.5V Transfer</td>
</tr>
<tr>
<td>Max. Overdrive</td>
<td>0.5V</td>
</tr>
</tbody>
</table>

- $V_{TN} = 1.5V$  $V_{TP} = -1.65V$

Table 1: 1/3-$V_{DD}$ vs. 1/2-$V_{DD}$ Performance Comparison.

Wordline clock DWL is required to be asserted for reference generation, then de-asserted once completed. A proposed circuit to do this is shown in figure 3. STROBE controls the onset of the precharge state. The OR gate on the bitlines is ratioed to detect when the bitlines are both at precharge level. It then asserts prechgdone which causes the DWL to drop. Note also that DWL is activated upon assertion of WL as well. The isolation clock $\bar{\phi}_{iso}$ is another critical timing signal. A proposed circuit for its generation is shown in figure 4. We must provide a delay between wordline assertion and isolation sufficient to allow signal development. This delay has been determined by simulation to be about 10ns. The circuit in Figure 4 employs a Schmitt Trigger to generate a stable delay between the wordline and the isolation clock. The circuit operates as follows: during precharge, the ratioed NOR gate has its output high. When a read is to take place, read is asserted.

When a read is to take place read is asserted along with the appropriate wordline WL. WL immediately turns on the transfer gate and signal development begins. However, assertion of $\bar{\phi}_{iso}$ is delayed by an amount controlled by the Schmitt trigger hence providing the signal development time. After the sense amplifiers latch, the NOR gate output goes low and $\phi_{iso}$ is deasserted, allowing cell rewrite to occur.

5 Test Results and Conclusions

The test chip is shown in figure 5. It contains 8 DRAM cells without timing circuitry. The cell design parameters are as follows:
Figure 3: Precharge Detection Circuit

Figure 4: Isolation Clock generation
$V_{BL} = 1V$ - The bitline precharge voltage.

$V_S = 1.5V$ - for a stored one

$C_S = 750fF$ - The cell capacitance.

$C_{BL} = 2.5pF$ - The bitline capacitance.

$T = 25\%$ - The Charge Transfer Ratio.

The bitline capacitance was chosen to be $2.5pF$ in order to let the RAM telescope to a maximum of 32 cells on the bitline. With these parameters, the cell area in $3\mu m$ CMOS technology is $96\mu m \times 45\mu m$ using an $18\mu m$ wide transfer gate. A comparable static RAM designed with minimum size transistors would be $110\mu m \times 80\mu m$. This $2X$ area advantage can be increased if either the transfer gate is made smaller or the cell size is decreased, at the cost of speed.

Testing was performed with the HP8180 data generator and response was measured from probing pads on chip using picoprobes. A bitline load of $2.5pF$ was used. Test waveforms for reading a one are shown in figure 6. Access time was measured to be 40ns while the cycle time was measured to be 100ns. The circuit had a refresh interval of approximately 20ms.

In conclusion, we have successfully designed and tested a high speed DRAM in a conventional CMOS process. The design featured a $1/3-V_{DD}$ bitline precharge to provide improved signal development time.

We have also been able to provide for a limited telescoping capability allowing between 1 to 32 cells on the bitline without redesign. This makes the components attractive for ASIC designers who need small register banks, but cannot afford the extra area of fully static designs.
Figure 6: Waveforms for reading a one. SCALE: 30ns/div 3V/div. Top waveform: Bitline; Bottom Waveform: Wordline

References


