DUAL SYSTOLIC ARCHITECTURES FOR DIGITAL SIGNAL PROCESSING IN VLSI

M. Yunik, W. Pries, R.D. McLeod, G.E. Bridges
P.G. Gulak and H.C. Card

VLSI Research Laboratory
Department of Electrical Engineering
Winnipeg, Manitoba, Canada R3T 2N2

ABSTRACT

The VLSI implementation of digital signal processing systems based upon matrix multiplication algorithms is presented. We illustrate these concepts using the example of an architecture which implements the Walsh transform. The matrix elements are well defined operations such as addition, subtraction or comparison, and in the Walsh domain lead to area-efficient layouts. One of the novel features of this work is the method by which the indices used to activate a particular processor are generated, with the result that the algorithm becomes independent of the problem size instance.

I. INTRODUCTION

Recently proposed VLSI architectures generally incorporate high degrees of parallel, pipeline, systolic or hierarchical techniques. Several VLSI computational and design models have also been proposed and a variety of metrics derived for performance evaluation [1,2,3]. Perhaps the most common are the VLSI grid model and the AT^2 metric. Aside from theoretical metrics there are also the practical limits imposed by a developing VLSI technology. These include packaging as well as limits upon maximum integration complexity.

In this paper, we are illustrating the implementation of a signal processing system based upon matrix multiplication. In the present study the matrix elements are limited to simple arithmetic functions defined by Boolean operations on their indices. One such problem instance includes the calculation of Walsh transforms.

The architecture we have selected is a dual systolic type, incorporating a novel method of matrix element or coefficient generation. It should be pointed out at this time that for these matrix operations the AT^2 metric has been shown [4,5] to have a lower bound of $O(n^2)$ for implementation on both shuffle exchange graphs (SE) and cube connected cycle graphs (CCC), while the systolic architecture has an AT^2 lower bound of $O(n^3)$. However, I/O limitations and the matrix coefficient generation complexity limit the physical realization of these matrix operations on either (SE) or (CCC) architectures using present technology. The resulting AT^2 metric for implementation of a reasonably sized structure using either architecture is then $O(n^4)$. With these considerations, the dual systolic architecture was chosen as a viable contender for the implementation of specific matrix multiplication problems such as the Walsh transform.

II. IMPLEMENTATION

The recurrence relation for systolic matrix multiplication, $\tilde{X} = W\tilde{x}$ is

$$X_i^{(1)} = 0$$

$$X_i^{(k+1)} = X_i^{(k)} + w_{ik}x_k \quad (1)$$

$$X_i = X_i^{(n+1)}$$

where $\tilde{X}, \tilde{x} \in R^n$. $\tilde{X}$ is defined as the Walsh transform of $\tilde{x}$ and $W = [w_{ik}]$. Walsh functions form a complete orthonormal basis in R^n space with an additional advantage that $W^{-1} = W/n$ where $w_{ik} \in \{-1, +1\}$. For natural ordering [6]

$$w_{ik} = (-1)^{\langle i,k \rangle} \quad (2)$$

where i,k are the matrix row and column indices represented in binary notation.

Since $\tilde{X}$ can be calculated using only addition and subtraction, the transform can be easily calculated systolically with relatively simple inner product step processors as shown in Fig. 1.

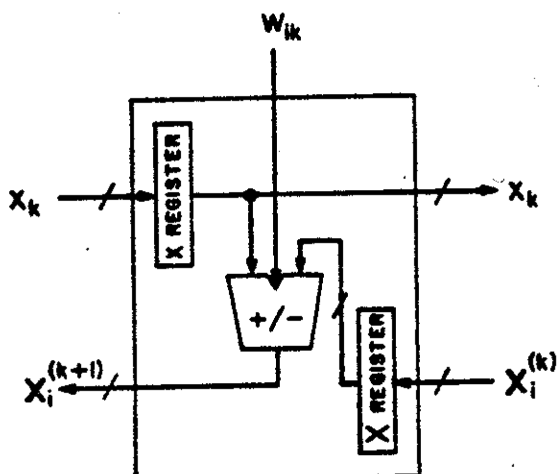

FIG. 1 Typical inner product step processor for systolic implementation of the Walsh transform.

The coefficient w_{ik} as computed in Eq. (2) can also be implemented using a modified linear systolic array of processors. The matrix element indicies are generated by counters at both ends of the array. Pass transistor logic is then employed to generate the appropriate matrix coefficients w_{ik} from the indices as shown in Fig. 2. Coefficient generation utilizing pass transistor logic greatly enhances VLSI implementation.

The dual systolic architecture for implementing the Walsh transform combines the coefficient generation array with the systolic matrix multiplication array as shown in Fig. 3. The top array of processors is used to generate the coefficients and any control signals with the second array or backbone being used to perform the matrix multiplication (addition or subtraction in the Walsh domain). Two on-board counters are used to generate the matrix element indices.

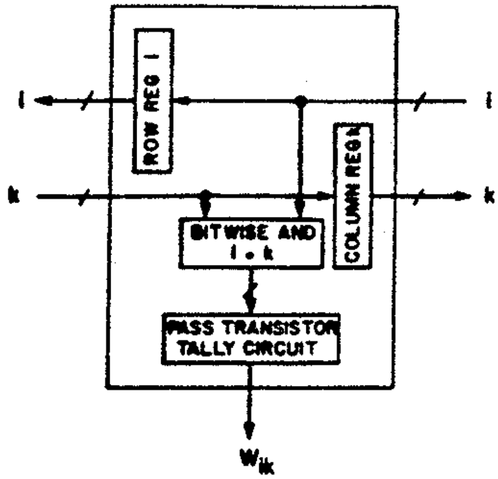

FIG. 2 Typical co-processor for array element generation.

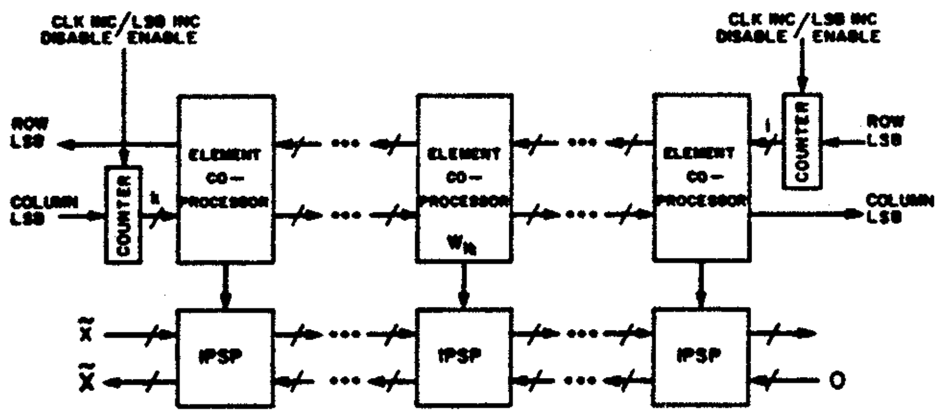

FIG. 3 Schematic of the dual systolic array processor.

The proposed dual systolic architecture appears to satisfy much of the criteria for VLSI realizability [7]. The design makes multiple use of each input data item, that is, the input and output data streams are pipelined and used by all processors. Moreover, successive matrix multiplication problems can also be pipelined with the addition of limited control logic. The design utilizes extensive concurrency; for an n point operation, an average of n/2 processors are computing simultaneously. The dual systolic design is also easily cascaded, this being accomplished by activating successive counters with the lowest order bit of the preceeding module. With respect to complexity, the different cells are few in number and of simple topology which would greatly reduce design and implementation costs. The data and control flow is simple and regular. The only global communication aside from power and ground is the system clock, which presents no problem for one dimensional arrays of almost any length.

As an example which represents the practical constraints for VLSI implementation a 1 K point transform was selected. A typical processor in the coefficient generation array requires two 10 bit registers for holding the matrix column and row indicies. Limited area is required to generate the matrix coefficient, since pass transistor logic is employed. A systolic matrix multiplication array processor requires a data register, an adder/subtract circuit, and an accumulation register, with the accumulation register being 10 bits wider than the associated data register. With these considerations it is easily seen that dual systolic architecture falls into the realm of present day integration technology.

III. SUMMARY

In summary, the dual systolic design appears to be feasible and realizable, particularly in systems that implement fixed, well understood computational routines.

In this paper we have demonstrated a novel method for generating the matrix elements for problem instances where they are represented by simple operations derived from their indicies. The specific case discussed was the dual systolic implementation of the Walsh transform. Although further research is required, we feel the dual systolic architecture may be utilized to realize a variety of DSP problems.

IV. ACKNOWLEDGEMENT

The financial support of the Natural Sciences and Engineering Research Council (NSERC) of Canada is gratefully acknowledged. W. Pries, R.D. McLeod, G.E. Bridges and P.G. Gulak also acknowledge support under NSERC graduate fellowships.

V. REFERENCES

[1] C.D. Thompson, "Area-time Complexity for VLSI", Proc. 11th Annual ACM Symposium on the Theory of Computing, pp. 81-88, 1979.

[2] G. Bilardi and F.P. Preprata, "An Architecture for Bitonic Sorting with Optimal VLSI Performance", IEEE Transactions on Computers, vol. C-33, no. 7, July 1984.

[3] J.D. Ullman, Computational Aspects of VLSI, Computer Science Press, Rockville, Maryland, 1984.

[4] H.S. Stone, "Parallel Processing with the Perfect Shuffle", IEEE Transactions on Computers, vol. C-20, no. 2, pp. 153-161, Feb. 1971.

[5] F.P. Preprata and J. Vuilleman, "The Cube-Connected Cycles: A Versatile Network for Parallel Computation", Comm. of the ACM, vol. 24, no. 5, pp. 300-304, May 1981.

[6] N. Ahmed, H.N. Schreiber, and P.V. Lopresti, "On Notation and Definition of Terms Related to a Class of Complete Orthonormal Functions", IEEE Trans. Electromagn. Compat., vol. EMC, no. 2, pp. 75-80, May 1973.

[7] H.T. Kung, "Why Systolic Architectures?", IEEE Computer Magazine, pp. 37-46, Jan. 1982.