University of Toronto FPGA Seminar

SimXMD
Co-Debugging Software and Hardware in FPGA Embedded Systems

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September 19, 2013

The “When Harry Met Sally” rule of CAD

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“Women and Men can never be friends.

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“Designers and Tools can never be friends.

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“Designers and Tools
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The Sex
will always get in the way.”

The "When Harry Met Sally" rule of CAD

"Designers and Tools
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The Semantics
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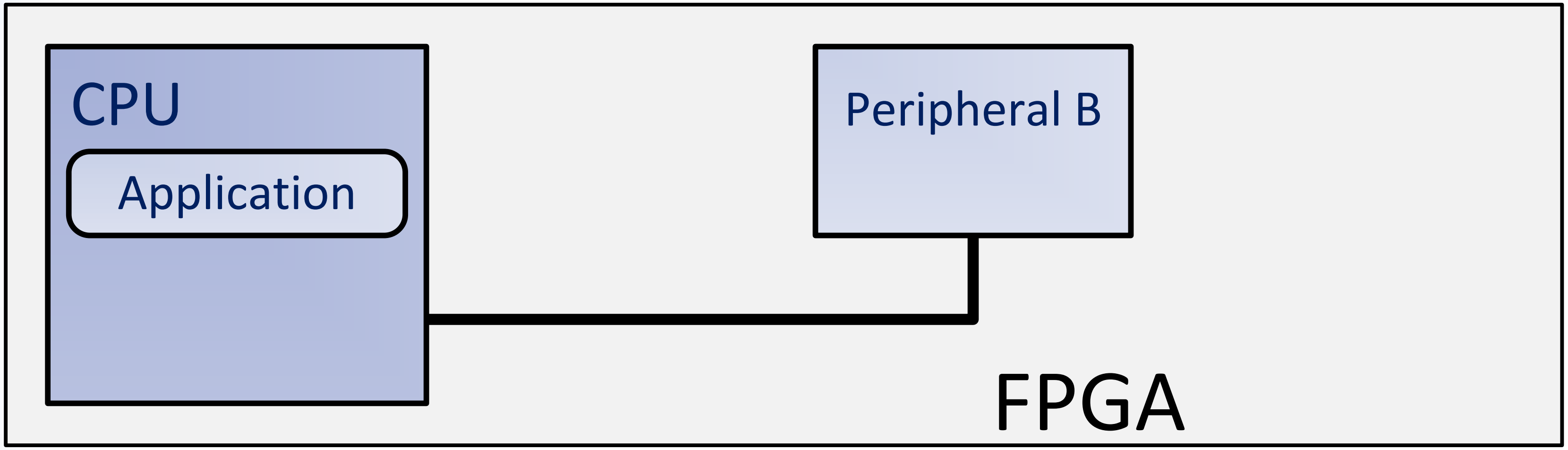
FPGA embedded systems



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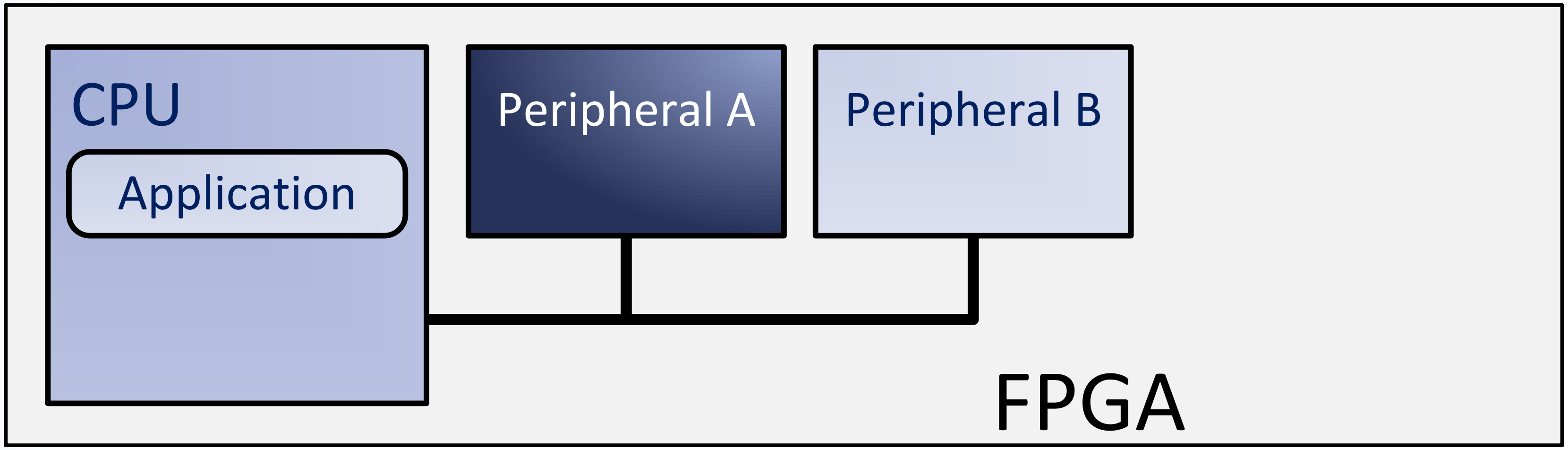

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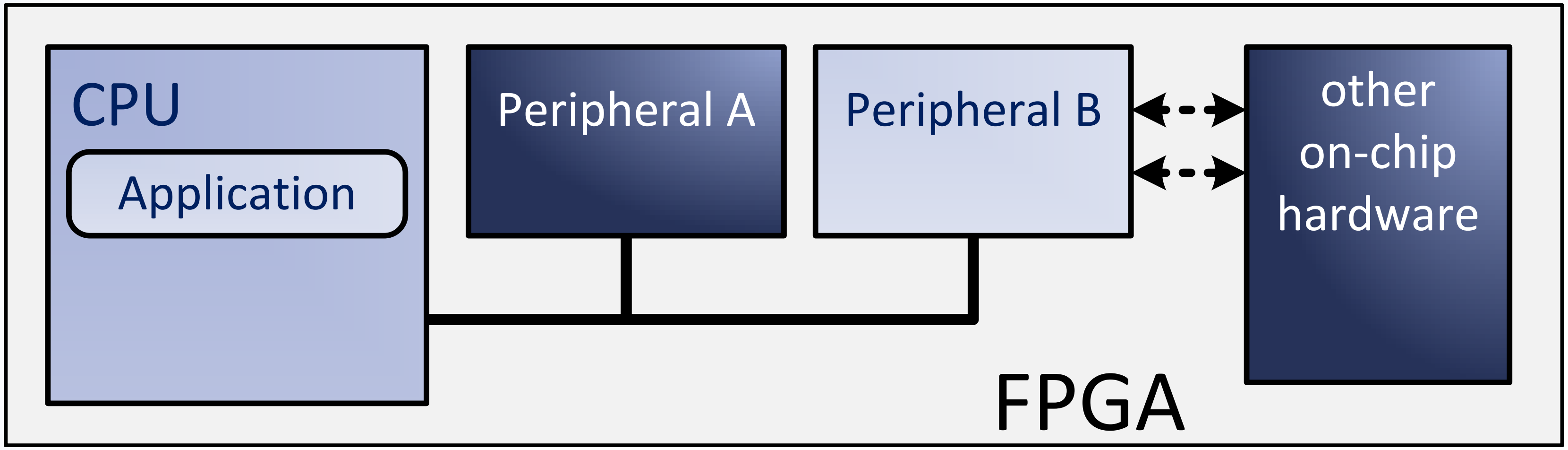

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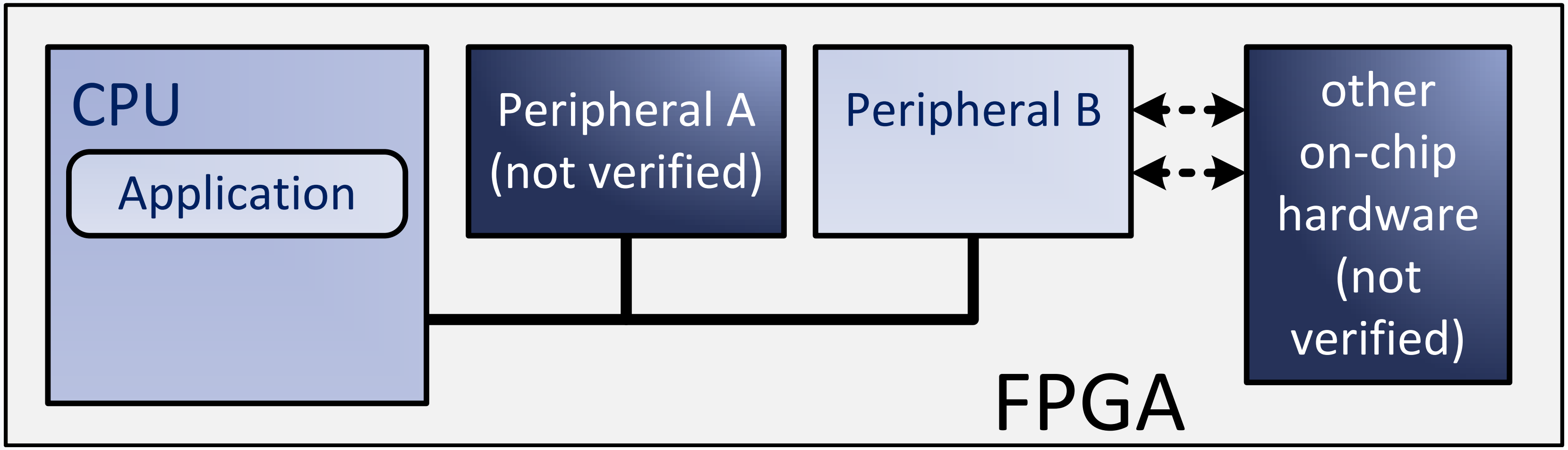

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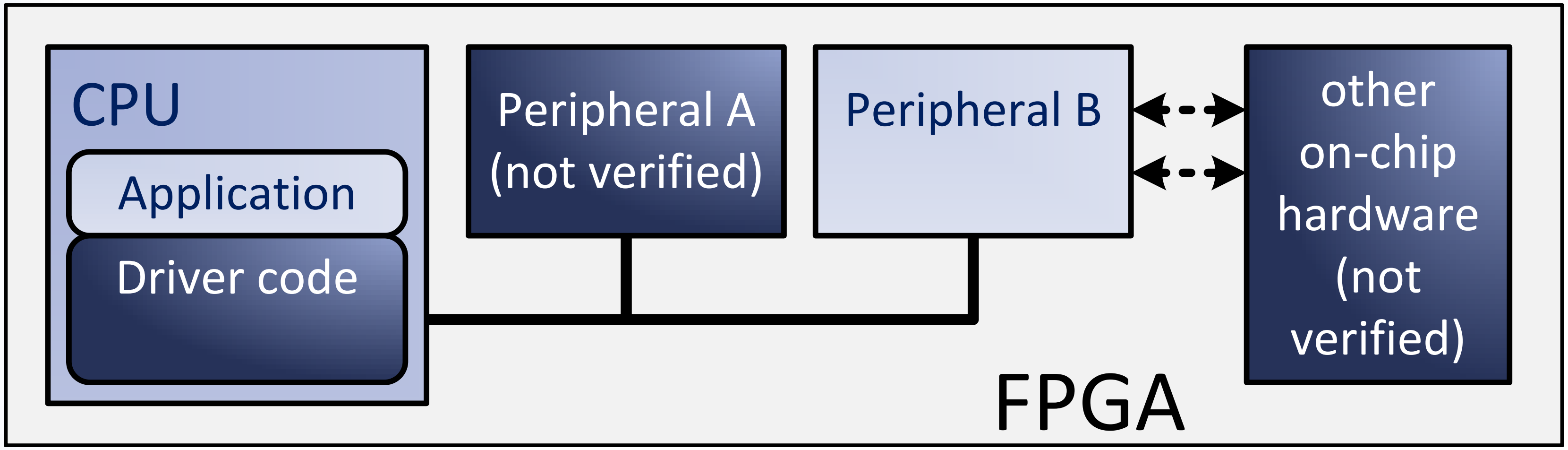
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Driver code
Peripheral A (not verified)
Peripheral B
other on-chip hardware (not verified)
FPGA

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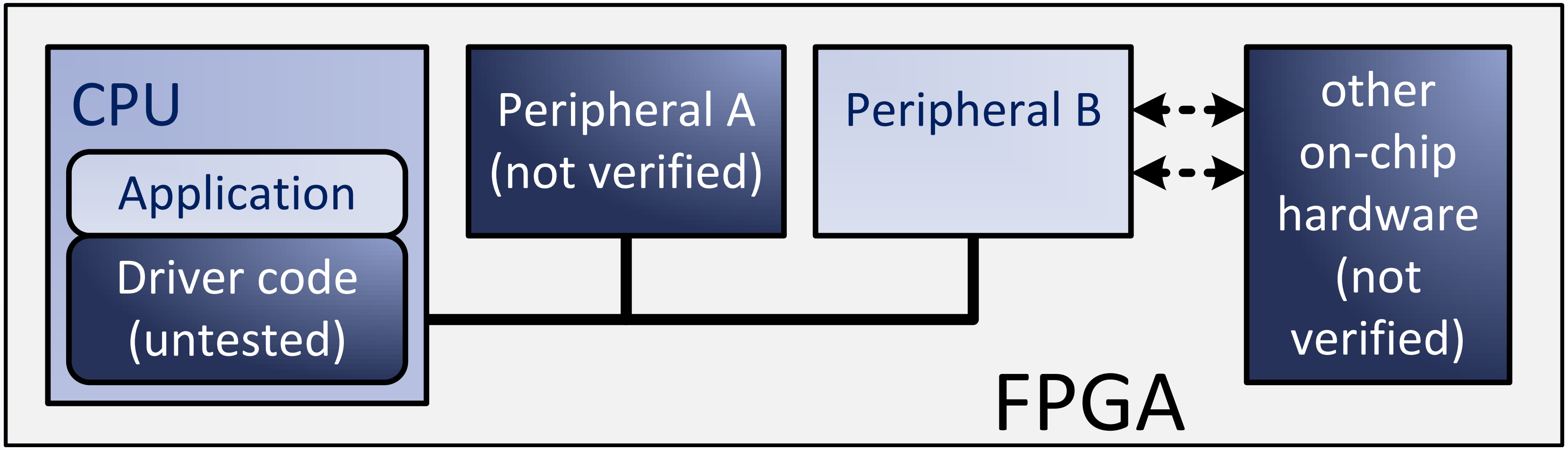

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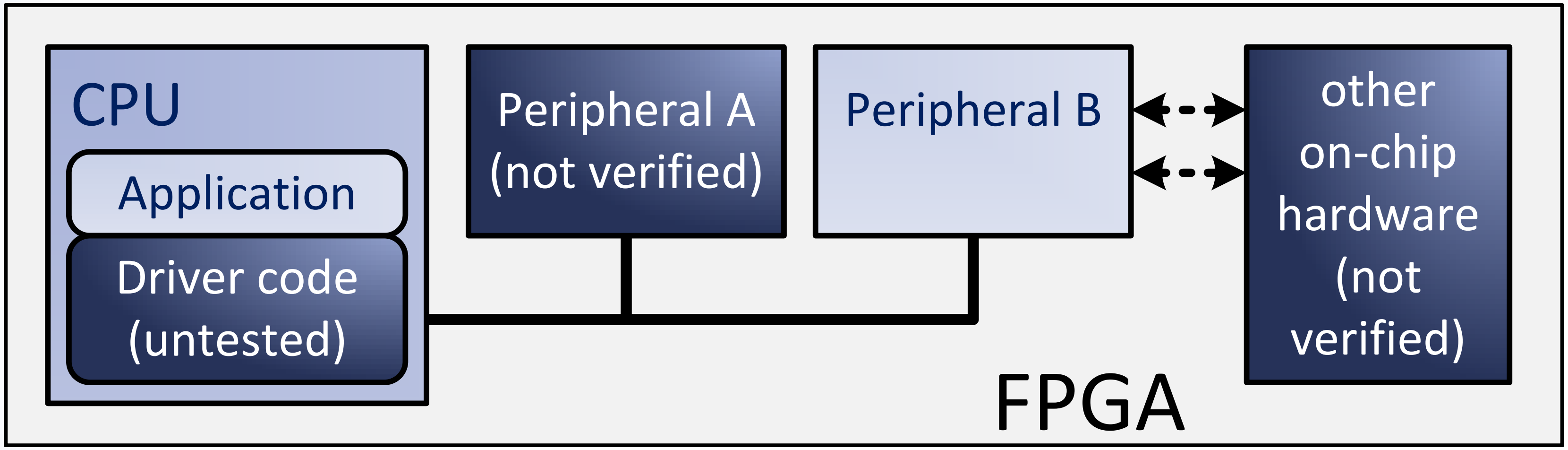
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Optimal: Debug hardware, software and their interaction together

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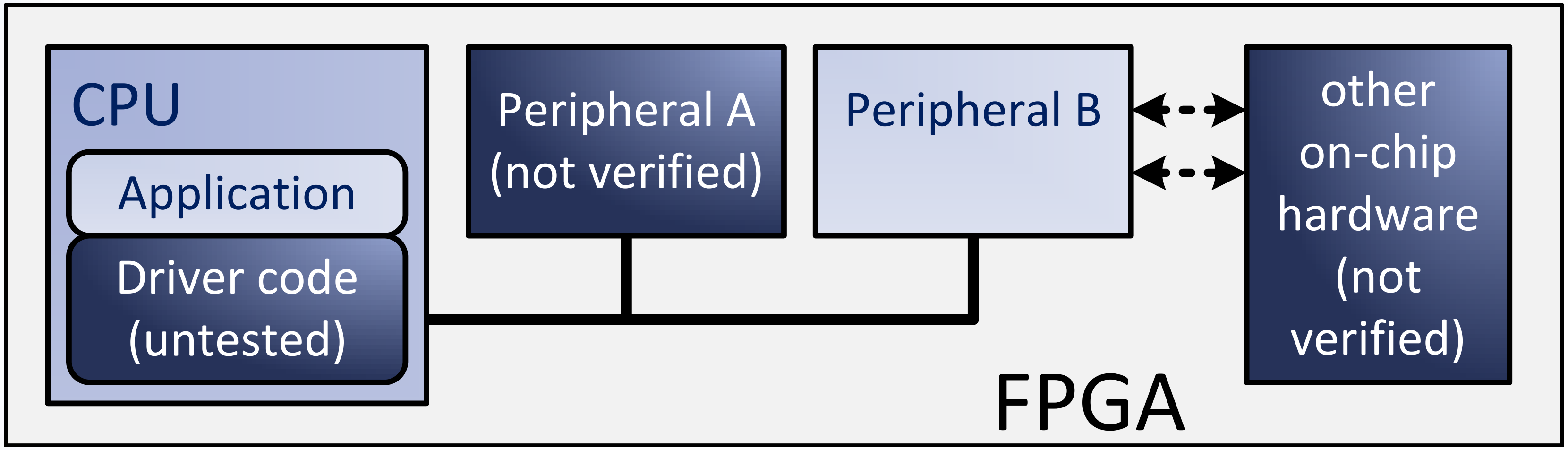
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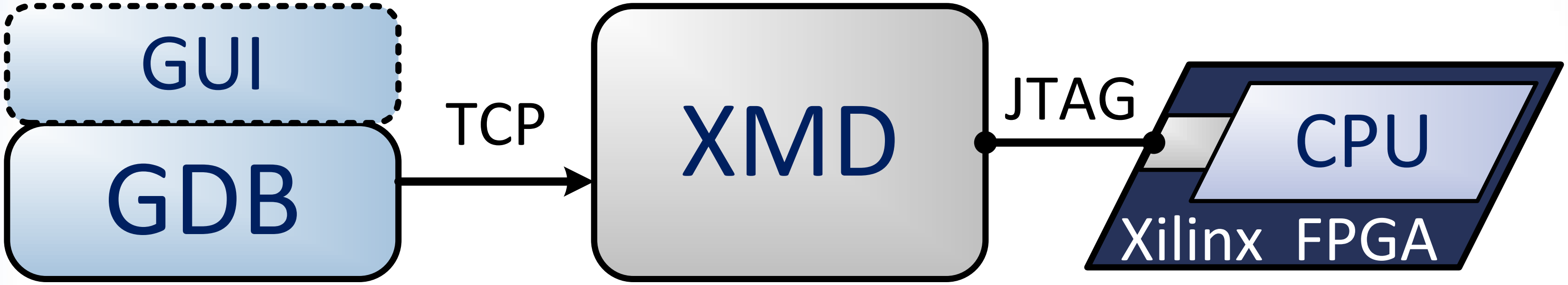
Embedded SW debugging chain



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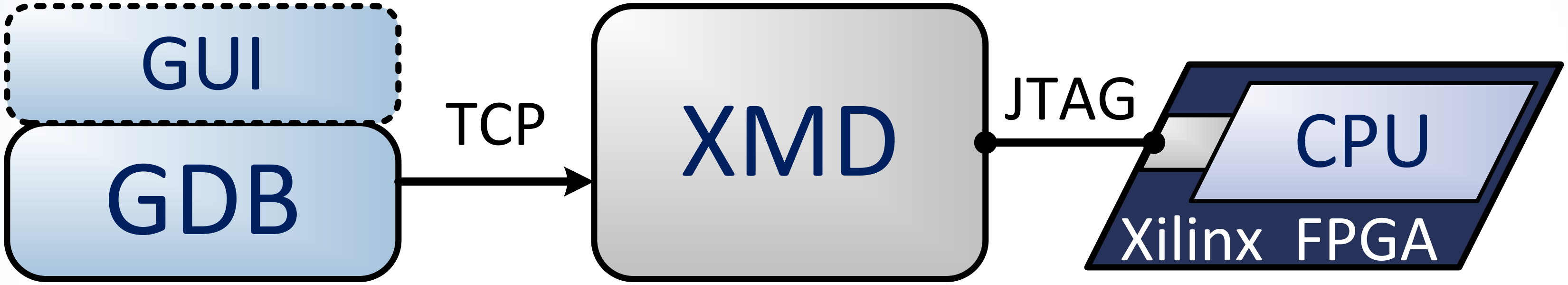
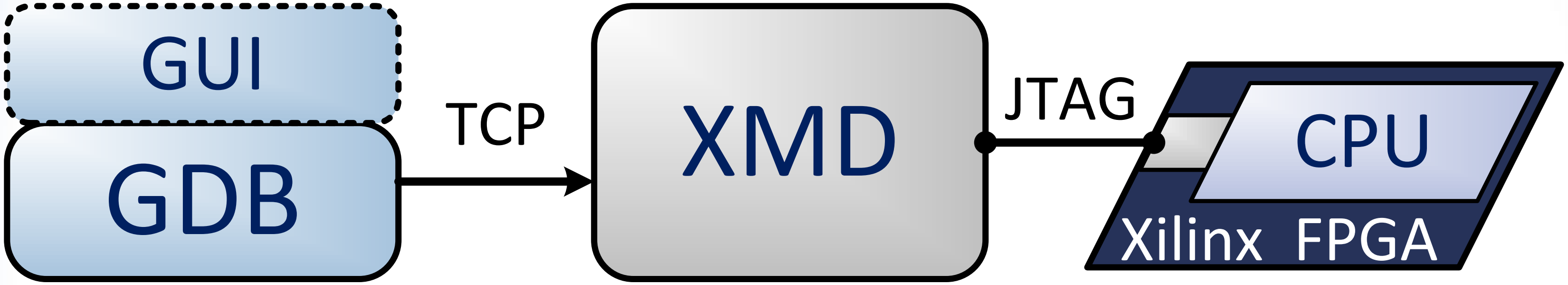


- Debugger on host system

Embedded SW debugging chain



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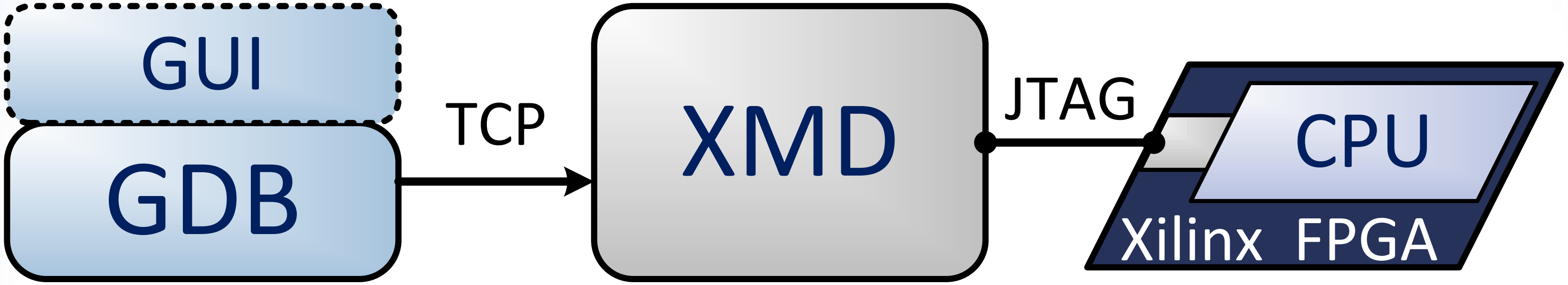
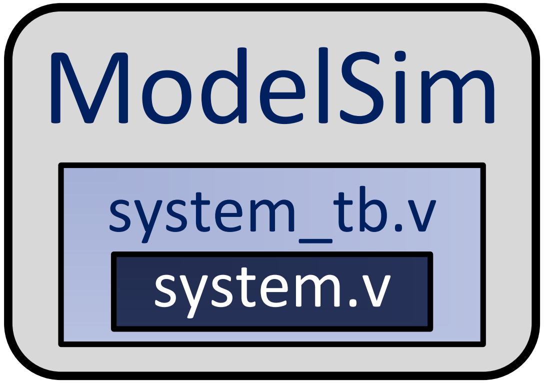


- Debugger on host system
- Vendor-specific interface software
- Software runs on target system

HW debugging



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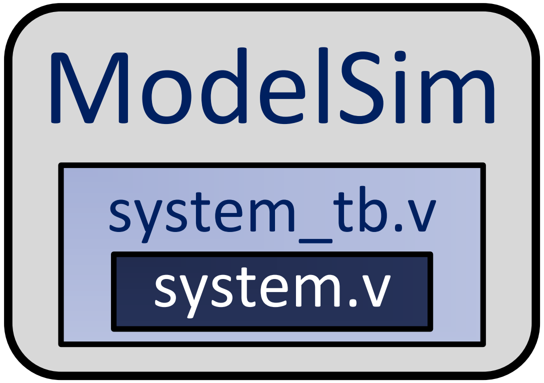
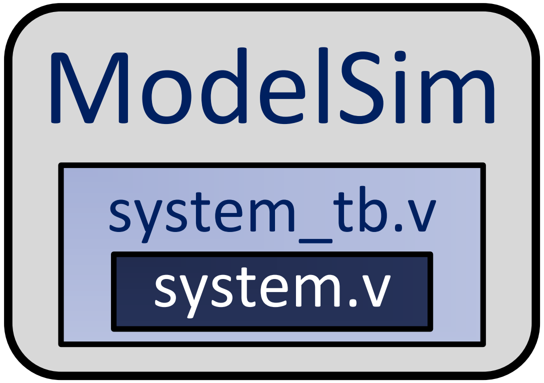


- Cycle-accurate digital simulator

HW debugging

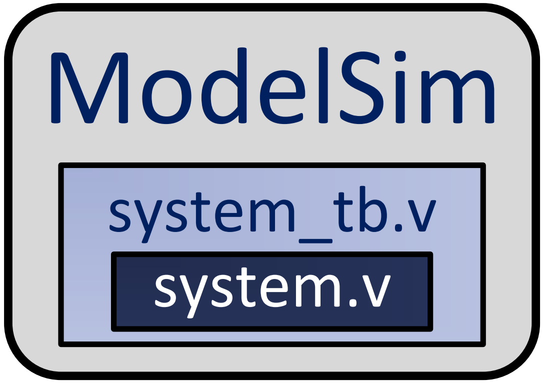

ModelSim

system_tb.v

system.v

- Cycle-accurate digital simulator
- A system model in HDL

HW debugging



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- Testbench instantiates and stimulates model

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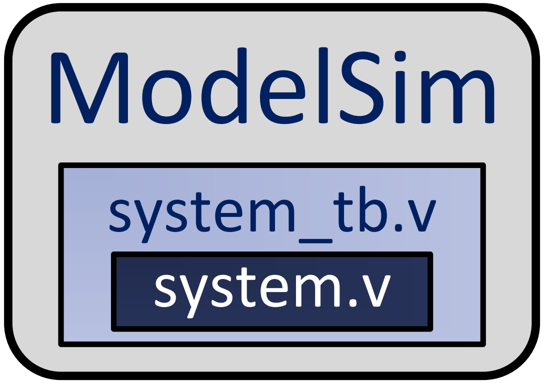
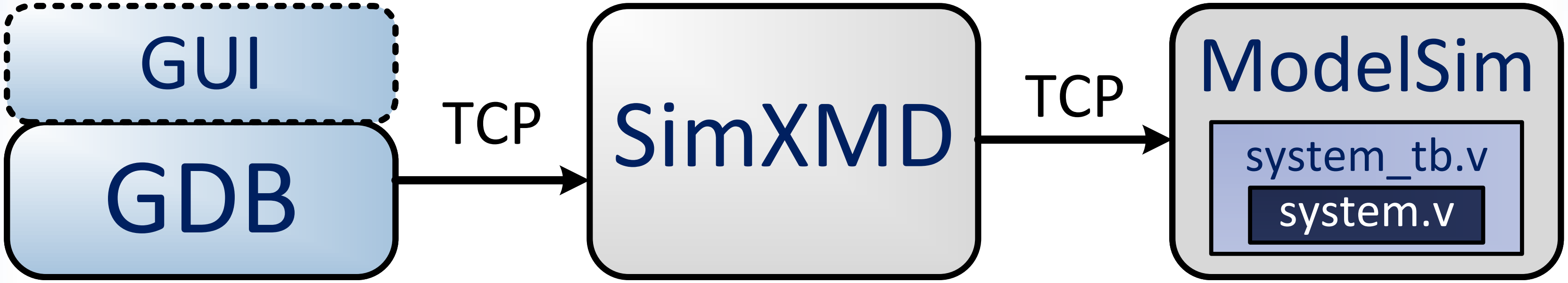


- Cycle-accurate digital simulator
- A system model in HDL
- Testbench instantiates and stimulates model
- All internal signals observable

HW/SW Co-Debugging?

GUI
GDB
ModelSim
system_tb.v
system.v

HW/SW Co-Debugging?



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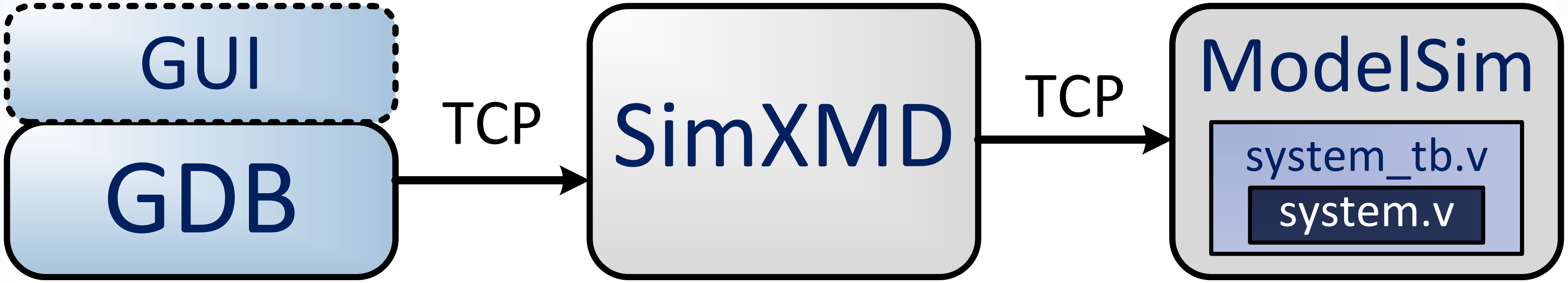
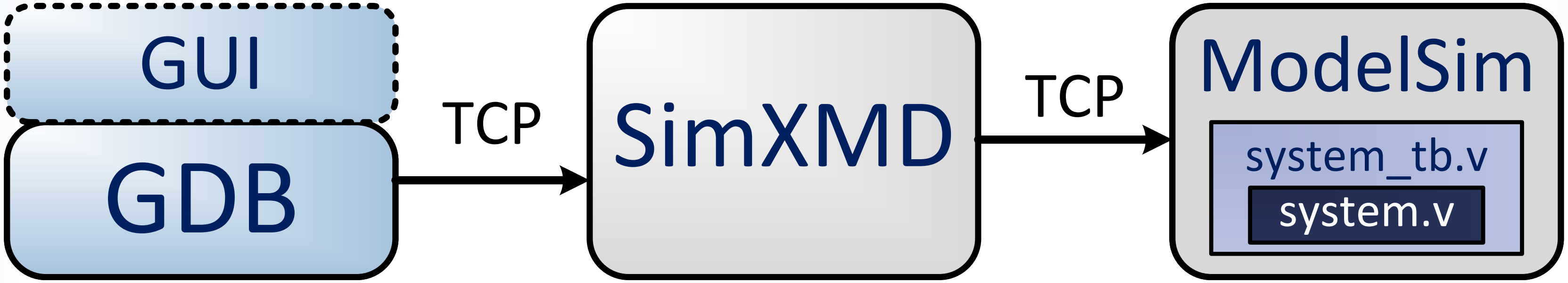


- SimXMD: Simulation-based eXperimental Microprocessor Debugger

HW/SW Co-Debugging?



- SimXMD: Simulation-based eXperimental Microprocessor Debugger
- Translates debugger requests into simulator commands

Key SimXMD enablers

- GDB Remote Serial Protocol
  - Defines requests and replies for:
    - Setting/deleting breakpoints
    - Advancing execution by instruction, line, breakpoint
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  - Reports all information about a finished instruction:
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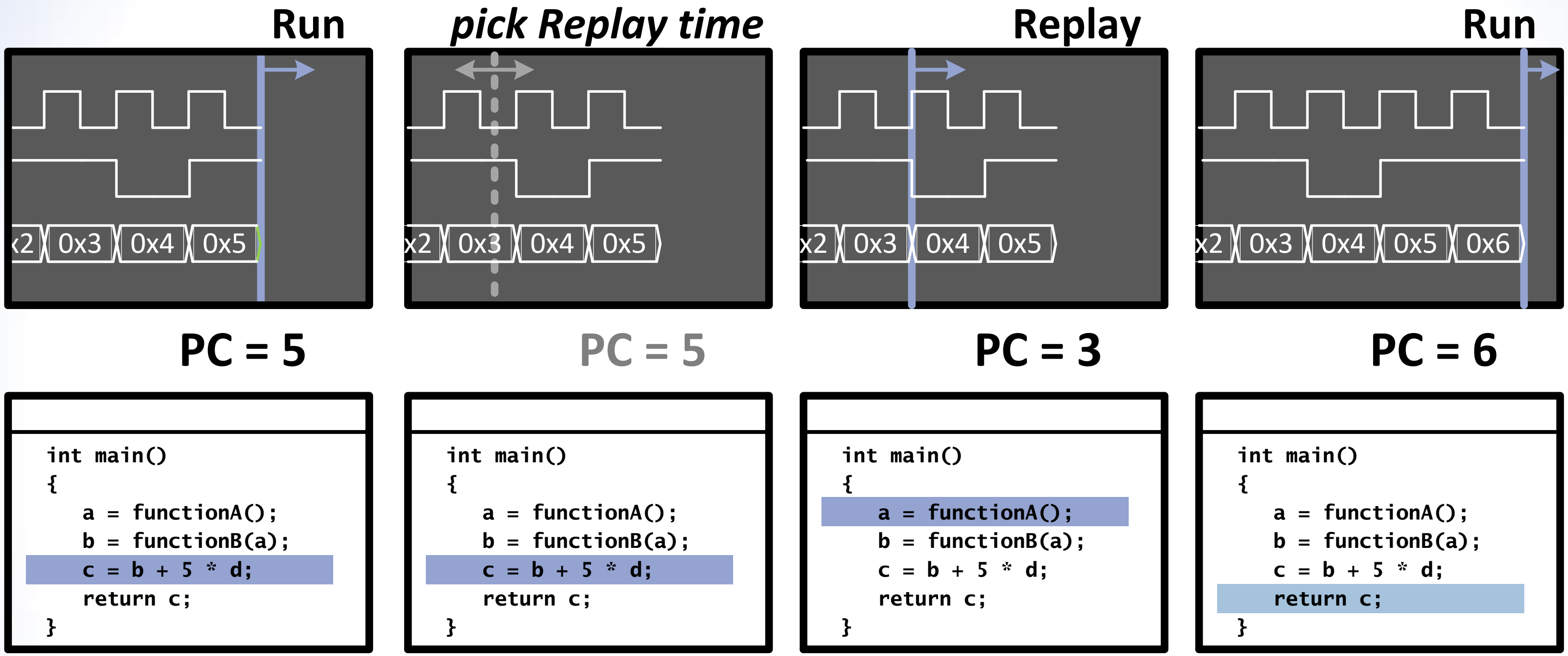
- ModelSim (Tcl) TCP server capability
  - Can receive remote commands and send back results

Operating SimXMD: Preparation

1. Simulation model generation by design tool
   - Currently: Xilinx Platform Studio
2. SimXMD is started (background operation)
   - Examines embedded project information
   - Modifies simulation model for Co-Debugging
3. Compilation of simulation model
4. Start of simulation
5. Start of preferred debugger (GUI)
6. Debugging at will

Operating SimXMD: Modes



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   b = functionB(a);
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- In *Run mode*, debugging drives the simulation
- In *Replay mode*, debugging iterates over previously simulated data

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- Digital hardware simulation models the complete memory hierarchy:
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- Digital hardware simulation models the complete memory hierarchy:
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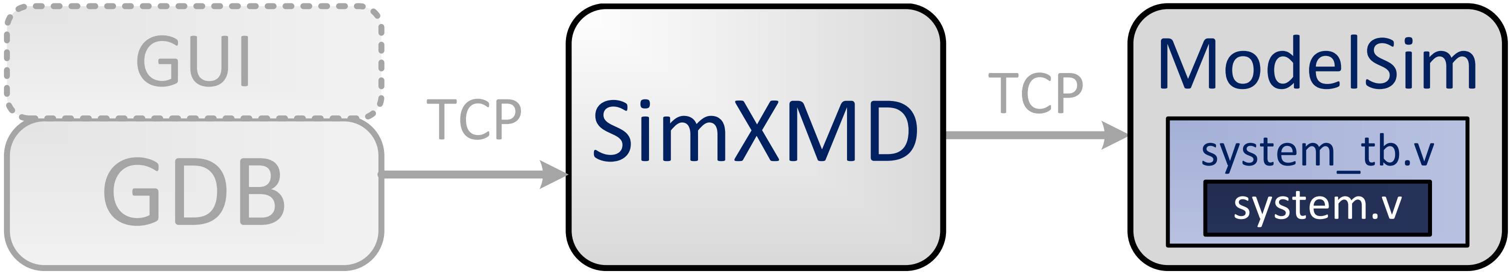
- Software debugging uses a flat, linear memory model:
  - The debugger requests a (virtual) memory address
  - The target hardware determines and reads the physical location

SimXMD memory access logging



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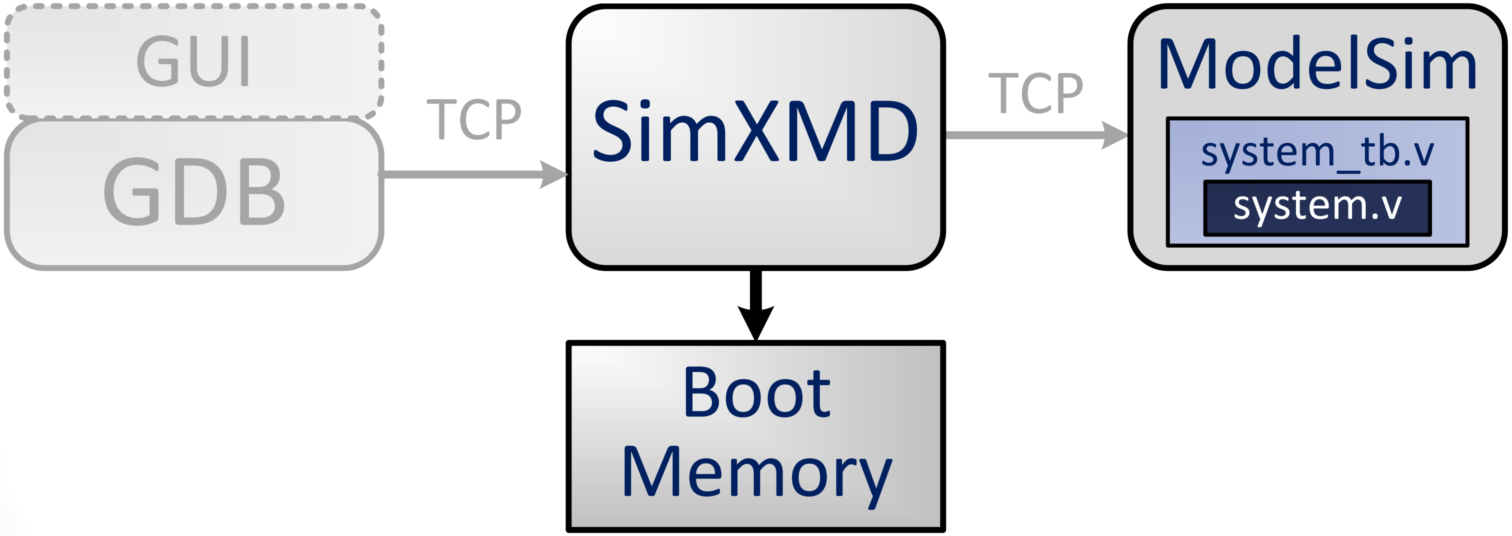

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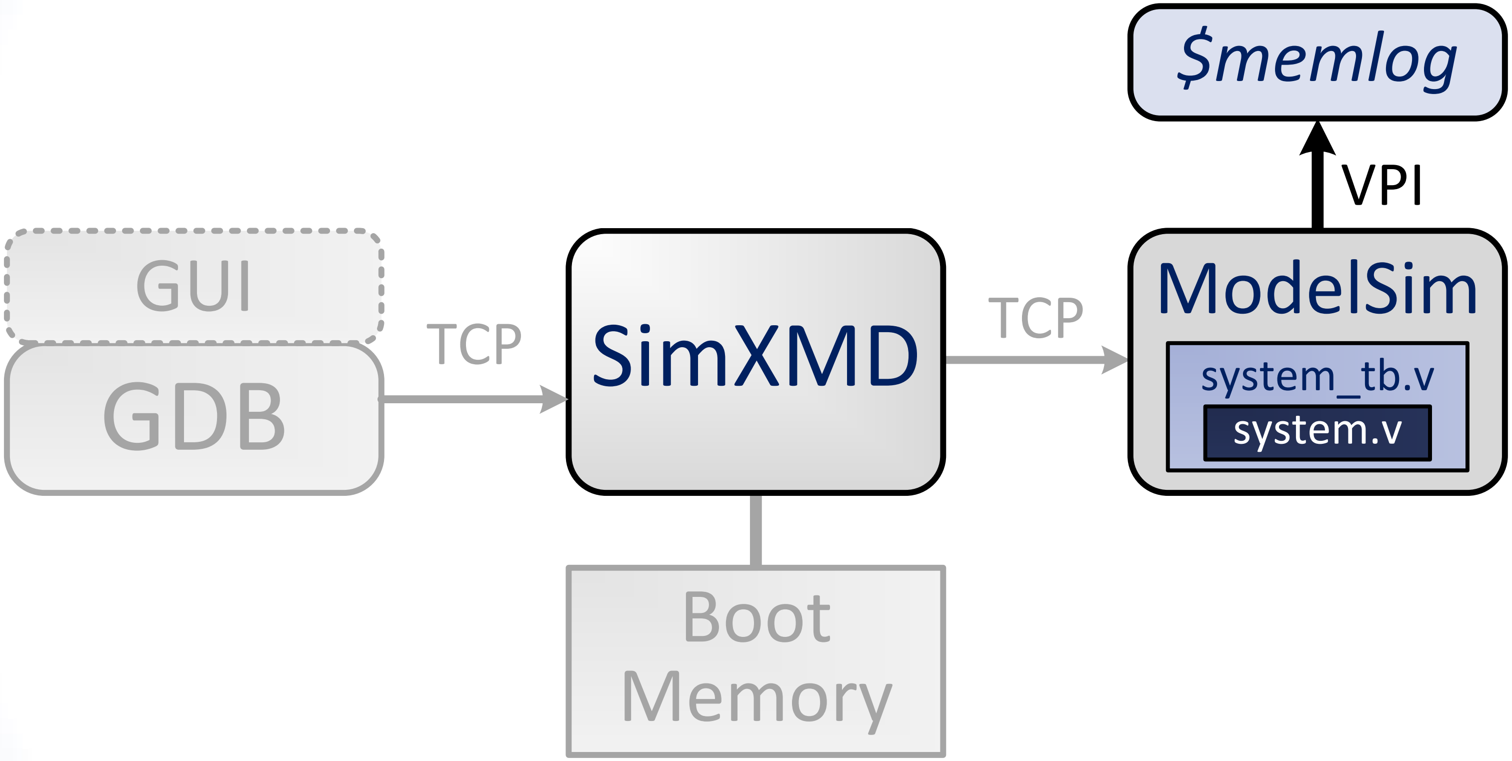

VPI:Verilog Procedural Interface

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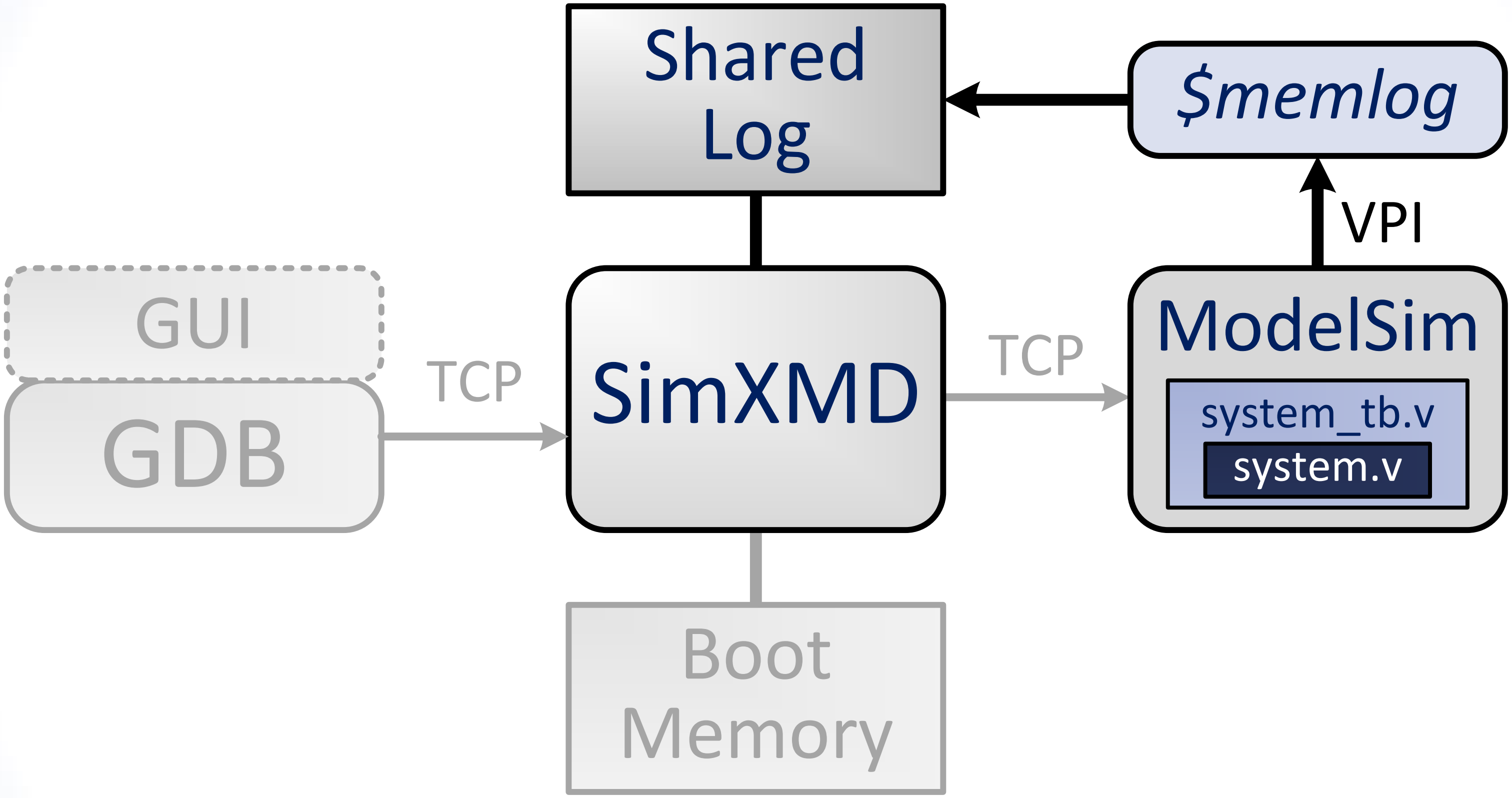

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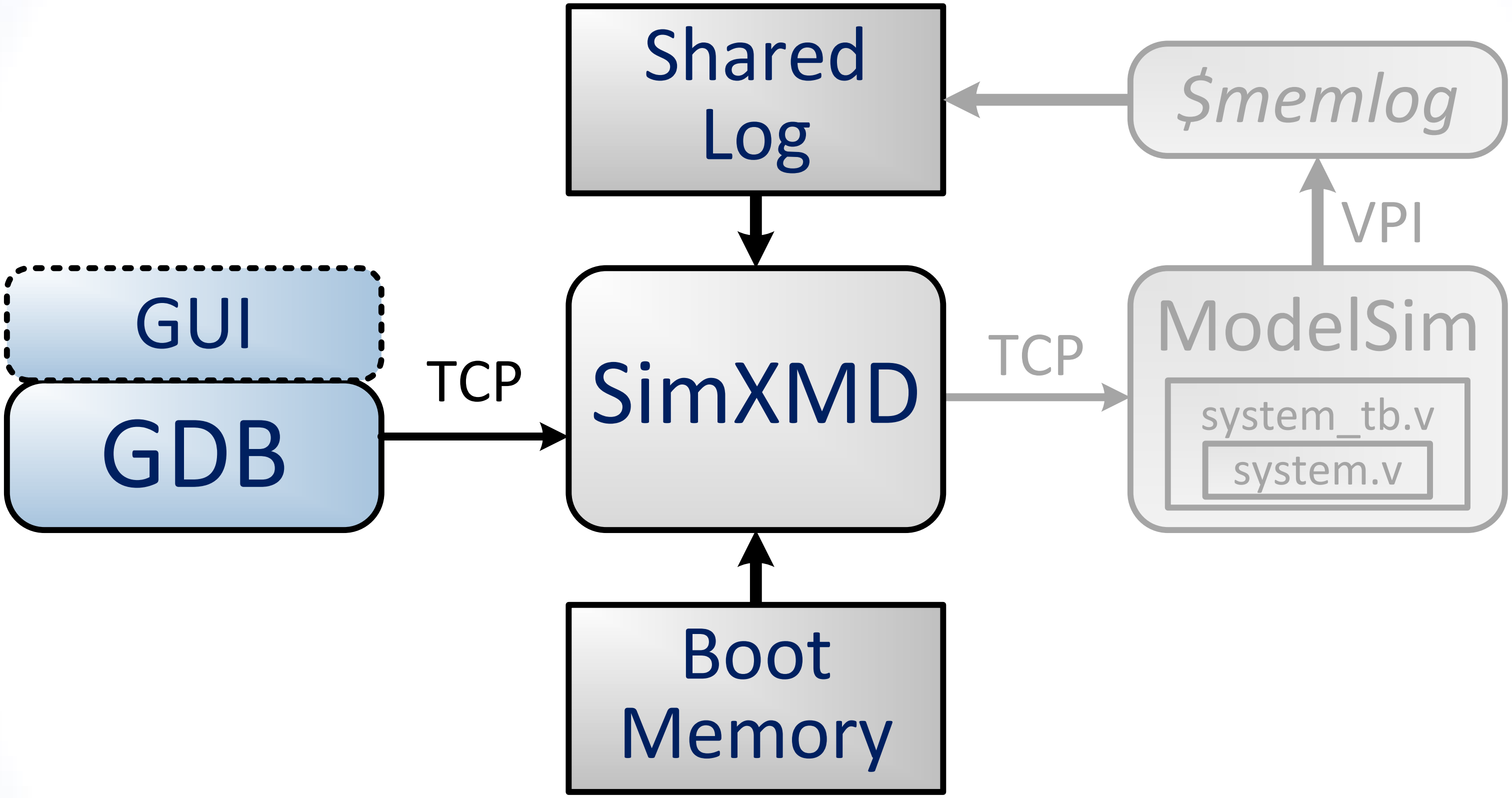
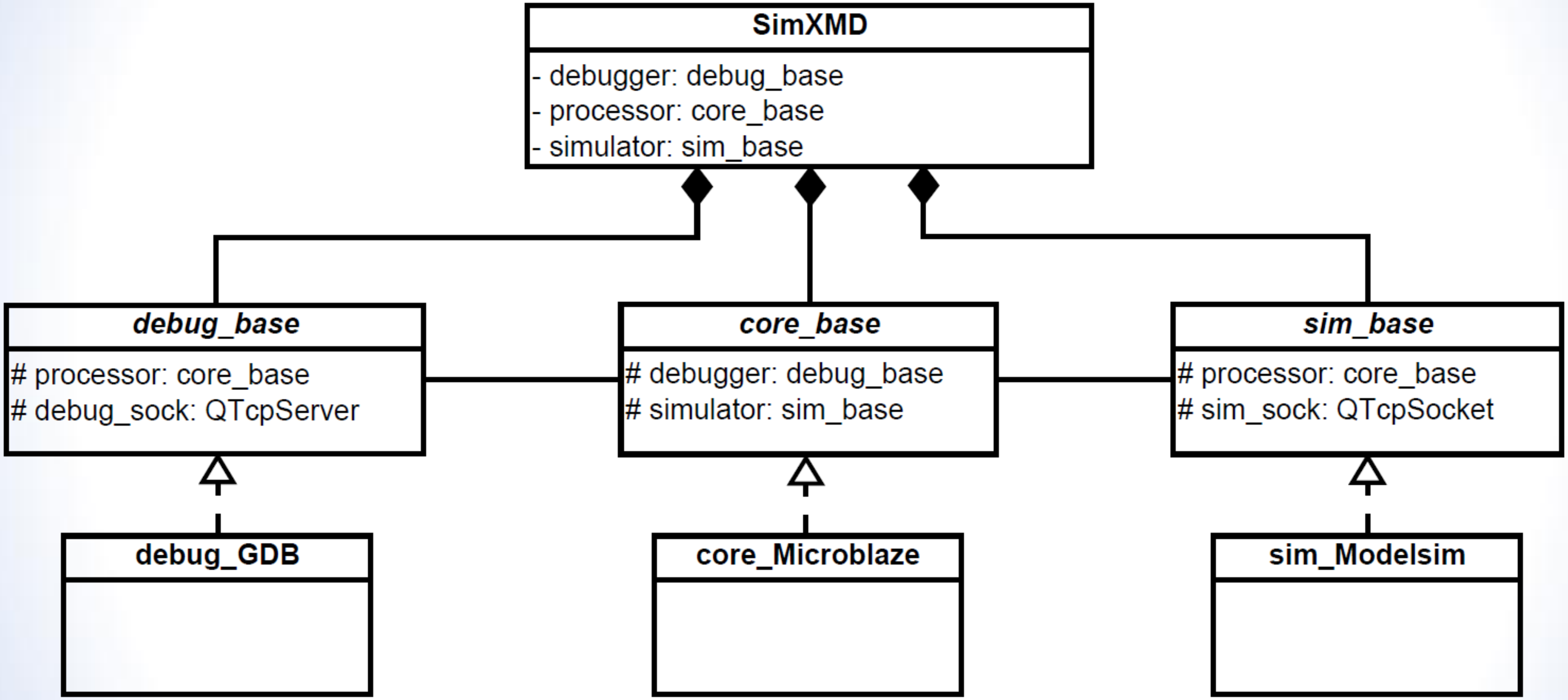


VPI:Verilog Procedural Interface

SimXMD tool support

- Xilinx Embedded Development Kit >= 13.x
  - Xilinx MicroBlaze Processor >= 8.x
- MentorGraphics ModelSim >= 6.6g
- Linux Operating System
- Debuggers
  - Command-line GDB
  - Xilinx SDK (Eclipse)
  - DDD
  - KDbg
  - Nemiver

SimXMD modular architecture



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- Trace Port reports actions after instruction completes; several cycles difference
- Not all MicroBlaze special registers reported
  - Not reported by Trace Port
  - Not used by GDB for anything

SimXMD and multiprocessors?

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- Future work:
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  - Concurrent debugging of several cores
- The same memory volatility issues apply:
  - Logging of virtual memory accesses per processor
    - Different virtual addresses - same physical address?
  - Race conditions likely

SimXMD Performance

- How much do the SimXMD modifications slow down simulation?

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- Test system:
  - Host: Intel i5 Nehalem 4-core, 2.5Ghz, 12GB RAM
  - Target: Xilinx Spartan 6 (Atlys board), JTAG
Microblaze @ 100MHz, 64kB on-chip BRAM
AXI bus, one GPIO peripheral
  - Application: Writing 32kB byte-by-byte into BRAM

SimXMD overhead

Write size	w/o SimXMD	w/ SimXMD
1 kByte	6.9 s	7.3 s
2 kByte	13.8 s	14.5 s
4 kByte	27.3 s	29.0 s
8 kByte	54.9 s	57.7 s
16 kByte	109.0 s	117.1 s
32 kByte	218.9 s	231.7 s

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Average overhead: 6.0%

SimXMD debugging speed

- Same system and application
- Let GDB execute script of 50 “steps” (1 code line)
- Average time for a single code step:

Hardware with JTAG	1.350 s
SimXMD Run mode	0.850 s
SimXMD Replay mode	0.313 s

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  - Hardware debugging "timed" by software sections
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- SimXMD's modular architecture facilitates extension to other processors and tools

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Thank you for your attention!

Questions?