

Integrated Circuits for Digital Communications

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Motivation

- Many exciting new applications for digital comm (previously, modems and satellites)
- xDSL (x=H,A, or V), ethernet, ATM, cable-modems, firewire, disk-drives, wireless, infrared, etc.
- Want to push up bit rate using same channels

Mainly Digital

- Tolerant to large noise and channel variations
- Tolerant to analog IC freq and dc variations
- Easier to design and test

Mainly Analog

- Smaller size and power at high-speeds



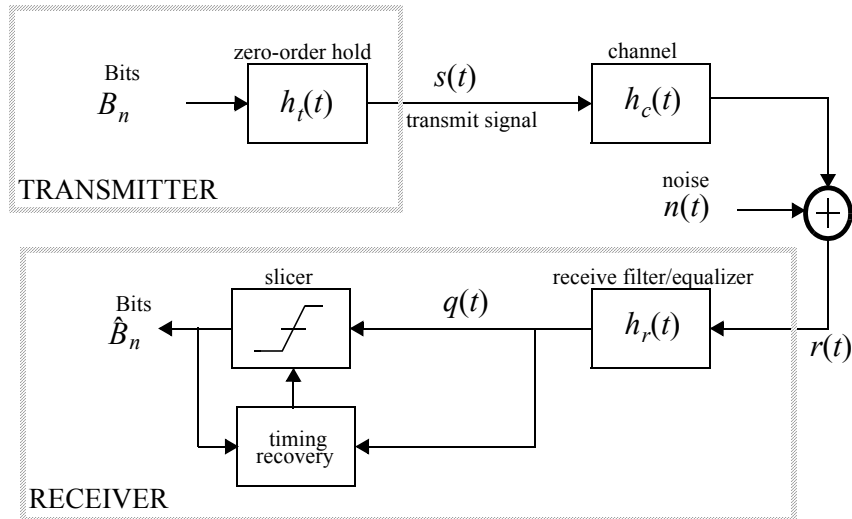
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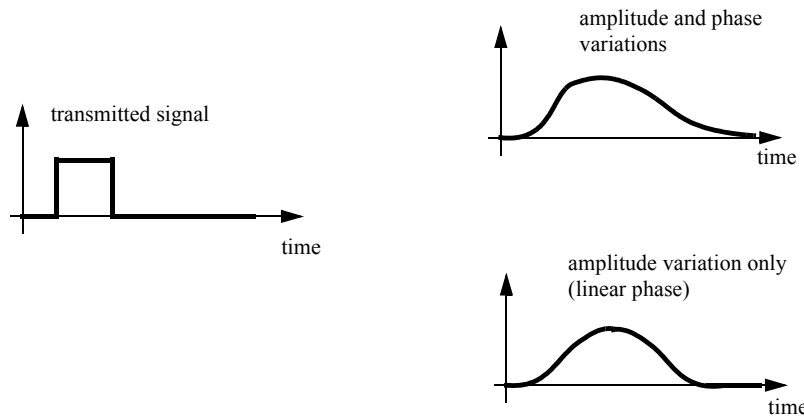
Basic Challenge

- Channel attenuates and phase changes signal, also noise added



Channel Amplitude and Phase Variations

- Amplitude variation (usually lowpass)
- Phase variations (no longer linear phase)



- Linear phase keeps symmetric pulses (intuitively better for less interference)

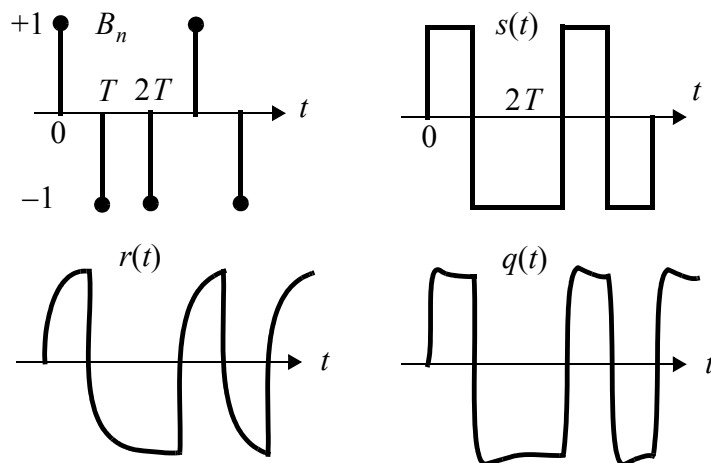


Channel Noise

- Noise and bandwidth limits how much digital information can be sent through channel
- Usually model noise as being added after channel impairment
- Can use filtered noise if not white
- Usually assume Gaussian noise because of central limit theorem and mathematically tractable
- Note that receive equalizer might *increase* noise if it has boost (noise enhancement)



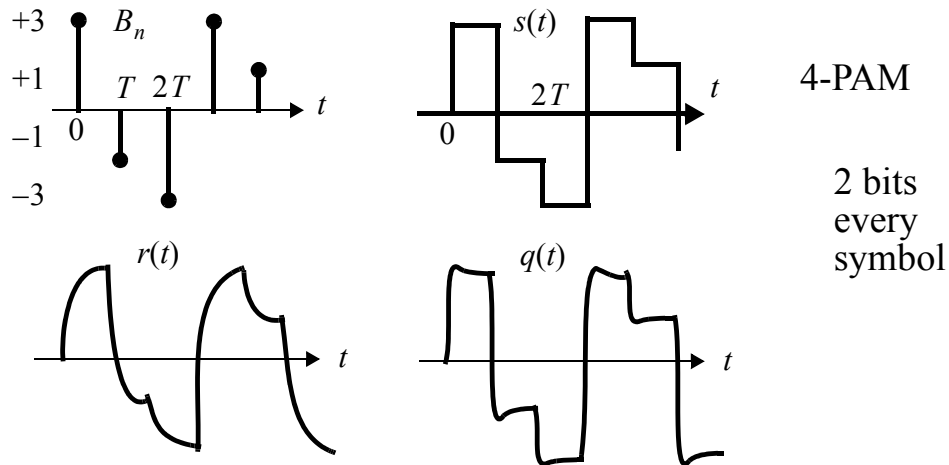
Low Noise - Large Bandwidth



- Not pushing maximum bits through channel
- Low noise — can use more levels for each symbol
- Large bandwidth — can increase symbol-rate



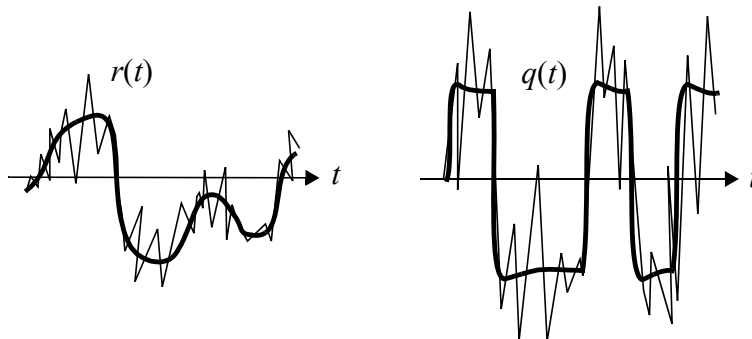
Multi-Level — Low-Noise, Large Bandwidth



- Twice the bit information over same bandwidth!
- More prone to noise causing errors
- Commonly called PAM (here 2B1Q — 4-PAM)



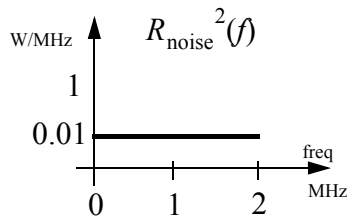
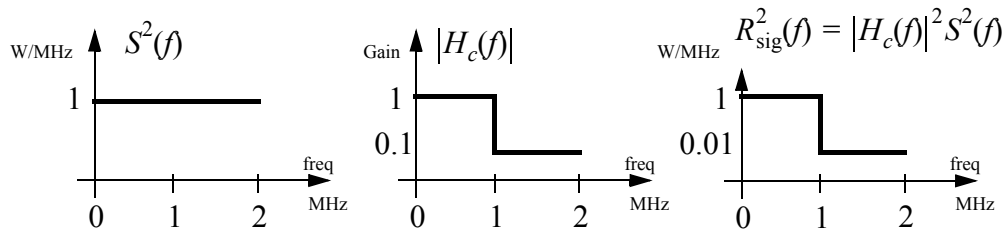
High Noise - Low Bandwidth



- Equalizing back to “square-wave” amplifies noise
- Particularly bad if most noise is at high frequencies
- Too many errors — need to equalize without much noise enhancement (or add coding)
- More errors with multi-level PAM (unless coded)



Noise Enhancement Example



Before Equalization

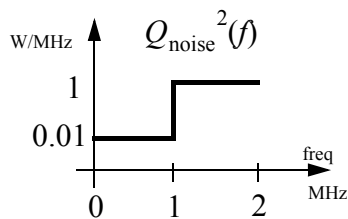
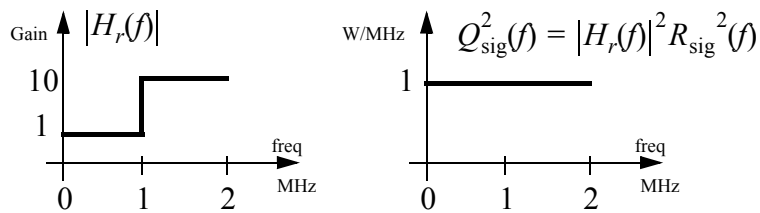
Signal power = 1.01 W

Noise power = 0.02 W

$$SNR = 10\log\left(\frac{1.01}{0.02}\right) = 17 \text{ dB}$$



Noise Enhancement Example



After Equalization

Signal power = 2 W

Noise power = 1.01 W

$$SNR = 10\log\left(\frac{2}{1.01}\right) = 3 \text{ dB}$$



ECE1392 Coverage

- High speed circuits for 1Gb/s (and up)
 - PLL, VCO, impedance, phase-detector, freq detectors, etc.
- Circuits and architectures for 1Mb/s - 1Gb/s
 - xDSL, ethernet, disk-drives, etc.
- Adaptive filter overview (both analog and digital)
- This course will cover circuits and systems for digital communications.
- **Suggested Prerequisites:**
 - ECE530 Analog Circuits
 - ECE417 Digital Communications



ECE1392 Grading

- Grading:
 - **Project** 50% due Nov 20, 2001
 - Transistor level project for high-speed DLL and low jitter multiplexor
 - Exam: 50% Dec. 4, 2001
(SINGLE 8.5" x 11" AID SHEET ALLOWED)

