

Analog Adaptive Filtering Techniques for High-Speed Data Communications

by

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Abstract

An area receiving significant attention both from academia and industry is data communications. Great effort is being placed at pushing data transmission rates over copper to near the Shannon limit which requires support electronics such as filters operating in the VHF range. Thus, tuning mechanisms are essential to accommodate fabrication and channel variations. One technology to accommodate these variations is that of analog adaptive filtering and is the main topic of this thesis. Specifically, this thesis is an investigation to determine and demonstrate the capability of analog adaptive filtering in practical high-speed applications. The issues that are addressed are the implementation of the tuning algorithm, simple and effective building blocks and the effects of DC offset.

Herein, a curve fitting approach is proposed for the adaptation algorithm and focus is placed on simple algorithms and simple filter building blocks that can accommodate a wide tuning range and high speed. Experimental results of a 100Mb/s transmit pulse-shaping filter verify the proposed adaptive techniques and highlight practical problems. This prototype is the first demonstration of an analog adaptive filter operating in the VHF range. Attaining a maximum processing frequency of 230MHz, it is also one of the fastest integrated filters reported in the technical literature. DC offset, being a major hindrance to optimal performance, is considered and its effect on four different possible variations of the basic

adaptive algorithm is investigated. As a result, one is able to choose the best implementation for a specific application and technology.

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Glossary of Terms

$\Sigma\Delta$	sigma-delta.
ADC	analog-to-digital convertor.
AGC	automatic gain control.
ASIC	application specific integrated circuit.
ATM	asynchronous transfer mode.
AWGN	additive white Gaussian noise.
BER	bit error rate.
BiCMOS	Bipolar CMOS.
biquad	biquadratic filter.
BJT	Bipolar Junction Transistor.
BW	bandwidth.
CDDI	copper distributed data interface.
CMFB	common-mode feedback.
CMOS	Complimentary Metal Oxide Semiconductor.
CMRR	common-mode rejection ratio.
CP_1	1 dB compression point.
$C_{SH_{AWGN}}$	Shannon AWGN bound for infinite BW signalling.
$_{SH_{AWGN}}(F_{eff})$	Shannon AWGN bound for signalling whose maximum frequency is F_{eff} .
$C_{SH_{NEXT}}$	Shannon NEXT bound for infinite BW signalling.
$C_{SH_{NEXT}}(F_{eff})$	Shannon NEXT bound for signalling whose maximum frequency is F_{eff} .
DAC	digital-to-analog convertor.
DFE	decision feedback equalizer.

DSP	digital signal processor.
EMI	electro-magnetic interference.
EPROM	erasable programmable read-only memory.
FCC	Federal Communications Commission.
FDDI	fiber distributed data interface.
FE	feedback equalizer (in feedback path of a DFE.)
FEXT	far-end crosstalk.
FFE	feed-forward equalizer (in forward path of a DFE.)
FIR	finite impulse response.
FSK	frequency-shift keying.
G_m -C	transconductance-C.
HDSL	high bit-rate digital subscriber line.
HD_i	i^{th} harmonic distortion.
\overline{HD}_i	i^{th} harmonic distortion component.
HFHQ	high frequency high Q .
HFLQ	high frequency low Q .
HL	high-to-low transition of data pulse.
ISDN	integrated services digital network.
ISI	inter-symbol interference.
IIR	infinite impulse response.
IM	intermodulation.
IM_i	i^{th} -order intermodulation distortion.
\overline{IM}_i	i^{th} -order intermodulation distortion component.
IP_3	third-order intercept point.
LAN	local area network.
LFHQ	low frequency high Q .
LFLQ	low frequency low Q .

LH	low-to-high transition of data pulse.
LMS	least mean square.
MLT-3	multi-level signalling (3-level).
NEXT	near-end crosstalk.
NRZ	non-return to zero.
NRZI	non-return to zero invert.
O/A	operational amplifier.
PAM	pulse amplitude modulation.
PCS	portable communication services.
PDR	peak dynamic range (also peak $\frac{S}{N+D}$.)
PLL	phase-lock loop.
PR4	partial response Class IV.
PSK	phase-shift keying.
PSRR	power-supply rejection ratio.
PW50	pulse-width 50% (pulse width at half amplitude).
QAM	quadrature amplitude modulation.
QSNR	quantizer signal to noise ratio.
RMS	root mean square.
SC	switched-capacitor.
SD-LMS	sign-data LMS.
SDR	signal to distortion ratio.
SE-LMS	sign-error LMS.
SFDR	spurious free dynamic range.
SIDR	signal to interference power spectral density ratio.
SIR	signal to interference ratio.
SNR	signal to noise ratio.
SNXR	signal to near-end crosstalk ratio.

SS-LMS	sign-sign LMS.
STP	shielded twisted-pair.
UTP	unshielded twisted-pair.
VHF	very-high frequency (30-300MHz).

CHAPTER 1

Motivation and State of the Art

Filters are among the most important signal processing blocks in any circuit network. These blocks function as transmitter pulse-shaping filters, receiver equalizers, echo cancellers, anti-aliasing filters, modulators, decimation filters, and others. The preferred technology for implementation is typically digital due to the high accuracy attainable. However, filters implemented in this technology tend to consume significant power and achieve processing speeds below those attainable using analog implementations. Thus, for low-cost, high-speed applications (>100MHz) designers tend to favor analog filters. However, these filters suffer from process variations, operating temperature, and parasitic effects; hence, tuning is essential.

Traditionally, the master/slave scheme has been successfully employed in tuning analog filters with bandwidths below 10MHz as will be noted from section 1.3. However, at higher frequencies second-order effects become more significant and this tuning scheme becomes less effective. In addition, at higher frequencies channel variations must also be accommodated which cannot be achieved using the master/slave technique. To account for channel variations, filter programmable arrays have been proposed. Thus, a given filter response among a quantized set of filter responses can be selected by a digital signal

processing (DSP) board which addresses the different responses through a serial interface. This approach requires significant area overhead and knowledge of channel variation characteristics.

Another alternative is to make use of adaptive techniques to tune against process as well as channel variations. In theory, much better accuracy (relative to other tuning schemes) can be obtained since the filter output response is constantly being optimized during service by minimizing the response error signal. The error signal is obtained by taking the difference between the filter output signal and a desired output. There has been some theoretical and experimental work done in this area [Brown 93], [Kozma 91], [Johns 91], [Cornett 90], [Voorman 82], [Fichtel 92] and [Kwan 91]. However, these works illustrate the concept and accommodate very low frequencies — a frequency range where analog techniques are typically not employed. This thesis investigates the practicality of analog adaptive filters for use in high-speed applications with focus on effective, yet simple adaptation techniques.

Unlike digital adaptive filter technology, which is now commercially mature, analog adaptive filter technology is still mostly at the experimental stage. However, an analog approach offers higher signal processing speeds, lower power dissipation, and smaller integrated circuit area. These advantages therefore warrant research work into analog adaptive filters. Progress in practical, efficient, yet simple algorithms for adapting high-frequency filters is required. Specifically, taking the difference of the filter output signal from a desired signal to obtain an error signal becomes more difficult at higher frequencies. In addition, a desired signal in most applications does not exist at all times. Hence, an alternative approach by making sample measurements on the filtered output at certain time instants and comparing with a reference template to obtain an error signal is sought. In addition, another technique that computes an error signal for each parameter tuned is also investigated for filters with two adaptive parameters. In other words, given a set of unknown filter parameters, we obtain a set

of sample measurements to provide the information to solve for these parameters. This new idea is investigated for adaptive pulse-shaping filters and adaptive equalization.

One of the mechanisms that degrades the performance of the adaptation algorithm is DC offsets. Thus, it is important to study the effects of DC offsets on four different possible realizations of the LMS algorithm so that the best performing algorithm in the presence of offsets, as well as other issues, can be chosen, and then, a proper compensation scheme be devised. To date, this study has not been pursued in the technical literature, and hence, will be dealt with in this dissertation. More about DC offsets and state-of-the-art compensation techniques will be discussed in section 2.3.2.

Finally, filter building blocks to support the technology by achieving high speed and providing a wide tuning range will be proposed.

The application area to benefit from this work is high-speed data communications. More specifically, we investigate analog pulse-shaping filters and equalizers to accommodate twisted-pair copper channels. While undoubtedly the transmission medium of the future is fiber, this copper channel will dominate short-hop links and will remain the channel of choice for at least the next ten years. Since state-of-the-art data transmission over copper is well below the theoretical limit, we believe that analog adaptive filters can not only accommodate present day proposals, but also help push low-cost, short-hop copper channels to near their theoretical capacities. It is hoped that the techniques discussed here will form a starting point for further research work into methods that will allow this push. It should be mentioned that the focus here is on data transmission over twisted-pair cables, however, the described adaptation techniques are also applicable to other copper channels such as the large installed coax base for video signal transport. In addition, the circuits described here achieve a dynamic range of 35dB. Based on the work in Chapter 2, this figure is sufficient for the half-duplex NRZ data transmission scheme chosen here, however, it is not sufficient for multi-level

signalling schemes or full-duplex transmission. For example, in Chapter 2 it will be noted that as the number of signalling levels increases so must the minimum signal to noise ratio to allow reliable detection. For full-duplex transmission, such as high bit-rate digital subscriber line (HDSL) which uses 2-4 wire hybrids, higher dynamic range would be required to detect the low level received signal buried in the high level transmit crosstalk.

In this chapter, a brief discussion on the reason why analog techniques are preferred at high speeds ($> 100\text{MHz}$) is given and alternative tuning schemes are reviewed. The state-of-the-art in continuous-time and adaptive filters is then presented. Next, the evolution in data communications is briefly reviewed to identify the major competing transmission media as well as to highlight the contributions that supported this evolution. Finally, reasons will be given as to why the copper channel will remain in service for at least the next ten years and will dominate short-hop links. These issues combined, form the basic motivation for analog adaptive filters for data transmission over copper.

1.1 Filtering Technology Choice

While it is apparent that this work focuses on continuous-time filters, it is informative to consider other technologies for implementation and provide arguments as to why this technology was preferred. The two other technologies: switched-capacitor (SC) and digital will be discussed.

The SC filter was originally proposed by Fried in 1972 [Fried 72] and today it is a mature technology that has proliferated in the telecom industry — most notably for its low power requirements and high accuracy. However, this technology's signal processing speed is limited to about 10MHz in today's silicon technology. The reason for this limitation comes from the fact that a SC filter is composed of sampled active integrators whose sampling rate, f_s , should be at most 1/5 the unity gain frequency of the op-amp which is about 1/10 the

transition frequency, f_t , of the process. To comply with Nyquist's sampling criterion, the maximum signal bandwidth that can be processed is then $\frac{f_s}{2}$. Finally, if a filter is to achieve a stopband performance for at least one decade above the maximum signal bandwidth before foldover, then a 1MHz filter passband bandwidth, f_o , in a 1GHz process should theoretically be attainable. Clearly, if the objective is to process signals in the 100MHz range, SC implementations are to be ruled out.

With the scaling down of device feature size and reduced supply voltages, non-ideal effects of analog building blocks become more prevalent and system performance degrades. Thus, robust high resolution digital realizations are preferred, albeit at increased integrated circuit area and increased power dissipation. Digital filters can be implemented using either a DSP or dedicated hardware when speed is critical. The maximum processing speed of a digital filter is limited to the reciprocal of the time latency of a multiplier accumulator operation for a given wordlength. In today's CMOS technology a 32b by 32b adder requires 3ns (24b adders require 1.5ns), while a 16b by 16b multiplier takes 4ns [Hwang 89], [Kernhof 89], [Yuan 91]. A throughput of 200MHz was recently achieved for a 12b x 12b multiplier and 27b accumulator operation in a 1 μ m CMOS process [Lu 93], while digital filters capable of clock rates in the 200MHz range have been reported in [Lin 90] and [Khoo 93]. With bipolar devices these processing speeds can be increased. Hence, digital filters can achieve relatively high processing speeds. However, since signals are analog in nature, digital filters require analog-to-digital converters (ADCs) which then put another limitation on attainable processing speed. At present, the fastest ADCs are flash converters whose average maximum sampling rate is about $\frac{f_t}{30}$ with accuracy no better than 8 bits. For a 10GHz process, a sampling rate of 330Msamples/s can be achieved, but constrains data transmission well below the Shannon bound on channel capacity. Furthermore, 8 bits (50dB) is not that much higher than the dynamic range an analog counterpart filter can achieve with significantly lower power dissipation and reduced IC area and system cost.

We are therefore obliged to implement our filters in the analog domain, if we wish to enhance data transmission performance at modest cost. Here, too, several architectures are available, but it is apparent from the technical literature [Culbert 88], [Nauta 92], [Veirman 92], [Lee 93], [Laber 93] that a transconductance-capacitor (G_m - C) architecture is the preferred choice at the high-frequency spectrum. Therefore, this style was adopted for this work. Table 1.1 gives a more detailed comparison of the three technologies discussed above. Notice that G_m - C filters must be tuned against process variations, aging, and operating temperature. Thus, tuning is essential for high-speed filters implemented in sub-micron technologies.

Table 1.1: Comparison of three technologies for implementing integrated filters.

	G_m -C	SC	Digital
Max Speed	$f_o \approx f_t/10$	$f_s \approx f_t/50$	$f_s \approx f_t/30$
SNR	75dB (at 1% THD)	90dB (at 1% THD)	108dB
Peak S/N+D @100kHz	63dB	73dB	—
SNR	50dB (at 1% THD)	56dB (at 1% THD)	50dB
Peak S/N+D @100MHz	< 45dB	48dB (for a 50MHz clock)	—
Power Dis. @100MHz	< 10mW/integrator	25mW per O/A (for a 50MHz clock)	ADC: 12mW/MHz Filter: 34mW/MHz
Area	0.0075mm ²	0.02mm ²	2mm ² /tap ADC 0.07mm ² /MHz
Overhead	tuning circuitry	anti-aliasing filter	ADC, anti-aliasing filter
Accuracy	depends on tuning mechanism	cap. ratio: 10bits	depends on wordlength
Non-ideal Effects	O/A finite dc gain, noise, slew-rate, temperature, parasitics	O/A finite DC gain, noise, slew-rate, temperature, clock feedthrough parasitics	overflow, quantization error of coefficients, ADCs, limit cycle
Niche	fast, low dynamic range, small area, low power applications	voice-band, low power	high resolution applications, complex algorithms

1.2 Filter Tuning Scheme

Choosing to use continuous-time analog filters to support high-speed copper-based services, implies designers must address the accuracy issue of these filters. It is known that process variations such as component tolerances and matching, in addition to aging and temperature fluctuations cause continuous-time filters to deviate from their nominal design

specifications. Consequently, a tuning mechanism is essential [Tsividis 93]. In addition, some of the filters required, such as channel equalizers, must also accommodate a variable environment or channel. For example, the response of a copper channel varies with cable length, ambient temperature, cable make-up, and load conditions. Channel response variation in a wireless medium comes from the different locations of the receiver from the base station. In a magnetic recording channel, variation in channel response comes from variation of the read head location relative to the center of the disk.

There are at least five different methods for tuning continuous-time filters. The most straightforward method, yet least practical, is manual tuning. This method is employed in many radio receivers today. A second method involves post-fabrication tuning which is normally performed at the factory and can be quite costly. It involves either the use of laser trimming or the storage of the tuning information in an on-chip EPROM [Plett 86]. Typically, process variations can be corrected for by using this scheme; however, variations that occur during service and channel variations are not accommodated. A third approach involves the implementation of several filters whose characteristics span the expected range of variation in filter response from the nominal. In this way, it is possible to switch in the different filter response as required in time during service. However, switching in filters can result in increased system latency, while the filter overhead comes at an expense in IC area and cost. Naturally, a control mechanism (usually a DSP) would be required to control the switching operation, thus, further increasing system cost. This method is deployed in accommodating recording channels [Veirman 92], [Laber 93].

A traditional approach to filter tuning is the master/slave technique where filter pole-frequency, f_o , and filter quality factor, Q , can be adjusted to compensate for process tolerances, aging, and temperature [Rao 77], [Tsividis 81], [Gopinathan 90]. This mechanism involves setting up a master filter, usually an oscillator, that matches the main or slave filter in some respect. The master's oscillation frequency is then phase-locked to a reference

frequency which corresponds to the pole-frequency of the tunable filter. By copying the parameters that govern the master's oscillation frequency onto the slave's corresponding parameters, one ensures the pole frequency of the filter is tuned to the appropriate location. Similarly, filter Q can also be tuned. Filter zeros, however, can not be tuned using this scheme in all applications. For this tuning scheme to be effective, good matching (1-3%) and tracking is required between master and slave [Tsividis 93 p. 405], [Veirman 92]. This requirement becomes more difficult to achieve in high-frequency applications due to parasitic effects which result in dependence between the two control loops, as can be observed from the effort in [Stefanelli 93]. Further, having the reference signal in band can lead to degradation in system SNR and can lead to intermodulation (IM) distortion. Moreover, this scheme does not accommodate channel variability.

Another approach to tuning is adaptive filtering [Kozma 91], [Kozma 93]. As mentioned earlier, this scheme requires the establishment of a filter error signal as a cost function to be minimized. Minimization is done, preferably yet not necessarily, during service in a least mean square sense via feedback. Since the filter error signal is constantly being minimized, good matching between filter constituent blocks is not as critical as in the master/slave scheme. Hence, both filter zeros and poles can be tuned offering more flexibility. As well, channel variability can be accommodated by this tuning mechanism. This mechanism has been employed in recent modems for equalization and is the reason for the improvement in the achieved capacities to be discussed in section 1.4. It is also the preferred choice for supporting high-speed services in either discrete or integrated form [Eugster 92], [Genlinx 93], [Twister 93], [Harrer 91].

1.3 State of the Art

In this section, we review the recent-reported contributions in the areas of programmable continuous-time filters, pulse-shaping filters, equalizers, and analog adaptive filters. The items

of observation are the process technology, the signal processing speed, the tuning mechanism, the tuning range, defined as the ratio of the maximum attainable frequency to the minimum attainable frequency, and performance in the proposed application.

1.3.1 Continuous-Time Tunable Filters

Recall from section 1.1 that the preferred filter technology for high speed is G_m - C . Thus, most, if not all, the recent contributions make use of this technology. Filters implemented in this technology show high sensitivity to process tolerances, especially in the most modern processes. To compensate for filter deviations, the master/slave PLL tuning technique has almost always been employed at moderate frequencies (below 10MHz) with successful results. However, at higher frequencies, where parasitic effects can no longer be ignored, this tuning scheme soon degrades. Consequently, an on-chip tuning mechanism is lacking in the most recent, yet most impressive, achievements in high-speed filtering. In this section, these contributions are highlighted. More detail on the transconductor architecture and performance are relegated to Chapter 4 where this discussion is more appropriate.

In [Nauta 92], a third-order elliptic lowpass filter in a $3\mu\text{m}$ CMOS process is described. The transconductor is a simple inverter, while the load capacitance is essentially parasitic capacitances. The filter is manually tunable from 22MHz to 98MHz by varying the DC supply voltage which sets transconductance. This filter requires a tuning voltage as high as 10V.

In [Snelgrove 92], a second-order filter in a $0.9\mu\text{m}$ CMOS process is described. Tuning is achieved manually with a tuning range over the entire VHF. The transconductor consists of two, single-stage, source-coupled input-pairs with a current mirror load. Fine pole-frequency tuning is achieved (tuning range of about 2) by varying input-pair transconductance through adjustment in the input common-mode voltage, while rough tuning is attained by using a switchable capacitor array. Filter Q is tunable by adjusting transconductor load resistance

which is essentially the inverse of the transconductance of a common-gate NMOS transistor. By varying this device's bias current, its transconductance is tuned. At the highest speed setting, the transconductors are typically loaded by only parasitic capacitances.

In [Lee 93], a fifth-order lowpass filter that is tunable from 24MHz-42MHz is described. The transconductor is implemented in a $2\mu\text{m}$ CMOS process and the tuning mechanism is manual. By adjusting transconductor bias current, the transconductance is varied, hence allowing adjustment in filter pole-frequency. Filter Q depends on a ratio of two capacitors: one on-chip fixed capacitor, the other an off-chip varactor.

In [Wyszynski 93b], simulation results for a third-order elliptic lowpass filter in an 8GHz bipolar process are presented. The filter is tunable over the range 200MHz-290MHz and makes use of single-stage, differential-pair transconductors.

In [Martinez 92], a fourth-order bandpass filter, implemented in a $1.5\mu\text{m}$ CMOS process, is described. Both filter pole-frequency and Q are tunable using an on-chip tuning mechanism. The filter pole-frequency is tunable over the range 7MHz-14MHz by varying the transconductance of the transconductors. The tuning mechanism assumes parasitic poles are 20 times larger than the filter pole-frequency, so their effects can be neglected. In this case, f_o , which is set by transconductor bias current, can be configured to track an external clock frequency that is down-scaled by a factor N , with N also the ratio of weighted current sources. This low-frequency reference clock is placed outside the filter bandwidth so that it does not deteriorate filter dynamic range. Having a low-frequency reference clock, allows the implementation of a G_m - C integrator whose time constant tracks that of a switched-capacitor integrator whose time constant can be well controlled. The pole-frequency of the filter is then an up-scaled version of the low-speed integrator through N . The Q tuning scheme works as follows. A first-order lowpass filter, whose pole frequency is set by the same f_o tuning mechanism, is input a pulse sequence. This same input is also supplied to a biquad filter. The

output envelopes of these two filters are then made to track. The output amplitude of the first-order filter depends on its pole frequency, while the biquad output envelope depends on the biquad bandwidth which is a function of Q . Hence, by tracking the two envelopes the biquad Q can be tuned and its control voltage can be replicated to the bandpass filter biquad sections. At high frequencies, where f_o is close to the parasitic capacitances, this tuning mechanism will deteriorate for the same reason as the master/slave technique.

In [Stefanelli 93], a fifth-order 7MHz elliptic filter that is based on the folded cascode transconductor structure in a $2\mu\text{m}$ CMOS process is disclosed. An on-chip master/slave scheme to tune filter pole-frequency is employed. However, it is reported that the scheme failed to perform due to mismatch between master filter and the slave filter.

While there are many filters reported in the literature that have successful on-chip tuning circuitry [Gopinathan 90], these filters all operate below 10MHz. Higher frequency filters seem to lack an on-chip tuning scheme. As well, they exhibit a rather low continuous tuning range, far below what is sufficient to cover process variations ($\pm 50\%$) as well as channel variations. The reasons for the low tuning ranges will be discussed in Section 4.1.1.

1.3.2 Pulse-Shaping Filters

Traditionally, discrete LC lowpass filters have been used to shape the emitted signal to meet the Federal Communications Commission (FCC) regulation concerning electro-magnetic emissions¹. This discrete realization was standard practice due to the lack of available technology and the high variations in process, even when the technology became available [Twister 93]. Consequently, these discrete solutions were not only bulky but costly. For example, in [Starlan] a seventh-order elliptic LC filter is disclosed. The filter has a cutoff frequency at 15MHz with 60dB suppression above 30MHz. The filter is manufactured using

1. In Canada, these regulations would be stipulated by the Department of Communications.

thick-film technology as the interconnect structure for the applied capacitors and inductors. This passive filter is packaged in a 9-pin single ceramic package of width 0.2" and length 1".

One approach to cost reduction is the use of signal rise and fall time synthesis and lowpass filtering of the transmit transformers to obtain some degree of harmonic suppression. Such a technique is employed in National Semiconductor's TWISTER transceiver chip [Twister 93]. However, this shaping mechanism only reduces electro-magnetic interference (EMI) at key frequencies by approximately 20dB which may be insufficient to pass the FCC Class B radiation limit for NRZI signalling at the standard transmit amplitude of $2V_{pp}$, but will meet the limit for MLT-3 signalling (see Section 2.1.1 for definition of terms).

By using adaptive techniques to compensate for process variations, it should be possible to achieve robust pulse-shaping filters in integrated form which are even more essential at higher transmission rates. In addition, it might be possible to drive the cables directly and adaptively correct for load variations, thus, eliminating the need for drive transformers.

1.3.3 Continuous-Time Equalizers

While at low frequencies digital and/or switched-capacitor equalizers have been used in modems, at higher speeds discrete and more recently integrated equalizers have been proposed. In this section, these proposals for both the copper channel and the magnetic recording channel are briefly discussed.

In [Harrer 91], a second-order equalizer is proposed for 125Mb/s NRZI signalling over unshielded twisted-pair cables. The equalizer consists of two fixed poles and two adjustable zeros. The technology is passive but no mention of the tuning mechanism is provided.

In [Genlinx 93], an equalizer for 270Mb/s binary transmission over a coaxial cable is disclosed. The equalizer is fabricated in a 12GHz bipolar process and accommodates 100m,

200m, and 300m cable lengths. The tuning scheme makes use of a peak detector that produces an output voltage proportional to the pulse height of the equalized signal. This output is an indicator of the signal strength, and for a well controlled channel will vary with cable length. When used in a feedback loop, this signal can be used to control equalizer high-frequency boost for the three cable lengths. This scheme, therefore, requires the equalizer parameters exhibit good tracking with cable length and transmit amplitude. These assumptions are valid in some applications but generally other variations such as temperature, bridge taps, and ohmic losses also affect channel response. In these cases, peak-detection adaptation will fail to provide optimal equalization. Thus, the challenge is to provide efficient and robust algorithms for adaptive analog equalizers that can account for both skin effect and ohmic losses, as well as other unforeseen channel impairments. Although not completely disclosed, the equalizer in [Twister 93] for 125Mb/s NRZI signalling over twisted-pair cables makes use of the same tuning technique.

As discussed in [Pai 92], equalizers for the magnetic recording channel have been switchable, fixed-frequency discrete LC or tap-delay lines and each customized for different sections of the disk (inner diameter, mid diameter, outer diameter). These equalizers are accurate to 5-10% over the entire disk [Pai 92], [Veirman 92]. Recently, integrated solutions have been proposed for reduced cost, size, and weight. To date, these schemes use a tuning procedure such as master-slave to account for process variations ($\pm 50\%$) [Khoury 91] and a digital controller together with a DAC to tune against channel variations (a factor of 2.5-5). [Khoury 91], [Laber 93], [Veirman 92]. In the following paragraphs, the more-recent contributions in this area are reviewed.

In [Veirman 92], a seventh-order equiripple linear-phase filter is discussed. The filter makes use of G_m -C integrators in a 9GHz bipolar process. The filter features a pole frequency tunable over the range 2MHz-10MHz with two programmable real zeros, symmetrically placed about the imaginary axis, for high-frequency boost. Tuning against channel variations

is achieved through external control voltages that are programmable by an external DAC and a DSP. This equalizer was designed for 15Mb/s data rates. In [Yamasaki 94], this same filter architecture in a $1\mu\text{m}$ BiCMOS process is employed for a 72Mb/s (72Mbaud) partial response class IV (PR4) retrieval system. The pole frequency is tunable over the range 3MHz-24MHz.

In [Laber 93], a sixth-order Bessel filter with two programmable zeros (placed as above) in a $1.5\mu\text{m}$ -4GHz BiCMOS process is presented. The G_m - C integrator input consists of triode-mode, source-coupled devices whose transconductance (hence filter pole-frequency) is adjusted by varying input device drain-source voltage. Tuning is obtained by varying stage transconductances controlled through an external serial interface. A 6-bit control word allows the variation in filter pole-frequency from 4.7MHz to 20.3MHz for 64 different possibilities. High-frequency boost is achieved by filter zero adjustment that is similarly controlled using a 5-bit serial interface giving 32 different slimming levels. To account for process variations, an external resistor is used and a circuit is devised that sets the transconductance of an on-chip transistor to replicate the inverse of this resistance. The controlling bias conditions for this transistor are then copied to the filter transconductors. The equalizer was designed for a 36Mb/s (36Mbaud) system.

In [Welland 94], a seventh-order equiripple linear-phase filter with two zeros (placed as above), implemented using G_m - C technology in a $0.8\mu\text{m}$ CMOS process, is disclosed. The tuning mechanism consists of programmable 7-capacitor arrays (one for each pole) giving a pole-frequency tuning range from 2.1MHz-17.1MHz. The zeros are tuned by varying transistor transconductance through an externally controlled digital register. This equalizer is used in a 36Mb/s (36Mbaud) system.

In [Choi 94], a seventh-order equiripple equalizer is utilized in a 64Mb/s (64Mbaud) system. The G_m - C equalizer was implemented in a $0.8\mu\text{m}$ -7GHz BiCMOS process. Rough pole-frequency tuning against channel variation is attained using a 2-bit capacitor array and a

3-bit transconductance array for 32 different frequency responses. Using both forms of tuning avoids a large transconductance spread and a large capacitance spread. The pole frequency is tunable over the range 6MHz-33MHz. To compensate against process and temperature variations, an on-chip master/slave PLL scheme is employed. Since the equalizer does not realize any zeros, high-frequency boost is achieved digitally using an FIR filter implemented in a digital ASIC. Consequently, a 72MHz 6-bit flash DAC is required.

For comparison, a completely digital adaptive equalizer for a 64Mb/s (64Mbaud) system is also noted here. This digital chip [Abbot 94] was implemented in a 0.8 μ m CMOS process. Equalization is achieved using a 9-tap adaptive FIR filter running at a maximum clock frequency of 78MHz. The FIR filter requires 6-bit data lines, 10-bit coefficient precision, 12-bit multipliers, and 15-bit adders. The equalizer alone dissipates 500mW at 72MHz with a total gate count of 5500 devices. A training sequence is employed for the adaptation cycle. Naturally, an analog front-end for this system is still required.

With the exception of the equalizers in [Laber 93], [Choi 94], and [Abbot 94], the reported analog equalizers all require prior knowledge of process variations and channel variations so that compensation parameters against the expected deviations can be sent to the appropriate programming control. Naturally, prior knowledge on channel variation in [Laber 93] and [Choi 94] is still required. Thus, this application forms a niche for analog adaptive equalizers that could constantly self-tune against process and channel variations without requiring prior knowledge about these variations. Such a solution might offer simpler circuitry for lower cost, lower power, and perhaps smaller size.

1.3.4 Analog Adaptive Filters

While digital adaptive filters are common-place in data transmission modems, to date, there have been very few reported results on analog adaptive filters. The reason for this lack

stems from the fact that digital implementations have met present data communication needs, and due to the lack of a well developed theory for adaptive continuous-time signal processing prior to [Johns 90]. In addition, there have been very few demonstrations of successful analog adaptive filters in a practical high-speed application. In high-data rate communications, analog adaptive schemes become more significant; hence, there is a growing need for the technology. In this section, the contributions reported in this field are reviewed.

Probably the earliest integrated analog adaptive filter was reported in [Voorman 82]. Therein, a 10MHz, 7-tap, analog, delay-line equalizer is described and employed in cancelling inter-symbol interference (ISI) or echo in video teletext. Coefficient update is implemented using an on-chip LMS algorithm that makes use of 4-quadrant Gilbert multipliers and integrators for the correlation of the error and gradient signals. A reference signal is derived by shaping the equalizer output signal to an expected waveform. Hence, the adaptation only works when the initial equalizer output is not significantly deviated from its expected output — alternatively only low levels of ISI are acceptable.

In 1984, a 5-tap, 100kHz, switched-capacitor, decision-feedback equalizer (DFE) was reported in [Yasumoto 84]. This equalizer was implemented to illustrate adaptive ISI cancellation for a dispersive data transmission channel. This adaptive FIR filter made use of the LMS algorithm requiring 4-quadrant Gilbert multipliers and one integrator per tap coefficient.

In 1991, an analog, continuous-time, adaptive filter implemented in a $2\mu\text{m}$ CMOS process was presented in [Kwan 91]. The filter is of second-order and provides lowpass, notch, and bandpass outputs displaying a maximum signal processing speed of 300kHz. The filter pole-frequency is the only adaptive parameter tuned using the LMS algorithm. The correlation of the lowpass and notch filter outputs is used to tune filter pole-frequency. For a sinusoidal input, zero coefficient variance (i.e. steady-state) implies the notch frequency is locked to that

of the input. This scheme allows the demodulation of a frequency-shift keying (FSK) input as demonstrated in the paper for a 260kHz carrier with frequency deviation of 47kHz.

Later that same year, an adaptive filter with tunable poles and zeros was demonstrated [Kozma 91]. A tuning approach that made use of a pseudo-random (PN) sequence of length 15 was used to tune a third-order filter to a desired transfer-function. The reference signal for adaptation, which made use of the sign-data LMS algorithm, was stored in an EPROM. This reference signal corresponds to the desired filter output for the given PN sequence input. Hence, the filter must be brought out of service during the adaptation cycle. The programmable and gradient filters were fabricated in a 3 μ m CMOS process and ran at 1kHz. The adaptation algorithm and the PN sequence generator were implemented using discrete hardware.

Recently, a second-order, analog, adaptive filter using switched-capacitor technology, implemented in a 3 μ m-1.6GHz BiCMOS process, was reported [Fichtel 92]. This disclosure shows how the filter can be used to demodulate an FSK waveform (similar to [Kwan 91]) and as an interference canceler in the 10kHz range.

For the technology to be fully accepted, demonstration of an analog adaptive filter working successfully at VHF (where analog is strong) in a real application is required. Also, simple yet efficient adaptation algorithms must be sought to keep power dissipation and circuit overhead to a minimum.

1.4 Data Communications: evolution and future prospects

The communication channel and the information being communicated has evolved considerably since the telephone was demonstrated in 1877 by Alexander Graham Bell. At that time, copper was the chosen channel for information transport, while the information itself

was voice. From that point in time, advances in telecommunications was born. Not long after his remarkable invention in 1877, Mr. Bell patented the twisted-pair cable which enhanced transmission quality due to improved system signal to noise ratio (SNR). In the late 1890's, advances in cable make-up and cable equalization in the form of loading coils were introduced which further improved transmission range. Half a century later, in 1947, the transistor was introduced which brought about a new era of innovation. Development into electronic switches and digital transmission to enhance transmission capacity began in 1955. As a result, the T1 1.544Mb/s *interoffice* digital transmission was introduced in 1962. It consisted of 24 voice-band channels sampled at 8kHz using pulse amplitude modulation (PAM) and then coded using 8b/sample pulse code modulation (PCM). The physical link consisted of screened twisted-pair telephone trunks with repeaters placed every 6kft. For longer links such as transcontinental routes, at about the same time, fiber served as the transport link. Recent advances in digital signal processing, coding, adaptive equalization, and VLSI technology are now making high-speed transmission on non-loaded *subscriber* loops possible. This service, which could also reduce the cost (installation and maintenance) of interoffice T1 trunks by reducing the number of repeaters, is known as high bit-rate digital subscriber lines or HDSL. HDSL is a scheme that proposes a transmission rate of 1.6Mb/s over two lines (800kb/s each) for distances of 12kft on 24 gauge twisted-pair without any bridge taps.

The introduction of the transistor brought to the marketplace inexpensive computers and consequently the demands for computer data transmission grew. To meet these demands, 300b/s and later 1200b/s modems using FSK were introduced in the early 1960's. Technological advances in the 60's and 70's led to the increase of these speeds to 2400b/s using phase shift keying (PSK), and together with echo cancellation techniques 4800b/s modems were available in the 80's. Recently, quadrature amplitude modulation (QAM), trellis coded modulation, coding, and adaptive equalization have been used to increase the data rate to 9.6kb/s, 14.4kb/s, 19.2kb/s, and 28.8kb/s [Lechleider 91], [Pahlavan 88], [Borsook 94].

To support the growing demands for greater information throughput within a given building, the 802.3 local area network (LAN) was defined in 1985 as a 10Mb/s Manchester coded baseband system. The physical layer or “Ethernet” was a 50Ω coaxial cable with a maximum segment length of 500m serving 100 stations. In 1988, standards appeared for a lower cost LAN known as “Cheapernet”. Cheapernet is an RG-58 (TV) cable with a maximum segment length of 200m supporting 30 stations. With the anticipation of even higher throughput intensive applications like imaging, real-time video, video conferencing, and multimedia, the 10Mb/s Ethernet would saturate. Even today, for many applications such as desktop publishing, the Ethernet is reaching saturation. This need for higher data throughput is the reason why the American National Standards Institute (ANSI) in 1982 began working on a standard for higher bit-rate LANs. The standard proposed was fiber distributed data interface, or FDDI. FDDI specifies a transmission rate of 125Mb/s (data rate of 100Mb/s with 25Mb/s timing overhead) on a distributed dual token ring fiber network supporting up to 500 stations with a maximum separation of 2km for a total link of 100km. However, because of the high cost of FDDI adapters (\$5k-10k, 10 times that of Ethernet), and the need for stripping copper and rewiring fiber to the desktop (about \$700/station), sales of FDDI products have kept low, except in pharmaceutical firms and some universities that have large LAN usage [Tsao 91], [Eugster 92]. For this reason, a group of vendors in 1990 began investigating cheaper alternatives. The proposal showed that 125Mb/s could be supported over shielded twisted-pair (STP) cables for a maximum cable length of 100m. Since the initial proposal, prospects for the same specifications over category 5 (datagrade) and category 3 (voicegrade) unshielded twisted-pair (UTP) cables have been brought to light. This alternative, also termed copper distributed data interface, or CDDI, offered a reduction in cost by more than one half. Since then, many vendors have joined the pool to bring FDDI to the global marketplace by providing CDDI products making 125Mb/s to the desktop a reality. This newest proposal has reshaped the original FDDI proposal for the future in that vendors are now proposing a twisted-pair link to the desktops with a maximum length of 100m and a fiber backbone.

While advances in voice and data transmission took place in their own arena, proposals for the integration of both media began to appear in 1971 and was termed Integrated Services Digital Networks, or ISDN. The concept was to replace the analog voice-band subscriber loop connecting to the T1 by a digital link supporting 160kb/s (2B1Q 4-PAM signalling, information rate of 144kb/s plus 16kb/s overhead). In 1985, proposals for Broadband Integrated Services Digital Networks (BISDN) appeared for an optical network supporting 150-600Mb/s data rates.

To this point, two major transmission media, namely copper and fiber, have been identified. A third medium is air. This medium initially served as the channel for radio signal transmission, private audio communication links, and later, as a trans-continental microwave telephone link through the use of satellite repeaters. In the early 1980s, public mobile cellular and cordless telephones appeared, and today, this channel is becoming more attractive as it offers the flexibility of portability. Thus, many vendors are gearing towards portable personal communication services (PCS). These include portable telephones, televisions, facsimile machines, and LANs.

While portability is a clear advantage, the service is expensive as base stations must be installed and wired to the local exchange. Also, in terms of data communications, the service lacks the capacity attainable using the other two media. For example, available wireless LANs currently support 4-16Mb/s links with 80ft coverage range from base station. Although this thesis focuses on filtering techniques to accommodate the copper channel, the techniques may be applicable or extended to the RF and IF sections of these wireless PCS. Hence, in this respect the wireless channel is a lesser competitor to copper than fiber, and so, the advantages and life expectancy of the copper channel relative to the fiber channel must be established.

Today, a new vision in telecommunications is generating immense research. This vision is “bandwidth on demand” or the integration of voice, data, and image using a packet

switching network protocol termed asynchronous transfer mode, or ATM. Current proposals for the physical layer are copper or fiber running at the optical carrier level 3 (OC-3) rate of 155Mb/s and a fiber link at the OC-12 rate of 622Mb/s. This global interconnection of voice, data, and video peripherals, either fixed or portable, is depicted in Figure 1.1.

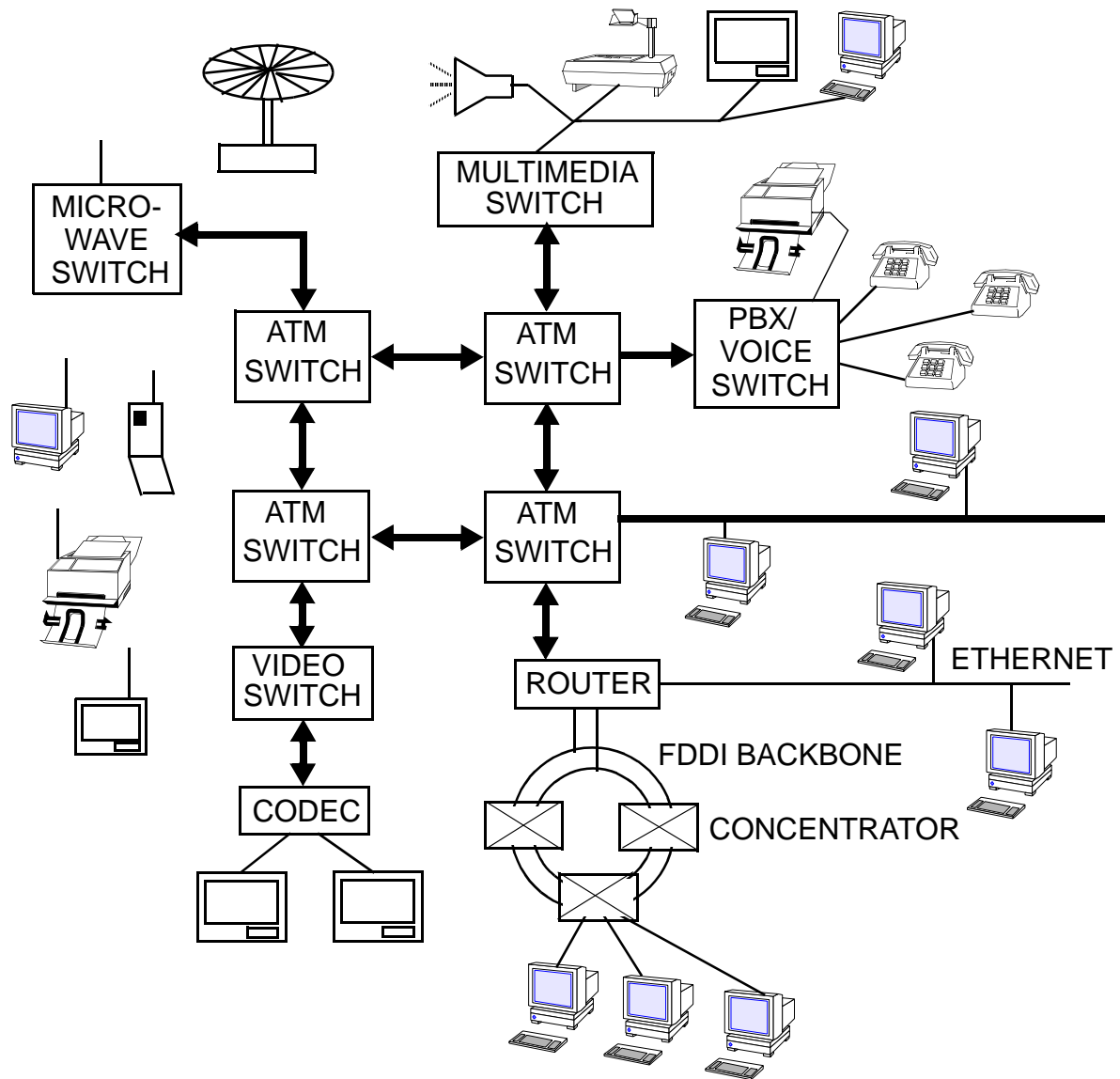


Figure 1.1: Anticipated future communication system.

1.5 Fibre vs. Copper: a case study

In order for the vision depicted in Figure 1.1 to become a reality, one must address the physical layer. Naturally, for the portable products a wireless medium is the only choice, but this channel will always be limited to short range. Thus, a backbone link will always be required. There is little question that the backbone medium of choice of the future will be fiber due to its higher transmission capacity and range. The question is, when will fiber deployment begin to favor copper deployment globally. In [Walkoe 91], the authors predict this transition will be in the year 2010. They also write that “we must make the best use of the existing \$100 billion copper plant in the U.S.”, and that “copper will dominate over fiber customer access for at least the next ten years” during which “copper access will ease the transition to fiber access by accelerating the use of higher speed services”. This notion is also shared by others [Jain 93], [Saunders 93], and it is not a surprising one since replacing copper with fiber is expensive and economics may prolong the introduction of new proposals into the marketplace — unless the service becomes essential. Copper, however, has a lower entry cost, and thus, will ease the introduction of the newer proposals into the marketplace. The speedier introduction into the marketplace will result in demands for even higher bandwidth and higher capacity, consequently accelerating the need for fiber. Not to mention that a copper solution would act as a competitor to its fiber counterpart and force the cost of fiber products down. To appreciate these notions, let us look at FDDI as a case study.

It is known that a fiber channel surpasses a copper one in terms of capacity and operating range. In addition, while a copper channel can be tapped without disturbing a connection in service, a fiber link cannot be tapped without disturbance. Thus, fiber offers better security. In addition, a copper channel is prone to EMI or noise pickup from other cables, photocopiers, power lines fluorescent tubing etcetera — a fiber channel does not. An unshielded copper channel transmitting high-speed data will act as an antenna radiating radio frequency waves that will interfere with nearby radio receivers and other copper links — clearly not the case

with fiber. In a typical transceiver, near-end crosstalk (NEXT), or transmit link bleeding of transmit power into the receiving link, forms one of the major items that limits the capacity of twisted-pair cables. A fiber channel is weakly affected by this mechanism. Copper cables also suffer a large attenuation as function of cable length. This attenuation is a second mechanism that limits cable capacity and range at high frequencies. Limitations in the capacity of a fiber channel come from chromatic dispersion which results in attenuation of the transmit power as function of cable length. Typically, this attenuation is not as severe as for copper, and thus, the usable range for fiber far exceeds that of copper at high frequencies. So, with the advantages of fiber over copper, why is copper deployment still preferred?

Copper exists in every structural complex, replacing it would only be justified when the capacity of copper becomes insufficient to carry required service data rates. Cost continues to be a major issue mainly because fiber is a new technology, thus, installation skills are still in their prime years. This makes material costs and labor expensive, not to mention the expensive installation equipment. Table 1.2 gives a comparison for the two transmission technologies as well as their relative costs for implementing a single “FDDI” port. Notice that today a fiber solution is 2-3 times more expensive than a copper one. Thus, it is understandable why managers were reluctant to rewire their buildings ever since the original proposal in 1982, and why only select vendors were offering FDDI products. Pursuant to the appearance of proposals for CDDI, more vendors entered the “FDDI” arena creating more activity in the concept which eased the product’s entry into the marketplace. CDDI, in turn, has brought fiber FDDI prices down (by one half from 1982) and accelerated proposals for even faster networks. Moreover, the price for fiber has come down from over \$1.10/ft in 1990 to \$0.65/ft as of today [Keough 92]. Usually, it is economies of scale that bring prices down, but when a product does not sell well, this mechanism fails — the case for fiber products.

As long as copper remains a feasible and cheaper alternative to fiber, it will be deployed and will form a vital role in the evolution for higher network speeds and more aggressive

telecommunication visions. Further, in the case of FDDI, for example, “even if an ideal cable type appears — one that costs next to nothing, supports infinite transmission distances, and produces negligible amounts of radiation — users will still need CDDI devices to connect it to” [Saunders 91]. Thus, this channel *must* be accommodated through various type of filtering functions to achieve practical systems. More so, we are currently operating well below the Shannon capacity for the copper channel. With research into more sophisticated coding and filtering techniques, the usable range of the copper channel can be extended which is a worthwhile endeavour that will allow the quick entry of future telecommunication proposals to the marketplace.

Table 1.2: Comparison of different transport media and the respective cost for “FDDI”

	Fiber	STP	Categ. 5 UTP	Categ. 3 UTP
Cable type	graded-index 62.5/125 μ m multimode fiber $\lambda = 1.3\mu$ m	150 Ω , 2 copper pairs wrapped in metal shielding and sheathed together in a braided metal shield, covered by PVC jacket	100 Ω , 4 copper pairs twisted together and protected by a thin PVC jacket 1cm twists	100 Ω , 4 copper pairs twisted together and protected by a thin plastic jacket 1ft twists
Diameter		10mm	5mm	3mm
Trans. range	2km, 100Mb/s	100m, 155Mb/s	100m, 100Mb/s	50m, 100Mb/s
Radiated EMI	none	some	high	high
Signal-to-NEXT ratio	∞	(100m) 48dB @ 62.5MHz	(100m) 40dB @ 62.5MHz	(100m) 30dB @ 62.5MHz
Attenuation	2dB/km	(100m) 8dB @ 62.5MHz	(100m) 12dB @ 62.5MHz	(100m) 31dB @ 62.5MHz
Noise sources	thermal	thermal, echo	thermal, crosstalk, impulse, echo, inductive	thermal, crosstalk, impulse, echo, inductive
Security	secure	can be tapped	can be tapped	can be tapped
Cable cost	\$0.70/ft	\$0.40/ft	\$0.25/ft	\$0.10/ft

Table 1.2: Comparison of different transport media and the respective cost for “FDDI”

	Fiber	STP	Categ. 5 UTP	Categ. 3 UTP
Time to terminate a connection	20 minutes	10 minutes	5 minutes	5 minutes
Wall outlet cost	\$33	\$33	\$11	\$11
Connector type	duplex SC	DB-9	RJ-45	RJ-45
Connector and jumper cost	\$323	\$83	\$20	\$20
Total cost: port, adapter, wire and installation	\$4773-\$9773	\$3315-\$4315	\$3000-\$3275	\$3000
Cost /UTP	3:1	1.5:1	1:1	1:1

1.6 Thesis Outline

Chapter 1 presented the academic challenges of, and the industrial benefits from, analog adaptive filtering, and hence, defined the motivations for this work. It was noted that efficient tuning algorithms are lacking and demonstration of an analog adaptive filter in a practical high-speed application is needed for the technology to be commercially viable. It should be noted that the focus here is on supporting the copper channel. This channel will remain viable for at least the next decade and forms a vital role in bringing newer and faster transmission to the marketplace. Further, even in the future “fiber world” copper will still be employed for short-hop connections. Hence, the benefit of analog adaptive filters in this area. Finally, the state-of-the-art pertaining to the topic of this thesis was reviewed.

In Chapter 2, the various issues involved in the transmission of data over copper cables are addressed. These issues impair detection capabilities, and hence, various filtering

operations to mitigate these impairments are required. Further, the theoretical limits within which communication can take place over copper cables are investigated and the results are compared with current attainable capacities.

In Chapter 3, the concept of curve fitting for the adaptation algorithm is illustrated through four examples. These examples make use of the basic idea but at the same time demonstrate possible variations. Hence, the chapter opens the door to further research based on the basic idea. Practical issues such as DC offsets are investigated for the pulse-shaping filter example and solutions are considered.

In Chapter 4, the circuits used for implementing a prototype system for testing the pulse-shaping example are discussed. The filter prototype was optimized for speed, linearity, and a wide tuning range.

In Chapter 5, experimental results for the prototype filter and the pulse-shaping system are presented. The results illustrate the practicality of the adaptive technology and the performance of the tuning algorithms. As well, practical issues such as DC offsets are highlighted.

In Chapter 6, the effects of different DC offsets on the performance of four common adaptive algorithms are analyzed. Based on the theoretical results, one is now better able to comment on the relative merits of each algorithm and choose the best algorithm for a particular implementation technology and application.

In Chapter 7, a summary of the thesis contributions is given and suggestions are made for exciting further research.

CHAPTER 2

Background Theory

This chapter presents the fundamental background material necessary for a proper understanding and appreciation of the remaining chapters. Copper channel transmission capabilities are explored in the light of the mechanisms that impair transmission performance. The supporting filtering functions required for reliable data transmission and the need for adaptive filters are addressed. Although data transmission over copper is the main focus of this work, related applications such as data retrieval systems are also treated. The latter part of this chapter briefly reviews state-space filter theory and important aspects of adaptive filtering and equalization.

2.1 Data Transmission Over Copper

This section reviews the issues involved in the transmission of data over a copper channel. These mechanisms, which must be addressed to effectively transmit reliable data over copper, include: electro-magnetic interference, cable propagation loss, channel noise, and crosstalk. Numerical examples are given for typical copper channels and these are used to analytically predict theoretical and attainable limitations on channel capacities.

2.1.1 Electro-Magnetic Interference (EMI)

When a signal is sent over a copper wire, some of the signal is emitted from the wire in the form of EMI. At higher transmission frequencies, the wire becomes a better radiating antenna and more signal is emitted. This emission, which is mostly concentrated at the fundamental frequency, is deleterious as it interferes with nearby radio receivers and adjacent copper wires through coupling. Consequently, government agencies impose various regulations that specify limitations on EMI radiated from a given device. For example, the FCC regulation in Title 47 Part 15 lists the field strength level radiated from an unintentional device and measured at a distance of 3m from the device. There are two classes in this regulation: Class A concerns equipment operated in a commercial environment, Class B concerns equipment operated in a residential installation. These limits are shown in Figure 2.1 [FCC], [Mazzola 91], [Lindsay 92].

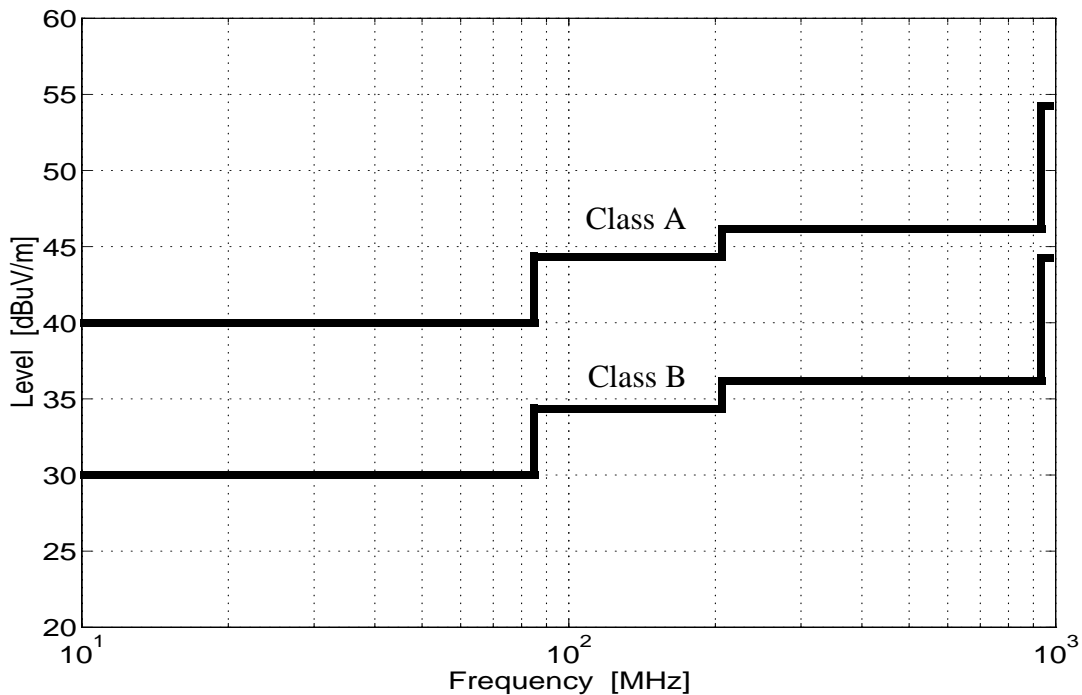


Figure 2.1: FCC line spectrum limits on maximum allowable EMI at 3m.

The most straightforward method to reduce emissions is to use twisted cables driven differentially, effectively cancelling emitted waves. Cable shielding is also possible at the expense of cable cost. More advanced techniques employ spectral shaping or coding to reduce emitted power. A recent proposal by Crescendo Communications Inc. [Mazzola 91] uses multilevel NRZI coding to reduce signal spectral power bandwidth occupancy. The standard accepted for CDDI, shown in Figure 2.2, was three level NRZI signalling, MLT-3. Notice that

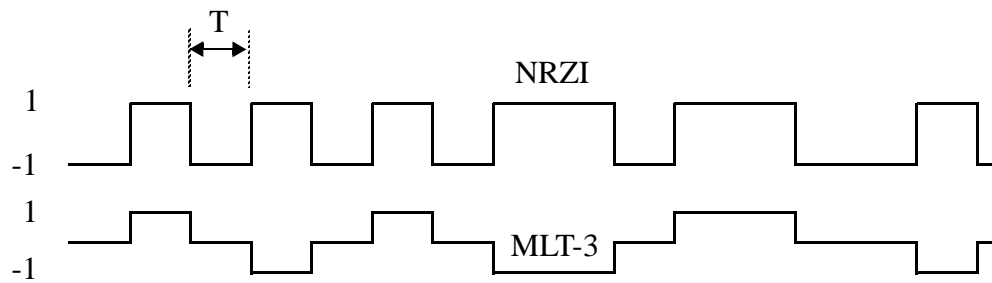


Figure 2.2: An example of NRZI and MLT-3 line codes.

the fundamental frequency for NRZI is 62.5MHz and that of MLT-3 is 31.25MHz for a 125Mbaud (also 125Mb/s) transmission rate. In fact, 90% of the signal power is concentrated at frequencies below 69MHz for NRZI and below 41MHz for MLT-3. Thus, MLT-3 would meet the FCC EMI regulation with more ease than NRZI.

To comply with EMI regulations, the signal power for the choice of line code must be limited to some level. This limitation is normally done by shaping (lowpass filtering) the emitted signal in conformity with a time domain and/or frequency domain template. A time-domain template for NRZI signalling for a bit rate of 125Mb/s over category 5 UTP is shown in Figure 2.3. The shaded area indicates the extreme values the output signal may take. A frequency domain template generally describes harmonic power suppression relative to the fundamental. For example, the template for 10Mb/s Manchester signalling over a coaxial cable is given in Table 2.2.

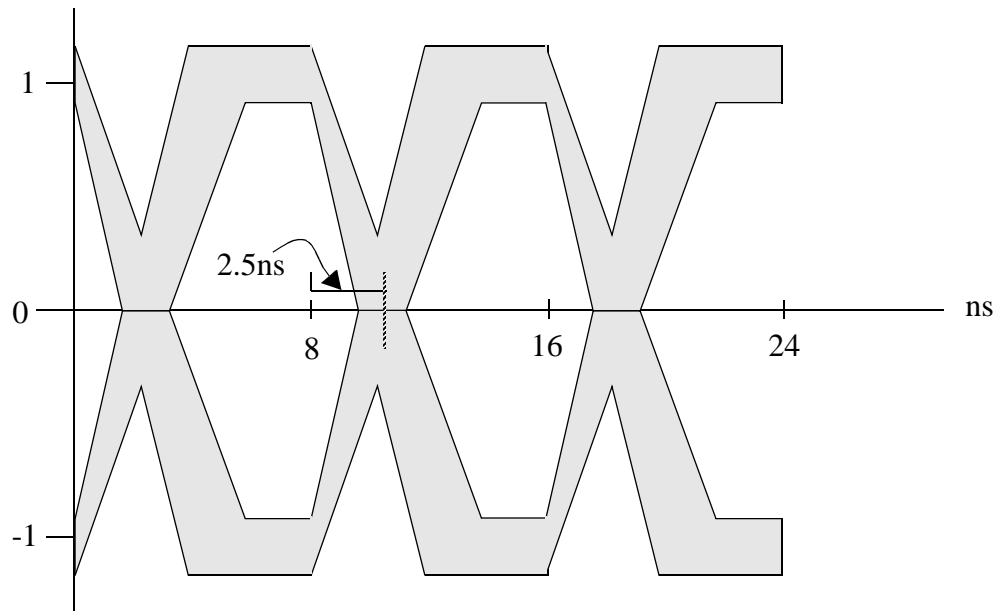


Figure 2.3: Transmit Envelope for 125Mb/s NRZI signalling on UTP.

Table 2.1: Frequency domain template for 10Mb/s NRZI signalling on coax.

Tone Location	Signal Level Below Fundamental
2nd and 3rd harmonic	at least 20dB
4th and 5th harmonic	at least 30dB
6th and 7th harmonic	at least 40dB
all higher harmonics	at least 50dB

2.1.2 Cable Attenuation

As frequency increases, the depth of penetration of a signal into a conductor decreases. Consequently, the resistance of the cable increases with signal frequency and this characteristic is known as “skin effect”. Skin effect gives rise to attenuation that increases linearly with the square root of signal frequency [Kalet 90], [Ungerboeck 92]. Specifically, an analytic model for the channel response is given by

$$|H_c(f)|^2 = e^{-\alpha l \sqrt{2f}} \quad (2.1)$$

where l is the length of the cable in meters and α is the loss parameter for a given cable. Typical values for α and the attenuation as function of frequency for 100m cable length is shown in Table 2.2.

Table 2.2: UTP loss data for 100m cables.

	Category 3	Category 5
$\alpha \quad (m \sqrt{Hz})^{-1}$	5.3526e-06	3.378e-06
Cable loss (dB/100m)	$.3 \sqrt{f} + 0.23f$ f in MHz	$.1 \sqrt{f} + 0.01f$ f in MHz

Clearly, this frequency-dependent cable loss will result in an imbalance in the amplitude of the frequency components of the received signal. This imbalance will be manifested in terms of ISI and will eventually lead to errors in the detected data. In addition, temperature variations also influence cable loss and the dependency is more pronounced at frequencies above the audio band [Bell 70]. Between room temperature and 40°C, attenuation increases by more than 20% or 20dB/kft in some instances for category 5 UTP [Saunders 92], [Johnston 91]. Thus, corrective action, namely equalization, must be taken to minimize ISI at the receiver to ensure reliable data detection. Recall from Chapter 1 that equalization was one of the schemes used to enhance modem transmission rates.

In many cases the cable or channel response varies in time not only due to temperature fluctuations and cable length but also due to cable make-up, presence of bridge taps, and load conditions. Thus, adaptive equalization must be employed [Harrer 91], [Qureshi 92]. At low frequencies, digital and/or switched-capacitor techniques are employed to realize various types of adaptive equalizers; most common are decision feedback equalizers (DFE) and fractionally spaced equalizers (FSE). For a detailed synopsis on adaptive equalizers, the reader

is referred to [Qureshi 85]. At high frequencies, analog equalizers are required and are usually referred to as bump or boost equalizers. Bump equalizers approximate the inverse of the cable response up to some frequency (usually the baud rate) and then roll off to prevent noise build up. These equalizers come in two forms: pre-equalizers (at the transmitter) and post-equalizers (at the receiver). Pre-equalizers are beneficial as they can enhance system SNR, whereas post equalizers do not enhance system SNR. However, pre-equalizers are not preferred at high frequencies since the higher transmit power will increase EMI. In Section 2.3.3, some background theory on equalization is given.

2.1.3 Noise

If an equalizer is used to account for channel attenuation and ISI, then the detection circuitry, placed after the equalizer, should result in zero detection error in the absence of noise. However, noise on the received signal will lead to some detection errors and limit the communication capabilities of a channel. For a copper channel, there are various sources that give rise to noise:

- Thermal:** Thermal noise is a phenomenon associated with Brownian motion of electrons in a conductor. These electrons are in continual random motion in thermal equilibrium and collide with the conductor molecules. Since each electron carries a unit negative charge, each flight of an electron between collisions with the molecules constitutes a short pulse of current. This rise in AC current is termed thermal noise. Thermal noise has a constant power spectral density versus frequency, and thus, behaves as a white noise source.
- Echo:** Echo noise results from the combination of imperfect hybrids and gauge changes on the line as well as signals reflected from bridge taps.
- Inductive:** Inductive noise is interference from 60Hz and its harmonics caused by power lines.
- EMI:** Electro-magnetic interference is noise coupled onto cable wires caused by electromagnetic radiation. Typical sources include

fluorescent lights, switching transients, lightning, photocopiers, and other electrical equipment.

Crosstalk: Crosstalk is noise caused by the coupling of signals from one cable to another when cables are in a common conduit.

To simplify the analysis of transmission capacities, it is customary to assume the noise at the receiver end is additive, has white Gaussian statistics, and is uncorrelated with the information signal. The cumulative distribution function, $p(v_n)$, of this zero-mean noise is given by,

$$p(v_n) = \frac{1}{\sigma_n \sqrt{2\pi}} \int_{-\infty}^{v_n} e^{-v^2/2\sigma_n^2} dv \quad (2.2)$$

where σ_n^2 is the variance of the noise. Since this noise is white, it is reasonable to assign the power spectral density as

$$N(f) = N_o \quad V_{rms}^2/Hz \quad (2.3)$$

Since there are no means of compensating for noise, this mechanism places an upper bound on the capacity of a given channel when infinite detection circuitry and transmission bandwidth are available. The relationship of this upper bound with noise and bandwidth performance of a transmission channel is discussed in Section 2.1.5.

2.1.4 Near-End Crosstalk (NEXT)

It was noted in the previous section that additive noise degrades detection capabilities. When the channel is copper, crosstalk, or the coupling of signals from one cable to another, also impairs detection. In fact, NEXT, the coupling of the transmit signal onto the received cable, dominates channel noise and limits the communication capabilities of the copper channel as will be seen in Section 2.1.6. Far-end crosstalk (FEXT), the coupling of the data signal from other transmitters onto the received cable, is less severe, and hence, will be neglected.

Crosstalk is modelled as a statistical phenomenon caused by the randomly varying differential capacitive and inductive coupling between adjacent two wire transmission lines. An analytic model for the NEXT transfer-function is [Cherubini 93], [Im 93], [Kalet 90], [Ungerboeck 92]:

$$|H_x(f)|^2 = K_n f^{3/2} \quad (2.4)$$

where K_n is a constant that depends on cable type. Typical values for K_n and the amount of crosstalk rejection as function of frequency is depicted in Table 2.3.

Table 2.3: UTP NEXT losses.

	Category 3	Category 5
$K_n \text{ (Hz}^{-3/2}\text{)}$	7.94e-14	6.31e-16
NEXT rejection (dB)	41 – 15log [f] <i>f</i> in MHz	62 – 15log [f] <i>f</i> in MHz

2.1.5 Theoretical Limitations on Capacity

At this point it is reasonable to ask — given the factors that impair transmission, what is the maximum transmission capacity of a given channel?

In the late 1940's, Claude Shannon of Bell Laboratories developed a mathematical model of information. His work gives some fundamental boundaries within which communication can take place. This bound on channel capacity is known as the Shannon limit and is given by [Stein 67], [Joshi 87]:

$$C_{SH} = \int_0^{\infty} \log_2 \left[1 + \frac{S(f)}{I(f)} \right] df \quad (2.5)$$

where $S(f)$ and $I(f)$ are the one-sided signal and interference power density spectra, respectively. The upper limit of the integral in (2.5) implies the signal power spectral density spans infinite frequency.

Consider a bandlimited channel whose transfer-function is $H_c(f)$ where

$$H_c(f) = \begin{cases} G, & f \leq F_{eff} \\ 0, & f > F_{eff} \end{cases}$$

In addition, let the signal power spectral density, $P_s(f)$ bandlimited to F_{eff} , be

$$P_s(f) = \begin{cases} P_o, & f \leq F_{eff} \\ 0, & f > F_{eff} \end{cases} \quad (2.6)$$

Assuming the noise is Gaussian with power spectral density $N(f) = N_o$, then the capacity of the channel under the above three assumptions becomes

$$\begin{aligned} C_{SH}(F_{eff}) &= \int_0^{F_{eff}} \log_2 \left[1 + \frac{|H_c(f)|^2 P_s(f)}{N(f)} \right] df \\ &= F_{eff} \log_2 \left[1 + \frac{P_{TOT}}{N_o F_{eff}} \right] \end{aligned} \quad (2.7)$$

The term $\frac{P_{TOT}}{N_o F_{eff}}$ represents the SNR at the receiver input where $P_{TOT} = G^2 P_o F_{eff}$. Observe that the Shannon capacity, (2.7), is a function of channel bandwidth and receiver SNR. It should be kept in mind that the Shannon limit assumes error free transmission and infinitely complex coding, filtering, and detection techniques which are difficult to achieve. Consequently, transmission capacities are significantly lower than the limit in (2.7).

Based on the previous section, the Shannon limit for the twisted-pair channel can be computed as outlined in Appendix 2.1. The results of interest at this point are respectively, the maximum channel rates¹ for a crosstalk dominated channel, $C_{SH_{NEXT}}(F_{eff})$, and a noise dominated channel, $C_{SH_{AWGN}}(F_{eff})$, supporting a bandlimited signal:

$$C_{SH_{NEXT}}(F_{eff}) = F_{eff} \left(\log_2 \left[\frac{|H_c(4/9F_{eff})|^2}{|H_x(4/9F_{eff})|^2} \right] + 0.4092 \right) \quad (2.8)$$

and

1. "Maximum channel rate", rather than "channel capacity", is used here since in obtaining these figures of merit, certain assumptions are made as explained in Appendix 2.1.

$$C_{SH_{AWGN}}(F_{eff}) = F_{eff} \log_2 \left[\frac{|H_c(4/9F_{eff})|^2 P_o}{N_o} \right] \quad (2.9)$$

Also of interest are the crossover points CO_{NEXT} and CO_{AWGN} , defined here as the points where the received signal power spectral density and the NEXT spectral density (or noise, whichever the case) are equivalent. For signal bandwidths above the crossover point, the theoretical channel rate does not increase with signalling bandwidth, as can be inferred from the argument inside the logarithm operators in (A2-3) and (A2-4) and from the results for category 3 UTP cable in Table 2.4. The table compares the maximum channel rates for

Table 2.4: Shannon channel rates and crossover points for 100m UTP cables.

	Category 3 UTP	Category 5 UTP
$C_{SH_{NEXT}}$	154.6Mb/s	1.07Gb/s
$C_{SH_{AWGN}}$	732Mb/s	1.84Gb/s
$C_{SH_{NEXT}}(62.5MHz)$	153Mb/s	639Mb/s
$C_{SH_{AWGN}}(62.5MHz)$	469Mb/s	600Mb/s
CO_{NEXT}	30MHz	190MHz
CO_{AWGN}	150MHz	370MHz

100m of category 3 and category 5 UTP cables. The assumed value for the received unshaped SNR (P_o/N_o) was 40dB with P_o flat over all frequencies.

It is clear that compensating for crosstalk is highly desirable if one wishes to enhance transmission capabilities to the Shannon noise bound. Since crosstalk depends on highly variable parameters such as the nature of cable coupling, ambient temperature, cable make-up, and load conditions, a crosstalk canceller must be adaptive. To date, this author has not come across such filters in use in high-speed transmission systems. However, at lower speeds these filters, in the form of echo cancellers, are employed in telephony and the fastest known modems (see Chapter 1).

2.1.6 Attainable Transmission Rates

From the previous sections, it can be seen that channel capacity depends on receiver signal to interference power spectral density ratio (SIDR) and effective transmission bandwidth F_{eff} . Maximization of transmission capacity therefore requires maximizing both parameters. However, these parameters are conflicting terms — higher F_{eff} results in lower SIDR. Since capacity is linearly proportional to F_{eff} and logarithmically proportional to SIDR, maximization of transmission capacity would best be done by increasing F_{eff} at a cost in reduced SIDR as long as it is technologically possible and complies with FCC EMI regulations. With this observation in mind, one must find the minimum acceptable system SIDR. This value, or alternatively the minimum acceptable signal to interference ratio (SIR), depends on the acceptable bit error rate (BER) for the application. Consider NRZI signaling in Gaussian noise and a slicer as a detector. Define QSNR (quantizer signal to noise ratio) as the minimum ratio between the RMS level of the peak “eye” opening of the transmit pulse and the RMS noise (or interference) level resulting in a given BER. For multi-level signalling, the minimum required SIR would be higher than the QSNR by a few dBs (due to the extra levels) depending on the number of levels, while at the cost of trellis coded modulation, the required SIR at the receiver can be relaxed. Using (2.2) and with reference to Figure 2.4, one can

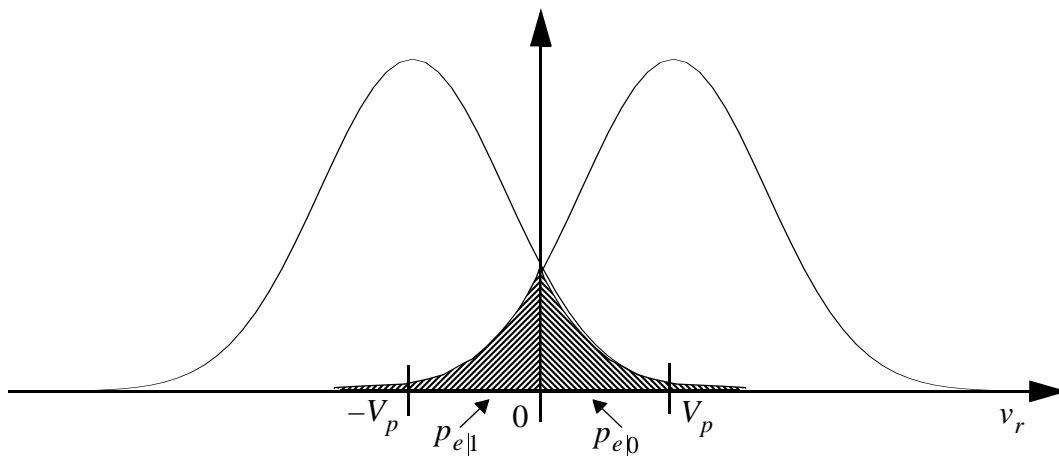


Figure 2.4: Error probability for NRZ signalling.

compute the probability of error for NRZI signalling, whose expected peak level at the receiver is V_p volts, as

$$p_e = \frac{1}{2}P(v_n > V_p) + \frac{1}{2}P(v_n < -V_p) \quad (2.10)$$

The solution of (2.10) yields

$$p_e = \frac{1}{2} \operatorname{erfc} \left[\sqrt{\frac{V_p^2}{2\sigma_n^2}} \right] \quad (2.11)$$

where it should be noted that $V_p^2/2\sigma_n^2$ represents the QSNR at the receiver. For a BER of 10^{-12} for example, (CDDI specification) a QSNR of 17dB is required.

Since NEXT dominates noise for a copper channel, a SNXR of at least 17dB is required. Thus, for category 5 UTP using (2.1) and (2.4), we obtain

$$10\log[e^{-2\alpha l \sqrt{2F_{eff}}}] = 10\log[K_n F_{eff}^{3/2}] + 17 \quad (2.12)$$

Equation (2.12) shows the trade-off relationship between maximum transmission bandwidth and maximum reach. For example, suppose we choose $F_{eff} = 62.5\text{MHz}$, this choice yields a maximum reach of $l = 100\text{m}$ for UTP-5 cables. The characteristics of this channel (assuming P_o/N_o is 40dB) versus frequency is shown in Figure 2.5. Observe from the Figure that a SNXR of 17dB occurs at 62.5MHz. Next, the signalling scheme must be chosen for the choice of F_{eff} . One possibility is NRZI, which would result in a baud rate (and bit rate) of 125Mb/s (the standard for CDDI). Comparing with the Shannon limit in Table 2.4 (third row, second column) for this SIR and F_{eff} , the rate obtained is only 20% the theoretical value predicted for a NEXT dominated channel. Thus, there should be room for improvement, either by using more bandwidth efficient codes or more complex detection algorithms. For example, consider MLT-3 which requires a SIR 3dB above the QSNR or 20dB (the three level code reduces the eye opening by 1/2). For the same channel (i.e. $l = 100\text{m}$), we obtain from Figure 2.5 that $F_{eff} = 60\text{MHz}$. Consequently, for the same bandwidth occupancy, the bit rate is 240Mb/s which is 38% of the theoretical limit for a

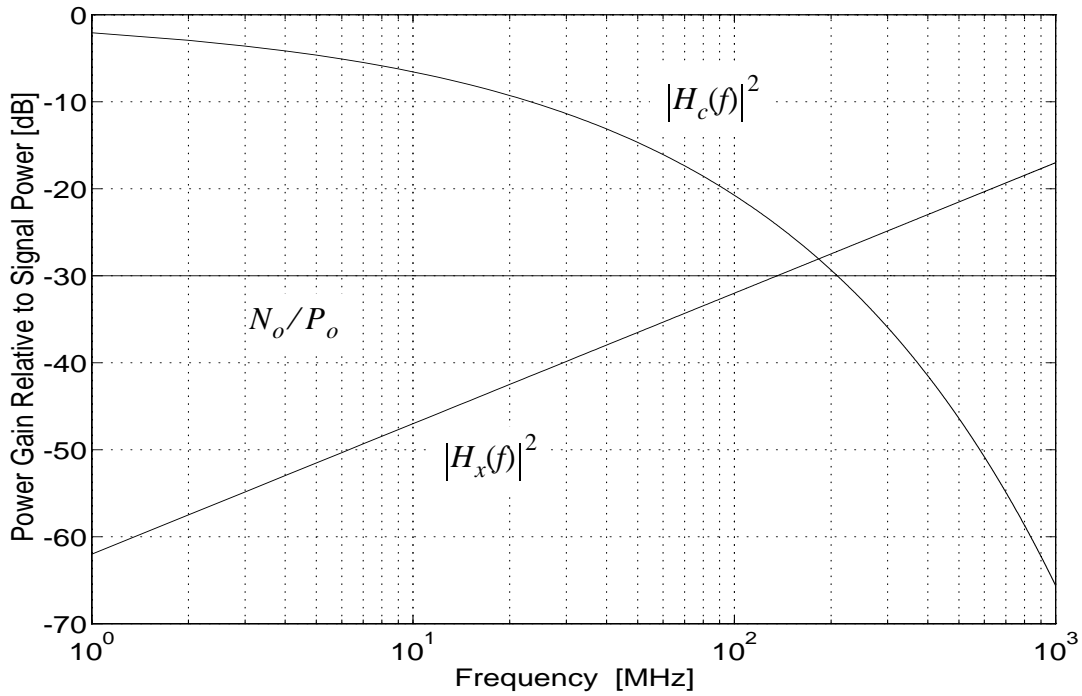


Figure 2.5: Cable attenuation, NEXT and noise as function of frequency.

NEXT dominated channel. Alternatively, a 4-level code such as 2B1Q which suffers a 7dB penalty relative to NRZI would require 24dB SIR. From Figure 2.5, this SIR means that $F_{eff} = 45MHz$ giving a baud rate of 90Mbaud. At 2bits/ baud a maximum bit rate of 180Mb/s is obtained which is 35% the theoretical value for similar bandwidth occupancy of 45MHz for a NEXT dominated channel. These results are summarized in Table 2.5. Naturally, to support these alternatives, pulse-shaping filters and equalizers that can accommodate the bandwidth requirements for the chosen line codes and maintain the received SIR at the appropriate level are needed. Improvement in attainable capacities to the theoretical limitations would come from even more sophisticated coding and detection techniques and NEXT cancellation. These results are very informative as they clearly show that the copper channel is capable of accommodating today's and anticipated near-future (see Chapter 1) data traffic. Hence, effort placed at implementing supporting circuitry for this channel is warranted.

Table 2.5: Attainable data rates for 100m of category 5 UTP with a BER of 10^{-12} for 3 line codes assuming a minimum SIR.

	NRZI	MLT-3	4-PAM
Minimum SIR	17dB	20dB	24dB
Max. Bw (MHz)	62.5	60	45
Attainable bit rate	125Mb/s	240Mb/s	180Mb/s
Rate /Shannon limit	1/5.10	1/2.66	1/2.86

2.2 Related Applications

While our main focus is on high speed data transmission over copper, the filtering techniques to be discussed could be extended to provide equalizers for magnetic recording systems, equalizers for computer backplanes, adaptive filtering for digital radio receivers, and others. This section addresses an area wherein some consideration has been done by the author.

2.2.1 Magnetic-Disk Storage Channels

In contrast to data communications over distance, recording deals with communication over time. It consists of a write head (coil) through which an alternating current is passed creating a magnetic field. Consequently, the magnetic flux particles in the media align in a direction that depends on the write current. In linear recording (voice recording), the angle subtended by the flux lines to the horizontal (for example) linearly depends upon the applied current, while in saturation recording (data recording), the angle subtended takes on one of two values. To retrieve the stored information, a read head (coil) is placed above the medium. Since the medium is in motion at constant velocity, a voltage is induced in the read head that depends on the rate of change of the magnetic field in the recording medium. The magnetic recording and retrieval process is qualitatively illustrated in Figure 2.6.

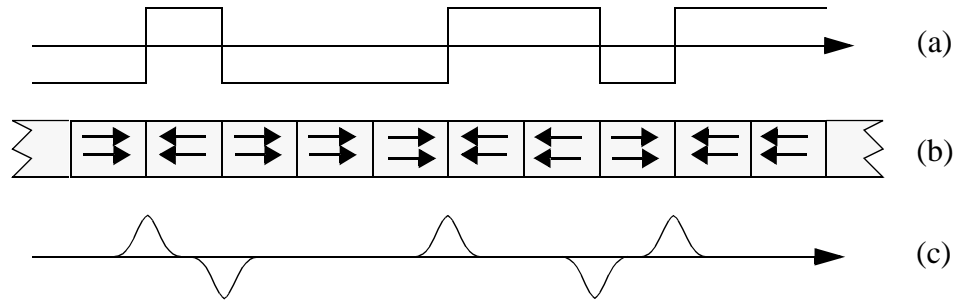


Figure 2.6: Illustration of magnetic recording. a) the NRZ waveform applied to the write head corresponding to the bit sequence “110010110”. b) the magnetization of one track. c) the voltage on the read head coil.

The recorded output, shown in Figure 2.6c, has been modeled using various models and the accepted model (though simplistic) for the pulse shape is

$$p(t) = \frac{1}{1 + (2t/PW50)^2} \quad (2.13)$$

where $PW50$ is a parameter that corresponds to the pulse width at half the pulse amplitude. This parameter depends on the flying height (distance from read head to the media), the media thickness, the linear velocity of the media, and the transition width. Observe from Figure 2.6c that the output should ideally consist of a series of impulses or delta functions (i.e. the derivative of the waveform in Figure 2.6a). Thus, $p(t)$ represents the magnetic channel impulse response, also known as the Lorentzian channel response. This channel is bandlimited, and thus, produces an output that is wider than the expected delta function. The transfer-function of this channel is given by

$$P(f) = j\pi^2 PW50 f e^{-\pi PW50 |f|} \text{sinc}[f] \quad (2.14)$$

In today’s mechanical technology $PW50$ varies between 50-200ns [Pan 92] and essentially limits the attainable data rates. Consider once again Figure 2.6, notice that an increase in the data rate would require narrower window spacings (narrower flux transitions). However, since the read pulses have a finite width due to the bandlimited channel, higher packing density will result in more ISI. Thus, an equalizer is required to mitigate ISI through

pulse slimming (increasing channel bandwidth). With proper equalization, it is possible to pack 2-2.5 bits per $PW50$. Based on the $PW50$ figures in [Pan 92], disk drives operating at 50Mb/s should be possible. Recently, disk drives operating at 64Mb/s and 72Mb/s have been reported [Choi 94], [Abbot 94] and [Yamasaki 94]. These systems require equalizers with pole frequencies up to 40MHz. Thus, for this speed requirement and the need for low power, low cost, and light weight (for laptops), analog solutions are preferred.

Since the flying height and media velocity are not well controlled from disk to disk, the $PW50$ varies, yielding a variable channel response. This variation is one reason why a single equalizer transfer-function is not sufficient. In addition, for a circular medium typical of a computer magnetic disk, the position of the read head relative to the center of the disk influences channel response, and thus, the amount of ISI. With reference to Figure 2.7, notice that for the same write pulse the flux transition spacings on a track closer to the inner diameter of the disk are narrower. Hence, more ISI would result there relative to a track closer to the outer diameter of the disk. This physical condition is another reason why a tunable equalizer is required. Schemes for constant density recording have been proposed to alleviate this effect so that transition spacings are equal along any track of the disk, requiring a variable data rate. But even with this approach, it appears that tunable equalizers are still required [Veirman 92], [Laber 93].

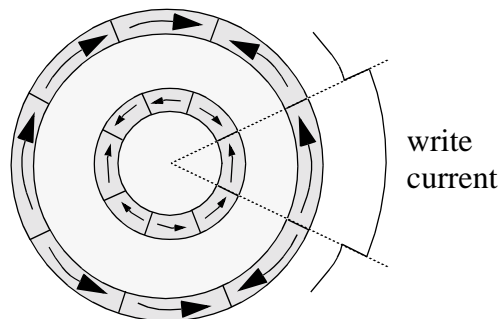


Figure 2.7: Illustrating effects of disk geometry on transition spacings.

Along with the quest for higher data rates, there is a need for higher density (storage density) at modest medium size. To increase density, track spacings must be reduced (see Figure 2.7), but it will increase NEXT from adjacent tracks and degrade detection. Thus, an adaptive NEXT canceller might be required in future data recording systems.

For completeness, it is appropriate at this point to briefly discuss the detection circuitry. The required electronics is schematically shown in Figure 2.8. By passing the derivative (with respect to time) of the equalized read pulse through a zero-crossing detector, it is possible to detect the occurrence of a pulse (flux transition) as well as extract timing information for clock recovery. However, far from the transition, the read output signal decays to zero — so noise will cause numerous zero crossings. To mitigate this problem, amplitude detection is also employed to gate out the correct transition as depicted in the figure.

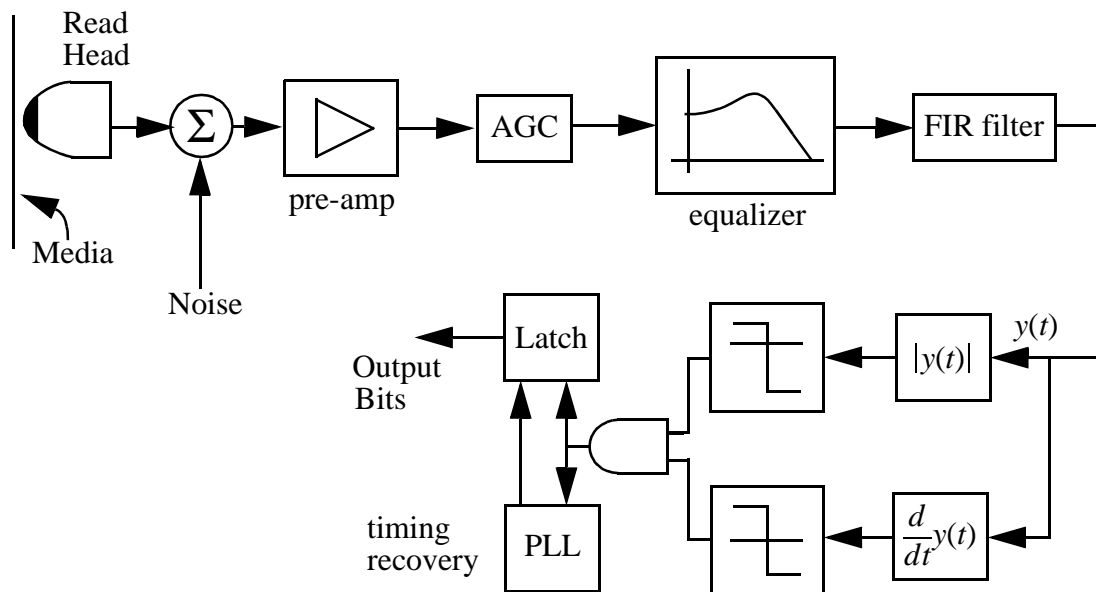


Figure 2.8: Block diagram of a typical magnetic recording read channel.

2.3 Filtering Fundamentals

In this section, fundamental concepts of filtering, which will be used in the remaining chapters, are reviewed.

2.3.1 State-Space Filters

Discussions on the implementation of analog filters can be found in [Sedra 78] and [Schauman 90]. In this thesis, the state-space notation is used, and thus, warrants a brief introduction. This notation describes a state-variable model of a passive filter. That is, a passive circuit is selected from filter design reference books or is otherwise developed to model the desired filter response. Then, the passive filter is modelled as a state-variable network where integrators emulate the current and voltage relationships of the inductors and capacitors in the passive prototype. These integrators are then interconnected according to the signal-flow diagram in the state-variable network. Thus, letting the input to the network be represented by $u(t)$ and the output be represented by $y(t)$, while the N states (outputs of the integrators) of an N^{th} order network be represented by $x_i(t)$, where $i \in \{1, N\}$, the describing equations of the network in the Laplacian domain can be shown to be [Snelgrove 86]

$$s\mathbf{X}(s) = \mathbf{A}\mathbf{X}(s) + \mathbf{b}U(s) \quad (2.15)$$

$$Y(s) = \mathbf{c}^T\mathbf{X}(s) + dU(s) \quad (2.16)$$

By manipulating (2.15) and (2.16) it can be shown that the describing function for the state-variable network, alternatively the transfer-function of the filter, is

$$T(s) = \mathbf{c}^T(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{b} + d \quad (2.17)$$

The eigenvalues of matrix \mathbf{A} solely describe the poles of the system, while the vectors \mathbf{c} and \mathbf{b} and the scalar d define the system zeros and are derived from a signal-flow diagram or from the pole-zero constellation. For example, consider the signal-flow graph for an arbitrary second order filter as shown in Figure 2.9.

The state-space system for this filter is

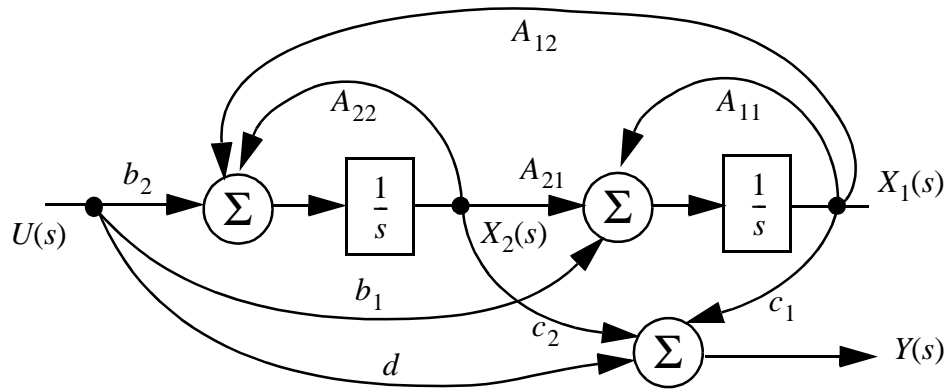


Figure 2.9: Signal-flow graph of an arbitrary second-order filter.

$$\begin{aligned}
 &= \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}, & \mathbf{b} &= \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} \\
 \mathbf{c}^T &= [c_1 \ c_2], & d &= d
 \end{aligned}$$

Notice that by simply changing the coefficients of the set space $\{\mathbf{A}, \mathbf{b}, \mathbf{c}, d\}$ arbitrary transfer-functions can be obtained. These adjustments can be done using any one or a combination of the methods outlined in Section 1.2.

2.3.2 Adaptive Filters

An adaptive filter is a tunable self-correcting filter wherein tuning is achieved through the minimization of a cost function — usually an error signal. The error signal is obtained by taking the difference between the filter output and a desired output. The desired output can be obtained by supplying a known input to the filter for which the optimal output can be pre-computed. This method is employed in adaptive filters that make use of a training sequence. Consequently, the adaptive filter must be brought out of service (off-line) during the tuning cycle. Alternatively, it is possible to obtain an error signal using an on-line procedure if the desired filter output at certain time instants is known, and then compared with the filtered output for the unknown (information signal) input. This thesis investigates the practicality of this new alternative.

Tuning of the filter is achieved by adjusting the coefficients that govern the response of the filter. This adjustment follows the method of steepest descent in that the coefficient update is specifically the negative of the mean-squared error gradient with respect to the coefficient, or mathematically

$$w_i(k+1) = w_i(k) - \mu \nabla_{w_i}(k) \quad (2.18)$$

where μ is the adaptation step-size and $\nabla_{w_i}(k) = \frac{\partial}{\partial w_i} E[e^2(k)]$ is the coefficient gradient for an arbitrary filter coefficient w_i . Since the evaluation of the derivative of the mean squared value of the error signal would require the observation of the error signal over all time, it is customary to replace the mean squared value by the instantaneous squared value of the error signal. Letting $\delta(k)$ represent the desired output and $y(k)$ the filter output at time instant k , then

$$e(k) = \delta(k) - y(k) \quad (2.19)$$

Taking the derivative of the instantaneous squared value of the error signal we obtain

$$\frac{\partial}{\partial w_i} e^2(k) = -2e(k) \frac{\partial}{\partial w_i} y(k) \equiv -2e(k) \phi_{w_i}(k) \quad (2.20)$$

where $\phi_{w_i}(k)$ is the gradient of the filter output with respect to the coefficient being tuned. Thus, the coefficient update algorithm, also known as the LMS adaptive algorithm in the adaptive signal processing literature [Widrow 85], [Treichler 87], is

$$w_i(k+1) = w_i(k) + 2\mu e(k) \phi_{w_i}(k) \quad (2.21)$$

For the system defined by (2.15, 2.16 and 2.17) it can be shown that [Johns 91]

$$\frac{\partial}{\partial A_{ij}} Y(s) = (s\mathbf{I} - \mathbf{A}^T)^{-1} \mathbf{c} X_j(s) \quad (2.22)$$

$$\frac{\partial}{\partial c_i} Y(s) = X_i(s) \quad (2.23)$$

$$\frac{\partial}{\partial b_i} Y(s) = \mathbf{c}^T (s\mathbf{I} - \mathbf{A})^{-1} U(s) \quad (2.24)$$

$$\frac{\partial}{\partial d} Y(s) = U(s) \quad (2.25)$$

The expression in (2.21) can be quite naturally extended to the analog domain [Johns 91], specifically

$$w_i(t) = 2\mu \int_0^t e(\tau) \phi_{w_i}(\tau) d\tau \quad (2.26)$$

Notice that the output states of the main filter (see also Figure 2.9) are simply gradients required to update the \mathbf{c} vector elements, and thus, the filter zeros. Adapting filter poles, as can be seen from (2.22), requires N filters similar to the main filter but whose \mathbf{b} vector corresponds to the \mathbf{c} vector of the main filter and the \mathbf{A} matrix transposed. The input to the gradient filter that produces the gradient signals to adapt the coefficients of the j^{th} column of the filter \mathbf{A} matrix is the filter gradient signal $X_j(s)$. Alternatively, it is possible to reduce the \mathbf{A} matrix to single row or single column [Johns 90] for which the single row or column governs all filter poles. In this way, it is sufficient to adapt only a single column or row, thus, requiring only 1 gradient filter.

The gradient term in (2.21) or (2.26) aids in governing the direction of coefficient adjustment. In certain application this direction can be extracted from the error signal itself without the need for the computation of the gradient signal. If this is the case, the circuitry for adjusting filter poles can be simplified even further. The techniques discussed herein focus on this simplification to reduce hardware complexity. Based on the above introduction, the general adaptive analog filter as depicted in Figure 2.10 should be evident.

The LMS algorithm, given in (2.21) or (2.26), has been investigated extensively in the technical literature and simplifications of this algorithm have been proposed. Some of these include the sign-data, the sign-error, and the sign-sign LMS algorithms [Treichler 87]. The motivation for these simplifications was to provide simpler hardware implementations. For example, as will be apparent from Chapter 6, the sign-sign LMS algorithm is completely digital. Thus, a multiplier becomes a simple XOR gate, while the integrator is an accumulator

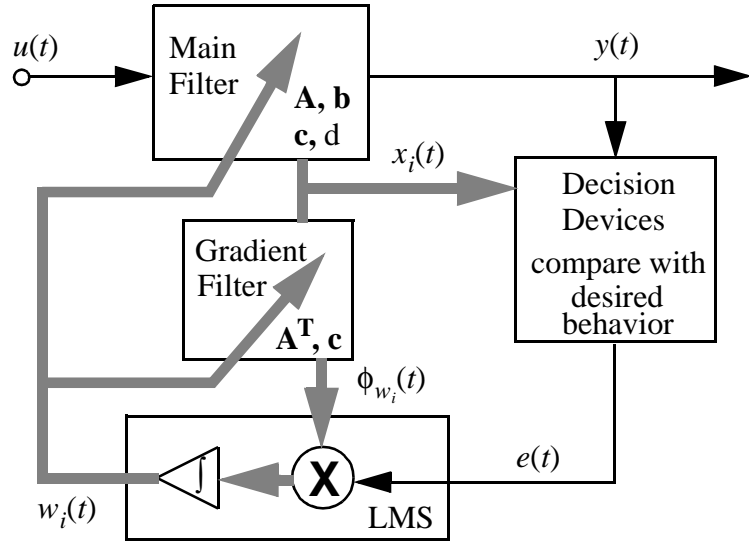


Figure 2.10: Block diagram of an adaptive analog filter. For the LMS block, it is possible to replace the integrator by an U/D counter and a DAC.

that is naturally undamped and does not suffer from input offset like its counterpart analog equivalent. As well, a fully digital algorithm allows the flexibility of complex and/or non-linear numerics without significant increase in hardware complexity. In addition, it allows a method to compensate for DC offsets in the LMS algorithm [Shoval 92], [Yu 94].

DC offset is one of the major imperfections that limits the performance of analog adaptive filters [Enomoto 83], [Johns 91], [Kwan 91], [Menzi 92], [Qiuting 92], [Tzeng 90], and [Fichtel 92]. These offsets lead to non-zero correlation between the error and gradient signals. For optimum adaptation, however, this correlation must be substantially zero. Non-zero correlation raises the residual output excess mean-squared error resulting in a non-optimal filter response. Consider the update expression in (2.21). Taking the expectation, $E[\bullet]$, of both sides of (2.21) and assuming that the algorithm has converged ($E[w_i(k+1)] = E[w_i(k)]$), we obtain

$$E[e(k)\phi_{w_i}(k)] = 0 \quad (2.27)$$

Hence, orthogonality between the error and gradient signals implies the filter is in its optimal mode at steady-state. Now consider the presence of DC offsets. Specifically, let m_e represent the DC offset on the error signal, m_{x_i} the DC offset on the i^{th} gradient signal, and m_i the equivalent DC offset at the input of the i^{th} integrator and at the output of the i^{th} multiplier. The update expression for the i^{th} coefficient in the presence of DC offsets becomes

$$w_i(k+1) = w_i(k) + 2\mu\{(e(k) + m_e)(\phi_{w_i}(k) + m_{x_i}) + m_i\} \quad (2.28)$$

Taking the expectation of both sides of (2.28) at steady-state, one obtains

$$E[e(k)\phi_{w_i}(k)] = -(m_i + m_e m_{x_i}) \quad (2.29)$$

The non-zero correlation in (2.29) due entirely to DC offsets is evident.

To date, various methods have been proposed to mitigate the problem of DC offsets. In [Kwan 91] and [Fichtel 92], manual trimming is employed.

In [Johns 91], it is proposed to pass the error signal through a high gain stage prior to correlation. This proposal results in a reduction of the finite correlation in (2.29) by the gain factor. Although this solution is effective in reducing the non-zero correlation in (2.29), attaining a high gain stage becomes more difficult at higher frequencies.

In [Tzeng 90], it is proposed to use two integrators per coefficient to realize the correlation in (2.26) with the integrators connected in cascade. At steady-state, the output of the second integrator (the one that feeds the coefficient), must have zero variance. Thus, its average input must be zero. Therefore, the output of the first integrator (the one that feeds the second integrator), must be exactly the negative of the input-referred offset of the second integrator. Since the output of the first integrator is a constant, its input must have zero mean. Assuming this first integrator is ideal (otherwise the same offset effect will take place), the mean of its input (the product of the error and gradient signals including their DC bias) must

be zero. Hence, the term m_i in (2.29) is nulled for reduced correlation. Since the first integrator must be ideal and its task is to track the input-referred offset of an opamp, the author proposes the use of a tapped resistor string which he claims is practical as its dynamic range need not be large. Naturally, complete nulling of m_i is not possible due to the quantized nature of the resistor string and the multiplier output offset.

In [Qiuting 92] and [Menzi 93], it is proposed to use offset cancelled integrators in a switched-capacitor technology. To cancel the integrator offsets due to clock feedthrough, the authors propose the use of a dummy offset-cancelled unity gain opamp whose output reflects the opamp output offset due to clock feedthrough. The output of this opamp is then input to each coefficient integrator realizing the LMS circuitry. Assuming the output due to clock feedthrough is the same for all the opamps in the LMS algorithm, partial cancellation of m_i is possible. Residual offset due to the multiplier output offset still remains. In [Qiuting 92], multiplier offset cancellation is proposed using the same technique employed in the offset-cancelled integrators. To minimize m_e , the authors AC-couple the error signal by passing the error signal through an amplifier with a lowpass filter in its feedback loop. In [Enomoto 83], this same method to minimize m_e is proposed, while all other offset sources are not dealt with.

In [Shoval 92], it is proposed to use the sign-sign variant of the LMS algorithm for adaptation. In this case, the algorithm lends itself to a digital implementation of the correlator. Specifically, the multiplier is replaced by an XOR gate and an up/down counter. For a synchronous system, the offset term m_i is non-existent. Two comparators are required to produce the sliced versions of the error and gradient signal to be input to the XOR gate. The cancellation of the other two offset terms as well as comparator input offset is achieved by placing a lowpass filter in the feedback path of a comparator. This configuration effectively AC-couples² the signal input to each comparator. For this method to be effective, the lowpass

filter in the feedback loop must itself be ideal. Hence, an up/down counter cascaded with a simple DAC is used.

For more information on adaptive filters the reader is referred to [Treichler 87] and [Widrow 85].

2.3.3 Equalization for Data Communications

As briefly stated in Section 2.1.2, an equalizer is a signal processing device designed to combat ISI. The earliest equalizer structure was the T -spaced transversal or tapped-delay-line equalizer. In such an equalizer, where T is the sampling time, the current and past sampled values of the received signal are linearly weighted by equalizer coefficients. These coefficients are chosen to force the samples of the combined channel and equalizer impulse response to zero at all but one of the T -spaced instants in the span of the equalizer. Thus, the equalizer simply attempts to realize the channel inverse response, and hence, mitigate ISI. Since the equalizer response is highpass (inverse of the lowpass channel response), it raises system noise degrading system SNR. This noise enhancement effect becomes more severe as transmission rates are pushed up to frequencies where the channel response becomes more and more lossy — alternatively when higher ISI is present. For this reason, the DFE structure has been preferred. This structure consists of a feedforward equalizer (FFE) and a feedback equalizer (FE) both of which are T -spaced transversal filters. The FE is used to cancel interference or ISI (also termed echo) from symbols which have already been detected. Thus, the weights of the FE are simply the samples of the tail of the system impulse response including the channel and the FFE. The FFE functions to remove some ISI, mostly that due to symbols which have not been detected as yet, hence it does not need to completely track the channel inverse response. Consequently, system noise enhancement is not as severe as for the T -spaced

2. Actually, this configuration filters out the median of input signal, but for most input statistics the median approximates the mean.

equalizer. Since the output of the FE is a weighted sum of noise-free past decisions, the feedback coefficients play no part in determining the noise power at the output.

One of the problems with transversal and decision feedback equalizer structures is the fact that they run at the baud rate and result in aliasing in the output spectrum. If the input signal bandwidth is non-zero at frequencies above $\frac{1}{T}$, the signal spectrum at the output of the sampler (equalizer input) will be folded about the frequency $\frac{1}{T}$. While this artifact of sampling is acceptable in the ideal case since only the input signal value at the sampling instants is important, sampler jitter results in phase errors in the aliased components. This effect can lead to nulls in the input spectrum for which the equalizer will be forced to correct. Consequently, noise enhancement becomes severe and system performance degrades. At higher frequencies sampler jitter becomes relatively more significant, and so, in practice fractionally-spaced equalizers (FSEs) are employed. In an FSE, the delay lines are placed at intervals which are a fraction of the sampling time (usually 1/2). In this case, aliasing is reduced and sampler jitter does not affect spectral response.

Continuous-time equalizers, like T -spaced equalizers, attempt to realize the channel inverse response up to the signal bandwidth of interest by providing high-frequency boost. Typically, equalizer zeros are placed to cancel the poles introduced by the channel in the signal bandwidth. Above this bandwidth, equalizer poles are placed to roll off the overall response, and thus, limit noise enhancement. The problem with an analog solution, however, is the deviation in filter response due to process and temperature variations. On the other hand, all equalizers are rarely of fixed response as they must track channel variations. Therefore, the majority of commercial equalizers are programmable. Thus, there is a growing interest for analog adaptive equalizers for high-speed data communications.

2.4 Summary

In this chapter, the relevant background material was presented. Specifically, we looked at the mechanisms which impair transmission over copper cables and the required filtering for reducing the effects of these degradations. We noted that copper transmission is currently below Shannon's theoretical limits, hence showing that by using more sophisticated filtering techniques, the copper channel can well serve foreseeable high speed applications. Finally, a brief review of state-space filters, adaptive filters, and equalizers was given to familiarize the reader with the concepts used throughout this thesis.

2.5 Appendix 2.1

The Shannon limit in (2.5) for infinite bandwidth signalling over a copper channel can be shown to be given by the following relationship.

$$C_{SH} = \int_0^{\infty} \log_2 \left[1 + \frac{|H_c(f)|^2 P_s(f)}{|H_x(f)|^2 P(f) + N(f)} \right] df \quad (\text{A2-1})$$

Here, it is assumed that the source of crosstalk, $P(f)$, is a transmitter whose power spectral density is similar to that produced by the information originating source, $P_s(f)$. The solution for (A2-1) gives the capacity for the channel in question. However, to obtain capacity one must use accurate models for the channel attenuation characteristics, the channel crosstalk behavior, and choose the optimal signalling spectrum. To solve (A2-1), we make use of the approximate models in (2.1) and (2.4). In addition, when we later solve for a noise dominated channel, a flat input signal spectrum is assumed. Since an optimum signal spectrum would be one obtained using the "water pouring" concept [Kalet 90], the results obtained here are slightly pessimistic. Hence, we will refer to the obtained rates as "maximum channel rate" rather than "channel capacity".

For the copper channel, substituting (2.1), (2.3) and (2.4) into (A2-1), we obtain

$$C_{SH} = \int_0^{\infty} \log_2 \left[1 + \frac{e^{-\alpha l \sqrt{2f}} P_s(f)}{K_n f^{3/2} P_s(f) + N_o} \right] df \quad (\text{A2-2})$$

Consider first the typical case where the NEXT dominates noise (i.e. $K_n f^{3/2} P_s(f) \gg N_o$). In this case, it can be noted that the signal power spectral density does not contribute to channel capacity since (A2-2) can be approximated by

$$C_{SH_{NEXT}} = \int_0^{\infty} \log_2 \left[1 + \frac{e^{-\alpha l \sqrt{2f}}}{K_n f^{3/2}} \right] df \quad (\text{A2-3})$$

Alternatively, in the absence of NEXT and assuming an unlimited flat signal power spectral density $P_s(f) = P_o$, we obtain

$$C_{SH_{AWGN}} = \int_0^{\infty} \log_2 \left[1 + \frac{e^{-\alpha l \sqrt{2f}} P_o}{N_o} \right] df \quad (\text{A2-4})$$

Both (A2-3) and (A2-4) can be solved numerically for different cables to provide the theoretical limitations on maximum channel rate for infinite bandwidth signalling.

Since unlimited signalling bandwidth is not a practical possibility, one can assume an effective bandwidth, F_{eff} , above which signal power spectral density is negligible. In addition, we also assume that the signal to interference power spectral density ratio (SIDR), the term S/I in (2.5), is significantly larger than unity which is a reasonable assumption if the detector is to detect the data reliably. In the presence of only NEXT, we obtain

$$C_{SH_{NEXT}}(F_{eff}) = \int_0^{F_{eff}} \log_2 \left[\frac{e^{-\alpha l \sqrt{2f}}}{K_n f^{3/2}} \right] df \quad (\text{A2-5})$$

The solution of (A2-5) yields

$$C_{SH_{NEXT}}(F_{eff}) = F_{eff} \left(\log_2 \left[\frac{|H_c(4/9F_{eff})|^2}{|H_x(4/9F_{eff})|^2} \right] + 0.4092 \right) \quad (\text{A2-6})$$

where we define the signal to NEXT ratio inside the logarithm operator in (A2.8) as SNXR.

Similarly, in the presence of noise only, it can be shown that (A2-4) reduces to

$$C_{SH_{AWGN}}(F_{eff}) = F_{eff} \log_2 \left[\frac{|H_c(4/9F_{eff})|^2 P_o}{N_o} \right] \quad (\text{A2-7})$$

CHAPTER 3

Adaptive Tuning Algorithms

A key difficulty in analog adaptive filters is the extraction of the error and gradient signals which are used by the LMS algorithm to tune the filter. This Chapter investigates new techniques for tuning analog adaptive filters used in various applications. Focus is placed on simple techniques that avoid the need for a training sequence. In this manner, on-line blind adaptation is possible and adaptation circuit overhead is kept to a minimum.

The techniques presented here are all descendents of one basic idea — the use of known signal characteristics at certain time instants and applying a curve fitting procedure to optimize filter response. Specifically, comparators are used to determine the sign difference between filter outputs and expected signal behavior at certain time instants to obtain the required error signal for adaptation as discussed in Section 2.3.2. Two adaptation philosophies are then adopted. The first involves obtaining a 1-bit error signal for *each* filter parameter being tuned. In this manner, separate coefficient gradient signals are not required and the adaptation algorithm is achieved by integrating each 1-bit error signal using an up/down counter and a DAC. Unfortunately, this approach becomes more difficult to achieve as the number of parameters increases. Hence, in the second approach, a *single* 1-bit error signal is also obtained using the same curve fitting approach and a multiplexor together with an integrator are used to correlate the error signal with the coefficient gradient signals to implement a general adaptation algorithm. It should be noted here that while these curve-fitting approaches allow

a simplified on-line blind adaptation, they require a restricted range of possible inputs and are most applicable for tracking minor process and channel variations. Inputs in this category are found in data communication applications where the filtered outputs at certain time instants are known. In addition, the linearity requirements of these applications is moderate (about 20-30dB, as found in Chapter 2) which is achievable using the filter circuit technology adopted herein.

Four examples are discussed to determine and demonstrate the general applicability of the underlying concepts:

- An adaptive pulse-shaping filter for which pole frequency and Q -factor are adapted while gradient computation is avoided. Two sample measurements are made to obtain two error signals to tune the two filter parameters.
- A second-order cable equalizer whose zero-frequency and DC gain are adapted by computing two error signals for each parameter tuned while the poles are fixed. As well, the adaptation avoids the need for gradient signals, thus, simplifying the algorithm circuitry.
- A fourth-order cable equalizer whose poles are fixed and whose zeros are adapted. In this example, coefficient adaptation is based on the correlation of an error and gradient signals.
- A sixth-order adaptive equalizer used to shape the read signal in a typical data retrieval system into a class-four, partial-response signal. Here, again, an error signal together with coefficient gradient signals are used for adaptation.

Finally, while simulation results should provide a first check, it is preferable to obtain experimental results to verify the theory and to demonstrate that the method is robust enough to tolerate practical impairments. Thus, for the sake of brevity, the simulation results for the pulse-shaper will not be provided as the experimental results of a prototype system are presented in Chapter 5. For the three other application examples, we do not as yet have experimental results, hence, demonstration of the adaptation techniques will be based on simulations.

3.1 Introduction to “eye” diagrams

A very effective method of measuring distortion in a transmission system is based on the *eye pattern*. Since this indicator is adopted in this thesis, the concept of “eye” patterns warrants a brief introduction at this point. An “eye” pattern can be viewed on an oscilloscope if the bit rate is used to trigger the horizontal sweep while the bit stream is supplied to the vertical deflection plates. For shaped NRZ data, the distinctive pattern that will be viewed is shown in Figure 3.1 for an ideal system.

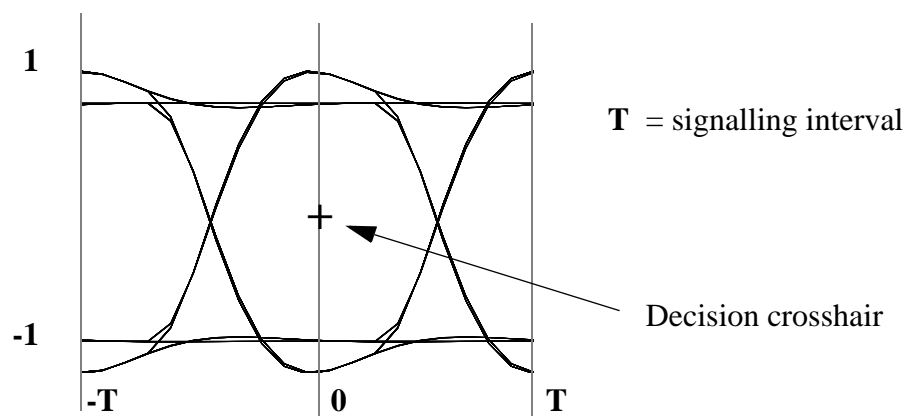


Figure 3.1: Eye diagram for NRZ data.

The decision making process (slicer) in the receiver can be represented by crosshairs in each “eye” as illustrated in the figure. The vertical hair represents the decision time, while the horizontal hair represents the decision level. To detect the data without error, the “eyes” must be open, meaning a decision area must exist within the open “eye”. The effect of practical degradations of the pulses is to reduce the size of the ideal “eye” as shown in Figure 3.2. A measure of margin against error is the minimum distance between the crosshair and the edges of the “eye”. These degradations usually fall into the two categories of amplitude distortion and timing distortion (also known as isochronous distortion) corresponding to vertical and horizontal displacement, respectively. Amplitude distortion results from ISI and echoes, and is represented by ΔA in Figure 3.2. Timing distortion arises from static decision time

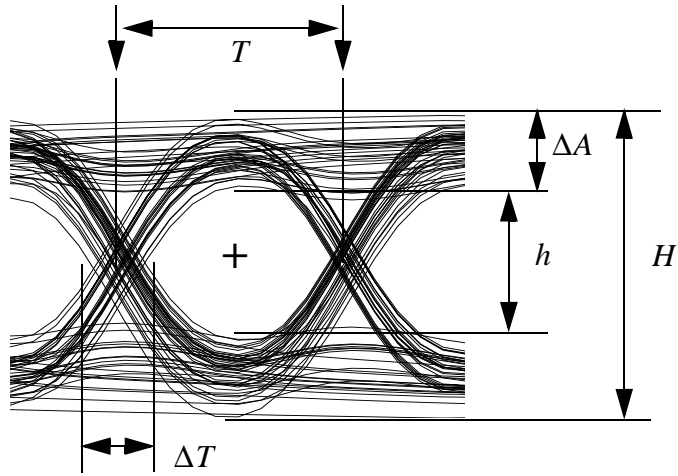


Figure 3.2: Illustrating the effects of degradation on eye quality.

misalignment, ISI, and jitter, and is represented by ΔT in Figure 3.2. These combined distortions affect the overall BER performance. Quantitatively, one can obtain the level of amplitude distortion from the resultant “eye” pattern as follows:

$$AD = \frac{H-h}{H} \cdot 100\% \quad (3.1)$$

while the SNR is affected accordingly

$$\Delta SNR = 20 \log \left[\frac{h}{H} \right] \quad (3.2)$$

Isochronous distortion (or peak-to-peak percentage jitter) is defined as

$$ID = \frac{\Delta T}{T} \cdot 100\% \quad (3.3)$$

Observe that for optimal “eye” opening both ΔA and ΔT must be minimized. For more information on “eye” patterns, the reader is referred to [Bell 70] and [Tugal 89].

3.2 Adaptive Pulse Shaping

Recall from Section 2.1.1 that in meeting EMI regulations a transmit pulse-shaping filter is required and the filtered output must conform to a time domain mask as illustrated in Figure 2.3. This application lends itself to our basic tuning strategy. For data communication signalling, the filtered output resembles the step response of the filter. Consider a second-order filter, or biquad, whose lowpass and bandpass transfer-functions are:

$$T_{LP}(s) = \frac{K\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \quad (3.4)$$

$$T_{BP}(s) = \frac{K\omega_o s}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \quad (3.5)$$

The step response (lowpass output) for this biquad can be shown to be

$$y_{LP}(t-t_o) = KV_{PP} \left(1 - \frac{1}{\sqrt{1 - \frac{1}{4Q^2}}} e^{-\frac{\omega_o}{2Q}(t-t_o)} \cos \left[\sqrt{1 - \frac{1}{4Q^2}} \omega_o(t-t_o) - \phi \right] \right) + y_{LP}(t_o) \quad (3.6)$$

for $Q > 0.5$ where V_{PP} represents the peak-to-peak step voltage, Q the biquad Q -factor and ω_o represents the filter bandwidth. The quantity ϕ is

$$\phi = \tan^{-1} \left[\frac{1}{2Q \sqrt{1 - \frac{1}{4Q^2}}} \right] \quad (3.7)$$

It is apparent from (3.4-3.7) that the step response for this biquad is characterized by the parameters ω_o , Q and K . For a given gain term, K , the tuning algorithm must extract and process ω_o and Q from the filter output(s).

3.2.1 Adaptation of Filter f_o

The biquad's parameters ω_o and Q also define the filter group delay. Thus, the lowpass output waveform (step response) will not only be shaped but delayed from the input as depicted in Figure 3.3. Also shown in Figure 3.3 is the time-domain template for the output pulse that must be satisfied. Observe that the lowpass output zero-crossing (also the mid-point

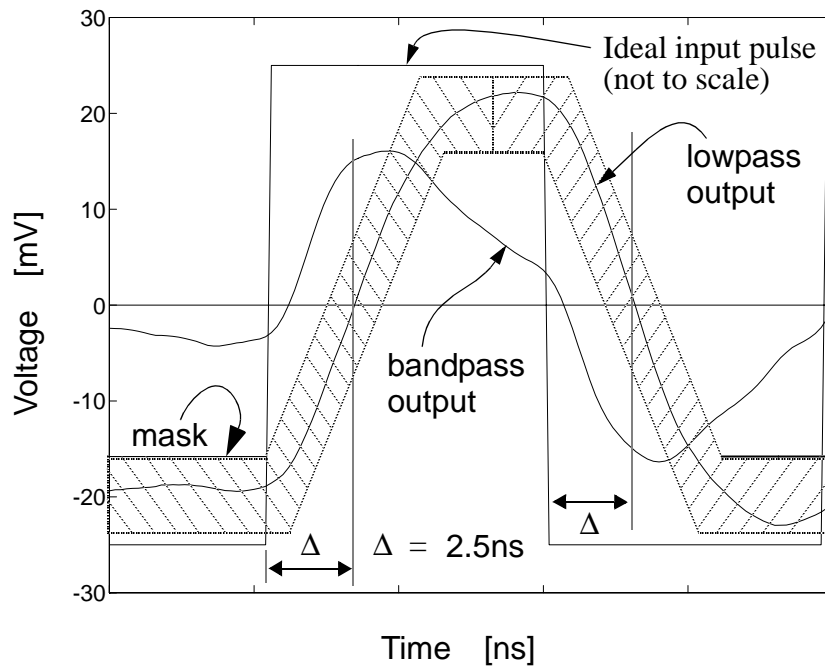


Figure 3.3: Lowpass and bandpass biquad outputs for 100Mb/s NRZ data.

transition for differential signalling) is delayed from the input zero-crossing. This delay, Δ , is inversely related to both ω_o and Q . To adapt the filter ω_o (or f_o), an error signal relating to the pole frequency must first be obtained. We propose to obtain this error signal by comparing (using a clocked comparator) the time of occurrence of the filter output zero-crossing to the nominal zero-crossing time. In our case, this nominal zero-crossing time occurs 2.5ns after a data transition. This 1-bit error signal is then integrated using an up/down counter whose output is fed to a DAC that controls the f_o coefficient.

Zero-crossing delay versus filter pole frequency for different Q values is shown in Figure 3.4. For constant Q , notice that the relationship between ω_o and Δ is monotonic, thus, simply

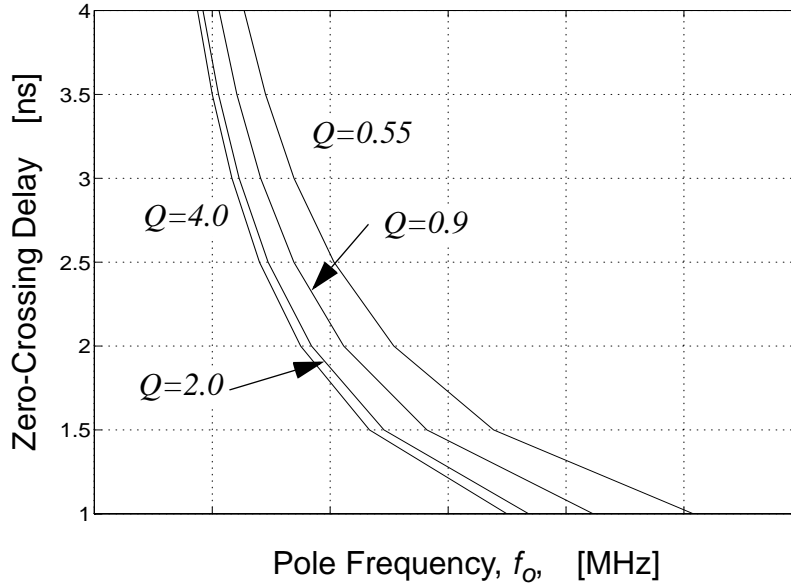


Figure 3.4: Zero-crossing delay as function of f_o and Q .

monitoring delay time is sufficient to determine whether the pole frequency is in error. For example, as shown in Figure 3.5, a filter mistuned too fast ($f_o > f_{o,opt}$) will exhibit an output zero-crossing that is early ($\Delta < \Delta_{opt}$) while a filter mistuned too slow ($f_o < f_{o,opt}$) will exhibit a zero-crossing that is late ($\Delta > \Delta_{opt}$) where $f_{o,opt}$ and Δ_{opt} are the optimal filter pole frequency and delay, respectively. The monotonic relationship in Figure 3.4 also guarantees that only a single solution for a given ω_o , Δ pair exists at a particular filter Q . Observe that the adaptive algorithm error signal can be simply obtained by computing the time difference between Δ_{opt} and Δ . It should be mentioned, however, that for the special case where f_o is mistuned extremely fast and Q mistuned extremely high, a condition where more than one zero-crossing in the output pulse may occur resulting in a non-monotonic relation, and hence, a local minimum in the adaptation performance.

Since the relationship between pole frequency and delay time is monotonic, the sign of the error signal is sufficient to determine in which direction to tune the pole frequency from its mistuned location. Therefore, the gradient signal is not required allowing a simplified algorithm. The algorithm can be further simplified by using the SE-LMS algorithm as follows. In Figure 3.5 we show the biquad differential lowpass output for two mistuned

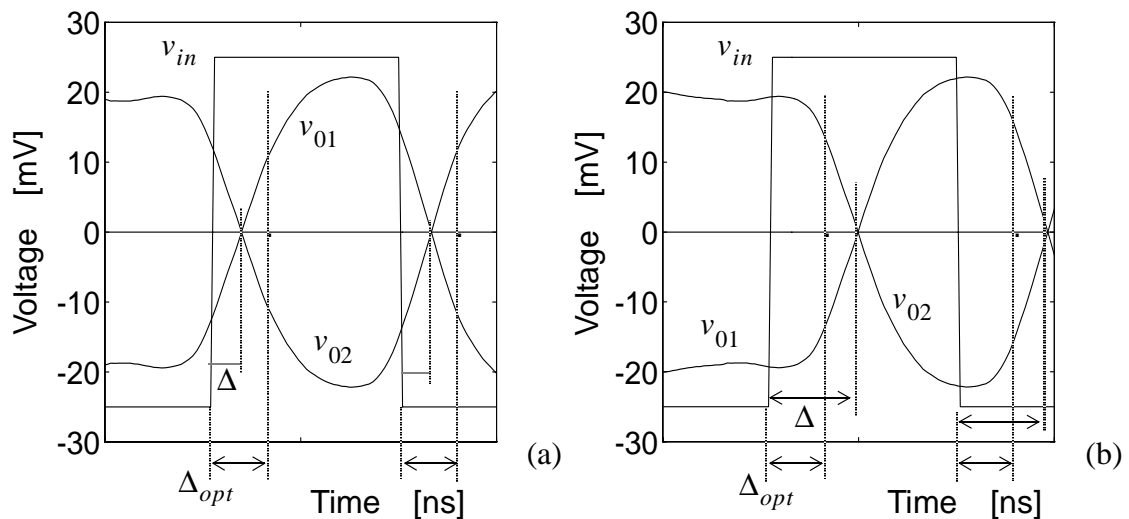


Figure 3.5: Illustrating the details when the filter is mistuned: (a) too fast; zero-crossing comes early and (b) too slow; zero-crossing comes late.

cases as well as the location of the optimal zero-crossing for the outputs. Consider the low-to-high (LH) transition of the data pulse in Figure 3.5a. To obtain the error signal relating to f_o , we compare v_{o1} to v_{o2} at the nominal delay time using a clocked comparator. In other words, we evaluate the $\text{sgn}[e_{f_o}(k)] = \text{sgn}[v_{o1}(t) - v_{o2}(t)]$ where $e_{f_o}(k)$ is the f_o error signal. Note that the time index k does not represent successive system clock periods, but instead, represents successive comparator clock sample instants which take place 2.5ns after the occurrence of data transitions. For the case in Figure 3.5a, the result of this comparison yields a digital “1”. This result means the filter is mistuned too fast and f_o should be decreased. Using a binary set of ± 1 and defining $F_o(k)$ to be a digital word applied to a DAC which controls the filter pole-frequency, the algorithm can be accomplished by evaluating the following expression for each data transition.

$$F_o(k+1) = F_o(k) + data(k) \oplus \text{sgn}[e_{f_o}(k)] \quad (3.8)$$

Here, the symbol \oplus denotes an “exclusive-OR” gate and the summation is implemented using an up/down (U/D) binary counter. This expression is evaluated for both a LH and high-to-low (HL) transition of the data stream, as in Table 3.1, and provides equivalent actions for both transitions under ideal conditions (see last column in Table 3.1). The length of the counter controls the integration time constant or convergence time. The DAC provides analog DC updates for the coefficient; the resolution of which governs the size of the steady-state limit cycle about the optimal coefficient value once convergence is attained. A discussion of these issues can be found in [Shoval 92].

Table 3.1: Truth table for comparator outcomes and resultant tuning information.

sgn[e(k)] for LH trans.	data(k)	result of \oplus	sgn[e(k)] for HL trans.	data(k)	result of \oplus	bit-time result of \oplus
1, (early)	1	-1	-1, (early)	-1	-1	-1-1
-1, (late)	1	1	1, (late)	-1	1	1,1

3.2.2 Adaptation of Filter Q

Observe from Figure 3.4 that delay time is a function of both filter pole-frequency and filter Q -factor. Hence, if the filter Q -factor is in error, the algorithm may converge to an incorrect value for f_o . Moreover, a mistuned Q value will result in signal shape variations (i.e. ringing when Q is high) which could violate the mask set out in Figure 3.3. For both these reasons, the filter Q -factor must also be tuned for a better curve fitting of the step response. To adapt filter Q , an error signal relating to filter Q must be extracted. To obtain this signal, we propose to compare the bandpass filter output at the same nominal zero-crossing time (2.5ns after a data transition) against some target reference level using a clocked comparator. As will be explained next, the bandpass output will exhibit a peak level, in the vicinity of the lowpass output zero-crossing, that dominantly depends on filter Q . Hence, the comparison is

sufficient to obtain an error signal that relates to filter Q . As in the f_o case, this 1-bit error signal is digitally integrated and the result is used to drive a DAC which controls the filter- Q .

The rate of change (slope) of the step response in (3.6) rises as the lowpass output increases and falls as this output reaches steady-state. In between, the slope will attain a peak level that will occur approximately when the filter output pulse crosses zero as can be noted from Figure 3.3. The slope output represents the biquad impulse response and can be easily obtained from the bandpass output which for a step input is

$$y_{BP}(t-t_o) = KV_{PP} \left(\frac{1}{\sqrt{1-\frac{1}{4Q^2}}} e^{-\frac{\omega_o}{2Q}(t-t_o)} \sin \left[\sqrt{1-\frac{1}{4Q^2}} \omega_o(t-t_o) \right] \right) + y_{BP}(t_o) \quad (3.9)$$

In Figure 3.6 the bandpass peak level, $V_{BP,PK}$, versus Q for different f_o values is

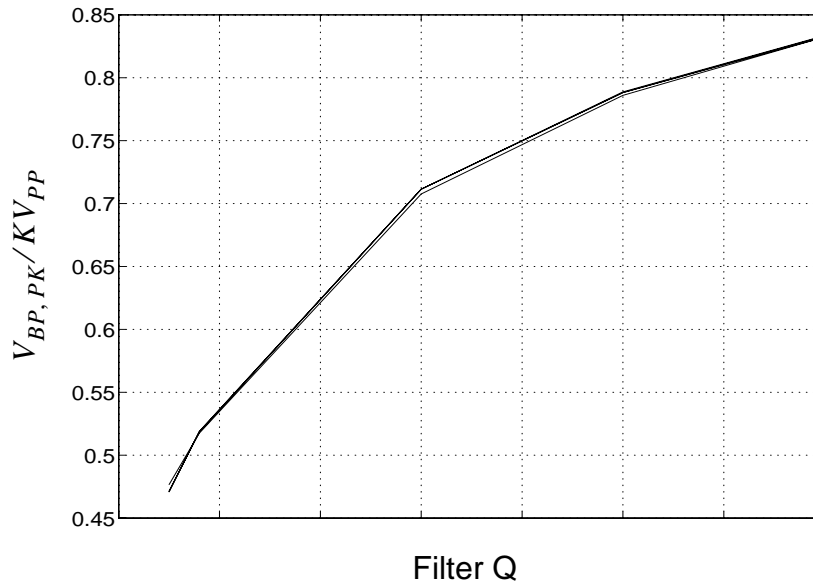


Figure 3.6: Bandpass peak level versus Q for $f_o = 10, 85, 100,$ and 200MHz .

plotted. Observe that the peak amplitude dominantly depends on Q and that once again a monotonic relation occurs between $V_{BP,PK}$ and Q . Hence, simply comparing the bandpass

output, $v_{o, bp}$, to a reference level, V_{REF} , at the optimal delay time is sufficient to determine the Q error signal, $e_Q(k)$, and the tuning direction without the need for a gradient filter. As before, based on the compared outcome, an U/D counter and a DAC can be used to automatically adapt the Q coefficient. Quantitatively, for differential signalling with $Q(k)$ the digital word applied to the DAC controlling filter Q , we have:

$$e_Q(k) = \left\{ \begin{array}{l} \left(\frac{V_{REF}}{2} - \frac{v_{o, bp}}{2} \right) - \left(\frac{-V_{REF}}{2} - \frac{-v_{o, bp}}{2} \right) = V_{REF} - v_{o, bp} \Leftrightarrow v_{o, bp} > 0 \\ \left(\frac{-V_{REF}}{2} - \frac{v_{o, bp}}{2} \right) - \left(\frac{V_{REF}}{2} - \frac{-v_{o, bp}}{2} \right) = -V_{REF} - v_{o, bp} \Leftrightarrow v_{o, bp} < 0 \end{array} \right. \quad (3.10)$$

and

$$Q(k+1) = Q(k) + data(k) \oplus \text{sgn}[e_Q(k)]. \quad (3.11)$$

Recall that the time index k represents successive comparator trigger times and takes place 2.5ns after data transitions.

Finally, we would like to note that in the previous two sections it was assumed that only one parameter was being adapted while the other was at its optimal location. When both parameters are mistuned, the adaptation procedures are applied to both. Since the adaptive algorithm iteratively tunes the coefficients to minimize their respective error signals, the algorithm will converge to the desired location. However, the convergence time will be somewhat longer than that attainable if it were possible to adapt the coefficients independently.

The system architecture for both f_o and Q tuning is shown in Figure 3.7.

3.2.3 DC-Offset Effects

It is known that DC offset in the adaptation algorithm leads to a residual mean-squared error. In other words, the coefficients converge to a non-optimal location that depends on the nature of the offset. This biased estimate results in a filter output error with respect to the

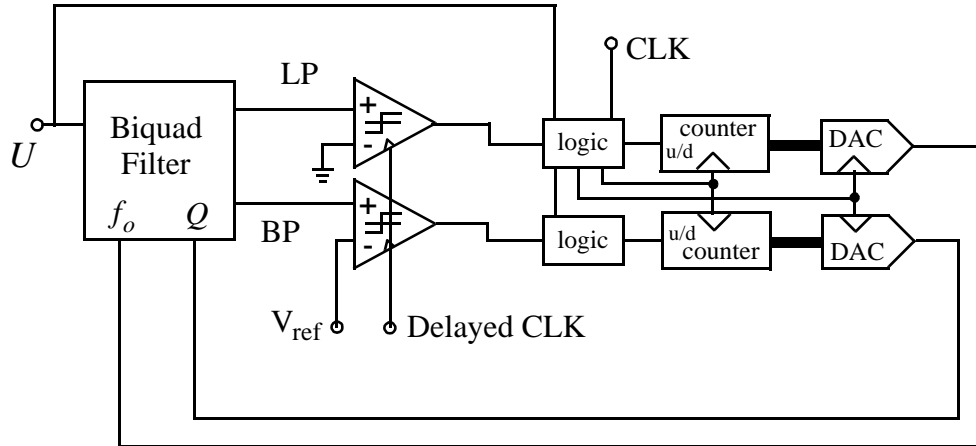


Figure 3.7: Block diagram of the f_0 and Q tuning architecture.

optimal filter output. The degradation, or residual MSE, due to various DC offset sources for different algorithm possibilities is analyzed in Chapter 6. Since most of the adaptation algorithm described above is digital, a single offset source can be lumped at the input of the comparators which models comparator input offset, signal differential bias, and filter-to-comparator interface circuit offset. Thus, the effect of this offset source on the proposed tuning algorithms for the pulse-shaping biquad is addressed in this section. As well, solutions to mitigate its effect are considered in Section 3.2.4.

Consider the f_0 -tuning scheme. There are two types of offsets: common-mode offsets and differential offsets. Since the comparator output depends on the difference between the two filter half-circuit outputs, any common-mode offset will not cause error. However, this feature is not the case for a differential offset. Consider Figure 3.8 in which a data pulse is shown together with the nominal outputs (with $v_{01,nom}$ dotted) and an offset-biased output for both a filter mistuned slightly fast and slightly slow. The offset alters the symmetry in the location of the zero-crossing between a LH transition and a HL transition of the input data. For example, in Figure 3.8a where the filter is mistuned too early, for a LH transition, the zero-crossing is early as it should be, while for a HL transition, the zero-crossing is late which

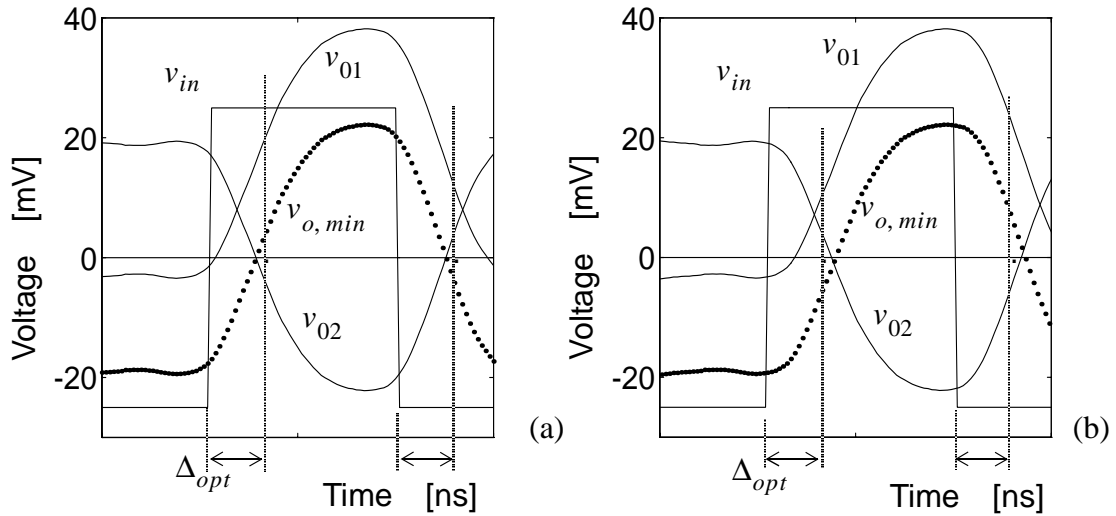


Figure 3.8: Effects of DC offset for a filter slightly mistuned (a) fast, (b) slow.

is in error. This asymmetry will result in inconsistency in the decision defined by (3.8) between consecutive data transitions. Consequently, the net effect per data bit cancels (i.e. one “-1” and one “1”) and the U/D counter will not advance in either direction. When this happens, the coefficient controlling f_o will stabilize at an incorrect location.

The effect of DC offset will be manifested when the filter f_o is near the nominal location such that the term $\Delta_{opt} - \Delta$ is small and the offset term dominates. When the term $\Delta_{opt} - \Delta$ is large, observe from Figure 3.8 that the algorithm will yield a correct response. Therefore, the convergence behavior for the f_o coefficient will take one of two possible trajectories depending on its initial value as shown in Figure 3.9 resulting in a non-reachable dead-band about the optimal coefficient value. Notice that this dead-band is a consequence of using the SE-LMS algorithm.

For the Q tuning mechanism, observe that if the comparisons in (3.10) are obeyed, any common-mode offset between the common-mode level of the signal $v_{o,bp}$ and V_{REF} will be cancelled and will not lead to errors in Q adaptation. Differential offset, however, will lead to

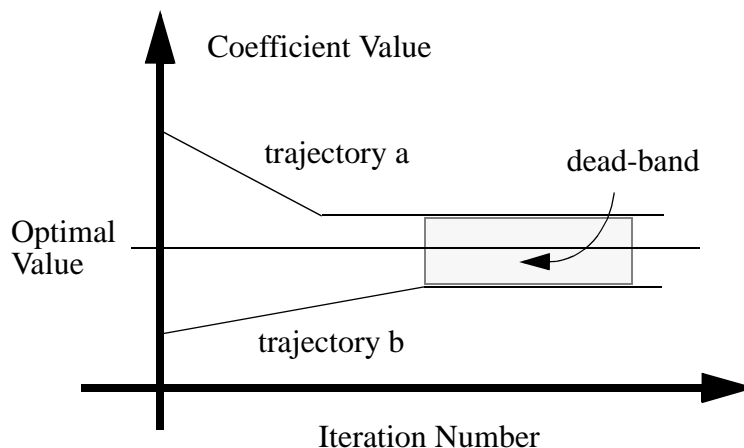


Figure 3.9: Coefficient trajectory for two different initial values.

inconsistency between resultant actions for the data transitions and lead to the same dead-band convergence behavior discussed above.

3.2.4 Some Solutions to the Offset Problem

The previous section discussed potential problems with the algorithm due to DC offsets. In this section, some techniques to overcome these problems are proposed.

Consider the f_o adaptation. It is possible to let the algorithm locate the dead-band as follows. Once inconsistent data as discussed in Section 3.2.3 is produced, the algorithm is to force the coefficient update in the same direction the update exhibited when consistent data was obtained. This procedure will continue until the coefficient reaches the other limit of the dead-band. At this point, the algorithm will start producing consistent outputs and drive the coefficient update in the opposite direction and the coefficient will once again enter the dead-band (but from the other extreme). The coefficient update will now continue in the same direction until the coefficient reaches the previous dead-band extreme. This process will continue and a limit cycle will be formed about the optimal coefficient value whose size will depend on the dead-band (effectively the amount of offset) and not the resolution of a single DAC LSB as would be the ideal case. Observe that the larger steady-state limit cycle for the

coefficient about its optimal value will result in f_o jitter that will correspond to zero-crossing jitter in the time domain, and hence, distortion. To eliminate the jitter effect, one can freeze the DAC in the middle of the dead-band once the limit cycle is detected. However, it is preferable to compensate for the offset directly.

For example, given knowledge of the transmit data and the inconsistent comparator outputs, it is possible to detect the offset error and apply a correction adaptively via a bias tap at one of the differential outputs. This solution makes use of the same tuning idea, but the unknown parameters are the DC offsets on the lowpass and bandpass outputs. Quantitatively, one must implement the following algorithm

$$V_{off}(k' + 1) = V_{off}(k') + \text{sgn}[e_{f_o}(k)] \wedge \text{sgn}[e_{f_o}(k - 1)] \quad (3.12)$$

where $V_{off}(k')$ is a digital word applied to a DAC that provides an offset term to v_{01} and \wedge represents a “NAND” gate. The time index k' indicates successive times for which the up/down counter is updated (i.e. for inconsistent zero-crossings) which occurs only when

$$\{data(k) \oplus \text{sgn}[e_{f_o}(k)]\} \oplus \{data(k - 1) \oplus \text{sgn}[e_{f_o}(k - 1)]\} = 1 \quad (3.13)$$

Similar procedures can be extended to the coefficient controlling filter Q .

3.3 Adaptive Cable Equalization

As mentioned in Chapter 2, equalization is used to combat ISI arising from the lossiness of the transmission channel. In Figure 3.10, a graphical illustration of the effect of equalization in the frequency domain is given. As can be inferred, the equalizer provides high-frequency gain to compensate for high-frequency channel loss. The result is an overall flat spectrum up to the signal bandwidth of interest. Above this bandwidth, the overall spectrum rolls off with frequency to prevent noise enhancement.

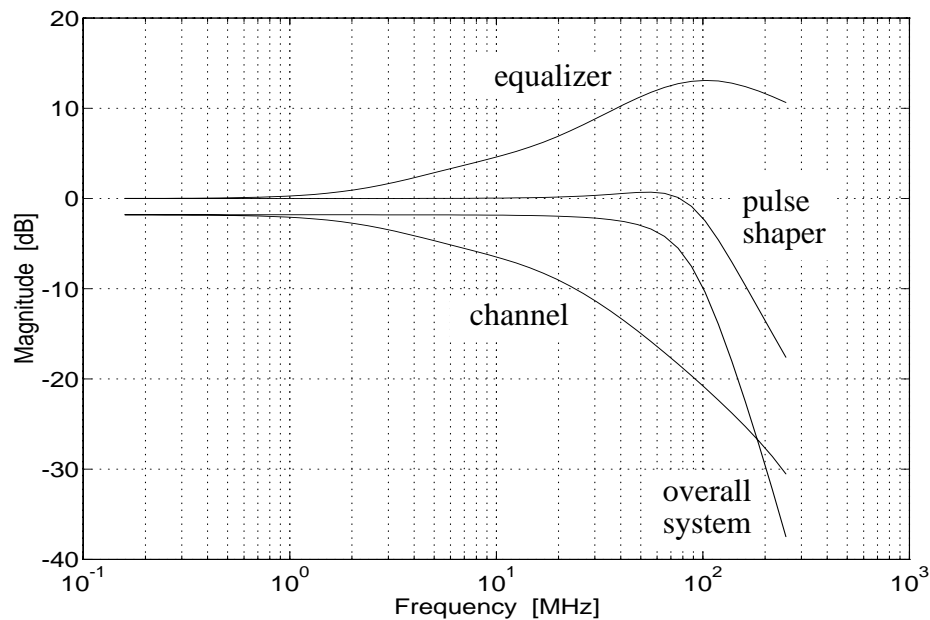


Figure 3.10: Illustrating the effects of equalization in the frequency domain.

Since the channel response varies with cable length, temperature, cable make-up, and load conditions as discussed in Section 2.1.2, an adaptive equalizer is required to track these variations. To adapt such an equalizer, we propose to make use of the same curve fitting approach at certain time instants in obtaining an error signal for adaptation. The general system architecture we propose to implement is shown in Figure 3.11. In the figure, a clocked comparator¹ is used to obtain the error signal. This comparator is triggered at certain time instants that are synthesized from the main clock in the “clock mux” block which is controlled by the “LOGIC” block. The reference level template (DAC²) is addressed by the “LOGIC” block as well, and hence, arbitrary reference levels can be selected. The “LOGIC” block, which controls the sample instants, can be decision directed (i.e. based on current and past data detected) as will be discussed in Sections 3.3.2 and 3.3.3. The “S/H” block may be required depending on the input requirements of the “LOGIC” block and the number of comparators used. Finally, the error signal is applied to the “LMS” block. The “LMS” block can use the

-
1. More than one comparator with different trigger times for each can be used to obtain the error signal at these various time instants if speed limitation is critical.
 2. A number of DACs to provide different reference levels can be used if speed limitation is critical.

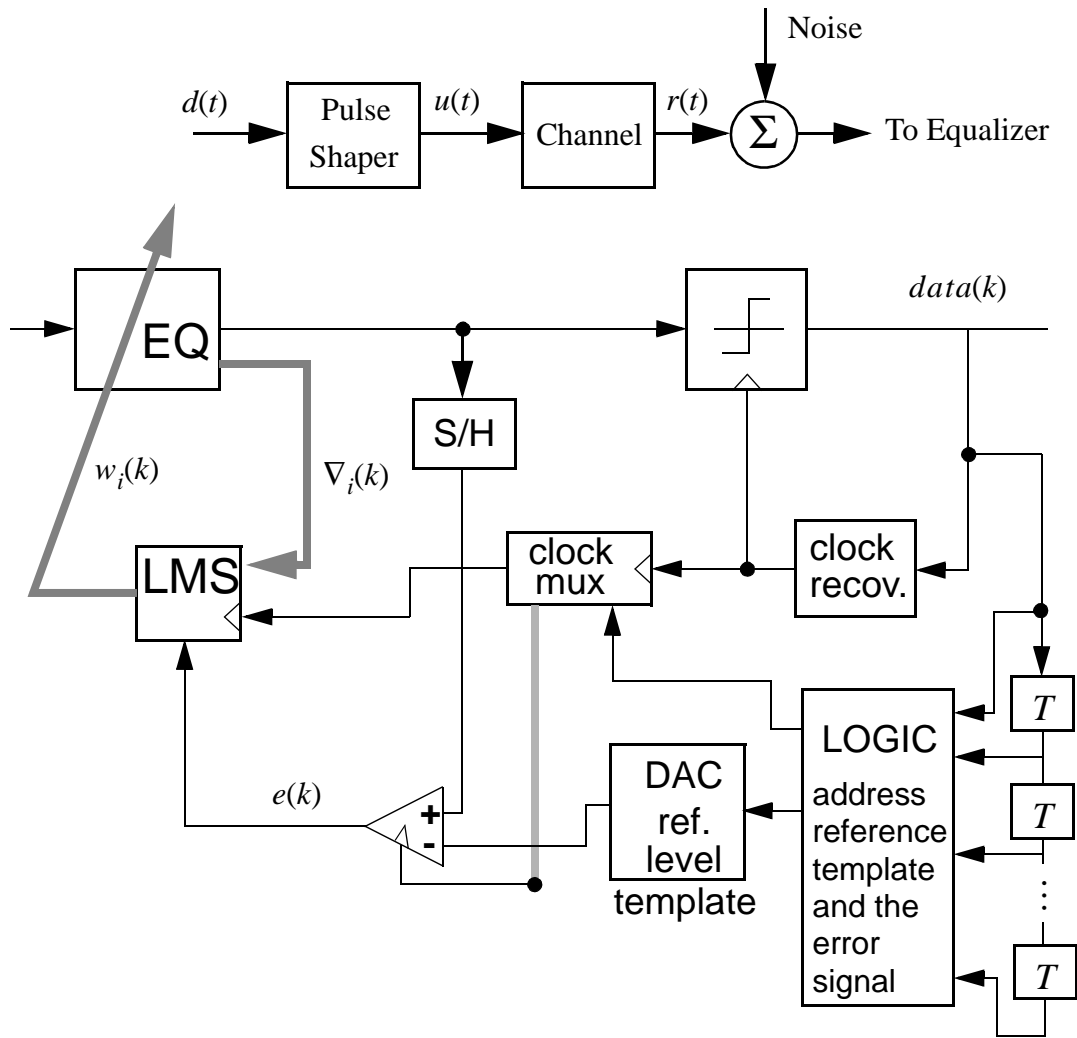


Figure 3.11: Proposed architecture for analog adaptive equalization.

error signal alone to adapt its respective filter parameter as discussed for the pulse-shaper and as will be discussed for the equalizer in Section 3.3.2, or it can make use of the error and coefficient gradient signals to adapt any arbitrary matrix or vector element in the state-space representation of the equalizer as described in Section 2.3.2.

In this section, a second-order and a fourth-order equalizer for 100Mb/s NRZ transmission over UTP cables will be investigated through simulation studies. For the biquad equalizer, two error signals are obtained: one to adapt equalizer zero-frequency and one to adapt equalizer

DC gain. Each error signal is obtained by comparing the equalizer output in the middle of the “eye” (the optimal slicing time) against an expected reference level. The two poles are not adapted and are placed near the baud frequency. For the fourth-order equalizer, three zeros and the DC gain are adapted while the poles are fixed. Rather than obtaining a separate error signal for each equalizer parameter being adapted, an error signal is computed at mid “eye” and the adaptation algorithm makes use of the coefficient gradient signals, as discussed in Section 2.3.2, to implement the LMS update equation to adapt the \mathbf{c} vector of the state-space equalizer. This vector controls the three equalizer zeros and the equalizer DC gain.

Before continuing, one must develop a model for a typical channel so that simulation studies can be performed.

3.3.1 Channel Modelling

For simulation purposes, we make use of copper twisted-pair cables characterized by (2.1) and Table 2.2. Using an optimization technique in FiltorX [Ouslis 90], various filters were obtained that match the amplitude response in (2.1) over the frequency range 1MHz-200MHz. These filter orders for the particular cable, as well as their pole-zero constellations, are given in Table 3.2.

Table 3.2: Linear filter models for UTP cables.

Cable	Order	Gain Coeff.	Poles (MHz)	Zeros (MHz)
100m-UTP4	1	0.075342	11.4618	Inf
100m-UTP4	2	0.0816869	2.684665, 16.180144	4.28785, Inf
100m-UTP5	2	0.9616636	3.095411; 19.23127	5.029195, Inf

Table 3.2: Linear filter models for UTP cables.

Cable	Order	Gain Coeff.	Poles (MHz)	Zeros (MHz)
100m-UTP5	5	0.7193048	2.171920, 9.756244, 31.7516455 $244.71 \pm j68.53$	2.995241, 16.695528, Inf Inf, Inf
125m-UTP5	2	0.0596037	2.0112605, 11.542047	3.0952268, Inf
75m-UTP5	2	0.1765658	5.430133, 36.367724	9.2497188, Inf

3.3.2 A Biquad Equalizer

Popular on-chip tuning schemes employ a dummy biquad whose degrees of freedom are optimized and these parameters are copied onto the main filter. We will first consider this approach and propose an adaptive optimization procedure.

A biquad whose degrees of freedom are DC gain, two poles, and one zero (the other at infinity to limit noise) can realize the simplest equalizer. The high-frequency boost can be attained by placing a real-axis zero in the vicinity of the dominant channel pole-frequency. Typically, peak detection is used to automatically position this zero to compensate for skin effect. Therefore, good tracking between cable length (skin effect) and filter zero-frequency is required. With this approach, other losses such as transmit level errors or a power splitter somewhere in the cable path which can be thought of as ohmic loss would degrade tuning performance as filter zero-frequency would incorrectly attempt to track ohmic losses as well. Our idea for tuning the equalizer is more general and is an extension of the tuning techniques for the pulse-shaping filter. Here, we propose to automatically tune both the equalizer zero-frequency and equalizer DC gain to compensate for both skin effect and ohmic losses. The equalizer poles have a relatively low Q factor and are positioned near the baud rate, f_b . The exact location of the poles is not critical, and hence, their positions can be controlled using standard techniques³.

Choosing to tune two parameters, zero frequency and DC gain, simplifies the architecture of Figure 3.11. Specifically, it is possible to avoid gradient computation and extract all the required information solely from the error signals as follows. Consider the pulse-shaping filter output “eye” diagram in Figure 3.12 which would also be the equalizer output for optimal

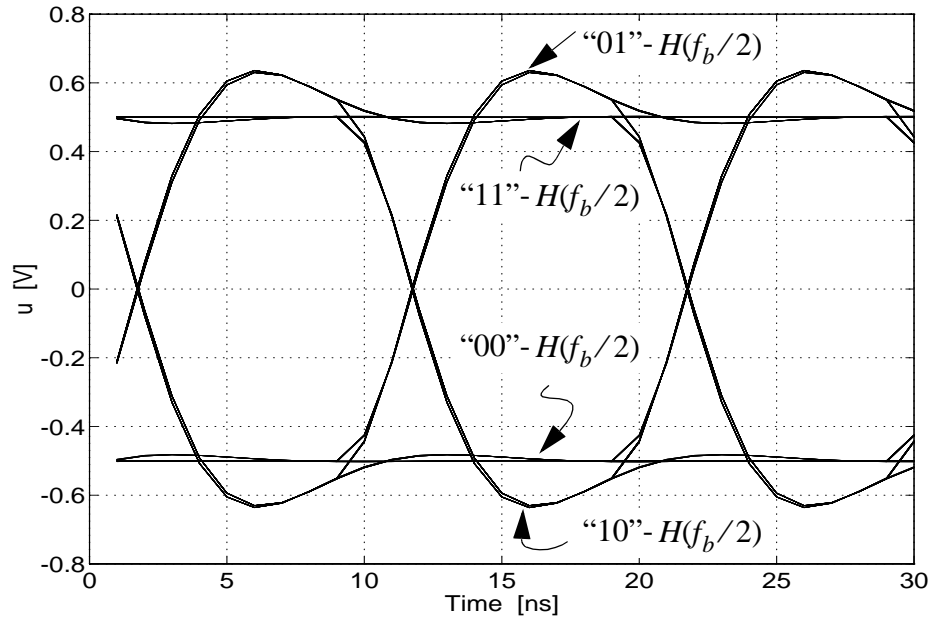


Figure 3.12: Pulse shaping filter output “eye” pattern.

equalization (i.e. flat response to f_b). This filter is a lowpass, second-order filter with a pole frequency, f_o , of 88MHz and a Q factor of 0.9. Observe that the system peak signal level at mid “eye” (also the optimal sampling instant) simply corresponds to the peak output level for a periodic data sequence at half the baud rate ($f_b/2$, i.e. the sequence 101010...). The system steady-state level can be obtained by monitoring the output level for a sequence that corresponds to an input of all ones or all zeros. Comparing these levels with a reference target level provides an error signal that can be used to adapt equalizer zero-frequency and equalizer DC gain. In the time domain, essentially two points of the biquad step response are being curve

3. For example, using an off-chip resistor and an on-chip tracking transconductor [Laber 93], or simply copying the pole frequencies of the pulse-shaping filter. Recall that in a typical transceiver, both filters are in close proximity.

fitted. What remains is the extraction of the two test patterns from the random output. For example, gating the error signal on detection of a “10” or “01” pattern provides a point measure on the overall attained peak level corresponding to an input at $f_b/2$ enabling tuning of equalizer zero frequency. To ensure low frequency spectral response flatness, gating the error signal on detection of an “x11” or “x00” pattern (where x is either “1” or “0”) as an estimate of the steady-state response allows tuning of equalizer DC gain. The gating operation is performed by the “LOGIC” block in Figure 3.11.

To test the idea, the above algorithm was implemented in “C” and the SE-LMS algorithm was employed. In addition, a phase-locked loop (PLL) was established for clock recovery. Basically, a clock was set up to run at 100MHz whose phase was adapted until the zero-crossing of the equalizer output data was aligned with the zero-crossing of the reference clock. To simulate analog functions, the system sampling rate was 1GHz which was also the speed of the phase comparator of the PLL.

As an initial test case, the first-order channel model for 100m UTP4 cables in Table 3.2 was used and the noise source was eliminated. The equalizer was the second-order system in Figure 2.9 with A_{ij} realizing the pole frequency and Q -factor copied from the pulse-shaper while $d = c_1 = 0$ and $c_2 = 1$. Note that in a practical transceiver both receiver and transmitter are in close proximity or even on the same chip. Hence, this approach of positioning equalizer poles is acceptable. The coefficients being adapted were b_1 and b_2 . To obtain the reference levels for the adaptation, the equalizer zero frequency was manually positioned to correspond to the channel pole frequency and the resultant “eye” diagram gave the levels 85mV and 120mV for the low-frequency and high-frequency reference levels, respectively. Since the channel consists of a single-pole filter, a single-zero equalizer should be sufficient to completely compensate for channel ISI. To test the idea, the equalizer was mistuned (zero at 4MHz) and then allowed to adapt. The initial equalizer output “eye” diagram is shown in Figure 3.13. After 30k iterations with an adaptation step-size of 0.0005, the system

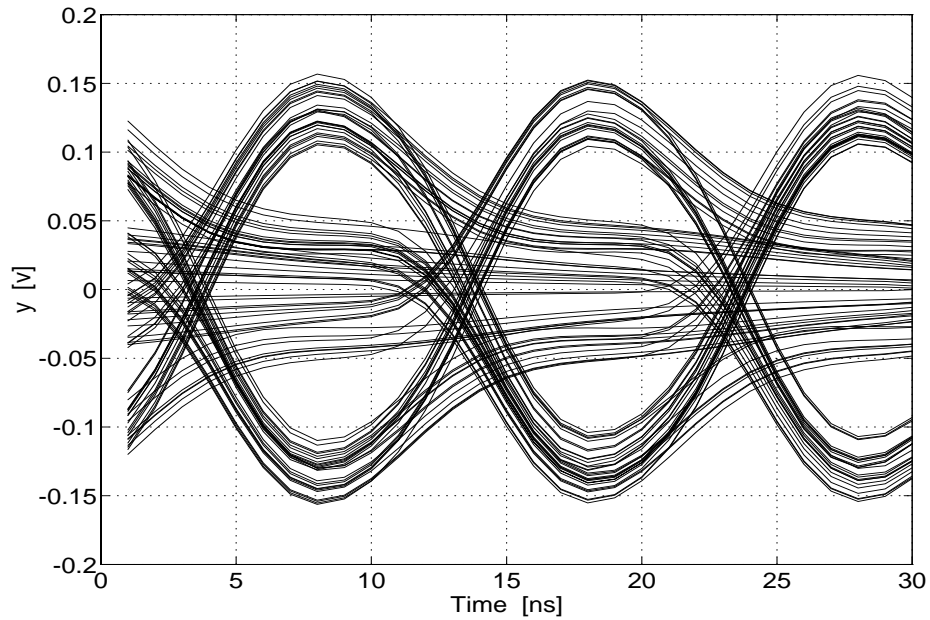


Figure 3.13: Initial equalizer output “eye” diagram for the first-order system.

converged with a residual MSE of -76dB and the zero frequency was at 11.5MHz which is comparable with the expected value of 11.46MHz in Table 3.2. The equalizer output “eye” pattern and the system constituent frequency responses are shown in Figure 3.14 and Figure

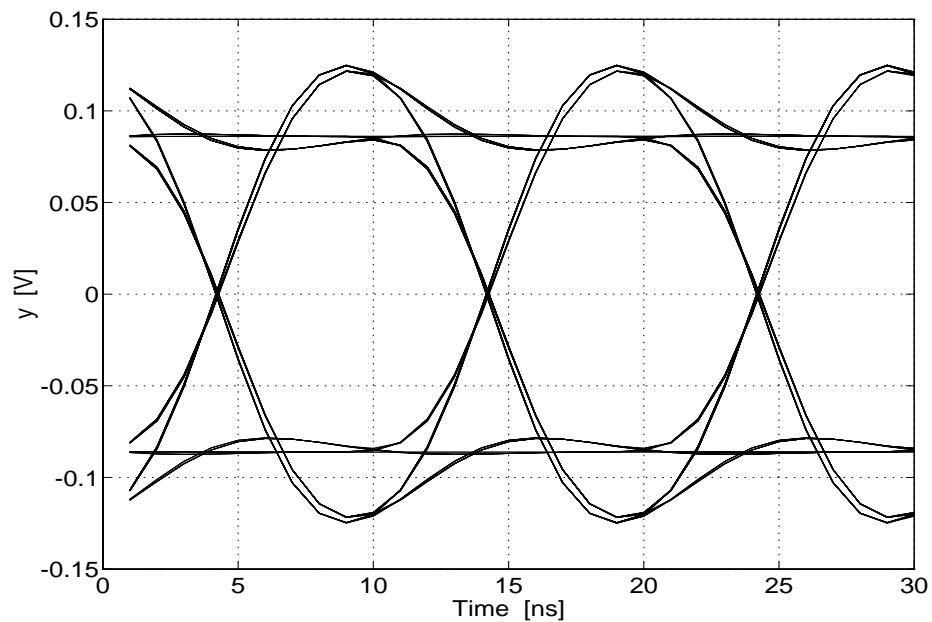


Figure 3.14: Equalizer output “eye” pattern after adaptation for 1st-order channel.

3.15, respectively. Notice that the “eye” diagram in Figure 3.14 resembles the one in Figure 3.12 for the pulse-shaping filter output, and the overall system spectral response in Figure 3.15 is flat in the span of the input frequency. Hence, optimal equalization has been achieved using

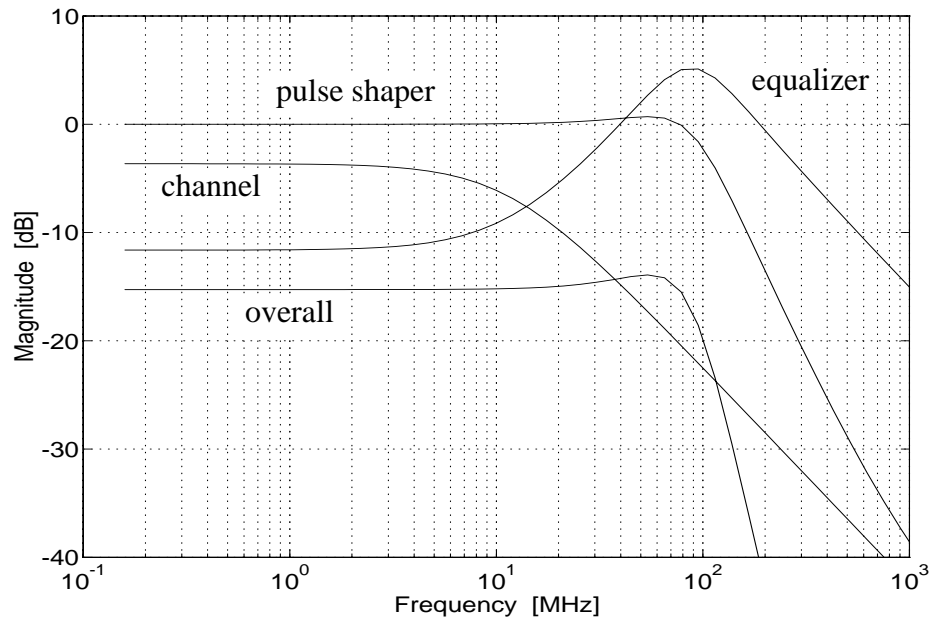


Figure 3.15: Frequency response for constituent blocks in the first-order system.

the adaptation algorithm proposed.

While the above results are to be expected since both the channel and equalizer have the same complexity, it is necessary to investigate algorithm performance for a more complex channel. Consider the second-order filter model for 100m UTP4 cables in Table 3.2. Starting at the same initial conditions as before, the adaptive filter converged after 50k iterations to a zero frequency at 13.29MHz with a residual MSE of -55dB. The equalizer output “eye” diagram and system frequency responses are shown in Figure 3.16 and Figure 3.17, respectively. The degradation in performance can be noted from the amplitude and timing distortions in the output “eye” diagram. Observe also that the algorithm ensures that both points in the overall system at $f_b/2$ and $f_b/4$ are optimized while the dip indicates the lack

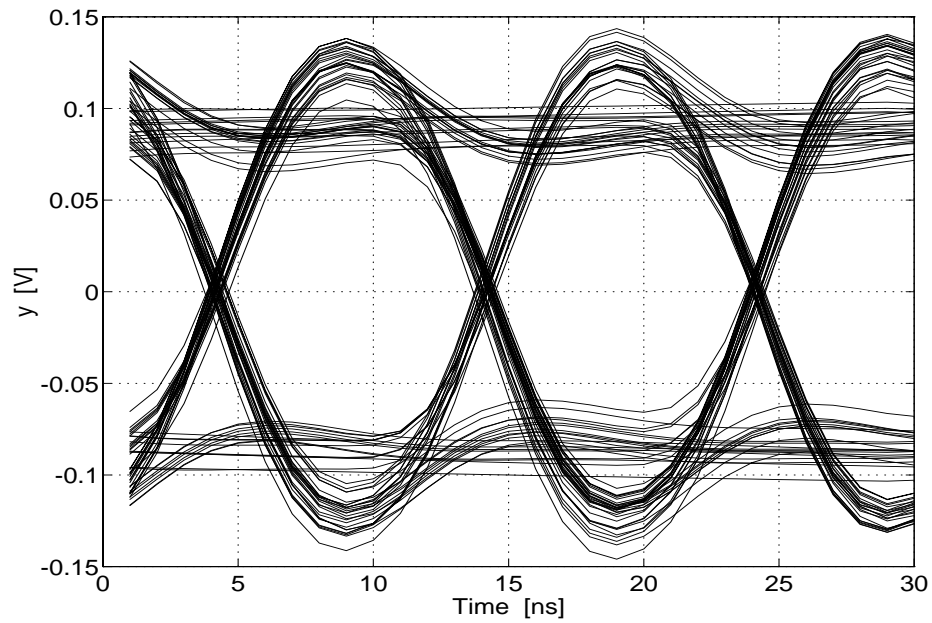


Figure 3.16: Equalizer output “eye” diagram for second-order channel.

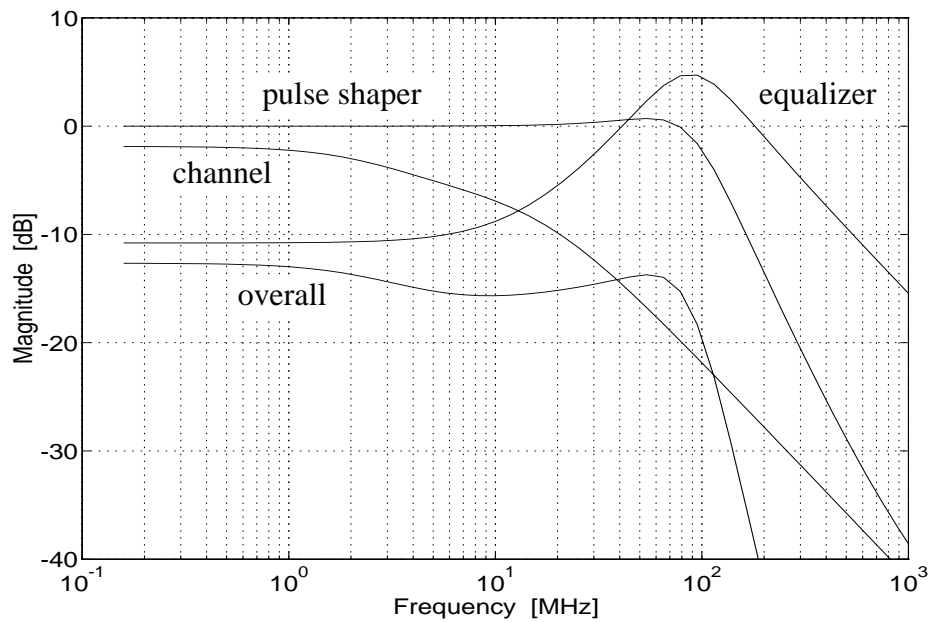


Figure 3.17: System frequency responses for second-order channel.

of test patterns in between these points. However, even if more points are chosen, an improved response will not really be attained as the adaptive system is under-modelled. Rather than

implementing a higher-order, slave equalizer comprising of scalable biquads whose parameters can be tuned based on the adaptive biquad, it was decided to experiment with a higher-order adaptive equalizer.

3.3.3 A Fourth-Order Equalizer

The tuning ideas presented so far can be extended quite naturally to higher-order filters. However, since more than two degrees of freedom will be adapted, it becomes more difficult to extract an error signal for each parameter being tuned. Thus, gradient computation will be required and a single error signal will suffice. This error signal can be obtained by comparing one sample point against a reference level, or several sample points against several reference levels. This approach implies slightly higher circuit complexity as the correlation of the error and gradient signals must be realized. Recall from Section 2.3.2 that the gradient signals for tuning filter zeros are essentially the filter output states. Hence, the hardware overhead in comparison with the requirements for the previous two examples is the multiplication of the error and gradient signals which is not trivial. In Chapter 7, a possible implementation is illustrated graphically.

Consider the second-order filter model for 100m UTP5 cables in Table 3.2. For optimal equalization, the inverse filter must be realized at least in the span of the signal spectrum. Thus, from Table 3.2 an ideal equalizer can be realized by the third-order pole-zero constellation in Table 3.3. The two additional poles at the baud rate were introduced to ensure

Table 3.3: Ideal equalizer poles and zeros to equalize 2nd-order 100m UTP5 cables.

poles (MHz)	zeros (MHz)
5.029195	3.0954
100.00	19.23127
100.00	

good noise bandlimiting. The ideal output “eye” diagram for this system in the absence of noise is shown in Figure 3.18 displaying good performance. Hence, one must be able to adapt

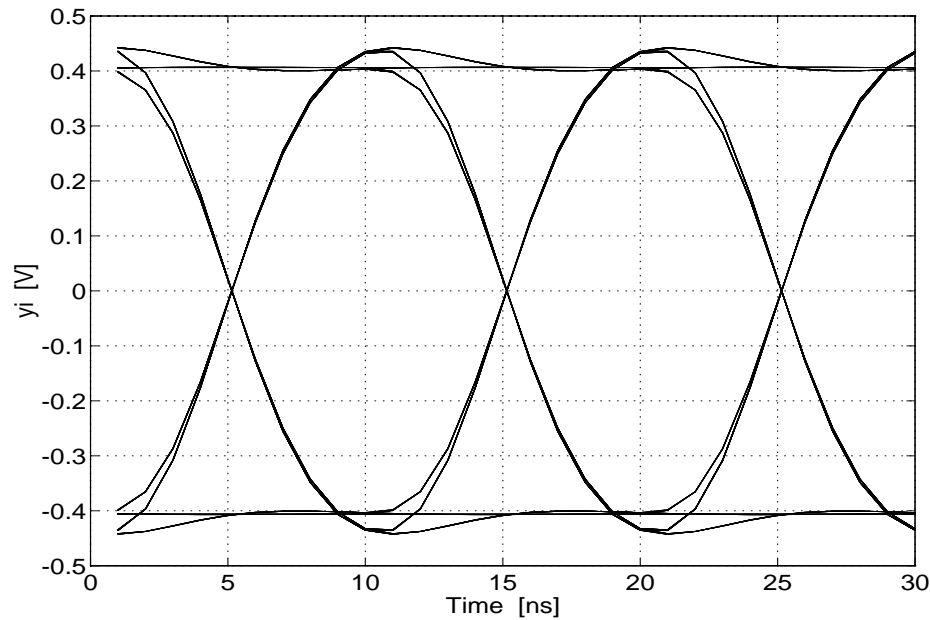


Figure 3.18: Fourth-order ideal equalizer noiseless output “eye” pattern.

the equalizer to this response. The tuning idea is to setup a template for the pulse shape based on the ideal “eye” diagram and compare the output level to each of the sample measurements in this template as shown in Figure 3.11. However, observe from Figure 3.18 that the ideal response output levels are not concurrent for each bit time, but rather they depend on the past data patterns. Taking into consideration one template sample at mid eye and observing the output for four possible data patterns by considering the present and the previous 2 bits detected, gives four different levels for the output, as shown in Table 3.4. Naturally, since the patterns were limited to a history of the last three bits, some residual MSE will result assuming the filter reaches a convergent location. This error can be given by

$$E[e^2(k)] = \frac{1}{N} \sum_{i=1}^N \Delta_i^2 \quad (3.14)$$

where N represents the number of samples over which the expectation is taken and Δ_i represents the difference between the quantized levels in Table 3.4 and the actual values the equalizer output level takes.

Table 3.4: Ideal output level for the bit patterns indicated.

k-2	k-1	k	ideal output level (V)
0	0	1	0.43255
1	1	0	-0.43255
0	1	0	-0.43535
1	0	1	0.43535
0	1	1	0.4034
1	0	0	-0.4034
0	0	0	-0.40615
1	1	1	0.40615

To test the above idea, a fourth-order equalizer was set up in accordance with Figure 3.11. The pole frequencies were fixed to approximate the ideal poles and these were located on the real axis at: 3MHz, 15MHz, and two at 100MHz (see the 5th-order model for the cable in Table 3.2). The noise source was white Gaussian with variance $0.005^2 V_{rms}^2$. The adaptation step-size was 0.005. A PLL was configured for clock extraction and as before the system sampling rate was 1GHz to simulate analog functions. The adaptation algorithm employed the SE-LMS procedure (error signal and gradient signals) with the gradients being the filter output states. The channel and initial mistuned equalizer output “eye” diagrams are shown in Figure 3.19 and Figure 3.20, respectively. This initial equalizer had its zeros at 2.8MHz, 10.0MHz, and 50MHz. After about 15M iterations, the equalizer converged to a steady-state MSE of -28dB with the zeros at: 2.31MHz, 10.171MHz, and 24.74MHz. This large number of iterations is due to the fact that the PLL had to adapt in the noisy environment before the filter could actually reach steady-state and because the full SE-LMS algorithm was simulated. The

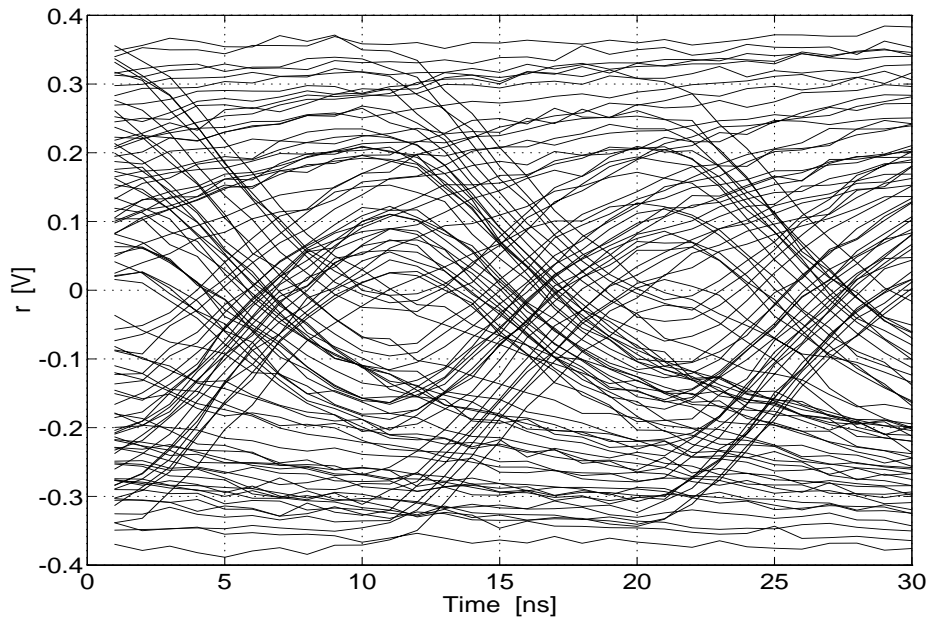


Figure 3.19: Second-order filter model for 100m UTP5 cables “eye” pattern.

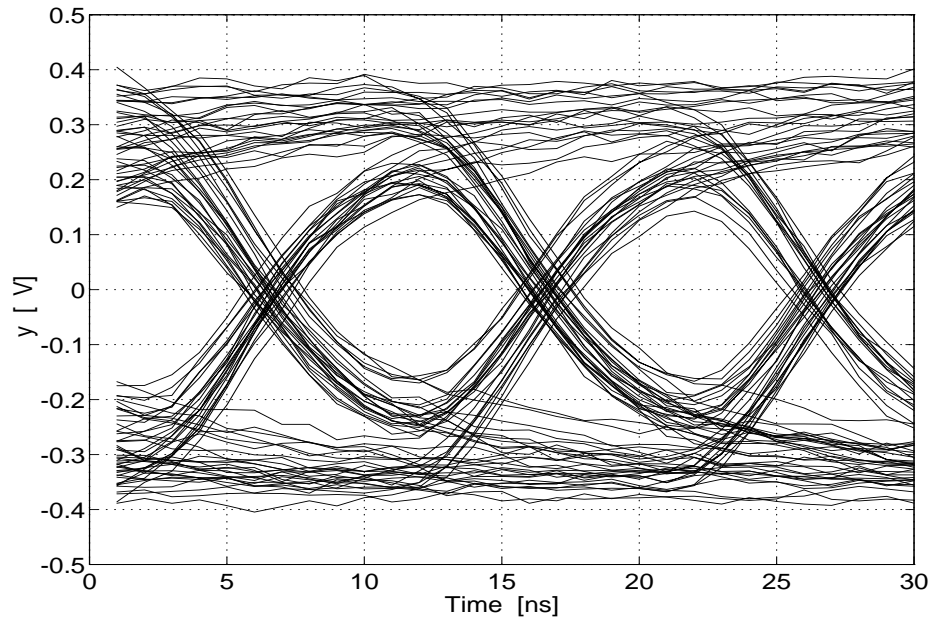


Figure 3.20: Initial equalizer output “eye” diagram.

equalizer output “eye” patterns and the various system block frequency responses are shown in Figure 3.21 and Figure 3.22, respectively.

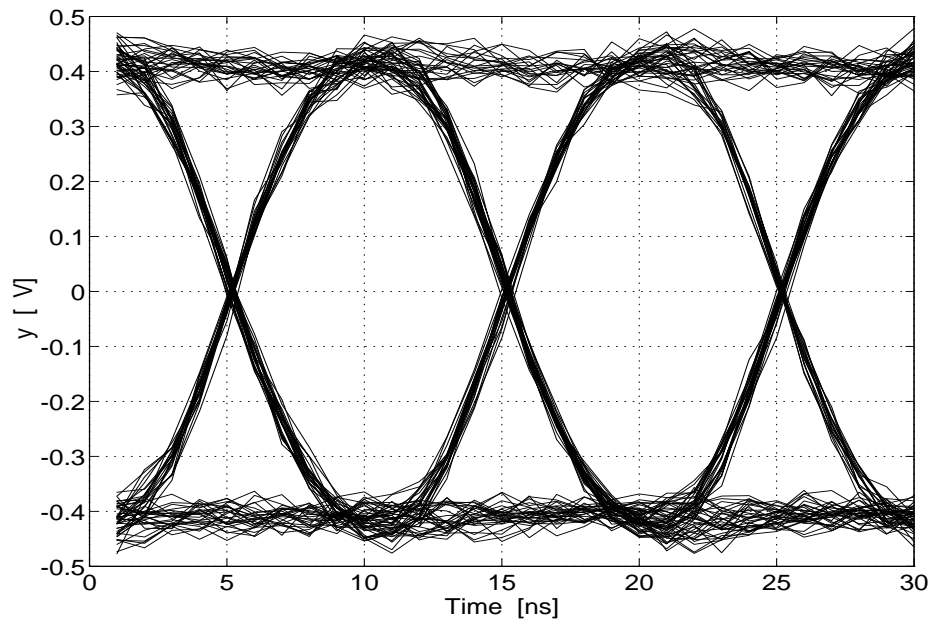


Figure 3.21: Equalizer output “eye” after adaptation for 100m cables.

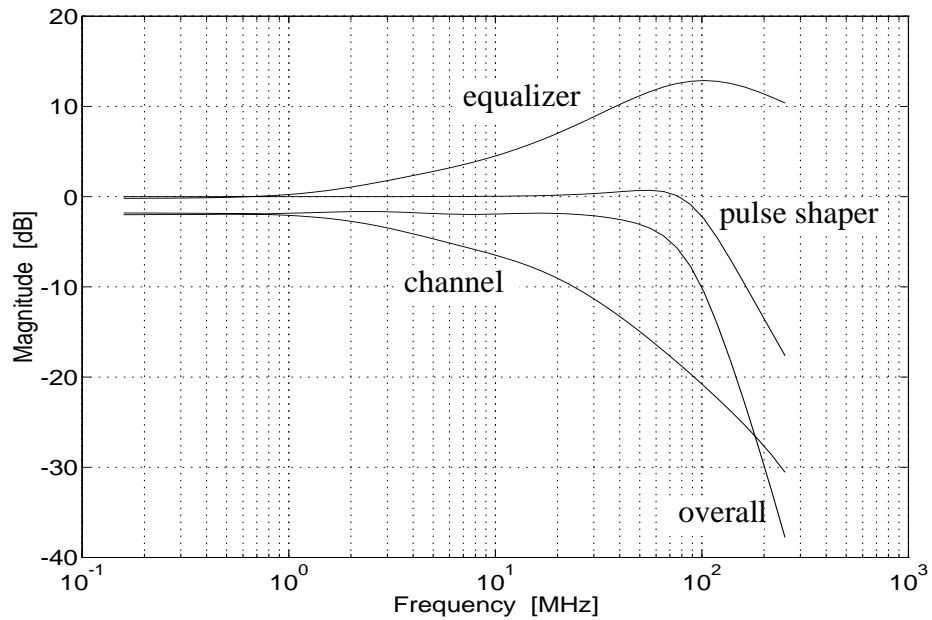


Figure 3.22: System frequency responses for 100m cables.

As a further test, the channel complexity was increased to the fifth-order model in Table 3.2, the equalizer was mistuned to the same location as the initial case for the above example, and the equalizer was allowed to converge according to the same technique. It was observed

that the equalizer converged to the following zero-frequency locations: 2.2137MHz, 8.999MHz, and 29.3546MHz after 15M iterations and sustained a residual MSE of -39dB. The output “eye” diagram for this case was similar to the one in Figure 3.21 while the frequency responses for the system is shown in Figure 3.23.

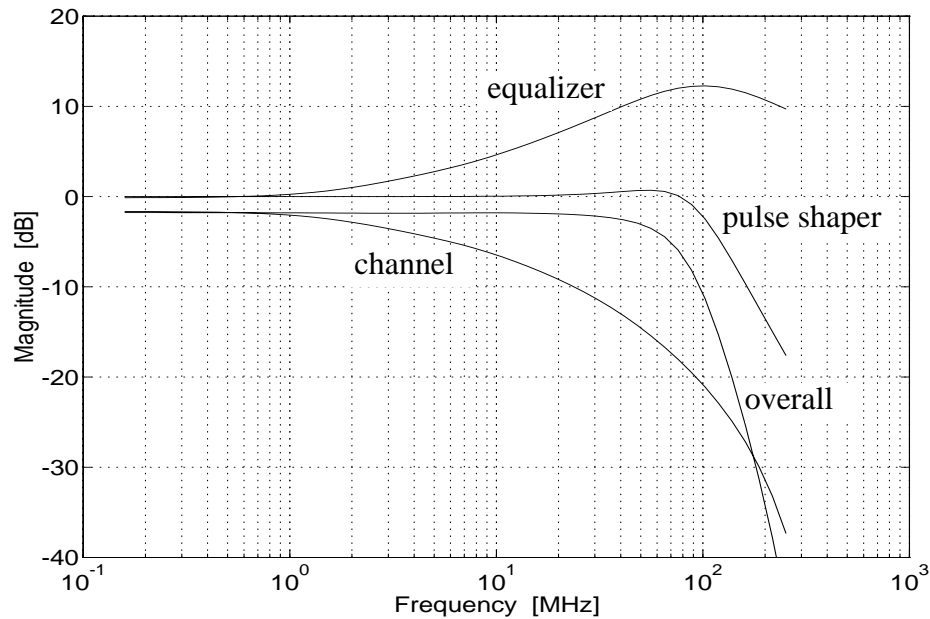


Figure 3.23: Frequency responses for the fifth-order cable model.

Further testing involved the cable models for the 125m cable and the 75m cable. For these cases, the initial equalizer transfer-function was tuned to the one obtained adaptively for the 100m cable and the performance of the algorithm in optimizing for this large channel variation was investigated. For both cases, the noise level and the reference levels for adaptation were as before. It was observed that both test cases converged after 15M and 6M iterations to an optimum location with a residual MSE of -25dB and -45dB for the 125m and 75m cables, respectively. The equalizer zeros for these systems were located at: 2.0407MHz, 9.3467MHz, and 18.341MHz for the 125m cable and 2.529MHz, 9.0838MHz, and 43.219MHz for the 75m cable. The output “eye” diagrams and frequency responses for these test cases are shown in Figures 3.24-3.27. Observe also from the residual MSEs quoted for the different cable lengths

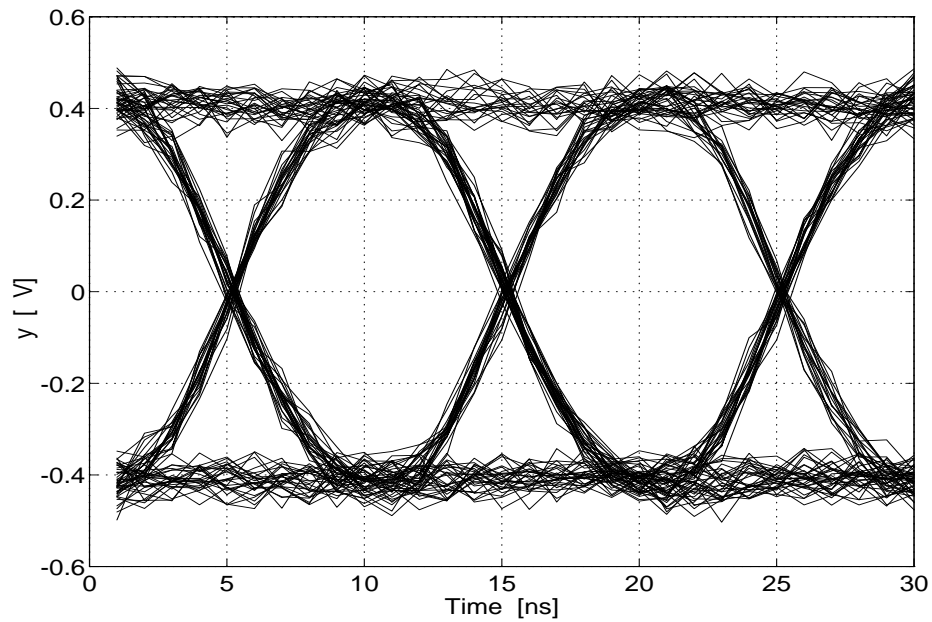


Figure 3.24: Equalizer output “eye” pattern for the 125m cable.

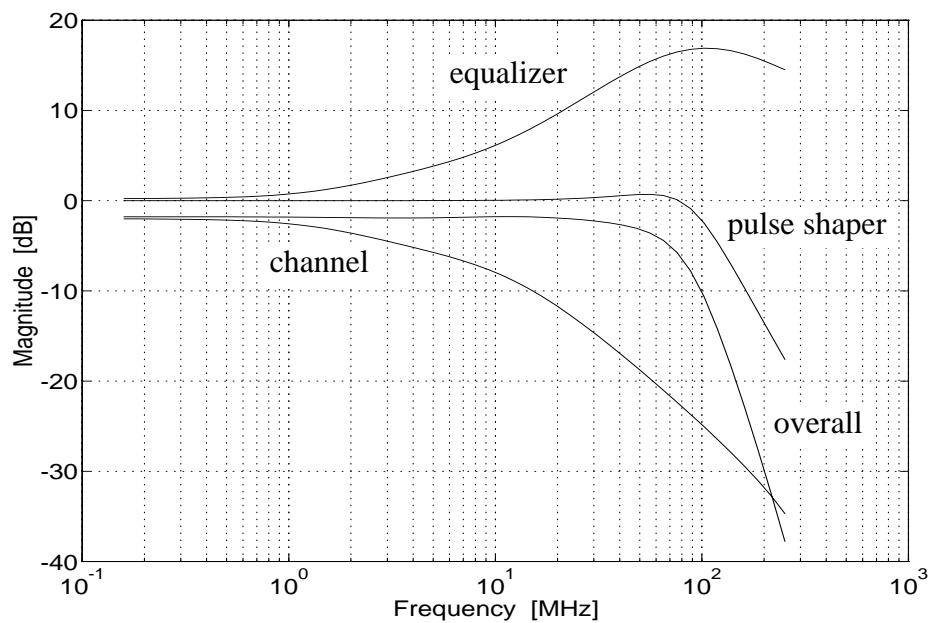


Figure 3.25: System frequency responses for the 125m cable.

and from the output “eye” diagrams that output noise increases with increased cable length as higher high-frequency boost is realized for equalization.

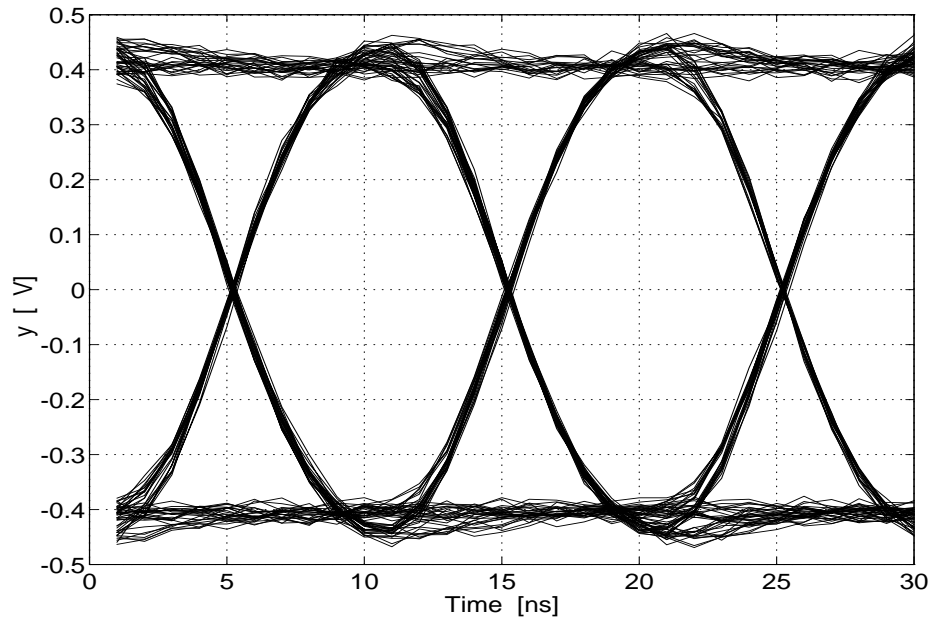


Figure 3.26: Equalizer output “eye” pattern for the 75m cable.

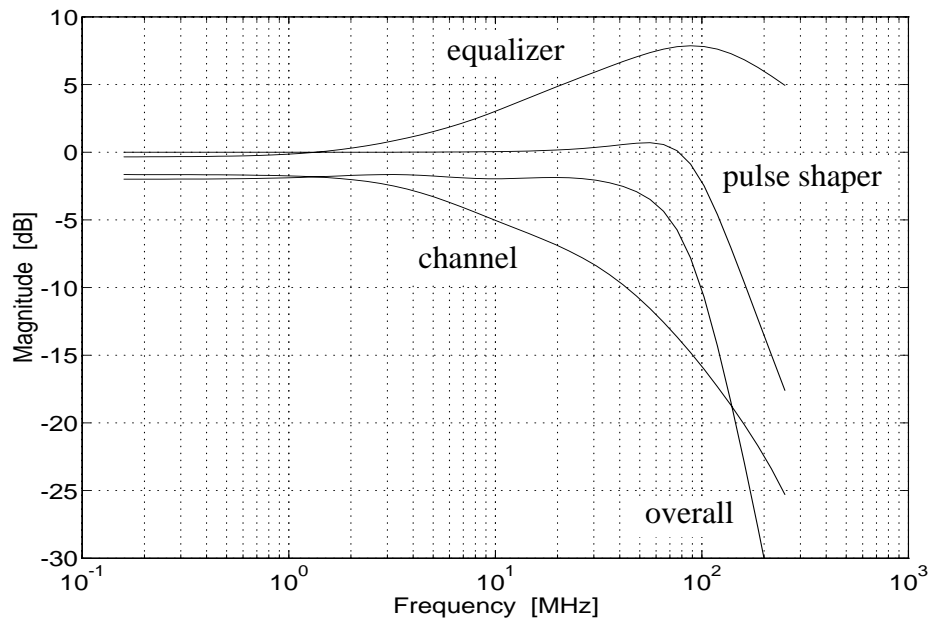


Figure 3.27: System frequency responses for the 75m cable.

3.4 Adaptive Equalization for PR4 Read Systems

The last application example we will consider is an analog adaptive equalizer for the magnetic recording media. While state-of-the-art equalizers for magnetic data storage employ externally programmable filter blocks, as discussed in Chapter 2, there is a growing need for adaptive equalizers that can track temperature and other unforeseen channel variations during operation [Uehara 93]. Here, we provide a methodology for realizing these equalizers.

A sixth-order equalizer, whose five zeros and DC gain are adapted, is investigated. The adaptation makes use of the standard LMS algorithm discussed in Section 2.3.2 in that a single 1-bit error signal is obtained and together with the equalizer coefficient gradient signals (i.e. the filter states in this case), the \mathbf{c} vector is adapted. The generation of the error signal makes use of the curve fitting approach using clocked comparators as in the previous cases.

3.4.1 Background

As was already mentioned, a bandlimited channel gives rise to ISI and when combined with noise, the net effect is a degradation in the “eye” pattern which impairs symbol detection. In Sections 3.3.2 and 3.3.3 it was shown that an equalizer can be used to flatten the overall response up to the signal bandwidth and then roll off to limit noise enhancement. At high recording densities, significant high-frequency boost would be required ($>25\text{dB}$) to flatten the response. Thus, partial-response signalling has been adopted. This signalling choice tolerates residual ISI, hence, the overall response is allowed to be lossy which reduces equalizer complexity (boost $< 15\text{dB}$) as well as output noise. For the analysis herein, the class-four partial response (PR4) signalling scheme will be used. The “eye” diagram for this pulse shape for 20Mb/s transmission is shown in Figure 3.28.

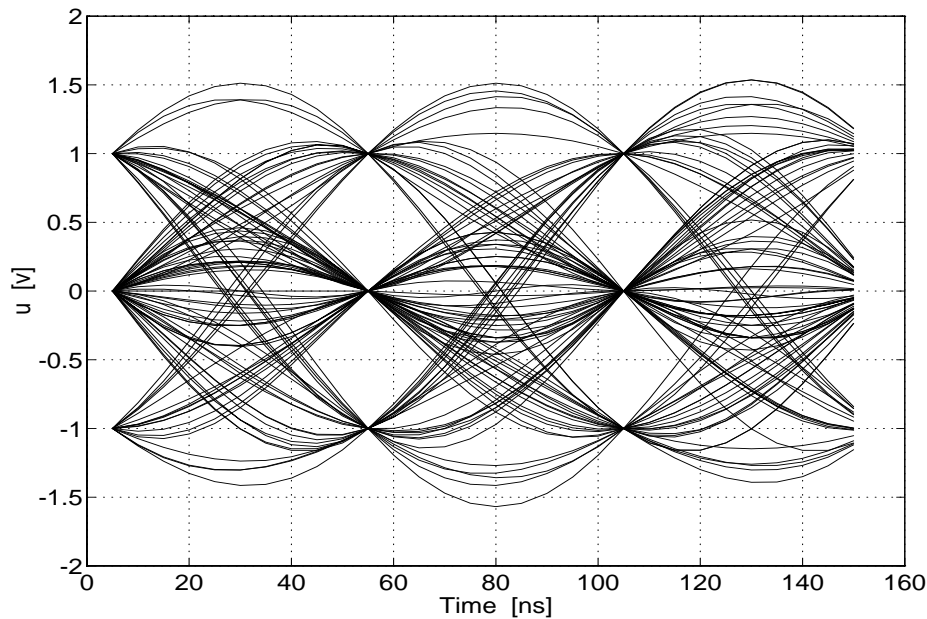


Figure 3.28: Eye diagram for PR4 signalling at 20Mb/s.

3.4.2 The Adaptive Equalizer: basic theory

Consider the setup shown in Figure 3.29. The input, $a(k)$, consists of the write data. The block labeled “1” implements an ideal bit-rate differentiator and is used to model the differentiation function that produces the read current from the flux patterns stored on the magnetic media. The channel approximates the Lorentzian pulse shape for the read head impulse response. This channel was modeled using a sixth-order Bessel lowpass filter with the normalized pole frequencies in Table 3.5. Three different channel responses will be investigated here: 3MHz, 3.5MHz, and 7MHz filters giving a PW50 of 115ns, 100ns, and 50ns, respectively. It should be mentioned here that although the Bessel response only approximates a Lorentzian shape, an ideal Lorentzian pulse is not critical to determine adaptation performance. In addition, most systems rarely produce an ideal Lorentzian pulse shape.

The block labeled “4” consists of a 200-tap FIR filter that realizes the PR4 response. The tap weights were obtained using the expressions provided in [Kabel 75]. The noise source in

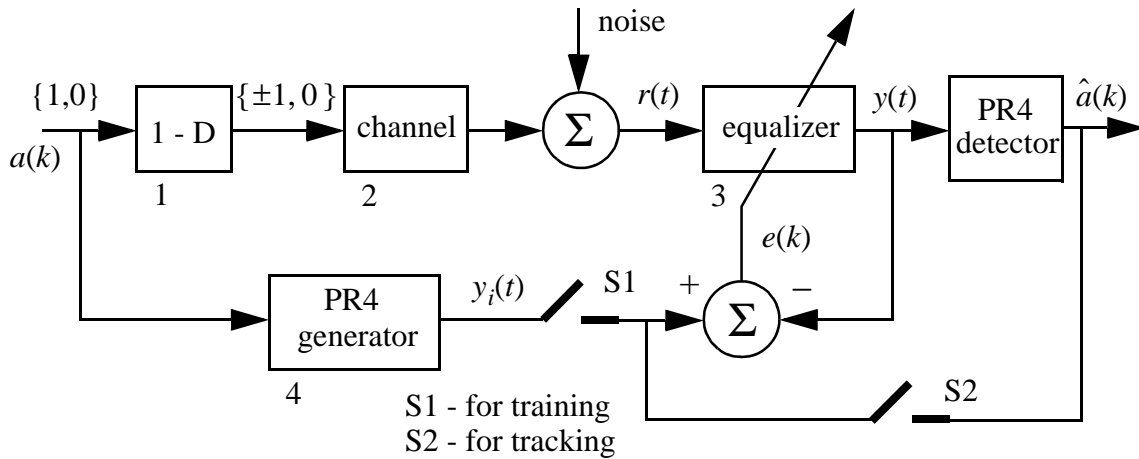


Figure 3.29: Setup used to simulate the magnetic recording channel.

Table 3.5: Normalized sixth-order Bessel filter used to generate the different channels.

normalized S-domain poles	normalized S-domain zeros
-1.5755 ± j0.3167	all at infinity
-1.3840 ± j0.9725	
-0.9353 ± j1.6630	

Figure 3.29 was white Gaussian noise of variance $0.04V_{rms}^2$ and shaped by a third-order, high-pass filter with a knee at 10MHz. The effect of both a lossy channel and noise is to degrade the “eye” quality as illustrated in Figure 3.30. The equalizer details are explained later. Finally, to simulate analog functions all blocks were run at a sampling frequency of 200MHz.

The first step in determining the equalizer parameters involves the choice of the equalizer poles and zeros that will ensure the output of the combination of blocks “1”-“3” match the output of block “4”. To achieve this match, we make use of standard adaptive theory to tune both poles and zeros of various filter orders until satisfactory results are obtained. This approach makes use of a training sequence for adaptation. Applying this technique resulted in the pole-zero system in Table 3.6. The poles and zeros depicted are in the digital domain and

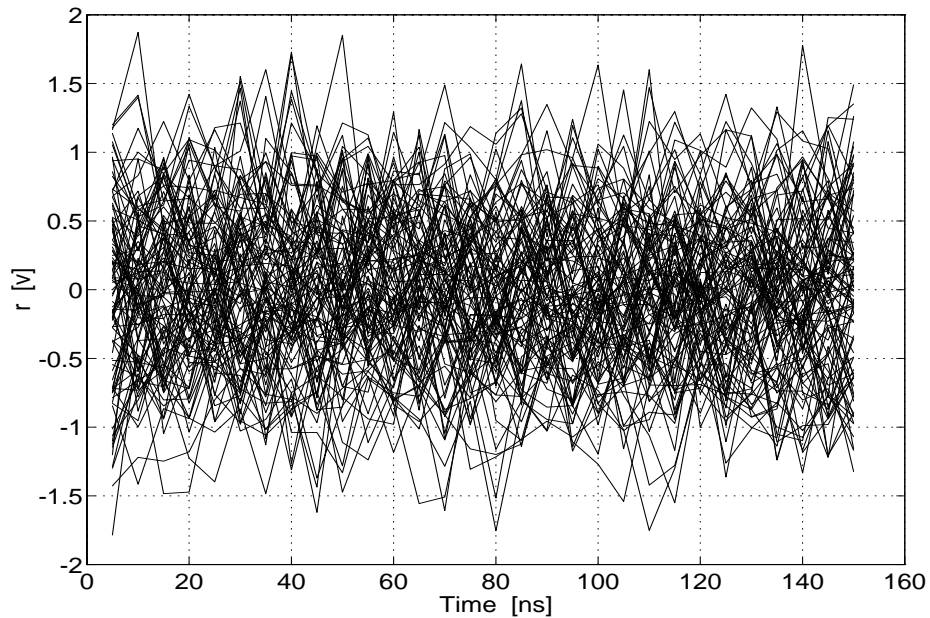


Figure 3.30: Equalizer input “eye” for 20Mb/s PR4 signalling in additive noise.

Table 3.6: Pole/zero constellation for the adapted equalizer using a training sequence.

normalized Z-domain poles	normalized Z-domain zeros
$0.9238 \pm j0.2547$	$0.7102 \pm j0.4171$
$0.8845 \pm j0.1928$	$1.1520 \pm j0.1185$
$0.8911 \pm j0.0583$	0.8199

can be easily transformed to the analog domain using the Bilinear transformation. The residual MSE was -31dB. The “eye” diagram for the overall system (blocks “1”-“3”) using the equalizer response in Table 3.6 is illustrated in Figure 3.31.

In a practical system, we propose to blindly adapt (i.e. S1 open and S2 closed in Figure 3.29) only the equalizers zeros to account for minor process variations and temperature fluctuations. Hence, the adaptation algorithm to be discussed is only useful for tracking purposes. The poles will be fixed and correspond to those given in Table 3.6. These poles can be positioned using standard techniques such as an external resistor or external programming.

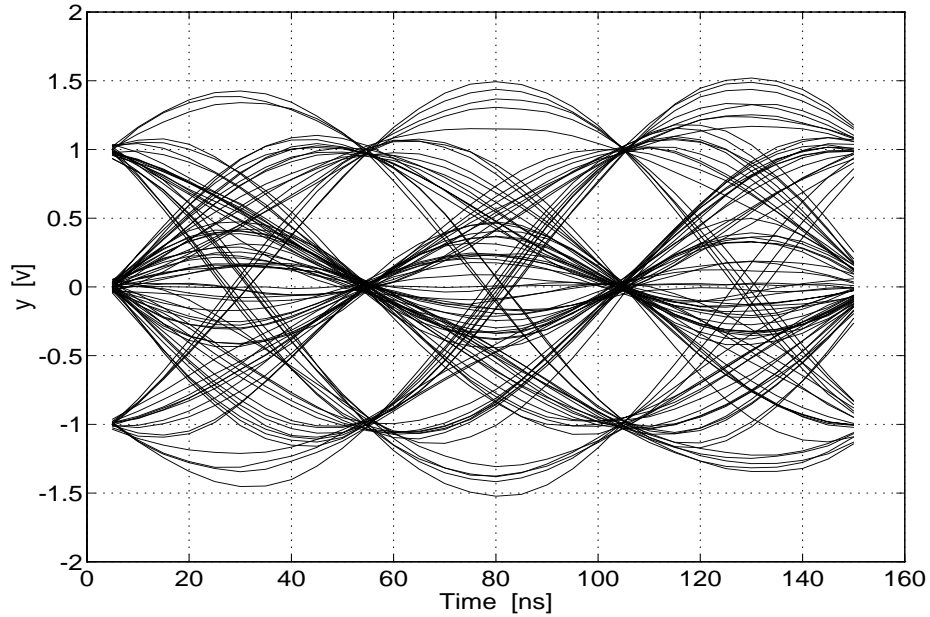


Figure 3.31: Equalizer output “eye” diagram after standard LMS adaptation.

As stated earlier, it was chosen to keep the poles fixed for reduced circuit complexity and prevention against possible instability.

A proposed adaptation algorithm is as follows. Assuming proper clock recovery, the equalizer output is sliced at the clock rate to detect the data as usual (i.e. decide on one of the three possible levels $\pm 1, 0$). In addition, we make use of additional slicers to obtain an error signal for adaptation as follows. Letting $y(t)$ represent the equalizer output then,

$$\begin{aligned}
 (k) &= 0 - y(t) & \text{if } -0.5 \leq y(t) \leq 0.5 \\
 (k) &= 1 - y(t) & \text{if } y(t) > 0.5 \\
 (k) &= -1 - y(t) & \text{if } y(t) < -0.5
 \end{aligned} \tag{3.15}$$

where the assumed values for the pulse peak-output levels (see Figure 2.6) are ± 1 V and the reference levels for computing the error signal are ± 0.5 V. This discrete nature of the error signal comes from the fact that the error signal is only available during the sample times.

At this point, we would like to point out some potential problems with this algorithm. First, it assumes satisfactory clock recovery. However, if the equalizer is initially significantly

mistuned such that clock recovery becomes difficult, the system will have a difficult time converging. Second, assuming the clock is properly recovered, there is no guarantee the algorithm will converge to produce the PR4 signal, since only a single sample measurement is evaluated and there may be more than one pulse shape that meets this level at this sample time. Finally, consider the case of AGC (see Figure 2.8) failure such that the pulse peak-output level is forced to be below the reference level at all times. In accordance with (3.15), the algorithm will force all the coefficients to zero at all sample instants resulting in zero output.

3.4.3 The Adaptive Equalizer: simulation verification

To test the idea presented above, the ideal equalizer poles were fixed according to the values in Table 3.6 while the zeros were initially mistuned according to the locations: 0.6433 , $1.0662 \pm j0.1433$, and $0.8199 \pm j0.2951$. The resultant initial “eye” diagram is illustrated in Figure 3.32 where significant (65%) distortion is evident. After 2M iterations with an

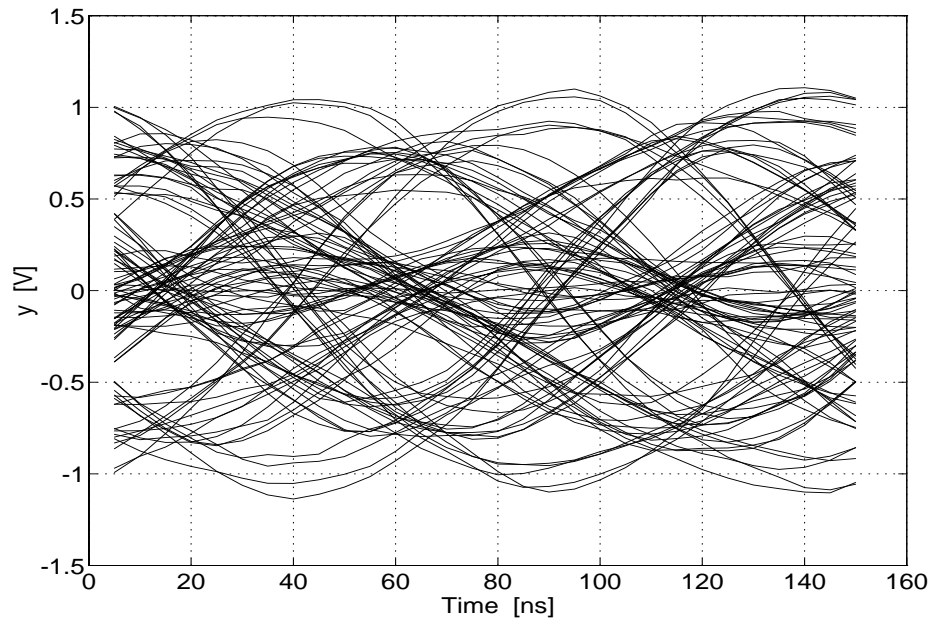


Figure 3.32: Mistuned equalizer output “eye” for 100ns PW50.

adaptation step size of 0.005, the system converged with a residual MSE of -33dB to the

pole-zero constellation in Figure 3.33. The overall system impulse response (blocks “1”-“3”) compared to the ideal impulse response (of block “4”) is shown in Figure 3.34. The system

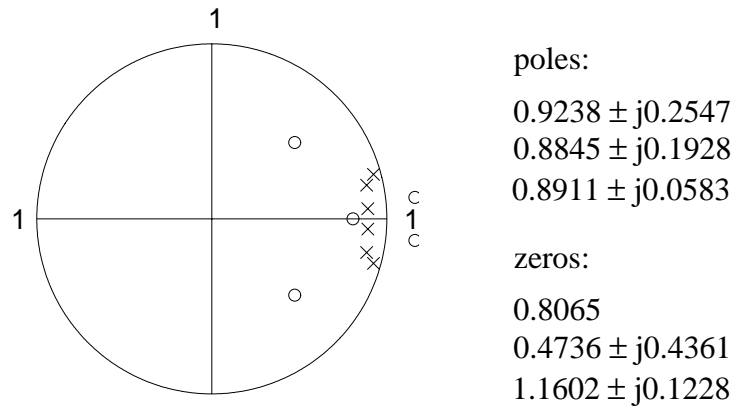


Figure 3.33: Equalizer pole-zero constellation for 100ns PW50 channel.

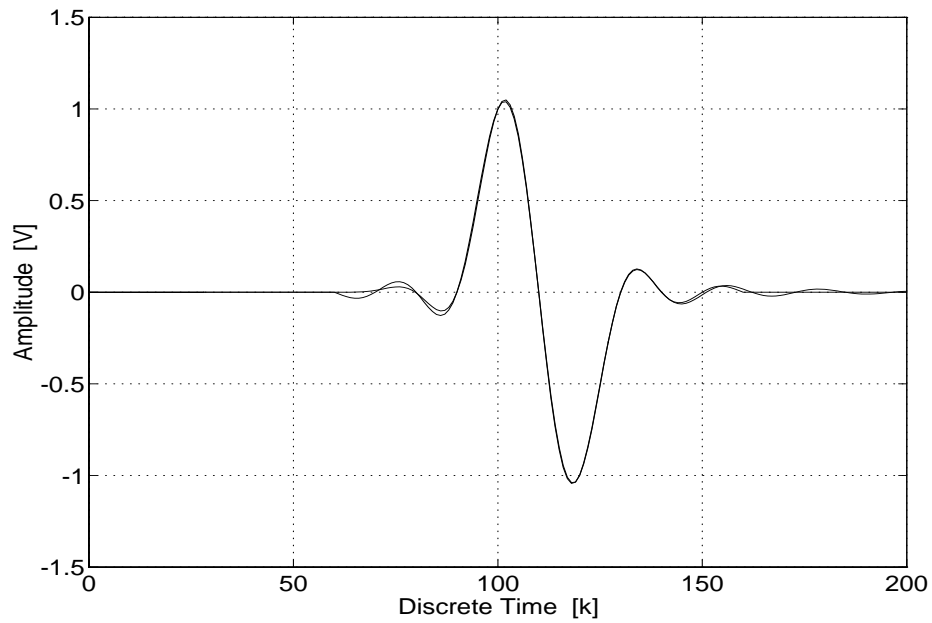


Figure 3.34: Ideal and system output impulse response for the 100ns PW50 channel.

output “eye” diagram is given in Figure 3.35 showing residual amplitude distortion of less than

10%. The reason for the residual distortion is due to the fact that an ideal match would require

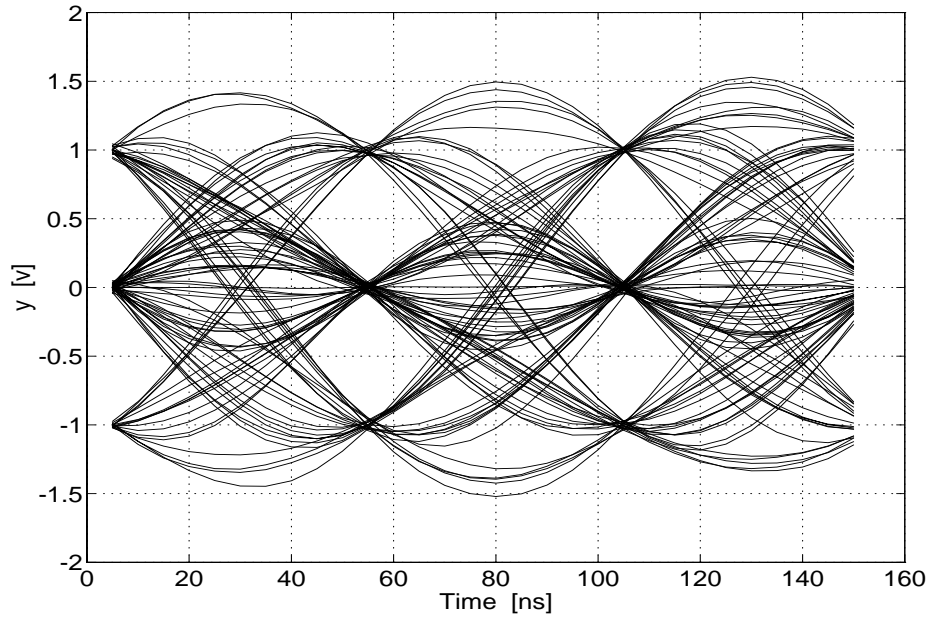


Figure 3.35: Equalizer output “eye” for 100ns PW50; zero adaptation only.

a much more complex equalizer; one that can more accurately match the amplitude and phase characteristics of the 200 tap FIR filter of block “4” in Figure 3.29. Figure 3.36 depicts the frequency response at the output of each of the blocks in Figure 3.29. Notice that the overall frequency response tracks the ideal PR4 frequency response. Finally, Figure 3.37 shows the denormalized equalizer frequency response for more clarity. Observe that peak boost occurs at 8MHz and is of value 10dB.

To determine the capability of the algorithm in tracking more extreme channel variations, the channel response was varied while the equalizer poles were fixed according to the values in Table 3.6. The equalizer zeros were adapted using the same procedure. Both the 7MHz Bessel response and the 3MHz Bessel response in Table 3.5 were simulated. For each case, the initial equalizer setting was essentially the response in Figure 3.33. The adaptation took

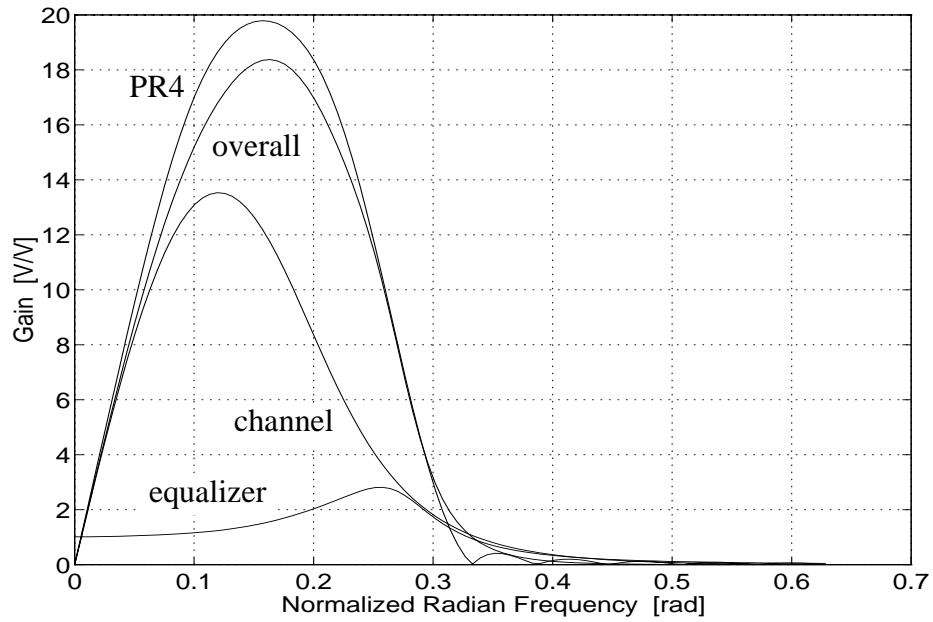


Figure 3.36: System constituent block frequency response and ideal response.

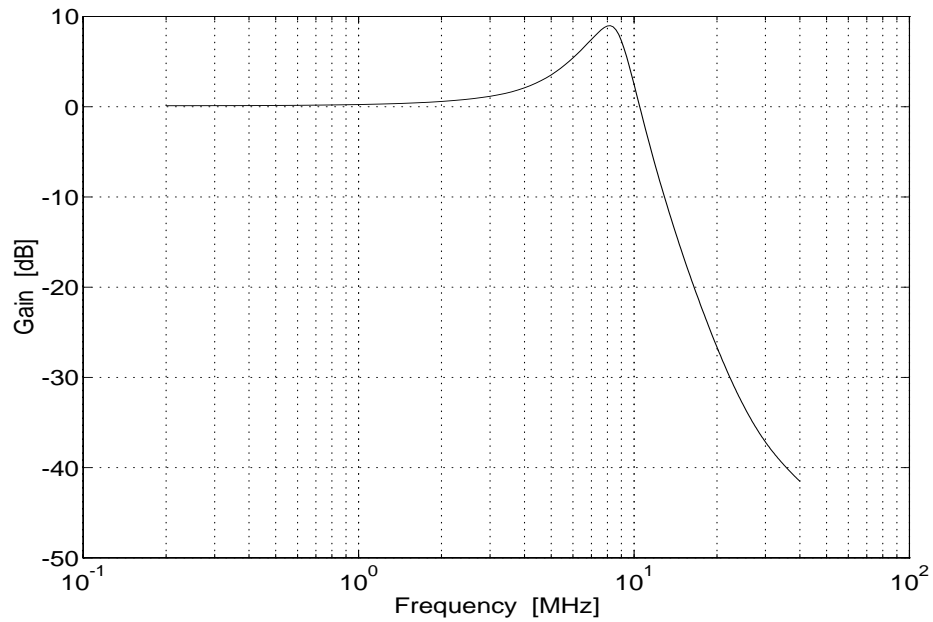


Figure 3.37: Denormalized equalizer frequency response.

about 2M and 3M iterations and the residual MSE was -29dB and -25dB for the 7MHz and 3MHz filters, respectively. Figures 3.38 - 3.45 illustrate the simulated results for these two test

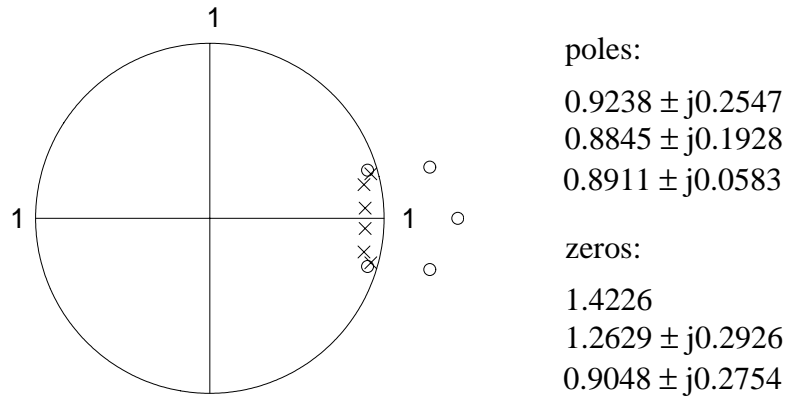


Figure 3.38: Equalizer pole-zero constellation for 50ns PW50 channel.

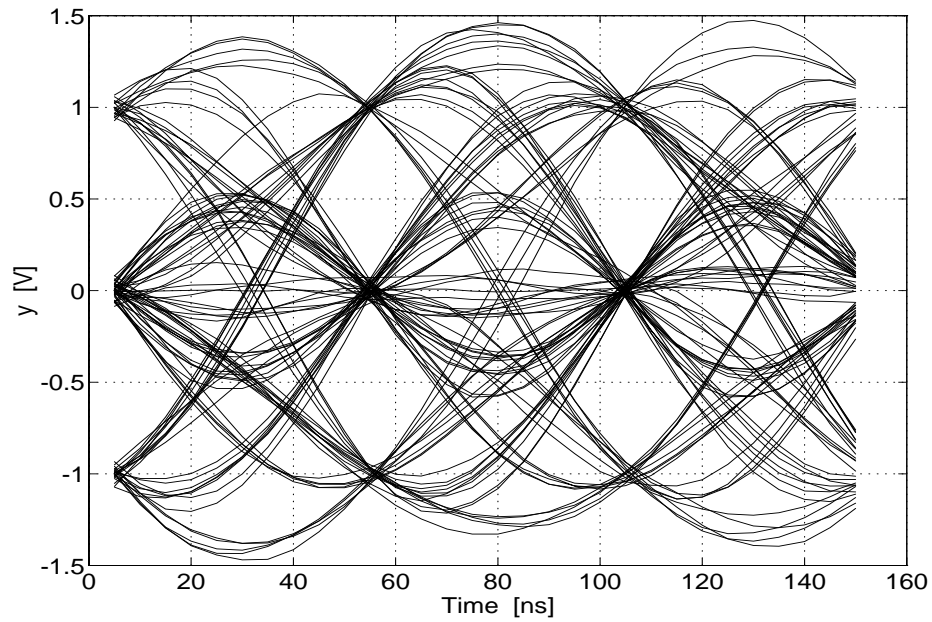


Figure 3.39: Equalizer output ‘eye’ for 50ns PW50; zero adaptation only.

cases. Observe that the 3MHz (pw50 = 115ns) channel system response has significant steady-state amplitude distortion (35%) degrading system BER. Hence, this result represents a channel requiring higher order equalization.

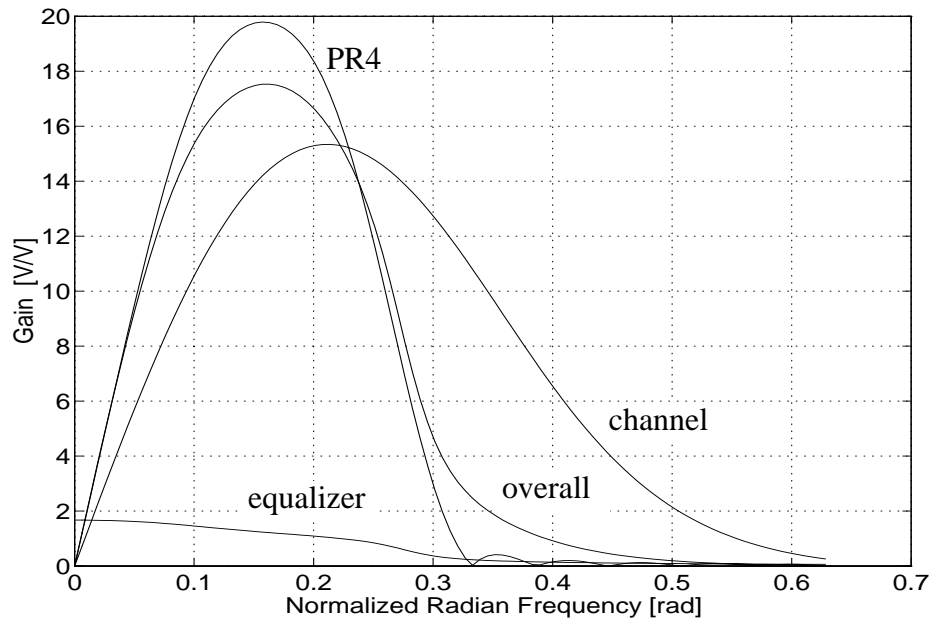


Figure 3.40: System constituent block frequency response and ideal response.

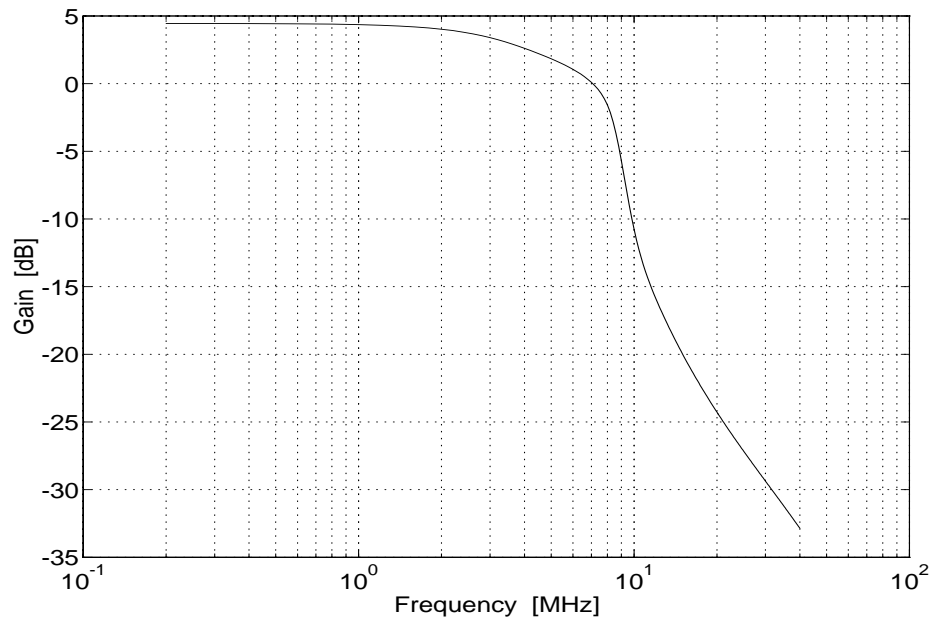


Figure 3.41: Denormalized equalizer frequency response.

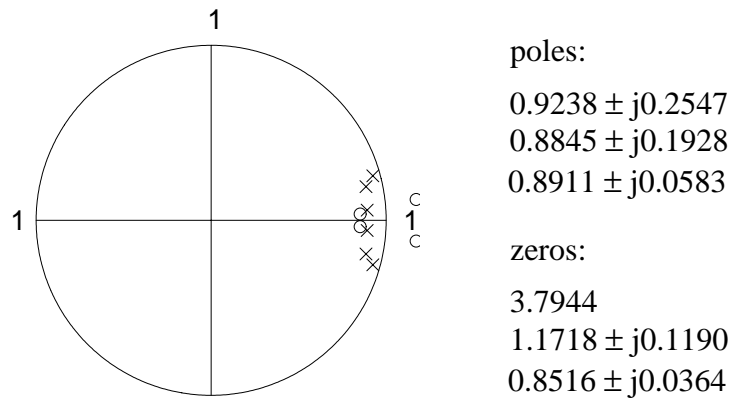


Figure 3.42: Equalizer pole-zero constellation for 115ns PW50 channel.

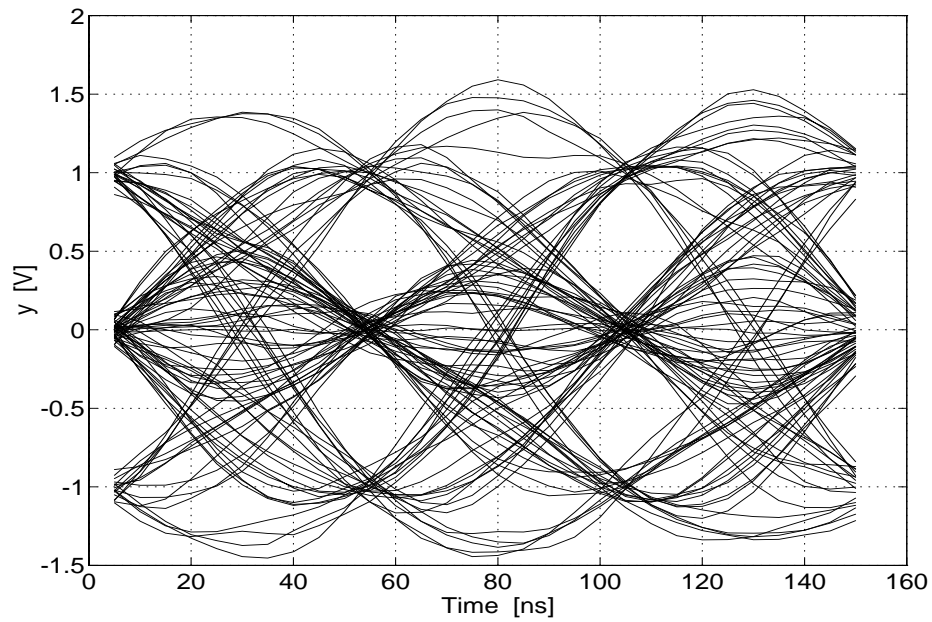


Figure 3.43: Equalizer output “eye” for 115ns PW50; zero adaptation only.

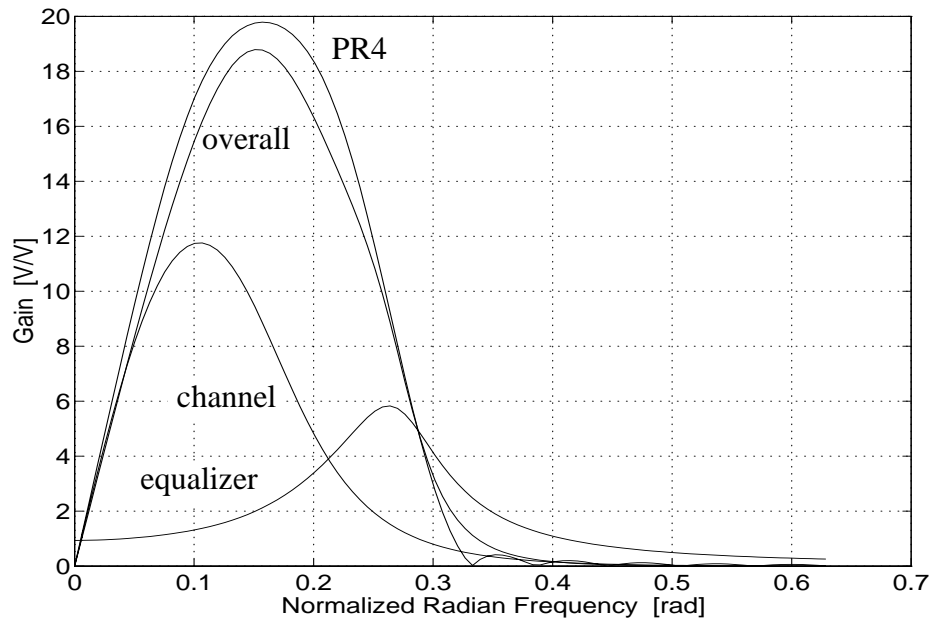


Figure 3.44: System constituent block frequency response and ideal response.

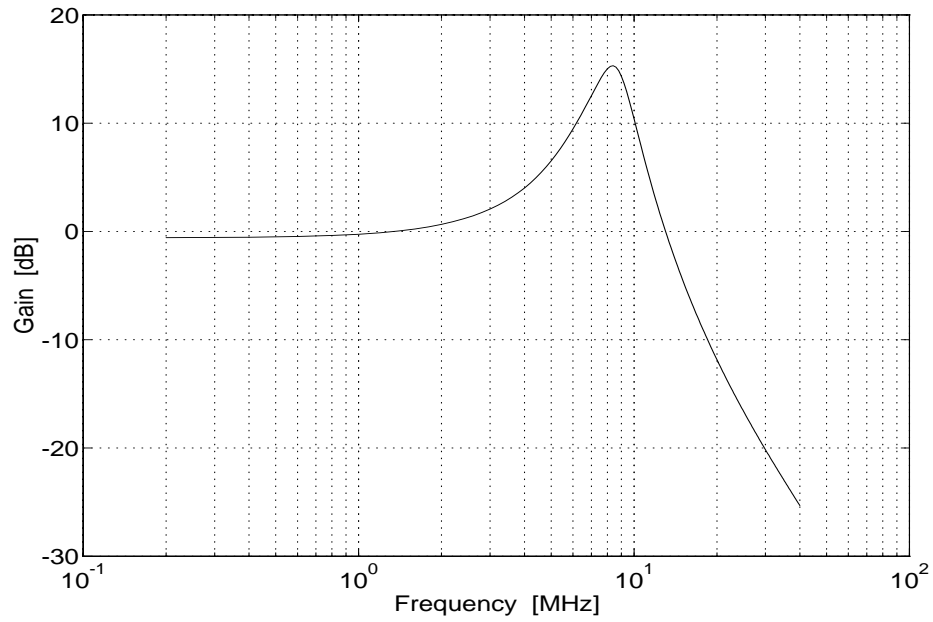


Figure 3.45: Denormalized equalizer frequency response.

3.5 System Non-idealities and Limitations

In Section 3.2.3, the effect of DC offset on the performance of the pulse-shaping filter was discussed. While DC offset is one source of non-ideality, other sources include comparator hysteresis, circuit delays, and clock timing jitter. These sources of non-idealities will be discussed in this section and it will be noted that their effects lead to distortion in the output signal. System limitations, such as speed constraints of the digital blocks and the practicality of the reference level choice, will also be addressed.

3.5.1 Comparator Hysteresis

First, consider the case of an ideal comparator. At convergence, the DAC output will continuously toggle 1 LSB due to the finite resolution of the DAC. This DAC limit cycle will result in a coefficient limit cycle such that the output level will jitter about the desired reference level. For example, in Figure 3.7, the lowpass output would jitter about its zero-crossing while the bandpass output will jitter about V_{ref} . This behavior implies some minor distortion in the output signal.

When comparator hysteresis is present, the same behavior at steady-state will occur. However, if the hysteresis is larger than the DAC induced jitter of the output signal in the ideal case, the hysteresis size will govern the amount of jitter at convergence. If the hysteresis is smaller, its effect will not be significant. One must therefore design the comparators for low hysteresis (at least to within the DAC induced jitter in the ideal case) by using clocked comparators that can be reset prior to each sample time.

3.5.2 Circuit Delays

While the effects of dynamic delays would average out and have a weak effect on the algorithms proposed, static delays in the comparator trigger times will result in an output error

similar to the offset problem. This error will be more severe if the sample point being tested occurs in a region where the signal gradient is large (i.e. at the zero-crossing of the output “eye”) than for sample points where the signal gradient is small (i.e. at mid “eye”). Hence, the choice of sample points and the method of generating the trigger times must be carefully investigated.

For example, in the pulse-shaper application discussed in Section 3.2, the f_o tuning stage is more sensitive to delay offset than the Q tuning stage. This larger sensitivity is a result of the slope at the measurement time being much higher at the lowpass zero-crossing than the at bandpass peak.

3.5.3 Clock Jitter

Similar to comparator clock delays, clock jitter will result in larger errors when the sample point being measured occurs at a high-slope region as opposed to a shallow-slope region. Clock jitter would manifest the same limit cycle behavior at steady-state as discussed in Section 3.5.1.

3.5.4 System Limitations

In all the applications discussed in this chapter, we looked at one update per bit time. There may be cases when the error signal is computed at more than one point in the span of the “eye” opening, or bit time (i.e. at mid “eye” as well as at the zero-crossings). As a result, the digital updates would be performed at a much higher rate. If this rate becomes impractical, it should be possible to make use of time alternating. Specifically, one can adapt the coefficients using an error signal based on one time instant for a given number of iterations and then continue with another time instant for some more iterations. The process is then repeated over all time. This scheme, however, would increase convergence time.

Alternatively, it is possible to update the coefficients at a slower rate (by ignoring data) to meet the capabilities of the digital circuitry. In fact, this approach was adopted in the test set-up to be described in Section 5.2.4 since the LMS circuitry was off-chip. Once again, convergence time increases for this approach.

Another limitation is the choice of reference levels for error signal computation. Recall from Section 3.3.3 that 4 absolute levels were chosen. Some of these require resolution to 3mV which may be difficult to achieve in a practical system. For the equalizer discussed, one can reduce the 4 absolute levels to 2. This modification will slightly increase the steady-state MSE in accordance with (3.14). To improve performance, it may be possible to use additional time instants such as at the zero-crossing for the output “eye” as well as at mid “eye”.

Perhaps the most significant limitation on system performance would come from the clock recovery circuit. For the equalizer adaptation approaches proposed here, the comparator trigger times are obtained from the recovered clock. However, the recovery depends on the equalizer output which in turn depends on the adaptation performance. Hence, this “catch-22” behavior may result in system “run-away” if the equalizer is initially severely mistuned such that clock recovery becomes impossible.

3.6 Summary

In this chapter, a method for obtaining the adaptation error signal was proposed. The main idea is to make sample measurements of the filter output(s) and compare with an expected level using clocked comparators at certain time instants. This technique is suitable for high-speed applications where taking the difference between two signals is difficult. Four examples were discussed to investigate and test the feasibility of the technique:

- A second-order pulse shaping filter whose two degrees of freedom were adapted was discussed. Testing for the filter output zero-crossing and the peak level of one of the filter output states provided sufficient information

to tune filter pole-frequency and Q -factor. Practical impairments such as DC offset were considered and solutions to reduce its effects were proposed. The practical feasibility of the technique will be demonstrated through experimental results in Chapter 5.

- A second-order cable equalizer for 100Mb/s transmission was then simulated. The equalizer zero frequency and DC gain were adapted based on two pieces of information derived from the output “eye” diagram. The results show that the algorithm optimized the filter response at frequencies corresponding to the test pattern selected for computing the error signal.
- While a higher-order filter can be implemented using cascade of biquads whose parameters are scaled multiples of the biquad being adapted, it was decided to look at general adaptation of the actual filter. This approach requires the correlation of an error and gradient signals. The biquad tuning techniques were extended to a fourth-order equalizer whose zeros were adapted. For this filter, the output pulse shape was curve fitted to a desired shape by testing for bit patterns and comparing the equalizer output with an expected output. The results show that the proposed technique is feasible for adaptive equalization over a fairly wide channel variation.
- As a final demonstration of possible application areas, an adaptive equalizer for the magnetic recording channel was investigated. While the results were based on preliminary simulations, it appears that the adaptation techniques are feasible in providing analog adaptive equalizers for this channel.

CHAPTER 4

Circuit Integration

Electronic filters consist of building blocks or integrators which, when interconnected in loops, produce a desired filtering function. Generally, the filter pole and zero frequencies depend on the integration time-constant of the constituent integrators. Five possible integrator technologies exist for implementing analog filters including discrete RLC, active-RC, MOSFET-C, transconductance-C (G_m -C), and active-LC. At the VHF range, the technology receiving most attention and the chosen technology for this project is G_m -C [Nauta 92], [Lee 93], [Laber 93], [Rezzi 93], [Veirman 92], [Koyama 93], [Wyszynski 93], [Georgantas 93], and [Dupuie 90]. In this chapter, the issues pertaining to the design of a transconductor are addressed, and a comparison of state of the art transconductors is given. Finally, a new transconductor topology is proposed for this project in the light of these issues.

4.1 Transconductance Amplifiers

A transconductor is a voltage to current converter whose transconductance is defined to be G_m . When loaded with a capacitor, C , an integrator is achieved. Since typically a transconductor consists of an open loop single-stage amplifier, high signal processing speeds can be achieved relative to filters implemented using other technologies except for monolithic active-LC filters, which are presently feasible only at ultra-high frequencies.

A G_m - C integrator exhibits an integration time-constant that depends on the ratio C/G_m which is not well controlled in IC processes. Thus, any transconductor must incorporate a tuning mechanism to account for process variations. The tuning component, being a critical design aspect, is therefore the major classification property for all possible transconductors. Based on this property, the numerous transconductors that have been reported in the literature can be grouped into three categories in the three process technologies: CMOS, bipolar, and BiCMOS. Examples of transconductors from each of the categories is shown in Figure 4.1. Notice that the transconductors in the figure are balanced to optimize linearity and SNR, and thus, dynamic range. In this section, the tuning component and relevant issues to consider in the design of a transconductor are addressed. As well, the performances of each of the transconductor styles in Figure 4.1, in light of these issues, are evaluated.

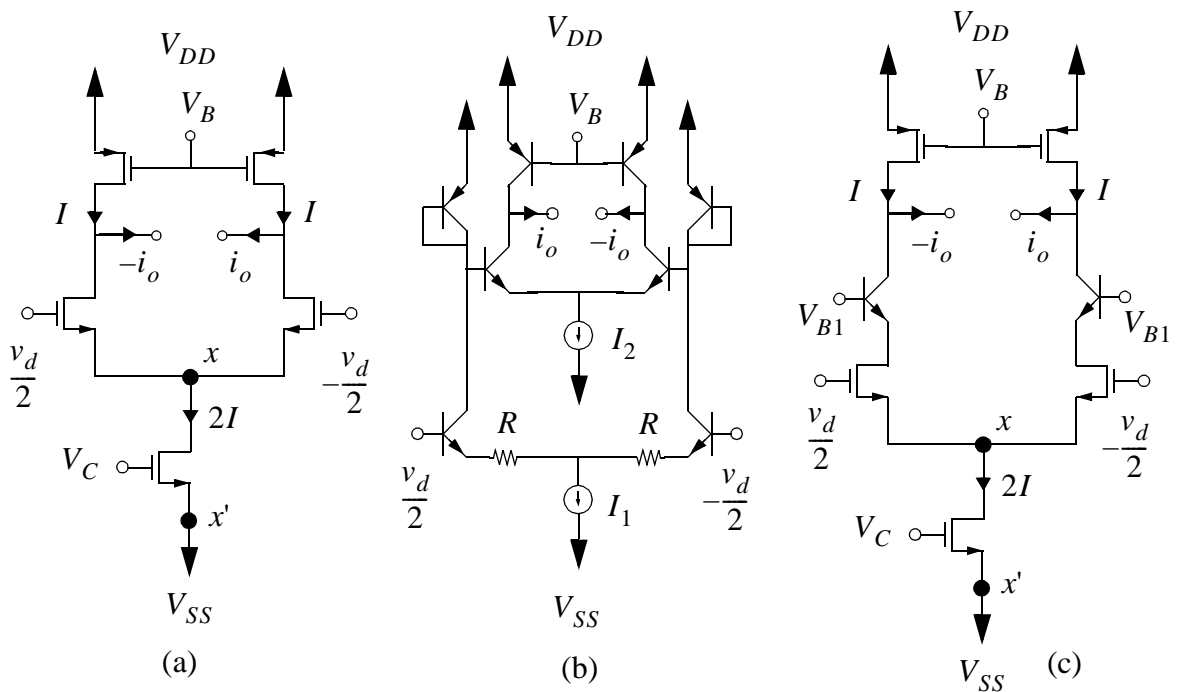


Figure 4.1: Illustrating three examples for transconductor tuning styles. Shorting nodes x and x' in Figures 4.1a and 4.1c is optional.

4.1.1 Tuning Mechanism: Trade-offs and Limitations

Since the ratio G_m/C defines the filter pole and zero frequencies, tuning is achieved by adjusting either G_m , C , or both. Switching in capacitors was reported in [Snelgrove 92] to allow tuning over the entire VHF range as well as in [Durham 92]. To occupy minimal integrated circuit area, the load capacitors were achieved by successively switching in parasitic capacitors of a series connected chain of MOS devices [Snelgrove 92]. Although this technique provides a broad tuning range, it is not the preferred practice for high-frequency on-line tunable filters where the parasitic effects the switches introduce (when capacitors are switched in and RC products) hinder performance, and where transient errors from switching may impair performance. For this reason, most transconductors in the literature focus on techniques to adjust G_m at a cost in a reduced tuning range. Defining the tuning range as $G_{m,max}/G_{m,min}$, the challenge is to optimize this ratio to permit tuning against process as well as channel variations while maintaining satisfactory filtering performance over the entire tuning range.

Consider the transconductor depicted in Figure 4.1a. Examples of transconductors classified under this category include [Culbert 86], [Culbert 88], [Nauta 92], [Plett 86], [Snelgrove 92], and [Lee 93]. These transconductors consist of an MOS input pair in the pinch-off mode whose transconductance governs the overall G_m . Tuning is achieved by varying the input-pair tail bias current [Plett 86], the input-pair gate bias level [Snelgrove 92], or the supply voltage [Nauta 92]. The tuning range for these transconductors is relatively low, about 2, especially in a leading edge technology. The mechanisms that limit the effective tuning range are transconductor input dynamic range or linearity, mobility degradation, velocity saturation, and output conductance as explained below.

Consider Figure 4.1a where tuning is achieved by varying the tail bias current $2I$. It can be easily shown that the input device transconductance is

$$m = \frac{\partial i_{DS}}{\partial v_{GS}} = 2\sqrt{IK} \quad (4.1)$$

where $K = \mu_o C_{ox} W/2L$ and the well known quadratic equation for a MOSFET in pinch-off was used. The overall circuit transconductance is ideally

$$\begin{aligned} G_m &\equiv \frac{i_o}{v_d} \\ &= \frac{g_m}{2} \end{aligned} \quad (4.2)$$

To maintain the input devices in saturation, it can also be shown that the maximum input signal should satisfy

$$|v_d| \leq \sqrt{2I/K} \quad (4.3)$$

Hence, tuning for low transconductance (lower frequencies, lower tail bias current) implies a lower input dynamic range, or alternatively, reduced linearity for a fixed peak differential signal swing.

Consider once again Figure 4.1a, but with node x shorted to node x' resulting in the transconductor described in [Snelgrove 92]. The circuit transconductance is

$$G_m = K(V_{CM} - V_t) \quad (4.4)$$

and can be tuned by adjusting V_{CM} . However, to prevent input device cutoff, the condition that must be satisfied is

$$|v_d| < 2(V_{CM} - V_t) \quad (4.5)$$

Once again, it can be noted that tuning for lower transconductance degrades input dynamic range. In a similar manner, it can be shown that the condition for the transconductor in [Nauta 92] is

$$|v_d| < 2(V_{DD} - V_t) \quad (4.6)$$

where V_{DD} is used to tune the transconductance, and again, tuning comes as a trade-off to input dynamic range. Consequently, to maintain a given linearity, the tuning range must be limited.

The second and more severe mechanism which limits the tuning range of these transconductors is device physical properties, most notably short-channel effects such as degradation of mobility and velocity saturation. A model for the MOSFET output current that models mobility degradation is [Duvvury 86], [Toh 88], [Chan 92]

$$i_D = K \frac{(v_{GS} - V_t)^2}{1 + \theta(v_{GS} - V_t)} \quad (4.7)$$

where θ depends on the vertical field in the channel. The model correctly predicts that short-channel devices are nearly linear at high v_{GS} . Consequently, from (4.1), g_m approaches a constant when $\theta(v_{GS} - V_t) \gg 1$ reducing the tuning range to 1. However, the expression for drain current becomes somewhat more complex when the effects of velocity saturation are included [Toh 88]. Fortunately, this effect also tends to linearize the output current in v_{GS} . However, it results in constant transconductance, and hence, degradation in the tuning range. These short-channel effects on device transconductance are shown in Figure 4.2. From the Figure, it is evident that the variation in g_m over a given span in v_{GS} is much reduced for the short-channel device relative to the ideal device implying a reduced effective tuning range. For completeness, it should be noted here that in [Snelgrove 92] a tuning range of 2 was experimentally obtained (without switching in capacitors), and a tuning range of 1.3 was obtained for a $0.8\mu\text{m}$ BiCMOS version [Ryan 92] of the circuits reported in [Nauta 92].

Another device physical parameter that affects the practical tuning range is device output conductance g_o , which normally sets the transistor output resistance R_o . This parameter increases with increasing device current and reduced feature size. Modern transistors have a

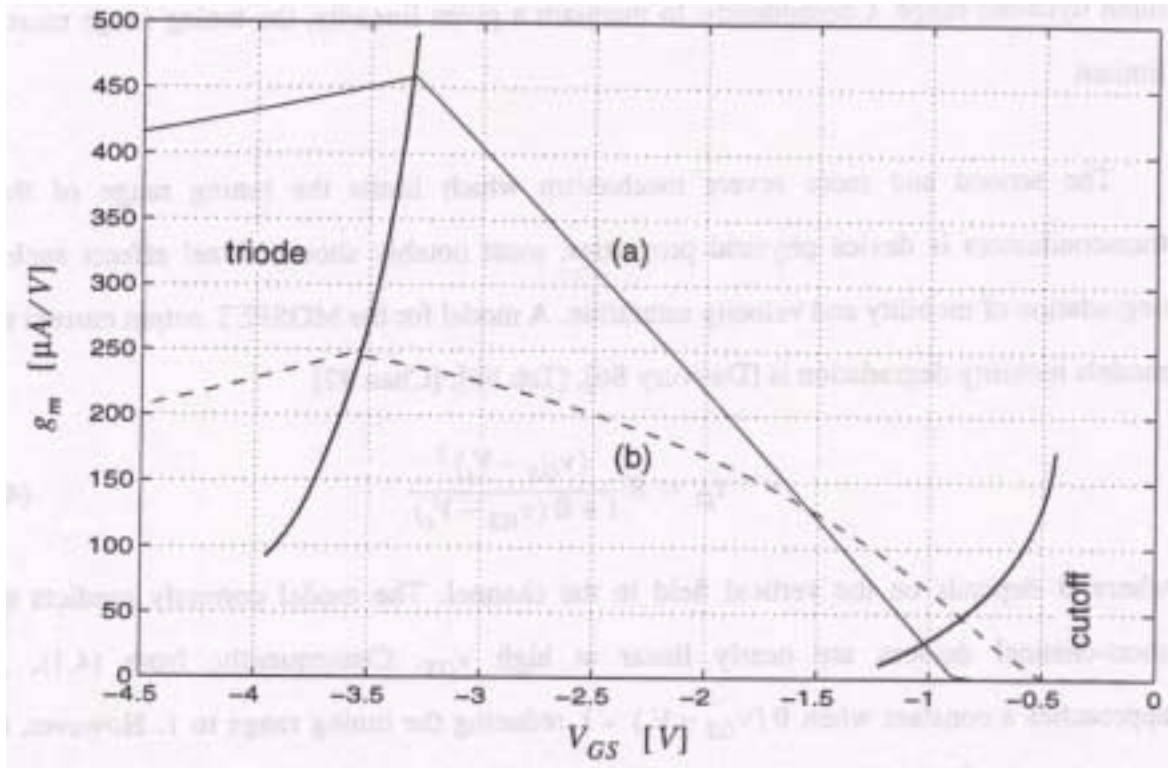


Figure 4.2: Simulated device transconductance for a 5.0 μ m/0.8 μ m PMOS transistor as function of gate-source bias with source-drain bias at 2.5V using: the level 1 (ideal square law) model (a) and the level 3 (short-channel) model (b).

large output conductance. Consequently, transconductors optimized for speed will exhibit a low DC gain, or $G_m R_o$. As the transconductor DC gain approaches unity, the element ceases to become a useful block. Hence, the tuning range is bounded by the available DC gain.

Figure 4.1b depicts the most common transconductor style in a bipolar process [Koyama 93], [Moree 93], [Veirman 92], [Veirman 93]. The tuning mechanism makes use of the log-antilog function of bipolar transistors and it can be shown that for ideal devices the overall transconductance is

$$G_m = \frac{I_2}{2RI_1} \quad (4.8)$$

Since G_m depends on the ratio of two bias currents, a transconductor with a large tuning range would exhibit a large power dissipation, and thus, places a limit on the available tuning range. In addition, limitations on the tuning range also come from input dynamic range constraints [Moree 93], [Rezzi 93], [Veirman 93], and shallow-junction effects as was the case for the CMOS transconductors. For example, to maintain the input devices in the active mode, it can be shown that the input signal swing should satisfy

$$|v_d| \leq 4I_1 R \quad (4.9)$$

Should one tune I_1 , the trade-off between tuning range and input dynamic range is quite evident. Alternatively, choosing to tune I_2 affects transconductor linearity and the effect is more severe in a shallow-junction processes where the ohmic emitter resistance tends to linearize the devices, in which case the log-antilog function is not ideally obeyed. This effect becomes more severe as the values of I_1 and I_2 differ, hence limiting the tuning range [Moree 93]. It appears from the literature that the tuning range for these transconductor styles varies between 2-5 [Koyama 93], [Moree 93], [Veirman 92].

For the BiCMOS transconductor in Figure 4.1c, the MOSFETs are operated in the linear or triode region and tuning depends on one of two possible topologies. In the first topology, the input voltage is supplied to the gate terminals of the MOSFETs, while their drain-source voltage, V_{DS} , is tuned by varying the base voltage of the bipolar devices to set the output transconductance [Alini 92], [Gatti 90], [Laber 93]. For this style, shorting node x to node x' as in [Laber 93], or leaving the current source in place as in [Alini 92] is optional. The transconductance for these transconductors can be shown to be

$$G_m \sim K \frac{V_{DS}}{1 + \frac{V_T}{V_{DS}}} \quad (4.10)$$

In the second topology, the input signal is supplied to the bipolar transistors while the MOSFETs realize an active emitter degeneration [Rezzi 93], [Baschiroto 93], [Tsividis 88],

[Martinez 93]. Tuning is achieved by varying the gate-source voltage, V_{GS} , of the MOSFETs, hence, the degeneration resistance sets the transconductance as follows

$$G_m = K(V_{GS} - V_t - V_{DS}) \quad (4.11)$$

Since the MOSFETs must remain in the linear region of operation, V_{DS} must be kept low otherwise transconductor non-linearity would rise. Consequently, the tuning range, as can be noted from (4.10), is constrained. For the second topology, the same linearity requirement constrains the variation in V_{GS} , and hence, the tuning range. These issues are discussed in [Rezzi 93] wherein a tuning range of 3 is predicted for the second transconductor topology. Typically though, for these transconductor styles a tuning range between 2-4 has been achieved. Here again, transconductor DC gain places a bound on the practical achievable tuning range.

Finally, it should be noted that various tuning mechanisms not only affect input dynamic range but may affect transconductor output common-mode level (see Section 4.1.3) [Plett 86] and output resistance. Specifically, in the transconductor of Figure 4.1a, the output resistance is inversely proportional to the bias current. Since tuning is achieved by varying the bias current, the net result is gain modulation as function of tuning. This effect can lead to tuning errors when the transconductor DC gain is used for tuning control, as variation in output resistance will interfere with adjustments in G_m .

4.1.2 Transconductor Frequency Response

An ideal integrator exhibits a phase response that lags by 90° over all frequencies. However, finite DC gain results in phase lead at low frequencies and parasitic poles lead to phase lag at high frequencies [Peterson 87]. It is therefore desirable to synthesize a transconductor with high DC gain and to place parasitic poles far from the unity-gain frequency, f_u , of the integrator which sets the maximum filter pole-frequencies. Since state-of-the-art bipolar devices exhibit lower output conductance and higher device transition

frequency, f_t , it is reasonable to expect higher transconductor DC gain and parasitic poles at higher frequencies in a complementary bipolar process relative to a CMOS or a BiCMOS process.

4.1.3 Transconductor Common-Mode Response and Offset

Since it is preferable to use fully balanced integrators when implementing high-frequency filters, a transconductor requires a mechanism, namely a common-mode feedback circuit, to set the common-mode level and prevent common-mode signal build-up from stage to stage. Note that when integrators are interconnected in loops to implement a filter, the differential circuit realizes a negative feedback loop while the common mode loop can be in positive feedback. Thus, to prevent instability, the common-mode feedback circuit must be designed such that the transconductor common-mode frequency response is smaller than unity over all frequencies. To prevent transient errors from potential common-mode disturbances, the common-mode feedback (CMFB) circuit must be relatively fast.

A common-mode feedback circuit usually detects the common-mode level of the transconductor output and supplies a correction signal through feedback, as shown in Figure 4.3. Letting the closed loop transfer-function of the CMFB circuit be represented by $\beta(s)$,

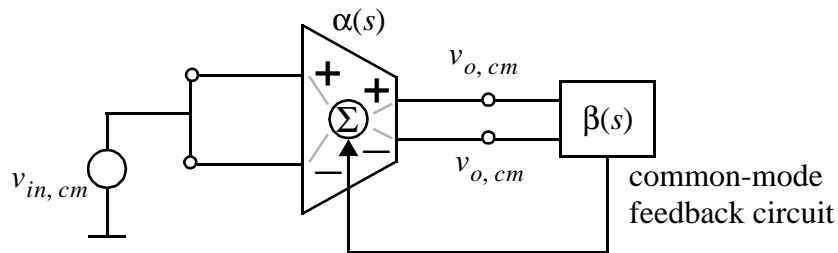


Figure 4.3: Illustrating the mechanism of common-mode feedback.

while the transconductor common-mode gain be represented by $\alpha(s)$, the following system transfer-function can be obtained:

$$\frac{v_{o, cm}(s)}{v_{in, cm}(s)} = \frac{\alpha(s)}{1 + \beta(s)} \quad (4.12)$$

It is therefore desirable to keep the response in (4.12) smaller than unity to ensure stability — typically by making $\alpha(s)$ small and $\beta(s)$ large.

When the common-mode feedback circuit suffers from non-linearity, the detected signal may contain a component term that depends on the transconductor differential output, causing differential to common-mode conversion. When fed-back, this component will force the transconductor half-circuit outputs to be asymmetrical displaying distortion. Thus, the non-linearity of the common-mode feedback circuit must be low enough over the entire differential output swing of the transconductor, so that it does not significantly degrade differential loop linearity.

Another issue to point out here is transconductor output common-mode variation or offset that results from the tuning mechanism. For example, in the transconductors of Figure 4.1, tuning will affect output common-mode. Naturally, the common-mode feedback circuit will attempt to correct for this effect. However, this additional burden on the common-mode feedback circuit is not desirable as it can leave its linear range of operation. It is possible to alleviate this effect by biasing the load transistors such that the current they produce will track the tuning control current. In this way, the common-mode feedback circuit is left to take care of common-mode fluctuations rather than tuning disturbances. However, this approach has not been pursued in [Plett 86], [Veirman 90], [Veirman 92], and [Gatti 90].

4.2 State of the Art Transconductors

Table 4.1 compares the performance of the transconductors presented in the recent literature. For the BiCMOS transconductors, the technology is specified according to the MOS channel length and the BJT f_t . Observe that the tuning ranges are limited to about 2 in a leading-edge CMOS process, 2-5 in a bipolar process, and 2-4 in a BiCMOS process. The limitations come from the issues discussed above and/or supply voltage limitations. Observe that to date, the fastest experimental reported transconductor has been by [Snelgrove 92]. The transconductors in [Wyszynski 93] and [Wyszynski 93b] are based on simulated Spice results using ideal Level 2 models and ideal *QuickChip*TM bipolar models, respectively. For the transconductors chosen for this project, the aim was to optimize transconductor tuning range while maintaining state-of-the-art performance in terms of transconductor speed.

Table 4.1: Comparison of reported transconductors.

Reference	Technology	$f_{u,max}$	Tuning Range	Power
Culbert 88	5 μ m CMOS	5MHz	12.4:1	50mW @ ± 5 V
Plett 86	5 μ m CMOS	630Hz	3.2:1	± 5 V
Wyszynski 93	2 μ m CMOS	1.59GHz	1.3:1	40mW @ ± 5 V
Lee 93	2 μ m CMOS	42MHz	1.8:1	5mW @ 5V
Snelgrove 92	0.9 μ m CMOS	300MHz	2:1	4mW @ ± 2.5 V
Angelo 90	3 μ m CMOS	9MHz	9:1	<50mW @ ± 5 V
Martinez 92	1.5 μ m CMOS	14MHz	2:1	<36mW @ ± 2.5 V
Nauta 92	3 μ m CMOS	98MHz	4.5:1	10V
Stefanelli 93	2 μ m CMOS	7MHz	10:1	30mW @ 5V
Moree 92	3GHz bipolar	7.5MHz	1.7:1	20mW @ ± 5 V
Veirman 92	9GHz bipolar	10MHz	5:1	10mW @ 5V
Veirman 90	bipolar	15MHz	3:1	5V
Koyama 93	2.5GHz bipolar	100MHz	1.7:1	7.5mW @ 5V
Wyszynski 93b	8GHz bipolar	2.7GHz	1.5:1	28mW @ ± 5 V
Alini 92	3 μ m BiCMOS	32MHz	4:1	7.5mW @ 5V
Fichtel 92	3 μ m-1.6GHz BiCMOS	10.7kHz	4:1	± 2.5 V
Baschiroto 93	2 μ m-7GHz BiCMOS	67MHz	1.7:1	1mW @ 5V
Laber 93	1.5 μ m-4GHz BiCMOS	20MHz	4.3:1	5V
Rezzi 93	1.2 μ m-5GHz BiCMOS	80MHz?	3:1, 10:1	3.5mW @ 5V

4.3 BiCMOS Transconductor Design

In this section, a new G_m - C topology, implemented for analog adaptive filter prototyping, is described. The key features of this transconductor are:

- It maintains state-of-the-art speed while dissipating reasonable power.
- It attains a wide tuning range by making use of a Gilbert multiplier for tuning via current steering.

- Since tuning does not require adjustment of the input-stage bias conditions, the tuning mechanism does not affect the input-stage dynamic range, and it is linear in the AC signal current.
- To maximize input-stage linearity, the input devices lack a tail bias current source. This technique results in a linear input stage when devices obey the ideal square law model. For short-channel devices, the lack of the tail-bias current source maximizes input-stage overdrive voltage for improved linearity.
- To ensure low common-mode gain, the input signal is applied to both signal paths (i.e. the transconductor load devices also serve as input devices). This feature also doubles the conversion efficiency.

The above key features, as well as other relevant issues such as frequency response, linearity, noise, common-mode response, offset, and output resistance are addressed. The circuits discussed were all implemented in Northern-Telecom's 0.8 μ m-10GHz, BiCMOS process.

4.3.1 Tuning Mechanism

Since the prime objective here is the ability to adapt against process and channel variations, a wide transconductor tuning range is necessary. To achieve this requirement, we make use of a Gilbert multiplier cell as a current steering mechanism to allow tuning while maintaining signal linearity. The transconductor is shown in Figure 4.4 where the aspect ratio for all the MOS transistors is 5 μ m/0.8 μ m with the exception of M_5 - M_8 which are each 2.5 μ m/0.8 μ m. The input MOS devices all have small aspect ratios to maximize processing speed as these devices' gate capacitance becomes part of the integration capacitance. The small aspect ratio compared with ordinary O/A style design means that mismatch effects are large. Consequently, transconductor CMRR is expected to be low. The BJT transistors all have 4 μ m x 0.8 μ m emitters (NN51111X [BATMOS 91]). The differential input stage consisting of the PMOS transistors M_1 and M_2 produces a differential current, $\pm i$, that is shunted by the

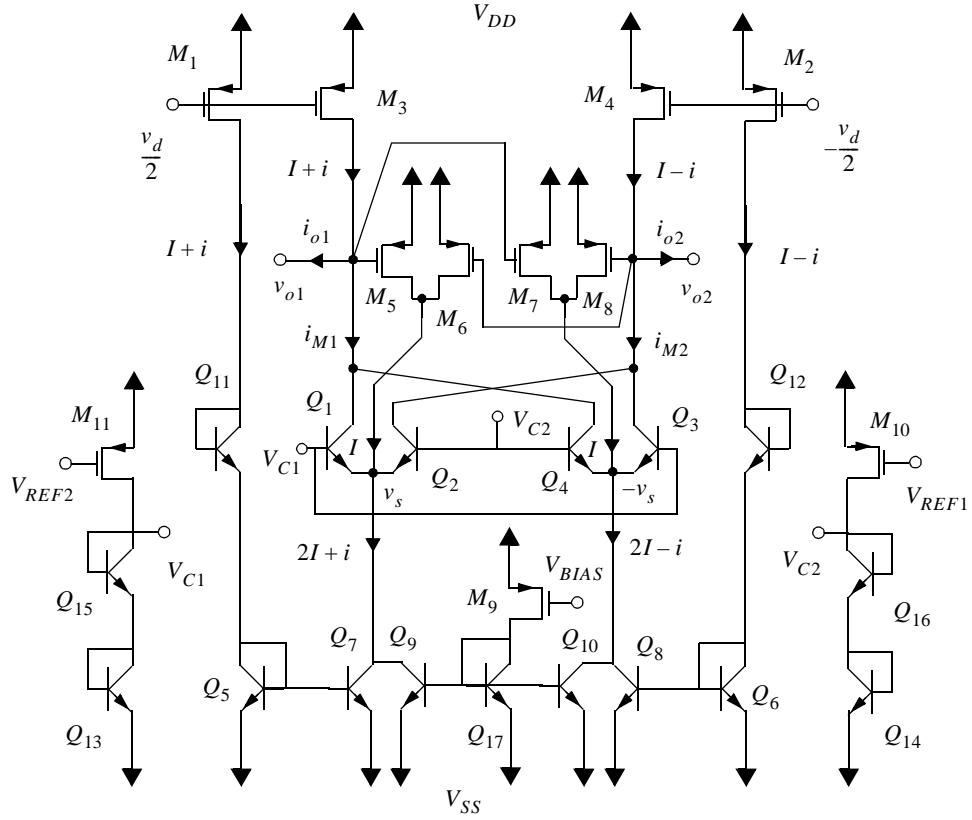


Figure 4.4: The BiCMOS transconductor; also F-cell.

Gilbert cell consisting of the BJTs Q_1 - Q_4 . The currents i_{M1} and i_{M2} appearing at the multiplier output ports are

$$\begin{aligned}
 i_{M1} &= i_{C1} + i_{C4} \\
 &= \frac{(I+i)\alpha}{1 + e^{-(V_{C1}-V_{C2})/V_T}} + \frac{(I-i)\alpha}{1 + e^{(V_{C1}-V_{C2})/V_T}}
 \end{aligned} \tag{4.13}$$

and

$$\begin{aligned}
 i_{M2} &= i_{C2} + i_{C3} \\
 &= -\frac{(I+i)\alpha}{1 + e^{(V_{C1}-V_{C2})/V_T}} + \frac{(I-i)\alpha}{1 + e^{-(V_{C1}-V_{C2})/V_T}}
 \end{aligned} \tag{4.14}$$

For $\alpha \sim 1$, equations (4.13) and (4.14) solve to:

$$i_{M1} = I + i \tanh\left(\frac{V_{C1} - V_{C2}}{2V_T}\right) \tag{4.15}$$

$$i_{M2} = I - i \tanh\left(\frac{V_{C1} - V_{C2}}{2V_T}\right) \quad (4.16)$$

where the control voltages V_{C1} and V_{C2} are used for tuning.

The transconductor in Figure 4.4 also contains a second input stage consisting of the PMOS transistors M_3 and M_4 which have the same aspect ratios and IC layout as M_1 and M_2 . Therefore, the net currents i_{o1} and i_{o2} appearing at the transconductor output terminals v_{o1} and v_{o2} , respectively are:

$$\begin{aligned} i_{o1} &= \left(1 + \tanh\left(\frac{V_{C2} - V_{C1}}{2V_T}\right)\right) i = -i_{o2} \\ &\equiv i_o \end{aligned} \quad (4.17)$$

The transconductance of the circuit in Figure 4.4 is

$$\begin{aligned} G_m &= \frac{i_o}{v_d} \\ &= \frac{1}{2} \left(1 + \tanh\left(\frac{V_{C2} - V_{C1}}{2V_T}\right)\right) g_m \end{aligned} \quad (4.18)$$

where:

$$g_m = \frac{\partial i_{D, M_1}}{\partial v_{GS, M_1}}, \quad i = i_{D, M_1} \quad (4.19)$$

Observe from (4.17) that, owing to the bipolar Gilbert multiplier cell, the tuning mechanism is linear in the signal current i , thus, input dynamic range is not compromised thereby as was the case for the transconductors discussed in section 4.1.1.

The transconductor in Figure 4.4 provides only positive *or* negative values for transconductance, or “2-quadrant” operation, as evident from (4.18) depending on its inter-connectivity within the filter network. To provide a transconductor that can be tuned for *both* positive and negative transconductance values, or “4-quadrant” operation, a second embodiment is described next.

Four-quadrant operation is obtained with the transconductor of Figure 4.5 which is similar to Figure 4.4 in all respects with the exception that the second differential input stage is replaced by the second differential input stage consisting of the PMOS transistors M_{31} , M_{32} , M_{41} , and M_{42} . These transistors have aspect ratios *half* the aspect ratios of the transistors M_1

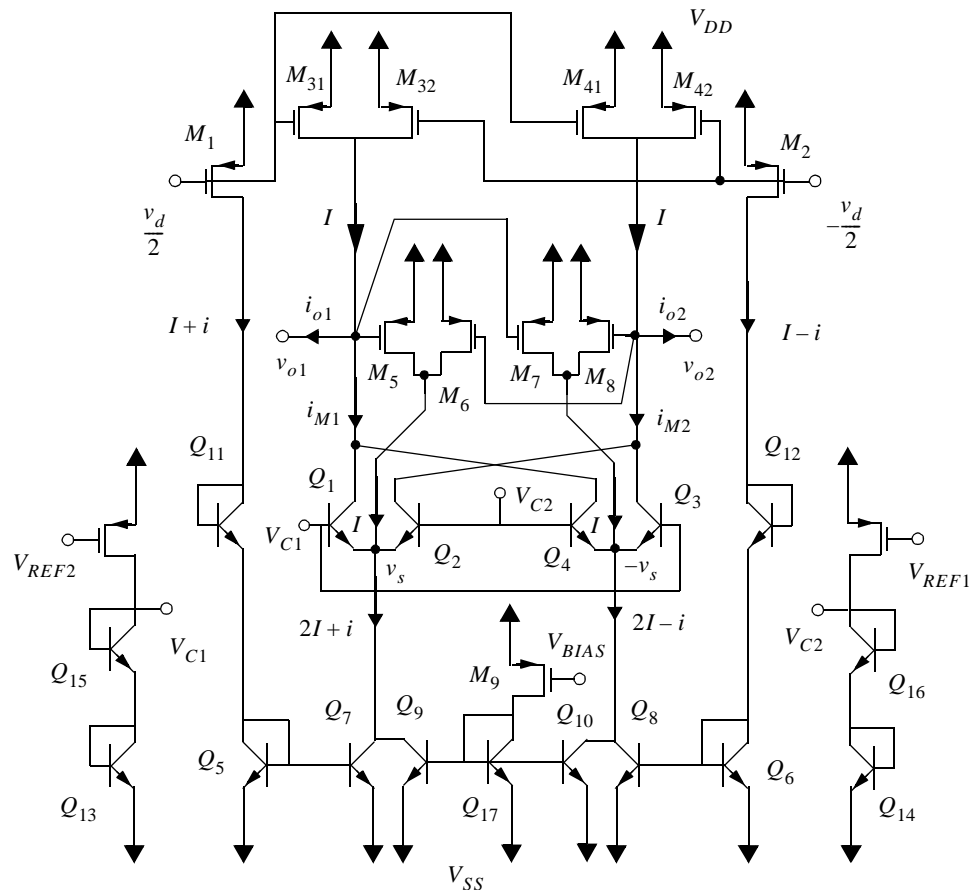


Figure 4.5: The second BiCMOS transconductor; also Q-cell.

and M_2 . In the IC layout, each of the transistors M_1 and M_2 consist of two parallel transistors each matched to the transistors comprising the second input stage. The transconductance of the circuit in Figure 4.5 is:

$$G_m = \frac{1}{2} \tanh\left(\frac{V_{C2} - V_{C1}}{2V_T}\right) g_m \quad (4.20)$$

The transconductance characteristics given by (4.18) and (4.20) are illustrated in Figure 4.6 as function of the multiplier control voltages. Notice that while the transconductor of

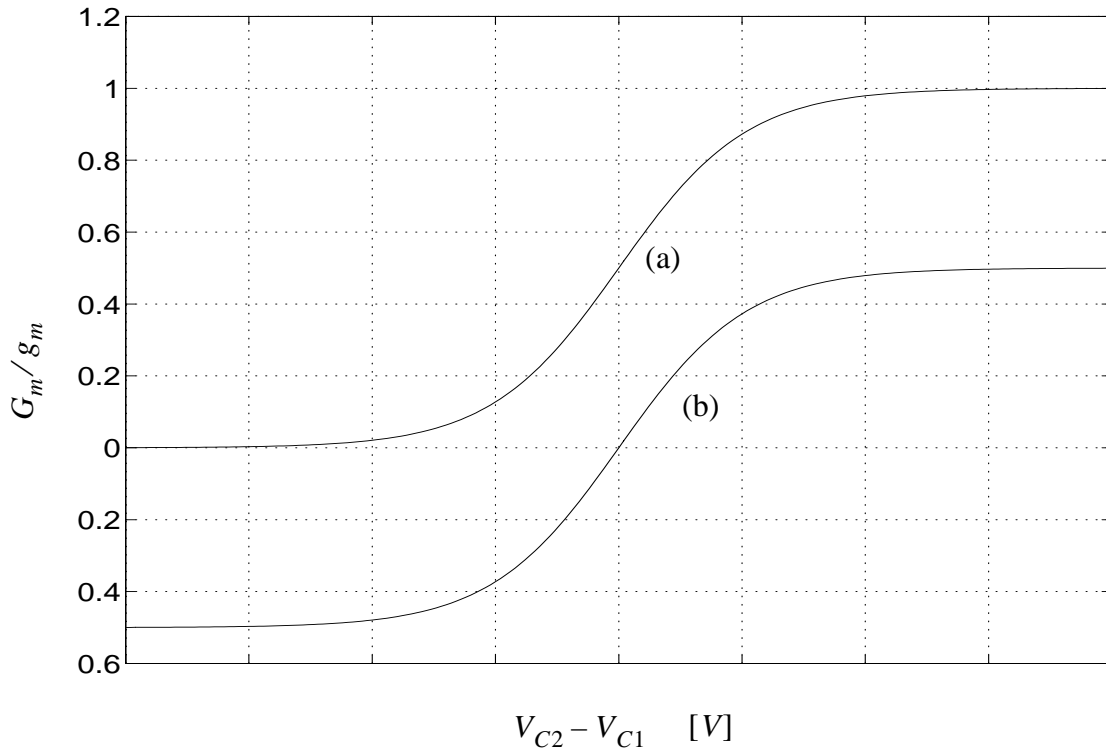


Figure 4.6: Theoretical transconductance characteristics for a) F-cell, b) Q-cell.

Figure 4.5 can be tuned for both positive and negative values for G_m , this transconductor runs half as fast as the transconductor in Figure 4.4 at similar quiescent power dissipation. Hence, when optimizing for speed for a specified power dissipation, transconductors realized using the topology of Figure 4.5 should only be used where tuning for both positive and negative transconductance is required, such as for cancelling transconductor finite output conductance as will be explained later.

Observe also that the entire tuning curves, shown in Figure 4.6, span a tuning voltage range of $\pm 4V_T$. Although the parasitic ohmic emitter resistances of the BJTs Q_1 - Q_4 may tend to linearize the curve and expand the voltage span, the resultant span would still be too narrow

for practical on-line tuning purposes. For this reason, the transconductors in Figures 4.4 and 4.5 each contain two buffer circuits shown on either side of the transconductors. These circuits expand the tuning voltage span to $\pm 1.75V$ between terminals V_{REF1} and V_{REF2} as shown in the simulated output curve in Figure 4.7 for both transconductors. In addition, the buffers

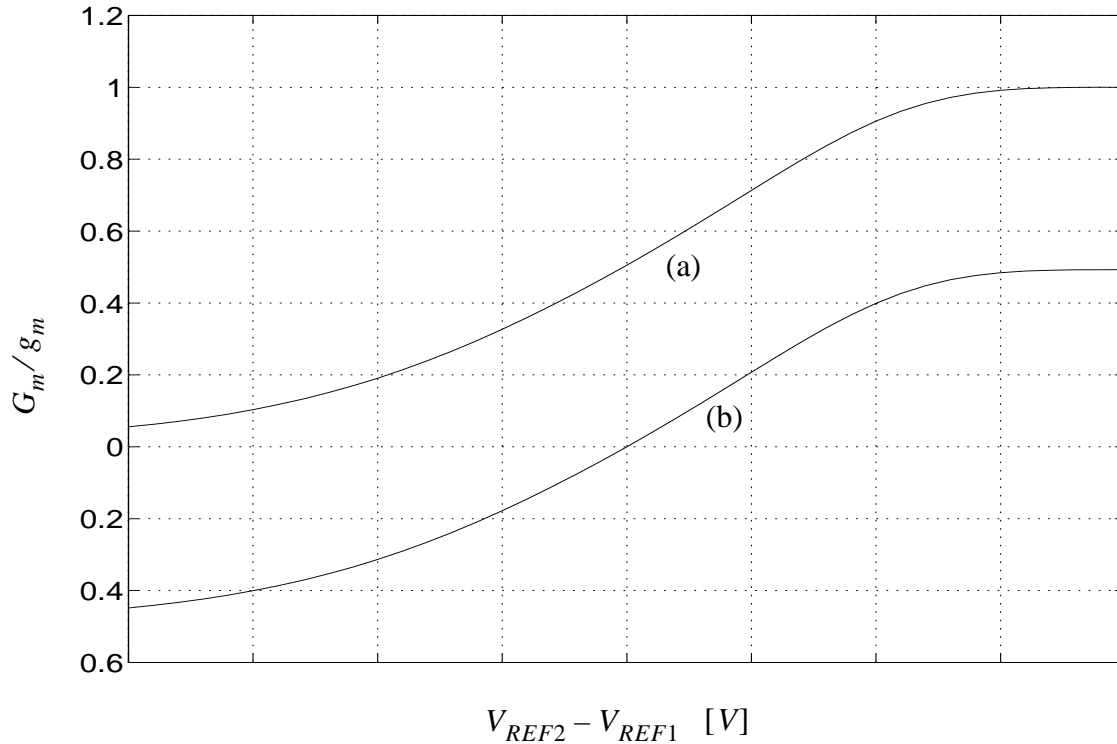


Figure 4.7: Simulated transconductance characteristic for a) F-cell, b) Q-cell

provide isolation between the control DC sources and any components of the AC signal that appear at V_{C1} and V_{C2} , as well as a low impedance load to AC ground.

From the curves in Figure 4.7, it appears that the tuning range for each transconductor should be infinite; however, the practical tuning range is about 17. This limit comes from the fact that the transconductor DC gain, $G_m R_o$, is 17. Hence, if G_m is tuned such that the DC gain becomes smaller than unity, the capacitively loaded transconductor, or integrator, will cease to be a useful block.

4.3.2 Linearity

Transconductors typically feature low linearity in the output current as function of the input voltage since they run open loop without local feedback. While linearization techniques are sometimes employed such as in [Durham 92], [Dupuie 90] and [Willingham 94], these techniques tend to compromise speed performance. To attain reasonable linearity, we make use of the approach presented in [Snelgrove 92]. Specifically, the standard differential-pair topology was modified by removing the input-pair tail bias current source as evident from Figures 4.4 and 4.5. For matched MOS input devices obeying the ideal square law expression, $\theta(v_{GS} - V_t) \ll 1$ in (4.7), it can be shown that the output current of both transconductors is linear in the input-signal voltage. When the input devices depart from the ideal conditions, linearity will degrade. However, for the short-channel devices implemented, the parameter θ in (4.7) tends to be large due to the higher vertical field that result in mobility degradation. Hence, mobility degradation combined with velocity saturation effects enhance linearity as discussed in Section 4.1.1 — especially at high overdrive voltage, $V_{GS} - V_t$, [Chan 92] which is maximized when the tail bias current source is removed.

Since the tuning mechanism relies on current steering rather than on input stage bias adjustment, tuning does not affect the bias conditions of the input stages. Hence, as can be noted from (4.17), *input-stage* linearity is preserved throughout the tuning range.

Figure 4.8 shows the simulated differential output current for the two transconductor styles as a function of the differential input voltage. The curves in Figure 4.8 show three distinct regions: region 1 is where both input devices are in pinch-off or the useful region of operation, region 2 is where one input device enters cutoff (depending on input signal polarity), and region 3 is where one device enters the triode region while the other is still in cutoff (depending on input signal polarity). These regions are differentiated and numbered respectively. A quantitative analysis for the input stage can be done to show that region 1 is

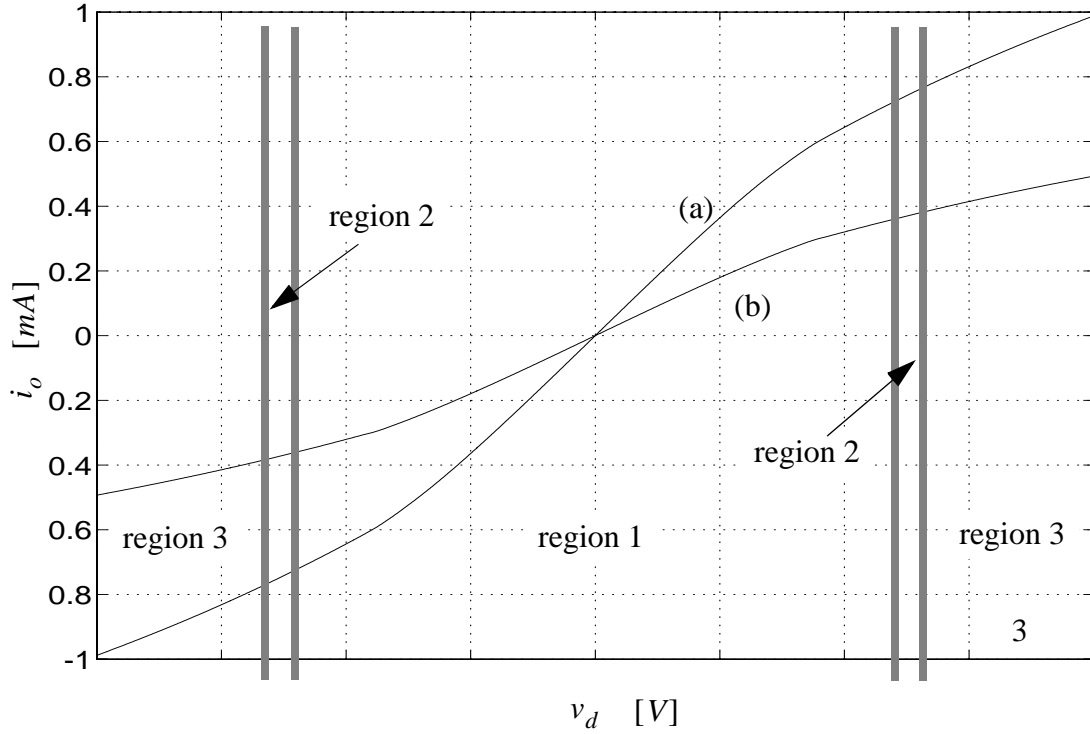


Figure 4.8: Output current vs. input voltage for the a) F-cell, b) Q-cell circuits.

bounded by the condition in (4.5), where V_{CM} is 2.5V and V_t is 0.8V in our case, while region 3 is bounded by the condition

$$|v_d| \geq 2(V_{SS} + 2V_{BE} - V_t) \quad (4.21)$$

Region 2 consists of the area where the input voltage is in between the bounds given by (4.5) and (4.21). For our case, V_{BE} is also about 0.8V. Hence, region 2 disappears and was shown in Figure 4.8 for illustration purposes only. From Figure 4.8, it is evident that the linear (useful) range spans a differential input signal swing of $\pm 2V$ for $\pm 2.5V$ supplies.

Since the Gilbert multiplier is linear in the input current, the overall linearity of the transconductor will depend on the linearity of the input stage depicted in Figure 4.8 and the relative matching of the devices. In terms of linearity as function of tuning, one would expect degradation in signal to distortion ratio at lower G_m where transconductance subtraction takes

place and where the distortion terms may not subtract effectively. Another effect that may degrade linearity is signal path phase error discussed in Section 4.3.4.

4.3.3 Noise

In this design, noise was not a major specification for the intended application as a SNR in the range 30-40dB is sufficient for the pulse-shaper. However, noise can be an issue.

The major sources of noise in the transconductors are the MOSFET shot noise, $\overline{i_d^2}$, the BJT shot noise, $\overline{i_s^2}$, and BJT base resistance thermal noise, $\overline{i_{rb}^2}$. These noise current densities appearing at the drain and collector terminals of the MOS and BJT devices, respectively, are modelled as follows [Gray 93]

$$\overline{i_d^2} = \frac{8}{3}kTg_{m,MOS} \quad [A^2/Hz] \quad (4.22)$$

$$\overline{i_s^2} = 2qI_C \quad [A^2/Hz] \quad (4.23)$$

$$\overline{i_{rb}^2} = 4kTr_b g_{m,BJT}^2 \quad [A^2/Hz] \quad (4.24)$$

where $g_{m,MOS}$ is the transconductance of the MOSFET, I_C is the collector current of the bipolar transistor, r_b is its base resistance, and $g_{m,BJT}$ is its associated transconductance. Typically, (4.23) and (4.24) are combined to give a net collector noise current density of

$$\overline{i_c^2} = 4kTg_{m,BJT}^2 \left(r_b + \frac{1}{2g_{m,BJT}} \right) \quad [A^2/Hz] \quad (4.25)$$

To determine output noise power density for either transconductor, we consider the major noise generating devices $Q_1 - Q_{10}$, $M_1 - M_9$, and the following two cases.

Case A: $V_{C2} = V_{C1}$. For this case, it can be noted that noise currents produced by M_1, M_2, M_9 , and $Q_5 - Q_{10}$ will split evenly at nodes $\pm v_s$, leading to correlated common-mode current noise components at the half-circuit outputs. Thus, when taken differentially, the net differential noise power due to these noise sources will be zero. The noise power produced at the output will come from $Q_1 - Q_4$, and $M_3 - M_8$. Considering for

now only the bipolar devices, as these dominate noise performance, the peak differential output noise power density due to each BJT $Q_1 - Q_4$ can be shown to be given by

$$\overline{v_{m,pk}^2} = 4kT \frac{g_{m,BJT}^2}{16} \left(r_b + \frac{1}{g_{m,BJT}} \right) (2R)^2 \quad [V_{rms}^2/Hz] \quad (4.26)$$

where R is the half-circuit output resistance and $g_{m,BJT} = I/V_T$ for the transconductors in Figures 4.4 and 4.5 (note that each BJT $Q_1 - Q_4$ has half the bias current I). When the transconductor integrators are tuned either fast or slow, the equality is not maintained and the output noise due to these BJTs will drop owing to emitter degeneration effects. Specifically, as will be shown in Section 4.3.3.1, degeneration reduces the effective noise gain. A graph illustrating the transconductor simulated differential output noise power densities due to a single BJT within the Gilbert multiplier and normalized to $1/\overline{v_{cm,pk}^2}$ (defined below) as function of tuning control is shown in Figure 4.9. Observe that thermal noise dominates shot noise.

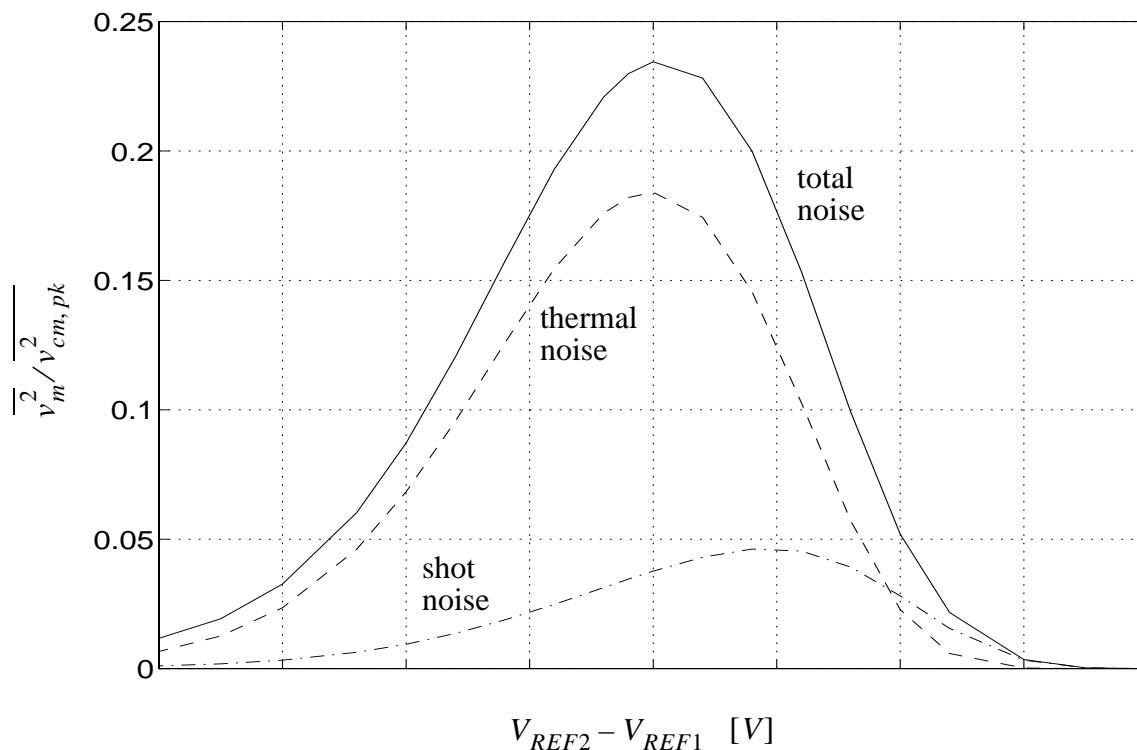


Figure 4.9: Noise components as function of tuning for a BJT within the multiplier.

Case B: $V_{C2} \gg V_{C1}$ or $V_{C1} \gg V_{C2}$. As can be observed from Figure 4.9, noise due to a BJT within the multiplier is quite low; however, the current split between each of these BJTs is significant (i.e. Q_1 and Q_3 are off). Thus, noise due to the current mirrors ($Q_5 - Q_{10}$) does not cancel at the differential output. It can be shown that the peak transconductor differential output noise power density, $\overline{v_{cm, pk}^2}$, due to a single BJT, $Q_5 - Q_{10}$, within the current mirrors is

$$\overline{v_{cm, pk}^2} = 4kTg_{m, BJT}^2 \left(r_b + \frac{1}{2g_{m, BJT}} \right) R^2 \quad [V_{rms}^2/Hz] \quad (4.27)$$

which is about four times $\overline{v_{m, pk}^2}$ as these devices have twice the gain. The simulated noise power densities due to these devices and normalized to $1/\overline{v_{cm, pk}^2}$ are shown in Figure 4.10.

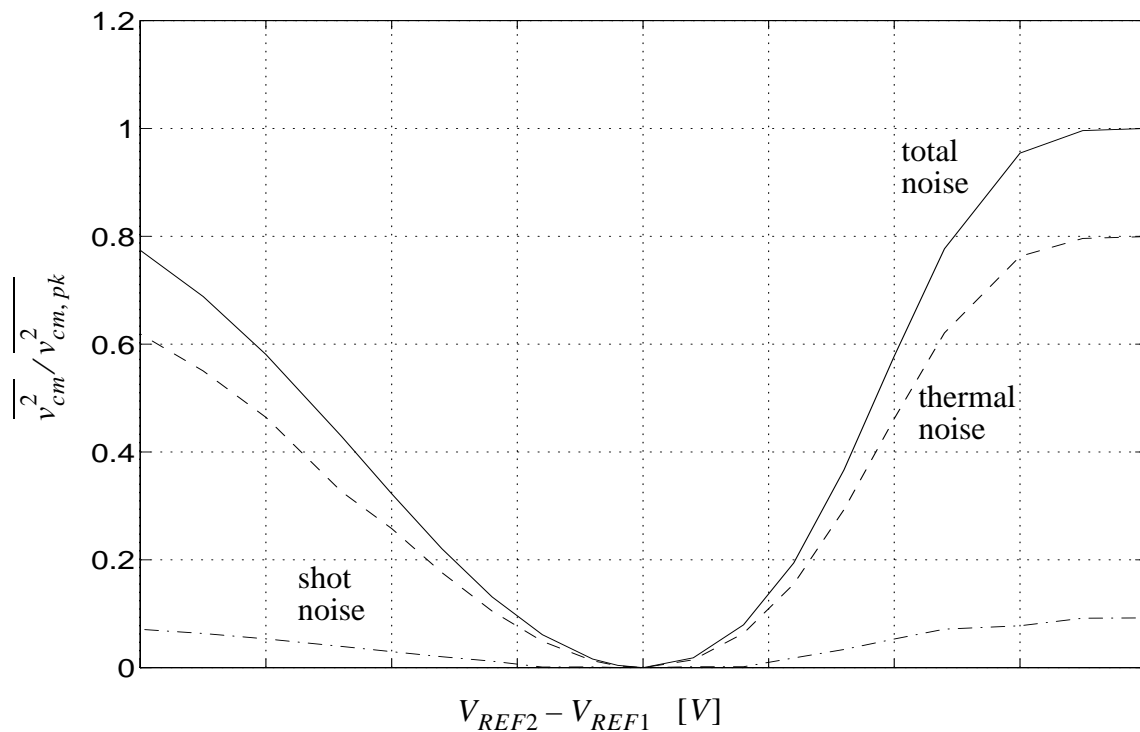


Figure 4.10: Noise components as function of tuning for a BJT within the mirrors.

The total transconductor differential output noise power density will be dominated by the four multiplier BJTs and the six current-mirror BJTs. The simulated result when normalized

to $1/v_{cm,pk}^2$ is shown in Figure 4.11. Observe that output noise power density is dominated by the BJTs $Q_5 - Q_{10}$, and that it varies by at most a factor of 6 or 7.8dB over the entire tuning range.

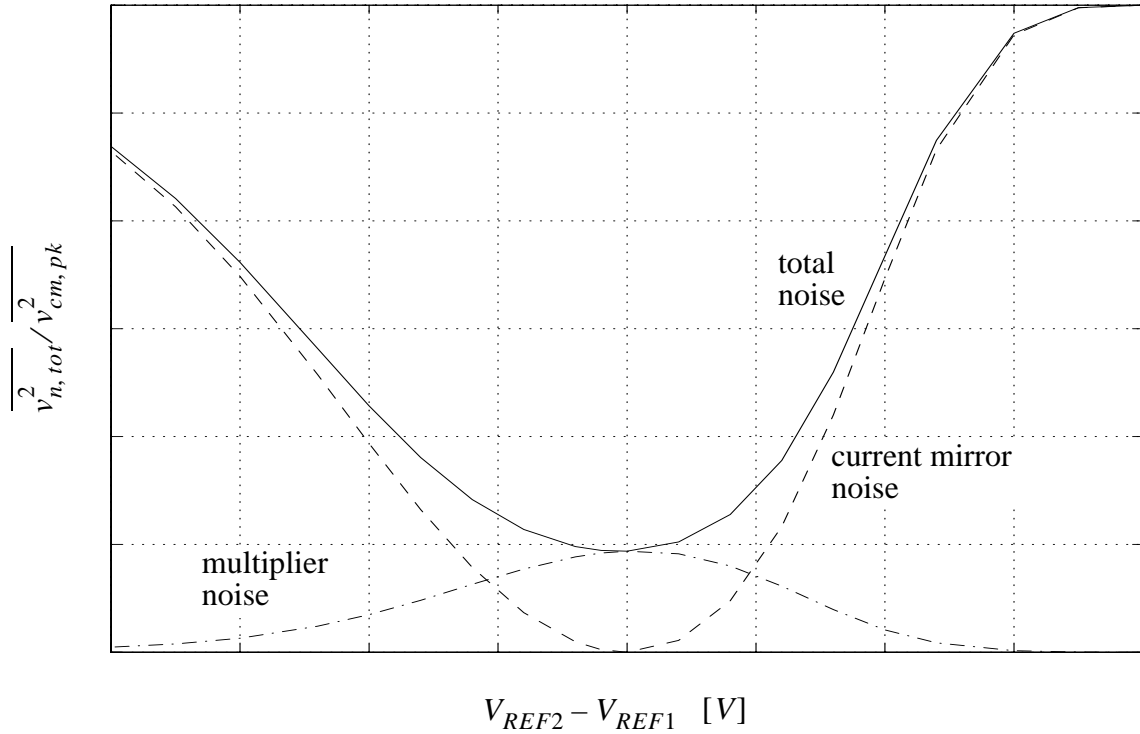


Figure 4.11: Normalized BJT output noise components as function of tuning.

To see why the bipolar devices dominate transconductor output noise, consider the MOS transistors $M_1 - M_4$. At the extremes of the tuning range, we obtain the following ratio of output noise

$$\frac{\overline{v_{n,BJT}^2}}{\overline{v_{n,MOS}^2}} = \frac{6}{4} \frac{4kTg_{m,BJT}^2 \left(r_b + \frac{1}{2g_{m,BJT}} \right) R^2}{\frac{8}{3}kTg_{m,MOS}R^2} \quad (4.28)$$

For our case, $r_b = 651\Omega$, $g_{m,MOS} = 200\mu A/V$, and $g_{m,BJT} = 8.6mA/V$ which results in a ratio of 590. In the real circuit, ohmic emitter resistance tends to provide degeneration reducing noise gain (as discussed in Section 4.3.3.1) for which the ratio becomes 244, or

24dB (verified also by simulation). This result implies that the SNR is 24dB worse than that caused by the MOSFETs alone as the bipolar transistors basically contribute noise and no signal gain (only signal attenuation). However, the MOSFETs process the signal and produce some noise. Although the CMFB circuit will generate additional noise, this noise was ignored in the analysis as its contribution is relatively small.

Finally, it should be apparent that for similar input levels the “2-quadrant” transconductor will display better SNR performance than the “4-quadrant” transconductor due to its higher signal gain. Also, note that as one tunes for lower G_m , signal power drops while noise power does not. Hence, SNR drops in contrast to the case of transconductors that are tuned by adjusting bias conditions for which both noise and signal drop as one tunes for lower G_m .

4.3.3.1 Noise Reduction Employing Emitter Degeneration

A common circuit technique to reduce BJT output noise is by employing emitter degeneration to reduce noise gain. To determine the amount of noise improvement by using emitter degeneration, some analysis and simulation studies were conducted. Consider a bipolar transistor with a single emitter degeneration resistance R . Then, the noise current appearing at the collector terminal can be shown to be

$$\overline{i_c^2} = 4kTg_m^2 \left[\frac{1}{1 + g_m R(1 + 1/\beta)} \right]^2 \left(r_b + \frac{1}{2g_m} + \left(\frac{(1 + 1/\beta)g_m R}{1 + (1 + 1/\beta)g_m R} \right)^2 R + \frac{g_m}{2\beta} R_{in}^2 \right) \quad (4.29)$$

where k is Boltzmann’s constant, T is the temperature in Kelvin and

$$R_{in} = r_b \parallel [(\beta + 1)(R + 1/g_m)] \quad (4.30)$$

The expression in (4.29) includes base resistance thermal noise, collector terminal shot noise, degeneration resistance thermal noise, and base terminal shot noise as indicated in the right-most parenthesis, respectively. For our case, $g_m = 0.0085A/V$, $r_b = 651\Omega$, $\beta = 76$, and $R = \overline{r_e}$ when no degeneration resistance is used. The parasitic emitter ohmic resistance, $\overline{r_e}$, is 30Ω . Using these values, we obtain a maximum collector noise current of

$$\overline{i_{c,max}^2} = 5.56 \times 10^{-22} \quad [A^2/H_z] \quad (4.31)$$

Letting $R = \bar{r}_e + r$, where r is the additional degeneration resistance, the noise reduction can be obtained and is illustrated in Figure 4.12 for various r and normalized to $1/\overline{i_{c,max}^2}$.

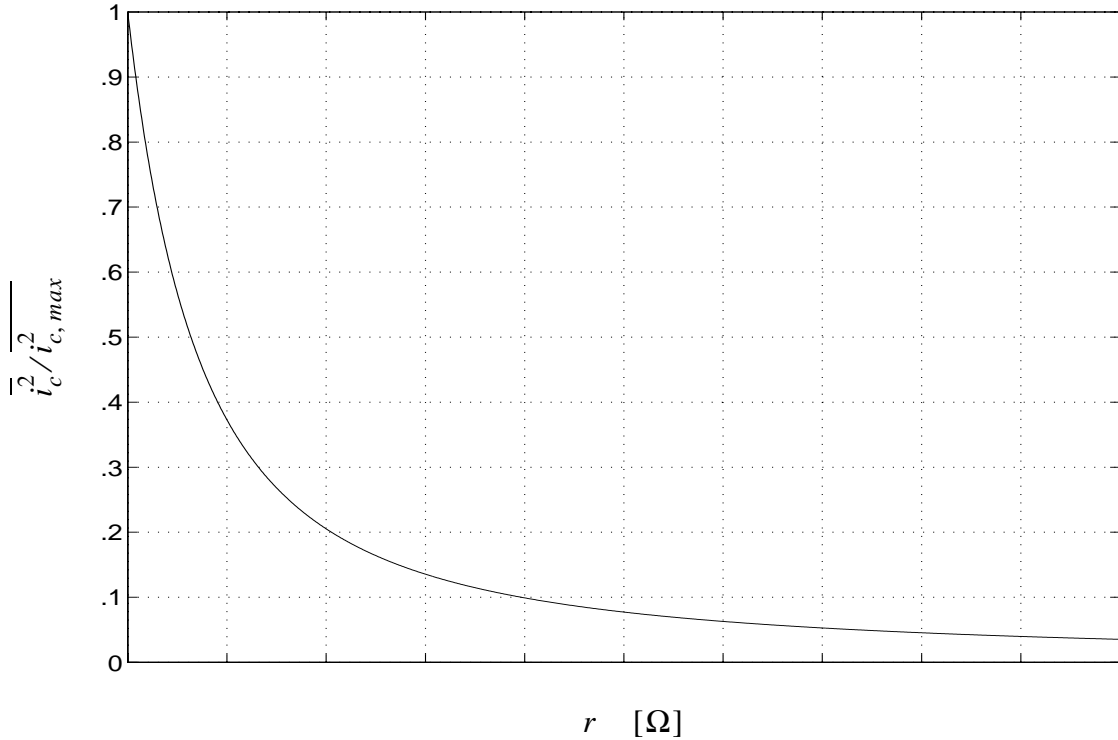


Figure 4.12: Normalized collector noise current for a BJT.

Observe that for resistor values above 500Ω , the additional reduction in noise current is relatively minimal. Choosing this value of resistance results in a reduction of the noise current by a factor of 13, as can be noted from the figure. This reduction was verified by simulating the transconductor (with emitter degenerating $Q_1 - Q_{10}$ and Q_{17}) tuned for maximum G_m for which noise is dominated by $Q_5 - Q_{10}$. At mid range, where noise is dominated by $Q_1 - Q_4$, using the result in (4.29) predicts a reduction in noise current by a factor of 6.7 in comparison with a simulated value of 9.1.

For the biquad filter using this degeneration technique, we simulated a reduction in noise power by a factor of 6.3 or 8dB. Together with double base contacts for all the BJTs, one can expect a reduction of 11dB. Hence, the expected improvement in SNR would be 11dB.

4.3.4 Frequency Response

Short-channel devices exhibit a high value for output conductance. Consequently, transconductor DC gain tends to be low — on the order of 10-20 in a submicron process [Nauta 92]. When loaded with a capacitor, the resultant integrator is therefore damped and far from ideal. A damped G_m - C integrator will cause filter poles and zeros to shift from their designed locations, thus, affecting filter response. Specifically, filter selectivity is limited by the natural Q of the integrators. To prevent sacrificing transconductor dynamic range and speed, rather than using cascode techniques to enhance DC gain, it is possible to load each transconductor with an adjustable transconductor that can realize a negative G_m to cancel the effects of finite output conductance as reported in [Nauta 92]. This approach was chosen for the prototype filter. However, since the G_m - C integrator is used to implement an adaptive filter, we prefer to correct for this effect within the filter network where its effect is most critical. For example, an adjustable feedforward term can be used to shift filter zeros, and a negative transconductance setting can be used to enhance loop Q .

Finite transconductor DC gain and parasitic poles and zeros will cause a G_m - C integrator to have a phase response that is not ideal [Peterson 87], [Snelgrove 92]. For the transconductor shown in Figure 4.4, summing the AC-signal from both input signal paths at the output results in an overall transconductance phase error that increases as the transconductor is tuned for lower transconductance (lower speed) because at low G_m settings, large signals are subtracted. This effect is illustrated graphically in Figure 4.13. Consider the signal path from M_3, M_4 to the output to be ideal in the sense that at the unity-gain frequency the phase shift is -90° . Let the M_1, M_2 signal path have a slight phase error as shown in Figure 4.13a. Summing signal

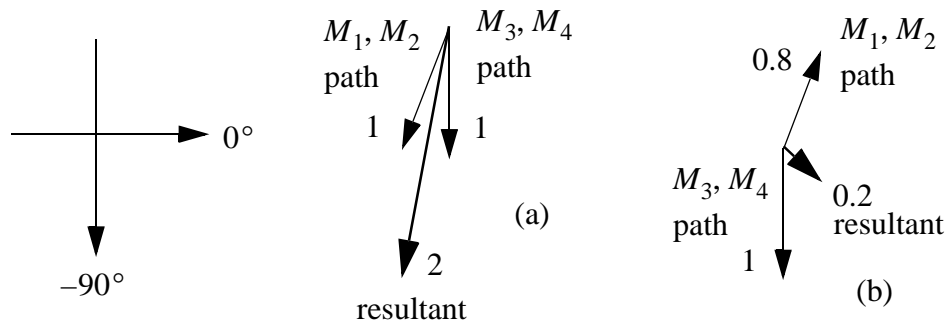


Figure 4.13: Illustrating magnitude and phase of output signal for two possible G_m settings: a) maximum G_m ; b) $0.2 G_{m, max}$

phasors at the output, for a setting giving a maximum value for G_m , results in the sum signal phasor to have roughly twice the magnitude component, as expected, but with a slight phase error. Now consider a low value for G_m . The result, depicted in Figure 4.13b, clearly shows that the resultant phasor has a large phase error. Therefore, it is expected that filters using this transconductor will display more distortion at lower frequencies. Naturally, higher distortion levels are also expected at higher frequencies where phase error due to parasitic poles will become more significant. For this reason, a filter should be designed such that its optimal response occurs when the transconductor in Figure 4.4 is set at $V_{C1} = V_{C2}$. The frequency responses of the unloaded F-cell transconductor for three tuning control settings are shown in Figure 4.14. Notice that the maximum speed is limited to about 600MHz due to the large collector-substrate capacitance of the Gilbert multiplier devices which is about 30fF per transistor. The effect of phase error is apparent and most notable at a low setting for G_m .

A final note at this point concerns conversion efficiency, defined as the ratio between the amount of linear output current to DC bias current. This ratio measures the attainable transconductor speed for a given power consumption and would best be optimized. In the transconductor of Figure 4.4, notice that the conversion efficiency would be halved if the second input stage were terminated as a simple active load. The second input stage, therefore, doubles the transconductor speed for the same bias current (power budget). The conversion

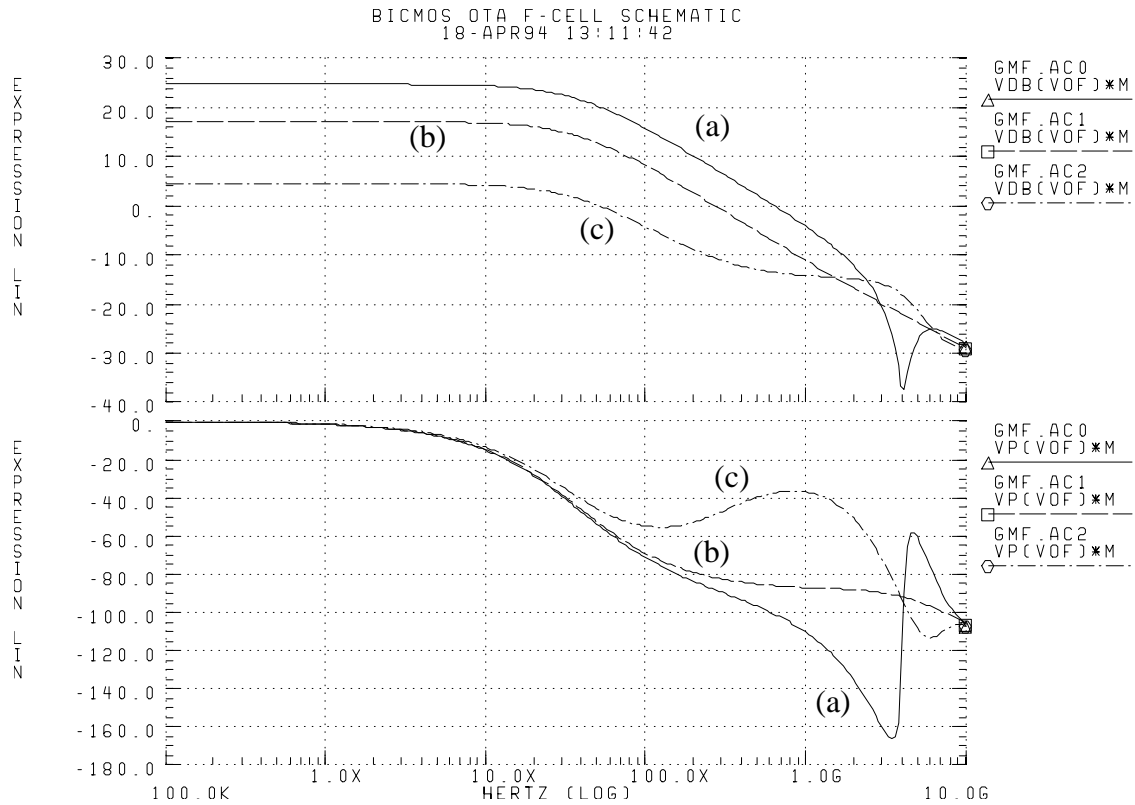


Figure 4.14: Unloaded F-cell transconductor frequency response for a setting of: (a) maximum G_m , (b) $0.5G_m$ and (c) $0.08G_m$.

efficiency of the transconductor in Figure 4.5 does not improve by having the input signal supply the second input stage.

4.3.5 Common-Mode Feedback

Choosing to eliminate the tail bias current sources for the input stages to enhance linearity implies that the common-mode gain increases. In fact, it can be easily shown that the common-mode gain of the transconductors in Figures 4.4 and 4.5 would be comparable to the differential gain when the transconductors' second input stages are terminated as load devices rather than input devices. Thus, this was the major reason for the second input stages; for matched input devices the transconductor common-mode signals cancel at the output for ideally zero common-mode gain. In a practical realization, the transconductor common-mode

gain would only appear as a mismatch error. Hence, a CMFB circuit to stabilize the output common-mode level is still required.

The common-mode feedback circuit, chosen for the prototype transconductor, is shown in Figure 4.4 and consists of the PMOS transistors M_5 - M_9 . Each pair of MOS devices M_5, M_6 and M_7, M_8 senses the transconductor output voltage to produce a common-mode current component that is referenced to that produced by M_9 . Since M_5 - M_8 are biased similar to the transconductor input transistors, M_1 - M_4 , and since transconductors run at equal input and output signal swings, the devices, M_5 - M_8 , should accommodate the entire transconductor output swing.

Unfortunately, the half-circuit outputs suffer from non-linearity that is manifested by a differential to common-mode conversion. This conversion error, when fed-back to the amplifier to vary the output common-mode voltage, will force asymmetry between the two transconductor half-circuit outputs. That is, each transconductor half-circuit output terminal, v_{o_i} , will consist of a desired differential signal, $\pm \frac{v_o}{2}$, a common-mode AC component, $v_{o, cm}$, and a common-mode DC bias, V_{CM} . For example, consider the model in (4.7) with $\theta(v_{GS} - V_t) \ll 1$, resulting in the ideal quadratic equation describing the MOSFET output current. Letting v_{o1} and v_{o2} represent the AC components of the transconductor output terminals, then for the transconductor in Figure 4.4 one obtains:

$$i_{D5} + i_{D6} = K[2(V_{DD} - V_{CM} - V_t)^2 - 2(V_{DD} - V_{CM} - V_t)(v_{o1} + v_{o2}) + (v_{o1}^2 + v_{o2}^2)] \quad (4.32)$$

The error term, Δi_{cm} , in the fed-back common-mode current consists of the AC terms:

$$\Delta i_{cm} = -K[2(V_{DD} - V_{CM} - V_t)(v_{o1} + v_{o2}) + (v_{o1}^2 + v_{o2}^2)] \quad (4.33)$$

Assuming the transconductor common-mode level has stabilized, then the error term given by (4.33) must be set to zero yielding

$$\frac{v_{o1}}{-v_{o2}} = \frac{1 + \frac{-v_{o2}}{2(V_{DD} - V_{CM} - V_t)}}{1 - \frac{v_{o1}}{2(V_{DD} - V_{CM} - V_t)}} \quad (4.34)$$

which ideally should be 1. It is evident from (4.34) that the CMFB circuit forces asymmetry due to a non-zero $v_{o,cm}$. Hence, distortion on each of the transconductor half-circuit outputs. The overall differential output

$$v_o = v_{o2} - v_{o1} \quad (4.35)$$

will be distortion free however, as the distortion is common to both outputs as depicted by the simulated transfer curves in Figure 4.15. Observe the effects of distortion on each half-circuit output voltage at higher input signal levels.

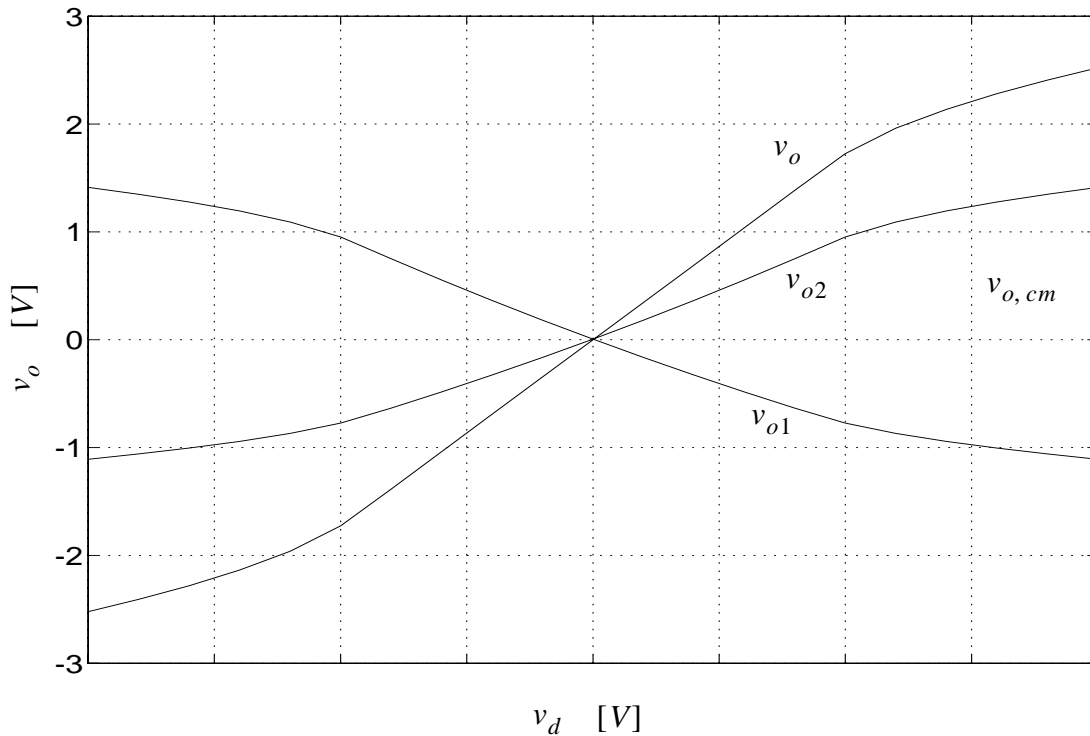


Figure 4.15: Illustrating transconductor output signal components.

At the other extreme of the model in (4.7) when $\theta(v_{GS} - V_t) \gg 1$, it can be shown that the distortion is no longer present. Granted short-channel devices are more linear, they are not ideally linear and a better common-mode feedback circuit would be preferable in a revision process.

4.3.6 Output Resistance

In Section 4.1.1, it was mentioned that transconductors which are tunable by changing bias currents exhibit an output resistance that is modulated by the tuning mechanism. To determine the output resistance of the transconductors in Figure 4.4 or 4.5, consider the BJT transistors Q_1 to Q_4 with output resistance $r_{oi} = V_A/i_{Ci}$. Assuming first that the output resistances of the current sources Q_7 - Q_{10} is infinite, one obtains using Kirchoff's current law at node v_s

$$\frac{v_{o1} - v_s}{r_{o1}} - g_{m1}v_s + \frac{v_{o2} - v_s}{r_{o4}} - g_{m4}v_s = 0 \quad (4.36)$$

Using Kirchoff's current law at node v_{o1} , one obtains

$$i_{o1} = \frac{v_{o1} - v_s}{r_{o1}} + \frac{v_{o1} + v_s}{r_{o2}} - g_{m1}v_s + g_{m2}v_s \quad (4.37)$$

for $v_{o1} = -v_{o2}$ the differential output resistance,

$$R'_{od} = \frac{v_{o2} - v_{o1}}{i_{o1}}, \quad (4.38)$$

looking down into the Gilbert cell is

$$R'_{od} = \frac{V_A}{I} (1 + \cosh[(V_{C1} - V_{C2})/V_T]) \quad (4.39)$$

If the output resistance of the current sources Q_7 - Q_{10} are taken into consideration, it can be shown that these have little effect on the result in (4.39) as they are in parallel with the

Gilbert multiplier BJT emitter resistances. A graphical illustration of this output resistance normalized to I/V_A over the useful tuning range is given in Figure 4.16.

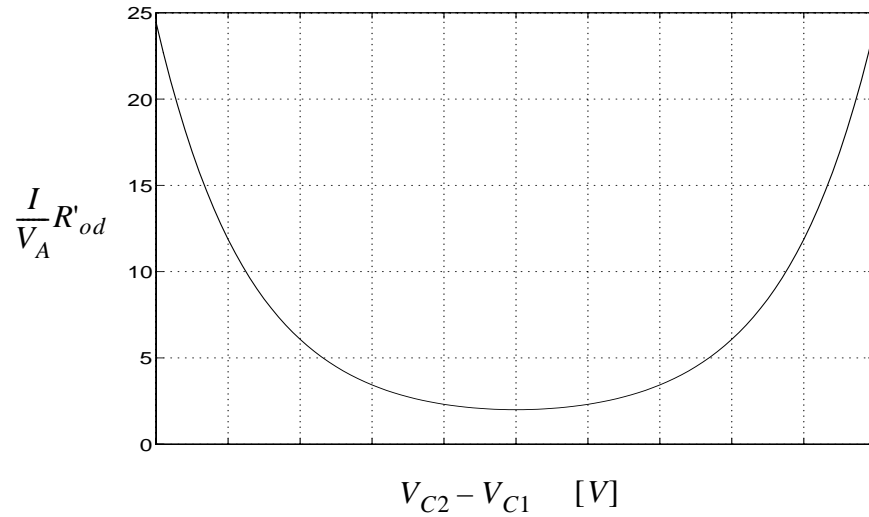


Figure 4.16: Theoretical normalized Gilbert cell output resistance.

The variation in R'_{od} as function of the tuning voltage is quite severe and can result in a local minimum when the element is used in an adaptive system. Fortunately, the transconductor differential output resistance, R_{od} , is the parallel combination of R'_{od} and the MOS differential output resistance which is much lower than R'_{od} . Thus, the effect is reduced as evident from the simulated plot in Figure 4.17 for the transconductor output resistance over the entire tuning range. At low settings for filter Q (low transconductor DC gain suffices), the effect is acceptable. However, this effect will be more severe as one connects a self-connected transconductor in parallel and tunes for negative transconductance to enhance filter Q (higher transconductor DC gain). Therefore, some modification of the basic transconductor cell is required in a revised circuit to ensure R'_{od} is dominated, such as by cascoding the Gilbert cell.

4.4 Biquadratic Filter

To determine the feasibility of analog adaptive filters for practical applications, a fully tunable biquad was implemented using the transconductors of Figures 4.4 and 4.5. This filter

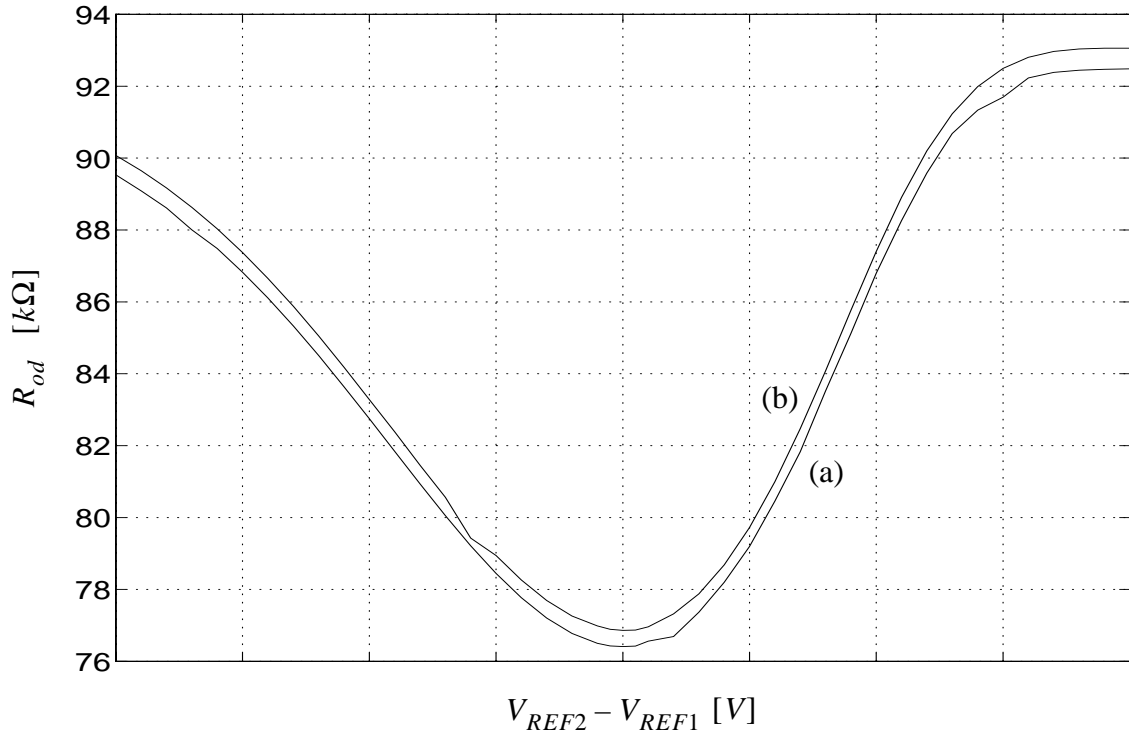


Figure 4.17: Transconductor output resistance vs. tuning control: a) F-cell, b) Q-cell.

is shown in Figure 4.18 The load capacitance $2C$ includes: 80fF poly-poly capacitors, 104.2fF MOS gate and drain-source capacitance, 56.5fF wire capacitance, and 175.8fF BJT collector-substrate capacitance for a total of 417fF. The state-space representation for this biquad, in accordance with Section 2.3.1, is .

$$\mathbf{A} = \frac{1}{C} \begin{bmatrix} -(g_{o12} + g_{ob}) & G_{m12} \\ -G_{m21} & -(G_{m22} + g_{o22} + g_{oi} + g_{o21}) \end{bmatrix}, \quad \mathbf{b} = \frac{1}{C} \begin{bmatrix} G_{mb} \\ G_{mi} \end{bmatrix} \quad (4.40)$$

$$\mathbf{c}_{BP} = [0 \ 1], \quad \mathbf{c}_{LP} = [1 \ 0], \quad d = 0 \quad (4.41)$$

where G_m represents the transconductor transconductance parameter and g_o represents the respective transconductor's output conductance. The \mathbf{c}_{BP} vector selects the filter bandpass function while the \mathbf{c}_{LP} selects the filter lowpass function. It can be easily shown that the transfer-functions corresponding to \mathbf{c}_{BP} and \mathbf{c}_{LP} , respectively are

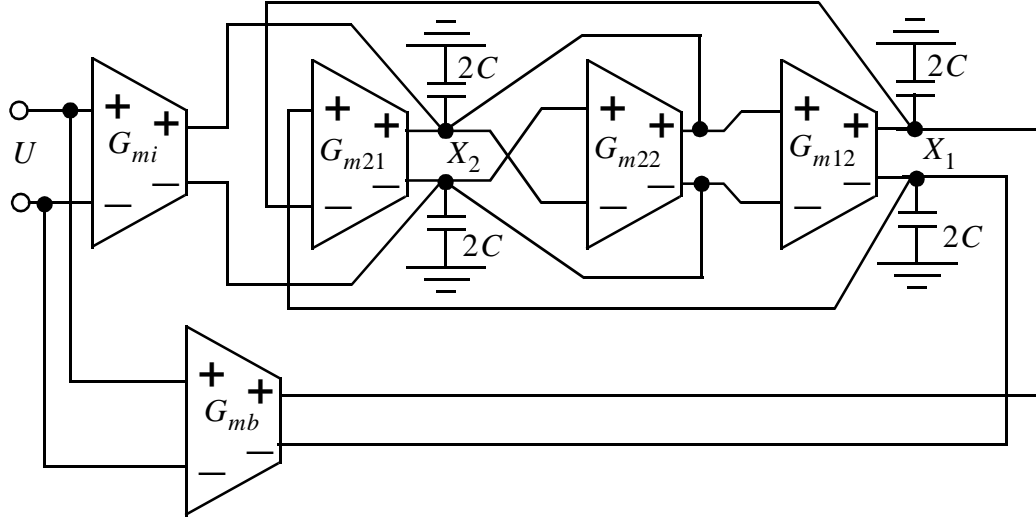


Figure 4.18: The biquad filter.

$$\frac{X_2}{U} = \frac{\frac{G_{mi}}{C}s + \frac{G_{mi}}{C^2}(g_{o12} + g_{ob}) - \frac{1}{C^2}G_{m21}G_{mb}}{s^2 + \frac{1}{C}(G_{m22} + g_{o22} + g_{oi} + g_{ob} + g_{o12} + g_{o21})s + \left[\frac{(g_{o22} + g_{oi} + g_{o21} + G_{m22})(g_{o12} + g_{ob}) + G_{m12}G_{m21}}{C^2} \right]} \quad (4.42)$$

$$\frac{X_1}{U} = \frac{\frac{G_{mb}}{C}s + \frac{G_{mi}G_{m12}}{C^2} + \frac{(g_{o22} + g_{oi} + g_{o21} + G_{m22})G_{mb}}{C^2}}{s^2 + \frac{1}{C}(G_{m22} + g_{o22} + g_{oi} + g_{ob} + g_{o12} + g_{o21})s + \left[\frac{(g_{o22} + g_{oi} + g_{o21} + G_{m22})(g_{o12} + g_{ob}) + G_{m12}G_{m21}}{C^2} \right]} \quad (4.43)$$

The filter f_o and Q are

$$f_o = \frac{1}{2\pi} \sqrt{\frac{(g_{o22} + g_{oi} + g_{o21} + G_{m22})(g_{o12} + g_{ob}) + G_{m12}G_{m21}}{C^2}} \quad (4.44)$$

$$Q = \frac{\sqrt{(g_{o22} + g_{oi} + g_{o21} + G_{m22})(g_{o12} + g_{ob}) + G_{m12}G_{m21}}}{G_{m22} + g_{o22} + g_{oi} + g_{ob} + g_{o12} + g_{o21}} \quad (4.45)$$

Observe from (4.42-4.45) that finite transconductor output conductances lead to both pole and zero frequency shifts and limit attainable filter Q . Since the filter is fully tunable, it is possible to mitigate this problem through tuning. For example, the transconductors G_{mi} , G_{m12} , and G_{m21} were realized using the topology in Figure 4.4 and are used to tune filter

gain coefficient via G_{mi} and the filter pole-frequency via either G_{m12} , G_{m21} or both. For these functions “2-quadrant” operation suffices. The transconductor G_{m22} was realized using the transconductor of Figure 4.5 so that it can be tuned to enhance filter Q by tuning for negative transconductance to cancel the denominator g_o terms of (4.45). Hence, “4-quadrant” operation was required to achieve a wide range of damping levels. The transconductor G_{mb} can be used to shift a mistuned bandpass transfer-function zero, $s_z = -(g_{o12} + g_{ob} - G_{m21}G_{mb})/C$, back to the origin. This transconductor (B-cell) is a scaled version of the transconductor in Figure 4.4. Specifically, all the MOSFETs have aspect ratios of $2.5\mu\text{m}/0.8\mu\text{m}$ with the exception of M_5 - M_8 which have an aspect ratio of $2\mu\text{m}/0.8\mu\text{m}$. The aspect ratio of M_9 is $4\mu\text{m}/0.8\mu\text{m}$.

Experimentation with this biquad in a practical application gives an understanding of the various issues to be considered in a higher-order filter. The experimental results and findings are given in Chapter 5.

4.4.1 Probes

Observe from Figure 4.18 that the filter output signals X_1 and X_2 are all at high impedance nodes. At the high frequency extreme, it becomes difficult to probe these nodes without affecting the circuit. Thus, 50Ω analog drivers were implemented. These probes consisted of $8\mu\text{m}/0.8\mu\text{m}$, common-source, open-drain, NMOS transistors biased at 1mA to drive external 50Ω resistors for analog probing as shown in Figure 4.19. Bipolar emitter followers could have been used, but a Darlington pair would be required to ensure high input impedance. Thus, for simplicity, the high impedance FET was preferred for testing purposes.

4.5 Comparators

Since the aim here is to investigate the practicality of analog adaptive filters, it was decided to configure the biquad as an adaptive pulse-shaping filter. In accordance with the

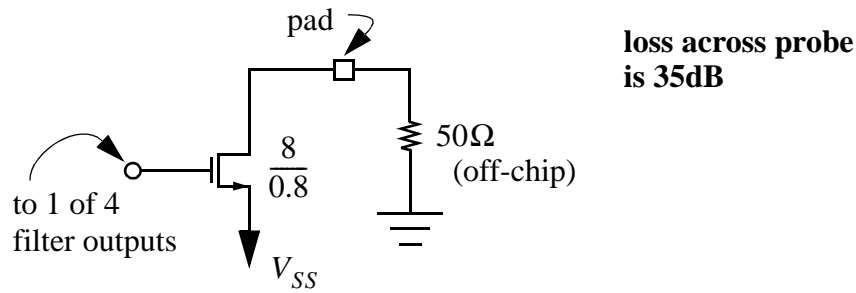


Figure 4.19: Schematic of the on-chip probe device and the off-chip load.

theoretical treatment in Section 3.2, two comparators, two U/D counters, two DACs, and various other digital circuitry are required. Note that the critical circuits in the system are the filter and the comparators. Hence, these circuits were integrated on a single die. The digital circuitry including the counters and the logic were implemented externally in labVIEW [labVIEW 93]. The DACs were external as well. The comparators used, shown in Figure 4.20, are those presented in [Bereza 94]. All bipolar transistors are NN52111X [BATMOS 92] except for the final emitter followers which are NN52114X. More detail on the comparator and biasing can be obtained from [Long 92].

4.6 Filter-to-Comparator Interface Buffers

Observe that the comparators consist of bipolar input devices which would significantly load the high-impedance filter output nodes. To prevent this effect, the most straight-forward approach would be to replace the input bipolar differential pairs by MOSFETs. However, in order not to sacrifice comparator speed, these MOSFETs would require a large aspect ratio to match the transconductance of the bipolar input devices. This large aspect ratio would manifest a large input gate capacitance and load the filter output nodes. For this reason, a fast, high-input impedance, low input-capacitance buffer was preferred. In addition, such a buffer shields the filter outputs from the comparators, thus, reducing the effects of glitches on the output analog signals due to comparator clocking. The buffer designed is shown in Figure

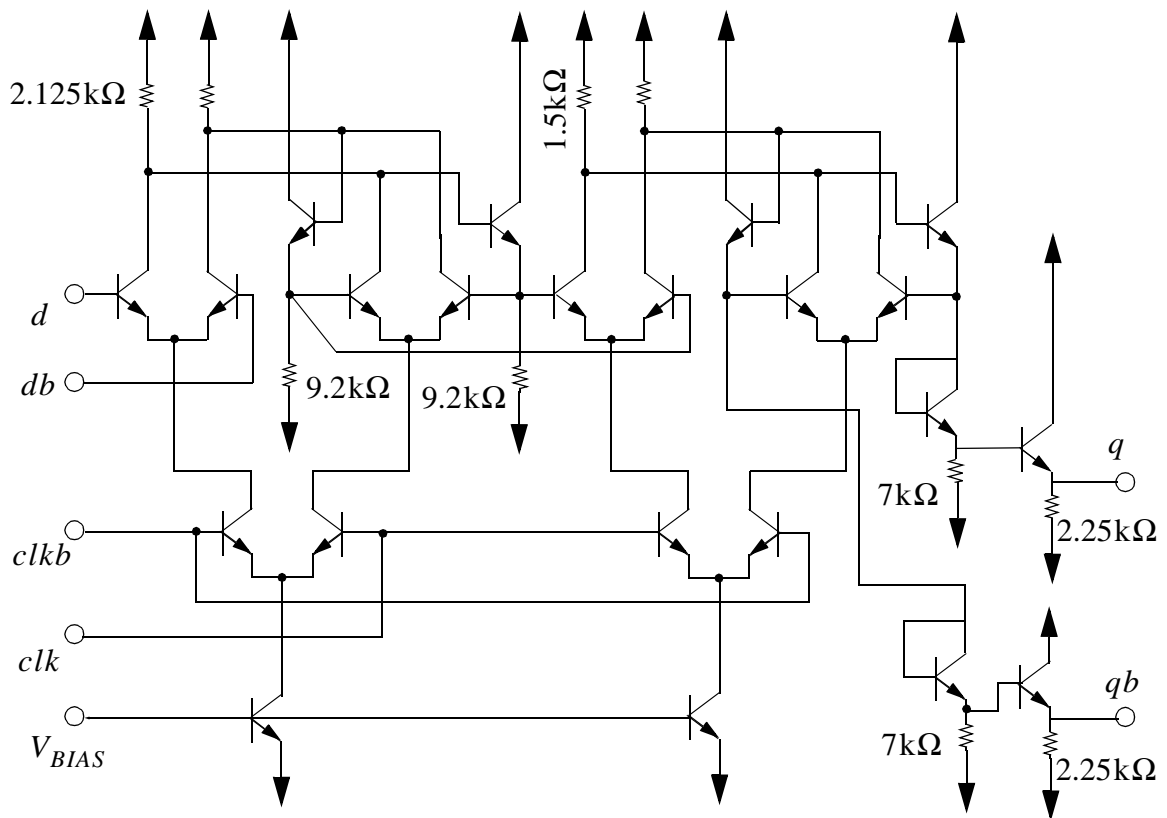


Figure 4.20: Partial circuit schematic for the clocked comparator.

4.21. Observe that this buffer is a potential source of mismatch due to the small MOSFETs and the resistors. These mismatches may lead to differential offset between the two complementary filter output signals leading to the comparator. Although MOSFET mismatches would dominate here, to minimize resistor mismatches the $7\text{k}\Omega$ resistors were made to have a large aspect ratio ($20\mu\text{m} \times 97\mu\text{m}$). The $3.5\text{k}\Omega$ resistors were two $7\text{k}\Omega$ resistors connected in parallel.

4.7 50Ω Digital Pad Drivers

To drive the comparator output (ECL levels) off-chip, a large current drive output buffer would be required. To achieve this requirement, a 50Ω digital pad driver supplied by BNR was used. This pad drive consists of a bipolar differential-pair, a bias circuit, and a

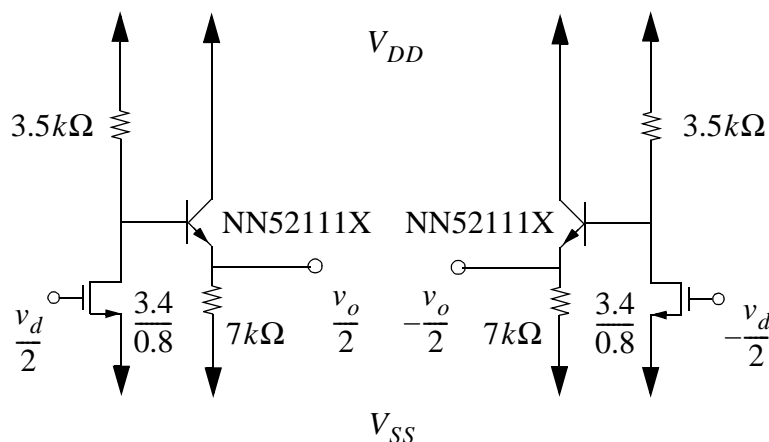


Figure 4.21: Schematic of the filter-to-comparator interface buffer.

high-current drive bipolar (NN564330) emitter-follower. It has a maximum bandwidth of 500MHz when driving a 50Ω load.

4.8 System Chip

The complete system chip, which measures 1.7mm x 1.1mm, is shown in Figure 4.22. As evident, it consists of the two pad drivers (top left corner), the biquad filter (the distinctive 5 transconductors in the bottom right-center), two comparators (below and on either side of the biquad filter), and the two filter-to-comparator interface buffers (note the large resistors). Also on chip, two transconductor test structures are visible to the left of the biquad.

4.9 Summary

In this chapter, issues pertaining to the design of transconductors including tuning range and linearity were discussed and it was explained why the many transconductors presented in the technical literature feature a tuning range below one decade. Also, the transconductor circuits we implemented to achieve a wide tuning range while maintaining satisfactory speed performance were presented. Comments were made about the performance of these circuits.

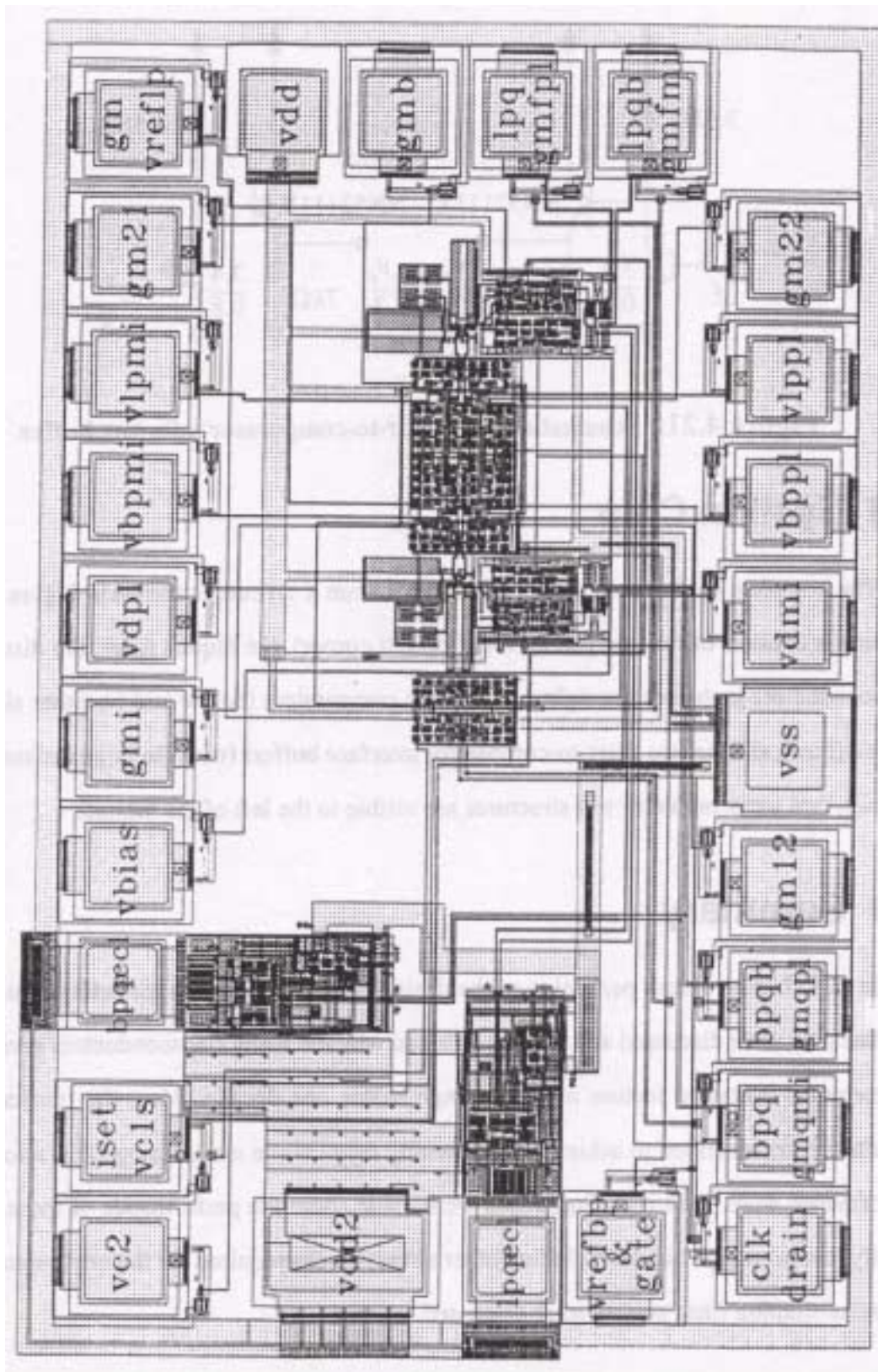


Figure 4.22: System chip layout plan.

Finally, the prototype biquad including other circuit blocks required for the implementation of the pulse-shaping filter system were discussed.

CHAPTER 5

Experimental Verification

In this chapter, experimental results for the circuits described in Chapter 4 are provided. These results include performance measurements of the transconductors, the biquad, and the adaptive pulse shaping filter. However, before presentation of these results, it is imperative that some background theory on the performance characteristics be reviewed.

5.1 Measurement Characteristics: Background

In this section, the necessary fundamental theory for various test procedures is addressed.

5.1.1 Harmonic and Intermodulation Distortion

One of the mechanisms which limits filter dynamic range is distortion. Distortion results from the deviation of a given linear system from the ideal behavior. This deviation is manifested by the production of harmonic terms of the input signal at the system output. Consider the system depicted in Figure 5.1 where the input is $v_{in}(t)$, the output is $v_o(t)$, and



Figure 5.1: A single-input single-output system.

the system is time-invariant but not necessarily linear. Although the output of such a system is best expressed in terms of a Volterra series [Schetzen 89], we make use of a Taylor series expansion about the operating point to simplify the analysis to obtain quantitative approximations for distortion figures¹. It should be mentioned that the Taylor series is a special case of the Volterra series in that all higher-order kernels are unit impulse functions. Hence, we assume the system output is memoryless and can be expressed as

$$v_o(t) = a_1 v_{in}(t) + a_2 v_{in}^2(t) + a_3 v_{in}^3(t) + a_4 v_{in}^4(t) + a_5 v_{in}^5(t) + \dots \quad (5.1)$$

where a_1 is the incremental first-order coefficient term and the higher-order coefficients, a_i , characterize non-linear distortion. For a fully differential system, all even scalar terms are ideally zero, while in a practical system these terms would be small. As a result, in fully differential systems, the cubic term typically dominates all other harmonic terms.

For a sinusoidal input of peak amplitude V_{pk} , it can be shown that

$$v_o(t) \approx a_1 V_{pk} \cos[\omega t] + \frac{a_3}{4} V_{pk}^3 (3 \cos[\omega t] + \cos[3\omega t]) \quad (5.2)$$

Since typically for low distortion $\frac{3a_3}{4} V_{pk}^3 \ll a_1 V_{pk}$, it is customary to approximate the linear (or first harmonic) component of the output signal as

$$\overline{HD}_1 \approx a_1 V_{pk} \quad (5.3)$$

and the 3rd harmonic component as

$$\overline{HD}_3 = \frac{a_3}{4} V_{pk}^3 \quad (5.4)$$

The 3rd harmonic distortion is the ratio of these two components, and thus, using (5.3) and (5.4), we have

1. The Taylor series approximation is valid for wideband amplifiers which are memoryless, however, strictly speaking, it is not applicable to filters as they are typically not memoryless. Hence, the analysis performed here is only approximate in describing filter distortion performance.

$$HD_3 \approx \frac{a_3}{4a_1} V_{pk}^2 \quad (5.5)$$

While HD_3 is a useful performance parameter for wideband amplifiers, it is generally not used to characterize narrowband filters. The reason is that this measurement does not describe the distortion level in the filter passband, and also, this distortion component is severely attenuated as it appears in the filter stopband.

As a result, to determine filter distortion performance for narrowband filters, the two tone inband intermodulation (IM) distortion test is adopted. Once again, for a fully differential system, the third-order intermodulation products are of prime concern. Third-order intermodulation results when two tones are present at the input of the filter and the 2nd harmonic of one tone mixes with the fundamental of the other tone. Defining the frequency separation between the two input tones, f_1 and f_2 , to be Δf , where f_1 is the lower frequency tone, intermodulation results in output tones \overline{IM}_{3L} and \overline{IM}_{3H} just below the lower input tone ($2f_1 - f_2 = f_1 - \Delta f$) and just above the upper input tone ($2f_2 - f_1 = f_2 + \Delta f$), respectively. To appreciate this result, consider once again the system in Figure 5.1. For two input tones of equal amplitude V_{pk} , the output can be approximated as

$$\begin{aligned} v_o(t) \approx & \left(a_1 V_{pk} + \frac{9a_3}{4} V_{pk}^3 \right) (\cos[\omega_1 t] + \cos[\omega_2 t]) + \frac{a_3}{4} V_{pk}^3 (\cos[3\omega_1 t] + \cos[3\omega_2 t]) \\ & + \frac{3a_3}{4} V_{pk}^3 (\cos[(2\omega_1 + \omega_2)t] + \cos[(2\omega_2 + \omega_1)t]) \\ & + \frac{3a_3}{4} V_{pk}^3 (\cos[(\omega_1 - \Delta\omega)t] + \cos[(\omega_2 + \Delta\omega)t]) \end{aligned}$$

Observe that the IM distortion component levels are

$$\overline{IM}_{3L} = \overline{IM}_{3H} = \frac{3a_3}{4} V_{pk}^3 \quad (5.6)$$

while third-order intermodulation distortion, assuming the distortion levels are low and that the filter response is fairly flat in the band occupied by the output fundamental and IM distortion tones, is

$$IM_3 \approx \frac{3a_3}{4a_1} V_{pk}^2 \quad (5.7)$$

Observe that (5.5) and (5.7) are easily related and one measure can be obtained from the other; as long as one accounts for the filter response. Also, observe that the intermodulation distortion result is more tight.

Notice also that the level of the distortion products depends on the input levels. Specifically, for every 1dB increase in the input levels, IM_{in} , the \overline{IM}_3 products increase by 3dB resulting in a proportionality ratio of 3:1 on a logarithmic scale for the generated \overline{IM}_3 distortions and the input tones. Thus, it is apparent that if the power level of the output fundamental tones, IM_{out} , are plotted along with their associated \overline{IM}_3 products on a logarithmic scale, these two curves would intersect at some level. This intersection point is referred to as the third-order intercept point, denoted as IP_3 [Carson 90]. Note that this point is actually a fictitious point as the output level of the filter would compress before reaching the intercept point. However, when operating in the linear region of the filter, this point is useful in determining the level of \overline{IM}_3 products for a given level of the input generating tones. It is also a useful benchmark when specifying the linearity of the filter. Specifically, when the units are in dB then:

$$\overline{IM}_3 = IP_3 - 3(IP_3 - IM_{out}) \quad (5.8)$$

As well, defining the signal-to-distortion ratio (SDR) to be the difference between the power of the two inter-modulating tones to their third-order distortion products, or mathematically,

$$SDR = IM_{out} - \overline{IM}_3 \quad (5.9)$$

one can show the following simple relationship (in dB)

$$IM_{out} = IP_3 - \frac{SDR}{2}. \quad (5.10)$$

The above formula indicates that if the third-order intercept point, IP_3 , is known and a signal-to-distortion ratio, SDR , is desired, the necessary output level, IM_{out} , can be quickly calculated. For example, if 1% ($SDR = 40\text{dB}$) IM distortion is desired, the output signal level should be 20dB below the IP_3 value.

5.1.2 Filter Compression

For any two port system, the output power level is ideally expected to follow the input power level. The proportionality constant represents the gain or loss of the system. However, no system is ideally linear, and thus, the proportionality constant is not maintained at high input power levels. Instead, system elements (amplifiers) begin to compress. For example, from (5.2) note that the overall first-order term, is

$$a_1 V_{pk} + \frac{3a_3}{4} V_{pk}^3 \quad (5.11)$$

The resulting effect of the third-order power series term in (5.11) on the amplitude of the fundamental represents the gain compression which can be put in the form

$$a'_1 = \left(1 + \frac{3a_3}{4a_1} V_{pk}^2\right) a_1 V_{pk} \quad (5.12)$$

$$= (1 + 3HD_3) a_1 V_{pk} \quad (5.13)$$

$$= (1 + IM_3) a_1 V_{pk} \quad (5.14)$$

An important measure of this behavior is termed the 1dB compression point, denoted as CP_1 . This point is simply the power level of a signal that overloads an amplifier such that its gain (a'_1 relative to a_1) is reduced by 1dB [Carson 90]. Based on (5.8) and (5.14), it can be shown that at the output CP_1 , the IM distortion is 10.9%, or alternatively, when the units are in dB then the output

$$CP_1 \approx IP_3 - 9.64 \quad (5.15)$$

Therefore, for wideband amplifiers the IM distortion can also be predicted from the measurement of output CP_1 . For example, for 1% IM distortion, the output signal level would have to be reduced below the CP_1 by 10dB.

5.1.3 Noise

The second mechanism which limits filter dynamic range is noise. In an integrated circuit there are various sources which produce noise. A fundamental lower limit on output noise can be obtained by estimating kT/C . For the biquad filter herein, the differential capacitance C was $209fF$. This capacitance results in an output noise voltage of $0.14mV_{rms}$.

The noise produced in an integrated circuit typically exceeds the fundamental limit above due to other sources of noise. Output noise power is evaluated as follows

$$\bar{e}_n^2 = \sum_{i=1}^N \int_0^{\infty} \overline{v_{ni}^2}(f) |T(f)|^2 df \quad (5.16)$$

where N represents the total number of noise sources, $T(f)$ the circuit transfer-function, and $\overline{v_{ni}^2}(f)$ is the i^{th} noise source's input-referred power spectral density.

Consider a system where the transfer-function can be defined by (3.5), repeated here for convenience.

$$T_{BP}(s) = \frac{K\omega_o s}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \quad (5.17)$$

Assume a single noise source and let the input-referred noise power density be a constant value of $1V_{rms}^2/Hz$. Then, using (5.16) and (5.17), the system output noise power is

$$\bar{e}_n^2 = \int_0^{\infty} \frac{K^2 f^2 f_o^2}{(f_o^2 - f^2)^2 + \left(\frac{ff_o}{Q}\right)^2} df \quad (5.18)$$

$$= \frac{\pi}{2} K^2 f_o Q \quad (5.19)$$

Observe that noise power is proportional to both filter pole-frequency and quality factor while for constant f_o , noise power is proportional to Q . Moreover, the integration in (5.18) is generally difficult to evaluate during experimentation, and thus, an effective “noise bandwidth”, BW_{eff} , is used to predict output noise power from the noise voltage density at some frequency. Consider once again the example above. At $f = f_o$, the bandpass output noise voltage density, $\bar{e}_n(f_o)$, is QV_{rms}/\sqrt{Hz} . Thus, using (5.19), it is reasonable to approximate

$$K^2 Q^2 BW_{eff} = \frac{\pi}{2} K^2 f_o Q \quad (5.20)$$

The result in (5.20) yields

$$BW_{eff} = \frac{\pi f_o}{2Q} = \frac{\pi}{2} BW \quad (5.21)$$

where BW is the bandpass output 3dB bandwidth. Using this result, the spectrum analyzer’s noise voltage density at f_o was recorded and a value for output noise voltage was experimentally obtained based on the result of (5.21).

5.1.4 Spurious Free Dynamic Range and Peak Dynamic Range

Spurious free dynamic range (*SFDR*) is defined as the ratio between the minimum discernible signal level (*MDS*) of a device and the level of the two input tones that generate intermodulation products, IM_{out} , at the same *MDS* level. For filters, the *MDS* is normally taken as the noise power. Thus, *SFDR* is essentially the filter SNR when the distortion level equals the noise power. This figure measures the filter maximum dynamic range (*SNR* in the absence of distortion) that can be achieved beyond which distortion begins to degrade dynamic range. When dealing with units of dB, eliminating the IM_{out} in (5.8) and solving for the *SFDR*, we obtain

$$SFDR = \frac{2}{3}(IP_3 - MDS) . \quad (5.22)$$

Peak dynamic range is defined as the ratio between the input signal level and the distortion combined with noise levels when both distortion and noise are at the same level. In this case, both the *SNR* and the signal to distortion ratio *SDR* are equivalent giving a peak dynamic range *PDR* where:

$$PDR = \frac{S}{N + D} \quad (5.23)$$

It can be noted that *PDR* is simply *SFDR* minus 3dB.

5.1.5 Common-Mode Rejection Ratio

When implementing differential circuits, one must keep in mind the conversion gains between differential to common-mode signals and common-mode to differential signals as discussed in [Snelgrove 92] and [VanPeteghem 90]. Of the two undesirable terms, the common-mode to differential conversion gain, $\frac{V_{od}}{V_{icm}}$, dominates in the tested circuits since we have used very small devices, and thus, mismatches are large. The common-mode rejection ratio (CMRR) measures the relative ratio between the differential gain and the undesirable conversion gain above.

5.1.6 Power-Supply Rejection Ratio

The power supply rejection ratio (PSRR) is obtained by grounding filter inputs and supplying the AC signal to either supply rail. The ratio between the resultant signal level at the filter output to the signal level at the supply input represents the filter response to power supply noise. The PSRR measures the relative ratio between the filter differential gain (the useful component) and the power supply gain (unwanted component). Higher PSRR implies better immunity to power supply disturbances.

5.2 System Chip Test Results

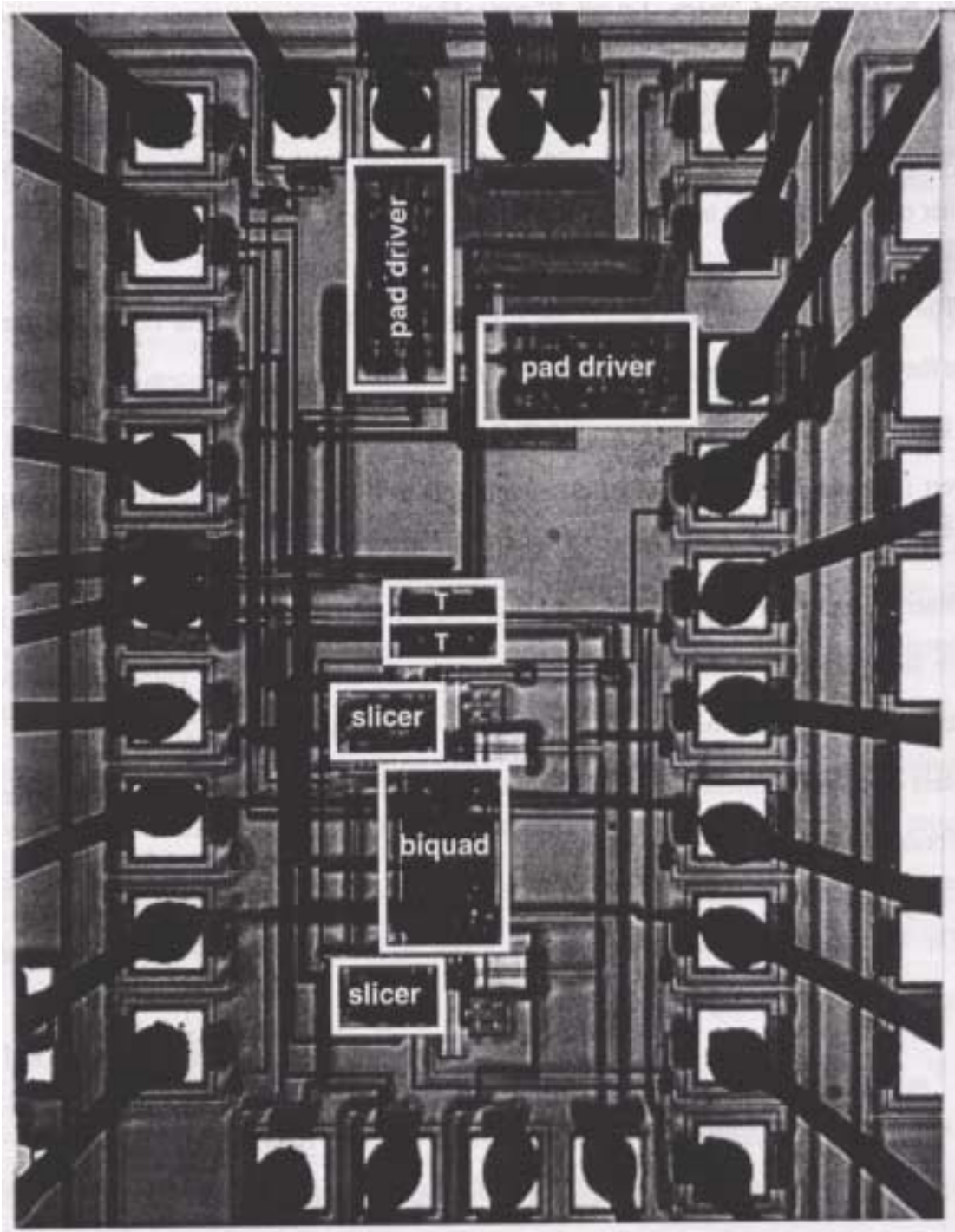
In this section, the experimental results of the system chip, whose photomicrograph is shown in Figure 5.2, are presented. Specific tests of the transconductors were done using another chip as described in Appendix 5.1.

The integrated circuit (IC) area of the entire system including pads is 1.7mm x 1.1mm, while the IC area of the biquad filter alone is 0.360mm x 0.164mm. The system chip was tested in a high-speed package with controlled 50 Ω impedance lines for the AC signal lines. To convert from single-ended signals (test equipment) to differential signals (filter topology) 50 Ω , 180 $^\circ$ power splitters were used. Similarly, the splitters were configured as power combiners at the filter outputs. The test setup and the measured splitter characteristics are shown in Figure 5.3. It also defines the naming convention we adopt herein. The power splitters are transformer based, and hence, have a limited frequency range of 1MHz to 500MHz. Thus, experimental data outside this range will be affected by the roll-off of these transformers.

The biquad filter transfer-functions as given by (4.42) and (4.43) are completely programmable by adjusting DC control voltages as follows:

- V_{mi} controls the transconductance G_{mi} which tunes the filter gain.
- V_{mb} controls the transconductance G_{mb} which tunes the filter zero-frequency.
- V_{m12} controls the transconductance G_{m12} which tunes the filter pole-frequency.
- V_{m22} controls the transconductance G_{m22} which tunes the filter Q .

The average current consumption from the positive supply (+2.5V) was 110mA and from the negative supply (-2.5V) it was 50mA. The remaining current was drawn from analog ground since the pad driver output connects to a 50 Ω load to ground. Therefore, the power



T = transconductor
slicer = comparator

Figure 5.2: System chip photomicrograph. For pad labels see Figure 4.22.

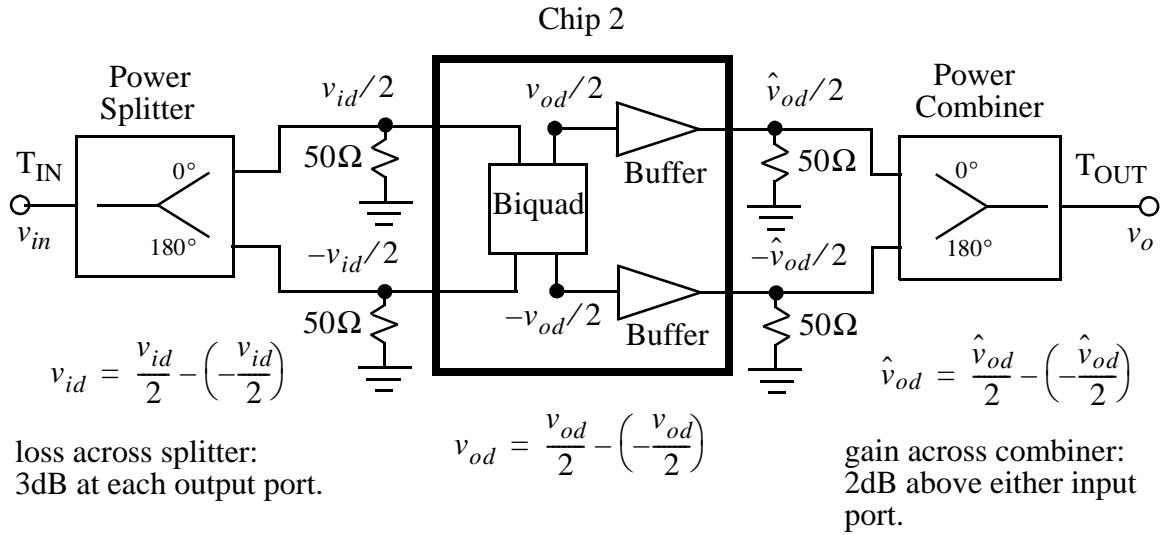


Figure 5.3: Illustrating the setup used to test the biquad filter.

dissipation of the entire system is 550mW (comparators turned off) which compares well with a simulated value of 530mW.

5.2.1 Biquad Pole Frequency and Quality Factor Tuning Range

To determine the minimum and maximum operating frequencies of the biquad, the control voltage V_{m12} for both G_{m12} and G_{m21} was swept through its entire tuning range while two different control voltages for G_{m22} were selected: $V_{m22} = -1.2V$ (medium Q), $V_{m22} = -0.092V$ (low Q). The other control voltages were fixed as follows: $V_{mi} = 1.74V$ (maximum filter gain), $V_{mb} = -0.575V$ (zero well below 1MHz). A plot of the experimental results for this test is shown in Figure 5.4. From the results, we note the filter can be tuned from 10MHz to 230MHz giving a tuning range of 4.5 octaves (tuning range ratio of 23) for 5V supplies. For a total power supply level of 3V, the filter worked satisfactorily and displayed a tuning range of 9MHz to 135MHz. Some of the results depicting the bandpass and lowpass outputs are shown in Figure 5.5. The input level, v_{in} , was -50dBm for the output responses shown in Figure 5.5, except for the high frequency high Q case which was -60dBm. The results for the same test but emphasizing the lower portion of the tuning range are shown in Figure 5.6.

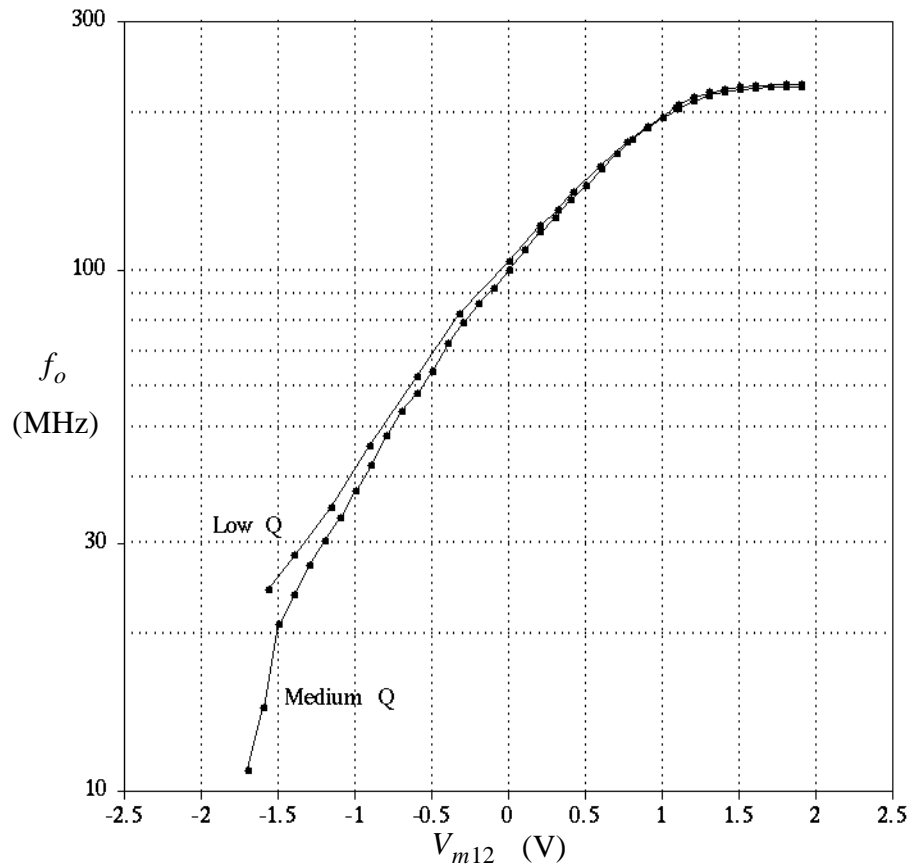


Figure 5.4: Illustrating pole frequency tuning range for two different filter Q s.

From Figures 5.5 and 5.6 we note that Q is not independent of f_o tuning and is more sensitive to tuning to f_o at a low setting for filter Q . This result is expected as can be obtained by examining the sensitivity of filter Q as function of G_{m22} and G_{m12} (see equations 4.44 and 4.45). The variation in filter Q as one tunes filter f_o is shown in Figure 5.7.

It is also interesting to examine the filter bandwidth, f_o/Q , as a function of f_o tuning. The results are shown in Figure 5.8 for a medium filter Q and a low filter Q , respectively. Observe that at lower frequencies the filter bandwidth is less sensitive to pole frequency-tuning, while at higher frequencies the sensitivity increases.

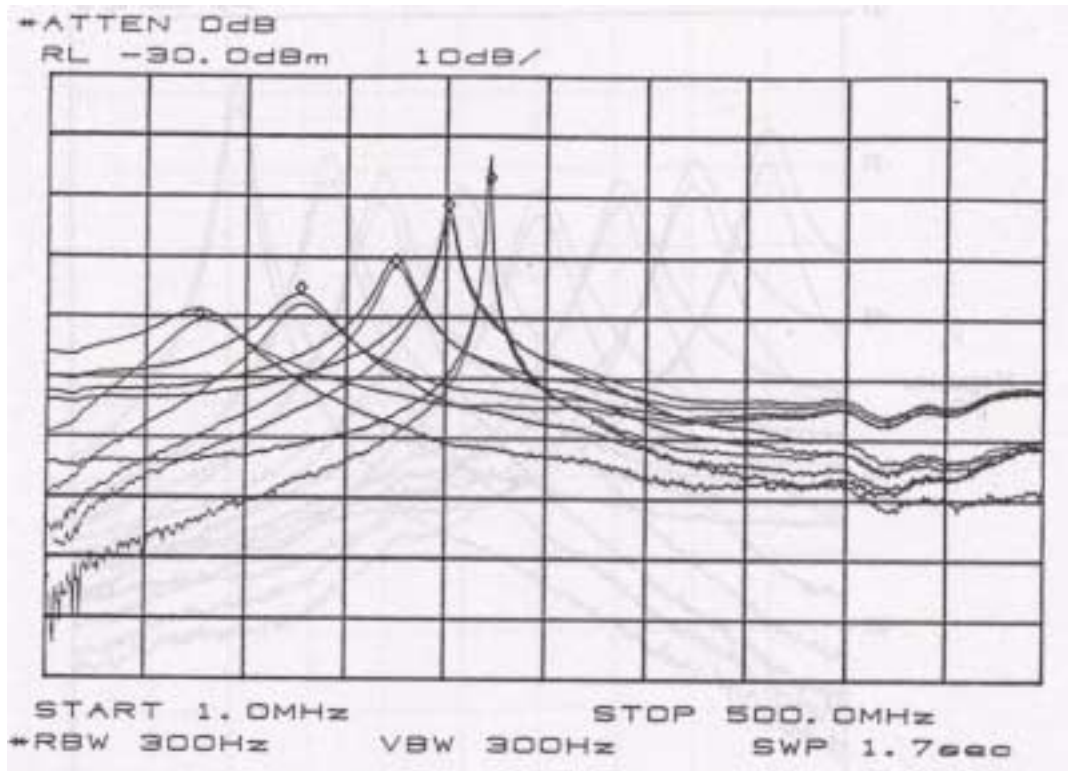


Figure 5.5: Illustrating pole frequency tuning for a medium value for filter Q .

The quality factor of the biquad can be tuned from about 1 to a value that can initiate filter oscillation. A plot of the maximum Q (Q_{max}) for a given f_o while ensuring the filter does not oscillate is given in Figure 5.9. Notice that Q_{max} is higher at higher frequencies and is a consequence of the fact that as we tune for lower speeds, the integrators become more ill phased due to the low DC gain which reduces the integrator inherent quality factor. Higher filter Q s were observed; the results of Figure 5.9 are somewhat pessimistic since it was ensured that at the quoted value for Q_{max} the filter was far from the oscillation point.

In Figures 5.10-5.12 we show the obtained bandpass filter response for various Q values at four different settings for filter f_o . Notice that the pole frequency is also not independent of Q tuning as evident from Figure 5.13. However, observe that the pole frequency becomes less sensitive to Q tuning at higher frequencies and at higher Q . This result is also expected and can be obtained by looking at the sensitivity of f_o as function of G_{m12} and G_{m22} from (4.44)

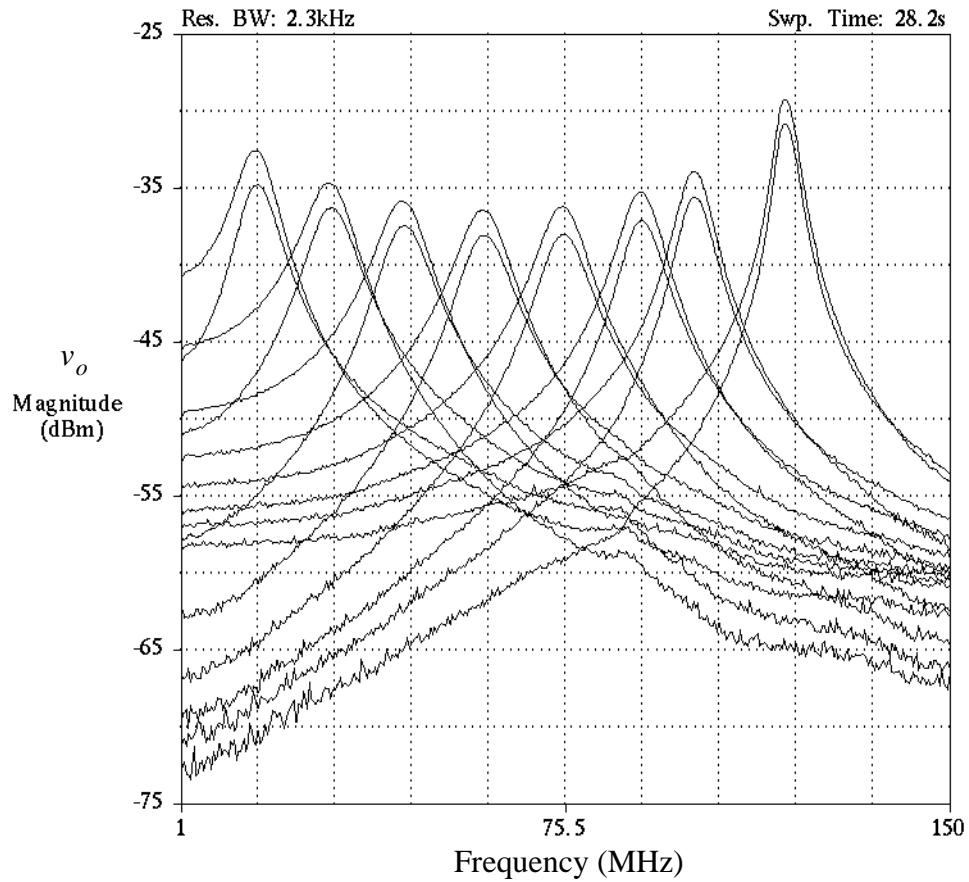


Figure 5.6: Illustrating pole-frequency tuning for a medium value for filter Q . Input level for each curve is -30dBm.

and (4.45). Although these dependencies exist, they should not be of great concern since an adaptive system will correct for this type of problem. In fact, this is one of the reasons why an adaptive filter is preferable to the master/slave technique.

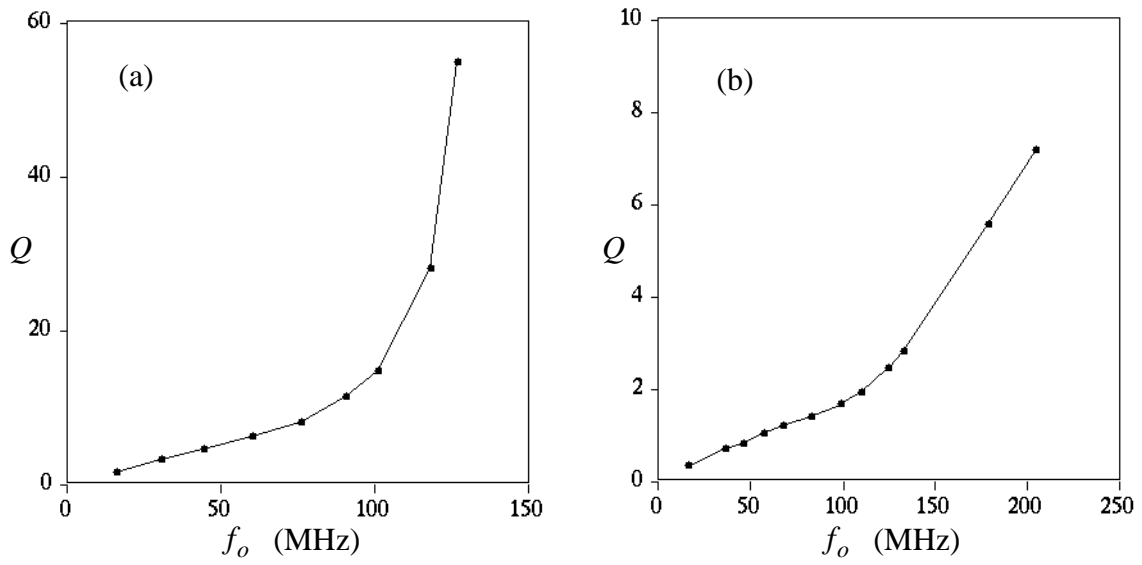


Figure 5.7: Illustrating Q deviation due to f_o tuning at: a) medium Q , b) low Q .

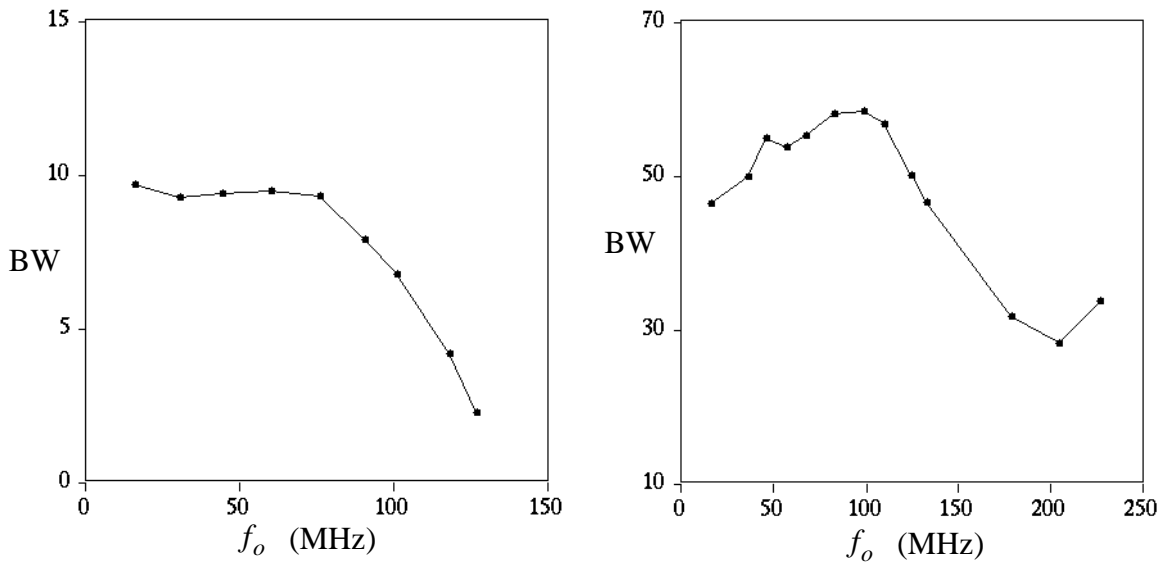


Figure 5.8: Illustrating BW deviation due to f_o tuning at: a) medium Q , b) low Q .

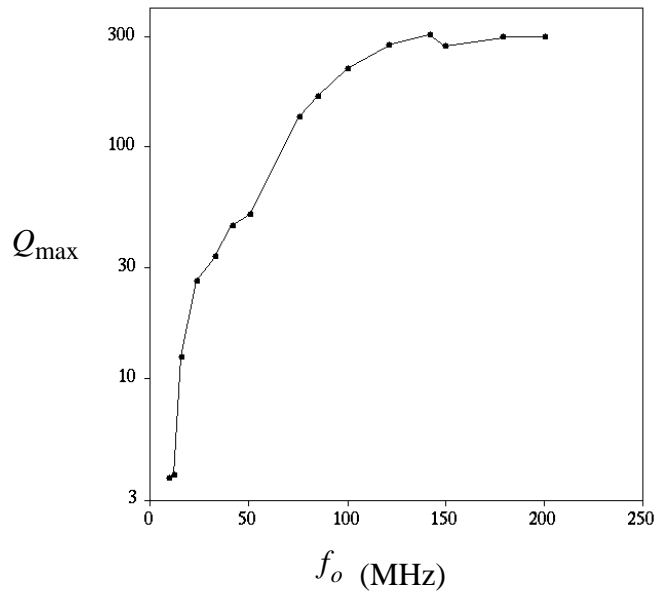


Figure 5.9: Illustrating the maximum Q as function of filter pole frequency.

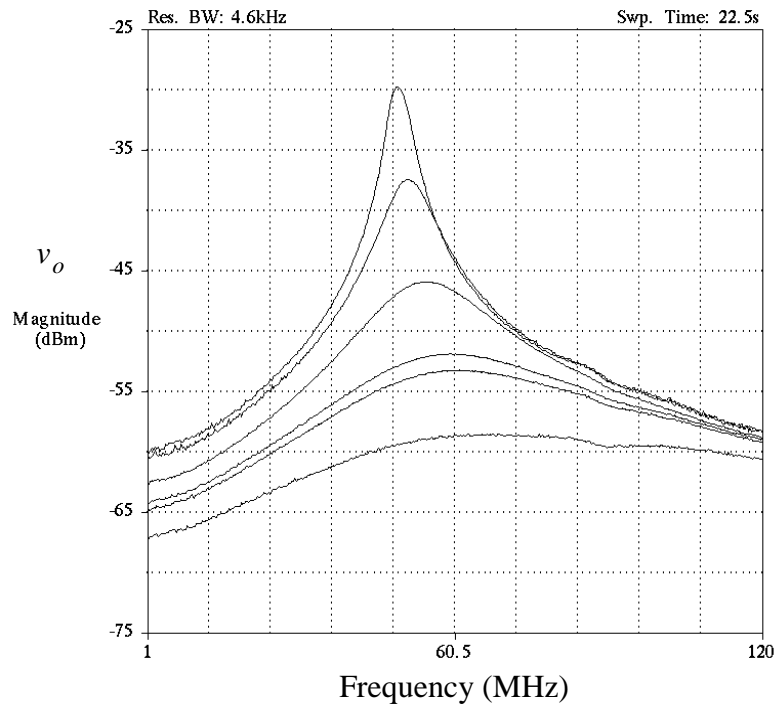


Figure 5.10: Bandpass filter output response for $f_o = 50\text{MHz}$ and various Q . Input level for each curve is -30dBm .

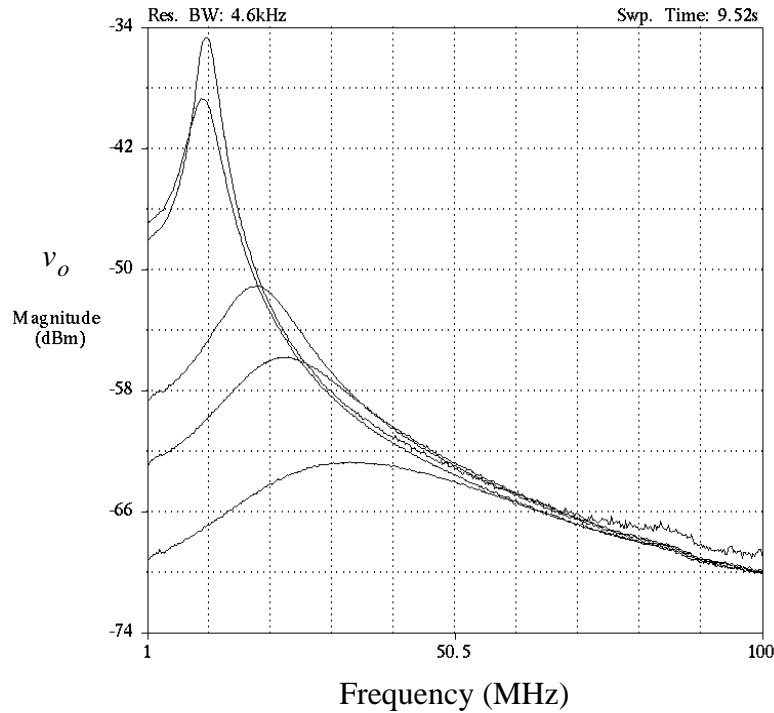


Figure 5.11: Bandpass filter response for $f_o = 10\text{MHz}$ and various Q . Input level for each curve is -40dBm .

5.2.2 Detailed Filter Characterization

In this section, we present detailed characterization and a general explanation of the experiment for one particular filter setting, namely $f_o = 100\text{MHz}$ and $Q = 15$. It should be mentioned here that for our intended application, filter pole-frequency is also about 100MHz but with a filter $Q = 2$. Unfortunately, since output noise at low filter Q s was dominated by the test equipment due to the low gain of the probe devices, detailed test results are discussed for the $Q = 15$ filter. The test procedures were also conducted, where possible, for three other filter settings to allow a comparison to determine the effects of f_o and Q on the performance of the filter. A summary of the results is presented in Section 5.2.3 together with a brief discussion.

The simulated and experimental curves for a filter setting of: $V_{mi} = 1.74\text{V}$, $V_{mb} = -0.575\text{V}$, $V_{m12} = -0.003\text{V}$ and $V_{m22} = -1.2\text{V}$ are depicted in Figure 5.14. From the figure, it

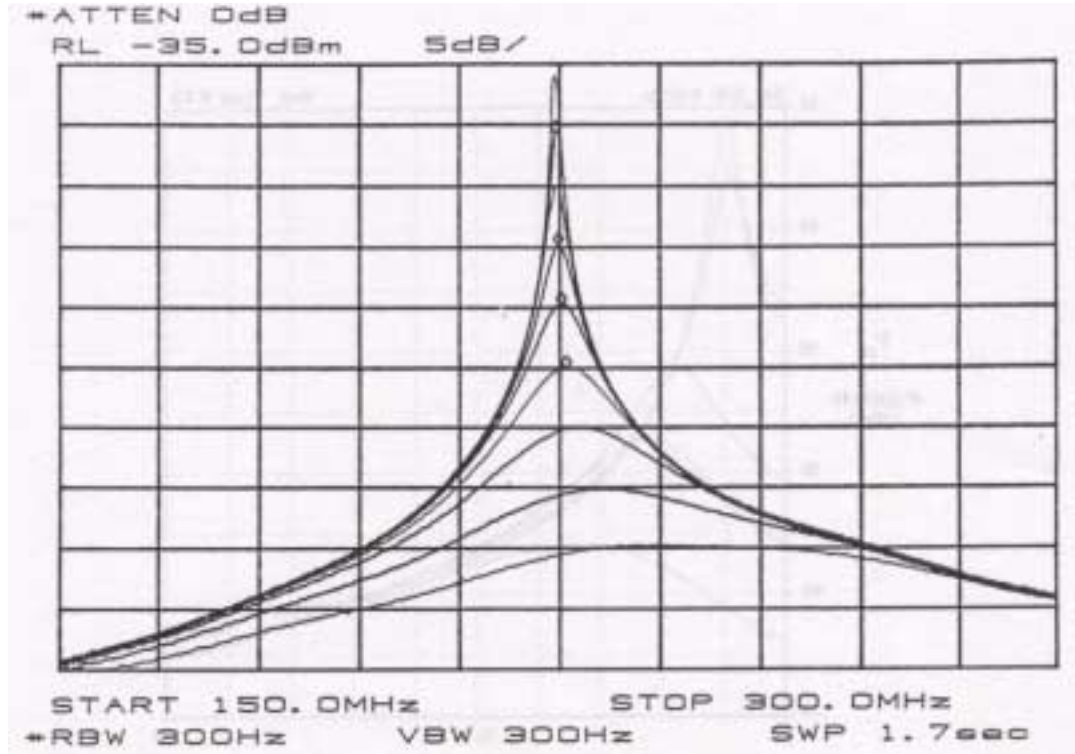


Figure 5.12: Bandpass filter response for $f_o = 227\text{MHz}$ and various values for Q . Input level for each is -50dBm .

can be noticed that the experimental results indicate the filter runs about 54% faster than expected and exhibits a much lower Q -factor. Recall from Section 4.4 and (4.20) that transconductor speed depends on G_m , which relates to input device g_m , while Q depends on transconductor output conductance. Thus, the experimental results imply that g_m is higher than its simulated value and device output conductance is larger than its simulated value. These effects are attributed to shorter fabricated channel lengths². The effect was also apparent from the transconductor test results (see Section 5.4). Hence, one can appreciate the need for post fabrication tuning which is why adaptive filters are important. For this filter setting, it can be obtained from the bandpass output response that $f_o = 100.4\text{MHz}$ while the lower 3dB frequency is at 97.2MHz and the upper 3dB frequency is at 103.8MHz . These results corresponds to a filter Q of 15. The responses in Figure 5.14 correspond to an input level v_{in}

2. Based on independent BNR test results, the fabricated batch had MOS electrical channel lengths 38% smaller than their target values and V_t was 10% smaller.

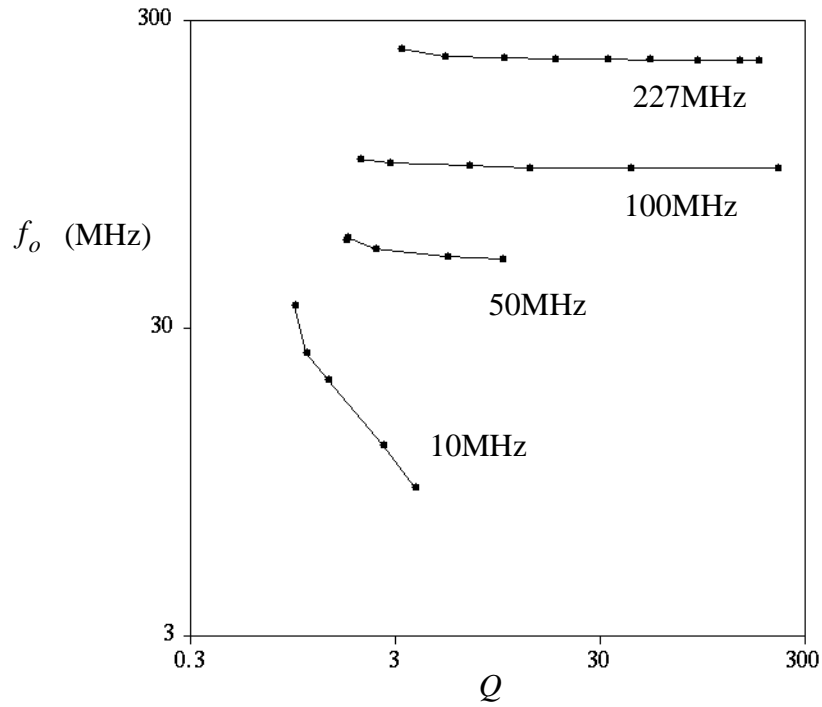


Figure 5.13: Variation in filter f_o due to Q tuning at three different f_o settings.

of -30dBm which is equivalent to a filter differential input v_{id} level of -27dBm or 10mV_{rms} (see Figure 5.3 for level conversion details). For the bandpass response, the output level v_o is -36.7dBm which corresponds to a differential filter buffer output level \hat{v}_{od} of -32.7dBm. The differential insertion loss across the output buffers was deduced experimentally to be 35dB which compares with the simulated value. Using this figure, we obtain an internal filter differential output level v_{od} of 2.3dBm or $291\text{mV}_{\text{rms}}$. Therefore, for this filter setting, the filter gain is 29.1V/V or 29.3dB.

5.2.2.1 Intermodulation Distortion and Harmonic Distortion

The experimental results for the IM test conducted are given in Table 5.1. The two input tones v_{in1} and v_{in2} were positioned at $f_1 = 99.3\text{MHz}$ and $f_2 = f_o = 100.4\text{MHz}$ resulting in the distortion products \overline{IM}_{3L} and \overline{IM}_{3H} at 98.2MHz and 101.5MHz, respectively. The measurements were done at the filter's bandpass output. The input tones were summed using

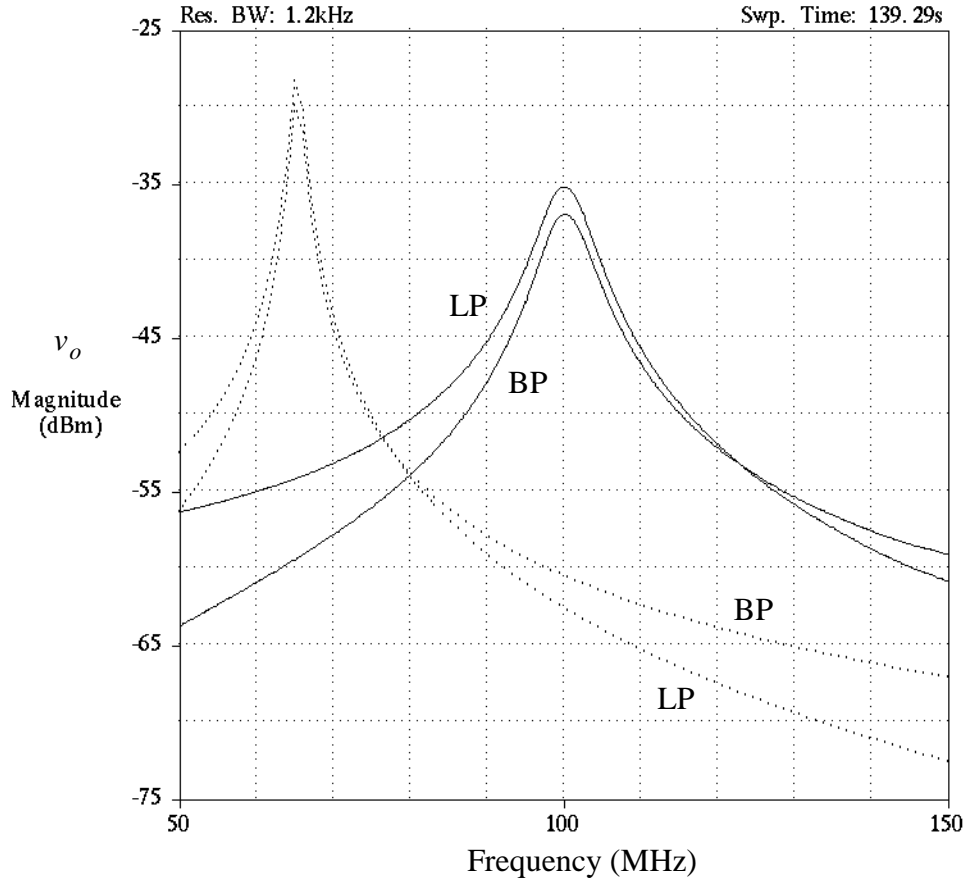


Figure 5.14: Simulated (dotted curves) and experimental (solid curves) results for the outputs of the 100MHz filter with a Q of 15.

a power combiner and supplied to the filter at node T_{IN} . Letting v_{in} represent the *rms* sum of v_{in1} and v_{in2} , letting v_o represent the *rms* sum of the output fundamental tones v_{o1} and v_{o2} , and letting $\overline{IM_3}$ represent the *rms* sum of the distortion products $\overline{IM_{3L}}$ and $\overline{IM_{3H}}$, the resulting output *SDR* would be given by the ratio $\frac{v_o}{\overline{IM_3}}$. From the results in Table 5.1, the intercept point at node T_{OUT} calculates to -21dBm. This corresponds to an internal differential filter bandpass output IP_3 of 18dBm ($1.8V_{rms}$), or a filter differential input IP_3 of -11.3dBm ($60.9mV_{rms}$) for the above filter setting. Based on the output IP_3 , the output level for any *SDR* can be obtained from (5.10). For example, we expect 1% distortion ($SDR = 40dB$) at a total differential filter output level of -2dBm ($177.6mV_{rms}$) giving a differential filter input level of -31.3dBm ($6.1mV_{rms}$). Observe also from the Table 5.1 that in the linear region of operation

the expected 3:1 ratio mentioned above is obeyed. Figure 5.15 shows the IM test for the case in row 1 of Table 5.1.

Table 5.1: Results for IM distortion: 100MHz, $Q = 15$, all entries in dBm.

v_{in1}	v_{in2}	v_{o1}	v_{o2}	\overline{IM}_{3L}	\overline{IM}_{3H}	SDR
-35.7	-36.1	-43.2	-43.2	-81.1	-80.1	37.4
-33.3	-34.0	-41.0	-41.8	-74.4	-74.2	32.9
-31.4	-31.7	-39.5	-38.4	-71.3	-67.1	29.8
-28.6	-28.1	-37.2	-34.6	-65.6	-57.6	24.3

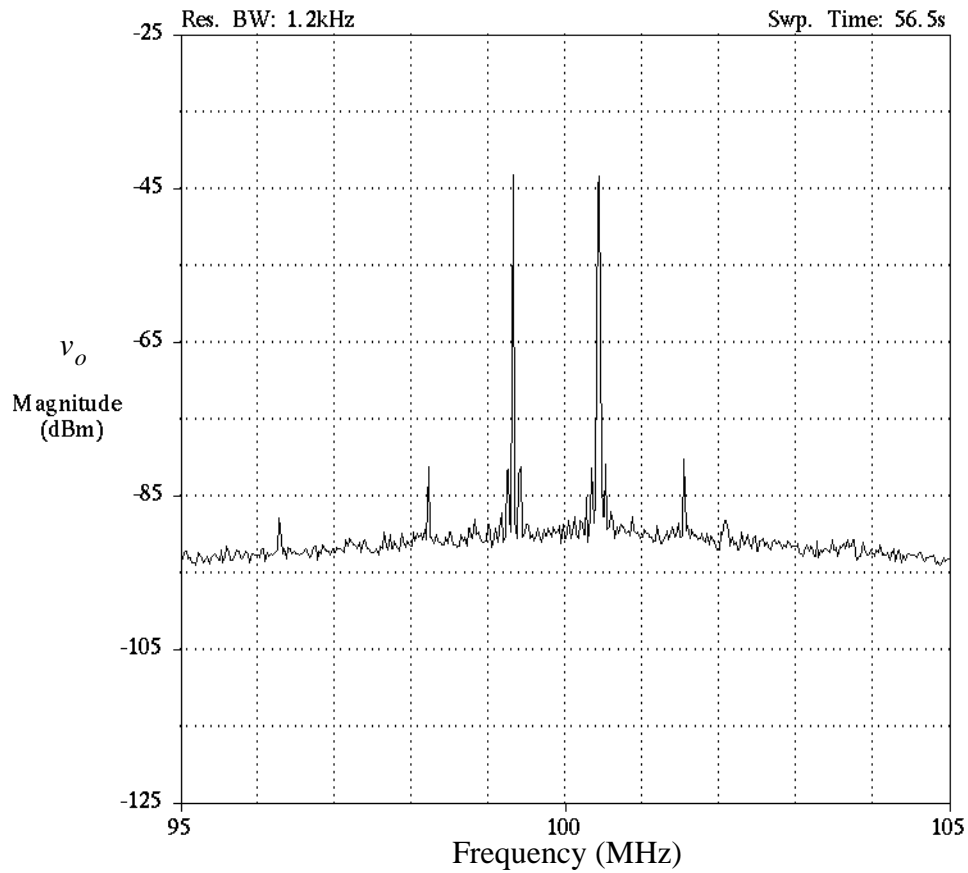


Figure 5.15: Measured IM distortion of the 100MHz, $Q=15$ filter.

Table 5.2 shows the IM test results for the 100MHz, $Q = 2$ filter — the setting for the intended application. From the results, we obtain an internal (before the probes) filter differential bandpass output IP_3 of 23dBm implying 500mV peak internal differential-output signal levels for 1% SDR . In comparison, the simulated differential IP_3 was 25dBm at the bandpass output which agrees well with the experimental value. However, simulation results indicate that the IP_3 level was 29dBm at the lowpass output. To understand the reason for the lower IP_3 at the bandpass output, consider the signal levels of the lowpass and bandpass outputs as seen in Figure 5.14, and refer to Figure 4.18. Since the bandpass output level is lower than the lowpass output level, but both outputs experience about the same SDR (due to the feedback loop), a lower IP_3 at the bandpass output is expected as seen by using (5.10).

Table 5.2: Results for IM distortion: 100MHz, $Q = 2$, all entries in dBm.

v_{in1}	v_{in2}	v_{o1}	v_{o2}	\overline{IM}_{3L}	\overline{IM}_{3H}	SDR
-15.4	-15.3	-45.9	-44.0	-96.0	-94.7	50.5
-13.1	-13.2	-43.0	-41.0	-90.5	-85.5	45.4
-9.6	-9.4	-39.6	-37.8	-81.4	-75.8	41.0
-7.2	-7.2	-37.1	-35.5	-74.3	-69.9	35.3

Since simulation and experimental results for the biquad filter are in reasonable agreement, it is likely that a simulation of the transconductor alone is accurate in predicting distortion performance. The simulated differential output IP_3 for an isolated integrator, G_{m12} , (with a tuning control voltage of -0.003V as in the filter loop given in Section 5.2.2) was 36dBm. However, the question arises as to why the filter performance is approximately 7dB worse than the transconductor alone. The reason is due to the fact that the filter peak at $f = f_o$ is proportional to filter Q . Hence, a linearity figure for the filter at low Q would more accurately predict transconductor performance. Analytically, it can be shown that for the biquad filter, $SDR \propto Q^{-3}$ while output $IP_3 \propto Q^{-1/2}$ for frequencies near f_o . These relationships were verified in a variety of simulations. For example, for an input level of

25mV_{rms} , the simulated SDR and IP_3 for different filter Q values were evaluated and the results are given in Table 5.2.

Table 5.3: Simulated SDR and IP_3 as function of filter Q .

Q	SDR [dB]	IP_3 [dBm]
1.9	83	29
2.8	73	27
4.45	60	24.5
0.8	104	33.5

Finally, it should be emphasized that distortion performance degrades at lower settings for G_m where transconductance subtraction takes place. This effect was also verified through simulation studies. As well, it should be mentioned here that simulation results showed that the SDR at the probe outputs was similar to the SDR at the filter outputs. Hence, the experimental measurements at the probe devices are reasonable in specifying filter performance. Recall that the probe devices are NMOS transistors which have the same gate-source voltage as the input devices. Since these NMOS devices have a lower V_t compared to the input PMOS devices, and since NMOS devices have a lower horizontal critical electric field, the linearization in output current due to mobility degradation and velocity saturation would be more pronounced. Hence, it is reasonable to expect better linearity from the probe devices than the input devices. Thus, transconductor linearity would always be worse than the linearity of the probe devices which explains why their effect on SDR was not apparent in the simulations.

5.2.2.2 Filter Compression Test

To determine the CP_1 , the filter differential input level was swept over a range of power levels and the filter peak bandpass output level was measured. The results of this test are given

in Figure 5.16. From the figure, we obtain an internal differential filter output CP_1 of 6dBm ($446\text{mV}_{\text{rms}}$) or a filter differential input CP_1 of -22.6dBm ($16.8\text{mV}_{\text{rms}}$).

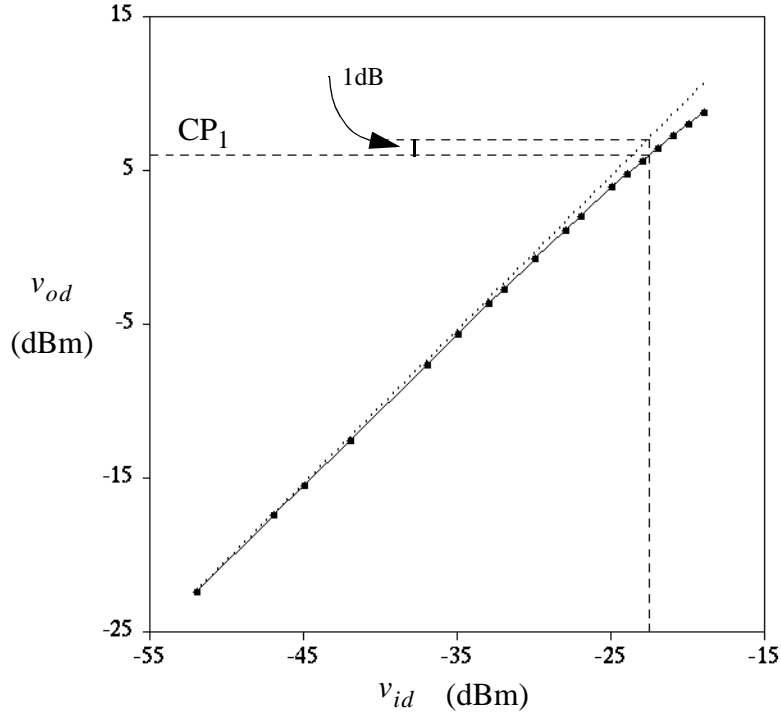


Figure 5.16: Measured filter compression at 100MHz and a Q of 15.

5.2.2.3 Noise Test

To measure filter output noise, the filter inputs were grounded and the spectrum at the bandpass output was observed. The result of this test is given in Figure 5.17a. The filter output spectrum is also given for comparison in Figure 5.17b for an input level v_{in} of -40dBm. Note that the noise spectrum has a similar response as the filter output. The measured peak spectral density is about $-91.3\text{dBm}/\text{Hz}$ or $.1\mu\text{V}_{\text{rms}}/\sqrt{\text{Hz}}$ on an internal differential filter output and the total internal differential output noise is $19.6\text{mV}_{\text{rms}}$. This noise level is quite high and is about 43dB higher than the kT/C bound found above. The reason is mostly attributed to the large base resistances ($650\text{-}1000\Omega$) of the BJTs, specifically $Q_5 - Q_{10}$. These devices exhibit a high transconductance, and hence, high noise gain to the output. Recall from Section 4.3.3 that a 24dB degradation in SNR is due to the

bipolar transistors. For this design, the smallest BJTs with a single base contact were used since the design was optimized for speed and power consumption. Larger BJTs with more base contacts to reduce base resistance and emitter degeneration could have been used to reduce the noise by at least 10dB as was discussed in Section 4.3.3.1. The cost for this alternative would have been more power consumption and a lower secondary transconductor pole. Considering the $19.6\text{mV}_{\text{rms}}$ total noise, we obtain a SNR of 19dB at the 1% IM distortion level found above. Thus, noise dominates the linearity of this filter. Finally, for this filter setting the measured differential input-referred noise density is $.21\mu\text{V}_{\text{rms}}/\sqrt{\text{Hz}}$ which compares well with a simulated figure of $.223\mu\text{V}_{\text{rms}}/\sqrt{\text{Hz}}$.

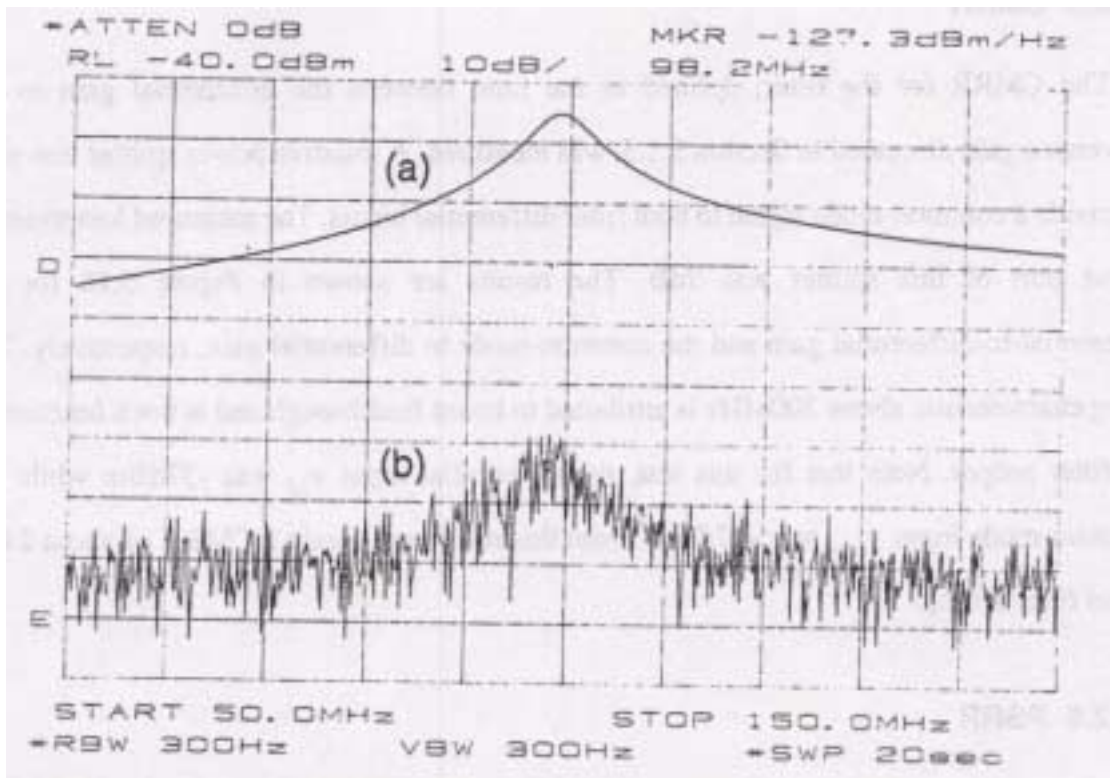


Figure 5.17: Filter noise response (a) and filter magnitude response (b). Filter input level is -40dBm.

5.2.2.4 SFDR and Peak Dynamic Range

Making use of the above results for IP_3 and the filter output noise, a $SFDR$ of 26dB for this filter setting is obtained. This value is somewhat marginal for data communication applications for proper “eye” opening. (Recall from Chapter 2 that at least 17dB is required). However, it should be noted that the filter Q is 15 which is more than would be required for pulse-shaping, tunable filters for example. At a lower Q , one would expect much lower distortion and noise, hence, a better $SFDR$ figure as will be noted from Table 5.5.

The peak dynamic range based on the above $SFDR$ is therefore 23dB.

5.2.2.5 CMRR

The CMRR for the filter, defined as the ratio between the differential gain to the conversion gain discussed in Section 5.1.5, was measured. A resistive power splitter was used to provide a common-mode signal to both filter differential inputs. The measured loss to either output port of this splitter was 7dB. The results are shown in Figure 5.18 for the differential-to-differential gain and the common-mode to differential gain, respectively. The rising characteristic above 300MHz is attributed to board feedthrough and is not a function of the filter proper. Note that for this test, the differential input v_{id} was -37dBm while the common-mode input v_{icm} was -47dBm. From this result, we obtain a CMRR of about 21dB at this filter setting.

5.2.2.6 PSRR

To measure the filter PSRR, the configuration in Figure 5.19 was used successively for each power supply. For an input level of -10dBm the level at v_{ps} for the positive supply was -22.08dBm. The output spectrum at v_o is shown in Figure 5.20a where it appears that the output level at 100MHz is -59.70dBm. For the same tuning voltages the differential gain from filter input v_{id} to system output v_o was -10dB (see section 5.2.2). Hence, the PSSR+ is 28dB.

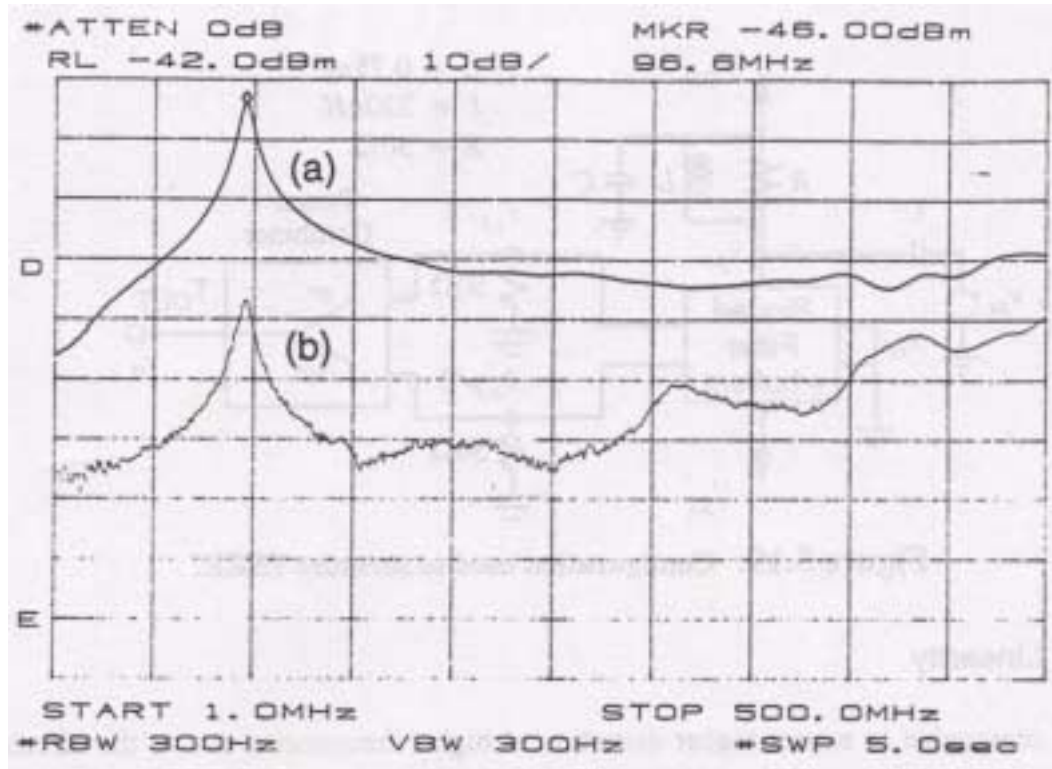


Figure 5.18: (a) filter differential response, (b) filter common-mode response. Both inputs are at -40dBm.

Similarly, for the negative power supply the level at v_{ps} was -32.78dBm. The output spectrum at v_o is shown in Figure 5.20b where it appears that the output level at 100MHz is -64.62dBm giving a PSSR- of 22dB. The lower PSRR for the negative supply is attributed the fact that the test-probe devices sense only the negative supply.

5.2.3 Results Summary and Discussion

The procedures outlined in Section 5.2.2 were repeated for three other filter settings to allow a comparison of filter performance. Additional relevant data is provided in Table 5.4 while a complete summary of the main results is given in Table 5.5. In this section, we discuss the results obtained.

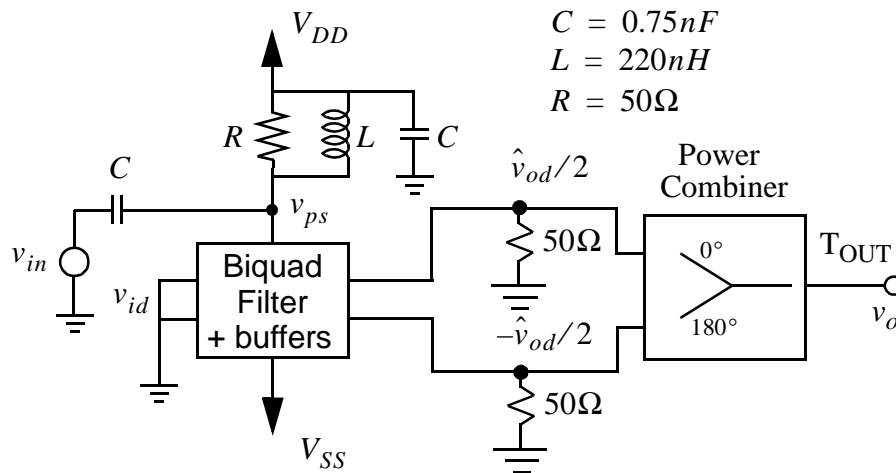


Figure 5.19: Configuration used to measure PSRR.

5.2.3.1 Linearity

It is reasonable to expect higher distortion at higher frequencies due to the effects of parasitic capacitors which become significant at high frequencies. Consequently, phase errors take place and if parasitics are mismatched between each half-circuit signal path, the overall differential signal will display distortion. Also, as mentioned in Section 4.3.4, at the low frequency end transconductance subtraction takes place. Hence, it is also reasonable to expect lower linearity at the low end, and thus, maximum linearity should take place when the filter (transconductor) is tuned to mid-range. This expectation can be noted from the experimental results for the IP_3 at the different filter settings. Also, the dependence of filter SDR and output IP_3 on filter Q , as discussed in Section 5.2.2.1, can be observed from the linearity results for the two 100MHz filter settings.

Finally, note from Table 5.5 that the analytic prediction in (5.15) is approximately observed.

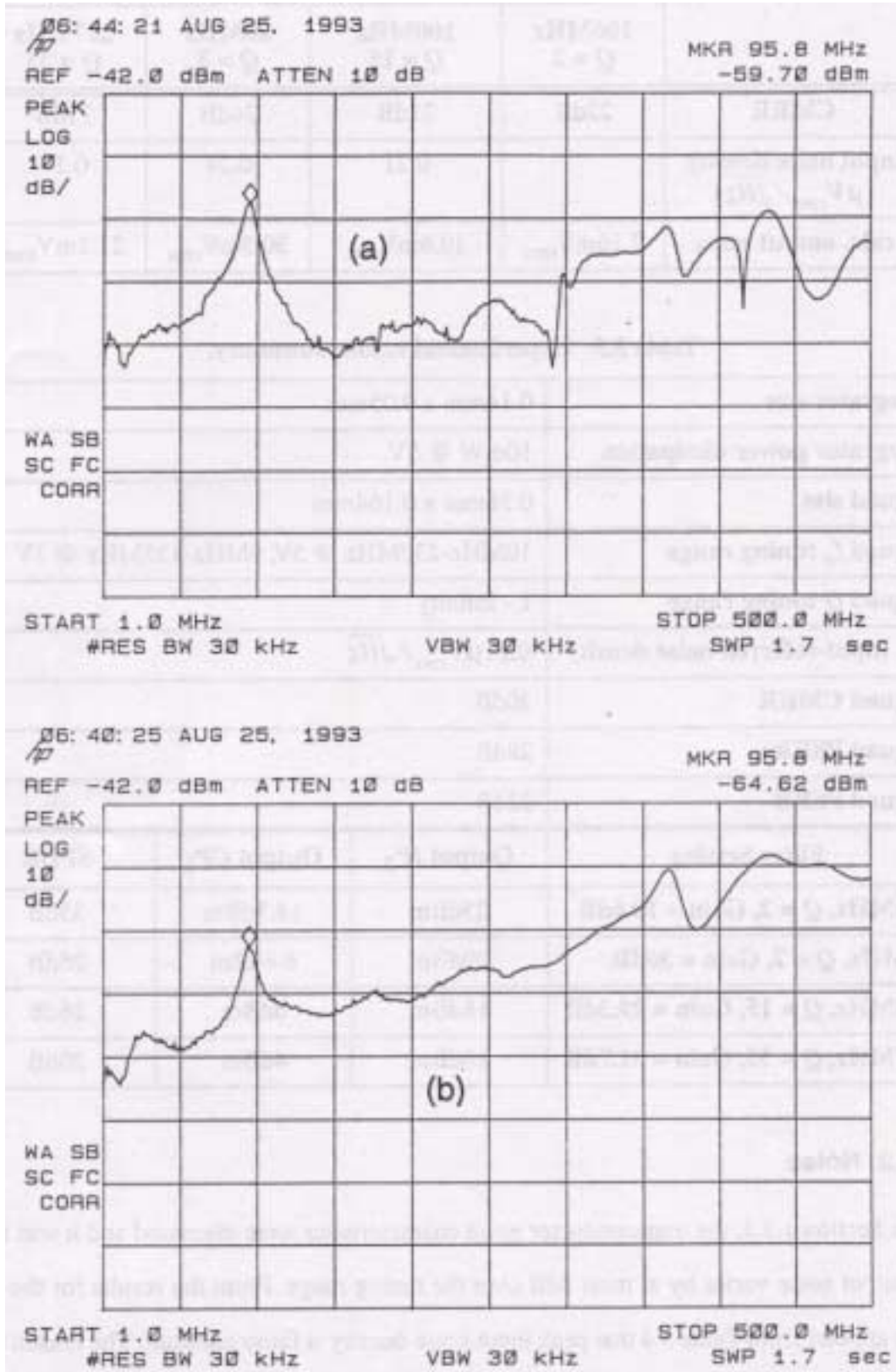


Figure 5.20: Output spectrums for an AC signal supplied to a) V_{dd} , b) V_{ss} .

Table 5.4: Additional test results.

	106MHz $Q = 2$	100MHz $Q = 15$	20MHz $Q = 2$	227MHz $Q = 35$
CMRR	22dB	21dB	24dB	21dB
input noise density [$\mu V_{rms}/\sqrt{Hz}$]		0.21	0.24	0.17
calc. output noise	7.16mV _{rms}	19.6mV _{rms}	30.5mV _{rms}	21.1mV _{rms}

Table 5.5: Experimental results summary.

Integrator size	0.14mm x 0.05mm		
Integrator power dissipation	10mW @ 5V		
Biquad size	0.36mm x 0.164mm		
Biquad f_o tuning range	10MHz-230MHz @ 5V, 9MHz-135MHz @ 3V		
Biquad Q tuning range	1 - Infinity		
Bq. input-referred noise density	$.21 \mu V_{rms}/\sqrt{Hz}$		
Biquad CMRR	20dB		
Biquad PSRR+	28dB		
Biquad PSRR-	22dB		
Filter Setting	Output IP_3	Output CP_1	SFDR
106MHz, $Q = 2$, Gain = 10.6dB	23dBm	14.3dBm	35dB
20MHz, $Q = 2$, Gain = 30dB	20dBm	6.6dBm	26dB
100MHz, $Q = 15$, Gain = 29.3dB	18dBm	6dBm	26dB
227MHz, $Q = 35$, Gain = 31.7dB	10dBm	4dBm	20dB

5.2.3.2 Noise

In Section 4.3.3, the transconductor noise characteristics were discussed and it was found that output noise varies by at most 8dB over the tuning range. From the results for the noise test, it appears from Table 5.4 that peak input noise density is fairly constant. The reason being that G_{mi} and G_{m22} were always tuned to one extreme of the tuning range dominating output

noise. Hence, variation in G_{m12} and G_{m21} did not affect the overall noise. It is therefore reasonable to assume constant input noise density for the filter, and, based on the theory in Section 5.1.3, one can claim that the filter output noise can be easily approximated using the expression

$$\overline{e_n^2} \approx \frac{\pi}{2} K^2 f_o Q \overline{v_n^2} \quad (5.24)$$

where $\overline{v_n}$ is given in Table 5.5 as $.1\mu V_{rms}/\sqrt{Hz}$. Thus, (5.24) clearly illustrates the effects of f_o , Q and K on output noise.

It should be mentioned here that the ideal transfer-function in (5.17) models the prototype filter transfer function in (4.43) where $K = \frac{G_{mi}}{G_m}$ and $G_m = G_{m12} = G_{m21}$. For the four cases tested, G_{mi} was set to its maximum value, hence,

$$K = \frac{G_{m,max}}{G_m} = \frac{230MHz}{f_o}. \quad (5.25)$$

5.2.3.3 CMRR

From the experimental data in Table 5.4, it can be noted that the *CMRR* is worse at higher frequencies and best at lower frequencies. Also, we note from the results of the 100MHz filter and the 106MHz filter that the *CMRR* is insensitive to filter Q . These observations are to be expected since the common-mode gain depends on circuit mismatch. The sources of mismatch are the BJT current mirrors which, due to base current loss, will result in the common-mode currents produced by the two input stages to be different. Also, any fabrication errors in the input devices will lead to mismatch and degrade the *CMRR*.

Consider the filter tuned for low speed implying $V_{C1} \gg V_{C2}$ for the transconductor in Figure 4.4. Hence, the output common-mode signal at the half-circuit output nodes will depend on the difference currents between M_3, M_1 and M_4, M_2 , respectively. Alternatively, for a setting giving maximum speed (i.e. $V_{C1} \ll V_{C2}$), the output common-mode signal at the

half-circuit output nodes will depend on the difference currents between M_3, M_2 and M_4, M_1 , respectively. In the layout, the transistor pairs M_1 and M_3 were each in close proximity as well as the pair M_2 and M_4 . However, each pair of transistors was not very close to the other pair. Hence, it is reasonable to expect better pair matching between M_3, M_1 and M_4, M_2 than M_3, M_2 and M_4, M_1 . Thus, the better experimental $CMRR$ at the lower speed is reasonable.

Finally, it should be mentioned that at higher frequencies feedthrough, due to capacitive coupling, is more pronounced. Thus, mismatched feedthroughs will also result in higher common-mode gain reducing $CMRR$ at the high frequency end. However, from the results in Table 5.4, it appears that between 100MHz and 227MHz the $CMRR$ is not degraded by this mechanism.

5.2.3.4 SFDR

The dependency of $SFDR$ on filter f_o and Q can be easily obtained from the expression in (5.22) which relates to the dependency of filter noise and linearity on these parameters.

5.2.4 Pulse Shaping Filter

To determine the practicality of adaptive techniques in the 100s of MHz range, the adaptive pulse-shaping filter, described in section 3.2, was implemented using the same biquad filter. A block diagram of the system is shown in Figure 5.21. While all critical high-frequency analog components were integrated, external circuitry consisted of two U/D counters, two low-frequency (not necessarily linear) 12-bit DACs, and simple digital logic.

The hardware configuration is illustrated in Figure 5.22. The oscillator serves as the system clock (100MHz) whose output is input to a delay board [Lussier 93]. This board consists of a Sony chip (CX1139Q) which is a programmable delay line/duty cycle controller. It provides three outputs including: the buffered input, the complement signal, and the

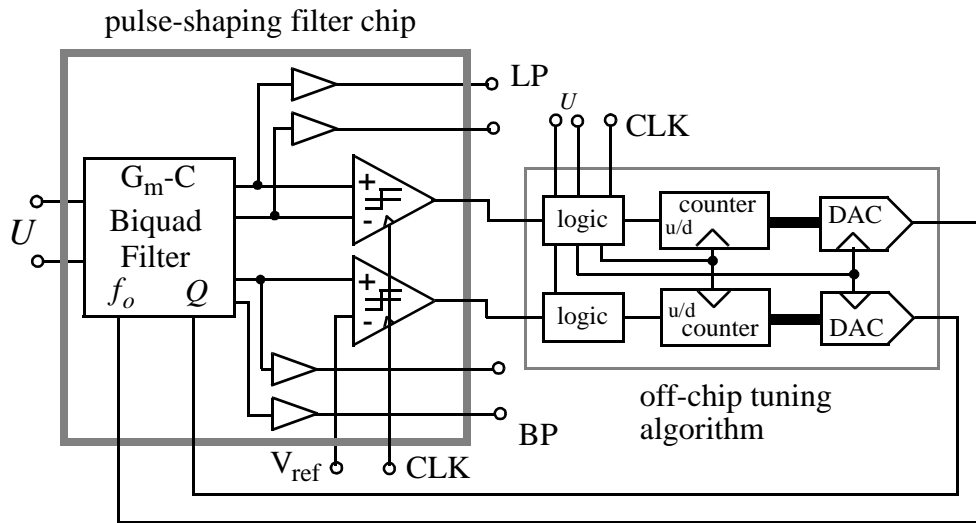


Figure 5.21: Block diagram of the adaptive pulse shaping filter system.

buffered input delayed by a given time that is user controlled through the selection of five bit lines giving 32 possible delays ranging from 0.775ns to 4.69ns. For the purposes of this work, the delay was set to 2.5ns. The two differential outputs of this board were input to a parallel to serial converter board. This board converts four 25Mb/s ECL NRZ data to a single differential NRZ data stream at 100Mb/s. Each output swings from -1.9V (digital low) to -1.1V (digital high) and is input to the filter chip. The delay between the filter input zero-crossing and the comparator trigger signal zero-crossing, measured at the filter chip inputs, was 2.64ns. Due to the input ECL levels, the filter chip rails were shifted to $V_{DD} = 1.0V$ and $V_{SS} = -4.0V$. Total chip power consumption was 640mW: 80mA from the positive supply and 140mA from the negative supply.

The comparator digital outputs were connected to two channels of the HP5214 4-channel, 1GS/s oscilloscope. The other two channels were connected to the filter input and output ports. The scope connected to the Ethernet via a general purpose interface bus (GPIB). On a remote SUN workstation labVIEW was running, and hence, the scope data was available to this software via the Ethernet. Based on the signal supplied from the scope (namely the 2 comparator outputs and the filter input signal), the LMS algorithm described in section 3.2 was

implemented. The outputs of the software (also of the algorithm) were two digital signals to address the two external DACs that drive the filter f_o coefficient (i.e. V_{m12} and V_{m21}) and the filter Q coefficient (i.e. V_{m22}). The other two controls were manually fixed as follows: $V_{mi} = -1.39V$ and $V_{mb} = -2.71V$.

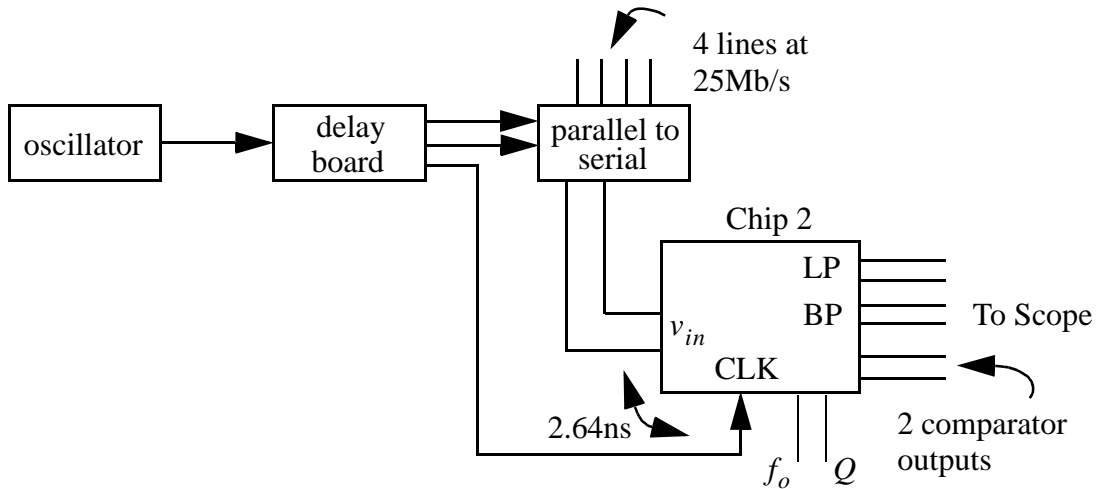


Figure 5.22: Hardware configuration for testing the system in Figure 5.21.

Since there are two degrees of freedom, there are four possibilities for a mistuned filter. These include: a filter mistuned to a pole frequency above nominal and a Q above nominal (HFHQ), a filter mistuned to a pole frequency above nominal and a Q below nominal (HFLQ), a filter mistuned to a pole frequency below nominal and a Q above nominal (LFHQ) and a filter mistuned to a pole frequency below nominal and a Q below nominal (LFLQ). Each of these possible initial conditions were set, and the filter was let to converge accordingly. Each iteration around the Ethernet-software loop took about 6s, hence, a coefficient update once in six seconds. The experimental coefficient trajectory for each of the initial conditions above are depicted in Figures 5.23-5.24. It is apparent that all four cases converged to the same final states. Observe that the steady-state limit cycle for the f_o coefficient is quite large (200mV). The reason for this behavior is due to DC offsets since the algorithm was modified to locate the dead-band introduced due to the offset as outlined in Section 3.2.4. As mentioned in

Section 3.2.4, the manifestation of this limit cycle leads to jitter in the filter output zero-crossing or variation in filter pole-frequency. The measured jitter was 422.5ps, that is, the attained output zero-crossing shifted from a minimal value of 2.8ns to a maximum value of 3.225ns. In the frequency domain, this zero-crossing jitter implies jitter in the filter pole-frequency. The filter pole-frequency was 111MHz at the 2.8ns delay and 95MHz at the 3.225ns delay for a total variation of 16MHz. Although this amount of jitter is small and may be tolerable in certain applications, it should be reduced by correcting for the offset problem. Compared with the target zero-crossing delay of 2.64ns, there is an error of at least 0.16ns which may be attributed to cable delays, experimental error and circuit performance error. The initial and final “eye” diagrams for each of the test cases are shown in Figures 5.25 and 5.26 where the improvement in “eye” opening, due to reduced ISI after convergence, is evident.

Observe from Figure 5.21 that to obtain the error signal for Q adaptation only a single-ended bandpass output was compared against a single-ended reference level. This single-ended circuitry was due to design time constraints, and so, a fully differential comparator was not fabricated. Consequently, there is no means of locating any dead-bands due to offset on the bandpass outputs.

Finally, in Figures 5.27-5.34 we illustrate the filter output spectra and the filter frequency responses before and after adaptation for the four cases investigated. In Figure 5.27(a), the filter NRZ input is also shown for comparison with the filter output spectra. Compared with unfiltered NRZ data, our pulse-shaping filter attains 10dB and 17dB harmonic suppression at the third and fifth harmonics of the fundamental frequency (50MHz), respectively.

5.3 Summary

In this chapter, a detailed characterization of the circuits implemented was performed. It was found that the tuning range of the filter spans 4.5 octaves (10-MHZ-230MHz at 5V) with

variable Q factors showing good tuning performance. Linearity was also satisfactory; however, noise performance was poor. Suggestions for improvement are given in Chapter 7. Finally, from the experimental results for the pulse-shaping filter, it is evident that adaptive analog filters using the idea of curve fitting are practical at high speed. Practical impairments such as DC offset and its effects on performance was also investigated and treated.

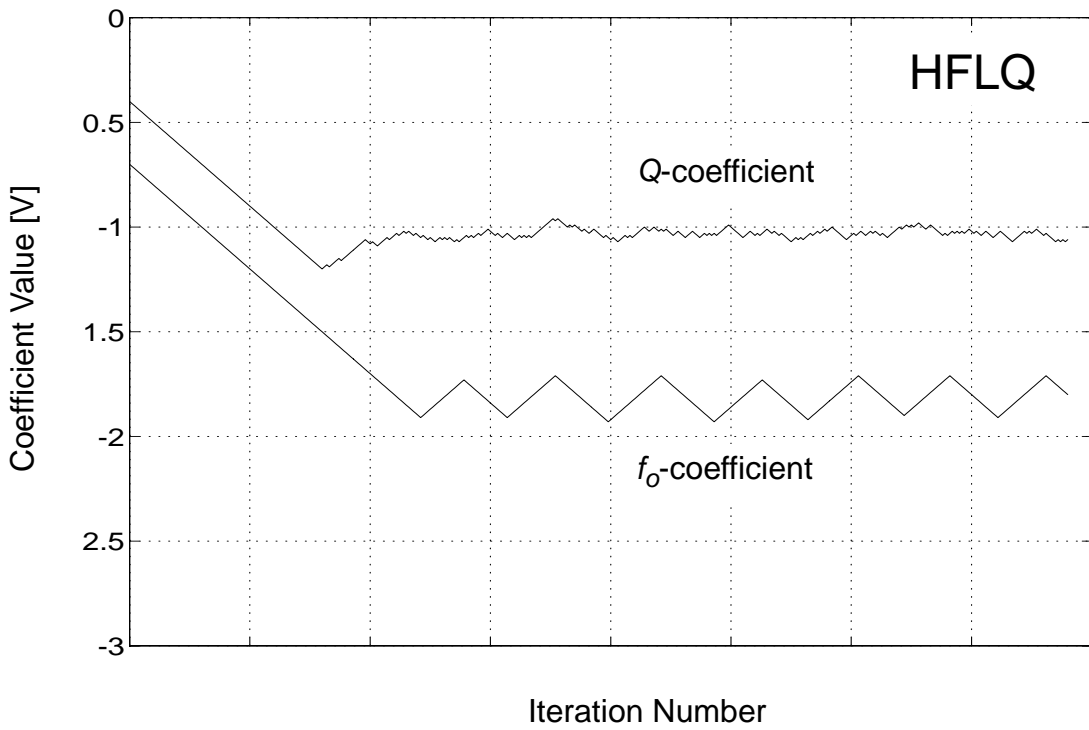
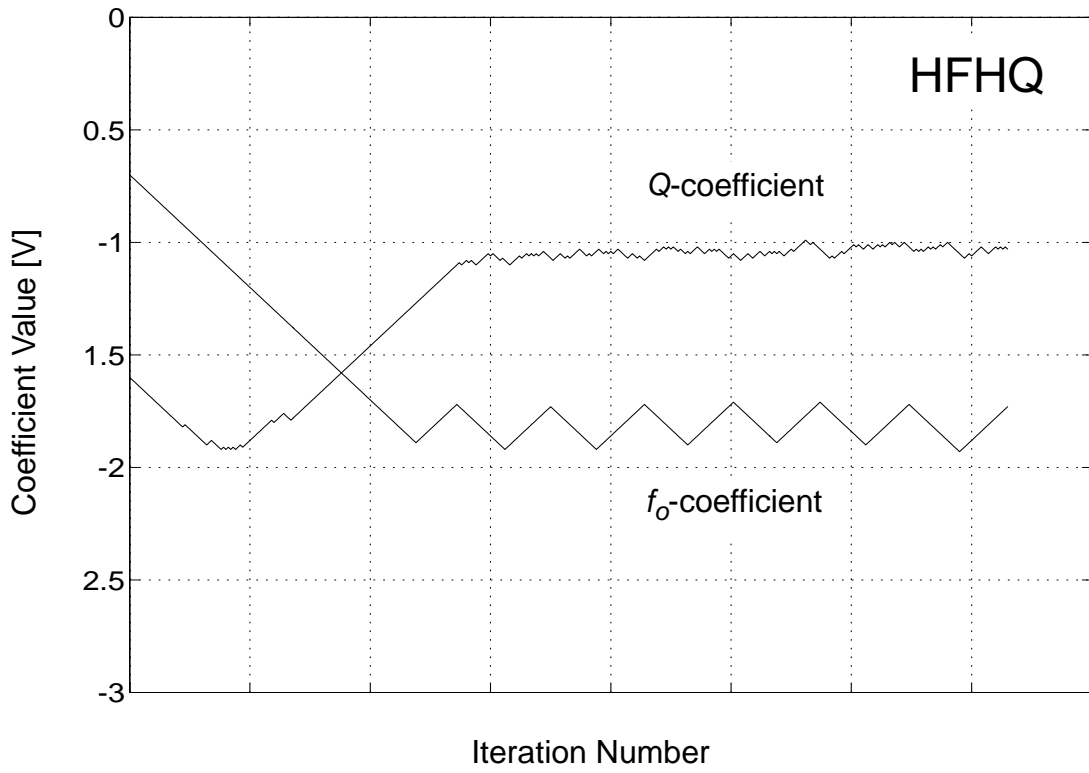


Figure 5.23: Experimental coefficient trajectory for the various test cases.

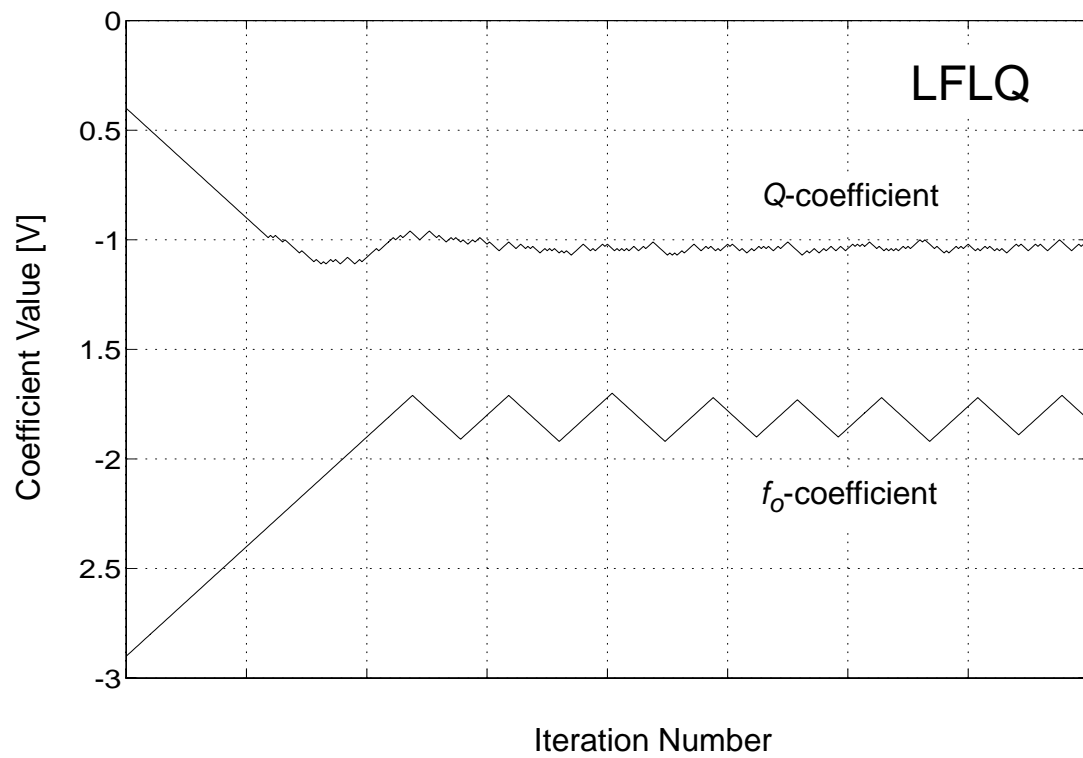
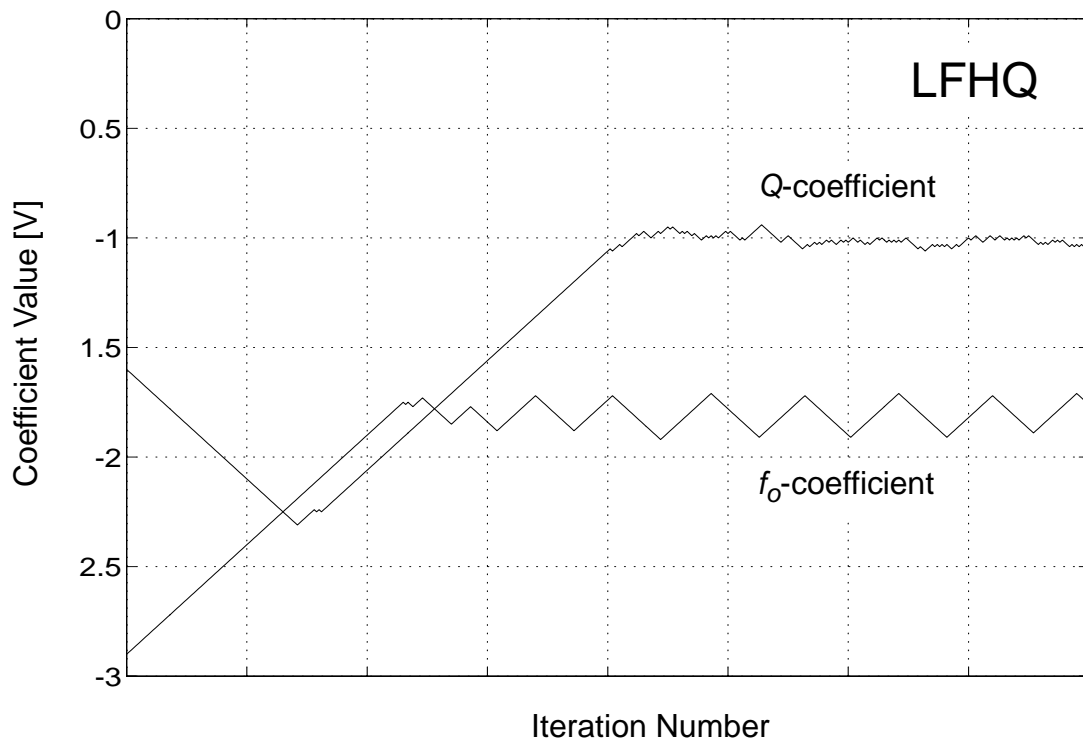


Figure 5.24: Experimental coefficient trajectory for the various test cases.

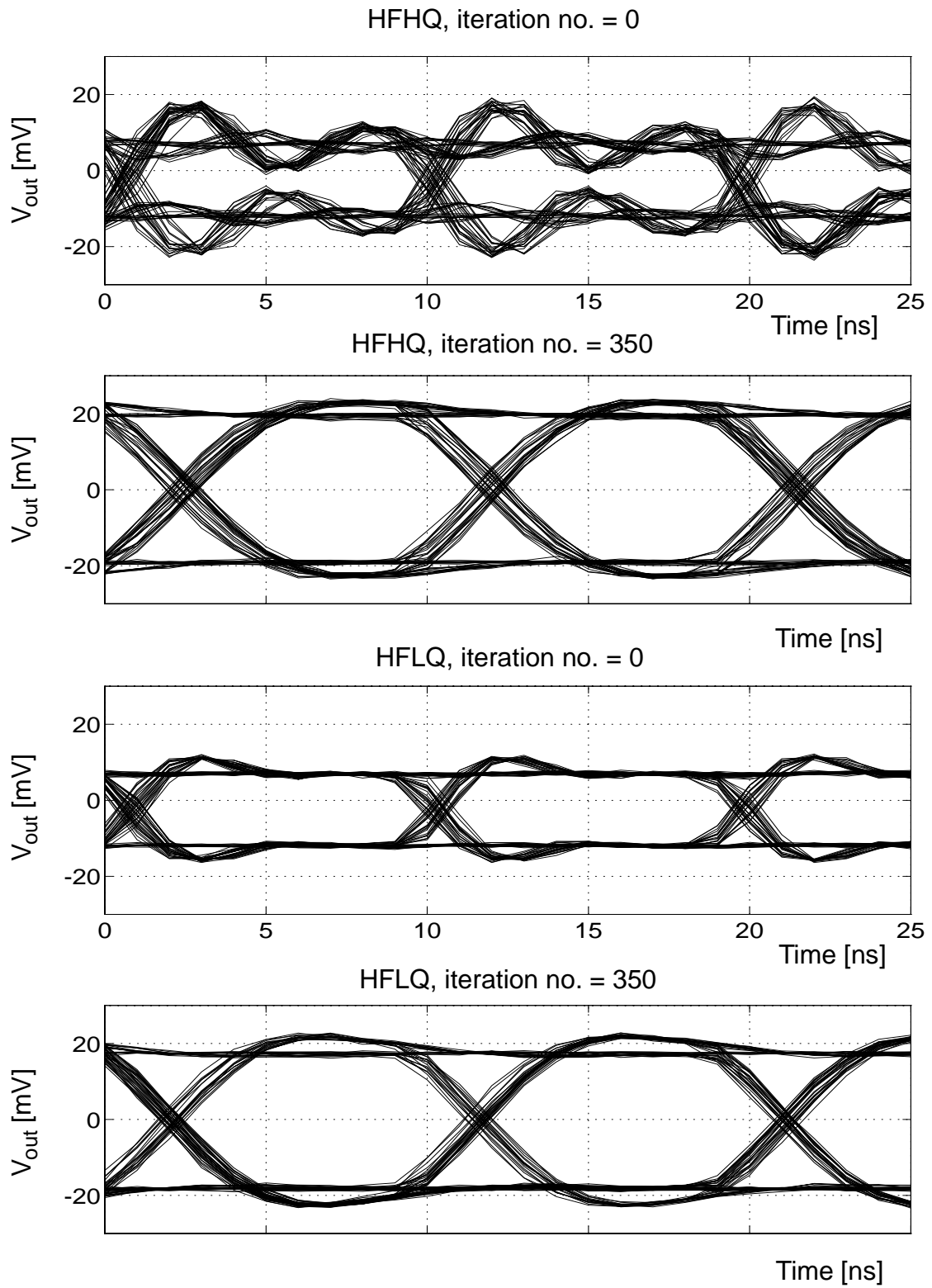


Figure 5.25: Filter initial and final output eye diagrams for various test cases.

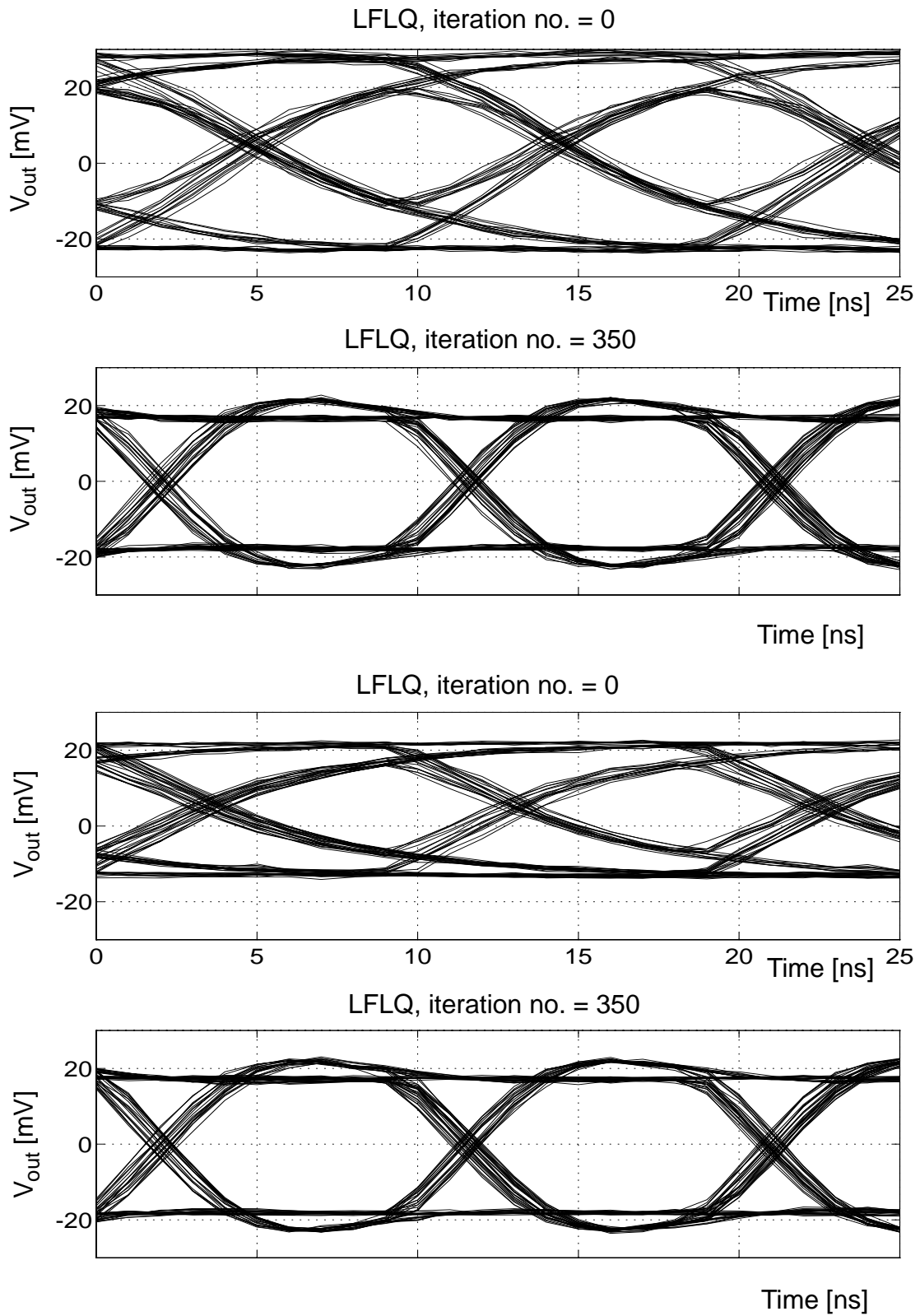


Figure 5.26: Filter initial and final output eye diagrams for various test cases.

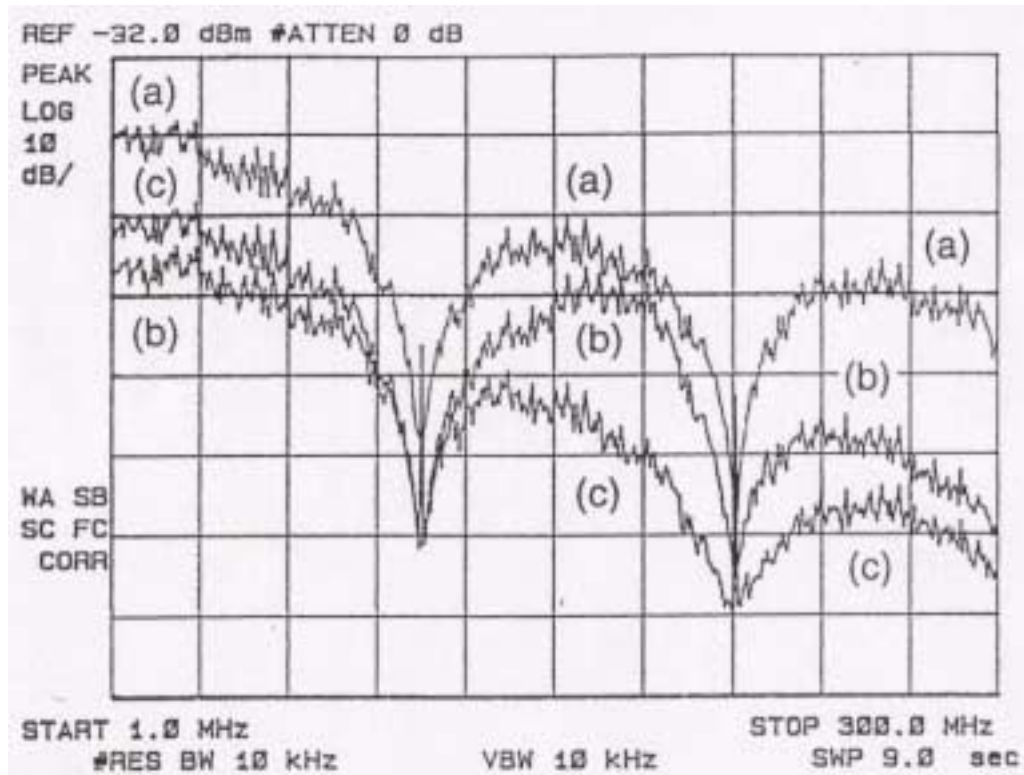


Figure 5.27: Filter input (a), initial (b) and final (c) spectra for the HFHQ case.

5.4 Appendix 5.1: Transconductor Test Structures

In this appendix, experimental results for a second chip submitted are provided. The chip photomicrograph is shown in Figure 5.35. It contains three tunable transconductors. Two transconductors are scaled differently and provide either “2-quadrant” (F-cell and B-cell) or “4-quadrant” (Q-cell) operation. The IC area of a single transconductor is 0.140mm x 0.050mm. For testing purposes, a board was built using discrete components to provide a single-ended to differential converter. This board was reliable only to about 8MHz. It was observed that each half-side of the differential output had a DC offset: -5.4mV on the positive output and 0.1mV on the negative output. (The results given here for the F-cell tests were made under the above condition, while the input offset difference was corrected for the Q-cell tests). The maximum power dissipation of a single transconductor is 10mW.

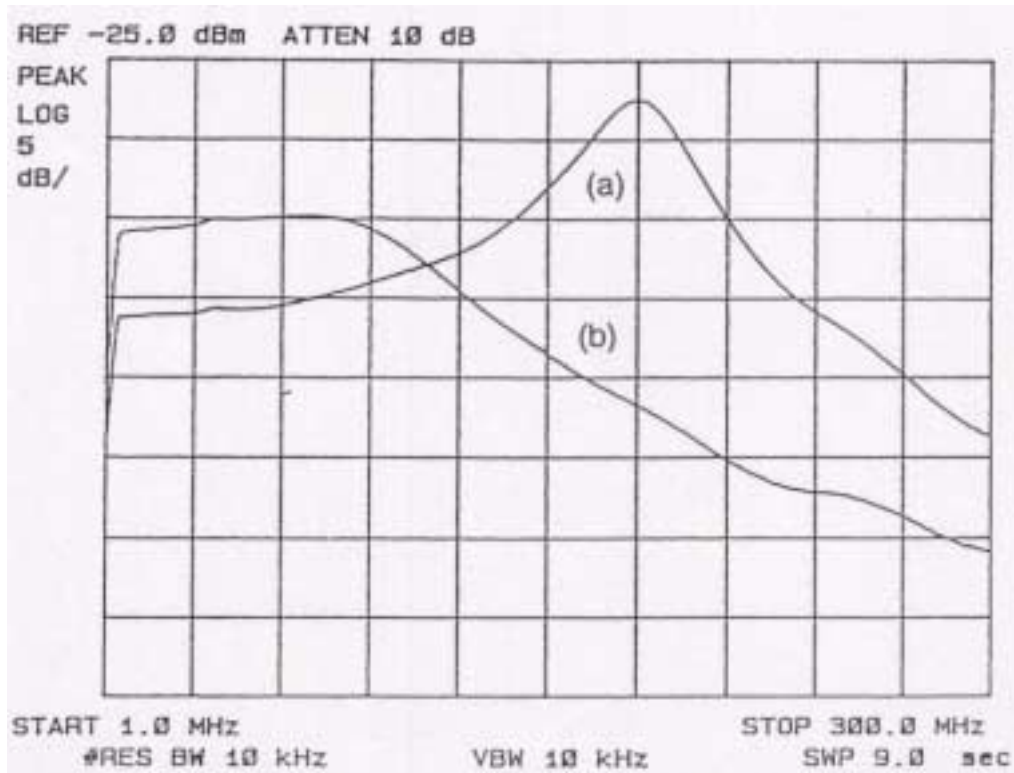


Figure 5.28: Filter initial (a) and final (b) frequency response for the HFHQ case.

It should be mentioned here that to properly characterize the *transconductors*, they would have to be tested open-loop without any loading. Since our transconductors operate up to 600MHz, and given the test equipment available, proper characterization would be difficult without compromising the high-frequency response due to instrument loading and the effect of the test-board. Another approach would be to load the transconductors to the filter frequency of interest, 100MHz, and characterize the resultant open-loop *integrator*. However, this test still requires a well controlled test-board and does not really characterize the actual transconductor. To allow some comparison with simulation, it was decided to load the transconductor with capacitors that dominate all parasitic capacitances and to measure only the low-frequency integrator parameters such as G_m and the DC gain $A_o = G_m R_o$. To obtain the high-frequency performance, it was decided to characterize the biquad filter at low filter Q which would give an indication on integrator linearity and noise performance. As for integrator non-idealities, such as finite DC gain and excess phase, these deviations would

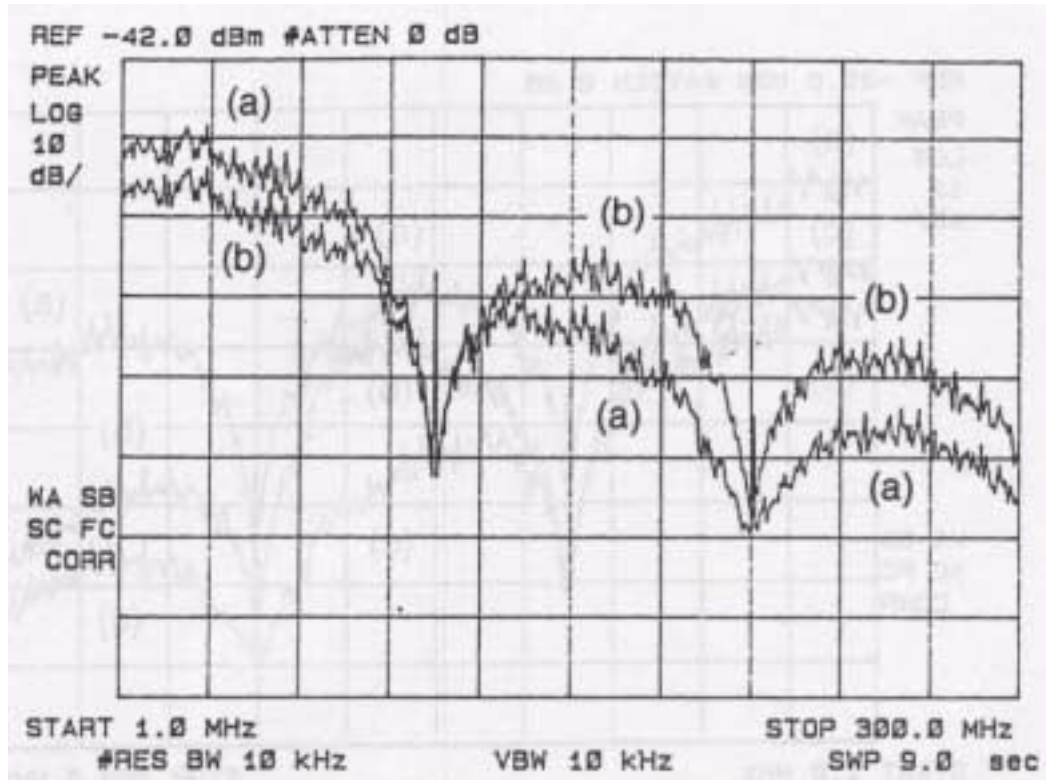


Figure 5.29: Filter initial (a) and final (b) spectra for the HFLQ case.

result in filter pole-frequency and Q deviation. These deviations can more easily be obtained from the filter results given knowledge of the filter transfer-function and the simulated and experimental results. For example, slight integrator phase error, which would be difficult to measure at 100MHz, can be obtained from filter Q error as filter Q deviation is related to integrator phase error magnified by filter Q [Sedra 78]. However, this analysis is beyond the scope of this work. In this section, the results of the tests feasible with the available test equipment will be presented.

5.4.1 F-cell Tests:

For the F-cell transconductor, the output offset on the negative output terminal was 67mV and on the positive output terminal it was -102mV. These offset values occurred since the transconductor was tested open loop. Hence, the amplification of the input offset which appeared at the output. Simulation results for the same input offset predicts 53mV on the

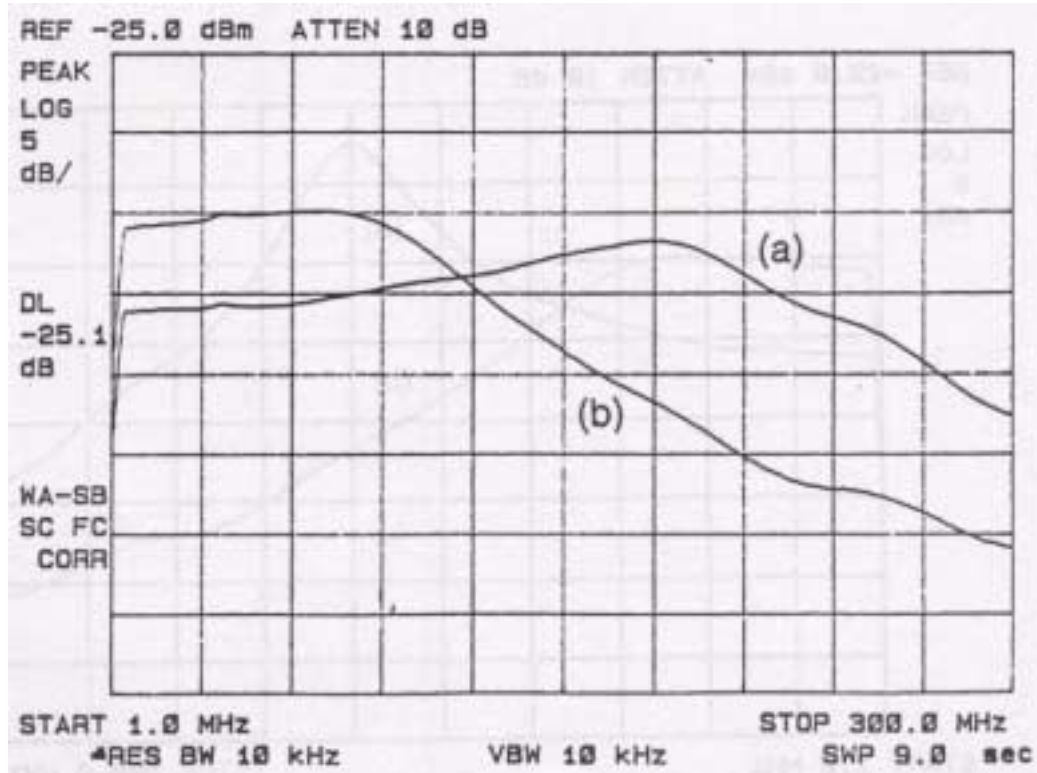


Figure 5.30: Filter initial (a) and final (b) frequency response for the HFLQ case. positive terminal and -41mV on the negative terminal. From the experimental results, we note an output common-mode offset of -17.5mV and a differential output offset of -170mV. The DC gain of the transconductor was found to be about 15.5V/V (23.8dB), from which it appears that 5.5mV of input offset comes from input pair mismatch while the other 5.5mV of input offset comes from board mismatch. The simulated DC gain is 17V/V (24.7dB).

The measured capacitance of the board per transconductor single-ended output was 13pF. Together with a 1pF integration capacitance on chip resulted in a load capacitance of 14pF whose value was used for comparison with simulation. This capacitive load implies a differential capacitance of 7pF. The frequency responses at the maximum setting for G_m (solid curves) compared with simulation (dotted curves) are shown in Figure 5.36. The plot shows the magnitude response for each half-circuit output of the transconductor (hence the four curves) together with the half-circuit input level which was -42.2dBm (2.45mV). It can be noted that the experimental maximum unity gain bandwidth for the above load is about

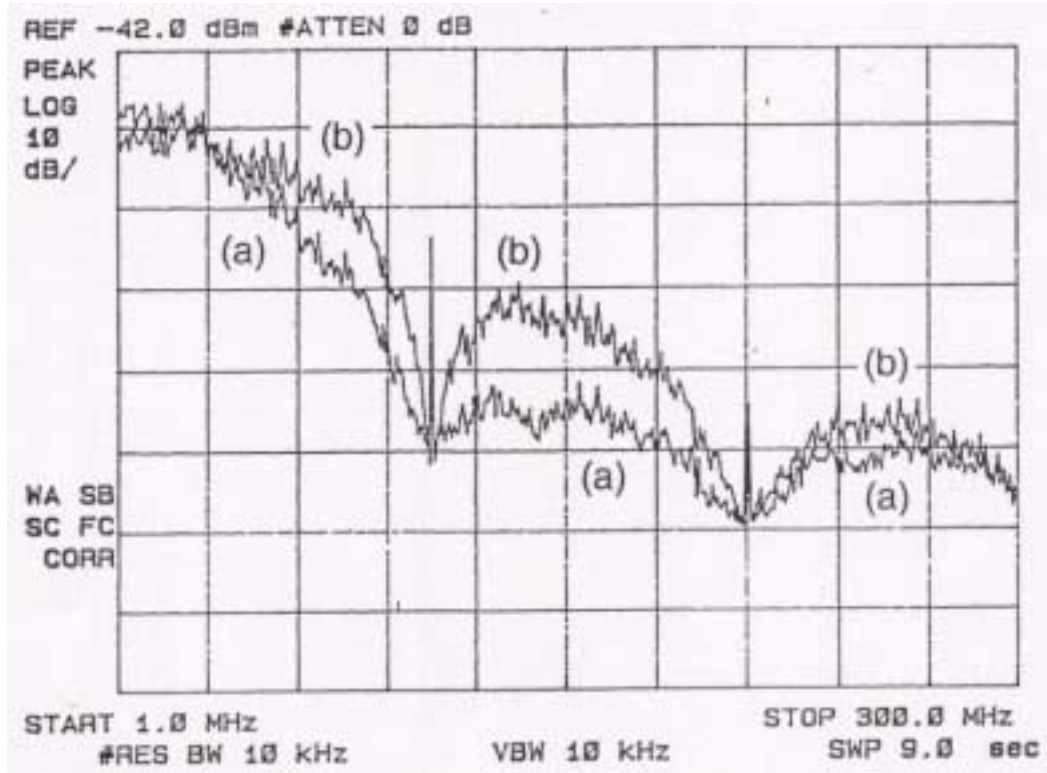


Figure 5.31: Filter initial (a) and final (b) spectra for the LFHQ case.

4.5MHz and the simulated value is 4.2MHz. The roll-off is not exactly -20dB/dec but higher and is partially attributed to board loss. The experimental value for G_m is then calculated to be about $200\mu\text{ A/V}$ and the simulated value is $185\mu\text{ A/V}$.

To compare the experimental results with simulations in more detail, consider the ideal case where the high-frequency effects of the test-board and the parasitic poles are ignored. For this case, the transconductor transfer-function can be given by

$$\frac{v_o(s)}{v_{in}(s)} = \frac{G_m R_o}{1 + sCR_o} \quad (\text{A5-1})$$

where R_o is the transconductor output resistance and is related to device output resistance $1/g_o$. Thus, the DC gain is given by $G_m R_o$ and the high-frequency roll-off is proportional to G_m/C as indicated in Figure 5.36. From this Figure, we observe that the experimental roll-off curve indicates that G_m is larger than its simulated value implying the process is slightly faster than expected via simulation. However, the experimental DC gain is lower

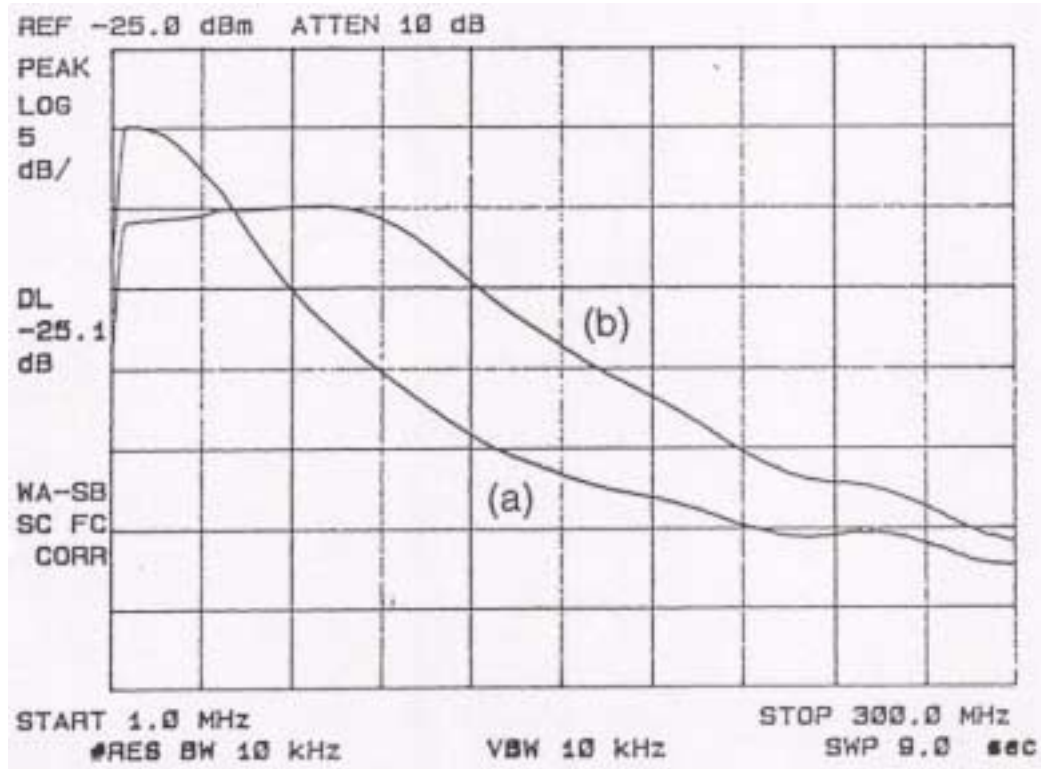


Figure 5.32: Filter initial (a) and final (b) frequency response for the LFHQ case. than the simulated value implying that device output resistance is lower than its simulated value. Therefore, one can assume that the fabricated channel length was shorter than predicted which would explain the observed higher speed and lower device output resistance. These observations were evident from Figure 5.14 as discussed in Section 5.2.2.

To determine the tuning range, the transconductor was tested at its maximum speed (7pF differential load) and the tuning control voltage was swept from -1.3V to 1.75V. The results are shown in Figure 5.37 which depicts G_m as function of the control voltage relative to the maximum G_m attainable. The simulated data is also plotted in the figure showing agreement between theoretical (Figure 4.6), simulation, and experimental results. The magnitude responses for the transconductor as function of the control voltage is depicted in Figure 5.38.

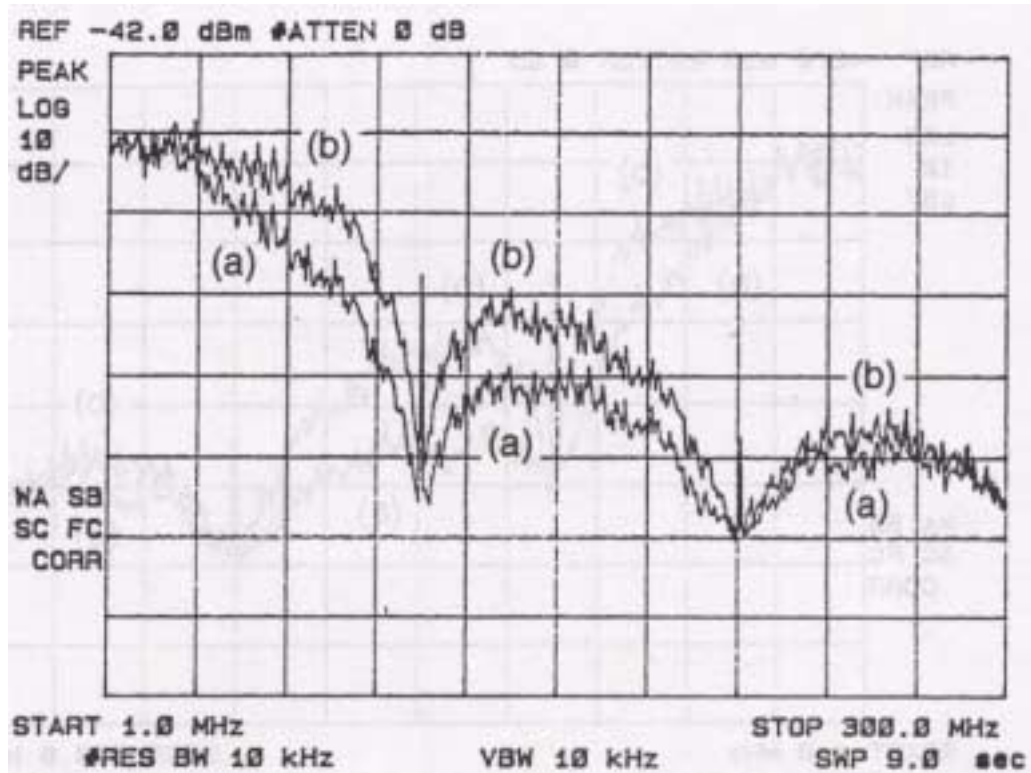


Figure 5.33: Filter initial (a) and final (b) spectra for the LFLQ case.

5.4.2 Q-cell Tests:

The “4-quadrant” transconductor was also tested. The input offset problem of the board was corrected and both transconductor inputs were resting at -1.6mV DC. A problem was noted in that the output offset at the positive terminal was 0.2V and -0.1V at the negative terminal. The frequency responses at the maximum setting for G_m (solid curves) compared with simulation (dotted curves) are shown in Figure 5.39. The plot shows the magnitude response for each half-output of the transconductor together with the half-side input level. For the simulation, the effects of the test board were modelled. From these results, we note that the experimental maximum DC gain of 17.2dB compares with a simulated maximum DC gain of 18.6dB. The experimental value for the maximum G_m can be extracted from the load conditions (7pF) and the maximum unity-gain frequency of 2MHz to be $88\mu\text{ A/V}$ whereas the

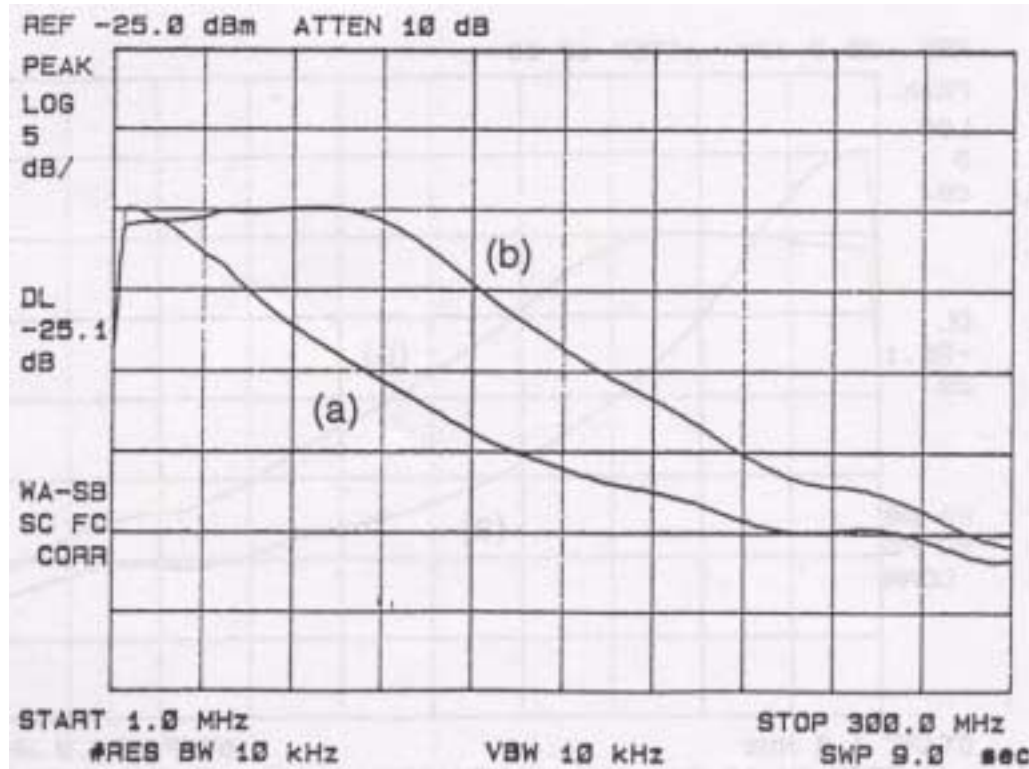


Figure 5.34: Filter initial (a) and final (b) frequency response for the LFLQ case. simulated value is $80\mu\text{ A/V}$. Thus, once again we note that the experimental G_m is larger than simulated and that the experimental device output resistance is lower than simulated.

To determine the tuning range, the transconductor was tested at its maximum speed (7pF differential load) and the tuning control voltage was swept from -2.05V to 1.75V. The results are shown in Figure 5.40 which depicts G_m as function of the control voltage relative to the maximum G_m attainable. The simulated data is also plotted in the Figure. The magnitude responses for the transconductor as function of the control voltage is depicted in Figures 5.41 and 5.42.

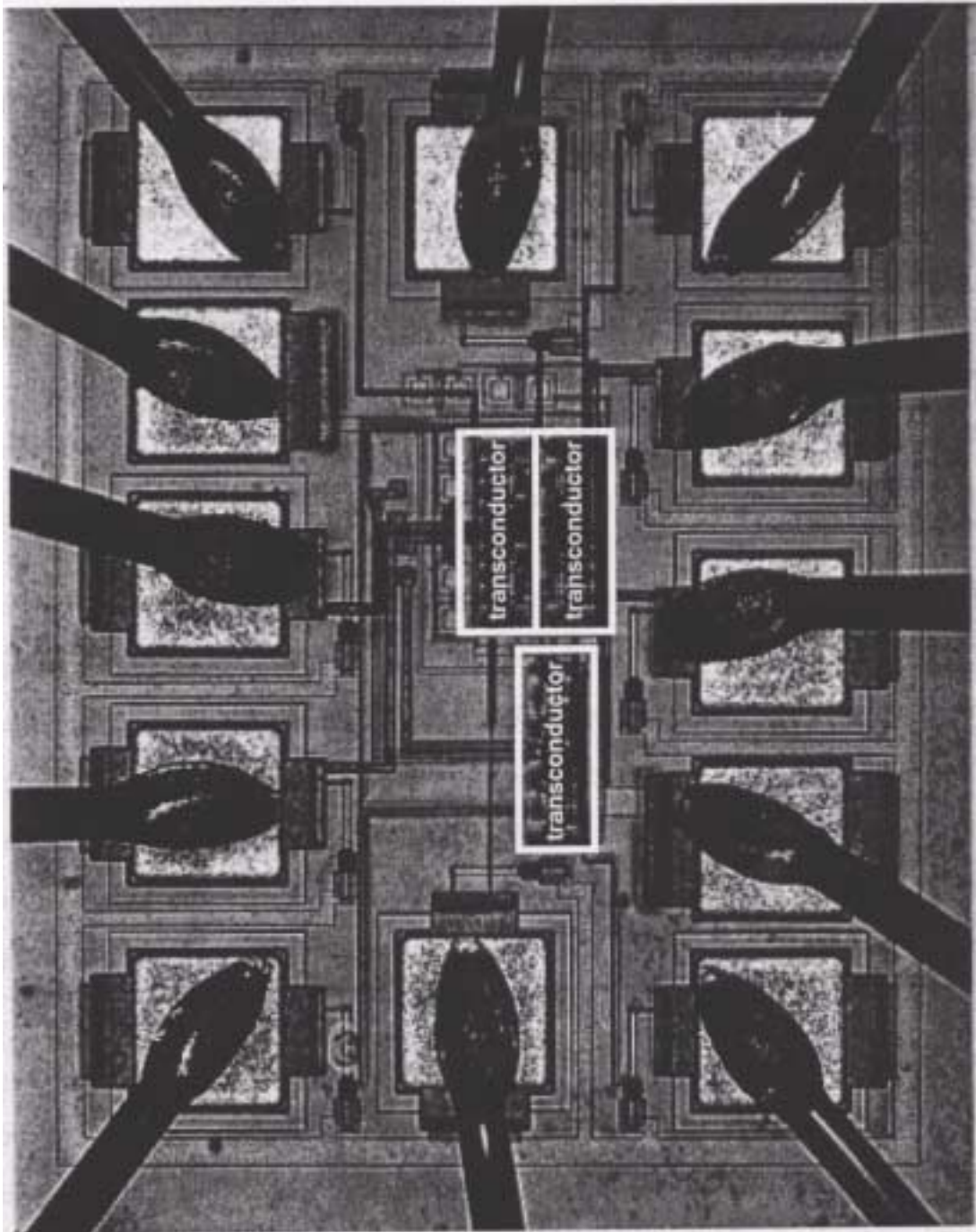


Figure 5.35: Test transconductors chip photomicrograph.

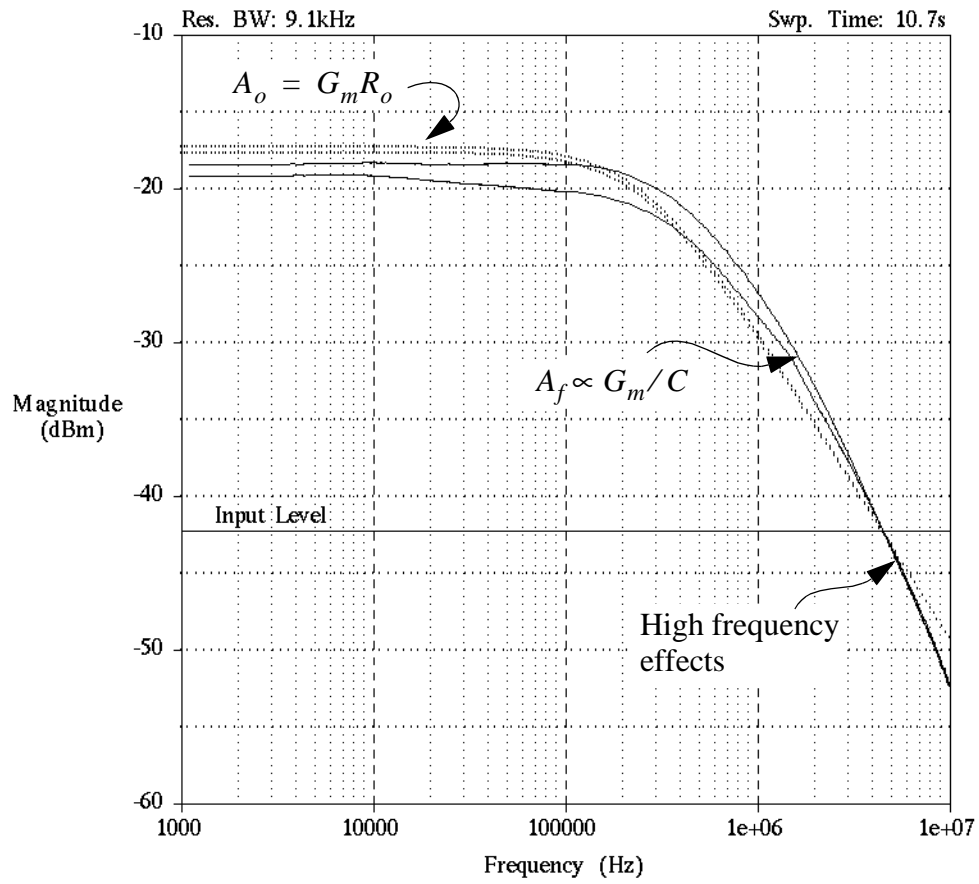


Figure 5.36: Experimental (solid curves) and simulated (dotted curves) magnitude responses for the transconductor outputs at maximum G_m and a 7pF differential load.

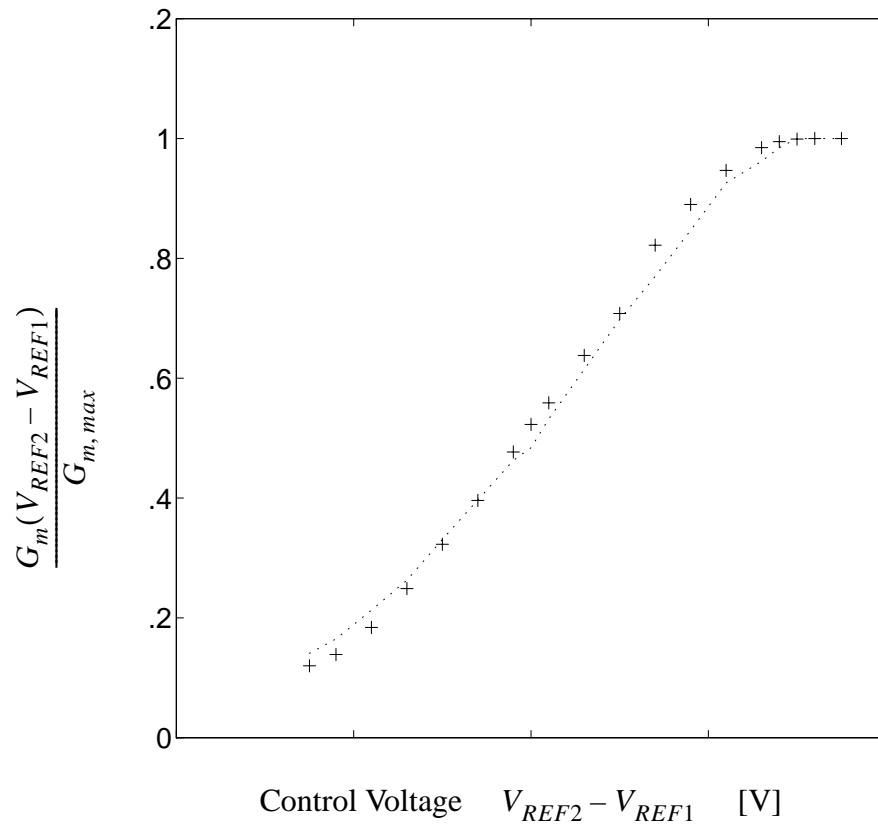


Figure 5.37: Experimental (plus symbols) and simulated (dotted curve) F-cell transconductance characteristics as function of the DC control voltages.

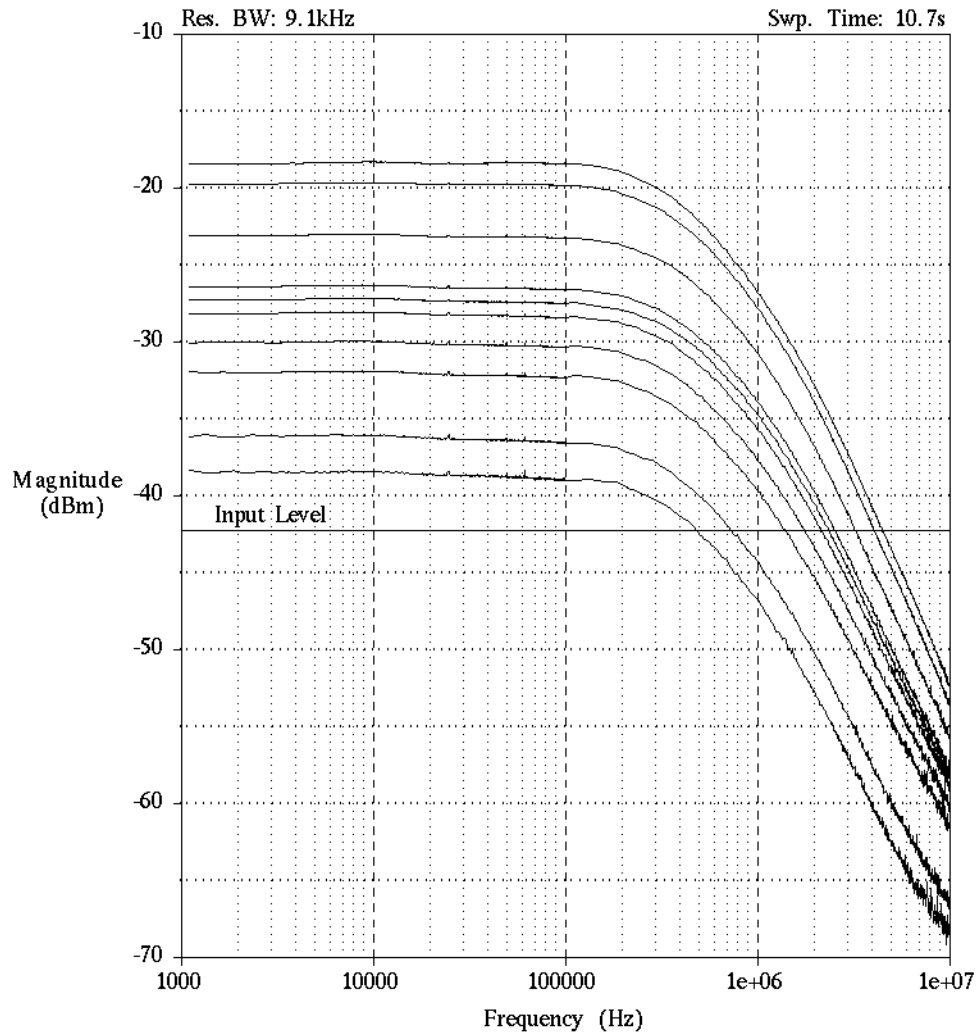


Figure 5.38: Experimental results for the F-cell transconductor magnitude response as function of the tuning voltage (top to bottom): 1.75V, 0.9V, 0.5V, 0.1V, 0.0V, -0.1V, -0.3V, -0.5V, -0.9V and -1.1V.

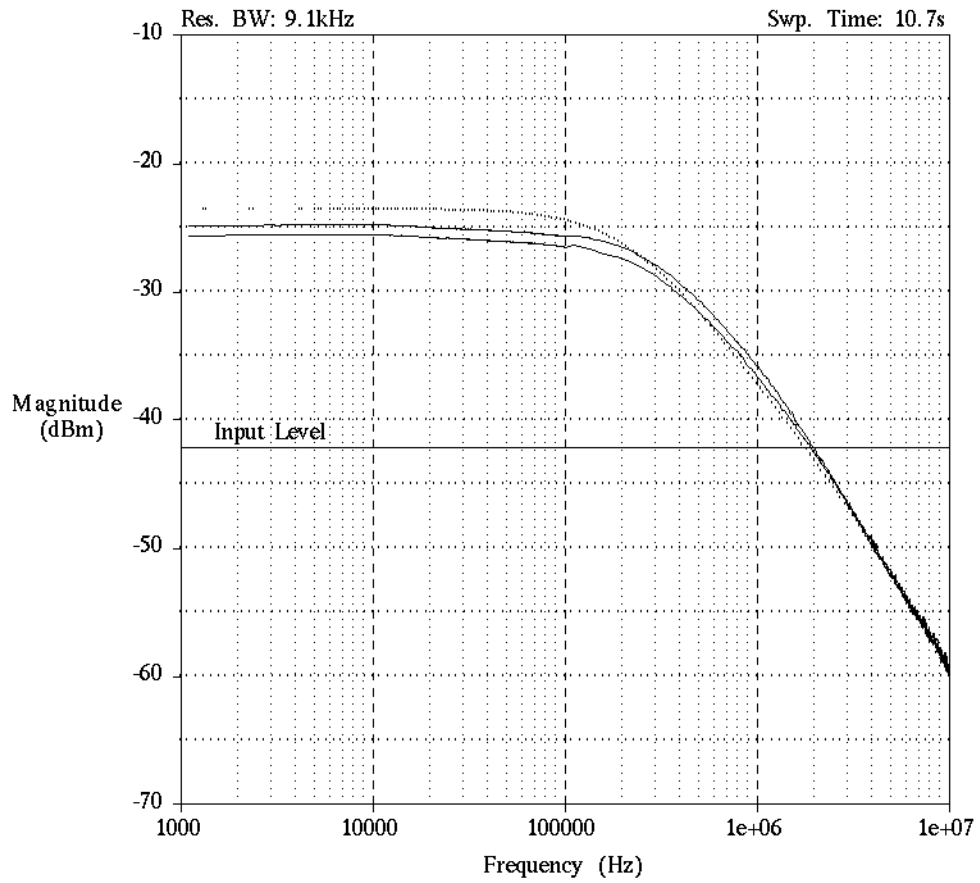


Figure 5.39: Experimental (solid curves) and simulated (dotted curves) magnitude response for the Q-cell transconductor at maximum G_m setting and 7pF load. The simulated half-circuit outputs were similar, hence the appearance of a single simulated curve.

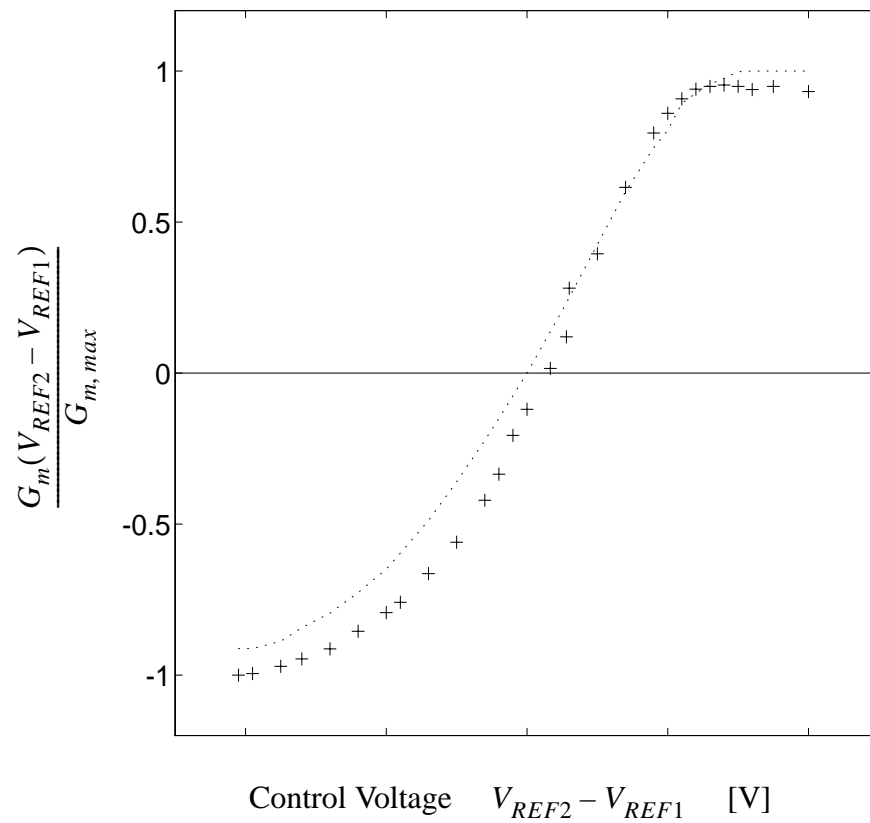


Figure 5.40: Experimental (plus symbols) and simulated (dotted curve) Q-cell transconductance characteristics as function of DC control voltage.

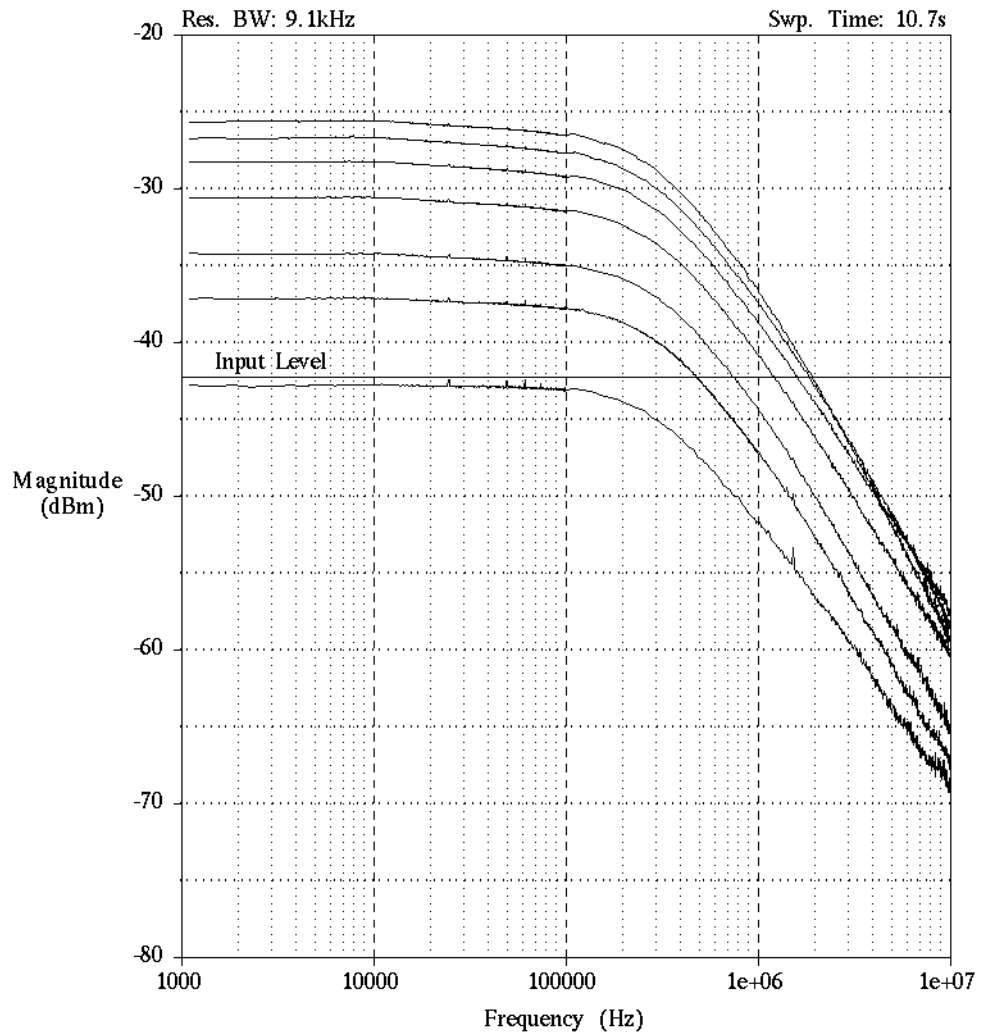


Figure 5.41: Experimental results for the Q-cell transconductor magnitude response as function of the tuning voltages (top to bottom): 1.75V, 1.1V, 0.9V, 0.7V, 0.5V, 0.3V, 0.28V.

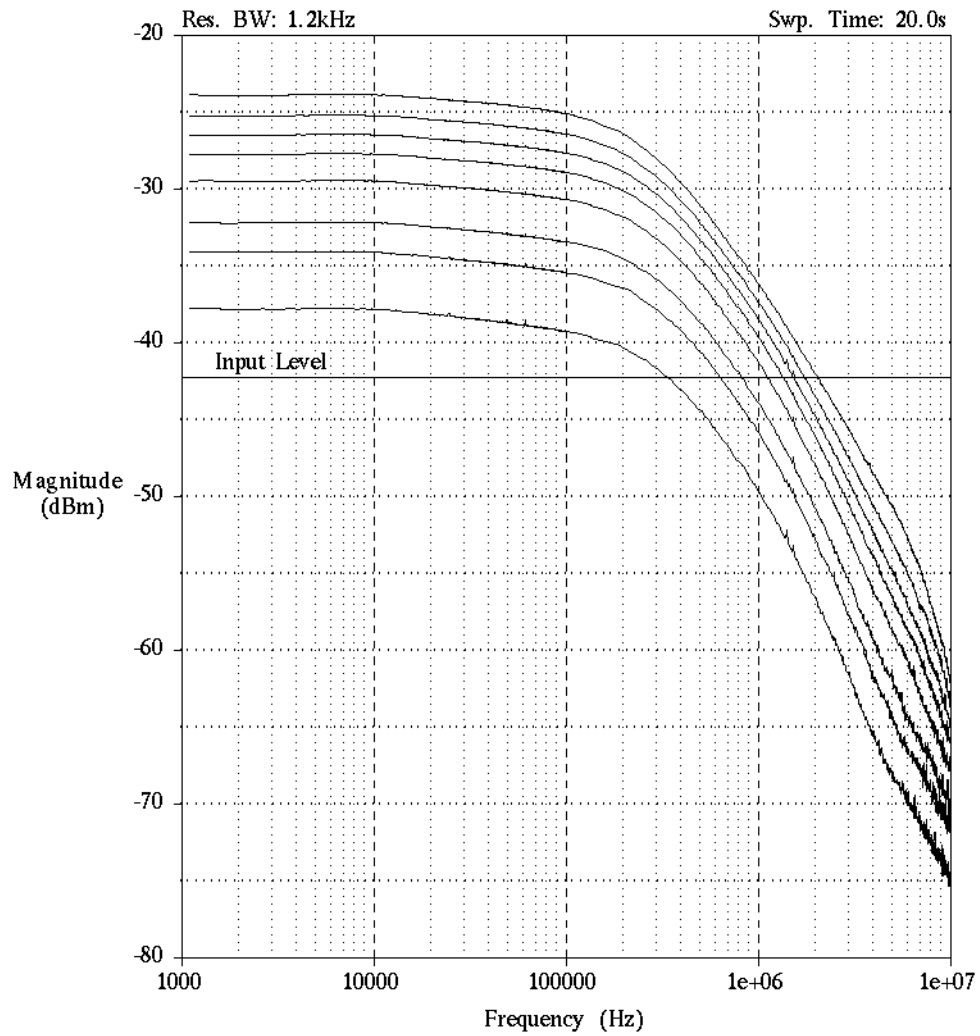


Figure 5.42: Experimental results for the Q-cell transconductor magnitude response as function of the tuning voltages (top to bottom): -1.95V, -1.2V, -1.0V, -0.9V, -0.7V, -0.5V, -0.3V, -0.2V, and -0.1V.

CHAPTER 6

DC Offset Effects

It is well known that DC offsets degrade the performance of analog adaptive filters. In this chapter, the effects of DC offsets on four variations of the stochastic gradient algorithm are analyzed. Assuming a Gaussian probability distribution for the input signal and error signal, the output mean squared error (MSE) performance in the presence of DC offsets is evaluated for each of the algorithms. The theoretical work is compared with computer simulations and the results, together with convergence properties of each of the algorithms and their respective hardware requirements, are used in selecting the most appropriate algorithm. Although a Gaussian input distribution is assumed, it may reasonably be inferred that the critical results obtained should also hold for other input distributions.

6.1 Introduction

The essence of an adaptive filter is the implementation of the algorithm that controls the coefficients of the programmable filter. Among the many possible algorithms, the least-mean-square (LMS) algorithm has been widely used due to its implementation simplicity. For even greater implementation simplicity, the sign-data, the sign-error, and the sign-sign LMS (SD-LMS, SE-LMS, and SS-LMS, respectively) algorithms have been proposed and investigated extensively in the technical literature [Treichler 87], [Johns 91], [Sari 82], [Sethares 88], [Classen 81], Dasgupta 86], [Duttweiler 82]. The findings of these

works show that all variants of the LMS algorithm converge only if the input signal is sufficiently exciting [Sethares 88] and that even when sufficiency conditions are met, the SS-LMS and the SD-LMS algorithms can diverge due to misalignment of the gradient signals [Sethares 88], [Classen 81], [Dasgupta 86]. That is, unlike the LMS or the SE-LMS algorithms which force the coefficient updates vector to move along a line in the coefficient space parallel to its gradient signal vector, the SD-LMS and the SS-LMS algorithms force the coefficient updates vector to move along a line in the coefficient space misaligned from its gradient signal vector and parallel to the *sign* of its gradient signal vector. Consequently, whereas in the former case the coefficient updates will, on average, move in a direction of “steepest descent” of the squared error surface, in the SD-LMS and the SS-LMS algorithm case the misalignment can lead to coefficient divergence and may also cause the coefficient updates to “climb” the error surface. In addition, it has been shown that while both the LMS and the SD-LMS algorithms will ideally force the filter coefficients to their optimal locations as the error signal is reduced to zero (i.e. zero MSE), the SE-LMS and the SS-LMS algorithms will experience finite minimum MSE. This finite MSE results from the fact that slicing the error signal prevents the *effective* error signal from reducing to zero. In fact, it has been claimed [Rohrs 86] that as the coefficients reach their optimal values and the error signal is reduced, the *effective* error signal increases, potentially causing the coefficients to jerk. Thus, it is tempting to use the LMS algorithm and dispense with the SS-LMS algorithm. However, when considering algorithm implementation, the LMS algorithm is the most complex while the SS-LMS algorithm is the simplest. The SD-LMS algorithm, being simpler than the LMS algorithm, requires N slicers and N trivial multipliers which is more complex than the SE-LMS algorithm requiring 1 slicer and N trivial multipliers where N is the number of coefficients being adapted. Thus, the choice of which algorithm to use is difficult.

When implementing *analog* adaptive filters, not only are algorithm architecture complexity and algorithm convergence important issues, but also DC offsets. Although some

publications have treated DC offsets in adaptive filters [Johns 91], [Enomoto 83], [Menzi 93], [Tzeng 90], [Quieting 92], few results are available on the effects of all sources of DC offsets on all four variations of the LMS algorithm. Since algorithm misalignment and algorithm convergence rate are covered extensively in the technical literature [Treichler 87], [Johns 91], [Sari 82], [Sethares 88], [Classen 81], [Dasgupta 86], [Duttweiler 82], this chapter focuses on the performance of the four variants of the LMS algorithm from a DC offset point of view. The results presented here should assist the designer in overcoming the perplexing issue of selecting the appropriate hardware implementation for the coefficient update algorithm.

To keep the analysis simple and tractable, discrete-time systems are used and, as a working example, an adaptive linear combiner whose input is zero-mean Gaussian noise will be assumed. Although this input forms a special case, intuitive comments will be given for arbitrary input statistics. The accuracy of the discrete-time system in analyzing the effects of DC offsets in a continuous-time linear combiner might be questionable. However, the relations obtained here are based on taking the mean and variance of the product of filter gradient and error signals. Since a continuous-time linear combiner can be well approximated by a discrete-time system running at a very high oversampling rate, the relations for such a system would not depart severely from those discussed herein as the sampling rate is increased. In addition, we would like to point out that often continuous-time techniques are used in implementing the signal path (i.e. the filter) while sampled-time techniques are used in realizing the adaptation algorithm. Thus, the analysis performed here, which focuses on DC offsets in the algorithm circuitry, is sufficient to provide detail as to the comparative performance of each of the candidate algorithms. Finally, while some approximations are made in deriving analytical expressions, simulation results are presented showing close agreement which is sufficient since typically only rough estimates of DC offset values are known.

6.2 Problem Formulation

For an adaptive linear combiner, as shown in Figure 6.1, the output at time index k is given

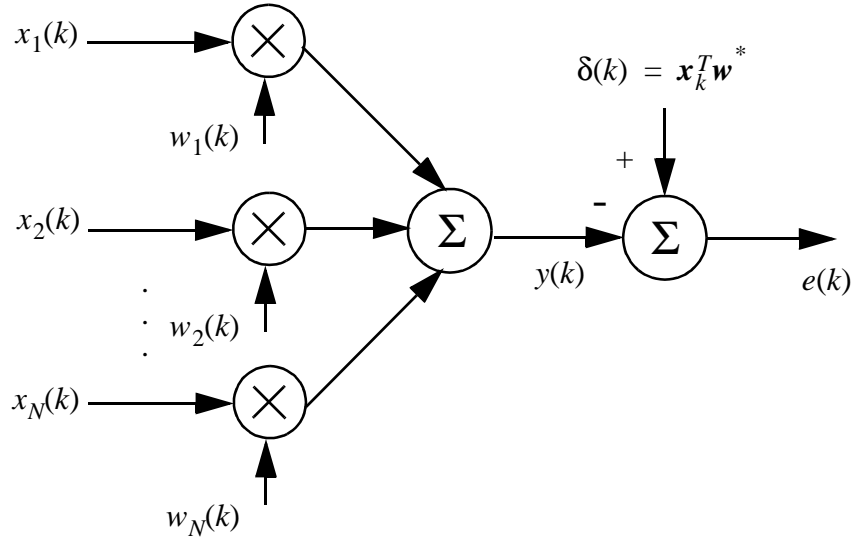


Figure 6.1: A general adaptive linear combiner.

by

$$y(k) = \sum_{i=1}^N w_i(k)x_i(k) \quad (6.1)$$

where $w_i(k)$ is the i^{th} coefficient value and $x_i(k)$ is the i^{th} gradient signal as well as the i^{th} input signal. In vector notation, (6.1) can be represented as

$$\mathbf{y}_k = \mathbf{x}_k^T \mathbf{w}_k \quad (6.2)$$

The error signal is

$$\begin{aligned} e(k) &= \delta(k) - y(k) \\ &= \mathbf{x}_k^T [\mathbf{w}^* - \mathbf{w}_k] \end{aligned} \quad (6.3)$$

where $\delta(k)$ is the desired response and \mathbf{w}^* is a vector of optimal coefficients. Defining \mathbf{c}_k to be the present coefficient estimate, or mathematically

$$\mathbf{c}_k = \mathbf{w}^* - \mathbf{w}_k \quad (6.4)$$

then (6.3) can be re-written as

$$e(k) = \mathbf{x}_k^T \mathbf{c}_k \quad (6.5)$$

Assuming the input is zero-mean, we have

$$E[\mathbf{x}_k] = \mathbf{0} \quad (6.6)$$

where $E[\bullet]$ represents the expectation operator. To allow a solution of otherwise very complicated expressions, it is also assumed that the gradient signals and the filter coefficient estimates are statistically independent, thus

$$E[\mathbf{x}_k^T \mathbf{c}_k] = E[\mathbf{x}_k^T] E[\mathbf{c}_k] \quad (6.7)$$

This assumption is not uncommon [Classen 81] and is acknowledged to be an approximation since coefficient computation depends on the gradient signals. However, for slow adaptation the coefficient estimates are weakly dependent on the gradient signals and the assumption invoked by (6.7) provides satisfactory steady-state results as will be noted from the simulation results herein. Equations (6.5-6.7) also yield

$$E[e(k)] = 0 \quad (6.8)$$

We also define $\sigma_x^2 \equiv E[x_i^2(k)]$ and $\sigma_e^2 \equiv E[e^2(k)]$ to be the mean-squared value of the gradient and the error signals, respectively. The quantity σ_e^2 represents the filter output MSE and is the performance measure to be evaluated for each of the four algorithms.

The LMS algorithm used to update the filter coefficients is given below with modeled DC offsets inserted at appropriate locations

$$\mathbf{w}_{k+1} = \mathbf{w}_k + 2\mu((\mathbf{x}_k + \mathbf{m}_x)(e(k) + m_e) + \mathbf{m}) \quad (6.9)$$

where

$$\mathbf{x} = [m_{x1} \ m_{x2} \ \dots \ m_{xN}]^T \quad (6.10)$$

is a vector representing the unwanted DC offsets on each of the gradient signals, m_e represents the unwanted DC offset on the error signal, μ is a small step size that governs the rate of adaptation, and \mathbf{m} is a vector representing the unwanted equivalent DC offsets at the input of the accumulator (integrator) and at the output of the multiplier where

$$= \begin{bmatrix} m_1 & m_2 & \dots & m_N \end{bmatrix}^T \quad (6.11)$$

The equivalent block diagram representing (6.9) for the i^{th} coefficient is depicted in Figure 6.2 for clarity. Upon substituting (6.4) into (6.9), one obtains

$$\text{LMS} \quad \mathbf{c}_{k+1} = \mathbf{c}_k - 2\mu((\mathbf{x}_k + \mathbf{m}_x)(e(k) + m_e) + \mathbf{m}) \quad (6.12)$$

The equivalent expression of (6.12) for the three other variants of the LMS algorithm SD-LMS, SE-LMS, and SS-LMS, respectively are:

$$\text{SD-LMS} \quad \mathbf{c}_{k+1} = \mathbf{c}_k - 2\mu(\text{sgn}[\mathbf{x}_k + \mathbf{m}_x](e(k) + m_e) + \mathbf{m}) \quad (6.13)$$

$$\text{SE-LMS} \quad \mathbf{c}_{k+1} = \mathbf{c}_k - 2\mu((\mathbf{x}_k + \mathbf{m}_x) \text{sgn}[e(k) + m_e] + \mathbf{m}) \quad (6.14)$$

$$\text{SS-LMS} \quad \mathbf{c}_{k+1} = \mathbf{c}_k - 2\mu(\text{sgn}[\mathbf{x}_k + \mathbf{m}_x] \text{sgn}[e(k) + m_e] + \mathbf{m}) \quad (6.15)$$

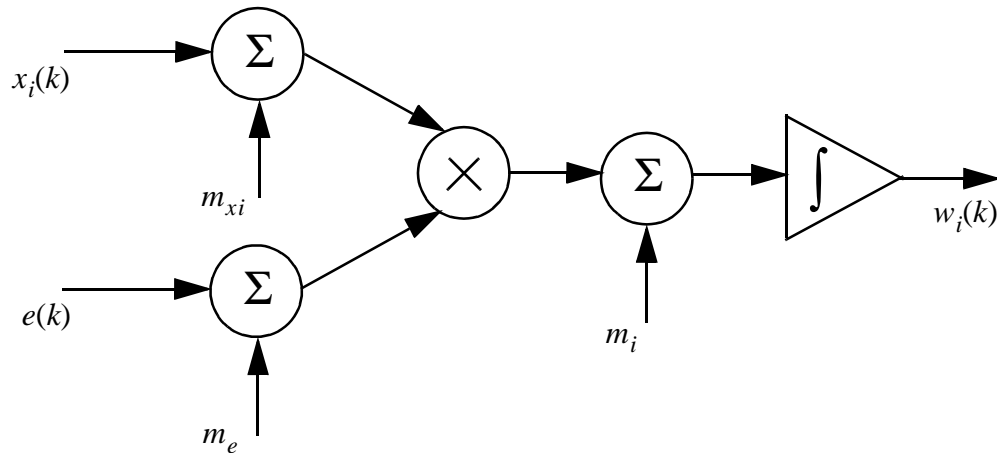


Figure 6.2: Details of the LMS update circuitry showing DC offset sources.

6.3 The LMS Algorithm

Taking the expectation of both sides of (6.12) we obtain

$$E[\mathbf{c}_{k+1}] = E[\mathbf{c}_k] - 2\mu E[(\mathbf{x}_k + \mathbf{m}_x)(e(k) + m_e) + \mathbf{m}] \quad (6.16)$$

At steady-state (i.e. as $k \rightarrow \infty$), we have $E[\mathbf{c}_{k+1}] = E[\mathbf{c}_k]$. Using this fact together with (6.6) and (6.8), (6.16) simplifies to

$$E[\mathbf{x}_k e(k)] = -(\mathbf{m} + m_e \mathbf{m}_x) \quad (6.17)$$

Substituting (6.5) and (6.7) into (6.17) results in

$$E[\mathbf{x}_k \mathbf{x}_k^T] E[\mathbf{c}_k] = -(\mathbf{m} + m_e \mathbf{m}_x) \quad (6.18)$$

Letting

$$\mathbf{R} \equiv E[\mathbf{x}_k \mathbf{x}_k^T] \quad (6.19)$$

and dropping the time index k (for mathematical convenience), at steady-state the following relations hold:

$$E[\mathbf{c}] = -\mathbf{R}^{-1}(\mathbf{m} + m_e \mathbf{m}_x) \quad (6.20)$$

$$E[\mathbf{c}^T] = -(\mathbf{m} + m_e \mathbf{m}_x)^T \mathbf{R}^{-T} \quad (6.21)$$

To solve for the residual MSE due to offsets, consider once again the expression in (6.12).

Taking the mean-squared value of both sides yields

$$\begin{aligned} E[\mathbf{c}_{k+1}^T \mathbf{c}_{k+1}] &= E[\mathbf{c}_k^T \mathbf{c}_k] - 4\mu E[\mathbf{c}_k^T ((\mathbf{x}_k + \mathbf{m}_x)(e(k) + m_e) + \mathbf{m})] \\ &\quad + 4\mu^2 E[((\mathbf{x}_k + \mathbf{m}_x)(e(k) + m_e) + \mathbf{m})^T ((\mathbf{x}_k + \mathbf{m}_x)(e(k) + m_e) + \mathbf{m})] \end{aligned} \quad (6.22)$$

Noting that at steady-state $E[\mathbf{c}_{k+1}^T \mathbf{c}_{k+1}] = E[\mathbf{c}_k^T \mathbf{c}_k]$, substituting (6.6) and (6.8) into (6.22) and dropping the time index as before, yields

$$\begin{aligned} 0 &= \mu E[(\mathbf{x}^T \mathbf{x} + 2\mathbf{x}^T \mathbf{m}_x + \mathbf{m}_x^T \mathbf{m}_x)(e^2 + 2em_e + m_e^2)] - \mu \mathbf{m}^T \mathbf{m} \\ &\quad - E[\mathbf{c}^T](\mathbf{m} + m_e \mathbf{m}_x) - E[e^2] - E[\mathbf{c}^T e] \mathbf{m}_x \end{aligned} \quad (6.23)$$

The solution of (6.23) for arbitrary μ is tedious and results in a value for the MSE that has a weak dependence on μ . Thus, assuming $\mu \rightarrow 0$, making use of (6.21) and noting from (6.5)

and (6.7) that for slow adaptation the last term in (6.23) is proportional to $E[\mathbf{x}_k]$ and is therefore negligible, (6.23) can be solved for the excess MSE at steady-state

$$\sigma_e^2 \approx (\mathbf{m} + m_e \mathbf{m}_x)^T \mathbf{R}^{-T} (\mathbf{m} + m_e \mathbf{m}_x). \quad (6.24)$$

The result in (6.24) shows that the excess MSE is inversely proportional to the power of the input signal through the \mathbf{R}^{-T} term; lower input signal powers, for fixed offset levels, produce higher excess MSE. The excess MSE is also directly sensitive to all offset sources. In analog implementations, the DC offset at the output of the multiplier and offsets at the input to the integrator, \mathbf{m} , would typically dominate (relative to m_e or \mathbf{m}_x). Clearly, to minimize the excess MSE, nulling of m_e or \mathbf{m}_x and \mathbf{m} would be required and may be plausible in certain applications using AC-coupling and offset cancelled integrators, respectively. On observing (6.24), it is also interesting to note that it is possible to minimize the excess MSE by adjusting the DC offsets to cancel one another rather than nulling m_e or \mathbf{m}_x and \mathbf{m} . However, satisfying this equality implies adaptively tracking a vector of integrator input offset and multiplier output offset, \mathbf{m} , to a vector of gradient signal bias, \mathbf{m}_x , scaled by $-m_e$. This approach is not a trivial one when considering hardware implementation. Finally, notice that the excess MSE due to this offset cannot be compensated by reducing μ .

6.4 The Sign-Data LMS Algorithm

Taking the expectation of both sides of (6.13), using (6.5-6.8) and simplifying as before yields

$$-\mathbf{m} = E[\text{sgn}[\mathbf{x} + \mathbf{m}_x] \mathbf{x}^T] E[\mathbf{c}] + E[\text{sgn}[\mathbf{x} + \mathbf{m}_x]] m_e \quad (6.25)$$

For a zero-mean Gaussian noise input with variance $\sigma_x^2 = R_{ii}$, it can be shown that (see Appendix 6.1):

$$E[\text{sgn}[\mathbf{x} + \mathbf{m}_x]] = \left[\text{erf} \left[\frac{m_{x1}}{\sqrt{2\sigma_x^2}} \right] \quad \text{erf} \left[\frac{m_{x2}}{\sqrt{2\sigma_x^2}} \right] \quad \dots \quad \text{erf} \left[\frac{m_{xN}}{\sqrt{2\sigma_x^2}} \right] \right]^T \equiv \mathbf{k}_{\mathbf{m}_x} \quad (6.26)$$

Using Price's Theorem [Price 58], it can be shown that (see Appendix 6.2):

$$E[\text{sgn}[\mathbf{x} + \mathbf{m}_x]\mathbf{x}^T] = \frac{1}{\sigma_x} \sqrt{\frac{2}{\pi}} \begin{bmatrix} e^{-m_{x1}^2/2\sigma_x^2} [R_{11} \ R_{12} \ \dots \ R_{1N}] \\ e^{-m_{x2}^2/2\sigma_x^2} [R_{21} \ R_{22} \ \dots \ R_{2N}] \\ \dots \\ e^{-m_{xN}^2/2\sigma_x^2} [R_{N1} \ R_{N2} \ \dots \ R_{NN}] \end{bmatrix} \equiv \mathbf{R}_{MX} \quad (6.27)$$

where $R_{ij} = E[x_i x_j]$ as before. Substituting (6.26) and (6.27) into (6.25) yields

$$E[\mathbf{c}^T] = -(\mathbf{m} + m_e \mathbf{k}_{\mathbf{m}\mathbf{x}})^T \mathbf{R}_{MX}^{-T} \quad (6.28)$$

Taking the mean-squared value of both sides of (6.13) and simplifying as done previously, one obtains

$$0 = \mu(N\sigma_e^2 + Nm_e^2 - \mathbf{m}^T \mathbf{m}) - E[\mathbf{c}^T](\mathbf{m} + m_e \mathbf{k}_{\mathbf{m}\mathbf{x}}) - E[\mathbf{c}^T \text{sgn}[\mathbf{x} + \mathbf{m}_x] e] \quad (6.29)$$

Using (6.7) and (6.27), the last term in (6.29) simplifies to

$$E[\mathbf{c}^T \text{sgn}[\mathbf{x} + \mathbf{m}_x] e] = E[\mathbf{c}^T \mathbf{R}_{MX} \mathbf{c}] \quad (6.30)$$

An analytical expression for the excess MSE requires the evaluation of (6.30). Consider the case for a Gaussian white noise; (6.30) reduces to

$$E[\mathbf{c}^T \text{sgn}[\mathbf{x} + \mathbf{m}_x] e] = \sqrt{\frac{2}{\pi}} \sigma_x \sum_{i=1}^N \hat{\sigma}_{c_i}^2 e^{-m_{xi}^2/2\sigma_x^2} \quad (6.31)$$

where $\hat{\sigma}_{c_i}^2 = \sigma_{c_i}^2 + E[c_i]^2$ and $\sigma_{c_i}^2$ represents the variance of c_i . Making use of the assumption in (6.7), one can derive using (6.5)

$$\sigma_e^2 = \sigma_x^2 \sum_{i=1}^N \hat{\sigma}_{c_i}^2 \quad (6.32)$$

Assuming the mean-squared value of all the coefficient estimates equal the same value, or mathematically, $\hat{\sigma}_{c_i}^2 \approx \hat{\sigma}_{c_j}^2 \equiv \hat{\sigma}_c^2$, the following expression, making use of (6.28-6.32) is obtained for the excess MSE as a function of the interfering offsets

$$\sigma_e^2 \approx \frac{\mu(Nm_e^2 - \mathbf{m}^T \mathbf{m}) + (\mathbf{m} + m_e \mathbf{k}_{\mathbf{m}\mathbf{x}})^T \mathbf{R}_{\mathbf{M}\mathbf{X}}^{-T} (\mathbf{m} + m_e \mathbf{k}_{\mathbf{m}\mathbf{x}})}{\frac{1}{N\sigma_x} \sqrt{\frac{2}{\pi}} \sum^N e^{-m_{xi}^2/2\sigma_x^2} - \mu N} \quad (6.33)$$

The expression in (6.33) assumes the case where the input signals $x_i(k)$ are Gaussian white, however, it is not clear if the same expression can be used for non-white inputs. Fortunately, (6.33) does give reasonable estimates for general inputs in the practical case where the square of the offsets on the gradient signals, m_{xi}^2 , are sufficiently small compared to the variance of the gradient signals, σ_x^2 . In this case, we can then approximate the exponential terms in (6.27) by unity and (6.30) can be reduced to

$$E[\mathbf{c}^T \text{sgn}[\mathbf{x} + \mathbf{m}_{\mathbf{x}}] e] = \frac{1}{\sigma_x} \sqrt{\frac{2}{\pi}} \sigma_e^2 \quad (6.34)$$

Upon substituting (6.28) and (6.34) into (6.29) an expression for the excess MSE is obtained that is given by (6.33) with m_{xi} in the denominator set to zero.

The expression in (6.33) shows that the performance of the SD-LMS algorithm is similar to the LMS algorithm from a DC offset point of view; the dominant offset terms appear explicitly in the numerator of (6.33). The difference here is that the excess MSE is a weak function of the input signal power¹ for small μ . This effect is a consequence of the slicing operation which results in the loss of information regarding the amplitude of the signal and would be similarly manifested for arbitrary input distributions.

6.5 The Sign-Error LMS Algorithm

Taking the expectation of both sides of (6.14) and simplifying as before yields

$$-\mathbf{m} = E[\mathbf{x} \text{sgn}[e + m_e]] + E[\text{sgn}[e + m_e]] \mathbf{m}_{\mathbf{x}} \quad (6.35)$$

1. Signal power, σ_x^2 , appears both in the numerator (via $\mathbf{R}_{\mathbf{M}\mathbf{X}}^{-T}$) and denominator of (6.33).

Assuming $e(k)$ has a Gaussian distribution at steady-state², using the results in Appendices 6-1 and 6-2 as well as (6.7), it can be shown from (6.35) that

$$E[\mathbf{c}^T] = -\sigma_e \sqrt{\frac{\pi}{2}} e^{m_e^2/2\sigma_e^2} \left(\mathbf{m} + \operatorname{erf} \left[\frac{m_e}{\sqrt{2}\sigma_e} \right] \mathbf{m}_x \right)^T \mathbf{R}^{-T} \quad (6.36)$$

Taking the mean-squared value of both sides of (6.14), simplifying as before and collecting terms, the following expression results

$$0 = \mu(N\sigma_x^2 + \mathbf{m}_x^T \mathbf{m}_x - \mathbf{m}^T \mathbf{m}) - \sigma_e \sqrt{\frac{2}{\pi}} e^{-m_e^2/2\sigma_e^2} - E[\mathbf{c}^T] \mathbf{m} - E[\mathbf{c}^T \operatorname{sgn}[e + m_e]] \mathbf{m}_x \quad (6.37)$$

Defining $\tilde{\mathbf{c}}^T$ to be a vector representing the AC component of the filter coefficient estimates, or mathematically, $\tilde{\mathbf{c}}^T \equiv \mathbf{c}^T - E[\mathbf{c}^T]$, and substituting into the last term in (6.37) yields

$$0 = \mu(N\sigma_x^2 + \mathbf{m}_x^T \mathbf{m}_x - \mathbf{m}^T \mathbf{m}) - \sigma_e \sqrt{\frac{2}{\pi}} e^{-m_e^2/2\sigma_e^2} - E[\mathbf{c}^T] \left(\mathbf{m} + \operatorname{erf} \left[\frac{m_e}{\sqrt{2}\sigma_e} \right] \mathbf{m}_x \right) - E[\tilde{\mathbf{c}}^T \operatorname{sgn}[e + m_e]] \mathbf{m}_x \quad (6.38)$$

The last term in (6.38) measures the correlation of $\tilde{\mathbf{c}}^T$ with $\operatorname{sgn}[e + m_e]$ and is approximated to zero since for slow adaptation the AC component of the filter coefficient estimates, $\tilde{\mathbf{c}}^T$, is small. Thus, (6.38) together with (6.36) provide a non-linear function in σ_e^2 that describes the MSE as function of μ and the interfering offsets.

While (6.38) is the main result for this section, it is also of interest to solve (6.36) for two limiting cases. To find the limiting value of the MSE for the case of small μ , set $\mu = 0$ and solve (6.38) to obtain

2. This assumption becomes better for small μ for which the AC component of the coefficients is small, and thus, the distribution of the error signal follows that of the input.

$$\lim_{\mu \rightarrow 0} \sigma_e^2 = \frac{-m_e^2}{\ln \left[\frac{\pi}{2} \left(\mathbf{m} + \operatorname{erf} \left[\frac{m_e}{\sqrt{2\sigma_e^2}} \right] \mathbf{m}_x \right)^T \mathbf{R}^{-T} \left(\mathbf{m} + \operatorname{erf} \left[\frac{m_e}{\sqrt{2\sigma_e^2}} \right] \mathbf{m}_x \right) \right]} \quad (6.39)$$

For the case of non-zero μ and $m_e = 0$, it can be shown from (6.36) and (6.38) that the excess MSE is

$$\sigma_e^2|_{m_e=0} = \frac{\pi}{2} \mu^2 \left(\frac{N\sigma_x^2 + \mathbf{m}_x^T \mathbf{m}_x - \mathbf{m}^T \mathbf{m}}{1 - \frac{\pi}{2} \mathbf{m}^T \mathbf{R}^{-T} \mathbf{m}} \right)^2 \quad (6.40)$$

Comparing (6.39) with the excess MSE for the LMS algorithm (6.24), observe that minimizing (6.39) implies the minimization of m_e or \mathbf{m} , while the minimization of (6.24) implies the minimization of the dominant offset term \mathbf{m} . Thus, in analog implementations, where the offsets represented by \mathbf{m} typically dominate (relative to m_e or \mathbf{m}_x), much better MSE performance in the presence of DC offsets can be achieved using the SE-LMS algorithm. This result can be seen from another perspective by taking the limiting values of ± 1 for the $\operatorname{erf}[\bullet]$ terms in (6.39) and keeping only the dominant offset terms in (6.24) to obtain the following ratio

$$\frac{\sigma_{e,LMS}^2}{\sigma_{e,SE-LMS}^2} \propto \frac{(\mathbf{m}^T \mathbf{R}^{-T} \mathbf{m}) \ln \left[\frac{\pi}{2} (\mathbf{m} \pm \mathbf{m}_x)^T \mathbf{R}^{-T} (\mathbf{m} \pm \mathbf{m}_x) \right]}{-m_e^2} \quad (6.41)$$

This ratio typically exceeds unity for practical offset levels including the case where the offset terms represented by m_e and \mathbf{m} are of the same size, owing to the natural logarithm operator. Similar reasoning can be applied to the SD-LMS algorithm. The minimization of the offset term m_e is not difficult as it entails the minimization of the input offset of a comparator³. This compensation can be achieved by using a clocked comparator or the

3. AC-coupling $e(t)$ to eliminate signal offset can be feasibly done offset-free using passive IC components for most high-speed applications.

technique in [Shoval 92] or [Yu 94]. Compensation of the dominant offset term, m , is feasible in integrated form, but its practical limiting value would be higher than that obtained by compensating m_e .

In the limiting case of $m_e = 0$, notice that in (6.40) the MSE is shaped by μ , and therefore, achieves better MSE performance for small μ than (6.24) or (6.33). However, observe from (6.40) that in the absence of DC offsets⁴ the SE-LMS algorithm, unlike the LMS or the SD-LMS algorithm, will sustain a finite excess MSE that depends on μ . This characteristic is a consequence of slicing the error signal which prevents the effective error signal from going to zero at steady-state. As well, notice that offset cancellation between offsets can also improve the excess MSE as mentioned for the LMS algorithm.

It is also of interest to note that the degrading effects of DC offsets can be alleviated by passing the error signal through a high gain stage prior to coefficient computation [Johns 91]. As a result, the MSE can be shown to be reduced by a factor proportional to the gain factor. This solution is intuitively simple, but becomes more difficult to achieve in high-frequency applications. It is instructive to point out that the SE-LMS algorithm inherently provides this high gain which, although non-linear, is frequency independent.

Finally, note that unlike the LMS and the SD-LMS algorithms, the effective error signal in (6.14) cannot exceed unity in magnitude. Thus, if on average $|m_i| > |x_i + m_{xi}|$, then c_i will diverge. Intuitively this means that if the signal component, x_i , is small relative to the offset component, $m_i - m_{xi}$, then the parenthesized term in (6.14) will be dominated by the offset component, resulting in the respective coefficient to saturate at its limiting value.

4. Not the case for analog circuits.

6.6 The Sign-Sign LMS Algorithm

Although the circuit implementation of the SS-LMS algorithm is quite simple, the analysis of its performance from an offset point of view is the most complex of the algorithms discussed so far. Thus, various approximations will be used to obtain results which depict the behavior of the excess MSE as a function of the interfering offsets. Simulation results will show that the analytical results obtained by using the approximations satisfactorily predict the behavior of the excess MSE.

Assuming $e(k)$ is Gaussian, taking the expectation of both sides of (6.15), one obtains

$$-\mathbf{m} = E[\text{sgn}[\mathbf{x} + \mathbf{m}_x] \text{sgn}[e + m_e]] \quad (6.42)$$

Making use of the work in [Sari 80] and the results of the previous sections, (6.42) can be approximated to give⁵

$$E[\mathbf{c}^T] \approx -\sqrt{\frac{\pi}{2}} \sigma_e e^{m_e^2/2\sigma_e^2} \mathbf{m}^T \mathbf{R}_{MX}^{-T} \quad (6.43)$$

Taking the mean-squared value of both sides of (6.15), one obtains

$$0 = \mu(N - \mathbf{m}^T \mathbf{m}) - E[\mathbf{c}^T \text{sgn}[\mathbf{x} + \mathbf{m}_x] \text{sgn}[e + m_e]] - E[\mathbf{c}^T] \mathbf{m} \quad (6.44)$$

Using [Sari 80], the procedure in obtaining (6.31-6.33), (6.43) and substituting (6.43) into (6.44) yields

$$0 \approx \mu(N - \mathbf{m}^T \mathbf{m}) - \frac{2\sigma_e}{\pi\sigma_x} e^{-m_e^2/2\sigma_e^2} \frac{1}{N} \sum_{i=1}^N e^{-m_{xi}^2/2\sigma_x^2} + \sqrt{\frac{\pi}{2}} \sigma_e e^{m_e^2/2\sigma_e^2} \mathbf{m}^T \mathbf{R}_{MX}^{-T} \mathbf{m} \quad (6.45)$$

Again, a non-linear function in σ_e^2 describes the MSE as function of μ and the interfering offsets.

5. Although we cannot rigorously derive the result of (6.43), we believe the approximation models the actual result. The validity thereof, can be noted from the previous results and the simulations. The derivation is based on the assumption of Gaussian signalling and repeated use of Price's Theorem.

As in the SE-LMS case, (6.45) can be solved for the limiting case of a small μ to give the excess MSE for the SS-LMS algorithm as

$$\lim_{\mu \rightarrow 0} \sigma_e^2 \approx \frac{-m_e^2}{\ln \left[\left(\frac{\pi}{2} \right)^{3/2} \sigma_x \frac{\mathbf{m}^T \mathbf{R}_{MX}^{-T} \mathbf{m}}{N} \right.} \quad (6.46)$$

$$\left. \frac{1}{N} \sum_{i=1} e^{-m_{xi}^2 / 2\sigma_x^2} \right]$$

With $m_e = 0$, (6.45) can be solved to give the excess MSE as

$$\sigma_e^2 \Big|_{m_e=0} \approx \left(\frac{\pi}{2} \mu \right)^2 \sigma_x^2 \left[\frac{N - \mathbf{m}^T \mathbf{m}}{N} \right. \quad (6.47)$$

$$\left. \frac{1}{N} \sum e^{-m_{xi}^2 / 2\sigma_x^2} - \sigma_x \left(\frac{\pi}{2} \right)^{3/2} \mathbf{m}^T \mathbf{R}_{MX}^{-T} \mathbf{m} \right]^2$$

The results show that the SS-LMS algorithm in the presence of DC offsets has much better excess MSE performance than the LMS algorithm or the SD-LMS algorithm for the same reasons as the SE-LMS algorithm. Notice in (6.46), as noted in (6.33), the predicted MSE is weakly dependent on the input signal power, σ_x^2 . As well, from (6.47) we see that in the absence of DC offsets, the SS-LMS algorithm, like the SE-LMS algorithm, will experience a residual excess MSE that is shaped by μ . Finally, note that if $|m_i| > 1$, it can be inferred from (6.15) that the sign of the parenthesized term will be governed by m_i and the coefficient estimate $c_i(k)$ will drift in a direction governed by this offset and the SS-LMS algorithm will diverge. This behavior is similar to that alluded to for the SE-LMS algorithm.

6.7 Numerical Verification

A 5-tap ($N=5$) linear combiner, as illustrated in Figure 6.3, was investigated to compare the simulated performance of the filter with the analytical predictions. The input, $g(k)$, was a

zero-mean white Gaussian distribution. The first-order lowpass filter was used to vary the input statistics to the linear combiner through the parameter α where

$$U(z) = \frac{1}{1 - \alpha z^{-1}} G(z) \quad (6.48)$$

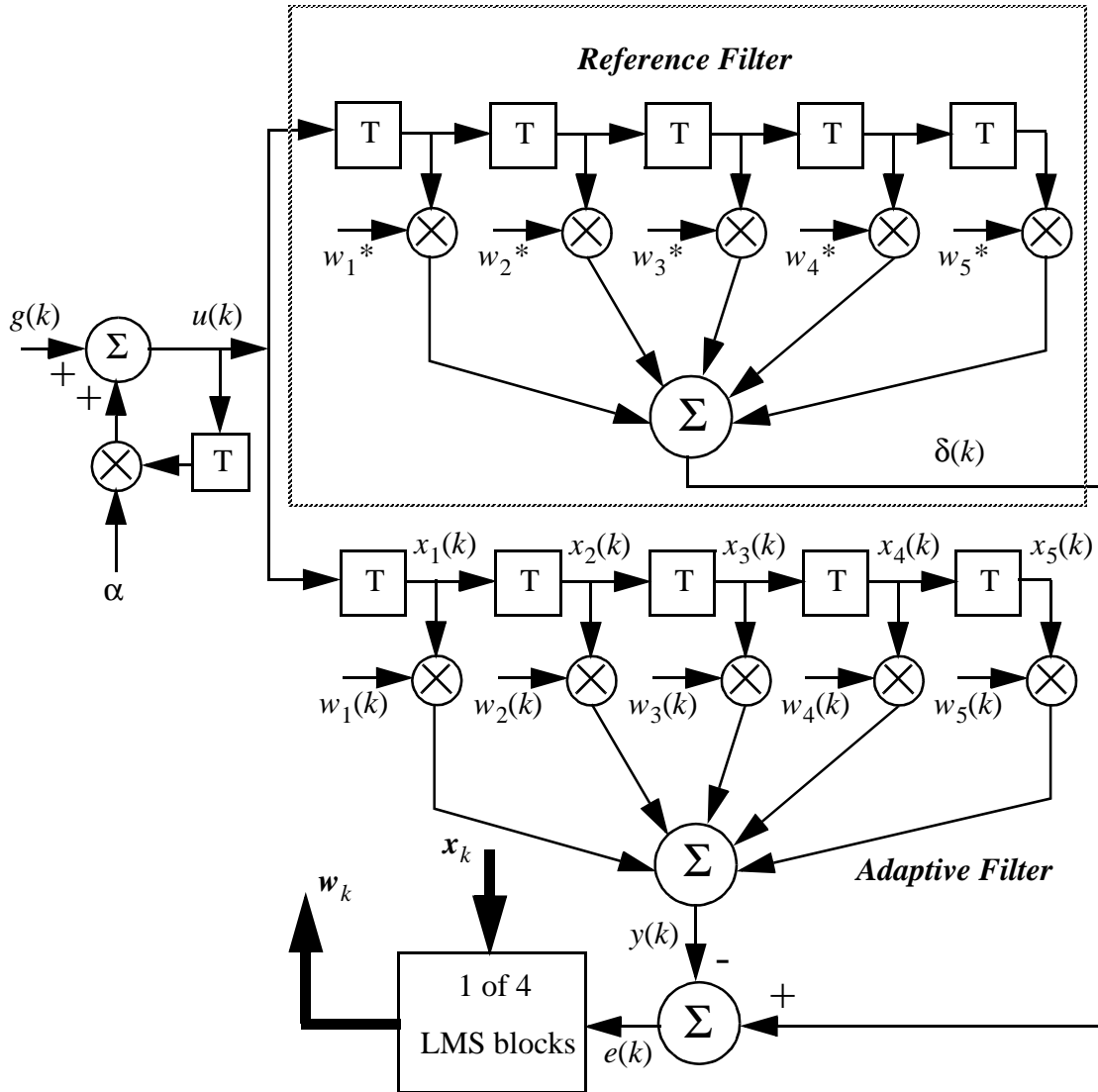


Figure 6.3: The setup used to simulate the adaptive filter.

The results of the simulations and the predicted analytical calculations for various cases are provided in Figures 6.4-6.9. The circles depict the predicted MSE calculated from equations (6.24), (6.33), (6.38), (6.45), and the simulated MSE, at the respective value for μ .

A non-linear equation solver, provided by the software package MATLAB [MATLAB 92], was used to solve (6.38) and (6.45). The solid lines and the dotted lines connect the circles obtained from the analytical expressions and the simulations respectively to exemplify the behavior of the MSE as function of μ . The offsets levels for Figures 6.4-6.7 are:

$$m_e = 0.01$$

$$\mathbf{m}_x^T = [0.02 \ -0.01 \ -0.03 \ -0.005 \ 0.07]$$

$$\mathbf{m}^T = [0.08 \ 0.01 \ -0.05 \ -0.02 \ -0.06]$$

while the offset levels for Figure 6.8 and Figure 6.9 are:

$$m_e = 0.02$$

$$\mathbf{m}_x^T = [0.02 \ 0.0 \ -0.07 \ 0.05 \ -0.008]$$

$$\mathbf{m}^T = [0.03 \ -0.1 \ 0.005 \ -0.08 \ -0.06]$$

The value for α , σ_x^2 and \mathbf{R} for Figures 6.4-6.9 sequentially are:

$$\alpha = 0, \ \sigma_x^2 = 1, \ \mathbf{R} = \begin{bmatrix} 0.9968 & -0.0010 & -0.0005 & -0.0040 & 0.0006 \\ -0.0010 & 0.9968 & -0.0010 & -0.0005 & -0.0040 \\ -0.0005 & -0.0010 & 0.9968 & -0.0010 & -0.0005 \\ -0.0040 & -0.0005 & -0.0010 & 0.9968 & -0.0010 \\ 0.0006 & -0.0040 & -0.0005 & -0.0010 & 0.9968 \end{bmatrix}$$

$$\alpha = 0.4, \ \sigma_x^2 = 1, \ \mathbf{R} = \begin{bmatrix} 1.1849 & 0.4722 & 0.1869 & 0.0711 & 0.0291 \\ 0.4722 & 1.1849 & 0.4722 & 0.1869 & 0.0711 \\ 0.1869 & 0.4722 & 1.1849 & 0.4722 & 0.1869 \\ 0.0711 & 0.1869 & 0.4722 & 1.1849 & 0.4722 \\ 0.0291 & 0.0711 & 0.1869 & 0.4722 & 1.1849 \end{bmatrix}$$

$$\alpha = 0.8, \sigma_x^2 = 1, \mathbf{R} = \begin{bmatrix} 2.7560 & 2.2019 & 1.7592 & 1.4051 & 1.2261 \\ 2.2019 & 2.7560 & 2.2019 & 1.7592 & 1.4051 \\ 1.7592 & 2.2019 & 2.7560 & 2.2019 & 1.7592 \\ 1.4051 & 1.7592 & 2.2019 & 2.7560 & 2.2019 \\ 1.1261 & 1.4051 & 1.7592 & 2.2019 & 2.7560 \end{bmatrix}$$

$$\alpha = 0.4, \sigma_x^2 = 0.25, \mathbf{R} = \begin{bmatrix} 0.2962 & 0.1180 & 0.0467 & 0.0178 & 0.0073 \\ 0.1180 & 0.2962 & 0.1180 & 0.0467 & 0.0178 \\ 0.0467 & 0.1180 & 0.2962 & 0.1180 & 0.0467 \\ 0.0178 & 0.0467 & 0.1180 & 0.2962 & 0.1180 \\ 0.0073 & 0.0178 & 0.0467 & 0.1180 & 0.2962 \end{bmatrix} = \frac{\mathbf{R}(\text{Figure 6.5})}{4}$$

$$\alpha = 0.65, \sigma_x^2 = 1, \mathbf{R} = \begin{bmatrix} 1.7232 & 1.1192 & 0.7240 & 0.4636 & 0.3028 \\ 1.1192 & 1.7232 & 1.1192 & 0.7239 & 0.4636 \\ 0.7240 & 1.1192 & 1.7232 & 1.1192 & 0.7239 \\ 0.4636 & 0.7239 & 1.1192 & 1.7232 & 1.1192 \\ 0.3028 & 0.4636 & 0.7239 & 1.1192 & 1.7232 \end{bmatrix}$$

$$\alpha = 0.9, \sigma_x^2 = 1, \mathbf{R} = \begin{bmatrix} 5.2106 & 4.6857 & 4.2141 & 3.7899 & 3.4121 \\ 4.6857 & 5.2106 & 4.6857 & 4.2141 & 3.7899 \\ 4.2141 & 4.6857 & 5.2106 & 4.6857 & 4.2141 \\ 3.7899 & 4.2141 & 4.6857 & 5.2106 & 4.6857 \\ 3.4121 & 3.7899 & 4.2141 & 4.6857 & 5.2106 \end{bmatrix}$$

The effects of μ and \mathbf{R} on the excess MSE for each of the four algorithms with the same offset levels are depicted in Figures 6.4-6.7. In Figure 6.4, we show the case for a Gaussian white noise input. In Figure 6.5 and Figure 6.6, we show the results for more colored Gaussian inputs as given by the \mathbf{R} matrices above. In Figure 6.7, unlike Figures 6.4-6.6, we show the results when the input power is smaller than unity. Observe that in this case (compared with Figure 6.5) the excess MSE using the LMS algorithm is greatly increased,

while the others are less sensitive to input power as was discussed herein. In Figure 6.8 and 6.9, we show another case for different offset levels. For the case of Figure 6.9, the LMS algorithm showed evidence of divergence for $\mu = 0.01$, hence this point is omitted from the plot. The results of Figures 6.4-6.9 verify the derived analytical expressions given by (6.24), (6.33), (6.38), and (6.45) for arbitrary offset levels and arbitrary \mathbf{R} matrices. Specifically, note that the SE-LMS and the SS-LMS algorithms are shaped by μ and that the limiting cases for $\mu \rightarrow 0$ expressed by (6.39) and (6.46) compare well with simulated data. Observe also from all the results that the SE-LMS and the SS-LMS algorithms achieve much better MSE performance in the presence of DC offsets. In addition, it is evident (Figures 6.6, 6.9) that the analytical results deviate from the simulation results at larger μ and for more colored inputs, as the approximations made become less appropriate for these conditions.

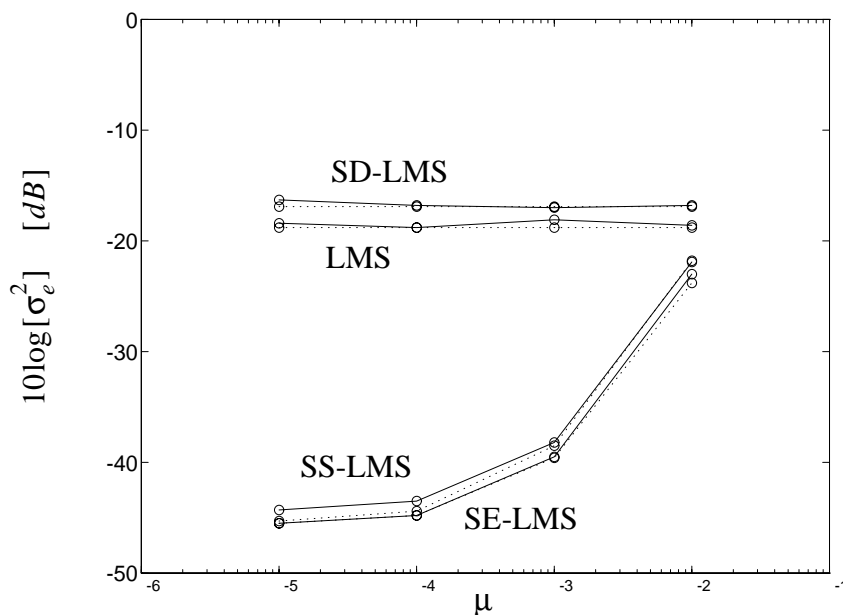


Figure 6.4: Theoretical (dotted lines) and simulated (solid lines) MSE for different offset levels for the four LMS based algorithms; $\alpha = 0$ and $\sigma_x^2 = 1$.

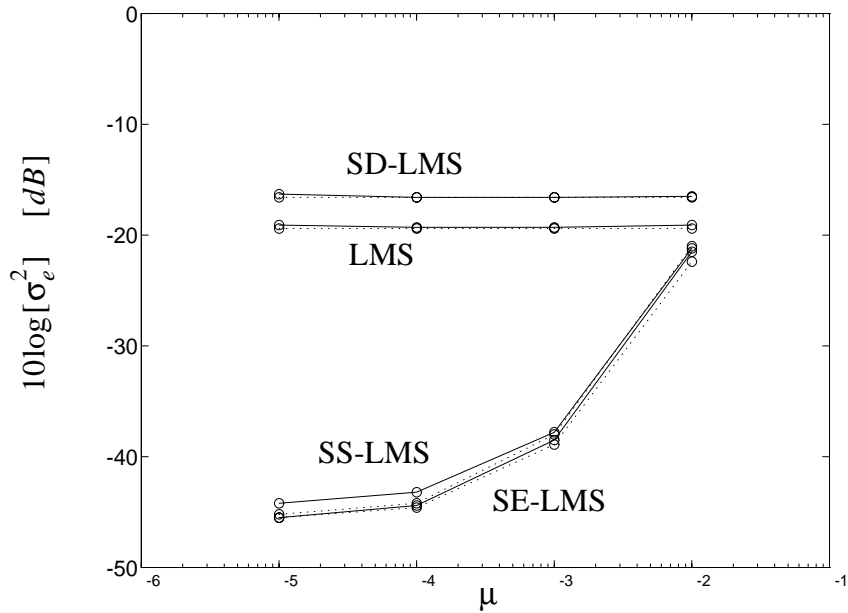


Figure 6.5: Theoretical (dotted lines) and simulated (solid lines) MSE for different offset levels for the four LMS based algorithms; $\alpha = 0.4$ and $\sigma_x^2 = 1$.

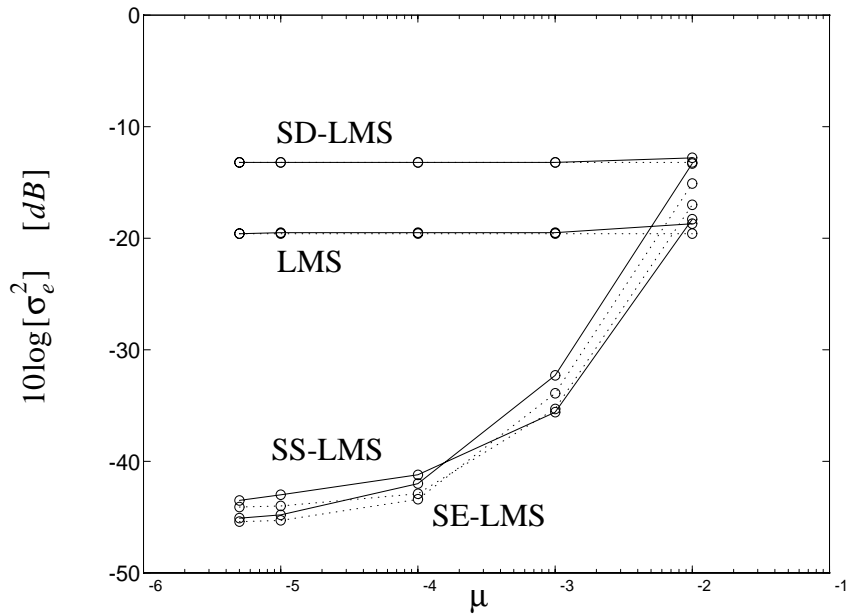


Figure 6.6: Theoretical (dotted lines) and simulated (solid lines) MSE for different offset levels for the four LMS based algorithms; $\alpha = 0.8$ and $\sigma_x^2 = 1$.

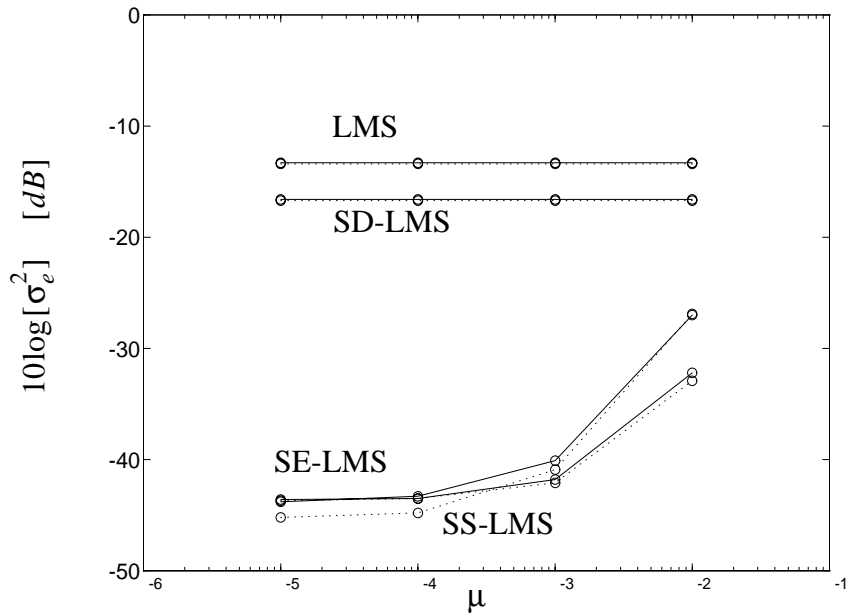


Figure 6.7: Theoretical (dotted lines) and simulated (solid lines) MSE for different offset levels for the four LMS based algorithms; $\alpha = 0.4$ and $\sigma_x^2 = 0.25$.

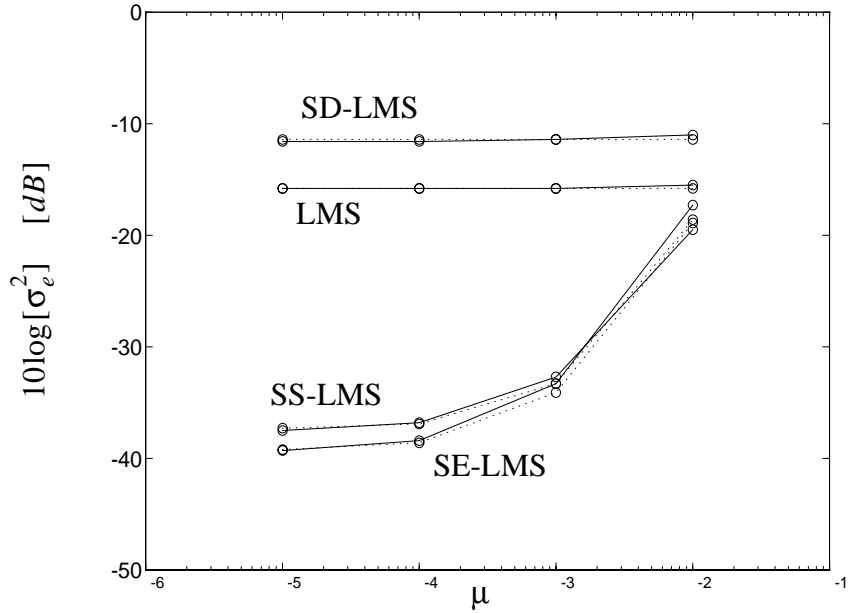


Figure 6.8: Theoretical (dotted lines) and simulated (solid lines) MSE for different offset levels for the four LMS based algorithms; $\alpha = 0.65$ and $\sigma_x^2 = 1$.

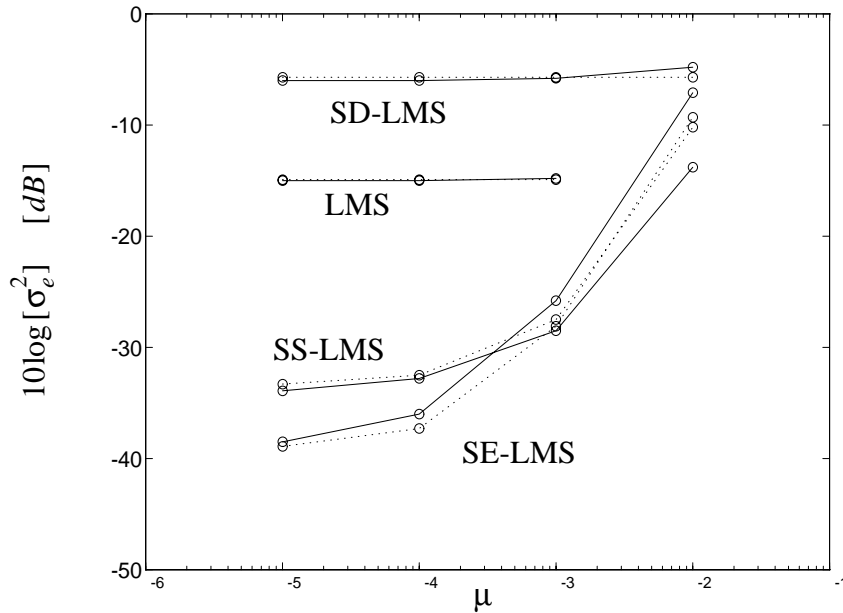


Figure 6.9: Theoretical (dotted lines) and simulated (solid lines) MSE for different offset levels for the four LMS based algorithms; $\alpha = 0.9$ and $\sigma_x^2 = 1$.

Figure 6.10 depicts the excess MSE for each of the algorithms as function of μ with $m_e = 0$. The offsets and the matrix \mathbf{R} (corresponding to a highly correlated input vector) for this simulation were:

$$\mathbf{m}_x^T = [0.02 \quad -0.01 \quad -0.03 \quad -0.005 \quad 0.07]$$

$$\mathbf{m}^T = [0.08 \quad 0.01 \quad -0.05 \quad -0.02 \quad -0.06]$$

$$\alpha = 0.95, \quad \sigma_x^2 = 1, \quad \mathbf{R} = \begin{bmatrix} 10.0934 & 9.5821 & 9.0970 & 8.6364 & 8.2027 \\ 9.5821 & 10.0934 & 9.5820 & 9.0970 & 8.6364 \\ 9.0970 & 9.5820 & 10.0934 & 8.5820 & 9.0970 \\ 8.6364 & 9.0970 & 9.5820 & 10.0934 & 9.5820 \\ 8.2027 & 8.6364 & 9.0970 & 9.5820 & 10.0934 \end{bmatrix}$$

These results validate the predicted behavior of (6.24), (6.33), (6.40), and (6.47). Specifically, it appears that as long as m_e is nulled, the MSE of an adaptive filter using the SE-LMS and the SS-LMS algorithms is shaped by μ . This effect is not true for the LMS

algorithm or the SD-LMS algorithm. Consequently, much better MSE performance in the presence of DC offsets can be attained using the SE-LMS or the SS-LMS algorithms.

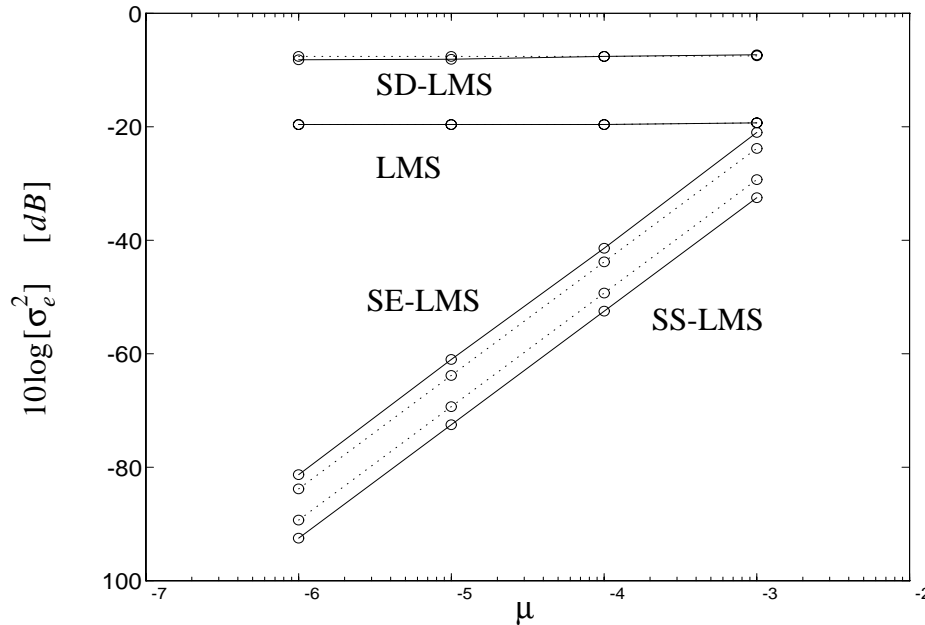


Figure 6.10: MSE as function of μ for the four LMS based algorithms with $m_e = 0$.

6.8 Summary

In this chapter, we have analyzed and provided analytic expressions for the performance of four coefficient update algorithms for analog adaptive filters from an offset point of view. We have found that both the SE-LMS and the SS-LMS algorithms achieve better MSE performance when DC offsets are present; especially when integrator offsets, which dominate in a practical analog system, are unavoidable and in high frequency applications where simply passing the error signal through a high-gain stage to reduce the effects of DC offsets [Johns 91] is impractical. For the SE-LMS and the SS-LMS algorithms, it was shown that by minimizing m_e the MSE can be reduced, whereas this is not the case for the LMS or the SD-LMS algorithms. The practicality of minimizing m_e was briefly discussed. It was observed that if offsets can be controlled, it is possible to reduce the excess MSE by having

the offsets cancel one another (most likely impractical). Also, some comments were given on the possibility of algorithm divergence due to excessive DC offsets.

In terms of implementation complexity, the LMS algorithm is the most complex while the SS-LMS algorithm is the simplest. Between the SD-LMS algorithm and the SE-LMS algorithm, the former is more hardware intensive as N slicers for the N gradient signals will be required while only 1 slicer would be required for the latter.

Having lower offset sensitivity, minimal circuit complexity, combined with the fact that the SD-LMS and the SS-LMS algorithms can diverge due to gradient signal misalignment [Classen 81], it appears the SE-LMS algorithm is the best choice as an algorithm for practical high-frequency analog adaptive filters.

Finally, we would like to point out that the analysis done here is idealized in the sense that the effects of noise, coefficient leakage due to damped integrators, and other analog circuit non-idealities were not considered. These issues are addressed in [Menzi 93]. The results presented and the issues discussed in this chapter are summarized in Table 6.1.

Table 6.1: Result summary.

Test Case	LMS	SD-LMS	SE-LMS	SS-LMS
input power	$\sigma_e^2 \propto 1/\sigma_x^2$	no effect	$\sigma_e^2 \propto 1/\ln[\sigma_x^2]$	no effect
no offsets	$\sigma_e^2 \rightarrow 0$ for $\mu \rightarrow 0$	$\sigma_e^2 \rightarrow 0$ for $\mu \rightarrow 0$	$\sigma_e^2 \propto \mu^2 \sigma_x^4$	$\sigma_e^2 \propto \mu^2 \sigma_x^2$
all offsets	σ_e^2 weakly depends on μ for $\mu \rightarrow 0$ LMS $\sigma_e^2 \propto (\mathbf{m} + m_e \mathbf{m}_x)^T (\mathbf{m} + m_e \mathbf{m}_x)$ SD-LMS $\sigma_e^2 \propto (\mathbf{m} + m_e \mathbf{k}_{\mathbf{m}_x})^T (\mathbf{m} + m_e \mathbf{k}_{\mathbf{m}_x})$		σ_e^2 strongly depends on μ for $\mu \rightarrow 0$ SE-LMS $\sigma_e^2 \propto \frac{m_e^2}{\ln[(\mathbf{m} + \mathbf{m}_x)^T (\mathbf{m} + \mathbf{m}_x)]}$ SS-LMS $\sigma_e^2 \propto \frac{m_e^2}{\ln[\mathbf{m}^T \mathbf{m} / e^{m_{xi}^2 / \sigma_x^2}]}$	
$m_e = 0$	$\sigma_e^2 \propto \mathbf{m}^T \mathbf{m}$	$\sigma_e^2 \propto \mathbf{m}^T \mathbf{m}$	σ_e^2 is scaled by μ^2 SE-LMS $\sigma_e^2 \propto \mu^2 (\mathbf{m}^T \mathbf{m}, \mathbf{m}_x^T \mathbf{m}_x)^2$ SS-LMS $\sigma_e^2 \propto \mu^2 (\mathbf{m}^T \mathbf{m}, e^{m_{xi}^2 / \sigma_x^2})^2$	
algorithm circuit complexity	1 multiplier/tap 1 integrator/tap	1 slicer/tap 1 trivial multiplier/tap 1 integrator/tap	1 trivial multiplier/tap 1 integrator/tap 1 slicer/filter	1 slicer/tap 1 XOR gate/tap 1 counter/tap 1 DAC/tap 1 slicer/filter
convergence	no gradient misalignment	gradients misaligned	no gradient misalignment	gradients misaligned

6.9 Appendix 6.1

Here we evaluate

$$E[\text{sgn}[\mathbf{x} + \mathbf{m}_x]] = \begin{bmatrix} E[\text{sgn}[x_1 + m_{x1}]] \\ E[\text{sgn}[x_2 + m_{x2}]] \\ \dots \\ E[\text{sgn}[x_N + m_{xN}]] \end{bmatrix} \quad (\text{A6-1})$$

Considering the i^{th} element, we obtain

$$\begin{aligned} E[\text{sgn}[x_i + m_{xi}]] &= -P(x_i + m_{xi} \leq 0) + P(x_i + m_{xi} > 0) \\ &= -P(x_i \leq -m_{xi}) + P(x_i > -m_{xi}) \\ &= -F_X[-m_{xi}] + (1 - F_X[-m_{xi}]) \\ &= 1 - 2F_X[-m_{xi}] \end{aligned} \quad (\text{A6-2})$$

where $P(\bullet)$ denotes the probability operator and $F_X[\bullet]$ denotes the cumulative distribution function. For a zero-mean Gaussian distribution with $m_{xi} \leq 0$, we have [Papoulis 91]

$$\begin{aligned} F_X[-m_{xi}] &= \frac{1}{\sqrt{2\pi}\sigma_x} \int_{-\infty}^{-m_{xi}} e^{-\frac{x_i^2}{2\sigma_x^2}} dx_i \\ &= \frac{1}{2} + \frac{1}{2} \text{erf}\left[-\frac{m_{xi}}{\sqrt{2\sigma_x^2}}\right] \end{aligned} \quad (\text{A6-3})$$

where $\text{erf}[u] = \frac{2}{\sqrt{\pi}} \int_0^u e^{-z^2} dz$. Noting that $\text{erf}[u]$ is an odd function in u and substituting (A6-3) into (A6-2) yields:

$$E[\text{sgn}[x_i + m_{xi}]] = \text{erf}\left[\frac{m_{xi}}{\sqrt{2\sigma_x^2}}\right] \quad (\text{A6-4})$$

Had we taken $m_{xi} > 0$ a similar result would have been obtained, thus, (A6-4) is true for all m_{xi} . The result of (6.26) is then easily obtained from (A6-4) and (A6-1).

6.10 Appendix 6.2

Here we evaluate

$$E[\text{sgn}[\mathbf{x} + \mathbf{m}_x]\mathbf{x}^T] = E \begin{bmatrix} \text{sgn}[x_1 + m_{x1}] \\ \text{sgn}[x_2 + m_{x2}] \\ \dots \\ \text{sgn}[x_N + m_{xN}] \end{bmatrix} \begin{bmatrix} x_1 & x_2 & \dots & x_N \end{bmatrix} \quad (\text{A6-5})$$

Considering the i,j^{th} element of the above matrix, for any two zero-mean Gaussian variables x_i, x_j , with covariance $E[x_i x_j] = \sigma_{x_i} \sigma_{x_j} \rho_{i,j}$, using Price's Theorem [Price 58] we obtain:

$$\frac{\partial}{\partial \rho_{i,j}} E[\text{sgn}[x_i + m_{xi}]x_j] = \sigma_{x_i} \sigma_{x_j} E \left[\frac{d}{dx_i} \text{sgn}[x_i + m_{xi}] \frac{d}{dx_j} x_j \right] \quad (\text{A6-6})$$

For the case of Gaussian signals (A6-6) becomes

$$\frac{\partial}{\partial \rho_{i,j}} E[\text{sgn}[x_i + m_{xi}]x_j] = 2 \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \frac{\delta(x_i + m_{xi})}{2\pi \sqrt{1 - \rho_{i,j}^2}} e^{-\left(\frac{x_i^2}{\sigma_{x_i}^2} + \frac{x_j^2}{\sigma_{x_j}^2} - \frac{2\rho_{i,j}x_i x_j}{\sigma_{x_i} \sigma_{x_j}}\right)/2(1 - \rho_{i,j}^2)} dx_i dx_j \quad (\text{A6-7})$$

Integrating the right side of (A6-7) with respect to x_i gives

$$\frac{\partial}{\partial \rho_{i,j}} E[\text{sgn}[x_i + m_{xi}]x_j] = \frac{1}{\pi \sqrt{1 - \rho_{i,j}^2}} \int_{-\infty}^{\infty} e^{-\left(\frac{m_{xi}^2}{\sigma_{x_i}^2} + \frac{x_j^2}{\sigma_{x_j}^2} - \frac{2\rho_{i,j}m_{xi}x_j}{\sigma_{x_i} \sigma_{x_j}}\right)/2(1 - \rho_{i,j}^2)} dx_j \quad (\text{A6-8})$$

After rearranging terms and completing the square (A6-8) simplifies to

$$\frac{\partial}{\partial \rho_{i,j}} E[\text{sgn}[x_i + m_{xi}]x_j] = \frac{e^{-m_{xi}^2/2\sigma_{x_i}^2}}{\pi \sqrt{1 - \rho_{i,j}^2}} \int_{-\infty}^{\infty} e^{-\left(\frac{x_j}{\sigma_{x_j}} + \frac{\rho_{i,j}m_{xi}}{\sigma_{x_i}}\right)^2/2(1 - \rho_{i,j}^2)} dx_j \quad (\text{A6-9})$$

Solving for (A6-9) yields

$$\frac{\partial}{\partial \rho_{i,j}} E[\text{sgn}[x_i + m_{xi}]x_j] = \sqrt{\frac{2}{\pi}} \sigma_{x_j} e^{-m_{xi}^2/2\sigma_{x_i}^2} \quad (\text{A6-10})$$

Integrating both sides of (A6-10) with respect to $\rho_{i,j}$ gives

$$E[\text{sgn}[x_i + m_{x_i}]x_j] = \sqrt{\frac{2}{\pi}}\sigma_{x_j} e^{-m_{x_i}^2/2\sigma_{x_i}^2} \int d\hat{\rho}_{i,j}^{\rho_{i,j}} \quad (\text{A6-11})$$

Solving this trivial integral and substituting for $\rho_{i,j}$ results in

$$E[\text{sgn}[x_i + m_{x_i}]x_j] = \sqrt{\frac{2}{\pi}}\frac{1}{\sigma_{x_i}} e^{-m_{x_i}^2/2\sigma_{x_i}^2} E[x_i x_j] \quad (\text{A6-12})$$

The expression in (6.27) follows readily by substituting (A6-12) into (A6-5).

CHAPTER 7

Conclusions and Suggestions for Future Work

The purpose of this thesis was to demonstrate the feasibility of analog adaptive filtering for data communications. This aim requires a means of implementing the tuning algorithm, supporting circuitry, and demonstration of an experimental prototype. Throughout this work, issues have been identified requiring additional research investigation. In this chapter, the contributions of this work are summarized and suggestions for further research are discussed.

7.1 Summary

In Chapter 2, an analysis was done to show that the current proposals for transmission over copper cables are far below the Shannon limit. This result identified the application area which we believe can benefit from analog adaptive filtering. This benefit would come from the use of pulse-shaping filters, equalizers, and NEXT cancellers to push data transmission over copper to higher data rates.

Adaptive filters require a means of updating the filter coefficients. This adaptation involves the correlation of a filter error signal and a coefficient gradient signal. In Chapter 3, it was proposed to obtain an error signal by making sample measurements on the filter output(s) and comparing with an expected output. These measurements are achieved using a

comparator clocked at time instants at which the expected output is known. This idea essentially makes use of a curve fitting approach to tuning. Also, to keep algorithm complexity to a minimum, it was explained how the error signal can solely be used to adapt a pulse-shaping filter's f_o and Q without the need for a gradient signal. Finally, preliminary simulation results were given for cable equalizers and for an equalizer for the magnetic recording channel. These equalizers were adapted using the same adaptation strategy.

In Chapter 4, the circuits used to implement a prototype filter for experimentation were discussed. A transconductor was proposed whose tuning mechanism makes use of a Gilbert multiplier. Owing to this mechanism, a wide tuning range was obtained and a transconductor input-stage whose linearity is not affected by the tuning mechanism was achieved.

Through experimentation in Chapter 5, it was verified that filtering in the VHF is possible and that the tuning procedure for the pulse-shaping filter is practical. This filter provides at least 10dB harmonic suppression while servicing a 100Mb/s NRZ input. Although the filter was second order, the algorithm can be extended to higher-order filters as explained below in Section 7.2. Practical issues requiring more research work such as the problem of DC offsets were also identified. Based on the results, we believe the tuning approach to equalization should prove favorable. In terms of the filter itself, the tuning range was quite wide (4.5 octaves) and the maximum frequency was 230MHz. This filter is one of the fastest integrated continuous-time filters reported in the literature.

In Chapter 6, a detailed analysis on the effects of DC offsets on four LMS algorithms was done. From the results, one is now in a better position to predict the effect of the offsets for a particular algorithm implementation. It is the author's recommendation to use the SE-LMS algorithm, as it is least susceptible to DC offsets and does not suffer from gradient signal misalignment. It is also compatible with the proposed ideas in Chapter 3 for generating the adaptation error signal.

7.2 Suggestions for Further Work

From the theoretical treatment in Chapter 2, it was noted that NEXT dominates twisted-pair cable capacity. It is therefore possible to push the capacities closer to the Shannon noise bound by exploiting NEXT cancellers. These filters would have to be adaptive as NEXT is a dynamic phenomenon. Such filters are employed in telephone hybrids as echo cancellers. Hence, NEXT cancellers should be feasible at VHF, and research work in this area should be conducted.

The pulse shaper and equalizers discussed here show that current proposals, such as CDDI, can be accommodated using these adaptive filters. However, more work is still required before these filters can be used in a commercial product. For the pulse shaper, a line driver is required while for both filters, it is necessary to implement a robust single chip adaptive filter (i.e. adaptation algorithm on chip). For the line driver, one possibility is a linear amplifier following the pulse shaper. However, the response of the amplifier and the actual cable itself (the amplifier load) will further shape the transmission pulse so that the pulse shaper will have to be pre-distorted to account for the effect. Another option might be to make the line one of the states of the actual adaptive filter (i.e. the load capacitance and impedance). In this way, it would be possible to tune against load variations as well as perform pulse shaping. Granted, the transconductor driving the cable will have to be modified for the high current drive capability.

Naturally, the biquad provides some EMI protection but not enough to pass FCC-B (it may pass FCC-A). A higher-order filter would therefore be needed for a real product. To tune this filter, the same mechanism can be used to tune filter f_o . This procedure implies all poles will be tuned together, either left (higher speed) or right (lower speed), in the frequency domain. Tuning for filter Q s requires more investigation for the particular filter order.

For the cable equalizers, it is imperative that experimental results be provided to verify the concepts. This verification is best done by implementing a fully adaptive filter (i.e. adaptation on chip). Alternatively, it is possible to use the existing pulse-shaping biquad for prototyping and configure it as an equalizer as discussed in Section 3.3.2. What is required, is a cable (or model of it) and an oscilloscope to monitor the “eye” diagram as the equalizer is adapting. The LMS algorithm can be done in labVIEW and would require some modification of the pulse-shaping program.

For the magnetic recording equalizer, more work in this area is needed as the simulations in Chapter 3 were only preliminary, and it was noted that the algorithm can fail for a certain condition. One needs to investigate algorithm robustness when more points are used in the curve fitting template. Also, for both the cable and recording equalizers, the poles were not adapted. However, work can be done on the possibility of tuning these poles together, left or right, in the frequency domain (like the pulse shaper) to cover a wider adaptation range. In this manner, there would be more control over possible instability and much simpler adaptation hardware.

DC offsets in the adaptation algorithm must be compensated and more work in this area is needed. Although one approach is possible [Shoval 92], it requires the implementation of the SS-LMS algorithm which may not be the best choice from a convergence point of view as discussed in Chapter 6. However, an offset cancelled comparator as in [Shoval 92] might be sufficient for the SE-LMS algorithm as noted in Chapter 6. As for the complete LMS implementation, one possibility is shown in Figure 7.1. In the Figure, the multiplier is a Gilbert cell, so sources of DC offset would come from this cell and the input of the $\Sigma\Delta$ converter.

Finally, at steady-state the adaptive filter coefficients will always fluctuate about the optimal values — either due to DAC quantization error or residual DC offsets or both. This effect will lead to residual distortion in the filter response as illustrated for the f_o coefficient.

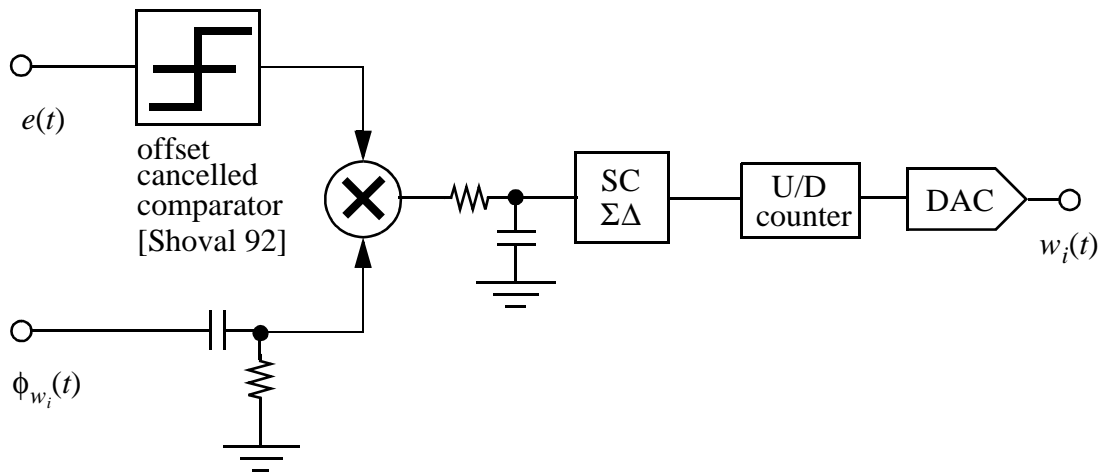


Figure 7.1: One implementation possibility for the SE-LMS algorithm.

One way to reduce the effect is to freeze the DAC once convergence is attained. For example, when a steady-state limit cycle occurs, the DAC can be frozen somewhere in the middle of this limit cycle (if the limit cycle is larger than a single DAC LSB). The question that must be resolved is the length of time the DAC is frozen and the mechanism for restarting the adaptation. The solution would depend on the application. This proposal should not be thought of as a means to compensate for the offset effect completely, but rather, an addition to the offset compensation mechanism employed as discussed in Section 3.2.4.

In terms of circuitry, it was pointed out in Chapter 4 that the CMFB circuit needs improvement and that the modulation of output resistance due to tuning must be reduced. As well, it would be nice to improve the transconductor DC gain. These issues were considered by [Kozma 94]. Also, it was mentioned in Chapter 5 that noise must be reduced significantly. One approach is to reduce the base resistance of $Q_1 - Q_{10}$ by using more base contacts. However, to preserve the speed, the BJT bias current may need to be scaled up. Emitter degeneration for these devices would also reduce noise by reducing the devices' gain as discussed in Section 4.3.3.1. Alternatively, other circuit topologies might be possible to ensure signal and noise gains are equal, or using a folded cascode transconductor and eliminating the

BJT current mirrors. Observe also that base-current loss due to the BJT current mirrors force a mismatch between the currents produced by the two input stages when summed at the transconductor output. This mismatch is a source of non-linearity and can be reduced by using current mirrors with base-current compensation and eliminating the diode level shifters or using emitter degeneration.

7.3 Other Application Areas

A related application area that can make use of adaptive equalization is computer backplanes. At today's high data rates, cable delay becomes significant. Thus, it is important that signals arrive at their destination synchronized in time. However, the distance from the originating source to the destination is variable, thus, delay time would vary. Current practice, other than optical fiber links, is to ensure all cable lengths are equal. This solution tends to clutter backplanes as short links have substantial overhead cabling to ensure their delay is equal to the delay of the longest link. Rather than account for delay by adding excess cable, an adaptive equalizer at each destination point that can compensate for variable cable lengths (much like the cable equalizers discussed in Chapter 3) would be useful — especially as technology is pushed to higher data rates.

Another application area for adaptive filtering is wireless communications. In wireless receivers, a bandpass filter tuned to the IF frequency is used to select a particular channel and reject neighboring channels and disturbances. An adaptive bandpass filter could be more useful and perhaps less complex than the typical PLL scheme for tuning this filter to track the IF.

A possible application area for adaptive filters is in $\Sigma\Delta$ converters. To attain higher conversion speeds, analog technology can be used to replace the current SC technique. Since the analog loop filter requires high accuracy in placing the poles and zeros, fabrication

tolerances must be controlled. Hence, there may be a possibility of using adaptive techniques to tune this filter. A preliminary demonstration of an analog, bandpass- $\Sigma\Delta$ modulator centered at 50MHz has been implemented by [Shoaei 94]. Tuning, at present, is achieved by using the master/slave technique. The master's oscillation frequency tracks an external reference frequency and its control voltages are copied to the slave filter which serves as the loop filter. The measured adjustment range is 30MHz and the frequency accuracy is 10%. The implementation makes use of two separate die of the biquad filter presented herein. Hence, the rather large frequency error is attributed to die mismatch as the entire system is not on a single die.

Another interesting area is digital television signal transport over copper. Systems for the delivery of telephony, data, and command and control information are being proposed over coax from the distribution point to the customer's house at rates of 155Mb/s (downstream, to the home) and about 51Mb/s (upstream, from the home). The cable system configuration is to drive a section of a few amplifiers from a distribution point with each sub-section between amplifiers containing some directional couplers to serve their respective houses. The transport problems in this application are: echo from the couplers as they have a return loss, echo from power splitters in the home, EMI radiation in the home as one can not guarantee good quality shielding and connectors there, and noise ingress in the upstream due to poorly shielded home wiring. Hence, this application requires transceivers with transmit shaping filters and receive echo cancellers/equalizers at each household and sub-section amplifier. The benefit of an analog solution that is adaptive would be in terms of circuit processing speed, chip area, cost, and power requirements.

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