CMOS Optical Preamplifier Design Using Graphical Circuit Analysis

by

Khoman Phang

A thesis submitted in conformity with the requirements
for the degree of Doctor of Philosophy
Graduate Department of the Edward S. Rogers Sr.
Department of Electrical and Computer Engineering
University of Toronto

CMOS Optical Preamplifier Design Using Graphical Circuit Analysis

Khoman Phang

The Edward S. Rogers Sr. Department of Electrical and Computer Engineering

University of Toronto

Degree of Doctor of Philosophy

2001

ABSTRACT

New requirements on optical receivers are being driven by the rapid expansion of optical communications beyond traditional fiber-optic links. This thesis discusses the design of transimpedance amplifiers that are used in the preamplifier stage of optical receivers. The three specific requirements that are addressed here are a wide dynamic range, ambient light rejection, and low-voltage operation.

To achieve a wide dynamic range, we present a fully-differential, variable-gain CMOS transimpedance amplifier. The proposed topology is simpler than previous designs and has improved stability. The implemented design consumes 8mW at 3V, and provides 70 MHz bandwidth with a dynamic range of 77dB, a maximum transimpedance gain of 19kΩ, and a gain range of 32dB.

To reject ambient light, we place an active feedback loop around the transimpedance amplifier. This topology eliminates the need for large passive components and improves the regulation of the photodiode bias voltage. However, the lower-frequency limit of this topology is dependent on the ambient light level. We experimentally verify this technique, and analyze the stability requirements of the feedback loop.

To achieve low-voltage operation, we develop a CMOS transimpedance amplifier capable of 1V operation without the use of low-threshold MOS transistors. The design has a wide output swing and maximizes the available bias voltage for the photodiode. The biasing of the MOS feedback resistor is performed using a charge pump to generate a stable gate voltage — a technique called dynamic gate biasing (DGB). The proposed design was implemented as part of an optical receiver front-end which also included two post amplifiers. The resulting front-end consumes 1mW from a 1V supply and provides 210kΩ transimpedance gain over a 50MHz bandwidth.

Also included in this thesis is the development and application of a graphical circuit analysis technique called DPI/SFG analysis that is based on driving-point impedances (DPI) and signal-flow graphs (SFG). We develop a general formulation of the technique, illustrate its use on a number of circuit examples, and apply it to the design and optimization of the low-voltage transimpedance amplifier.

Acknowledgements

Many people helped to make this thesis possible. I am indebted to my supervisor, David Johns, for being my mentor for the last ten years, for guiding me, both personally and professionally, and for providing me with the opportunities that I needed to grow as both a researcher and instructor. I wish to thank Professors Ken Martin, John Long, and Igor Filanovsky for their valuable comments and suggestions throughout the thesis. To Professor Adel Sedra: my sincere thanks for your advice, support, and wisdom throughout the years. Many thanks to Professor Keith Balmain and to Gerald Dubois for their help with the EMC chamber, and to Dr. Agustin Ochoa Jr. and Takis Zourntos for their helpful discussions on the DPI/SFG method. On a broader note, I wish to acknowledge the many professors in the Department of Electrical and Computer Engineering who have inspired me with their teaching. I endeavour to pass on to future students that which I have so richly inherited from them.

I wish to thank my friends at the University of Toronto for their invaluable technical assistance and for making my years here so special. In particular, I want to thank Bahram Zand, James Maligeorgos, Steve Hranilovic, Ali Sheikholeslami, Wynstan Tong, Kasra Ardalan, Vincent Gaudet, Steve Jantzi, Stephen Alie, Bryn Owen, and Karen Kozma. A special thanks to my dear friends Angela Chuang, Ben Schwartz, and Ravi Ananth for their constant encouragement, support, and prayers during my studies.

To my wife, Du: thank you for your tireless support of our family throughout this work. To you I owe everything — with compound interest! My deepest thanks to my parents for their unfailing love and support, and for teaching Du, me, and our wonderful sons, Damen and Steven, the true meaning of family.

Finally, I wish to acknowledge the funding support provided by the Natural Sciences and Engineering Research Council of Canada (NSERC), Micronet, and the University of Toronto. IC fabrication was facilitated by the Canadian Microelectronics Corporation (CMC).

Table of Contents

CHAPTER

1 Introduction

1.1 OVERVIEW

Optical communications is one of the cornerstones of today's revolution in information technology. Vast distances of optical fiber span the globe, connecting the world together in an intricate communications infrastructure. With the drive towards portable and multimedia communications, we are increasingly faced with the challenge of bringing the capacity of our communications infrastructure directly to the user, providing seamless access to vast quantities of information, anywhere and anytime. Whether it is the transfer of an image from a digital camera to a laptop computer or the communication of data within a massively parallel computer, there is an urgent need to develop new methods of high speed data communications.

Light offers many advantages as a medium for communication. Whether travelling through free space or through optical fiber, light enjoys unequalled channel bandwidth, and is capable of data rates in the terabits per second. This immense capacity is due to the nature of the photons that constitute an optical signal. Unlike electrons, photons react weakly to their environment and to one another. As such, optical signals neither generate nor are sensitive to electromagnetic interference (EMI), parasitic coupling, and other problems faced by electrical signals [Montrose,1996].

Given their advantages, optical links are rapidly expanding into application areas beyond traditional fiber-optic links [Woodward,1999]. Three sample applications of so-called "carrier" applications that are concerned with transporting information across the greatest possible distance are free-space intersatellite links [Thompson, 1991], [Begley,1994], [Alexander,1997], fiber-to-the-home (FTTH) [Faulkner,1989], [Kwok,1995], and terrestrial free-space links for inter-building communications [Jolt], [AirFiber], [Terabeam], [CableFree], [Eardley,1996].

Shorter distance applications include optical-based local area networks (LANs) as represented by Asynchronous Transfer Mode Passive Optical Networks (ATM-PON) [Van de Voorde,1997] and Gigabit Ethernet standards [Gigabit,1998]. Applications that involve optical communications within digital systems or in large computers — generally referred to as optical interconnect [Li,2000], [Bristow,1999] — include smart pixel arrays [Chen,2000], [van Blerkom,1998], [Zheng,2000], optocoupler arrays [Rooman,2000], and optical backplanes [Funada,1999]. Finally, so called "optical wireless links" provide a communications solution for portable applications [Heatley,1998]. In particular, short-range "point-and-shoot" systems in accordance to the Infrared Data Association (IrDA) provide a simple solution for transferring information to and from portable devices, offering high data rates at low cost and with a small form factor that is not prone to mechanical wear [Williams,2000].

The success of such short-range systems is particularly telling of how optical communication systems are likely to proliferate in the future: as of 1998, over 100 million laptops, digital cameras, and other devices were shipped equipped with IrDA-compatible serial ports [IrDA,1999], and currently over 40 million new devices are being produced yearly [Williams,2000]. The IrDA wireless link has overshadowed both the Universal Serial Bus (USB) and IEEE 1394 FireWire to become the leading serial-port alternative for connectivity [IrDA,1999].

Figure 1.1 shows the basic elements of an optical link. On the transmit side, an information source produces a data stream that is encoded and sent to the appropriate drive circuitry used to modulate the optical signal generated by either a light emitting diode (LED) or laser. The signal propagates through free space or through a waveguide such as optical fiber until it reaches the photodetector on the receiver end. The photodetector converts the optical signal into an electric current that is sensed by the optical preamplifier and regenerated to a sufficiently strong voltage signal from which the original data can be recovered by the demodulator.

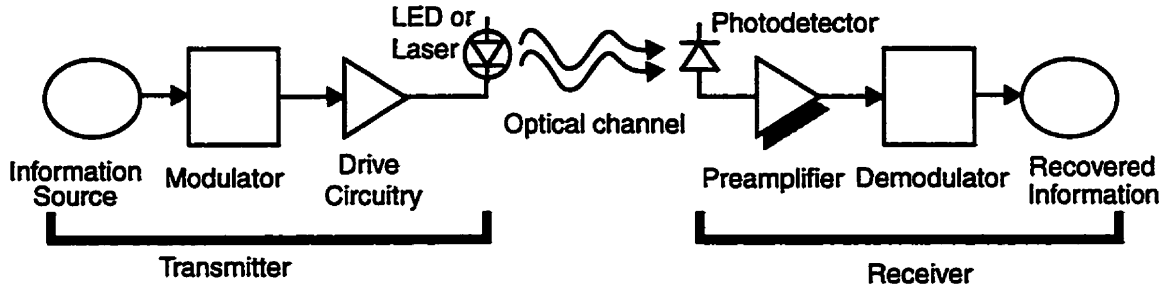


Figure 1.1 Block diagram of a typical optical link.

The expansion of optical communications into new applications has created exciting opportunities for the research and innovation of optical receivers. While the growth of fiber-optic networks in the last few decades has refined our understanding of optical receivers, its primary focus has been on speed and sensitivity. With the expansion of optical communications comes new requirements on receiver designs.

Probably the most widespread trend has been that of increased system integration and the drive to reduce system components, cost, and size. Traditionally, optical receivers have not been subject to many system level constraints since optical receivers for long-haul fiber-optic networks are principally designed for performance rather than cost. As such, they have typically used advanced high-speed semiconductor technologies such as GaAs and Si bipolar processes.

Increasingly, new optical receiver designs are being implemented in low-cost, high-integration technologies such as CMOS. However, the desire to implement in CMOS implies a need to design receivers that keep pace with developments in CMOS technology. One of the dominant trends is the continual reduction of system supply voltage as illustrated by the forecasted trend shown in Figure 1.2 from the Semiconductor Industry Association [SIA,1997]. Upper and lower boundary lines are drawn to highlight the fact that the 'industry standard' voltage is disappearing, being replaced instead by a range of voltages encompassing different applications. Increasingly, the supply voltage is seen as an adaptable design parameter used to

optimize performance and minimize power [Liu,1993], [Frank,1997], [Geppert,2000]. Logic circuits that operate with supply voltages near or even below the threshold voltage [Svensson,1998], [Soeleman,1999] are being reported alongside analog circuits that do the same [Vittoz,1994], [Sansen,1998], [Wong,1999], [Duque-Carrillo,2000]. Low-voltage operation is partly driven by the desire for low power in portable applications and in applications that require battery back-up such as fiber-to-the-home (FTTH) [Nakamura,1999], [Sackinger,1999]. In the end, low-voltage operation will be crucial to the long-term viability of integrated optical receivers.

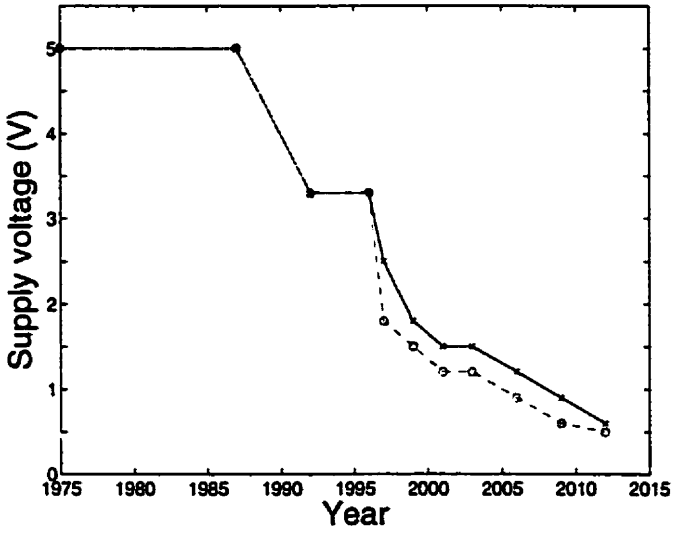


Figure 1.2 Projected trends in system supply voltages. Dashed and solid lines represent anticipated lower and upper bounds respectively.

Another emerging trend in optical receivers is the desire for greater dynamic range. The dynamic range is a measure of the variation in signal strength that can be tolerated by the receiver while still meeting performance requirements such as the bit error rate. The minimum signal is determined by the receiver's noise while the maximum signal is determined by the overload or saturation point of the receiver. Traditionally, receivers for long-haul fiber-optic networks have not required as wide a dynamic range because the received signal levels have been optimized to be small in order to maximize link distance and to minimize the need for repeaters

[Ohhata,1999]. With many of the new applications, more flexibility is required and the link distance and associated path losses are less stringently controlled. In such cases, the receiver must compensate by having an increased dynamic range. If the requirement is modest, the increase can be achieved through additional gain control stages at the front end of the receiver. However, if the required increase is great, additional steps must be taken right at the preamplifier stage. For instance, current IrDA standards for optical wireless systems allow a variable link distance from 0 cm up to 100 cm. Over this distance, the irradiance may vary from 500 mW/cm^2 down to 4 $\mu W/cm^2$, representing a span of over five orders of magnitude [IrDA,1997].

For applications in which the optical signal travels through free space, the rejection of ambient light is an additional receiver requirement. If the ambient light is low relative to the signal, it can be easily rejected through filtering in later stages of the receiver. However, if the ambient light is much stronger than the signal, the ambient light must be rejected right at the preamplifier to prevent it from overwhelming the signal. For instance, current IrDA standards specify a maximum ambient light level of 490 $\mu W/cm^2$ that is over a hundred times larger than the minimum signal intensity of 4 $\mu W/cm^2$ [IrDA,1997].

In summary, we have pointed out three additional receiver requirements — low-voltage operation, wide dynamic range, and ambient light rejection — that are common to many new applications of optical links. One application in particular, optical wireless communications, pushes these requirements to their extreme, motivating us to investigate how these new requirements can be addressed at the optical preamplifier stage.

1.2 THESIS OUTLINE

This thesis constitutes an extended study of optical preamplifier circuits designed to address the emerging requirements placed on optical receivers. Our primary focus will be on the optical wireless application where these requirements are most clearly needed. In general, optical wireless receivers have more modest band-

widths than fiber-optic receivers. This is partly because optical wireless is a low cost application, and partly because the large path losses that are incurred through free-space transmission require the use of large LED's and photodiodes that are more difficult to drive and interface [Barry,1994]. Such devices typically have active areas on the order of a few square millimeters. Current industry standards support data rates of 4 Mb/s [IrDA,1997], but higher rates of 16Mb/s and above are being investigated.

In this thesis, we aim for data rates on the order of 100 Mb/s, a rate that is comparable with current LAN rates and one that is sufficiently fast to support real-time video applications.[1] In the process of developing our preamplifier circuits, we formulate a graphical method of circuit analysis based upon driving-point impedances (DPI) and signal-flow graphs (SFG) that we will refer to as the DPI/SFG analysis method.

The following are the main contributions of the thesis:

- a variable-gain transimpedance amplifier with improved stability,
- an active feedback structure for rejecting ambient light at the preamplifier,
- a novel topology for low-voltage transimpedance amplifiers,
- the development of dynamic gate biasing (DGB) as a general technique for low-voltage analog circuits, and
- a general formulation of the DPI/SFG analysis method and its application to circuit design.

Chapter 2 provides the basic background needed for the rest of the thesis. Included is an overview of photodetectors and optical preamplifiers, and a review of previously reported solutions to the new design requirements. The chapter also reviews signal-flow graphs, and the traditional circuit analysis techniques. Included is a discussion of the limitations of each of the techniques, and the motivation behind the DPI/SFG analysis method.

Chapter 3 describes the new optical preamplifier structures for enhanced dynamic range, ambient light rejection, and low-voltage operation. We propose a

1. Assuming 8 bits/pixel, 640 x 480 pixels/frame, and 40 frames/sec.

technique called dynamic gate biasing (DGB) that uses charge pumps for the stable biasing of transistors. The challenge of analyzing the low-voltage transimpedance amplifier is highlighted to motivate the discussion of graphical circuit analysis in Chapter 4.

Chapter 4 presents the DPI/SFG analysis method. The chapter begins with a history of the technique and discusses its current limitations. It then presents a general formulation of the method based on Kirchhoff's Current Law. Numerous examples are presented to aid the reader with the details of the technique and to highlight its ability to provide insight into a circuit's operation.

Chapter 5 applies the DPI/SFG analysis method to the design and optimization of the low-voltage transimpedance amplifier introduced in Chapter 3. The design process and the ability of DPI/SFG analysis to provide insight into the operation of circuits is emphasized.

Chapter 6 presents the implementation details and experimental results of two fabricated integrated circuits that were used to verify the proposed preamplifier designs. Finally, in Chapter 7, the thesis is summarized and directions for future work are discussed.

REFERENCES

AirFiber Inc., Web Site, http://www.airfiber.com/index.htm.

S. B. Alexander, *Optical Communication Receiver Design*, SPIE Optical Engineering Press, London, UK, Chapter 1, 1997.

J. R. Barry, *Wireless Infrared Communications*, Kluwer Academic Pub., Boston, Mass., Chapter 3, pp. 49-52, 1994.

D. L. Begley, editor, *Selected Papers on Free-Space Laser Communications II*, SPIE Optical Engineering Press, Bellingham, Vol. MS100, 1994.

J.P. Bristow and S. Tang, editors, *Optoelectronic interconnects VI*, Proc. SPIE, vol. 3632, San Jose, CA, January 1999.

CableFree Solutions Ltd., Web Site, http://www.cablefree.co.uk.

H. D. Chen, "Flip chip bonded hybrid CMOS/SEED optoelectronic smart pixels," *IEE Proc. Opto-*

electronics, vol. 147, no. 1, pp. 2-6, February 2000.

J. F. Duque-Carrillo, J. L. Ausin, G. Torelli, J. M. Valverde, and M. A. Dominguez, "1-V Rail-to-Rail Operational Amplifiers in Standard CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 33-44, January 2000.

P. L. Eardley and D. R. Wisely, "1Gbit/s optical free space link operating over 40m — system and applications," *IEE Proceedings on Optoelectronics*, vol. 143, no. 6, pp. 330-333, December 1996.

D. W. Faulkner, D. B. Payne, J. R. Stern, and J. W. Ballance, "Optical networks for local loop applications," *IEEE J. Lightwave Tech.*, vol. 7, no. 11, pp. 1741-1751, November 1989.

D. J. Frank, P. Solomon, S Reynolds, and J. Shin, "Supply and Threshold Voltage Optimization for Low Power Design," *IEEE Int. Symp. Low Power Electronics and Design*, pp. 317-322, 1997.

M. Funada et al., "Proposal for a novel optical bus system using optical sheet bus technology," *Optoelectronic Interconnects VI*, J.P. Bristow and S. Tang, editors, Proc. SPIE, vol. 3632, San Jose, CA, January 1999.

L. Geppert and T. S. Perry, "Transmeta's magic show," *IEEE Spectrum*, vol. 37, no. 5, pp. 26-33, May 2000.

The Gigabit Ethernet Standard, IEEE Standard 802.3z, 1998.

D. J. T. Heatley, D. R. Wisely, I. Neild, and P. Cochrane, "Optical Wireless: The story so far," *IEEE Commun. Mag.*, pp. 72-82, December 1998.

Infrared Data Association (IrDA), *Serial Infrared Physical Layer Link Specification*, Version 1.2, http://www.irda.org, Nov. 1997

Infrared Data Association (IrDA), The *IrDA Bulletin*, http://www.irda.org, May-July 1999.

Jolt Ltd., Wireless Optical Communications, Web Site, http://www.jolt.co.il.

T. Kwok, "A vision for residential broadband services: ATM-to-the-home," *IEEE Network*, vol. 9, no. 5, pp. 14-28, Sept.-Oct. 1995.

Y. Li, E. Towe, and M. W. Henry, editors, *"Special Issue on Optical Interconnections for Digital Systems," Proceedings of the IEEE*, June 2000.

D. Liu and C. Svensson, "Trading Speed for Low Power by Choice of Supply and Threshold Voltages," *IEEE J. Solid-State Circuits*, vol. 28, no. 1, pp. 10-17, Jan. 1993.

M. Montrose, *Printed Circuit Board Design Techniques for EMC Compliance*, IEEE Press, New York, 1996.

M. Nakamura and N. Ishihara, "1.2V, 35mW CMOS optical transceiver ICs for 50Mbit/s burst-mode communication," *Electronic Letters*, vol. 35, no. 5, pp. 394-395, 4 March 1999.

K. Ohhata, T. Masuda, K. Imai, R. Takeyari, and K. Washio, "A Wide-Dynamic Range, High-Transimpedance Si Bipolar Preamplifier IC for 10-Gb/s Optical Fiber Links," *IEEE J. Solid-State Circuits*, vol. 34, no. 1, pp. 18-24, January 1999.

C. Rooman, D. Coppee, and M. Kuijk, "Asynchronous 250Mb/s Optical Receivers with Integrated

Detector in Standard CMOS Technology for Optocoupler Applications," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 953-958, July 2000.

E. Sackinger, Y. Ota, T. J. Gabara, W. C. Fischer, "15mW, 155Mb/s CMOS Burst-Mode Laser Driver with Automatic Power Control and End-of-Life Detection," *IEEE ISSCC Dig. Tech. Papers*, pp. 386-387, February 1999.

W. Sansen, M. Steyaert, V. Peluso, E. Peeters, "Toward Sub 1V Analog Integrated Circuits in Submicron Standard CMOS Technologies," *IEEE ISSCC Dig. Tech. Papers, pp. 186-187*, February 1998.

SIA (Semiconductor Industry Association), *International Technology Roadmap for Semiconductors*, http://www.semichips.org, p. 17, 1997.

H. Soeleman and K. Roy, "Ultra-Low Power Digital Subthreshold Logic Circuits," *Int. Symp. Low Power Electronics and Design*, pp. 94-96, August 1999.

C. Svensson and A. Alvandpour, "Low Power and Low Voltage CMOS Digital Circuit Techniques," *IEEE Int. Symp. Low Power Electronics and Design*, pp. 7-10, August 1998.

TeraBeam Corporation, Web Site, http://www.terabeam.com.

B.J. Thompson, editor, *Selected Papers on Free-Space Laser Communications*, SPIE Optical Engineering Press, Bellingham, Vol. MS30, 1991.

D. A. van Blerkom, C. Fan, M. Blume, S. C. Esener, "Transimpedance Receiver Design Optimization for Smart Pixel Arrays," *IEEE J. lightwave Tech.*, vol. 16, no. 1, pp. 119 - 126, January 1998.

I. Van de Voorde, and C. Van der Plas, "Full service optical access networks: ATM transport on passive optical networks," *IEEE Commun. Mag.*, vol. 35, no. 4, pp. 70-75, April 1997.

E. A. Vittoz, "Low-Power Design: Ways to Approach the Limits," *IEEE ISSCC Dig. Tech. Papers, pp. 14-18*, February 1994.

S. Williams, "IrDA: Past, Present and Future," *IEEE Personal Communications*, vol. 7, no.1, pp. 11-19, February 2000.

L. S. Y. Wong, C. Y. Kwok, and G. A. Rigby, "A 1-V CMOS D/A Converter with Multi-Input Floating-Gate MOSFET," *IEEE J. Solid-State Circuits*, vol. 34, no. 10, pp. 1386-1390, October 1999.

T. K. Woodward, A. V. Krishnamoorthy, "1-Gb/s Integrated Optical Detectors and Receivers in Commercial CMOS Technologies," *IEEE J. Selected Topics in Quantum Electronics*, vol. 5, no. 2, pp. 146-156, March/April 1999.

X. Z. Zheng, P. J. Marchand, D. W. Huang, and S. C. Esener, "Free space parallel multichip interconnection system," *Applied optics*, vol. 39, no. 20, pp. 3516-3524, July 2000.

CHAPTER

2 Background

This chapter provides the background needed for the thesis. The chapter begins with an overview of photodetectors, optical preamplifiers, and transimpedance amplifiers. It then discusses the receiver design requirements, and reviews previously reported solutions. Having provided a context for our work on optical preamplifiers, the chapter focuses on the circuit analysis aspects of this thesis by discussing the limitations of current circuit analysis techniques, providing a basic review of signal-flow graphs, and discussing the motivation for DPI/SFG analysis.

The development of fiber-optic communications can be traced back to the 1970's. Since that time, an extensive body of literature has developed for optical receivers and photodetectors for fiber-optic applications that can provide the interested reader with a more comprehensive treatment of these subjects [Kressel,1982], [Personick,1985], [Miller,1988], [Alexander,1997]. In addition, there are two excellent references that deal specifically with optical wireless systems, their optoelectronics, and other design issues at the circuits and system level [Barry,1994], [Hranilovic,1999].

2.1 PHOTODETECTORS

Photodetectors are semiconductor devices that convert incident light into an electric current. There are various types of photodetectors such as photovoltaic cells, photodiodes, and phototransistors. For high-speed optical communications, photodiodes are preferred given their superior frequency response. Photodiodes are usually operated under reverse-bias conditions. Like other semiconductor diodes, photodiodes possess a finite carrier transit time. From a circuit design standpoint, however, we can suitably model the photodiode's electrical behaviour with the small-signal equivalent circuit model shown in Figure 2.1.

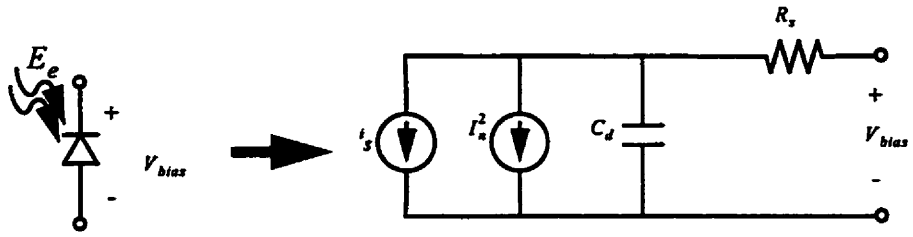


Figure 2.1 Small-signal equivalent circuit model of photodiode.

The main photocurrent, i_s, is generated through the creation of electron-hole pairs when photons from the incident light penetrate the diode. The sensitivity of the photodetector is a function of the wavelength, and so to maximize power efficiency, the emission wavelength of the optical source should be spectrally matched to the photodiode. Silicon photodiodes, which are commonly used in low-cost applications, have a peak spectral efficiency in the near infrared region. Figure 2.2 shows the normalized spectral sensitivity of a typical silicon photodiode[1], and shows how it is spectrally matched to GaAs LEDs (e.g. Temic TSHF5400).

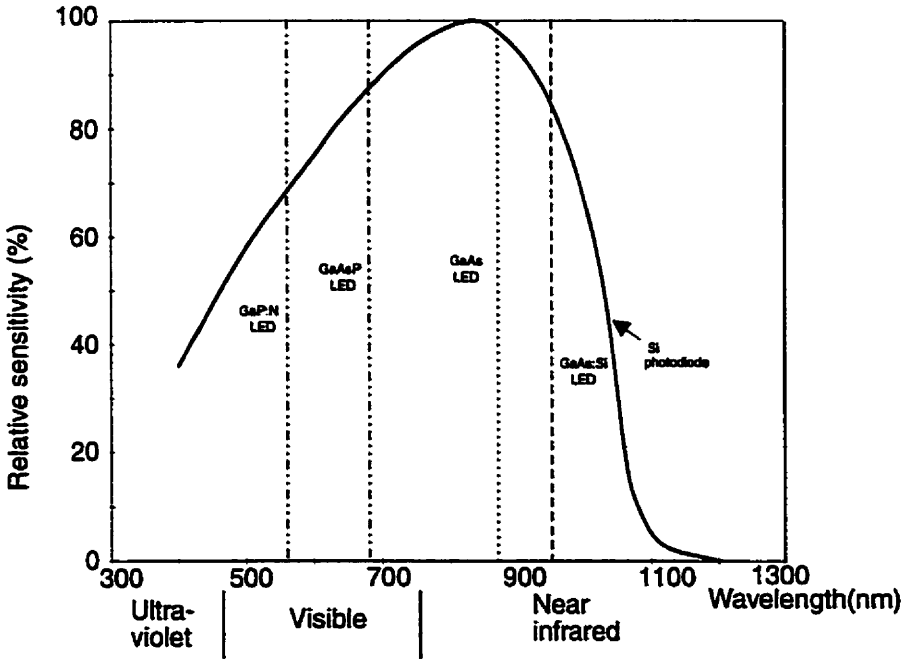


Figure 2.2 Relative spectral sensitivity of Temic BPV22NF silicon photodiode and emission peaks of several types of LEDs.

1. Data taken from Temic's BPV22NF photodiode.

There is a linear relationship between the photocurrent, i_s, and the irradiance, E_e, which is a measure of the intensity of the incident light and is given in W/m^2. The photocurrent is calculated by

$$i_s = \frac{\eta q}{h\upsilon} A_{eff} E_e = R\varnothing_e$$

where η is the quantum efficiency of device (typically in the range of 0.6 to 0.9), q is a unit electron charge (1.69×10^{-19} C), h is Planck's constant (6.626×10^{-34} J/s), υ is the frequency of the light, and A_{eff} is the effective area of the photodiode and accounts for the effect of the lens. The collective term, $R = \eta q/h\upsilon$, is commonly known as the responsivity of the device, and is in units of A/W. The product, $\varnothing_e = A_{eff}E_e$, is the received optical power in Watts. For example, the Temic BPV22NF is rated to provide $85nA$ of photocurrent per 1 $\mu W/cm^2$ irradiance at 870 nm. The current source, I_n^2, models the shot noise generated by the dc current which includes the photodiode's intrinsic dark-current as well as photocurrent due to background light. The noise has a white spectrum with a normalized noise power density given by

$$I_n^2(f) = 2qI_s \qquad A^2/Hz \tag{2.1}$$

where I_s is the dc component of i_s.

The remaining two elements of the model, R_s and C_d, represent the series resistance of the diode and the diode capacitance. Since the photodiode is operating under reverse-bias conditions, the capacitance C_d is dominated by the depletion capacitance across the p-n junction. As a result, C_d is greatly dependent on the applied bias voltage, as illustrated in Figure 2.3 for the BPV22NF photodiode. This characteristic is particularly significant when designing low-voltage receivers where the maximum reverse bias that can be applied to the photodiode is severely limited.

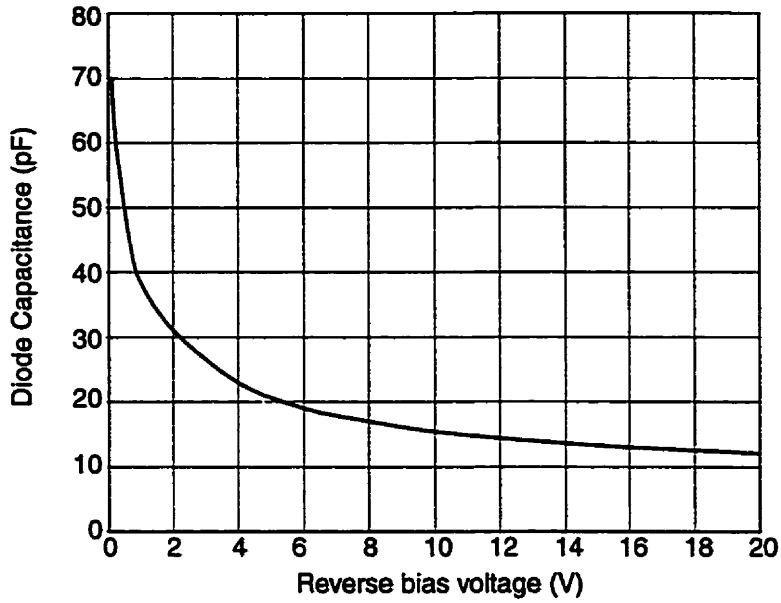


Figure 2.3 Photodiode capacitance vs. bias voltage for the Temic BPV22NF.

2.2 OPTICAL PREAMPLIFIER STRUCTURES

The optical preamplifier performs the critical function of interfacing the photodiode to the rest of the receiver. Typically, the preamplifier converts the received photocurrent into a voltage signal. The preamplifier plays a crucial role in determining many aspects of the overall performance of the receiver including speed, sensitivity, and dynamic range.

Optical preamplifiers are typically based on a either a termination resistor or a transimpedance amplifier. In the first approach, the photodiode is attached to a load resistor, R_L, as shown in Figure 2.4. The current signal, i_s, is converted into a voltage by the load resistor, and the resulting voltage signal is buffered by the voltage amplifier. The capacitance C_T represents the total capacitance associated with the photodiode and the amplifier.

The choice of the load resistance affects both the frequency response and the noise performance of the preamplifier. The intrinsic bandwidth of the preamplifier is equal to $1/(2\pi R_L C_T)$ because of the RC network. The noise can be analyzed using

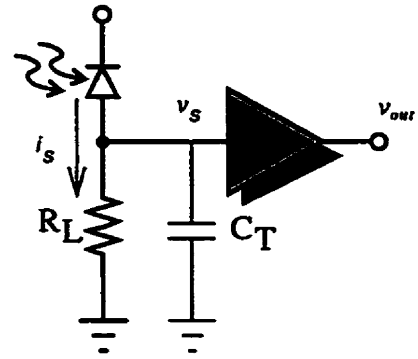


Figure 2.4 Optical preamplifier based on a termination resistor.

the small-signal noise model shown in Figure 2.5. Here, the thermal noise of the load resistor is modeled by current source I_{nRl}^2 with a normalized power of

$$I_{nRl}^2(f) = \frac{4kT}{R_L} \qquad A^2/Hz \tag{2.2}$$

where k is Boltzmann's constant ($1.38 \times 10^{-23} JK^{-1}$) and T is the absolute temperature in Kelvin. The noise of the voltage amplifier is modeled by current source I_n^2 and voltage source V_n^2. Because the desired signal is in the form of a current, the signal can be directly compared to the noise currents that are injected into the same node. It is easy to show that the noise contribution due to V_n^2 is independent of R_L when the input impedance of the voltage amplifier is very large. Since the noise current of I_n^2 is also independent of R_L, the only way to minimize the total noise is by reducing I_{nRl}^2 through maximizing R_L.

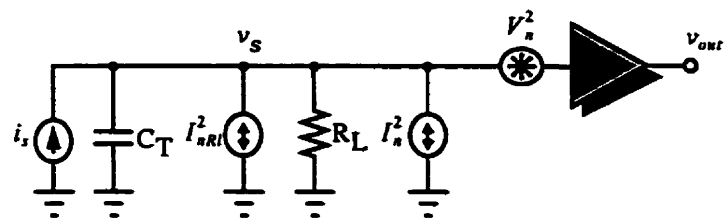


Figure 2.5 Small-signal noise model of the optical preamplifier based on a termination resistor.

This observation leads to two approaches to choosing the resistance of R_L. In the so-called low-impedance design [Barry,1994], resistor R_L is made small (for example, 50Ω for transmission line matching) to satisfy the bandwidth requirement at the cost of increased noise. Alternatively, in so-called high-impedance designs [Smith,1982], [Alexander,1997], [Muoi,1984], resistor R_L is made very large to minimize noise at the cost of reduced bandwidth. Typically, the resulting preamplifier bandwidth is below that of the signal, and additional equalization in the form of high-pass filtering is necessary to achieve the required bandwidth. Although the high-impedance design has been shown to provide the highest sensitivity of all optical preamplifiers [Personick,1973], the design suffers from a limited dynamic range due to the integration effect resulting from the large RC time constant [Muoi,1984].

Optical preamplifiers based on the transimpedance amplifier are currently the most popular because they avoid the dynamic range problem associated with high-impedance designs, and because they provide a good compromise between the wide bandwidth of the low-impedance design and the low noise performance of the high-impedance design [Muoi,1984]. In a transimpedance amplifier, a resistor R_f is placed across the gain stage as shown in Figure 2.6. Here, the resistor can be made large because the negative feedback reduces the effective resistance seen by the photodiode by a factor of $(1 + A)$ where A is the open-loop voltage gain of the amplifier. As a result, the bandwidth can be matched to that of the signal, eliminating the need for equalization. In addition, the thermal noise contribution of the feedback resistor is minimized. The closed-loop transimpedance gain is defined as the ratio

$$\frac{v_{out}}{i_s} = -\frac{A}{1 + A} R_f \approx -R_f \tag{2.3}$$

so that for large open-loop gains, the transimpedance gain is simply the negative of the feedback resistance.

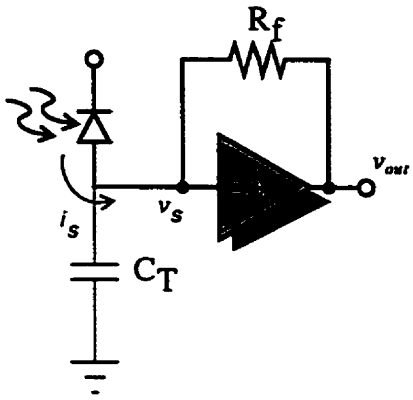


Figure 2.6 Optical preamplifier based on a transimpedance amplifier.

2.3 TRANSIMPEDANCE AMPLIFIER DESIGN REQUIREMENTS

Traditionally, the design challenge of fiber-optic preamplifiers has been in optimizing the trade-offs between sensitivity, speed, and transimpedance gain. As discussed in the previous chapter, new applications of optical communications have introduced additional receiver requirements such as wide dynamic range, ambient light rejection, and low-voltage operation. This section discusses each of these requirements in greater detail, and reviews previously reported solutions.

2.3.1 Wide Dynamic Range

A wide dynamic range is essential in order to accommodate variable link distances. Current IrDA standards, for instance, require an optical dynamic range of 51dB in order to support a link distances range of 0 cm up to 100 cm[IrDA,1997]. Although the dynamic range of a transimpedance amplifier is greater than that of a high-impedance design, it is still insufficient to handle such a wide input range. As illustrated in Figure 2.7, there are three principal techniques for extending the dynamic range of the preamplifier: 1) output signal limiting, 2) input current steering, and 3) variable transimpedance gain.

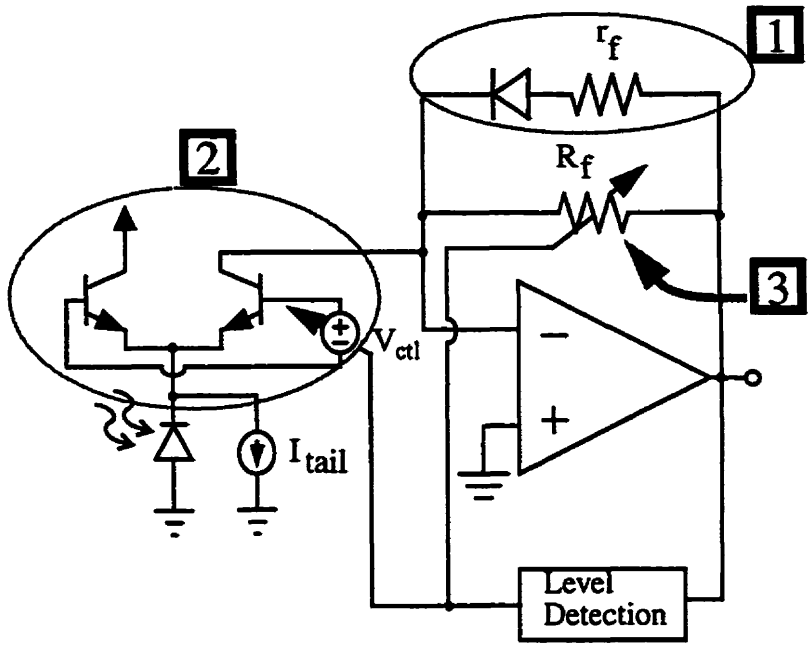


Figure 2.7 Various methods of increasing dynamic range: 1) output signal limiting, 2) input current steering, and 3) variable transimpedance gain.

The simplest technique is to limit the output swing as represented by the diode clamp in Figure 2.7. While limiting does not affect the lower limit of the dynamic range, it does increase the upper limit by allowing the receiver to accept strong signals that would have otherwise overloaded the receiver and prevented normal operation. Limiting can be performed either within the preamplifier [Yamazaki,1997], or in cases where the dynamic range requirements are more modest, externally by following the preamplifier with a limiter circuit [Nakamura,1999], [Ohhata,1999]. The advantage of limiting is that it does not require level detection circuitry. However, the process of limiting destroys the amplitude information of the received signal. As such, limiting can only be used with binary signalling schemes. In addition, limiting introduces pulse width distortions that result out of the uneven gain applied to different portions of the pulse. Finally, for applications in which ambient light is an issue, limiting removes information that helps separate the ambient light from the information signal.

The second technique, input current steering, also improves the dynamic range by increasing the maximum acceptable signal level of the preamplifier. It uses a dif-

ferential pair before the preamplifier to realize an adjustable attenuation of the signal current based on the control voltage, V_{ctl} [van den Broeke,1993], [Owen,1982]. The technique is shown conceptually in Figure 2.7.

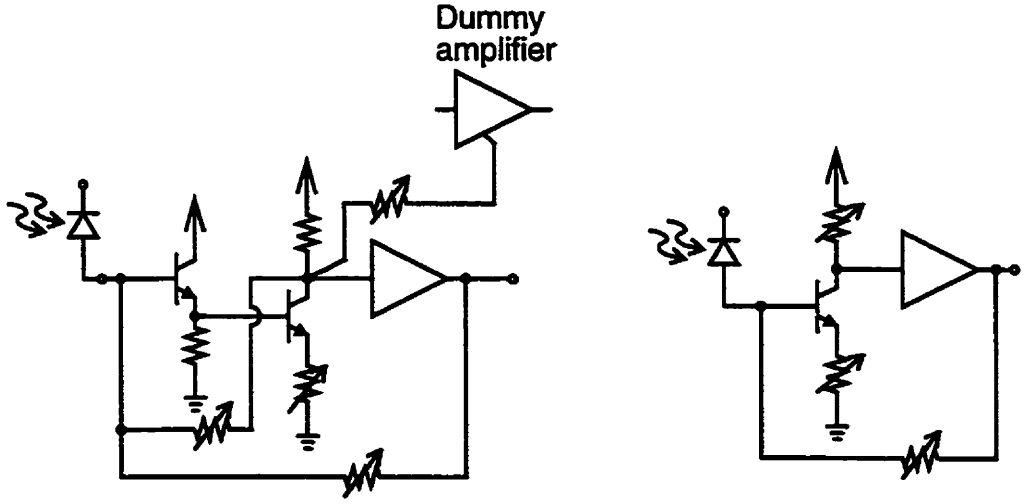
In practice, bipolar transistors are much more effective than MOSFETs for implementing the differential pair. Bipolar transistors provide much larger transconductances for the same bias current, and this is important in two respects. Firstly, the differential pair must present a low impedance to the photodiode to ensure that it does not affect the frequency response of the overall preamplifier. Secondly, a low impedance is required to help prevent fluctuations in the photodiode bias voltage when a signal is present. With bipolar transistors, a sufficiently low impedance can be achieved with much less bias current, and this reduces the noise introduced by the tail current source, I_{tail}. The exponential voltage-to-current characteristic of bipolar transistors also helps to ensure that the photodiode bias voltage remains well regulated across a wide range of signal currents. In summary, the practical need for bipolar transistors makes the current steering technique unattractive for use in CMOS optical preamplifier designs.

The final technique uses a transimpedance amplifier that is capable of variable gain. Recall that the feedback resistor, R_f, is one of the major sources of noise, and that its noise current contribution is inversely proportional to its resistance. Thus for weak signals, a large R_f is desired to both minimize the noise and maximize the output signal. On the other hand, for strong signals, a small R_f is desired since the maximum input current is limited to V_{max}/R_f where V_{max} is maximum output of the amplifier before distortion. Therefore, by adapting R_f in accordance to the signal strength, we can increase the dynamic range without sacrificing sensitivity.

Unfortunately, variable-gain transimpedance amplifiers are challenging to implement because their stability is affected by changes to the feedback resistor. The BiCMOS implementation presented in [Meyer,1994] and shown in Figure 2.8a requires an additional dummy amplifier simply to generate a bias voltage and three *additional* variable resistors to ensure stability. Similarly, the design presented in [Khorramabadi,1995] and shown in Figure 2.8b requires two *additional* variable

resistors. In both designs, the additional variable resistors are heuristically fine tuned with no discernible tracking relationship with the main feedback resistor, making these circuits both difficult to design, and prone to modeling errors. These problems are further complicated for fully-differential implementations where the required number of variable resistors is doubled.

As discussed in the next chapter, part of the problem with these existing designs is their use of the traditional gain stage comprised of a common-emitter amplifier followed by an output buffer. The stability of the preamplifier can be greatly enhanced and preamplifier circuit significantly simplified by adopting a different topology for the gain stage. This thesis presents an alternative topology that requires only one additional variable resistor whose resistance linearly tracks the main feedback resistor. This simplified structure is used to realize a fully-differential variable-gain transimpedance amplifier whose stability depends only on the tracking of identical pairs of resistors. The bandwidth of the proposed preamplifier is also better controlled than those of the previously mentioned designs. Controlling the bandwidth improves sensitivity by rejecting out-of-band noise without the need for additional filtering. Although a constant-bandwidth, variable-transimpedance amplifier was presented in [Wilson,1997], experimental results for that work have yet to be reported.



a) [Meyer,1994] b) [Khorramabadi,1995]

Figure 2.8 Two existing variable-gain transimpedance amplifier designs.

2.3.2 Ambient Light Rejection

In an optical wireless link, the receiver must operate in the user environment, and must be able to detect signals even in the presence of strong ambient light. Ambient light affects a receiver by generating additional shot noise at the photodiode and by superimposing an additional light signal on top of the desired signal. The contribution of shot noise can be calculated with Equation (2.1) using the average current level of the ambient light. Additional shot noise reduces a receiver's sensitivity, but is unavoidable since the noise has a white spectrum and is added directly to the desired signal. In contrast, the ambient light signal itself can be electrically filtered if it is constant or varying at a much lower frequency than the desired signal. In situations where the desired signal is weak, the photocurrent generated by ambient light can overwhelm the signal. For instance, current IrDA standards specify a maximum ambient light level of $490\mu W/cm^2$ that is over a hundred times larger than the minimum signal intensity of $4\mu W/cm^2$ [IrDA,1997].

There are various sources of ambient light, both natural and artificial. For optical wireless receivers that typically use Si photodiodes, we are primarily interested in characterizing ambient light sources in the near infrared spectrum [Moreira,1997,1995]. Direct sunlight is the most intense source of ambient light with significant power in the infrared spectrum. However, its intensity varies slowly. Incandescent and fluorescent lamps are the two most common artificial light sources. Incandescent lamps also radiate significant power in the infrared spectrum. Since they are powered directly off the line voltage, their intensity is modulated at the power line frequency (i.e., 50Hz or 60Hz) and its higher harmonics. In contrast, fluorescent lamps driven by electronic ballasts emit relatively low levels of infrared light, but they produce periodic light fluctuations with significant harmonic components up to 1MHz [Moreira,1997], [Narasimhan,1996].

There are two main alternatives for rejecting ambient light at the preamplifier. One solution is to ac couple the photodiode to the preamplifier as shown in Figure 2.9a [Palojarvi,1997], [Ritter,1996], [Petri,1998]. Here the high-frequency signal

current, i_s, passes through, while the dc component, I_{dc}, is blocked and shunted away through resistor, R. This solution has two major drawbacks. Firstly, for monolithic implementations, large on-chip resistors and capacitors are required to achieve a sufficiently low high-pass cut-off frequency, and to minimize the noise contributed by the additional resistor. These passive elements occupy significant area and are sensitive to parasitic-coupled noise. Secondly, the bias voltage across the photodiode varies with the average photocurrent since the voltage at the anode is given by $I_{dc} \times R$. As a result, the overall receiver bandwidth is affected by the signal and ambient light levels.

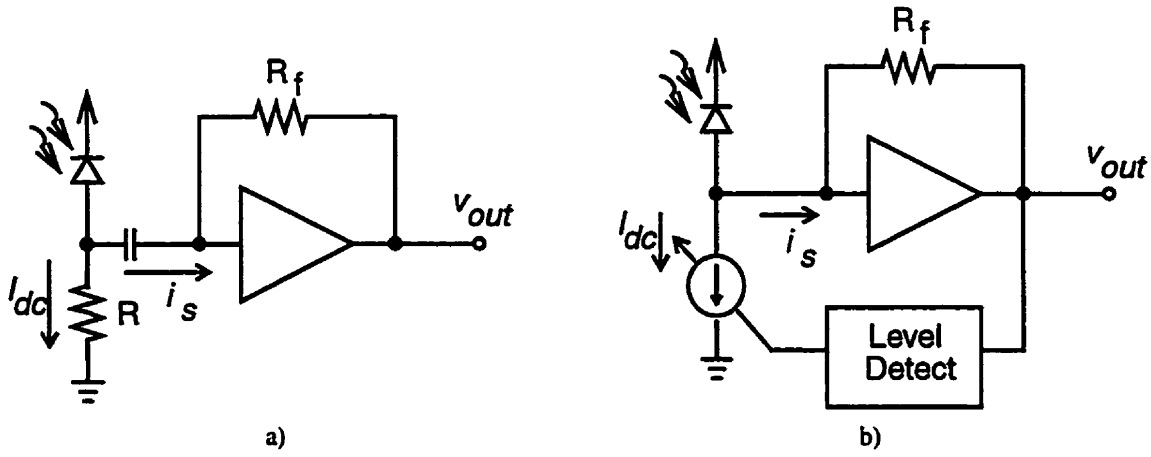


Figure 2.9 Ambient photocurrent rejection techniques: a) ac coupling, b) active feedback loop.

The alternative to a passive RC network is to use an active feedback loop around the transimpedance amplifier as shown in Figure 2.9b. Level detection based on the peaks of the signal is effective [Tanabe,1998], [Swartz,1993], but assumes that the average current is constant and requires a reset mechanism. An alternative is to use average level detection. Although this is essentially achieved in the preamplifier presented in [Brass,1994], the resulting dc rejection is more of a side effect of the biasing requirement of the preamplifier. This thesis presents an alternative structure in which the feedback loop does not impose constraints on the design of the transimpedance amplifier. The resulting ambient light rejection circuit requires less area and effectively regulates the photodiode bias voltage.

2.3.3 Low-Voltage Operation

As mentioned in Chapter 1, low-voltage operation has become a design requirement for many new applications of optical communications. The two main motivating factors are system integration, and lower power consumption, especially for portable applications [Neuteboom,1997], [van der Woerd,1992] and those requiring battery backup [Nakamura,1999], [Sackinger,1999]. Traditional fiber-optic systems have not had to deal with low supply voltages because they have largely been designed for performance rather than cost. As such, a good deal of work remains on the development of low-voltage optical transmitters and receivers.

For the transmitter, the challenges principally involve light generation and modulation. As supply voltages decrease, they will approach the forward-bias voltage required to turn on many of today's LEDs and laser diodes. New emitter designs, such as vertical cavity surface emitting lasers (VCSELs), are being developed especially for low-threshold operation [Sugimoto,1997], [Iga,1999], [Yang,1995]. In addition, the modulation of light to encode information is also a challenge, and novel techniques allowing high-speed modulation in spite of low voltages are currently under investigation [Shi,2000], [Qasaimeh,1997].

On the receiver end, the main challenges of low-voltage operation are a reduced signal swing that limits dynamic range, and a low photodiode bias voltage which lowers quantum efficiency and increases device capacitance. The preamplifier, in particular, must being able to maximize the photodiode reverse bias voltage while simultaneously maintaining a large signal swing. These are conflicting goals for many existing transimpedance amplifier designs as illustrated by the single-transistor amplifier shown in Figure 2.10. In Figure 2.10a, the anode of the photodiode drives the input of the amplifier. An optical pulse generates a photocurrent is that sourced into amplifier which converts it into a negative-going pulse at the amplifier's output. The maximum output voltage swing is given by $V_{GS} - V_{sat} = V_t$ where V_t is the threshold voltage of a MOSFET. For a typical 0.35μm CMOS process, the threshold voltage is about 0.6V, and so the swing represents about 60% of a

1V supply. Unfortunately, this large swing is achieved at the cost of a reduced bias on the photodiode. The bias voltage is $V_{DD} - V_{GS} \approx 0.2V$, or only about 20% of the supply voltage. The opposite problem is encountered when the transimpedance amplifier is driven from the cathode of the photodiode. To reverse bias the photodiode, the anode is now connected to ground. Here, the bias voltage on the photodiode has been increased to 0.8V. Unfortunately, the photocurrent is now sunk by the photodiode, resulting in positive going pulses at the amplifier's output. If we assume a minimum voltage drop across the bias current source of $V_{sat} \approx 0.1V$, the output swing is then limited to $V_{DD} - V_{sat} - V_{GS} \approx 0.1V$. In summary, many transimpedance amplifier designs couple the output swing and photodiode bias such that only one of the two can be made large.

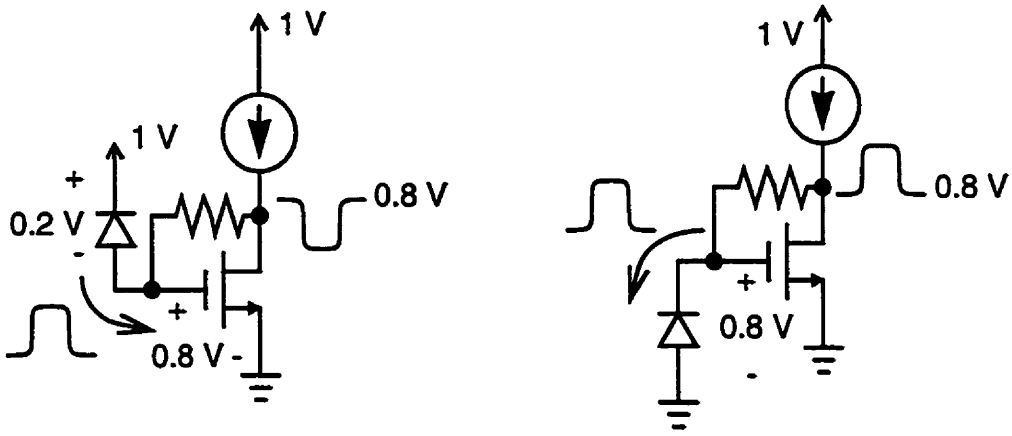


Figure 2.10 Two single-transistor transimpedance amplifiers: a) anode connected input, b) cathode connected input.

Few existing designs have tried to push below 2V operation where such issues become critical. To our best knowledge, only two sub-2V optical receivers have been reported [van der Woerd,1992], [Nakamura,1999]. The first design — intended for the programming of hearing aids — is limited to very low data rates, and cannot be compared with designs intended for high-speed communications. The second design, an integrated optical transmitter and receiver, achieves 1.2 V operation, but requires the use of low-threshold MOS transistors. We believe innovations at both

the device and circuit level will be required to ensure the long-term feasibility of low-voltage optical receivers. In this thesis, we present a 1V optical receiver front-end implemented in a standard CMOS process without low-threshold devices. The design incorporates both a novel transimpedance amplifier and a novel voltage doubler capable of accepting input levels below 1V. The feedback resistor is implemented using a MOSFET operating in the linear region, and the gate of the MOSFET is biased by the voltage doubler.

While the interest in low-voltage optical receivers has emerged quite recently, much work has already been done to develop low-voltage analog circuits. Innovations such as the switched-opamp [Steyaert,1993] and the nested-Miller compensation technique [You,1997] are good examples. One observation that applies to many low-voltage circuits is that they differ significantly from their traditional counterparts, and as such must be reanalyzed. Such was our experience with the low-voltage transimpedance amplifier, and it called upon us to further investigate alternative methods of circuit analysis which is the subject of the next section.

2.4 CIRCUIT ANALYSIS TECHNIQUES

Nodal and mesh analysis are the two traditional forms of linear circuit analysis. Each involves deriving a set of linear equations using Kirchhoff's Current (KCL) and Voltage (KVL) Laws [Bobrow,1987]. Other circuit analysis techniques specifically suited for analyzing feedback structures include topology-based feedback analysis and feedback analysis based upon return ratios.

Topology-based feedback analysis, as exemplified by [Sedra,1998], is performed by partitioning a feedback circuit into a forward amplifier and a feedback network as shown in Figure 2.11. This method requires us to identify the method used to sample the output and the method used to mix the feedback signal back to the input.

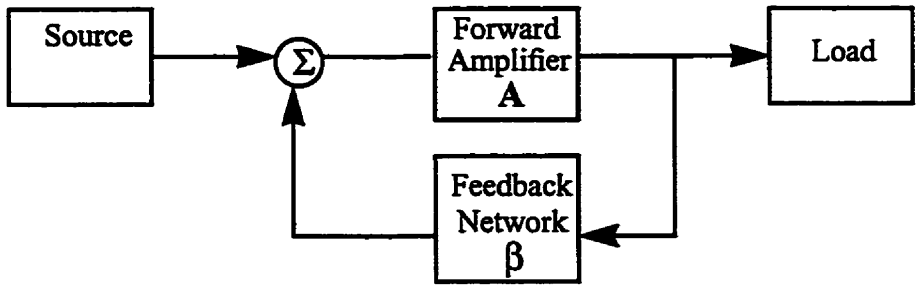


Figure 2.11 General structure of the feedback amplifier.

The alternative method of analyzing feedback circuits requires determining the *return ratio* of a dependent source in an active device found in the feedback circuit. The return ratio is then used to calculate quantities such as gain, and input and output impedance [Rosenstark,1986]. Originally outlined by Bode [Bode,1945], its main advantage over topology-based analysis is that it neither requires the partitioning of the amplifier into two distinct components nor requires the identification of the sampling and mixing mechanisms. If we consider the model of the feedback amplifier shown in Figure 2.12 in which the controlled source x_b represents, for instance, the transconductance of a transistor that is part of the internal feedback, the return ratio, T, can be defined by the following passage:

> *"The return ratio, T, with reference to controlled source x_b is defined as the negative of the variable x_a which is produced when the dependent source x_b is replaced by an independent source of the same nature and polarity but of strength k, all independent sources are set to zero and all other conditions in the system are left unchanged from their normal operating conditions."*[2]

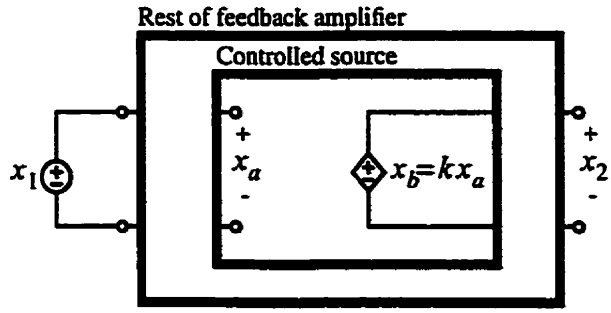


Figure 2.12 Feedback amplifier model [Rosenstark,1986].

2. [Rosenstark,1986], p. 12.

2.4.1 Transistor Feedback Amplifier: A Comparative Example

To illustrate and compare these three circuit analysis techniques, consider the two-stage feedback amplifier taken from [Rosenstark,1986][3] and shown in Figure 2.13. Assuming the transistors have a transconductance $g_m = 100mS$ and $\beta = 100$, let us determine the input and output resistance as well as the voltage gain of the amplifier.

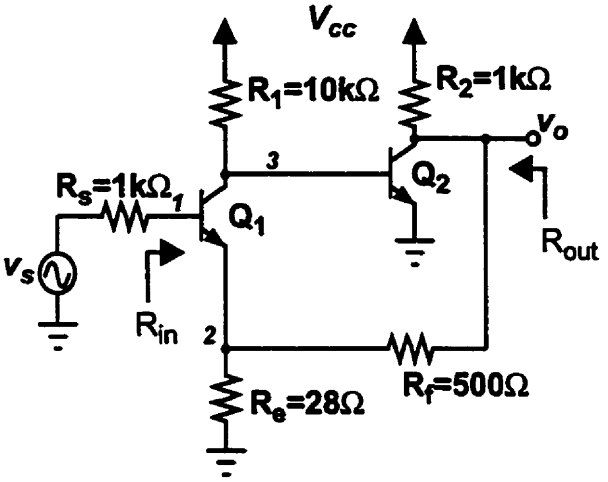


Figure 2.13 Two-stage amplifier with feedback.

Nodal Analysis

We proceed by deriving a small-signal circuit and determining a set of nodal equations using KCL at nodes 1, 2, 3, and v_o. The resulting relations can be expressed in the following state-space equation:

$$\boldsymbol{AX} + \boldsymbol{Bu} = \mathbf{0} \tag{2.4}$$

where

$$\boldsymbol{B} = \left[-1/R_s\ 0\ 0\ 0\right]^T = \left[-0.001\ 0\ 0\ 0\right]^T$$

$$\boldsymbol{X} = \left[v_1\ v_2\ v_3\ v_o\right]^T$$

$$u = v_s$$

3. Ibid, p. 13.

$$A = \begin{bmatrix} 1/R_s + 1/r_e - g_m & g_m - 1/r_e & 0 & 0 \\ -1/r_e & 1/r_e + 1/R_f + 1/R_E & 0 & -1/R_f \\ g_m & -g_m & 1/R_1 + 1/r_\pi & 0 \\ 0 & -1/R_f & g_m & 1/R_2 + 1/R_f \end{bmatrix}$$

$$= \begin{bmatrix} 0.002 & -0.001 & 0 & 0 \\ -0.101 & 0.1387 & 0 & -0.002 \\ 0.1 & -0.1 & 0.0011 & 0 \\ 0 & -0.002 & 0.1 & 0.003 \end{bmatrix}$$

For $v_s = 1V$, the solution is

$$X = -A^{-1}Bu = \begin{bmatrix} 0.9942 & 0.9883 & -0.5305 & 18.34 \end{bmatrix}^T$$

and the gain is simply the output voltage, or

$$Gain = v_0/v_s = 18.34.$$

The input resistance can be calculated indirectly using the expression

$$R_{in} = \frac{v_s}{i_s} - R_s = \frac{v_s}{(v_s - v_1)/R_s} - R_s = 170k\Omega$$

To determine the output resistance, we can inject a unit test current at the output and calculate the resulting output voltage. As such, matrix A and vector X remain unchanged but now

$$B = \begin{bmatrix} 0 & 0 & 0 & -1 \end{bmatrix}^T$$

$$u = i_{test}$$

By setting the test current to unity, the resulting solution is

$$X = \begin{bmatrix} 0.1069 & 0.2139 & 9.7213 & 9.4331 \end{bmatrix}^T$$

and the output resistance is

$$R_{out} = \frac{v_o}{i_{test}} = 9.43\Omega$$

Direct nodal analysis is mathematically exact and straightforward to solve with the aid of calculators or computers capable of matrix operations. However, notice that the solution required the substitution of numbers into the parameters; had we kept the parameters and performed a symbolic analysis of the circuit, the resulting expressions would have been very complex and far too cumbersome to provide much insight into the circuit's operation.

Topology-Based Feedback Analysis

Greater insight into the effect of feedback on this amplifier can be obtained using topology-based analysis. Although other interpretations are possible, the feedback amplifier in Figure 2.13 can be seen as series-shunt configuration in which the output voltage is sampled and then mixed back to the input as a voltage signal. Following the process outlined in [Sedra,1998], we can partition the circuit into a forward amplifier and feedback network as shown in Figure 2.14.

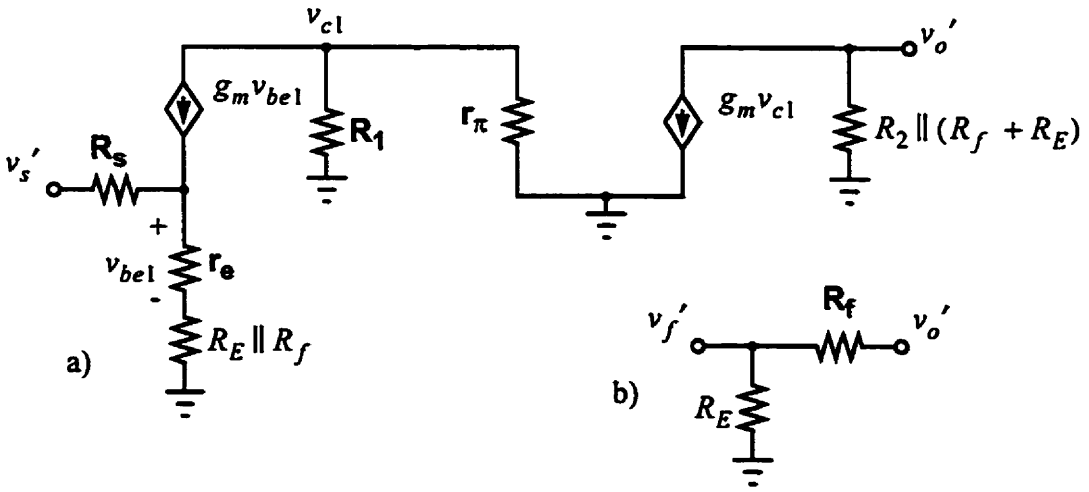


Figure 2.14 Topology-based feedback analysis: small-signal circuits for a) forward amplifier and b) feedback network.

The gain of the forward amplifier can be expressed as

$$A = \frac{v_o'}{v_s'} = \frac{v_o'}{v_{c1}} \times \frac{v_{c1}}{v_s'} \approx 671.6$$

where

$$\frac{v_o'}{v_{c1}} = -g_m \times R_2 \| (R_f + R_E)$$

$$\frac{v_{c1}}{v_s'} = -\alpha i_e (R_1 \| r_\pi) = \frac{(\beta + 1)(r_e + R_E \| R_f)}{R_s + (\beta + 1)(r_e + R_E \| R_f)} \times -\frac{\alpha (R_1 \| r_\pi)}{r_e + R_E \| R_f}$$

The feedback network, comprised of a simple resistor divider can be expressed as

$$\beta = \frac{R_E}{R_E + R_f} = 0.053$$

Thus the resulting loop gain is $A\beta = 671.6 \times 0.053 = 35.62$. To determine the closed-loop gain, we apply the standard closed-loop feedback expression

$$Gain = A_f = \frac{v_o}{v_i} = \frac{A}{1 + A\beta} = \frac{671.6}{1 + 35.62} = 18.34$$

The input resistance of the forward amplifier can be seen to be

$$\begin{aligned} R_{inA} &= R_s + (\beta + 1)(r_e + R_E \| R_f) \\ &= 1000 + 101 \times (9.9 + 28 \| 500)\Omega = 4.678k\Omega \end{aligned}$$

Although not immediately apparent, the source resistance R_s must be included when determining R_{inA} since the derivation of the feedback equation assumes that R_s is absorbed into the input resistance of the forward amplifier. The output resistance of the forward amplifier is

$$R_{outA} = R_2 \| (R_f + R_E) = 1000 \| (500 + 28)\Omega = 345.5\Omega$$

With the application of feedback, the input resistance is increased while the output resistance is decreased, both by a factor of $(1 + A\beta) = 36.62$. As such, the port

resistances of the feedback amplifier are

$$R_{in} = (1 + A\beta)R_{inA} - R_s = 36.62 \times 4678\Omega - 1k\Omega = 170k\Omega$$

$$R_{out} = \frac{R_{outA}}{1 + A\beta} = \frac{345.5}{36.6}\Omega = 9.43\Omega$$

and we arrive at the same results obtained using nodal analysis. In addition, however, we also gain some degree of insight into the role of feedback in this circuit, and have determined the loop gain to be a measure of the amount of feedback used in the circuit.

Unfortunately, there are numerous limitations with this technique. Firstly, we face the challenge of trying to make all circuits conform to the classical feedback structure. As such, this technique is limited to circuits with a single or dominant feedback loop. In addition, we must identify the topology that best reflects the feedback sampling and mixing mechanisms of the circuit. Often this is not apparent. For circuits that do not approximate the ideal feedback structure, all nonidealities such as loading effects must be accounted for by adding port parameters to the principle blocks. The values of these parameters are obtained through a process of modifying the original circuit and deriving various characteristics under short-circuit and open-circuit conditions. This process is involved and prone to mistakes. Lastly, this analysis implicitly assumes that both the forward amplifier and feedback network are unilateral. In other words, we assume that the signal traverses forward only through the amplifier and the output is fed back only through the feedback network. With many practical circuits, this is an assumption whose validity is difficult to ascertain, and should the underlying assumptions prove to be inaccurate, there is essentially no recourse. With this method, the accuracy of every analysis must be verified using exact analysis or computer simulation. As such, this method is not exact and is best thought of as an intuitive aid to understanding feedback circuits.

Feedback Analysis Using Return Ratios

The third method of analyzing the feedback amplifier uses return ratios. The entire solution is given in [Rosenstark,1986][4] so only a summary is presented here. To calculate the return ratio, the small-signal circuit is altered so that the original voltage dependent current source is replaced by an independent source, $x_b = \beta$, as shown in Figure 2.15. The return ratio, determined as the negative of x_a, is calculated to be $T = 34.9$. In addition, two characteristics called the asymptotic gain, $A_\infty = 18.9$, and the direct transmission gain, $A_o = 0.388$, are determined in order to apply the Asymptotic Gain Formula to find the actual closed-loop gain:

$$A_f = A_\infty \frac{T}{1+T} + \frac{A_o}{1+T} = 18.9 \times \frac{34.9}{35.9} + \frac{0.388}{35.9} = 18.4 \tag{2.5}$$

The input and output resistance are obtained using Blackman's Impedance Formula [Blackman,1943]. The formula states that a port impedance is given by

$$Z_{port} = \frac{v_{port}}{i_{port}} = Z^\circ \frac{1+T_{sc}}{1+T_{oc}} \tag{2.6}$$

where

- T_{sc} is the return ratio when the port in question is shorted to ground,
- T_{oc} is the return-ratio when the port in question is open-circuited, and
- Z° is the measured port impedance when the internal feedback is disabled.

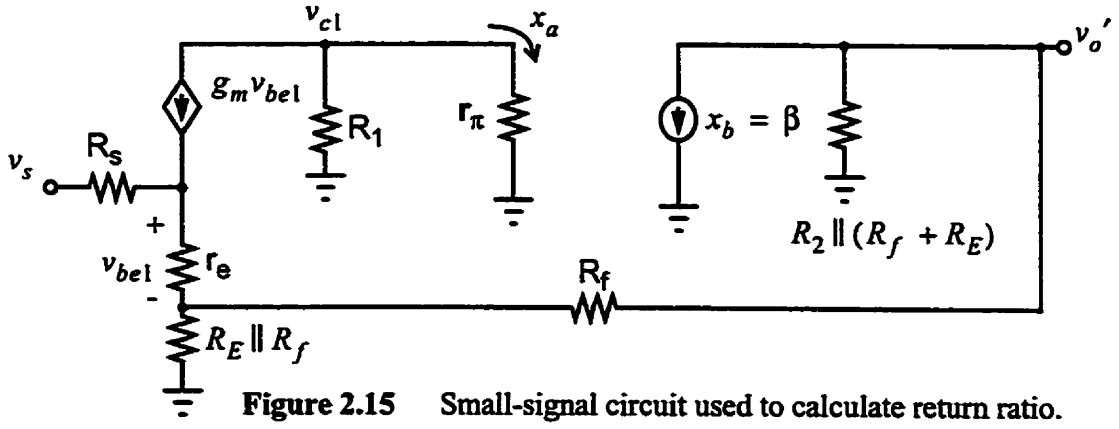


Figure 2.15 Small-signal circuit used to calculate return ratio.

4. Example 2.1, pp. 12-23.

In this circuit, the feedback can be disabled by setting the β of transistor Q_2 to zero. For the input port, we get the following results:

$$Z_{in}^{\circ} = 4.78k\Omega \qquad T_{sc} = T \qquad T_{oc} = 0$$

Thus, the final input impedance at dc is given by

$$Z_{in} = Z_{in}^{\circ} \times (1 + T_{sc}) = 4.78k\Omega \times (1 + 34.9) = 171k\Omega$$
$$\therefore R_{in} = 171k\Omega$$

For the output port, we get the following results:

$$Z_{out}^{\circ} = 338\Omega \qquad T_{sc} = 0 \qquad T_{oc} = T$$

The final output impedance at dc is given by

$$Z_{out} = Z_{out}^{\circ}/(1 + T_{oc}) = 338\Omega/(1 + 34.9) = 9.43\Omega$$
$$\therefore R_{out} = 9.43\Omega$$

As expected, the final analysis results are the same as those obtained with the other analysis methods. We see that similar to topology-based feedback analysis, analysis using return ratios also provides some insight into the effect of feedback on this circuit. The advantage here over topology-based analysis is that there is no need to partition the circuit, or to identify the feedback mixing and sampling mechanisms. Unfortunately, this analysis method still shares many of the same limitations. Both methods require breaking the internal feedback and analyzing modified versions of the circuit. Determining port impedances involves measuring a variety of port parameters under short-circuit and open-circuit conditions. This process is involved, not at all intuitive, and so prone to mistakes. The concept of a return ratio is also, at best, a difficult concept when applied to real circuits, as illustrated by the rather awkward definition given back on page 25, and as pointed out by Rosenstark himself:

> *"...it is very difficult to define the input or output impedance of a feedback amplifier if feedback is absent...[We acknowledge] the futility of attempting to model a feedback amplifier as a nonfeedback amplifier to which feedback has been added."*[5]

Although the return ratio of 34.9 is close to the loop gain of 35.6, the two values are not the same, and it is difficult to relate these quantities [Hurst,1992]. Finally, neither feedback analysis technique is suitable for analyzing circuits with multiple feedback loops or otherwise more complex feedback structures.

As our feedback amplifier example amply demonstrates, detailed circuit analysis is challenging even for relatively simple circuits. From the papers that are occasionally published and that attempt to present a clearer explanation of feedback [Hurst,1992], [Nikolic,1998], or an alternative means of analyzing circuits [Kelly,1970], [Ochoa,1998], [Davis,2000], there remains a general sense that there is still room for improving the way we analyze circuits. In Chapter 4, we develop and refine the DPI/SFG analysis method, a graphical circuit analysis technique that uses driving-point impedances (DPI) and signal-flow graphs (SFG). The technique requires no approximations, makes no assumptions, and is not limited to circuits with a single feedback loop. Because of its use of signal-flow graphs, the DPI/SFG method provides a designer with a visual representation of the circuit dynamics that enhances his or her insight into a circuit's operation. This characteristic is illustrated in the circuit examples in Chapter 4, and in Chapter 5 where the method is used in the analysis and design of a low-voltage transimpedance amplifier. In addition, Appendix A presents the analysis of the above transistor feedback amplifier using the DPI/SFG method, and compares the various circuit analysis techniques discussed in this thesis.

5. [Rosenstark, 1986], p. 23.

2.5 AN OVERVIEW OF SIGNAL-FLOW GRAPHS

Signal-flow graphs have long been used in many areas of engineering. Originally devised by Mason for linear networks [Mason,1953], they are a mainstay of network theory and are commonly applied to areas as diverse as automatic control and data communications. This section provides an overview of linear signal-flow graphs, largely for the benefit of today's reader who may not have had much exposure to network and graph theory. Much of the following material is derived from [Haykin,1970] and the reader is also referred to [Mason,1960] and [Chen, 1991 and 1997] for a more thorough treatment of this fascinating area.

A graph is a collection of points and lines, respectively referred to as *nodes* and *branches*. Each end of a branch is connected to a node and both ends of a branch may be connected to the same node. A signal-flow graph is a diagram which depicts the cause and effect relationship among a number of variables. The variables are represented by the nodes of the graph, while the connecting branches define the relationship. A typical signal-flow graph is shown in Figure 2.16. The figure has four nodes, each representing a node signal x_j. Between a pair of nodes j and k lies a branch with a quantity called the branch transmittance t_{jk}, represented here by the letters a to f.

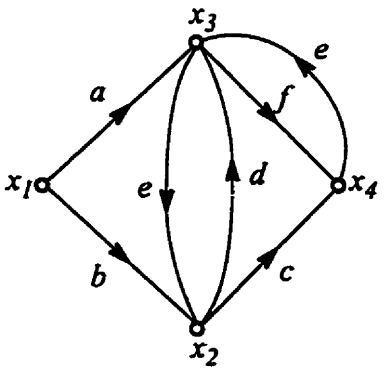


Figure 2.16 A linear signal-flow graph.

The flow of signals in the various parts of the graph is dictated by the following three basic rules which are illustrated in Figure 2.17:

1. Figure 2.17a: A signal flows along a branch only in the direction defined by the arrow and is multiplied by the transmittance of that branch.

2. Figure 2.17b: A node signal is equal to the algebraic sum of all signals entering the pertinent node via the incoming branches.

3. Figure 2.17c: The signal at a node is applied to each outgoing branch which originates from that node.

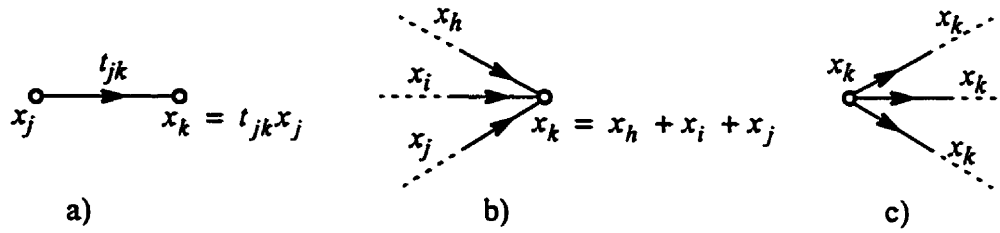


Figure 2.17 Illustrating three basic properties of signal-flow graphs.

From these basic rules are derived the four elementary equivalences shown in Figure 2.18 which guide one in the manipulation of signal-flow graphs. These equivalences are sufficient for the complete reduction of a graph containing no feedback loops. To handle graphs that incorporate feedback loops, there are two additional equivalence relations. Consider a self-loop in which a node signal is fed back to itself as illustrated on the left-hand side of Figure 2.19a. The signal-flow graph represents the relation

$$x_3 = x_2 = Lx_2 + x_1 \tag{2.7}$$

from which x_3 can be expressed exclusively in terms of x_1 as

$$x_3 = \frac{1}{1 - L}x_1 \tag{2.8}$$

and represented by the right-hand side of Figure 2.19a. Figure 2.19b illustrates the classic feedback structure comprised of a gain stage A, surrounded by a feedback

network β. The signal-flow graph represents the pair of equations

$$x_3 = Ax_2 \tag{2.9}$$

$$x_2 = \beta x_3 + kx_1 \tag{2.10}$$

from which we obtain the familiar expression

$$\frac{x_3}{x_1} = \frac{kA}{1 - A\beta} \tag{2.11}$$

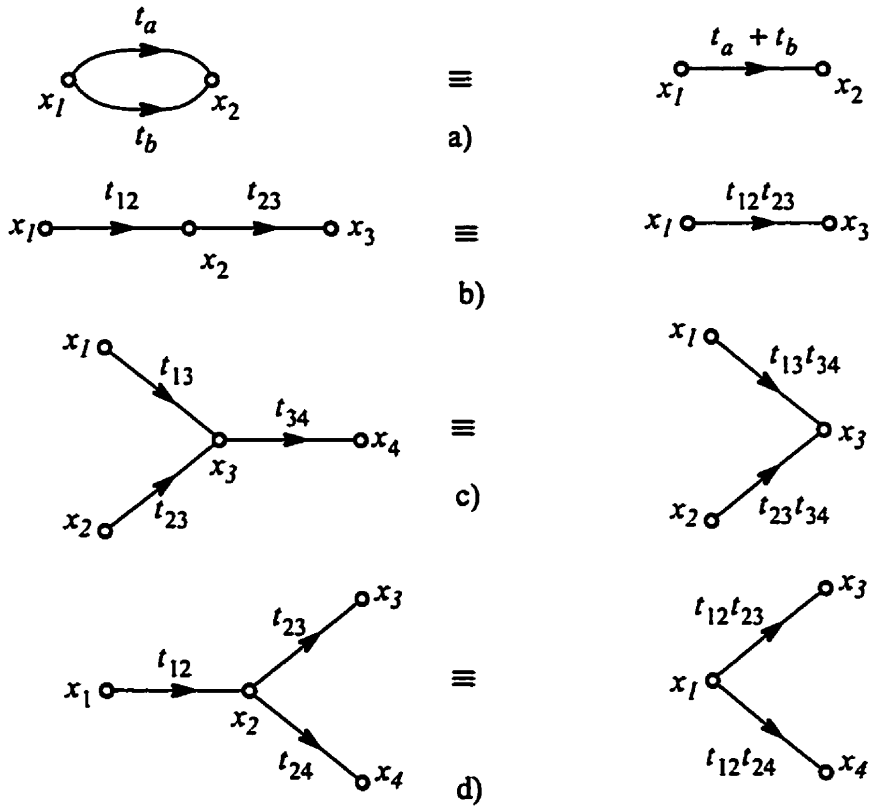


Figure 2.18 Four elementary equivalences of signal-flow graphs.

In contrast to Equations (2.8) and (2.11), most textbooks have a plus rather than minus sign, a result of adopting a convention whereby the feedback signal is subtracted rather than added back to the input node. Since the difference is only one of convention, we will continue with our existing convention in order to remain consistent with the signal-flow graph algebra. The quantities L and $A\beta$ are commonly known as the loop gain.

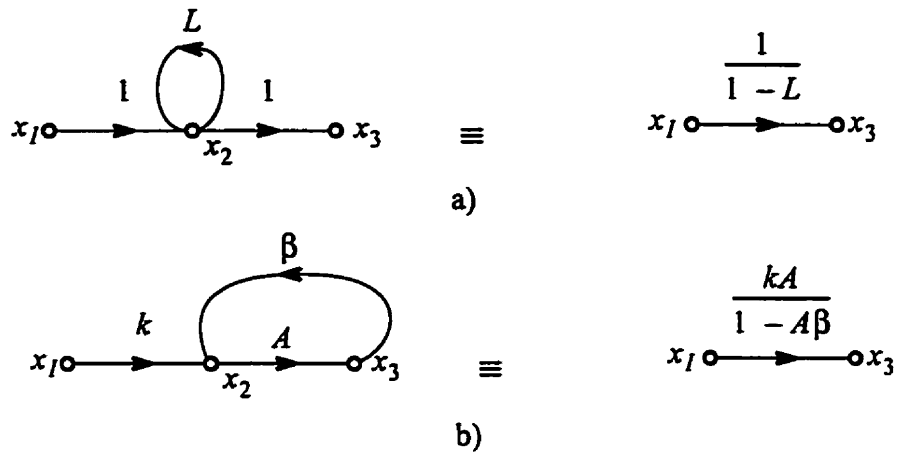


Figure 2.19 Collapsing feedback loops a) self-loop, b) general feedback loop.

By using the elementary equivalences in Figures 2.18 and 2.19, any transfer function can be derived from a signal-flow graph by successively collapsing internal nodes until only the input and output nodes remain. Figure 2.20 illustrates this process. The resulting transfer function is

$$\frac{x_{out}}{x_{in}} = \frac{abc}{1 - cd - bce}. \tag{2.12}$$

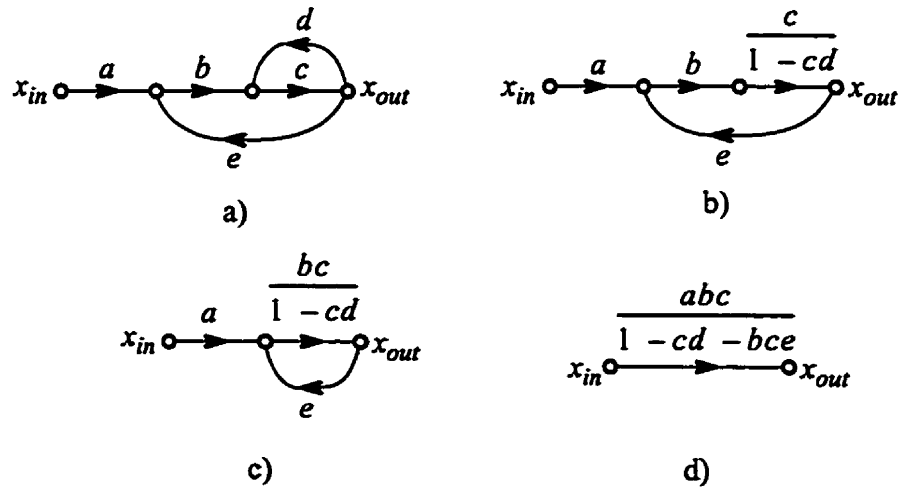


Figure 2.20 Determining a transfer function through collapsing of signal-flow graph.

2.5.1 Mason's Direct Rule

The manipulation of signal-flow graphs is an effective and straightforward means of determining transfer functions for relatively small graphs. However, such manipulations quickly become unwieldy for larger graphs, and for such situations the transfer function can be computed directly. Comparing Equation (2.12) to the original signal-flow graph in Figure 2.20a, we notice that the transfer function can be expressed as

$$\frac{x_{out}}{x_{in}} = \frac{P_1}{1 - (L_1 + L_2)} \tag{2.13}$$

where $P_1 = abc$ represents the forward transmission path from input to output, and $L_1 = cd$ and $L_2 = bce$ represent the loop gains of the two feedback loops found in the graph. In general, the transfer function of a signal-flow graph can be derived using the following expression, commonly known as Mason's Direct Rule [Mason,1960]:

$$\frac{x_{out}}{x_{in}} = \frac{1}{\Delta} \sum_{k=1}^{n} P_k \Delta_k \tag{2.14}$$

where

- P_k = transmittance of the kth forward path from input x_{in}, to output, x_{out}
- Δ = 1 - (sum of all individual loop gains)

  + (sum of loop gain products of all possible sets of nontouching loops taken two at a time)

  - (sum of loop gain products of all possible sets of nontouching loops taken three at a time)

  +...

and

- Δ_k = the value of Δ for that portion of the graph not touching the kth forward path.

2.6 SUMMARY

In this chapter, we discussed the photodetector and optical preamplifier that make up the front-end of an optical receiver. The transimpedance amplifier is the most common preamplifier structure, and we described the three principal new requirements that we wish to address in this thesis: a wide dynamic range, ambient light rejection, and low-voltage operation. In preparation for our discussion of a graphical circuit analysis technique, we reviewed existing analysis techniques such as nodal analysis, and feedback analysis based on amplifier topology and return ratios. In addition, we reviewed the basic conventions of signal-flow graphs and outlined Mason's Direct Rule.

REFERENCES

S. B. Alexander, *Optical Communication Receiver Design*, SPIE Optical Engineering Press, London, UK, Chapter 6, pp. 173-201, 1997.

J. R. Barry, *Wireless Infrared Communications*, Kluwer Academic Pub., Boston, Mass., Chapter 3, pp. 49-52, 1994.

R. B. Blackman, "Effect of Feedback on Impedance," *Bell System Tech. Journal*, vol. 22, pp. 269-277, Oct. 1943.

L. S. Bobrow, *Elementary Linear Circuit Analysis*, 2nd Ed., HRW Inc., New York, NY, 1987.

H. W. Bode, *Network Analysis and Feedback Amplifier Design*, Van Nostrand, New York, 1945.

E. Brass, U. Hilleringmann, and K. Schumacher, "System Integration of Optical Devices and Analog CMOS Amplifiers," *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 1006-1010, August 1994.

W. K. Chen, *Active Network Analysis*, World Scientific, Singapore, 1991.

W. K. Chen, *Graph Theory and Its Engineering Applications*, World Scientific, Singapore, 1997.

A. M. Davis, "Some Fundamental Topics in Introductory Circuit Analysis: A critique," *IEEE Trans.on Education*, vol. 43, no.3, pp. 330-335, August 2000.

S. S. Haykin, *Active Network Theory*, Addison-Wesley, Reading, Massachusetts, Chapter 10, 1970.

S. Hranilovic, *Modulation and Constrained Coding Techniques for Wireless Infrared Communication Channels*, Masters thesis, Dept. Elec. and Comp. Eng., Univ. of Toronto, Canada, 1999.

P. Hurst, "A Comparison of Two Approaches to Feedback Circuit Analysis," *IEEE Trans. Education*, vol. 35, no. 3, pp. 253-261, August 1992.

K. Iga, "Surface Emitting Lasers," *Electronics and Communications in Japan*, Part 2, vol. 82, no. 10, pp. 70-82, 1999.

Infrared Data Association (IrDA), *Serial Infrared Physical Layer Link Specification*, Version 1.2, http://www.irda.org, November 1997

R. D. Kelly, "Electronic Circuit Analysis and Design by Driving-Point Impedance Techniques," *IEEE Trans. on Education*, vol. E13, no. 3, pp. 154-167, Sept. 1970.

H. Khorramabadi, L. Tzeng, and M. Tarsia, "A 1.06 Gb/s -31 dBm to 0dBm BiCMOS Optical Preamplifier Featuring Adaptive Transimpedance," *IEEE ISSCC Digest of Tech. Papers*, pp. 54-55, February 1995.

H. Kressel (Editor), *Semiconductor Devices for Optical Communications*, 2nd Ed., Springer-Verlag, Berlin, Germany, 1982.

S. J. Mason, "Feedback Theory – Some properties of signal flow graphs," *Proc. IRE*, vol. 64, pp. 1144-1156, Sept. 1953.

S. J. Mason and H. J. Zimmermann, *Electronic Circuits, Signals and Systems*, J. Wiley and Sons Inc., New York, Chapter 5, 1960.

R. G. Meyer and W.D. Mack, "A Wideband Low-Noise Variable-Gain BiCMOS Transimpedance Amplifier," *IEEE J. Solid-State Circuits*, vol. 29, no. 6, pp. 701-706, June 1994.

S. E. Miller and I. P. Kaminow (Editors), *Optical Fiber Telecommunications II*, Academic Press, San Diego, 1988.

A. J. C. Moreira, R. T. Valadas, and A. M. de Oliveira Duarte, "Optical interference produced by artificial light," *Wireless Networks*, vol. 3, pp. 131-140, 1997.

A. J. C. Moreira, R. T. Valadas, and A. M. de Oliveira Duarte, "Characterization and Modelling of Artificial Light Interference in Optical Wireless Communication Systems," *IEEE Int. Symp. on Personal Indoor Mobile Radio Commun.*, vol. 1, pp. 326-331, September 1995.

T. V. Muoi, "Receiver Design for High-Speed Optical-Fiber Systems," *IEEE J. Lightwave Tech.*, vol. LT-2(3), pp. 243-267, June 1984.

M. Nakamura and N. Ishihara, "1.2V, 35mW CMOS optical transceiver ICs for 50Mbit/s burst-mode communication," *Electronic Letters*, vol. 35, no. 5, pp. 394-395, 4 March 1999.

R. Narasimhan, M. D. Audeh, J. M. Kahn, "Effect of electronic-ballast fluorescent lighting on wireless infrared links," *IEE Proc. Optoelectronics*, vol. 143, no. 6, pp. 347-354, December 1996.

H. Neuteboom, H. et al, "A single battery, 0.9 V operated digital sound processing IC including AD/DA and IR receiver with 2 mW power consumption," *IEEE ISSCC Dig. Tech. Papers*, pp. 98-99, February 1997.

B. Nikolic, S. Marjanovic, "A General Method of Feedback Amplifier Analysis," *IEEE Proc. Int.*

Symp. Circuits Systems, vol. 3, pp. 415-418, May 1998.

A. Ochoa, "A Systematic Approach to the Analysis of General and Feedback Circuits and Systems Using Signal Flow Graphs and Driving-Point Impedance," *IEEE Trans. Circ. and Syst. II*, vol. 45, no. 2, pp. 187-195, Feb. 1998.

K. Ohhata, T. Masuda, K. Imai, R. Takeyari, and K. Washio, "A Wide-Dynamic Range, High-Transimpedance Si Bipolar Preamplifier IC for 10-Gb/s Optical Fiber Links," *IEEE J. Solid-State Circuits*, vol. 34, no. 1, pp. 18-24, January 1999.

B. Owen, "PIN-GaAs FET optical receiver with a wide dynamic range," *Electronic Letters*, vol. 18, no. 14, pp. 626-627, 8 July 1982.

P. Palojarvi, T. Ruotsalainen, and J. Kostamovaara, "A Variable Gain Transimpedance Amplifier Channel with a Timing Discriminator for a Time-of-Flight Laser Radar," *Proc. European Solid-State Circuits Conf.*, pp. 384-387, September 1997.

S. D. Personick, "Receiver Design for Digital Fiber Optic Communications Systems, I and II," *Bell Syst. Tech. Journal*, vol. 52, no. 6, pp. 843-886, July-August, 1973.

S. D. Personick, *Fiber Optics, Technology, and Applications*, Plennum Press, New York, 1985.

C. Petri, S. Rocchi, and V. Vignoli, "High Dynamic CMOS preamplifiers for QW diodes," *Electronics Letters*, vol. 34, no.9, pp. 877-878, 30 April 1998.

O. Qasaimeh, S. Singh, P. Bhattacharya, "Electroabsorption and electrooptic effect in SiGe-Si quantum wells: realization of low-voltage optical modulators," *IEEE J. Quantum Electronics*, vol. 33, no. 9, pp. 1532-1536, September 1997.

S. Rosenstark, *Feedback Amplifier Principles*, Macmillan Publishing Co., New York, Chapter 2, 1986.

M. B. Ritter, F. Gfeller, W. Hirt, D. Rogers, and S. Gowda, "Circuit and System Challenges in IR Wireless Communication," *IEEE ISSCC Digest of Tech. Papers*, pp. 398-399, February 1996.

E. Sackinger, Y. Ota, T. J. Gabara, W. C. Fischer, "15mW, 155Mb/s CMOS Burst-Mode Laser Driver with Automatic Power Control and End-of-Life Detection," *IEEE ISSCC Dig. Tech. Papers*, pp. 386-387, February 1999.

A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 4th Ed., Oxford Univ. Press, New York, Chapter 8, 1998.

Y. Shi et al., "Low (sub-1-Volt) Halfwave Voltage Polymeric Electro-optic Modulators Achieved by Controlling Chromophore Shape," *Science*, vol. 288, pp. 119-122, 7 April 2000.

R. G. Smith and S. D. Personick, "Receiver design for optical fiber communication systems," in *Semiconductor Devices for Optical Communication*, 2nd Ed., H. Kressel, Ed., Chapter 4, pp. 89-160, Springer-Verlag, Berlin, Germany, 1982.

M. Steyaert, J. Crols, and S. Gogaert, "Switched-Opamp, a Technique for Realizing Full CMOS Switched-Capacitor Filters at Very Low Voltages," *Proc. Eur. Solid-State Circuits Conf.*, pp. 178-181, September 1993.

Y. Sugimoto and K. Kasahara, "Future Prospects of VCSELs: Industrial View," *Vertical Cavity Lasers, Tech. for a Global Information Infrastructure, 1997 Dig. IEEE/LEOS Summer Topical*

Meetings, pp. 7-8, August 1997.

R. G. Swartz, Y. Ota, M. J. Tarsia, and V. D. Archer, "A Burst Mode, Packet Receiver with Precision Reset and Automatic Dark Level Compensation for Optical Bus Communications," *Symp. on VLSI Technology*, Kyoto, Japan, pp. 67-68, May 1993.

A. Tanabe, M. Soda, Y. Nakahara, A. Furukawa, T. Tamura, and K. Yoshida, "A Single Chip 2.4 Gb/s CMOS Optical Receiver IC with Low Substrate Crosstalk Preamplifier," *IEEE ISSCC Digest of Tech. Papers*, pp. 304-305, February 1998.

L.A.D. van den Broeke, A.J. Niewkerk, "Wide-Band Integrated Optical Receiver with Improved Dynamic Range Using a Current Switch at the Input," *IEEE J. Solid-State Circuits*, vol. 28, no.7, pp. 862-864, July 1993.

A.C. van der Woerd, "Low-voltage low-power infra-red receiver for hearing aids," *Electronics Letters*, vol. 28 no. 4, pp. 396-398, 13 February 1992.

B. Wilson and J. D. Drew, "Novel Transimpedance Amplifier Formulation Exhibiting Gain-Bandwidth Independence," *IEEE Proc. Int. Symp. Circuits and Systems*, vol. 1, pp. 169-172, June 1997.

D. Yamazaki et al., "156Mbit/s preamplifier IC with wide dynamic range for ATM-PON application," *Electronic Letters*, vol. 33, no. 15, pp. 1308-1309, 17 July 1997.

G. M. Yang, M. H. Macdougal, and P. D. Dapkus, "Ultralow threshold vertical cavity surface emitting lasers obtained with selective oxidation," *Electronic Letters*, vol. 31, no. 11, pp. 886-888, 25 May 1995.

F. You, S. H. K. Embabi, and E. Sanchez-Sinencio, "Multistage Amplifier Topologies with Nested Gm-C Compensation," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2000-2011, December 1997.

CHAPTER

3 New Transimpedance Amplifier Structures

In this chapter, we develop a number of transimpedance amplifier structures to address the three principal design requirements outlined in Chapter 2: wide dynamic range, ambient light rejection, and low-voltage operation. We begin by describing a fully-differential, variable-gain, transimpedance amplifier with improved stability compared with reported designs. Next, we present a general feedback structure for rejecting ambient light. Finally, we develop a novel topology for a low-voltage transimpedance amplifier. In the process, we introduce a technique called dynamic gate biasing that is used in the low-voltage amplifier. Throughout this chapter, we will present simulation results of the proposed designs.

3.1 A DIFFERENTIAL TRANSIMPEDANCE AMPLIFIER WITH WIDE DYNAMIC RANGE

As mentioned in the previous chapter, reported variable-gain transimpedance amplifiers are difficult to stabilize [Meyer,1994], [Khorramabadi,1995]. The key problem with these designs is that they are based on the traditional two-stage topology consisting of a common-source gain stage followed by an output buffer. By adopting a different topology for the gain stage, the stability of the preamplifier can be greatly enhanced and preamplifier circuit significantly simplified.

Figure 3.1 shows the proposed structure together with the traditional topology. The main difference is the shunt feedback second stage that is used in place of the source follower. The proposed structure was originally presented by Hullett and Moustakas for fixed-gain transimpedance amplifiers [Hullett,1981]. The structure adopts a transconductance-transimpedance gain stage [Cherry,1963], [Cherry,1968] with an additional output stage that provides small-signal inversion to achieve negative feedback. The open-loop voltage gain of the amplifier is,

$$A = -\left(\frac{v_{out}}{i_o} \times \frac{i_o}{v_{in}} \times -1\right) \approx g_{m1} R_1 \tag{3.1}$$

which is typically in the range of ten to a few hundred. Coincidentally, the same expression is obtained for the traditional design assuming the output source follower has unity gain.

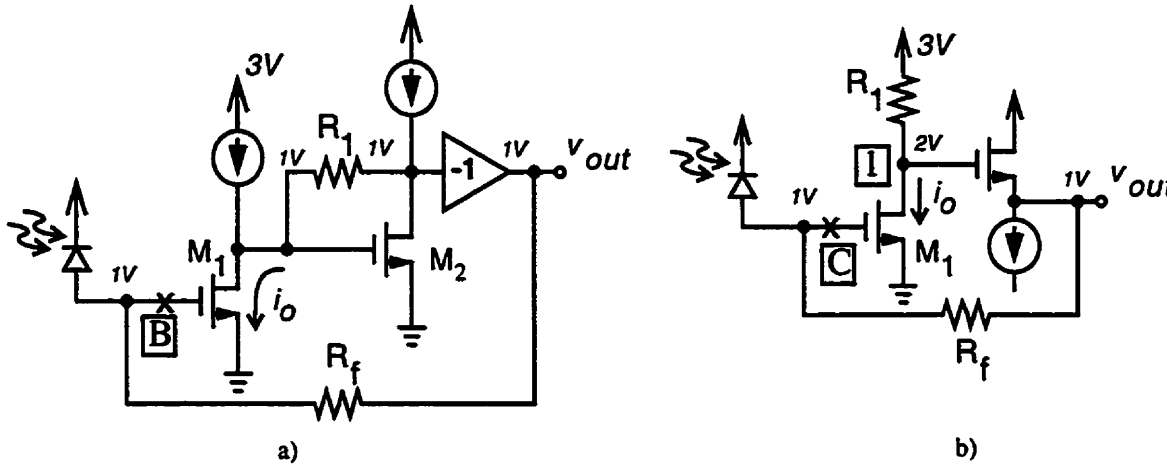


Figure 3.1 Two transimpedance amplifiers: a) proposed (local shunt feedback), b) traditional.

The stability of these circuits can be analyzed by breaking their feedback loops at points B and C. Figure 3.2 shows the main features of the loop gain for both circuits. The frequency where the loop gain of the transimpedance amplifiers is unity is approximately

$$\omega_t \approx \frac{A}{R_f C_{PD}} \approx \frac{g_{m1} R_1}{R_f C_{PD}} \tag{3.2}$$

where C_{PD} is the photodiode capacitance. The stability of the amplifiers is determined by the relative position of ω_t to the non-dominant pole, ω_{p2}. From Equation (3.2), we see that ω_t increases when R_f is reduced. In contrast, we can assume the non-dominant pole is not significantly affected by R_f. High-frequency gain peaking occurs when ω_t comes too close to ω_{p2}. To prevent this, the unity-gain fre-

quency should track changes in R_f. Specifically, if resistor R_1 could track R_f, ω_t would remain constant and stability would be maintained. In addition, since the closed-loop bandwidths of the transimpedance amplifiers are approximately equal to the unity-gain frequency,

$$BW \approx \frac{1+A}{R_f C_{PD}} \approx \frac{g_{m1} R_1}{R_f C_{PD}} \approx \omega_t \tag{3.3}$$

by having R_1 track R_f, we ideally also achieve a bandwidth that is constant and independent of the transimpedance gain.

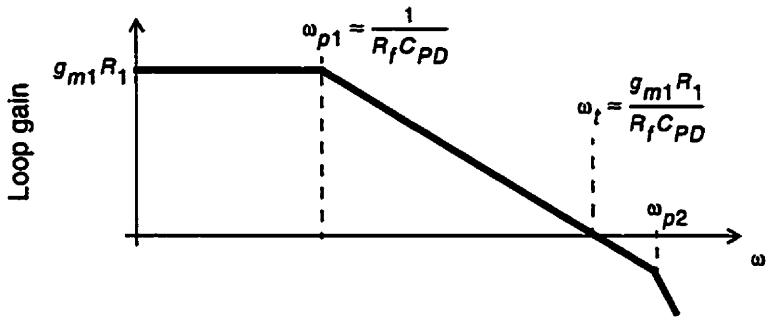


Figure 3.2 Frequency plot of loop gain for both transimpedance amplifiers.

In summary, adapting either transimpedance amplifier for variable gain requires the tracking of resistors R_1 and R_f. The difficulty in meeting this tracking requirement is the key difference between the two structures. Tracking is difficult in the traditional topology for a number of reasons. First, as we can see from Figure 3.1b, the terminal voltages of R_1 and R_f are very different. Given a low supply voltage, these resistors will likely be realized with different MOSFET types to ensure that the transistors remain in triode operation: R_1, biased close to Vdd, requires a p-channel device while R_f, biased closer to ground, requires an n-channel device. Getting MOS resistors to track when one is n-type and the other is p-type is inherently challenging. Secondly, there is a voltage drop across R_1 that is not present across R_f. The voltage drop occurs because R_1 is responsible for supplying the bias current of M_1. As a result, R_1 is always closer to saturation than R_f, making tracking especially difficult when the signals are large. As a result, the existing

designs based on this topology introduce a source-degeneration resistor for M_1 whenever handling large signals in order to maintain stability. The voltage drop across R_1 also implies that changing R_1 changes the bias voltage on node 1. The amplifier reported in [Meyer,1994] attempts to solve this by leaving the original R_1 fixed, and by adding another variable resistor with one terminal connected to node 1 and the other terminal connected to the equivalent node of a dummy transimpedance amplifier that is required simply in order to recreate node 1's bias voltage.

The problems involved in tracking R_1 and R_f are avoided with the proposed design because R_1 is now placed in a shunt configuration much in the same way as R_f. As illustrated in Figure 3.1a, the resistors have essentially identical terminal voltages, with one terminal biased at $V_{GS1,2}$ and the other terminal connected to the output. Thus, both resistors can be implemented using the same type of MOSFET. The problem of a fixed voltage drop across R_1 is eliminated because neither resistor handles any bias current. This structure also nicely accounts for any nonlinearities in R_1 and R_f; in large signal conditions when the MOSFETs approach saturation, they do so in conjunction and tracking is maintained.[1] This characteristic suggests that the structure is equally well suited for limiting amplifier designs that use nonlinear feedback elements to achieve clamping. Although R_1 and R_f can be designed to track to any fixed ratio, we can simplify the design by making R_1 and R_f equal.

Optimizing the bandwidth requires an analysis of the proposed amplifier. A small-signal model is shown in Figure 3.3 where C_f is the shunt feedback capacitance across the gate and drain of M_2, and C_i and C_o are the total capacitances at the internal node and output node respectively.

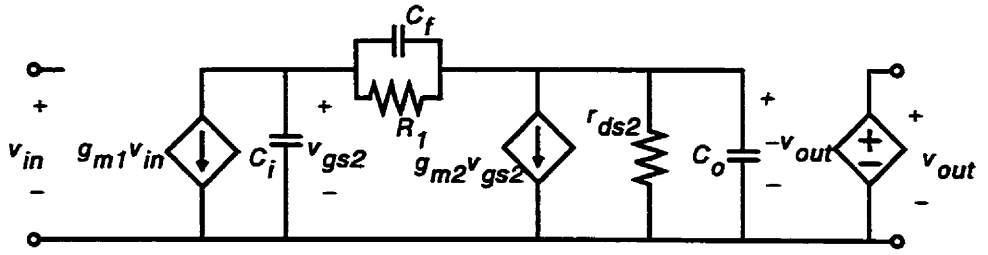


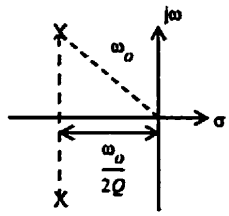
Figure 3.3 Small-signal model of three-stage amplifier.

1. Strictly speaking, this is only true of the final differential structure in which the inverting third stage is eliminated.

Because of the presence of the two capacitors, C_i and C_o, the second stage exhibits a second-order response. Assuming $g_{m2} \gg 1/r_{ds2}$ and $1/R_1$, and $C_f \ll C_i$ and C_o, the frequency response is approximately

$$A(s) \equiv \frac{v_{out}}{v_{in}}(s) \approx -\frac{g_{m1}}{C_i C_o} \times \frac{sC_f + (1/R_1 - g_{m2})}{s^2 + \frac{g_{m2}C_f}{C_i C_o}s + \frac{g_{m2}}{C_i C_o R_1}} \tag{3.4}$$

By tuning C_f, we can make the poles of this transfer function complex, resulting in the following design equations:



$$\omega_o \approx \sqrt{\frac{g_{m2}}{C_o C_i R_1}} \tag{3.5}$$

$$Q \approx \frac{1}{C_f}\sqrt{\frac{C_o C_i}{g_{m2} R_1}} \tag{3.6}$$

There are many ways to approach the design of this circuit. Typically, a variable-gain transimpedance amplifier is optimized at its maximum gain setting for a desired bandwidth, and at lower gain settings only the stability of the circuit needs to be confirmed [Meyer,1994]. We can begin with the design of the second stage. For a given bandwidth — which, as shown earlier, is essentially equal to ω_t — we can determine the maximum value of R_1 using Equation (3.5) by estimating the values of g_{m2}, C_i, and C_o based on device geometry and power dissipation, and by choosing a non-dominant pole frequency, ω_o, sufficiently higher than ω_t (a reasonable choice is $\omega_o \approx 2\omega_t$). Equation (3.6) can then be used to find the value of C_f corresponding to the desired Q-factor. A Q-factor of $1/\sqrt{2} = 0.71$ was selected to achieve a maximally-flat response [Sedra,1997] for the internal second-stage transimpedance amplifiers. Given the photodiode capacitance, C_{PD}, and estimating g_{m1}, Equation (3.2) then determines the maximum value of R_f.

The differential version of the variable-gain transimpedance amplifier is shown in Figure 3.4. Compared to the single-ended version in Figure 3.1a, the transconductance first stage is now realized using a p-channel differential pair. This allows

the input transistors to be placed in an isolated n-well to reduce substrate noise at the cost of slightly greater thermal noise [Johns,1997]. Devices M_5 and M_6 operate single-endedly, biasing each output at around 1V, and eliminating the need for common-mode feedback. The inverting buffer required in the single-ended design is eliminated in the differential version. Instead, small-signal inversion is accomplished by simply cross-coupling the differential outputs [Coppoolse,1996]. The maximum signal current is determined by the tail current of the input differential pair. This is because the differential signal current that passes through $R_{fa,b}$ is essentially mirrored to the internal current, i_o, that passes through $R_{1a,b}$. Current i_o is supplied by the differential pair and so is limited to half the tail current.

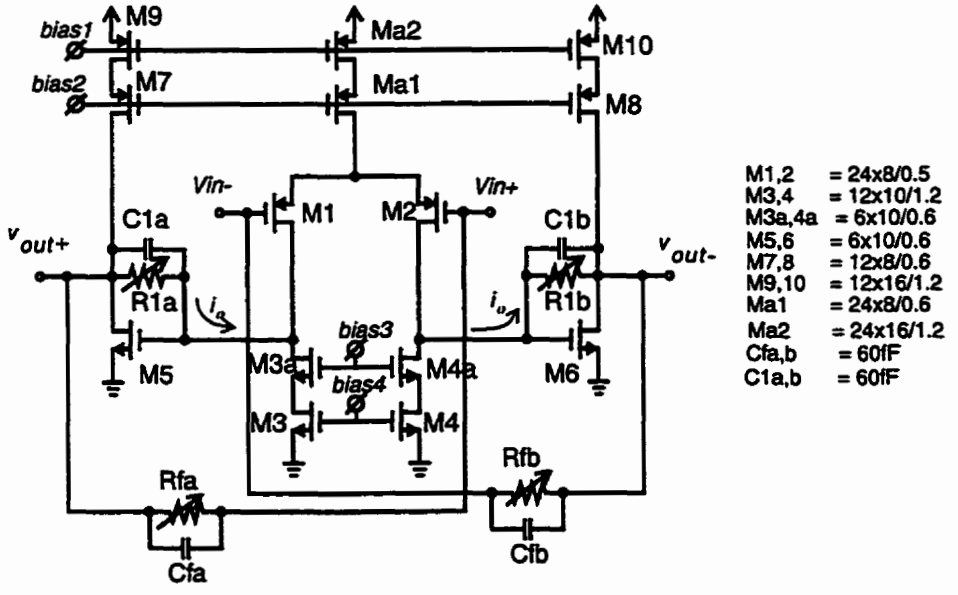


Figure 3.4 Fully-differential CMOS variable-gain transimpedance amplifier.

The transimpedance amplifier is designed to provide a maximum gain of 20 kΩ over a 70 MHz bandwidth. We assume an input capacitance of 5 pF which is typical of large photodiodes used in optical wireless receivers. Device models for a 0.35μm CMOS process were used, and the final transistor dimensions are shown in Figure 3.4. Using a transistor excess noise factor of 2/3 [Abidi,1986], the total simulated input-referred noise current of this amplifier at its maximum gain is 44nA, which over a bandwidth of 70MHz, represents an average noise current density of $5.3\,pA/\sqrt{Hz}$. A detailed noise analysis of this circuit is presented in [Hullett,1981].

In order to keep the power dissipation below 10 mW, we limit the tail current of the transimpedance amplifier's input differential pair to 800 μA. This sets the maximum input current to 400 μA. If we define the dynamic range of the amplifier as the ratio of the 44nA noise floor obtained at its maximum sensitivity, to its maximum input current of 400μA, this preamplifier has a dynamic range of 79.2 dB (electrical) or 39.6 dB (optical).

With a transimpedance gain of 500Ω, a 400 μA current produces a 200 mV output voltage. Hence, the variable-transimpedance amplifier is designed to provide gains from 20 kΩ (86 dBΩ) down to 500 Ω (54 dBΩ), representing a gain range of 32 dB. The simulation results shown in Figure 3.5 were obtained using the pass transistor arrays described below. The results verify that the frequency response of the amplifier is well behaved across the gain range. The simulated bandwidth is also well regulated, varying only within a factor of two (i.e., from 68 MHz to 130MHz) while the gain varies by a factor of 40 (32dB). The drop in bandwidth at the lowest gain setting can be attributed to the increased significance of g_{m5} and g_{m6} on the transimpedance gain of the internal second-stages. Strictly speaking, the transimpedance gain of these stages is proportional to $(1/g_{m5,6} - R_{fa,b})$, and not simply $-R_{fa,b}$ as assumed in the earlier discussion of the loop gain.

The four variable resistors of the transimpedance amplifier are identical. In order to realize the desired gain range, each resistor is comprised of three pairs of pass transistors as illustrated in Figure 3.6a. Each pass transistor can either be turned off or set to one of two resistance values by controlling the gate bias voltages as shown in the inset of Figure 3.6b. With three differently scaled pass transistors, each having three settings, the digitally-controlled pass-transistor array has the ability to realize $3^3 = 27$ different resistance values. In order to maximize linearity, complementary n- and p-channel MOSFETs are used, and the n-wells of the p-channel devices are tied to the output of the array to eliminate the body effect. A penalty in speed of about 40% is incurred as a result of the added capacitance due to the n-wells. Simulations show that the variable resistor remains within ±10 % of its nominal value for voltage drops within $\pm 0.3V$.

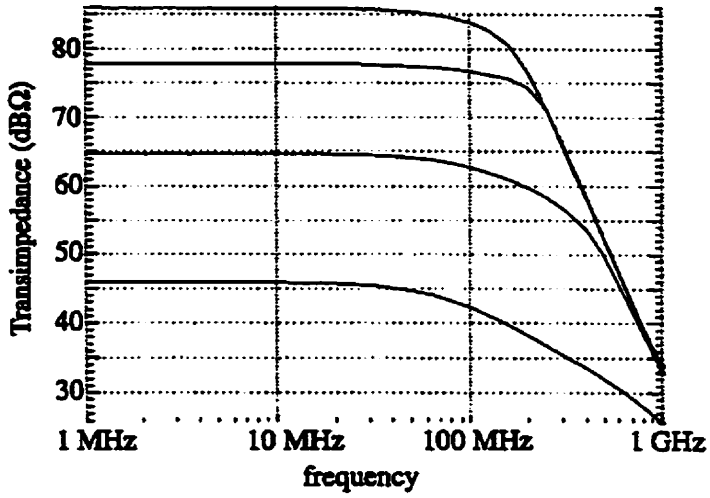


Figure 3.5 Simulated frequency response of variable-gain transimpedance amplifier.

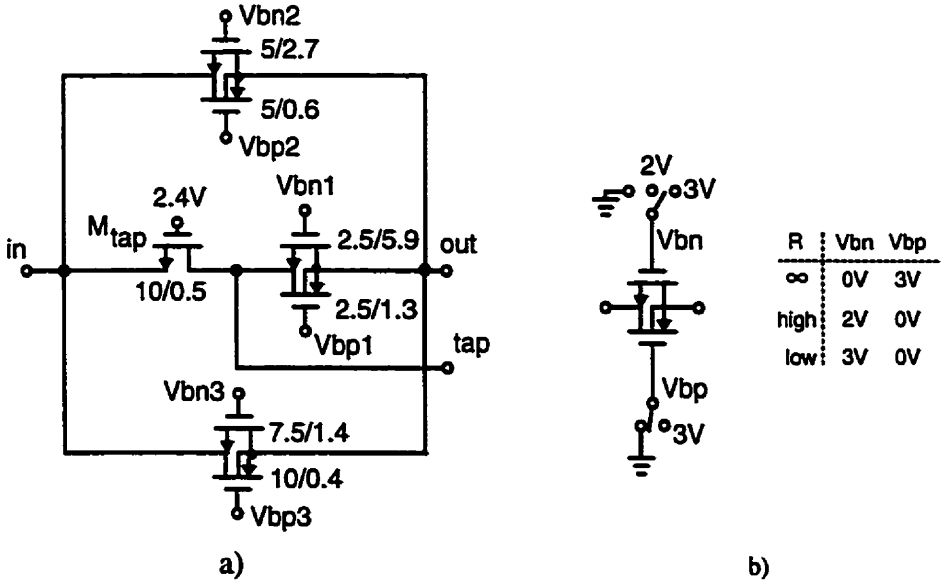


Figure 3.6 a) Pass-transistor array used to implement variable resistor, b) detail of pass transistor.

3.2 A FEEDBACK TOPOLOGY FOR AMBIENT LIGHT REJECTION

As described in Chapter 2 on page 20, photocurrent due to ambient light can be rejected at the preamplifier stage by placing a feedback loop around the transimpedance amplifier. The proposed structure is shown in Figure 3.7 where the outer feedback loop is comprised of an error amplifier and transistor, M_{ctl}. The rejection circuit operates as follows: the dc component of the photocurrent produces an offset in the average levels of the differential outputs as illustrated in Figure 3.8a. This offset is integrated over time by the error amplifier. Transistor M_{ctl} acts as a variable current sink which, at steady-state, draws the average photocurrent, I_{dc}, away from the signal path as shown in Figure 3.8b. The average photocurrent consists of the ambient photocurrent and the dc component of the signal.

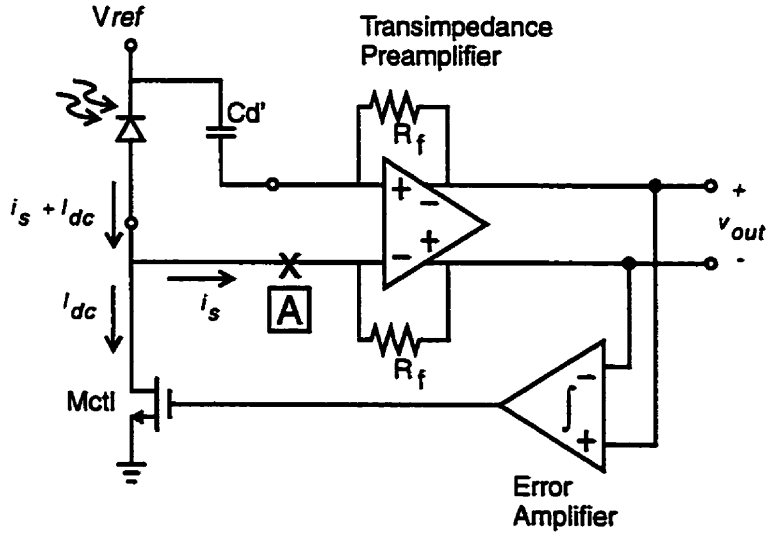


Figure 3.7 Optical preamplifier with ambient photocurrent rejection.

Using a differential signal path helps maximize the preamplifier's immunity to noise from the power supply and substrate. The photodiode, however, is connected to only one terminal. This creates an asymmetry at the input of the differential structure. As a result, an additional capacitor C_d', shown in Figure 3.7, is required at the other input of the transimpedance amplifier in order to match the photodiode capacitance and to rebalance the circuit. Perfect matching ensures that noise injected at the bias voltage, V_{ref}, appears as a common-mode signal that is effectively rejected

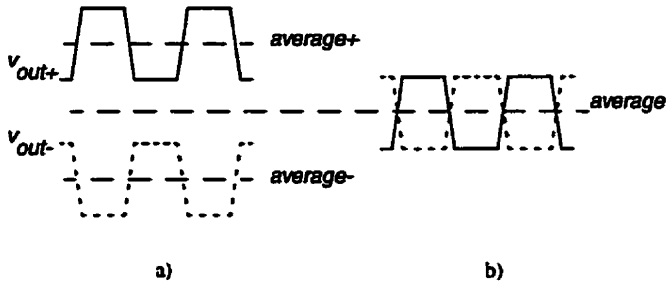


Figure 3.8 Differential output waveforms a) without ambient photocurrent rejection, b) with rejection.

by the differential structure. In practice, however, some mismatch can be expected, and additional measures such as adding an on-chip tuning capacitor [Yoon,1997] may be required to improve matching. Another solution is to use the differential topology presented in [Zand,1999] that altogether eliminates the need for the dummy capacitor.

The characteristics of the ambient photocurrent rejection circuit can be studied by breaking the loop at point A in Figure 3.7. The loop gain is given by

$$L(s) = A_{TIA}(s) \times A_{err}(s) \times g_{mctl} \tag{3.7}$$

where $A_{TIA}(s)$ and $A_{err}(s)$ are the frequency responses of the transimpedance amplifier (TIA) and error amplifier respectively, and g_{mctl} is the transconductance of M_{ctl}. Since the error amplifier acts as an integrator, in the ideal case its frequency response is given by

$$A_{err}(s) = \omega_{Terr}/s \tag{3.8}$$

where ω_{Terr} is the unity-gain frequency of the error amplifier. The resulting closed-loop response of the feedback structure is

$$\frac{v_{out}}{i_s}(s) = \frac{A_{TIA}(s)}{1 + L(s)} \approx A_{TIA}(s) \times \frac{s}{1 + s/\omega_{HP}} \tag{3.9}$$

where

$$\omega_{HP} = A_{\mathrm{TIA}}(0) \times \omega_{Terr} \times g_{mctl}$$

From Equation (3.9), we see that the frequency response of the feedback structure is essentially that of the original transimpedance amplifier, $A_{TIA}(s)$, with an additional high-pass filter with cut-off frequency ω_{HP}.

The analysis above assumes that the error amplifier is an ideal integrator. In reality, the error amplifier will have both a finite dc gain and additional high-frequency poles. The finite gain places a limit on the attenuation of the ambient photocurrent. However, this is not a major concern since the ambient photocurrent only needs to be attenuated enough so as to not saturate the preamplifier. The high-frequency poles of the error amplifier, in contrast, are a concern because they affect the stability of the feedback structure.

Nyquist's stability criteria requires that the loop gain of this structure, given by Equation (3.7), must have a magnitude less than unity when the phase equals $180°$. This condition implies an upper limit on the value of g_{mctl} that is related to the maximum transimpedance gain. In addition, the error amplifier should be designed so that its high-frequency poles are located significantly beyond those of the transimpedance amplifier in order to not affect the passband response.

The error amplifier was designed using a common two-stage CMOS opamp topology [Johns,1997] and is shown in Figure 3.9. The large bias current at the output stage was required to move the non-dominant poles to a sufficiently high frequency. Pole-splitting and lead compensation through transistor M_{comp} and a substantial 5 pF capacitor also helped ensure stability. The optimized circuit has a dc gain of 94 dB and a dominant pole at 150 Hz, and its open-loop response is shown in Figure 3.10 for various compensation resistor values.

Returning to the issue of an upper bound for transconductance g_{mctl}, since transistor M_{ctl} is biased by current I_{dc}, g_{mctl} is proportional to the square root of I_{dc}. This leads to the interesting observation that the preamplifier's high-pass cut-off frequency is a function of the average photocurrent. This relationship can be seen in the simulated frequency response shown in Figure 3.11 for different average photocurrents from 5 μA down to 5 nA.

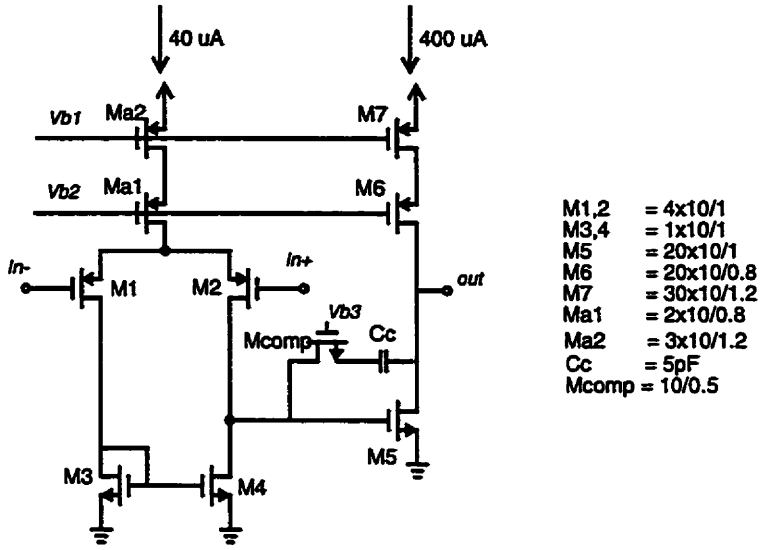


Figure 3.9 Error amplifier circuit.

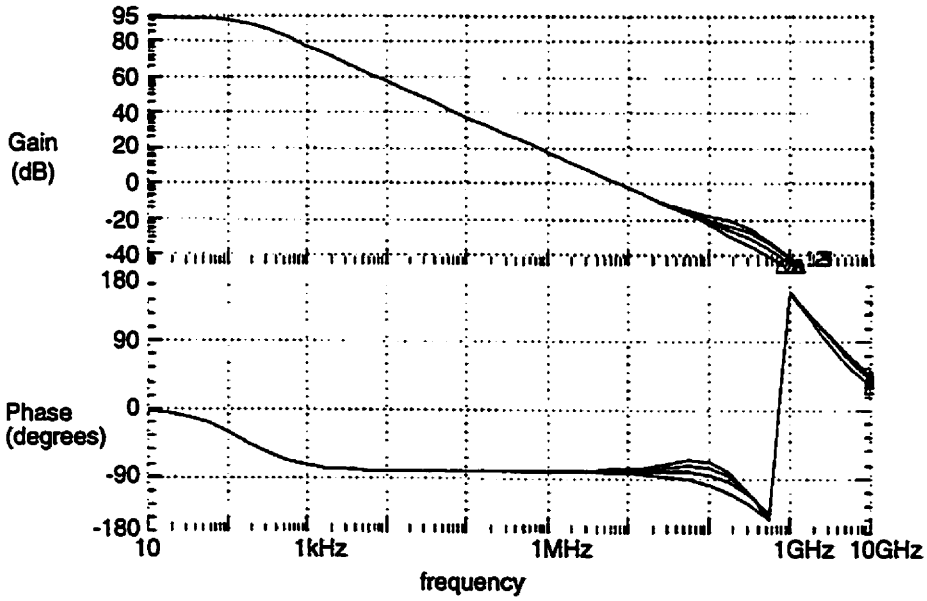


Figure 3.10 Simulated open-loop gain of error amplifier.

Understanding the implications of this dependency on I_{dc} is easier when we consider the signal and ambient light sources separately. The most critical situation occurs when the ambient light overpowers the signal. Here I_{dc} is essentially the photocurrent due to the ambient light. From Figure 3.11, we can conclude that the feedback loop is self-regulating in this case, becoming more effective at rejecting

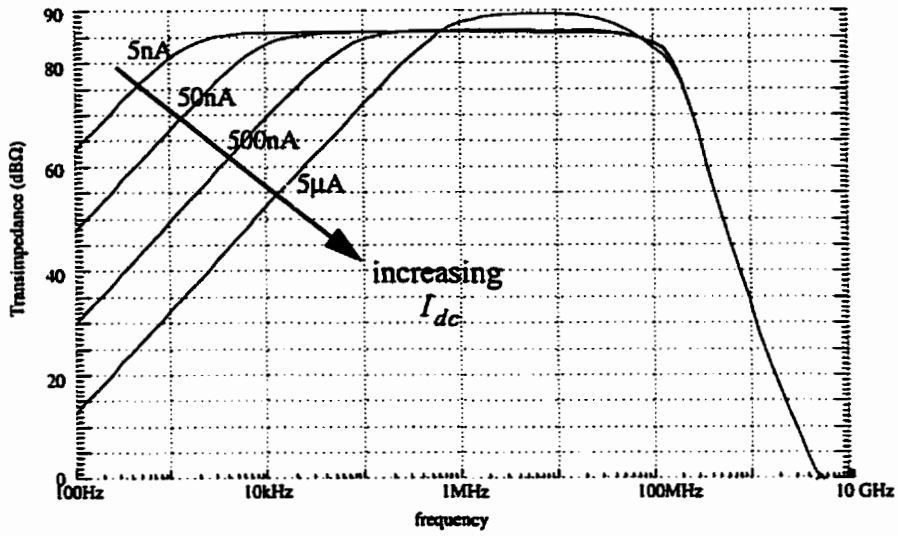


Figure 3.11 Frequency response of preamplifier with dc photocurrent rejection for different current levels.

ambient light as the level increases. When the level is low, the feedback loop — or more precisely, transistor M_{ctl} — is nearly off. Since M_{ctl} is located right at the input, any thermal noise it generates adds directly to the signal current. Having M_{ctl} turn off maximizes the preamplifier's sensitivity in low ambient light. When the signal is much stronger than the ambient light, the saturation of the preamplifier can be prevented by simply adjusting the preamplifier gain. Thus, the ambient photocurrent rejection circuit is not critical here, and can be disabled or limited in order to eliminate this dependency on I_{dc}.

In situations involving large dc photocurrents, provisions are required to limit both g_{mctl} and the highpass cut-off frequency in order to prevent the preamplifier from filtering the signal. For instance, from Figure 3.11 we see that at 5μA, the cut-off frequency exceeds 1 MHz, and the outer feedback loop is beginning to affect the passband response of the transimpedance amplifier. Ideally, we would like some method of limiting the current that passes through transistor M_{ctl}. This limit must be greater than the ambient photocurrent generated by the photodiode under the brightest conditions (e.g. direct sunlight). A potential solution would be to redirect the excess photocurrent into another current source that is static, but which can be switched on when needed. In this way, the new current source does not change the

loop dynamics, but simply off-loads some of the current transistor Mctl would otherwise need to draw.

Fluorescent lamps with electronic ballasts require special consideration. These lamps do not have strong emissions in the infrared spectrum, so saturation of the preamplifier is usually not a problem. However, the rapid firing of the ballasts produces interference patterns with harmonics that can reach 1 MHz [Moreira,1997]. Consequently, additional high-pass filtering may be needed further along in the receiver to reject this interference.

3.3 A LOW-VOLTAGE TRANSIMPEDANCE AMPLIFIER

As mentioned in Chapter 2, one of the primary challenges of designing optical preamplifiers capable of low-voltage operation is maximizing both the output signal swing and the bias voltage for the photodiode. Towards this end, we developed the novel transimpedance structure shown in Figure 3.12. This circuit merges two separate ideas: a sub 1-V current mirror [Rijns,1993], [Peluso,1997] and a transimpedance amplifier based around a current-gain amplifier [Wilson,1997].

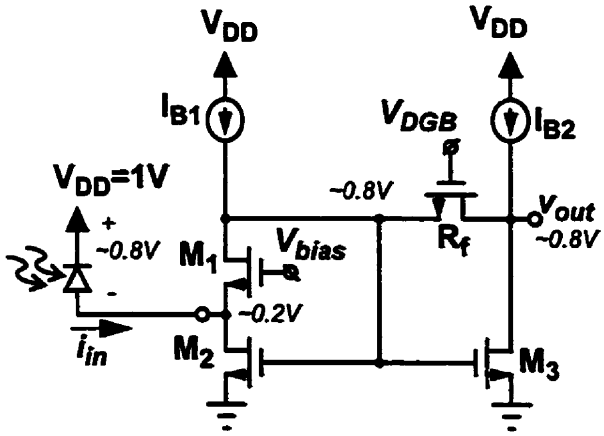


Figure 3.12 A low-voltage transimpedance amplifier.

The sub 1-V current mirror is shown in Figure 3.13. The current mirror differs from a normal mirror circuit with the additional device M_1 at the input. Since the

impedance looking into the source of M_1 is much lower than the impedance looking into the drain of M_2, the input current will be redirected up through M_1 and into node A. The injected charge will adjust the gate voltage of M_2 such that at steady state, the input current is redirected down through M_2. Since M_3 has the same gate-to-source voltage as M_2, the input current is duplicated at the output. However, unlike a normal mirror whose input is biased at V_{GS2}, the input voltage here is $(V_{bias} - V_{GS1})$ which is adjustable and can be reduced to V_{DSsat2}, the saturation voltage of M_2, before device M_2 drops out of the active mode of operation.

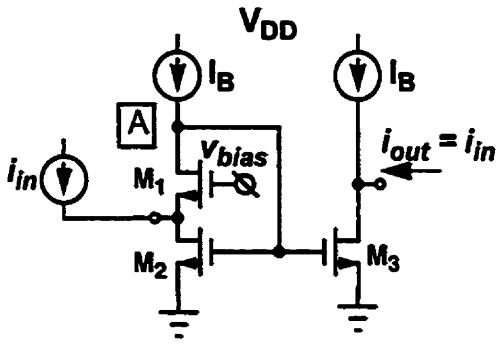


Figure 3.13 Sub 1-V current mirror.

A transimpedance amplifier based around a current-gain amplifier is shown in Figure 3.14. The amplifier uses the traditional transimpedance structure of a gain stage shunted by a feedback resistor, but the traditional voltage amplifier is replaced by a current amplifier. The schematic convention used here is adopted from [Johns,1997][2]. Here, the arrow marks the input and the direction of current flow, and A_i is the open-loop current gain. It can be shown that the transimpedance gain of this structure is

$$\frac{v_{out}}{i_{in}} = \frac{R_f A_i - R_{in}}{1 + A_i} \approx -R_f$$

where R_{in} is the amplifier's input resistance which is typically low. A direct implementation of Figure 3.14 using the current mirror in Figure 3.13 would require that

2. Chapter 6, p. 266.

the feedback resistor be attached across the input and output ports of the current mirror as found in other so-called 'current-mode' designs [Vanisri, 1992 and 1995]. Unfortunately, such a configuration would set the output bias voltage to that of the input terminal, or V_{DSsat2}, and the resulting circuit would have essentially no output swing. To overcome this problem, the left terminal of the feedback resistor is instead attached to node A in Figure 3.13.

The ability to vary the gain of a transimpedance amplifier is especially crucial in enhancing the dynamic range of low-voltage circuits where the signal swings are severely limited. In addition, a constant bandwidth is desirable for variable-gain transimpedance amplifiers because it helps eliminate out-of-band noise, thereby enhancing sensitivity in even the lowest gain settings.

Ideally, the topology shown in Figure 3.14 achieves this desired gain-bandwidth independence by virtue of its use of a current amplifier [Wilson,1997]. Recall that the feedback signal in a transimpedance amplifier is a current. When the gain stage is a current amplifier, the feedback signal is simply the output current of the amplifier and is independent of the value of R_f which determines the overall transimpedance gain.

In contrast, when the gain stage is a voltage amplifier, the feedback resistor is used to convert the output voltage back into the feedback current. The smaller the resistance, the larger the feedback current. Increasing the feedback signal in turn increases the closed-loop bandwidth of the transimpedance amplifier. As discussed in Section 3.1, gain-bandwidth independence can be achieved by having the open-loop gain track the transimpedance gain, as represented by the tracking of resistors R_1 and R_f in the two designs shown in Figure 3.1. Thus, through different mechanisms, both the proposed transimpedance amplifiers represented by Figure 3.1a and Figure 3.12 achieve gain-bandwidth independence.

Returning to the proposed preamplifier circuit in Figure 3.12, we can see that the input voltage can be set to V_{DSsat2} which is about 200mV. The resulting photodiode bias voltage is $(V_{DD} - V_{DSsat2})$ which, for a 1V supply, is about 0.8V or

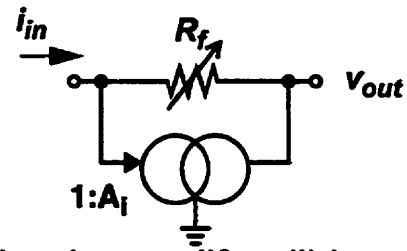


Figure 3.14 Transimpedance amplifier utilizing a current gain stage.

80% of the supply. This amplifier possesses a large output swing because data pulses from the photodiode are injected into the preamplifier, resulting in negative-going output pulses. Since the output is biased at $V_{GS3} = V_{tn} + V_{DSsat3}$ and can swing down to V_{DSsat3}, the amplifier has an output swing equal to the threshold voltage, V_{tn}. For a 0.6V threshold voltage, an output swing of 0.6V represents 60% of a 1V supply. Thus, in contrast to the designs presented in Chapter 2, the proposed structure achieves both a large bias voltage and large signal swing. It should be noted that the bias voltage is maximized because of the use of a common-gate input stage. Thus, the possibility exists for other common-gate topologies [Vanisri, 1992 and 1995] to provide a large bias voltage while having otherwise distinct characteristics.

Having proposed a novel low-voltage circuit topology, the next step is to analyze the circuit and to optimize the design. The basic dc characteristics of transimpedance gain and input and output resistance can be derived from a few observations based on the simplified dc small-signal circuit shown in Figure 3.15. The first observation is that the input current is divided amongst the drain currents of M_2 and M_3, so that

$$i_{in} = g_{m2}v_A + g_{m3}v_A \tag{3.10}$$

or equivalently that

$$v_A = i_{in}/(g_{m2} + g_{m3}) \tag{3.11}$$

Secondly, the output voltage is given in terms of v_A by

$$v_{out} = v_A - R_f g_{m3} v_A \,. \tag{3.12}$$

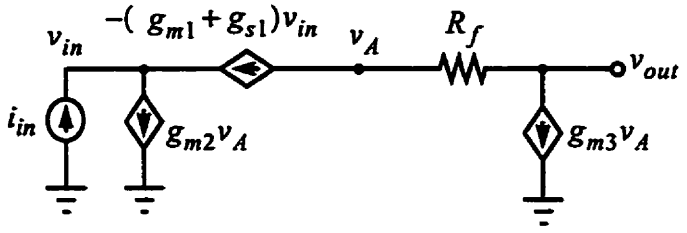


Figure 3.15 Simplified DC small-signal circuit of low-voltage preamplifier.

By combining Equations (3.11) and (3.12), we obtain the dc transimpedance gain

$$\frac{v_{out}}{i_{in}} = -\frac{g_{m3}R_f - 1}{g_{m2} + g_{m3}}. \tag{3.13}$$

The input resistance is obtained by simply applying KCL to the input terminal

$$i_{in} = g_{m2}v_A + (g_{m1} + g_{s1})v_{in} \tag{3.14}$$

which combined with Equation (3.11) gives

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{g_{m3}}{g_{m2} + g_{m3}}(g_{m1} + g_{s1})^{-1}. \tag{3.15}$$

The output resistance can be determined by applying a test current at the output as shown in Figure 3.16. From this circuit come the two relationships,

$$i_x = g_{m2}v_A + g_{m3}v_A \tag{3.16}$$

$$v_x = v_A - g_{m2}v_A R_f \tag{3.17}$$

and the resulting output resistance is

$$R_{out} = \frac{v_x}{i_x} = \frac{1 + g_{m2}R_f}{g_{m2} + g_{m3}}. \tag{3.18}$$

While the preamplifier's dc characteristics can be derived quite easily, the optimization of the design requires a deeper understanding of the frequency response of the circuit which is much more complex. Figure 3.17 plots the simulated frequency responses of four implementations of the proposed preamplifier using different tran-

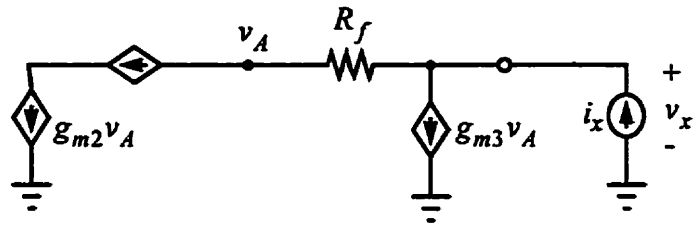


Figure 3.16 Small-signal circuit for determining the preamplifier output resistance.

sistor sizings and resistor values. The responses vary significantly in their resulting bandwidths and gains, and the trade-offs become even more complex when we also consider their noise performance. The analysis of this circuit is challenging. As we shall see, this circuit possesses no less than three feedback loops that are coupled together, making it difficult to apply the traditional feedback analysis techniques reviewed in Chapter 2. Nodal analysis is an option, but the resulting transfer functions are too cumbersome to help guide our design. As an example, the transimpedance gain of the circuit is given by

$$\frac{v_{out}}{i_{in}}(s) = \frac{Y_f - g_{m3}}{\dfrac{Y_A Y_1 Y_f}{g_{m1}} + \left[\dfrac{Y_f}{g_{m1}} Y_1 (Y_A + Y_L) + Y_A Y_L\right] + \left[g_{m3} Y_f \dfrac{Y_1}{g_{m1}} + g_{m2} Y_f + Y_f (Y_L + Y_A)\right] + (g_{m2} + g_{m3}) Y_f} \tag{3.19}$$

where

$$\begin{aligned} Y_1 &= s(C_{PD} + C_{in}) \\ Y_L &= s(C_L + C_{out}) \\ Y_A &= sC_A \\ Y_f &= 1/R_f + sC_f \end{aligned} \tag{3.20}$$

C_{PD} is the photodiode capacitance, C_{in} and C_{out} are the total input and output capacitances contributed by the amplifier, C_A is the total capacitance seen on node A, and R_f and C_f are the shunt feedback resistor and capacitor. Similarly complex expressions can be derived for the input and output impedance and noise densities

of the amplifier. In practice, we need to derive a set of relations that embody the essence of the circuit and characterize its design trade-offs. DPI/SFG analysis has the potential to fulfill this requirement. The method is presented in Chapter 4, and its application to the low-voltage transimpedance amplifier is presented in Chapter 5. Before proceeding, however, we need to conclude this section by discussing one final design challenge for the low-voltage transimpedance amplifier: the implementation of the feedback resistor.

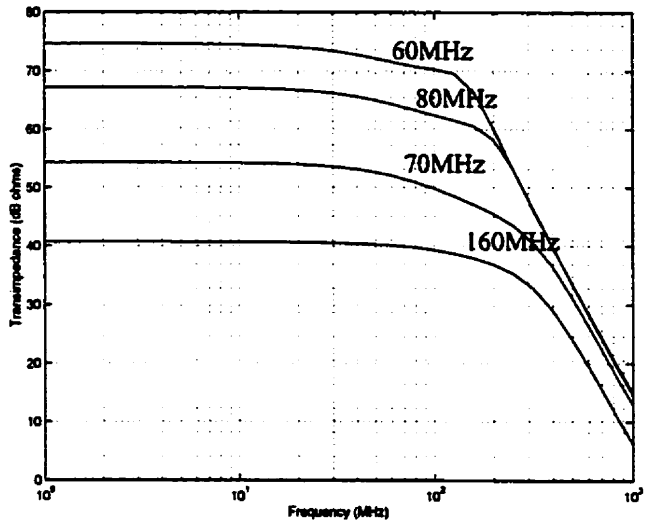


Figure 3.17 Simulated frequency responses of four low-voltage transimpedance designs with 3 dB bandwidths as indicated.

3.3.1 Dynamic Gate Biasing

The variable feedback resistor of the transimpedance amplifier can be implemented using either an NMOS or PMOS transistor operating in the linear region. An NMOS device is preferred, however, because its decreased resistance under large negative-going signals realizes soft limiting that further enhances the dynamic range of the preamplifier. Biasing the gate of the NMOS device is a challenge. As illustrated by the typical bias voltages in Figure 3.12, the source and drain of device R_f are already biased near the supply. For a 1V supply and without low-threshold devices, a charge pump is required to bias the gate above the available supply. In

order to induce a conductive channel in the MOSFET, the bias voltage should be approximately

$$V_{DGB} = V_{GS2} + V_{GSRf} \approx 2V_{GS2}$$

or basically double the gate-source bias voltage of a transistor.

Figure 3.18 illustrates two techniques for generating such a bias voltage. The first technique, shown in Figure 3.18a, involves using a voltage doubler to power a bias network consisting of a current source driving two, stacked, diode-connected MOSFETs. Since the voltage doubler uses a capacitor to maintain its output level, any current drawn by the bias network produces a ripple in the output voltage that is proportional to the current. Given the sensitivity of the preamplifier, any systematic ripple in the bias voltage should be avoided. An alternative technique illustrated in Figure 3.18b uses the voltage doubler to double the gate-source voltage of a single transistor and then to directly drive the MOSFET gate — a process referred to here as dynamic gate biasing (DGB). With DGB, no current is drawn from the charge pump, and ideally no ripple is generated. In practice, some ripple is generated through parasitic current leakage, charge injection, and clock feedthrough. These nonidealities will be discussed as part of the experimental results presented in Chapter 6.

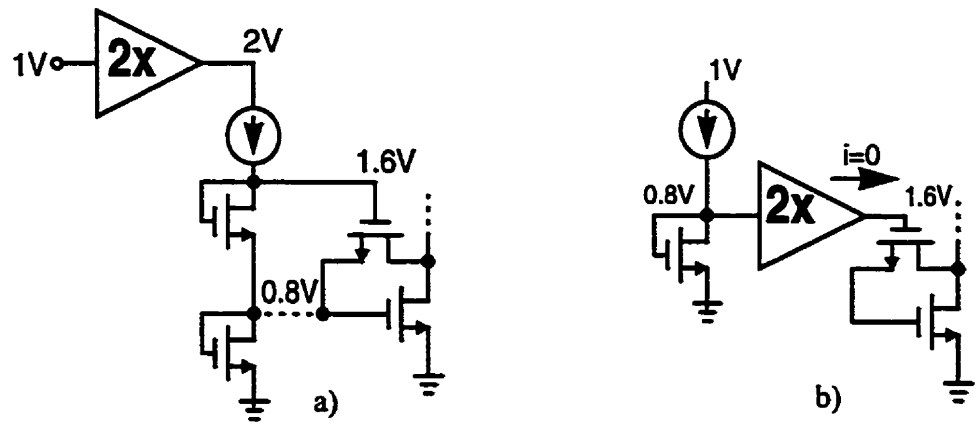


Figure 3.18 Two options for generating double a gate-source voltage.

While the use of DGB is quite established in memory circuits [Calligaro,1996], [Gerber,1981] and switched-capacitor circuits [Wu,1998], [Cho,1995], there has been little reported work in applying it to the stable biasing of transistors. Previous publications have already suggested using this technique for opamp compensation networks [Zhou,1997] and for tuning continuous-time filters [Monna,1994], but to date, no experimental results have been presented. We believe our work is the first experimental verification of DGB, and that DGB will likely become an increasingly common technique as analog designers look for ways to meet the challenge of decreased supply voltages.

The voltage doubler required for DGB is unique in numerous respects. Firstly, power efficiency is not a concern since the doubler is only driving the gates of MOSFETs and does not supply output power. Secondly, the doubler has a separate input because the bias voltage we wish to double is different from the supply. Thirdly, the doubler can accept input levels that lie near the threshold voltage. This ability is important in low-voltage applications where the bias voltages are often only slightly higher than the device threshold voltage.

There are numerous doubler and multiplier circuits, but few are suited for low-voltage operation. The two traditional topologies are the Dickson [Dickson,1976] and Cockcroft-Walton [Cockcroft,1932] charge pumps. Both designs use strings of diodes and so suffer a forward-biased diode voltage drop of about 0.7V between stages, making them extremely inefficient at low supply voltages. A modified Dickson topology capable of operating down to a 1.2V supply was presented in [Wu, 1996] and further enhanced in [Wu, 1998], but the necessary modifications are complex, and the circuit still suffers from a forward-biased diode voltage drop at the output. The output is also prone to large ripples due to the diode-configured output stage. Designs that are based on switched-capacitor techniques are generally simpler and better suited for low-voltage operation [Silva-Martinez,1994], [Favrat,1998]. The doubler presented in [Silva-Martinez,1994] is efficient and provides good accuracy, but its NMOS output switch requires an internal voltage tripler that could pose a reliability problem if implemented in today's deep sub-micron

CMOS technologies with low gate breakdown voltages. In contrast, the doubler presented in [Favrat,1998] avoids the need for a voltage tripler by using a PMOS output switch. The design is simple and efficient, and we chose this design as the basis for our doubler circuit.

The basic CMOS doubler circuit is shown in Figure 3.19 [Nakagome,1991]. The circuit uses a clock signal Φ_1 and its non-overlapping opposite Φ_2. The circuit operates in the following manner: switches M_1 and M_2 are alternately switched on and off in order to charge capacitors C_1 and C_2 to the voltage V_B (assuming the low level of the clock is equal to 0V); when the charging is complete, the clock signals at the top plates of the capacitors, Φ_1' and Φ_2', will be the same as the original clock signals but will have been shifted up by V_B as illustrated in Figure 3.20. Output switches sw_1 and sw_2 are timed so that the output load sees only the high phases of Φ_1' and Φ_2', and the resulting output voltage is constant at

$$V_{OUT} = V_{pp} + V_B$$

where V_{pp} is the peak-to-peak swing of the clock signals. Normally,

$$V_B = V_{pp} = V_{DD}$$

and the output is double the supply voltage. In order to double a bias voltage, one could imagine simply powering the doubler circuit using the bias voltage. Unfortunately, as discussed in [Favrat,1998] and [Wu,1998], voltage doublers have difficulty operating with supply voltages near the threshold voltage. However, by making a clear distinction between the desired bias voltage and the supply voltage, we can redesign the voltage doubler to greatly expand its operating range.

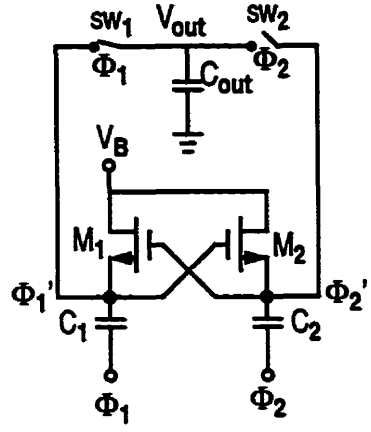


Figure 3.19 Basic Charge pump cell with output switches.

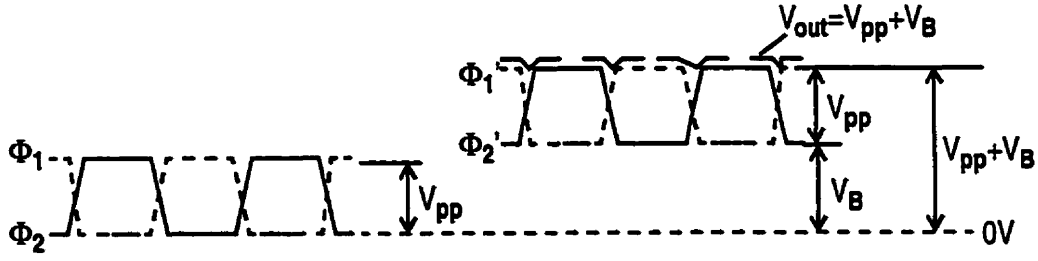


Figure 3.20 Steady state waveforms for charge pump.

The proposed bias voltage doubler circuit is shown in Figure 3.21. The circuit overcomes the low-voltage constraint by using, wherever possible, clock signals that have the full-supply swing. The circuit consists of three tightly-coupled charge pump cells: the main cell responsible for doubling the bias voltage, and two cells responsible for driving switches. Clock signals Φ_1 and Φ_2 switch from 0V to $V_{DD} = 1V$, while signals Φ_{1VB} and Φ_{2VB} have a reduce swing equal to the bias voltage, V_B, which we will assume here to be 0.85V. To help reduce clutter in the schematic, the gate connections of $M_{1,2}$ and $M_{5,6}$ were extended from the gate straight through the device where the body terminal is normally found. As such, the gates of $M_{1,3,5}$ are connected together as are those of $M_{2,4,6}$.

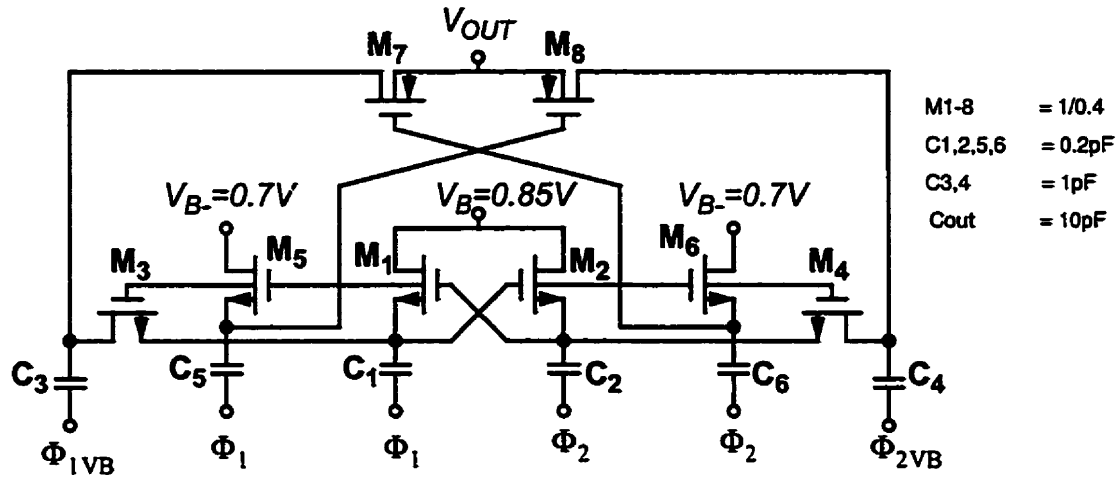


Figure 3.21 Proposed bias voltage doubler.

The central charge pump is shown in Figure 3.22. As shown on the side, the pump generates clock signals with the full 1V swing of the supply and an independent level shift of $V_B = 0.85V$. The main charge pump responsible for generating the bias voltage is highlighted in Figure 3.23. Instead of the usual cross-coupling of gates, the switches are driven by the central charge pump. During Φ_1, switches M_1 and M_3 close to connect the top plate of C_3 to V_B. At the same time, the bottom plate is connected to 0V. During Φ_2, the bottom plate is raised to V_B and the top plate is boosted to double V_B. Capacitor C_4 undergoes the same operations, but on the opposite clock phases.

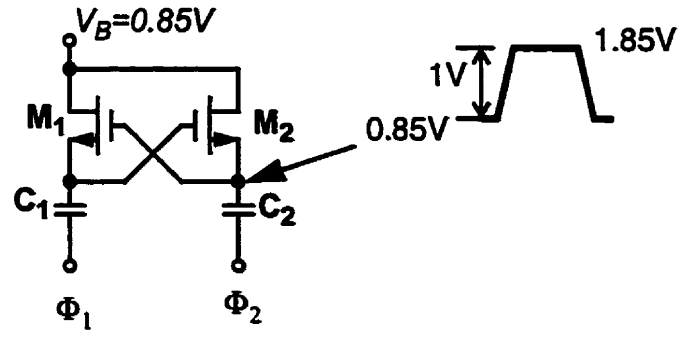


Figure 3.22 Central charge pump for generating main switch control signals.

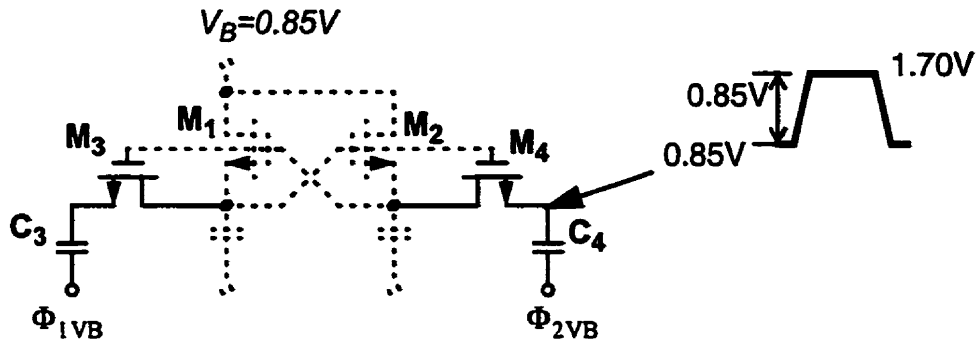


Figure 3.23 Main charge pump for doubling the input bias voltage.

Finally, the output switches M_7 and M_8 are driven by the third charge-pump, highlighted in Figure 3.24. Compared to the central charge pump, the third charge-pump uses a slightly lower level-shift voltage so that the gate-source voltages of switches M_7 and M_8 are 0V when the switches are open and 1V when the switches are closed. Although the output switches could have been connected to the central pump, the additional charge pump provides an added degree of freedom for improving the output resistance of the switch. For example, given a worse case threshold voltage of -0.8V, the gate-source voltage in excess of the threshold would be reduced to 0.05V. With the separate charge pump, this voltage is 0.2V, or four times greater.

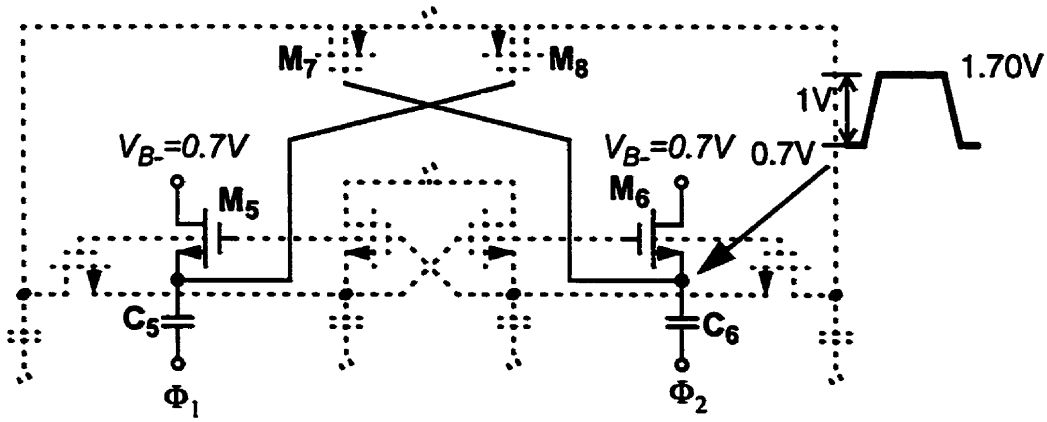


Figure 3.24 Charge pump for driving output switches.

The bias voltage doubler requires non-overlapping clock signals to clearly define the two phases of the circuit's operation. A non-overlapping clock generator based on [Martin,1981] was incorporated into the doubler circuit and is shown in Figure 3.25.

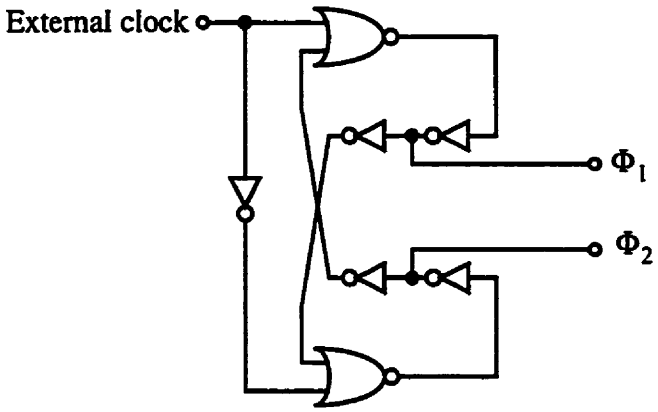


Figure 3.25 Non-overlapping clock generator.

To illustrate the expanded range of the proposed bias voltage doubler over that of the basic charge pump cell shown in Figure 3.19, we ran two simulations of the two circuits at start up. For the basic charge pump, the supply voltage was equal to the desired bias voltage. A small output load capacitance of 0.5 pF was chosen to speed up the transient response. The first simulation used an input voltage of 0.85V and is shown in Figure 3.26. We see that both circuits come to within 20mV of the ideal level. The slight undershoot is a result of parasitic capacitance on the top plates of the level-shifting capacitors. This undershoot can be easily compensated for by increasing the input bias voltage. The response of the proposed doubler is faster due to the reduced switch resistance afforded by the dedicated charge pump driving the output switches. In the second simulation, the input bias voltage is reduced to 0.75V. As shown in Figure 3.27, only the proposed doubler circuit manages to reach the desired level in this case. With the basic charge pump, the 0.75V supply provides a reduced clock swing that is barely enough to initially turn on switches M_1 and M_2, and the switches quickly become ineffective as the threshold voltages of switches M_1 and M_2 increase due to the body effect.

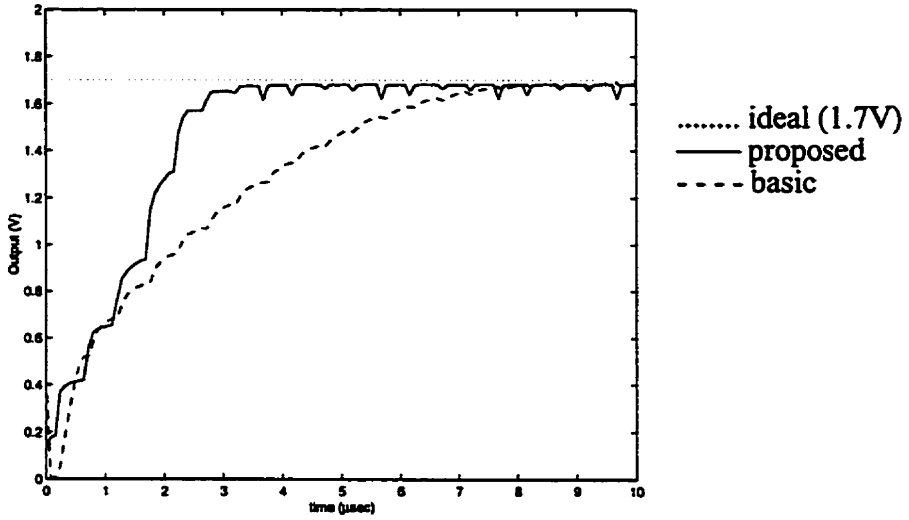


Figure 3.26 Simulation comparison of step-up responses for proposed bias voltage doubler and basic charge pump to a 0.85V input ($C_L = 0.5pF$).

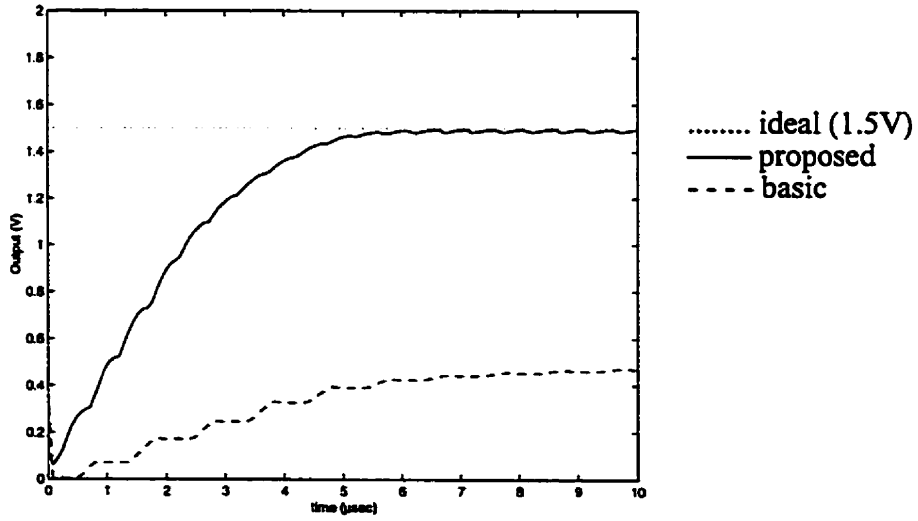


Figure 3.27 Simulation comparison of step-up responses for proposed bias voltage doubler and basic charge pump to a 0.75V input ($C_L = 0.5pF$).

3.4 SUMMARY

In this chapter, we presented circuit techniques to reject ambient light, to enhance the dynamic range, and to enable the low-voltage operation of transimpedance amplifiers. Enhanced dynamic range was achieved through a fully-differential, variable-gain, transimpedance amplifier. The amplifier uses an internal shunt feedback topology, and overcomes many of the stability challenges found in previous designs. Simulation results were presented for a CMOS implementation that consumed 8mW at 3V, and provided 70 MHz bandwidth over a 77dB dynamic range with a maximum transimpedance gain of 20kΩ and a gain range of 32dB.

Ambient light rejection was achieved by placing the proposed transimpedance amplifier within a larger feedback loop. The feedback topology eliminated the need for large passive devices and improved the regulation of the photodiode bias voltage. We analyzed the stability requirements of this structure and its implications on the component error amplifier. The low-frequency behaviour of the circuit was found to be dependent on the ambient light level, and we discussed ways to regulate the feedback loop to control this dependency.

Low-voltage operation was achieved with a novel transimpedance amplifier structure and with dynamic gate biasing. The transimpedance amplifier was capable of 1V operation without the use of low-threshold devices, yet provided a wide output swing and maximized the available bias voltage for the photodiode. We described dynamic gate biasing and the use of charge pumps to bias and tune MOS resistors. The complex internal feedback mechanisms of the proposed amplifier makes its analysis difficult, and motivates our investigation into the DPI/SFG method, a graphical circuit analysis technique that is presented in the next chapter.

REFERENCES

A. A. Abidi, "High-Frequency Noise Measurements on FETs with Small Dimensions," *IEEE Trans. Electron Devices*, vol. 33, pp. 1801-1805, November 1986.

C. Calligaro et al., "Positive and Negative CMOS Voltage Multiplier for 5-V-Only Flash memories," *Proc. of IEEE Mid-West Symp. Circ. and Syst.*, vol. 1, pp. 294-297, 1996.

E. M. Cherry and D. E. Hooper, "The design of wide-band transistor feedback amplifiers," *Inst. Elec. Eng. Proc.*, vol. 110, no. 2, pp. 375-389, February 1963.

E. M. Cherry and D. E. Hooper, *Amplifying Devices and Low-Pass Amplifier Design*, John Wiley, New York, pp. 543-558, 1968.

T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166-172, March 1995.

J. D. Cockcroft and E. T. S. Walton, "Further developments on the method of obtaining high-velocity positive ions," *Proc. Royal Society London*, 131, 169, 1932.

R. Coppoolse, J. Verbeke, P. Lambrecht, J. Codenie, and J. Vandewege, "Comparison of a Bipolar and a CMOS Front End in Broadband Optical Transimpedance Amplifiers," *Proc. 38th Midwest Symp. on Cir. and Sys.*, Brazil, pp. 1026-1029, Aug. 1996.

J. Dickson, "On-chip High-Voltage Generation in NMOS Integrated Circuits Using an Improved Voltage Multiplier Technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 6, pp. 374-378, June 1976.

P. Favrat, P. Deval and M. J. Declercq, "A High-Efficiency CMOS Voltage Doubler," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 410-416, March 1998.

B. Gerber, J. Martin, and J. Fellrath, "A 1.5V single-supply one transistor CMOS EEPROM," *IEEE J. Solid-State Circuits*, vol. SC-16, no. 6, pp. 195-200, June 1981.

J. L. Hullett and S. Moustakas, "Optimum transimpedance broadband optical preamplifier design," *Optical and Quantum Electronics*, vol. 13, pp. 65-69, 1981.

D. A. Johns and K. W. Martin, *Analog Integrated Circuit Design*, Wiley, Toronto, 1997.

H. Khorramabadi, L. D. Tzeng, and M. J. Tarsia, "A 1.06 Gb/s -31 dBm to 0dBm BiCMOS Optical Preamplifier Featuring Adaptive Transimpedance," *IEEE ISSCC Digest of Tech. Papers*, pp. 54-55, Feb. 1995.

K. Martin and A. S. Sedra, "Switched-Capacitor Building Blocks for Adaptive Systems," *IEEE Trans. Circ. and Syst.*, vol. 28, no. 6, pp. 576-584, June 1981.

R. G. Meyer and W. D. Mack, "A Wideband Low-Noise Variable-Gain BiCMOS Transimpedance Amplifier," *IEEE J. Solid-State Circuits*, vol. 29, no. 6, pp. 701-706, June 1994.

G. L. E. Monna et al., "Charge Pump for Optimal Dynamic Range Filters," *IEEE Int. Symp. Circ. and Syst.*, vol. 5, pp. 747-750, 1994.

A. J. C. Moreira, R. T. Valadas, and A. M. de Oliveira Duarte, "Optical interference produced by artificial light," *Wireless Networks*, vol. 3, pp. 131-140, 1997.

Y. Nakagome et al., "An experimental 1.5 V 64Mb dram," *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 465-472, April 1991.

V. Peluso, P. Vancorenland, M. Steyaert, and W. Sansen, "900mV differential class AB OTA for switched opamp applications," *Electronics Letters*, vol. 33, no. 17, pp. 1455-1456, 14 August 1997.

J. J. F. Rijns, "54 MHz switched-capacitor video channel equaliser," *Electronics Letters*, vol. 29, no. 25, pp. 2181-2182, 9 December 1993.

A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 4th ed., Oxford University Press, New York, pp. 718-722, 1997.

J. Silva-Martinez, "A Switched Capacitor Double Voltage Generator," *IEEE Proc. Mid-West Symp. Circuits and Systems*, vol. 1, pp. 177-180, 1994.

T. Vanisri and C. Toumazou, "On the Design of Low-Noise Current-Mode Optical Preamplifiers," *J. Analog Integrated Circuits and Signal Processing*, vol. 2, no. 3, pp. 179-195, September 1992.

T. Vanisri and C. Toumazou, "Integrated High Frequency Low-Noise Current-Mode Optical Transimpedance Preamplifiers: Theory and Practice," *IEEE J. Solid-State Circuits*, vol. 30, no. 6, pp. 677-685, June 1995.

B. Wilson and J. D. Drew, "Novel Transimpedance Amplifier Formulation Exhibiting Gain-Bandwidth Independence," *IEEE Proc. Int. Symp. Circuits Systems*, vol. 1, pp. 169-172, June 1997.

J. T. Wu, Y. H. Chang and K. L. Chang, "1.2V CMOS Switched-Capacitor Circuits," *IEEE ISSCC Dig. Tech. Papers*, pp. 388-389, February 1996.

J.-T. Wu, and K.-L. Chang, "MOS Charge Pumps for Low-Voltage Operation," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 592-597, April 1998.

T. Yoon, B. Jalali, "1.25 Gb/s CMOS Differential Transimpedance Amplifier For Gigabit Networks," *Proc. European Solid-State Circuits Conf.*, pp. 140-143, Sept. 1997.

B. Zand, K. Phang, and D.A. Johns, "Transimpedance Amplifier with Differential Photodiode Current Sensing," *IEEE Int. Symp. Circuits and Systems*, Orlando, FA, vol. 2, pp. 624-627, May 1999.

J. Zhou et al., "Charge-Pump Assisted Low-Power/Low-Voltage CMOS Opamp Design," *IEEE Proc. Int. Symp. Low Power Electronics and Design*, pp. 108-109, 1997.

CHAPTER

4 The DPI/SFG Analysis Method

4.1 INTRODUCTION

A good circuit analysis technique can aid circuit design. Beyond determining correct voltages and currents, it should also provide insight into the circuit's operation and dynamics. This chapter describes an approach to circuit analysis based on driving-point impedance (DPI) analysis and signal-flow graphs (SFG), appropriately named DPI/SFG analysis [Ochoa,1998]. The method involves representing circuit equations using signal-flow graphs and then performing graph algebra and using graph reduction techniques to obtain circuit transfer functions [Ochoa,1999a].

There are numerous advantages to circuit analysis using the DPI/SFG method. First, the method provides a systematic procedure for deriving a signal-flow graph representation of a circuit. The resulting visual representation can enhance a designer's understanding of the dynamics of a circuit. Arguably, the signal-flow graph (SFG) is a more intuitive representation than a set of linear equations derived from nodal or loop analysis. The technique requires no approximations or assumptions, and is not limited to circuits with a single feedback loop. The structure of the SFG mirrors that of the circuit, enabling one to correlate a circuit's behaviour with its structure. In analyzing feedback circuits, DPI/SFG analysis does not involve the physical breaking of feedback loops. Consequently, it avoids the intrusive and error-prone process of analyzing altered circuits that is inherent in feedback analysis based on topology [Sedra,1998] or return ratios [Rosenstark,1986]. Manipulating an SFG is also fundamentally different than altering a real circuit because an SFG represents an abstract algebra with a complete set of axioms and rules for manipulation. An SFG's branches and nodes are ideal elements that can be freely manipulated without having to consider loading effects. Finally, DPI/SFG analysis, unlike topology-based feedback analysis, neither requires one to determine the feed-

back topology of a circuit nor to assume that the feedforward and feedback components are unilateral.

Of course, no analysis technique is without its limitations. The DPI/SFG analysis method only applies to linear circuit networks, including small-signal circuits. As such, all dependent sources must be a linear function of parameters and signals within a circuit. Although all node voltages are represented in the SFG, the currents flowing through circuit elements are generally not represented directly. Instead, the technique uses the concept of *short-circuit currents* that will be described in this chapter. Consequently, an additional stage of computation is sometimes required to determine currents flowing through elements.

Although DPI/SFG analysis has only recently been reported [Ochoa,1998], many of its elements can be traced back to the circuit analysis techniques and interpretations developed by Mason and Zimmermann [Mason,1960]. For example, they introduced the concepts of short-circuit currents, driving-point impedances, and the placement of auxiliary voltage sources for analyzing circuits.[1] As well, in the process of developing node-voltage basis analysis, they described how such concepts could be applied to forming signal-flow graphs — in essence, describing a framework for DPI/SFG analysis.[2] In the end, however, a systematic analysis method was never formulated from these concepts. The concepts were included largely to provide a physical interpretation of Mason and Zimmermann's techniques, and they were presented alongside many other possible interpretations of circuit behaviour.

The DPI/SFG method was first presented as an analysis technique in its own right by Ochoa [Ochoa,1998]. Ochoa's description of the technique derived from a circuit analysis method based upon driving-point impedances and the use of auxiliary voltage sources to disable feedback [Kelly,1970]. Essentially, Ochoa extended Kelly's work by proposing a systematic application of auxiliary voltage sources throughout a circuit in order "to produce a system of coupled subcircuit problems that are easier to solve than the original circuit." [Ochoa,1998] In addition, he dem-

1. See [Mason, 1960], Section 2.6, pp. 20-24.
2. Ibid, Section 5.5, p. 152.

onstrated the effectiveness of representing such systems using signal-flow graphs. Ochoa has since applied the DPI/SFG method to noise and stability analysis [Ochoa,1997, 1999a].

Thus far, DPI/SFG analysis has been explained principally through specific circuit examples, making it difficult to generalize the method for arbitrary circuit networks. For example, none of the reported examples involve floating voltage sources. In this thesis, we develop a general formulation of the method suitable for all linear networks, first by justifying driving-point impedance analysis as a cause-and-effect interpretation of Kirchhoff's Current Law, and then by applying signal-flow graph theory. Throughout this chapter, we illustrate the method on a range of circuits involving transistors and ideal building blocks. Our two particular contributions are in showing how circuits with floating voltage sources are handled, and in re-deriving Blackman's Impedance Formula using DPI/SFG analysis.

The final contribution of this chapter is in the area of education. Our motivation for pursuing the development and refinement of the DPI/SFG method is deeply rooted in the belief that we can improve the way in which we analyze and teach feedback circuits. This chapter is intended to give the reader a thorough understanding of the DPI/SFG method. Throughout the chapter, original circuit examples are presented to illustrate how DPI/SFG analysis is applied to a wide variety of circuits. These examples are meant to help the reader with the mechanics of the method as well as to highlight some of the strengths of DPI/SFG analysis in providing insight into the operation of circuits.

4.2 CIRCUIT ANALYSIS USING DRIVING-POINT IMPEDANCES

Consider an internal node within an arbitrary circuit network comprised of passive elements and current sources as illustrated in Figure 4.1.

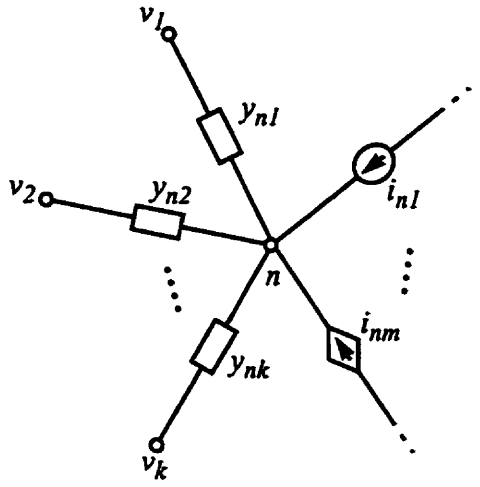


Figure 4.1 General circuit node.

From Kirchhoff's Current Law (KCL), we can express the net current into node n as

$$\sum_{j=1}^{k} (v_j - v_n) y_{nj} + \sum_{j=1}^{m} i_{nj} = 0 \tag{4.1}$$

This can be rewritten in a cause-and-effect form in which the effect — node voltage v_n — is presented as the result of the various causes — all admittances, current sources, and the other node voltages:

$$v_n = \underbrace{\left[\sum_{j=1}^{k} y_{nj}\right]^{-1}}_{\text{Driving-point impedance}} \underbrace{\left[\sum_{j=1}^{k} v_j y_{nj} + \sum_{j=1}^{m} i_{nj}\right]}_{\text{Short-circuit current}} = Z_{DP} \times I_{SC} \tag{4.2}$$

Equation (4.2) is in the form of Ohm's Law, and indicates that the voltage at a node can be expressed as the product of an impedance and a current. We can reinterpret this form of KCL for linear networks in terms of auxiliary voltage sources as shown in Figure 4.2. For the moment, we can imagine that each of the node voltages are now determined by an independent voltage source.

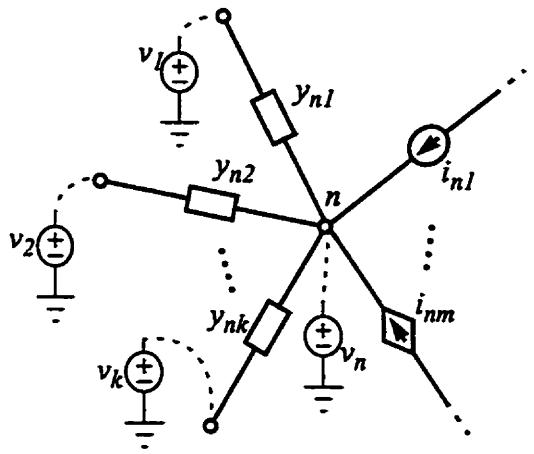


Figure 4.2 Interpreting Kirchhoff's Current Law using auxiliary voltage sources.

From Equation (4.2), we see that the impedance term is simply the inverse of the sum of the admittances of all passive elements attached to the node. More generally, the term can be interpreted from Figure 4.2 as the impedance seen at node n when all current sources (including dependent sources) and the auxiliary voltage sources at other nodes are set to zero. We define this as the *driving-point impedance (DPI)* of a node, and represent this impedance by the symbol Z_{DP}.

The second term of Equation (4.2) represents the superposition of currents flowing into node n that are generated by individual current and voltage sources when all other sources including v_n are zeroed. Initially, *all* current and voltage sources are treated as being independent; later, the constraints for all dependent sources are put back in place to re-establish the circuit's true behaviour. Although, the validity of temporarily treating dependent sources as independent is not clearly stated in some circuit theory textbooks [Davis,2000], the practice is well-established [Mason,1960] and is sometimes referred to as *taping* [Davis,1998]. Since the second term of Equation (4.2) can be interpreted as the net current that flows into source v_n when v_n is zeroed and node n is essentially shorted to ground, we define this current as the *short-circuit current* of a node, and represent it with the symbol I_{SC}. It is important to distinguish this short-circuit current from the actual net current that enters the node, which of course, is always constrained to zero by KCL.

The representation of a node voltage as a $Z_{DP} \times I_{SC}$ product can be used to analyze entire circuits. As a first attempt, the procedure can be expressed in the following steps:

1. Attach auxiliary voltage sources, v_n, to each node of the linear circuit network.
2. Determine the driving-point impedance and short-circuit current of each node.
3. Finally, the circuit equations are represented by the DPI relations for each node,

$$v_n = Z_{DPn} \times I_{SCn} \tag{4.3}$$

and by the relations that dictate the values of all sources, both dependent and independent.

Ultimately, the concept of placing auxiliary voltage sources is not essential. The idea is simply a convenient paradigm for guiding our analysis and allowing us to apply our traditional understanding of superposition.

EXAMPLE 4.1 A SIMPLE LINEAR CIRCUIT

We can demonstrate DPI analysis with a simple example. Consider the circuit in Figure 4.3, and determine the node voltages given that $R_a = 1\Omega$, $R_b = 5\Omega$, and $I_{dc} = 1A$.

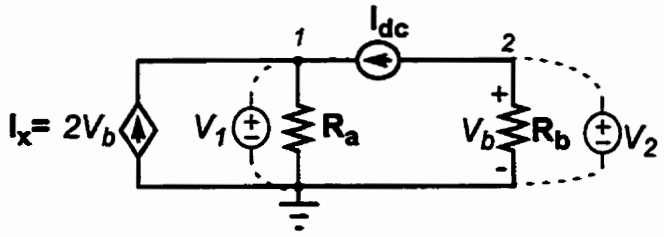


Figure 4.3 Simple circuit example to demonstrate DPI analysis.

Begin by placing auxiliary voltage sources at nodes 1 and 2. When current source I_{dc} is zeroed, nodes 1 and 2 are isolated. As such, the driving-point impedances are

$$Z_{DP1} = R_a$$
$$Z_{DP2} = R_b$$

For the short-circuit current of node 1, we see that we have contributions from both current sources, thus

$$I_{sc1} = I_{dc} + I_x$$

For node 2, current is being drawn out of the node by source I_{dc} thus,

$$I_{sc2} = -I_{dc}$$

The final step involves re-establishing the original constraint placed on current source, $I_x = 2V_b$, and setting the node voltages to the products of their respective driving-point impedances and short-circuit currents:

$$V_2 = I_{SC2} \times Z_{DP2} = (-1)(5) = -5V$$
$$V_1 = I_{SC1} \times Z_{DP1} = (I_{dc} + I_x)(R_a) = (I_{dc} + 2V_b)R_a$$
$$= (1 + 2(-5)) \times 1 = -9V$$

4.2.1 The Complete DPI Analysis Procedure

To date, published material on DPI/SFG analysis have not shown how the method can be applied to circuits that contain floating or dependent voltage sources. In this section, we refine the DPI analysis procedure to accommodate for voltage sources. Voltage sources pose a slight problem in the practical application of KCL because the current through a voltage source is unconstrained. Since both nodal and DPI analysis techniques are simply applications of KCL, both techniques require provisions for handling voltage sources. For nodal analysis, this includes the concept of the *supernode* [Bobrow,1987]. No new concepts are required for DPI analysis. However, the procedure that was outlined in the previous section needs to be reformulated and generalized. Consider the simple circuit in Figure 4.4 that contains one floating voltage source. If we attempt to follow the same procedure used in

EXAMPLE 4.1, we find that the driving-point impedance for both nodes is zero since the nodes are shorted to ground by the voltage sources. For the same reason, the short-circuit currents of both nodes are infinite. Thus,

$$Z_{DP1} = Z_{DP2} = 0$$
$$I_{sc1} = I_{sc2} \rightarrow \infty$$
$$\therefore V_1 = V_2 = Z_{DP1} \times I_{sc1} = \text{undefined}$$

and we have no answer.

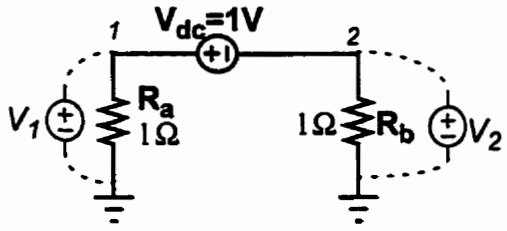


Figure 4.4 Example circuit containing a voltage source.

The problem lies in our choice of auxiliary voltage sources. From Figure 4.4, it is clear that a circuit with two nodes can have at most two independent voltage sources, and by adding both v_1 and v_2, we have overdetermined the system. In practice, we need to reduce the number of auxiliary voltages sources we add by the number of voltages sources that exist in the original circuit. Notice that we have not changed the DPI method, and so no proof is required for the modification. We have simply made explicit how DPI analysis is applied to circuits containing voltage sources in order to uphold the principle of superposition.The placement of auxiliary voltage sources is covered in the first step of the procedure which can now be expressed in the following way:

1. Given an arbitrary linear circuit network containing $n+1$ nodes (one of which is reference ground), and k voltage sources (including dependent ones), attach n-k auxiliary voltages sources, each with the negative terminal grounded, to individual nodes in the network so that when *all* voltage sources are zeroed, every node is effectively shorted to ground.

In graph theory, this amounts to creating a network in which we can select a *tree* made up entirely of voltage sources. A tree is defined as a graph with n nodes and containing a minimum number of branches (i.e., n-1) that manage to span all the nodes of the graph. It is useful to recognize that a tree cannot contain any loops: any graph containing loops has greater than the minimum number of branches since the removal of any one branch of a loop does not affect the number of nodes spanned. The remaining two steps of the analysis procedure must be adapted to reflect the fact that now not every node is associated with an auxiliary voltage source. The complete DPI analysis procedure can now be expressed in the following steps:

DPI Circuit Analysis Procedure

1. Given an arbitrary linear circuit network containing $n+1$ nodes (one of which is reference ground), and k voltage sources (including dependent ones), attach n-k auxiliary voltages sources, each with the negative terminal grounded, to individual nodes in the network so that when *all* voltage sources are zeroed, every node is effectively shorted to ground.

2. Determine the driving-point impedance (Z_{DP}) and short-circuit current (I_{SC}) for each node with an auxiliary voltage source.

   The driving-point impedance is the impedance seen by the auxiliary voltage source when *all* other sources — whether voltage or current, dependent or independent, existing or auxiliary — are set to zero. Algebraically, it is the inverse of the sum of all admittances attached to the node:

$$Z_{DPn} = \left[\sum_j y_{nj}\right]^{-1} \tag{4.4}$$

   where y_{nj} represents the total admittance between nodes n and j.

   The short-circuit current represents the net current that flows *into* the auxiliary voltage source when the source is set to zero. The short-circuit current is a linear function of *all* the other sources in the circuit which, for the moment, are considered independent. When the circuit does not contain any floating voltage sources, the short-circuit current is given by

$$I_{SCn} = \sum_j v_j y_{nj} + \sum_k i_{nk} \tag{4.5}$$

where v_j represents the voltage at node j and i_{nk} is the k'th current source attached to node n. When floating voltage sources exist in the circuit, the short-circuit current contributions of those sources must be added to Equation (4.5). These currents must be determined by analyzing the circuit.

3. Re-establish the original behaviour of the circuit by applying the constraint

$$v_n = Z_{DPn} \times I_{SCn} \tag{4.6}$$

to all of the auxiliary voltage sources. For all other sources, both voltage and current, re-establish their original values or their dependence relationships. All remaining nodes without an auxiliary voltage source have their voltage determined as a sum of existing and auxiliary sources.

Returning to the circuit in Figure 4.4, this time we add only one auxiliary voltage source at either node 1 or 2. If we decide to use node 1, the voltage at node 2 is then determined by

$$V_2 = V_1 - V_{dc}$$

When V_{dc} is zeroed to determine Z_{DP1}, V_1 sees R_b together in parallel with R_a. Thus

$$Z_{DP1} = R_a \| R_b = 0.5\Omega$$

For the short-circuit current, with V_1 set to zero, the voltage at node 2 is $-V_{dc}$. This generates a current that flows from node 2 to node 1, thus

$$I_{SC1} = \frac{V_{dc}}{R_b} = 1A$$

As a result, the node voltages are

$$V_1 = I_{sc1} Z_{DP1} = (1A)(0.5\Omega) = 0.5V$$
$$V_2 = V_1 - V_{dc} = -0.5V$$

This section has focussed on the first half of the DPI/SFG method, namely circuit analysis using driving-point impedances. The second half of the method deals with the representation of DPI analysis using signal-flow graphs.

4.3 DPI/SFG: COMBINING DPI ANALYSIS AND SIGNAL-FLOW GRAPHS

DPI/SFG analysis combines driving-point impedance analysis and signal-flow graphs. DPI relations are of the form

$$v_n = Z_{DPn} \times I_{SCn} \tag{4.7}$$

and they are naturally represented in signal-flow graphs because they represent a cause-and-effect relationship. DPI/SFG analysis follows the same procedure outlined in Section 4.2.1 for DPI analysis. There are certain characteristics that signal-flow graphs take on when derived from DPI analysis. The basic DPI relation in Equation (4.7) is represented in the SFG space by two nodes, I_{SCn} and v_n, and a connecting branch Z_{DPn}. Short-circuit current node I_{SCn} has only one outgoing branch with a transmittance, Z_{DPn}, but may have many incoming branches. Conversely, the auxiliary voltage source node v_n has only one incoming branch, Z_{DPn}, but may have many outgoing branches. To help distinguish these nodes from more general ones, we employ the node conventions shown in Figure 4.5. Apart from this, however, the signal-flow graphs presented here conform to the standard rules and conventions.

A systematic procedure can be used to help construct signal-flow graphs in DPI/SFG analysis. Begin by drawing all the $Z_{DP} \times I_{SC}$ node pairs, then add the driving-point impedance for each node. Fill in the transmittance branches by working from each voltage node and by adding a transmittance branch from the present node to each short-circuit current node that the present node affects. Finally, add the transmittance branches that re-establish the constraints on the dependent sources, and place node values to specify the values of independent sources.

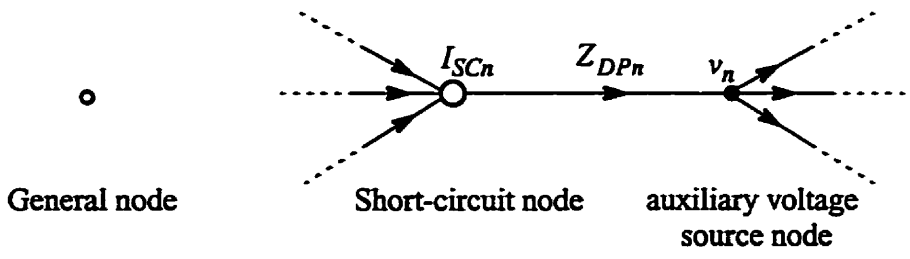


Figure 4.5 Basic node conventions.

EXAMPLE 4.2 A LINEAR CIRCUIT WITH FLOATING VOLTAGE SOURCES

This example serves to illustrate how DPI/SFG analysis can be applied to general linear circuits, including those containing voltage sources. The circuit is shown in Figure 4.6 and includes two floating voltage sources, one of which is dependent. All resistor values are given in units of Siemens ($S = A/V$), and we want to determine the node voltages.

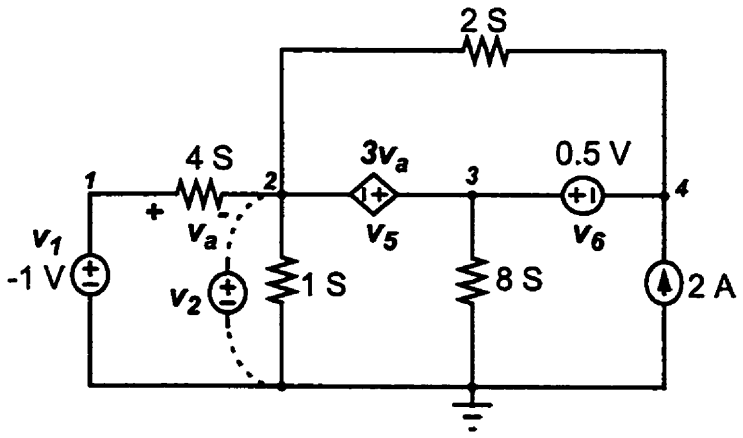


Figure 4.6 Sample circuit with voltage and current sources.

Since the circuit has four nodes that are not ground and contains three voltage sources, we only need to add one auxiliary voltage source. In order for all nodes to be shorted to ground when all sources are zeroed, the auxiliary source can be placed at nodes 2, 3, or 4. Since dependent source v_5 is a function of voltages at nodes 1 and 2, we can choose node 2 so that v_5 becomes simply the difference between sources v_1 and v_2. Our four voltage sources are then v_1, v_2, v_5, and v_6. To determine Z_{DP2}, we zero all sources except v_2, obtaining the circuit shown in Figure 4.7. By inspection,

$$Z_{DP2} = \frac{1}{4 + 1 + 8}\Omega = \frac{1}{13}\Omega$$

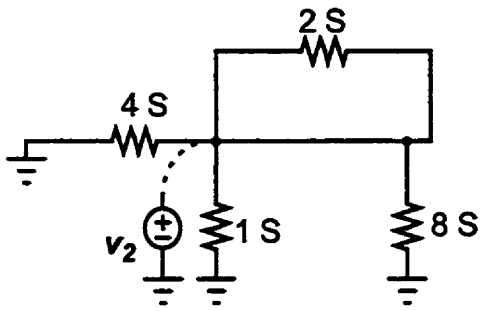


Figure 4.7 Simplified circuit for determining Z_{DP2}.

Notice how the 2S conductance can be ignored as its terminals are shorted together. Short-circuit current i_{sc2} is determined by considering the effect of each source separately. With a little practice, the following procedure can be done by inspection. For the sake of clarity, however, we illustrate the individual short-circuit components in Figure 4.8. Notice from the subcircuits of sources v_5 and v_6, that any element connected across the source does not contribute to the short-circuit current as the element and source form a loop around which current can circulate.

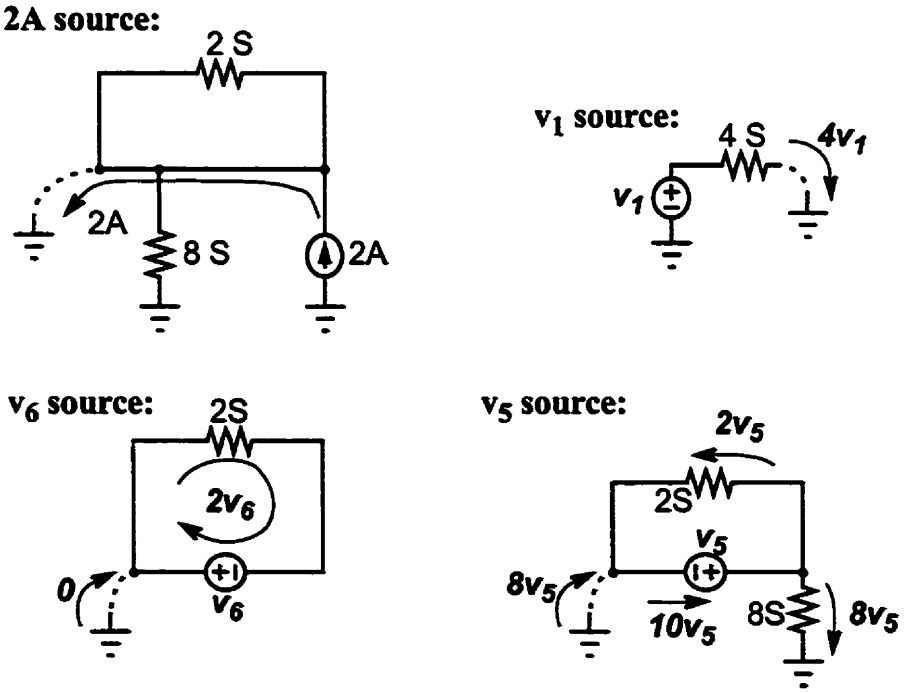


Figure 4.8 Simplified circuits illustrating short-circuit contributions of four separate sources.

The final step involves re-establishing the constraints on the voltage sources, giving

$$
\begin{aligned}
v_1 &= -1V \\
v_2 &= Z_{DP2} I_{SC2} \\
v_3 &= v_2 + v_5 \\
v_4 &= v_2 + v_5 - v_6 \\
v_5 &= 3(v_1 - v_2) \\
v_6 &= 0.5V
\end{aligned}
$$

The resulting SFG is shown in Figure 4.9a. Node voltages v_3 and v_4 are left out in order to simplify the graph. These nodes are not part of the chosen voltage tree, and their values can be easily determined once the voltages of the tree are known. The SFG can be simplified to that in Figure 4.9b which conforms to the traditional feedback structure of Figure 2.19 found on page 37, and as such, we can use the equivalence relation to obtain the final equations:

$$
\begin{aligned}
v_2 &= \frac{1/13}{1 - 24/13} \times 22 = -2V \\
v_5 &= 3(v_1 - v_2) = 3V \\
v_3 &= v_2 + v_5 = 1V \\
v_4 &= v_1 + v_5 - v_6 = 0.5V
\end{aligned}
$$

Notice from the SFG that, because of the zero transmittance, the value of v_6 has no affect on the voltage at node 2! Again, this is because any current v_6 generates circulates around through the 2S conductance resulting in no net current into node 2. Such observations help illustrate the way in which signal-flow graphs can provide us with insight into the operation of a circuit, revealing relations that are not immediately apparent from the circuit.

4.4 DETERMINING PORT IMPEDANCES

Once an SFG has been generated for a circuit, the port impedance at any node can be determined by inserting a test current source at the node of interest and determining the effect of its current on the node voltage. Although one can also apply a

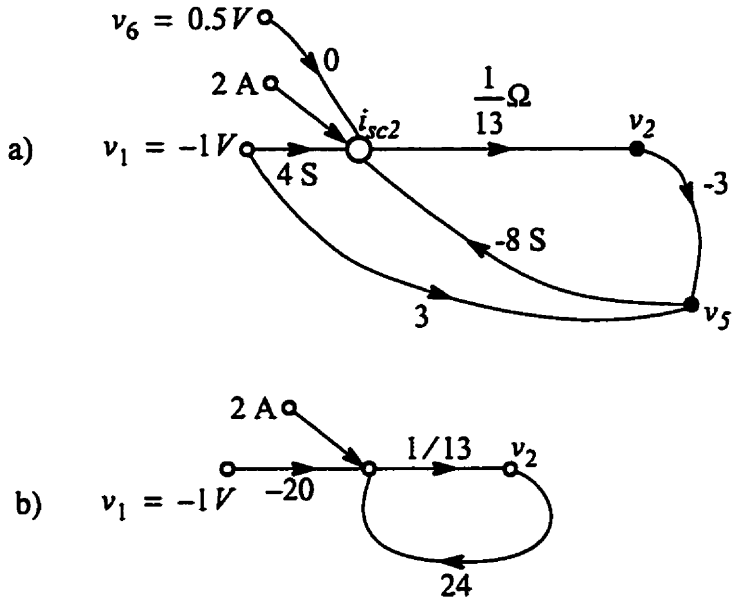


Figure 4.9 a) Final signal-flow graph for circuit in Figure 4.6, b) Simplified SFG.

voltage and measure the current drawn from the test source, the fact that the current is not represented on the SFG complicates the process. Consequently, in practice, a test current is preferable. As we shall see in the following examples, determining port impedances using DPI/SFG analysis is convenient because a good portion of the calculations are common with those for determining other transfer characteristics, thereby reducing the total work involved.

EXAMPLE 4.3 A UNITY-GAIN OPERATIONAL AMPLIFIER CIRCUIT

Besides illustrating the calculation of port impedances, this example also highlights how DPI/SFG analysis can be applied to circuits utilizing operational amplifiers. We wish to find expressions for the gain and the input and output resistance of the unity-gain buffer shown in Figure 4.10a while accounting for the finite gain and finite input and output resistance of the op amp.

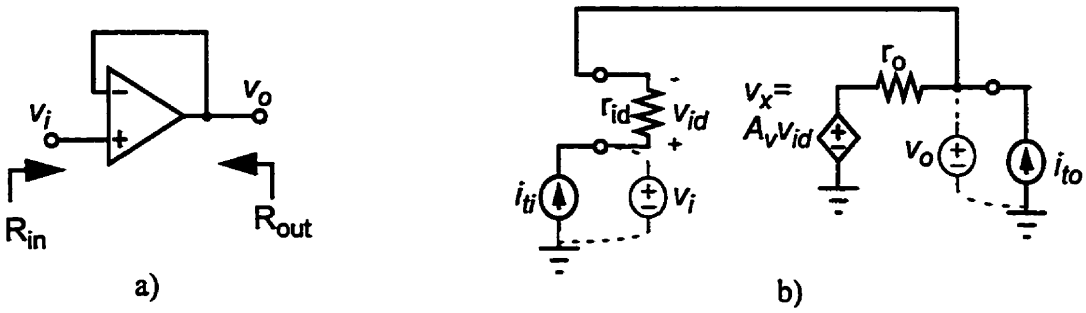


Figure 4.10 a) Unity-gain buffer, b) Schematic showing internal op amp model, and the test current sources for determining the input and output resistance.

Figure 4.10b shows the schematic of the unity-gain buffer complete with the op amp's internal model, and test current sources i_{ti} and i_{to} used to measure the input and output resistances respectively. The circuit has three nodes so we use the existing voltage source v_x, and place two auxiliary sources v_i and v_o at the input and output of the amplifier. In contrast to EXAMPLE 4.2, all voltage sources are referenced to ground. As such, calculating the short-circuit currents is much easier, and the intermediate SFG that is shown in Figure 4.11 can be readily determined by inspection. The final SFG shown in Figure 4.12 is obtained by explicitly representing the constraint on voltage source v_x,

$$v_x = A_v v_{id} = A_v v_i - A_v v_o.$$

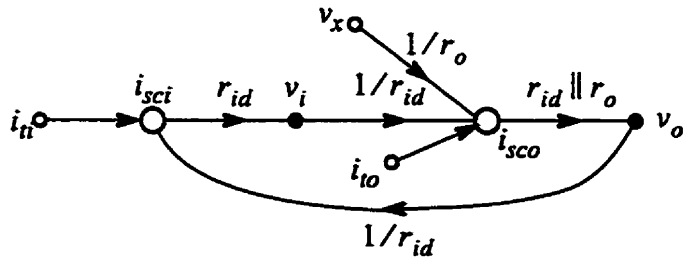


Figure 4.11 Signal-flow graph for unity-gain circuit prior to adding constraints on dependent sources.

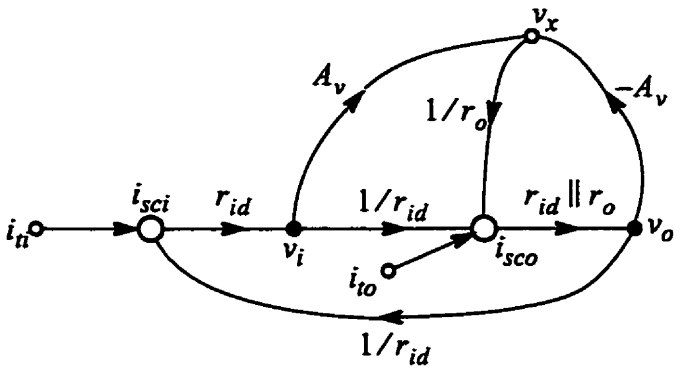


Figure 4.12 Final signal-flow graphs for unity-gain circuit showing all voltage constraints.

The final signal-flow graph can be simplified as shown in Figure 4.13 to highlight the relationships needed to find the gain and input and output resistances.

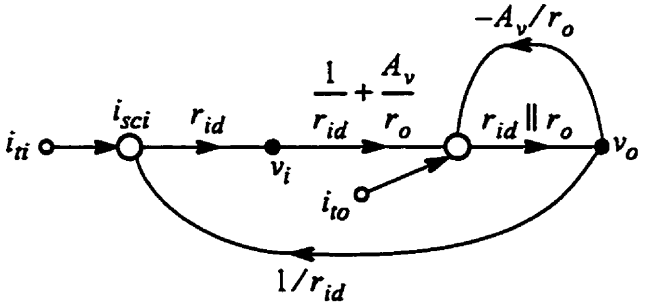


Figure 4.13 Simplified SFG from Figure 4.12.

The voltage gain can now be easily determined by inspection

$$\frac{v_o}{v_i} = \left(\frac{1}{r_{id}} + \frac{A_v}{r_o} \right) \times \frac{r_{id} \| r_o}{1 + r_{id} \| r_o \times A_v / r_o} \tag{4.8}$$

It is useful to note that, for the voltage gain, v_i is considered an independent source. Thus, the graph can be opened at node v_i using the substitution theorem, and the feedback path from v_o to i_{sci} can be disregarded. We can simplify Equation (4.8) by utilizing the fact that

$$r_{id} \gg r_o \qquad \text{and} \qquad 1/r_{id} \ll A_v/r_o$$

thus giving us the expected approximation of unity,

$$\frac{v_o}{v_i} \cong \frac{A_v}{r_o} \times \frac{r_o}{1 + A_v} = 1 - \frac{1}{1 + A_v} = \frac{A_v}{1 + A_v} \approx 1 \tag{4.9}$$

For the input resistance, we apply a test current i_{ti} while setting i_{to} to zero. We can use Equation (4.9) to simplify the expression for the input resistance

$$R_{in} \equiv \frac{v_i}{i_{ti}} = \frac{r_{id}}{1 - r_{id} \times \frac{v_o}{v_i} \times \frac{1}{r_{id}}} \cong \frac{r_{id}}{1 - \left(\frac{A_v}{1 + A_v}\right)} = r_{id}(1 + A_v) \tag{4.10}$$

Equation (4.10) is consistent with our knowledge that feedback increases the input resistance by a factor of $(1 + A_v)$. For the output resistance, we set the input voltage v_i to zero and apply test current i_{to}. With $v_i = 0$, the feedback loop from v_o to i_{sci} is again disabled, and the resulting resistance is

$$R_{out} \equiv \left.\frac{v_o}{i_{to}}\right|_{v_i = 0} = \frac{r_{id} \| r_o}{1 + r_{id} \| r_o \times A_v/r_o} \cong \frac{r_o}{1 + r_o \times A_v/r_o} = r_o/(1 + A_v) \tag{4.11}$$

Once again, Equation (4.11) is consistent with our knowledge that feedback *decreases* the output resistance by a factor of $(1 + A_v)$.

4.4.1 Deriving Blackman's Impedance Formula

In addition to determining the port impedances of general circuit networks, DPI/SFG analysis is particularly effective for analyzing feedback amplifiers. In this section, we illustrate how Blackman's Impedance Formula can be derived using DPI/SFG analysis. Although other derivations using signal-flow graphs exist [Robichaud,1961], the following derivation uses DPI/SFG analysis to derive the sig-

nal-flow graph of a general feedback amplifier.

To explain Blackman's Impedance Formula, consider the feedback amplifier model shown in Figure 4.14. Within the amplifier is a controlled source, w, that is related to the controlling quantity x by

$$w = kx$$

where k is constant parameter. Although shown as voltages in the figure, the quantities w and x may represent either voltages or currents. As initially presented in Section 2.4, Blackman's Impedance Formula states that the impedance at a port of a feedback amplifier is given by

$$Z_{port} = \frac{v_p}{i_p} = Z^\circ \frac{1 + T_{sc}}{1 + T_{oc}} \tag{4.12}$$

where

- T_{sc} is the return ratio with reference to controlled source w when the port is shorted to ground,
- T_{oc} is the return-ratio when the port is open-circuited, and
- Z° is the open-loop impedance, defined as the measured port impedance when the internal feedback is disabled, either by forcing the controlled source w to zero or equivalently by setting the parameter k to zero.

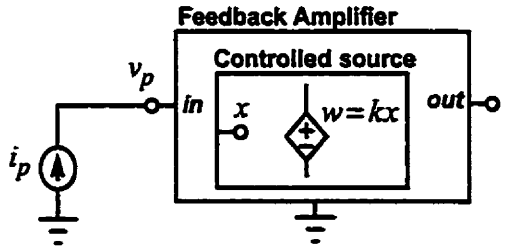


Figure 4.14 Feedback amplifier model.

In DPI/SFG analysis, the port impedance is determined by applying a test current, i_p, to the port of interest and measuring the resulting voltage, v_p. The SFG for the feedback amplifier is shown in Figure 4.15. The graph is complete in that all possible interactions between the port and the controlled source have been repre-

sented by the various transmittance branches. For instance, transmittance T_{wp} represents the overall transfer function from the controlled source w to the short-circuit current node of the port. In practice, these transmittance branches are determined through collapsing appropriate portions of the signal-flow graphs of actual circuits.

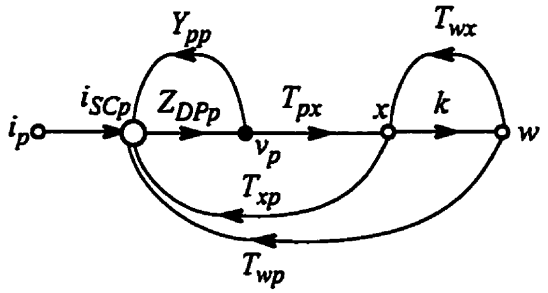


Figure 4.15 General SFG of feedback amplifier in Figure 4.14.

To relate the SFG in Figure 4.15 to Blackman's Impedance Formula, we need to re-represent the graph in terms of the open-loop impedance, Z^o. When the feedback is disabled, we obtain the graph shown in Figure 4.16a. The graph can be simplified down to Figure 4.16c where Z^o is given by

$$Z^o = \frac{Z_{DPp}}{1 - Z_{DPp}(Y_{pp} + T_{px}T_{xp})} .$$

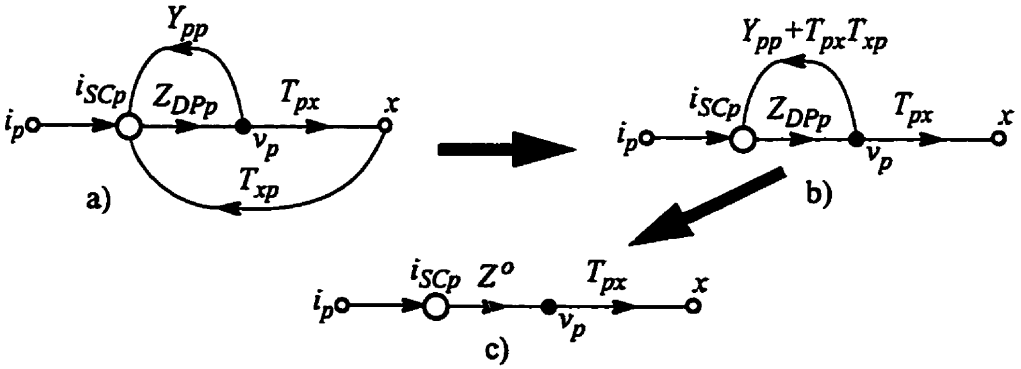


Figure 4.16 Collapsing the SFG of the feedback amplifier with feedback disabled.

The feedback amplifier can now be represented by the alternative SFG shown in Figure 4.17. Using Mason's Direct Rule to find the port impedance, v_p/i_p, we see

that

$$\begin{aligned} P_1 &= Z^\circ \\ \Delta_1 &= 1 - L_2 \\ \Delta &= 1 - (L_1 + L_2) \end{aligned} \tag{4.13}$$

and the port impedance is given by

$$Z_{port} \equiv \frac{v_p}{i_p} = \frac{P_1\Delta_1}{\Delta} = Z^\circ \frac{1 - L_2}{1 - (L_1 + L_2)} \tag{4.14}$$

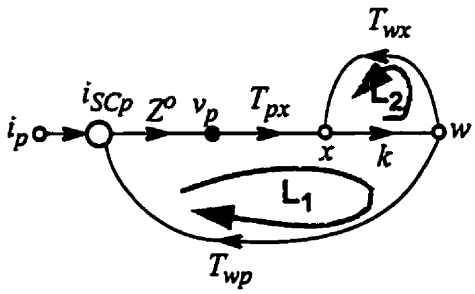


Figure 4.17 Alternative SFG for the feedback amplifier.

Equation (4.14) is in fact an alternative representation of Blackman's Impedance Formula. To recognize this, we need to determine the physical significance of the terms L_2 and $(L_1 + L_2)$. Because w is a controlled source, it is possible to split node w into separate source and sink nodes, w_{source} and w_{sink} as shown in Figure 4.18.

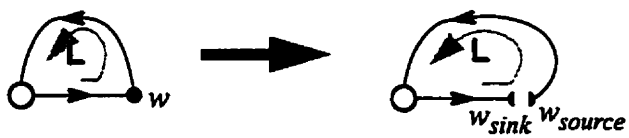


Figure 4.18 Splitting node w.

The loop transmittance, L, is equal to the ratio, w_{sink}/w_{source}, which is simply the negative of the return ratio T_w that is referenced to the controlled source, w. From Figure 4.17, we can see that

$$L_2 = -T_w\big|_{v_p = 0}$$

$$L_1 + L_2 = -T_w\big|_{i_p = 0}$$

Forcing the port voltage to zero is equivalent to shorting the port to ground. Thus, $-L_2$ is equivalent to the *short-circuit return-ratio*, T_{sc}. Similarly, forcing the port current to zero is equivalent to open-circuiting the port. Thus, $-(L_1 + L_2)$ is equal to the *open-circuit return-ratio*, T_{oc}. Consequently, Equation (4.14) can be rewritten as

$$Z_{port} = Z^{\circ}\frac{1 + T_{sc}}{1 + T_{oc}}$$

and we have back our original form of Blackman's Impedance Formula.

The above analysis illustrates the ease with which Blackman's Impedance Formula can be derived using DPI/SFG analysis. Indeed, the formula as represented in Equation (4.14) can be obtained by inspection, and most of the effort above was in relating the SFG in Figure 4.15 and the terms in Equation (4.14) to the established concepts of return-ratios and open-loop impedance. Our derivation makes no assumption of the nature of the internal feedback in the amplifier. The derivation is simple, and in contrast with existing derivations, avoids the need to assume an active element (i.e., a triode vacuum tube in [Blackman,1943] or a controlled voltage source in [Rosenstark,1986], [Chen,1991]). Such assumptions are required when the analysis is performed in terms of return-ratios because, in practice, return-ratios need to be determined through a process of analyzing modified versions of the original circuit. In DPI/SFG analysis, the need for return-ratios is altogether eliminated.[3]

In DPI/SFG analysis, all manipulations are performed on the *signal-flow graph* representation of the circuit — not on the actual circuit. Because the signal-flow graph is an abstract algebraic representation, graph manipulations can be performed freely without fear of altering the behaviour of the circuit. In contrast, the traditional application of Blackman's Impedance Formula requires one to perform a sequence

3. Although we can readily determine them in DPI/SFG analysis, return-ratios are no longer a necessity.

of circuit modifications where the port in question is alternately shorted to ground and then opened up, the feedback loop is broken, and where test signals are injected into internal nodes. The process is extremely intrusive, and only if all the manipulations of the circuit are performed properly is the final result correct.

4.5 ANALYZING TRANSISTOR CIRCUITS

In this section, we apply the DPI/SFG method to transistor circuits. Because transistors are basic devices that exhibit many nonidealities, transistor circuits are in general more challenging to analyze than circuits comprised of higher level building blocks such as op amps. The analysis of transistor feedback amplifiers is particularly challenging; often times, the unilateral assumptions commonly made of the feedforward and feedback portions of the circuit do not hold. Bipolar transistors, for instance, are not unilateral even at dc. One of the major strengths of DPI/SFG analysis is its ability to visually represent such complex interactions.

4.5.1 Signal-Flow Graphs of Transistors

Prior to analyzing transistor circuits, we need to develop the signal-flow graphs (SFGs) of individual devices. We can then use these SFGs to derive the larger SFGs of complete circuits. Figure 4.19 shows the basic bipolar transistor with impedances attached to each terminal. The impedances have been included to make explicit their contribution to the SFG of the device.

The associated small-signal T-model and hybrid-π model representations of the circuit are shown in Figure 4.20a and Figure 4.20b respectively. In our analysis, it is helpful to keep in mind the following relations:

$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m} \qquad \alpha = \frac{\beta}{\beta + 1} \tag{4.15}$$

In addition, there are three other relationships that can be easily derived:

$$r_e = r_\pi \| \frac{1}{g_m} \qquad r_\pi = r_e \| \left(-\frac{1}{g_m} \right) \qquad g_m = \frac{1}{r_e} + \frac{1}{r_\pi}$$

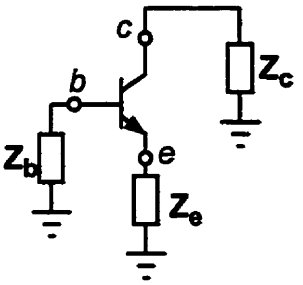
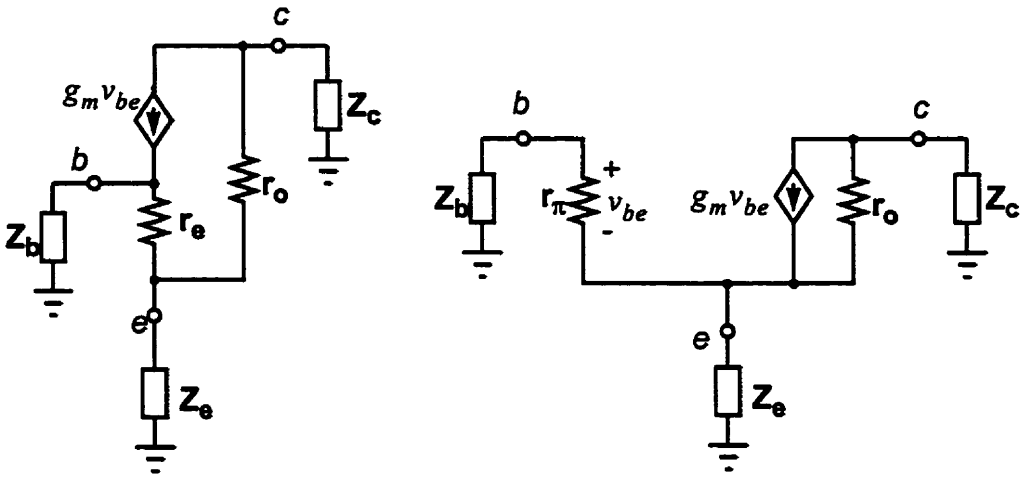


Figure 4.19 Bipolar transistor with impedances on each terminal.

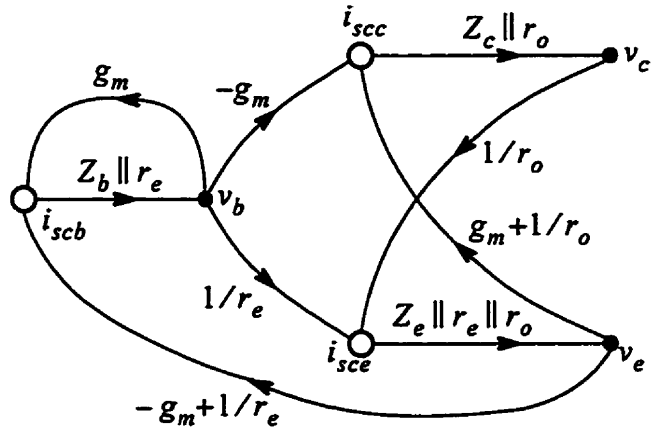


a) T-model b) Hybrid-π model

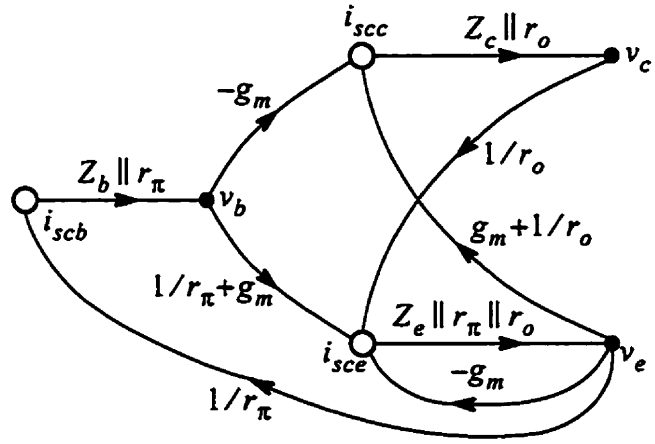
Figure 4.20 Two common small-signal models of BJT transistors.

By applying DPI/SFG analysis to the small-signal models in Figure 4.20, we obtain the two SFGs shown in Figure 4.21. Notice that feedback exists even in single-transistor circuits, and that the location of the feedback depends on the small-signal model. In the T-model, the transconductance element feeds into the base. Consequently, the feedback is represented by a loop around the base. Similarly, in the hybrid-π model, the feedback is represented with a loop around the emitter. While both models are equivalent in terms of their terminal behaviour, the T-model better represents the physical operation of the bipolar transistor. Specifically, it

shows for an npn device, the redirection of electrons from the base to the collector by virtue of the transconductance element.



a) T-model



b) Hybrid-π model

Figure 4.21 Corresponding signal-flow graphs for the two small-signal models shown in Figure 4.20.

The SFG for MOS transistors can be derived in the same manner. Although the MOS transistors can also be modeled with both the T-model and the hybrid-π model, the hybrid-π model as shown in Figure 4.22 better reflects the physical operation of the device because the gate is explicitly shown as an open circuit. With the T-model, the gate appears to be connected to the voltage-controlled current source and the source resistance, and it is only the exact relationship between these two elements that ensures the gate current remains zero. The body effect can been incorpo-

rated into the model by adding the term g_s to the transmittances originating from the source voltage node, v_s. The SFG of the hybrid-π model is shown in Figure 4.23; apart from the renaming of the terminals, the SFG of the MOSFET is very similar to that of the bipolar transistor.

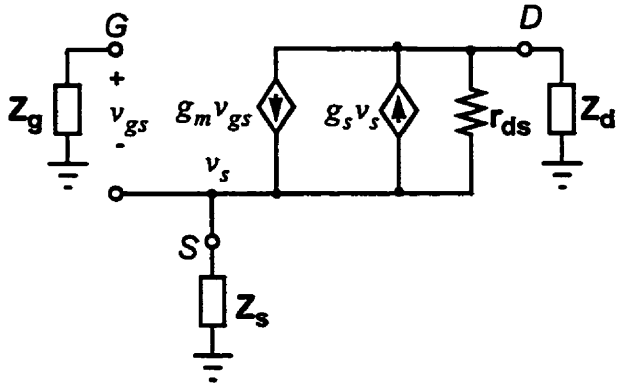


Figure 4.22 Small-signal hybrid-π model of a MOS transistor.

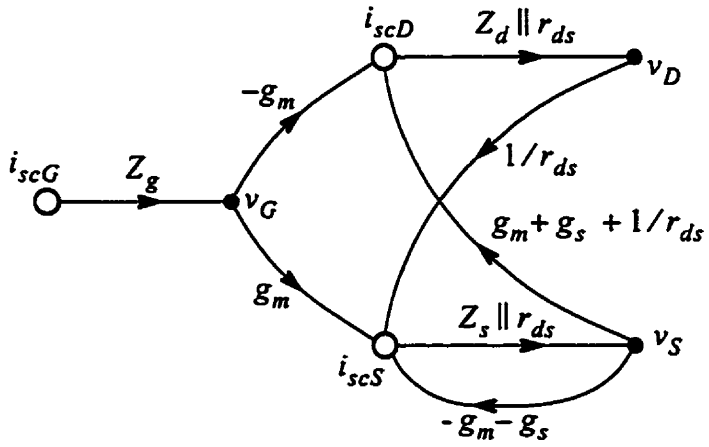


Figure 4.23 SFG for a MOSFET based on the hybrid-π model.

The small-signal transistor models presented here are sufficient for many applications. However, more complex small-signal models exist that better model a transistor's performance at high frequencies. High-frequency models for both bipolar and MOS transistors are presented in Appendix B. Included with the models are the corresponding signal-flow graphs.

4.5.2 Transistor Circuit Examples

EXAMPLE 4.4 A SOURCE FOLLOWER AMPLIFIER

We want to determine the gain of the source follower amplifier shown in Figure 4.24. The amplifier is biased with a simple current mirror, and it can be easily shown that the impedance looking into the output of the current mirror is simply r_{ds2}. As such, the SFG for the amplifier is essentially the SFG of transistor M_1 as shown in Figure 4.25. Since the drain of M_1 is connected to ground in the small-signal sense, much of the SFG for the MOSFET can be eliminated, as illustrated by the dashed lines. The gain of the amplifier can be seen to be

$$\begin{aligned}\frac{v_{out}}{v_{in}} &= g_{m1} \times \frac{r_{ds1} \parallel r_{ds2}}{1 + (r_{ds1} \parallel r_{ds2}) \times (g_{m1} + g_{s1})} \\ &= \frac{g_{m1}}{g_{m1} + g_{s1} + 1/r_{ds1} + 1/r_{ds2}} \\ &\approx \frac{g_{m1}}{g_{m1} + g_{s1}}\end{aligned} \tag{4.16}$$

which is the expected voltage gain of a source follower when the body effect is taken into account.

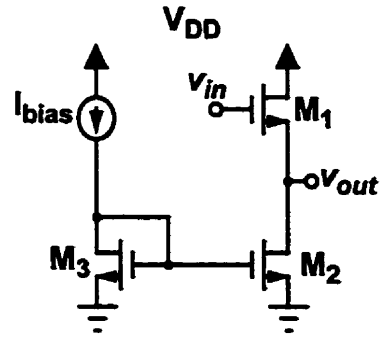


Figure 4.24 Source follower amplifier.

Note that the final gain expression in Equation (4.16) can be obtained directly by applying the Source Absorption Theorem.[4] From a DPI/SFG perspective, the trans-

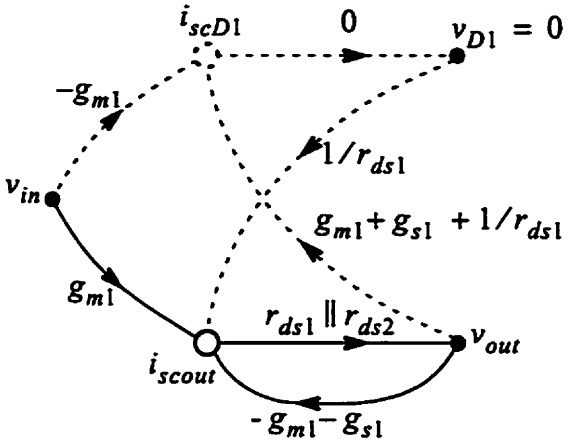


Figure 4.25 SFG for the source follower amplifier.

conductance feedback path is collapsed to create a single forward path whose transmittance is simply the original DPI of the node with a new resistance of $1/g_m$ placed in parallel as shown in Figure 4.26.

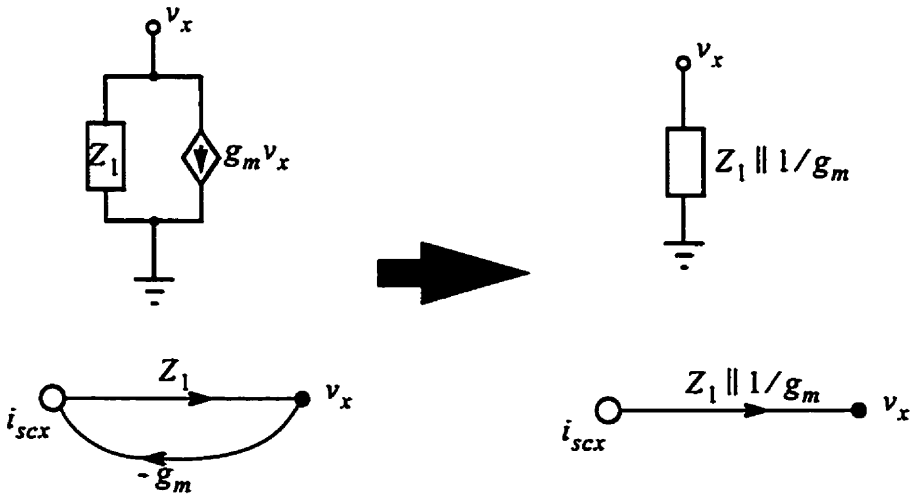


Figure 4.26 The source absorption theorem: collapsing a transconductance feedback path into a resistance.

One of the common challenges of analyzing the source follower amplifier is recognizing that feedback exists in the amplifier. With DPI/SFG analysis, the feedback is explicitly represented in the SFG. Moreover, we have shown that this difficulty in

4. See [Sedra, 1998], Appendix E.

recognizing the feedback can be traced to the unintended use of the Source Absorption Theorem. Using this theorem has the unfortunate consequence of hiding the feedback because the transconductance element which feeds back a current in response to a voltage is represented only as a resistance. DPI/SFG analysis allows us to make a distinction, in essence bringing out lost details in the circuit's operation.

EXAMPLE 4.5 A CASCODE CURRENT MIRROR

This example illustrates the type of insight that DPI/SFG analysis provides in contrast to traditional nodal analysis. We wish to determine the output impedance of the MOSFET cascode current mirror shown in Figure 4.27. We begin by setting the dependent current source of transistor M_2 to zero, and obtain the small-signal diagram shown in Figure 4.28.

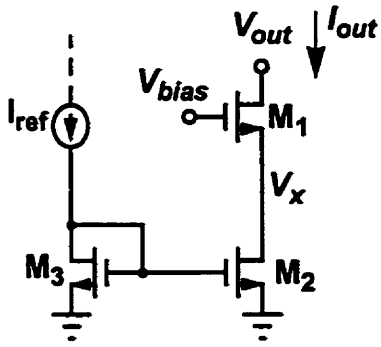


Figure 4.27 MOS transistor cascode current mirror.

Solution using Nodal Analysis

Using Kirchhoff's Current Law at nodes *out* and x, gives us the following equations:

$$i_{out} + g_{m1}v_x + (v_x - v_{out})/r_{ds1} = 0 \tag{4.17}$$

$$-g_{m1}v_x + (v_{out} - v_x)/r_{ds1} = 0 \tag{4.18}$$

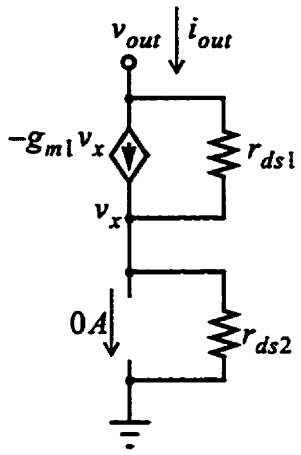


Figure 4.28 Small-signal circuit for determining output resistance of cascode current mirror.

Either by substituting Equation (4.18) into (4.17) or simply by noting that the current i_{out} is forced to flow through r_{ds2}, we obtain

$$v_x = i_{out} r_{ds2} \tag{4.19}$$

By finding an expression for v_x in terms of i_{out}, we can now solve the output resistance

$$\begin{aligned} R_{out} \equiv \frac{v_{out}}{i_{out}} &= r_{ds1} + r_{ds2} + g_{m1} r_{ds1} r_{ds2} \\ &= r_{ds2} + (1 + g_{m1} r_{ds2}) r_{ds1} \\ &\approx (1 + g_{m1} r_{ds2}) r_{ds1} \end{aligned} \tag{4.20}$$

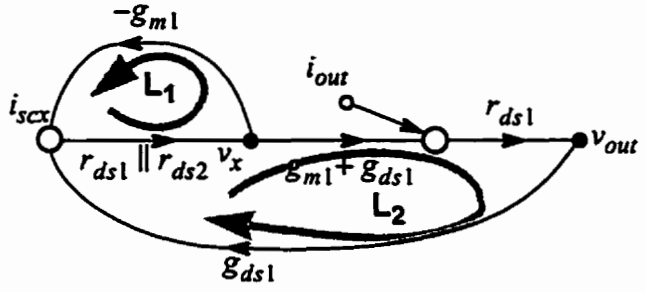
Equation (4.20) tells us that the output impedance of a cascode current mirror is enhanced by roughly $(1 + g_{m2} r_{ds2})$ times that of a simple current mirror. Apart from providing the correct algebraic result, however, nodal analysis provides little else in terms of understanding this circuit. Nodal analysis gives no insight into the feedback mechanism; the $(1 + g_{m2} r_{ds2})$ term resembles the common feedback expression $(1 + A\beta)$ but it is unclear how we can relate the two expressions, and why an additional r_{ds2} term appears in the answer.

Trying to analyze this circuit using topology-based feedback analysis is challenging; comprised of only a single dependent current source and two resistors, it is

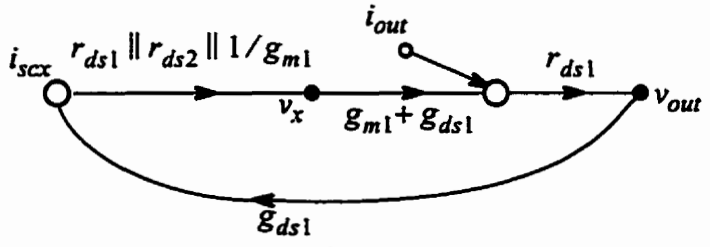
unclear what feedback topology (e.g., shunt-series) is applicable, and how the circuit can be partitioned into a forward amplifier and feedback network. It turns out that this circuit actually employs unconditionally stable *positive* feedback — a situation that is normally not considered in topology-based feedback analysis.

Solving using DPI/SFG Analysis

The SFG for the small-signal circuit in Figure 4.28 is given in Figure 4.29a. We see immediately that there are two feedback loops in this circuit. Loop L_1 is the feedback provided by the transconductance associated with transistor M_1. Since the loop gain of L_1 is $g_{m1}(r_{ds1} \| r_{ds2}) \gg 1$, the transmittance from i_{scx} to v_x is roughly $1/g_{m1}$. Thus, feedback causes node x to appear as a low impedance node even though its driving-point impedance of $r_{ds1} \| r_{ds2}$ is quite high.



a)



b)

Figure 4.29 SFG for determining output resistance of cascode current mirror a) complete graph, b) graph showing only main feedback loop.

In order to help us analyze loop L_2, we can collapse loop L_1 using the Source Absorption Theorem as shown in Figure 4.29b. The loop gain of L_2 is

$$L_2 = (r_{ds1} \| r_{ds2} \| 1/g_{m1})(\ g_{m1}+g_{ds1}) \times r_{ds1} \times g_{ds1} = \frac{g_{m1}+g_{ds1}}{g_{ds1}+g_{ds2}+g_{m1}} \tag{4.21}$$

$$= 1 - \frac{g_{ds2}}{g_{ds1}+g_{ds2}+g_{m1}} \approx 1 - \frac{g_{ds2}}{g_{m1}} < 1$$

Equation (4.21) shows that L_2 is positive and that we have a positive feedback loop. Stability is guaranteed because the loop gain is less than one; however, the value will be close to one since $g_{ds2}/g_{m1} \approx 0$. The output impedance is given by the closed-loop expression

$$R_{out} \equiv \frac{v_{out}}{i_{out}} = \frac{A}{1-A\beta} = \frac{r_{ds1}}{1-L_2} = r_{ds1} \times \frac{g_{ds1}+g_{ds2}+g_{m1}}{g_{ds2}}$$

$$= r_{ds1} \times \frac{g_{ds1}+g_{ds2}+g_{m1}}{g_{ds2}} = r_{ds1}+r_{ds2}+g_{m1}r_{ds1}r_{ds2} \tag{4.22}$$

$$\approx (1+g_{m1}r_{ds2})r_{ds1}$$

As expected, we obtain the same expression as Equation (4.20). We can now see that the output impedance will be enhanced because r_{ds1} is divided by $(1-L_2)$ which is near zero. In the process of obtaining the answer, we have gained a deeper understanding of the circuit using DPI/SFG analysis compared with using nodal analysis.

4.6 SUMMARY

In this chapter, we brought together the essential elements of the DPI/SFG analysis method. We advanced the current understanding of DPI/SFG analysis with the following contributions:

- We developed a general formulation of the method, first by justifying driving-point impedance analysis as a cause-and-effect interpretation of Kirchhoff's Current Law, and then by applying signal-flow graph theory.
- We extended the DPI/SFG analysis procedure to handle circuits with floating voltage sources.
- We used the method to derive Blackman's Impedance Formula.
- We derived the small-signal signal-flow graphs of both bipolar and MOS transistors.

Throughout the chapter, we have provided original examples that serve to highlight the relative strengths of DPI/SFG analysis over existing circuit analysis techniques. We showed that while nodal analysis is exact, it provides little insight into a circuit's operation. DPI/SFG analysis stands out in its ability to provide greater insight into the dynamics of circuits without sacrificing accuracy.

A final point that can be raised about DPI/SFG analysis is whether the method, with its driving-point impedances and short-circuit currents, truly represents reality. Specifically, DPI/SFG analysis imposes a cause-and-effect relationship between currents and voltages when, in truth, voltages and currents are inseparable. Just as chickens create eggs as much as eggs create chickens, the question of which came first is irrelevant from a design perspective, and is a matter best left to philosophers and evolutionary theorists. Modeling dynamic systems using cause-and-effect relationships has long been used by engineers because it is effective. As long as we do not lose sight that our models are just that — models — our practice of imposing order on reality should continue to serve our engineering purposes well.

REFERENCES

R. B. Blackman, "Effect of Feedback on Impedance," *Bell System Tech. Journal*, vol. 22, pp. 269-277, Oct. 1943.

L. S. Bobrow, *Elementary Linear Circuit Analysis*, 2nd Ed., HRW Inc., New York, NY, Chapter 2, pp. 65-69, 1987.

W. K. Chen, *Active Network Analysis*, World Scientific, Singapore, 1991.

A. Davis, *Linear Circuit Analysis*, Harper, New York, pp.167-168, 1998.

A. M. Davis, "Some Fundamental Topics in Introductory Circuit Analysis: A critique," *IEEE Trans. on Education*, vol. 43, no.3, pp. 330-335, August 2000.

R. D. Kelly, "Electronic Circuit Analysis and Design by Driving-Point Impedance Techniques," *IEEE Trans. on Education*, vol. E13, no. 3, pp. 154-167, Sept. 1970.

S. J. Mason and H. J. Zimmermann, *Electronic Circuits, Signals and Systems*, J. Wiley and Sons Inc., New York, Chapter 5, 1960.

A. Ochoa, "On Stability in Linear Feedback Circuits," *Proc. of IEEE Mid-West Symp. Circ. and Syst.*, pp. 51-55, Aug. 1997.

A. Ochoa, "A Systematic Approach to the Analysis of General and Feedback Circuits and Systems Using Signal Flow Graphs and Driving-Point Impedance," *IEEE Trans. Circ. and Syst. II*, vol. 45, no. 2, pp. 187-195, Feb. 1998.

A. Ochoa, 1999a. *Crystal Clear Circuit Analysis: Graph Algebra, Port Impedance, and Noise Translations Using DPI/SFG*, published by QEDesign, 1179 Blue Bird Canyon Trail, Vista, CA 92084.

A. Ochoa, 1999b. "Translating Noise Signals in Linear Circuits," *Proc. of IEEE Mid-West Symp. Circ. and Syst.*, Las Cruces, NM, pp. 51-55, Aug. 1999.

S. Rosenstark, *Feedback Amplifier Principles*, Macmillan Publishing Co., New York, Chapter 2, 1986.

L. P. A. Robichaud, M. Boisvert, and L. Robert, *Graphes de Fluence*, Presses de l'Universite Laval, Quebec, pp. 60-63, 1961 (French).

A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, 4th Ed., Oxford Univ. Press, New York, Chapter 8, p. 701, 1998.

CHAPTER

5 Circuit Design Using the DPI/SFG Method

This chapter makes use of the DPI/SFG analysis method in the design of the low-voltage transimpedance amplifier introduced in Chapter 3. The preamplifier is shown again in Figure 5.1. We begin from an analysis perspective by using DPI/SFG analysis to derive algebraic expressions of the main transfer characteristics of the preamplifier. We then approach the circuit from a design perspective, using DPI/SFG analysis to derive a simplified model of the preamplifier and to derive a set of relations that characterize the main design trade-offs to be made with regards to speed, noise, and gain. We verify the accuracy of our model by comparing our analytic results with those obtained from SPICE circuit simulations. Having verified the analytic model, we proceed to explore the design space of the preamplifier in order to arrive at our final circuit design.

Additional preamplifier requirements such as dynamic range and photodiode bias voltage are not discussed here because such characteristics relate to the large-signal behaviour of the preamplifier, and do not require detailed small-signal analysis.

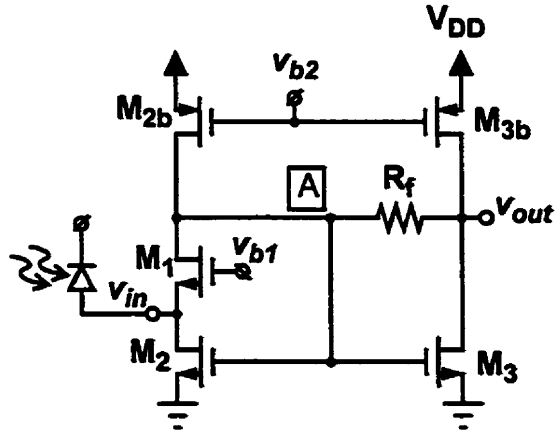


Figure 5.1 Proposed low-voltage optical preamplifier.

5.1 ANALYSIS OF THE LOW-VOLTAGE TRANSIMPEDANCE AMPLIFIER

The small-signal circuit of the optical preamplifier is shown in Figure 5.2. The following simplifications were made:

- The drain-source resistances of all transistors can be ignored because all nodes of the circuit are relatively low impedance.
- The body effect only applies to M_1 since the sources of M_2 and M_3 are grounded.
- The main parasitics have been lumped together into admittances Y_{in}, Y_A, and Y_L. Thus

$$Y_{in} = sC_{in} = s(C_{PD} + C_{gs1} + C_{db2}) \tag{5.1}$$

$$Y_A = sC_A = s(C_{gs2} + C_{gs3} + C_{db1} + C_{dbp2}) \tag{5.2}$$

$$Y_L = sC_L = s(C_{OUT} + C_{dbp3} + C_{db3}) \tag{5.3}$$

$$Y_f = 1/R_f + sC_f \tag{5.4}$$

where C_{PD} is the capacitance of the photodiode, C_{OUT} is the output load capacitance, and C_{gs} and C_{db} are respectively the various gate-source and drain-bulk parasitic capacitances found in the circuit.

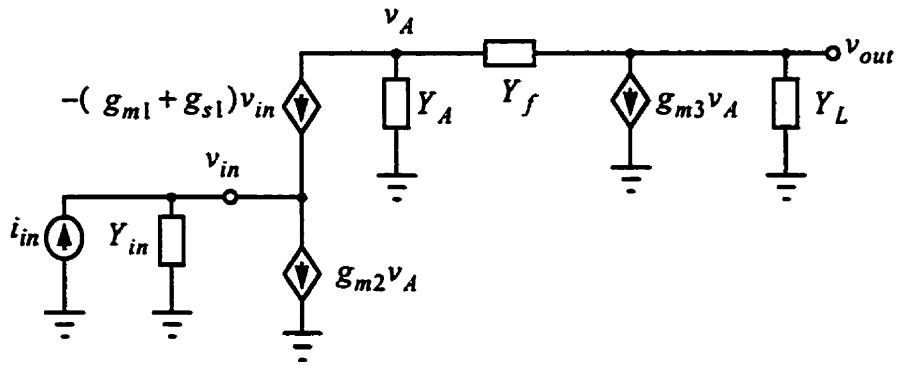


Figure 5.2 Small-signal circuit of optical preamplifier.

The signal-flow graph of the preamplifier is shown in Figure 5.3 superimposed on the circuit schematic. Figure 5.3 illustrates how the structure of the SFG mirrors that of the circuit, enabling a designer to better visualize the circuit's dynamic behaviour. The SFG is redrawn in Figure 5.4 to highlight the feedback loops in the circuit. The preamplifier contains three feedback loops: L_1, the transconductance

feedback that is associated with the common-gate configuration of M_1, L_2, the feedback loop that extends from the input terminal to the gate of M_2 through M_1, and L_3, the feedback loop around M_3 through resistor R_f. The presence of overlapping feedback loops makes this structure difficult for analysis using conventional feedback techniques.

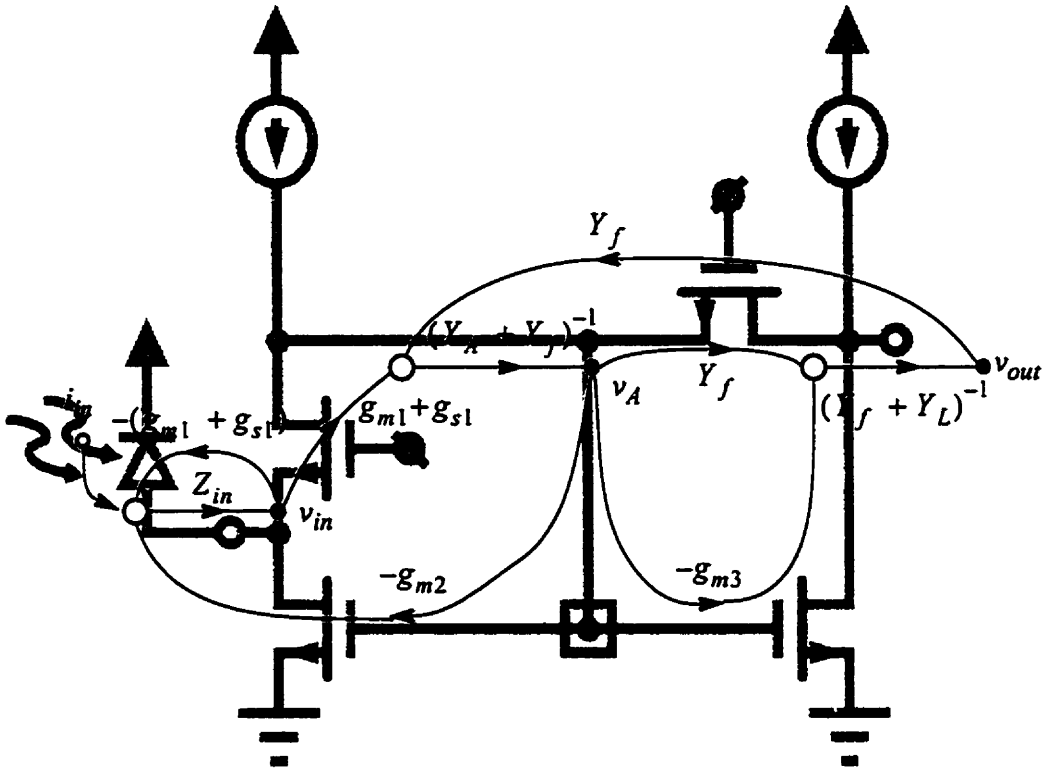


Figure 5.3 Signal-flow graph of optical preamplifier superimposed on circuit schematic.

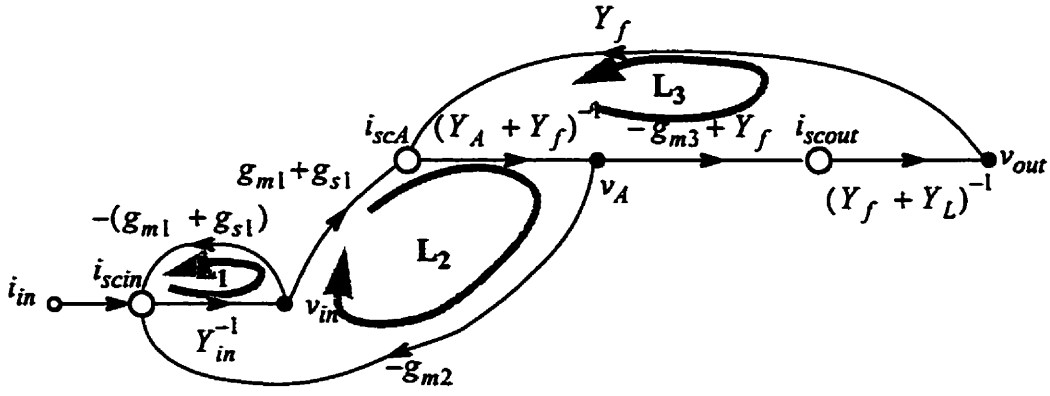


Figure 5.4 Signal-flow graph of preamplifier highlighting the existing feedback loops.

The transimpedance gain of the circuit can be determined using Mason's Direct Rule. The basic expression is

$$\frac{v_{out}}{i_{in}} = \frac{P_1\Delta_1}{1-(L_1+L_2+L_3)+L_1L_3} \tag{5.5}$$

where P_1 is the forward transmission path from i_{in} to v_{out},

$$P_1 = \frac{(g_{m1}+g_{s1})(-g_{m3}+Y_f)}{Y_{in}(Y_A+Y_f)(Y_f+Y_L)} \tag{5.6}$$

and loops L_1, L_2, and L_3 are given by

$$L_1 = \frac{-(g_{m1}+g_{s1})}{Y_{in}} \tag{5.7}$$

$$L_2 = \frac{-g_{m2}(g_{m1}+g_{s1})}{Y_{in}(Y_A+Y_f)} \tag{5.8}$$

$$L_3 = \frac{(-g_{m3}+Y_f)Y_f}{(Y_A+Y_f)(Y_f+Y_L)} \tag{5.9}$$

By combining Equations (5.1) through (5.9), we can obtain the following expression for the transimpedance gain:

$$\frac{v_{out}}{i_{in}}(s) = \frac{1/R_f+sC_f-g_{m3}}{a_3s^3+a_2s^2+a_1s+a_0} \tag{5.10}$$

where the coefficients of the denominator are given by

$$a_3 = \frac{C_{in}}{(g_{m1}+g_{s1})}[C_AC_L+C_f(C_A+C_L)]$$

$$a_2 = \frac{C_{in}}{g_{m1}+g_{s1}}\left(g_{m3}C_f+\frac{C_A+C_L}{R_f}\right)+C_AC_L+C_f(C_A+C_L)$$

$$a_1 = \frac{C_{in}g_{m3}}{(g_{m1}+g_{s1})R_f}+g_{m2}C_L+(g_{m2}+g_{m3})C_f+\frac{C_A+C_L}{R_f}$$

$$a_0 = (g_{m2}+g_{m3})/R_f$$

At dc, the transimpedance gain is

$$\frac{v_{out}}{i_{in}}(0) = \frac{g_{m3}R_f - 1}{g_{m2} + g_{m3}} \tag{5.11}$$

which is the same expression as Equation (3.13) that we derived in Chapter 3 using the simplified dc circuit model.

To further demonstrate the accuracy of Equation (5.10), we looked at four designs with different sets of transistor and resistor parameters, and we simulated these circuits in SPICE and then extracted the small-signal parameters and used them in Equation (5.10). The analytic and SPICE simulation results are plotted together in Figure 5.5. The results are in excellent agreement within 1dB and validate the initial approximations made in the small-signal circuit.

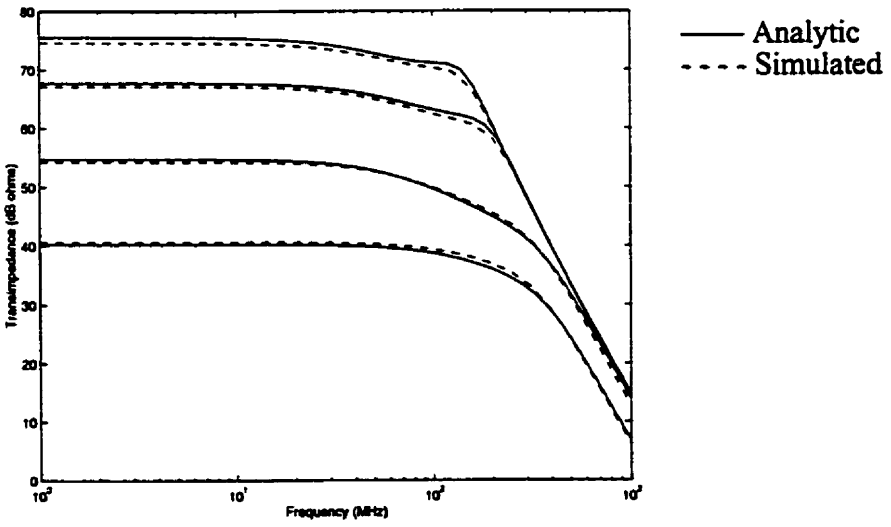


Figure 5.5 Comparison of simulated vs. analytical frequency responses of four preamplifier designs.

Thus far we have done little more than verify the accuracy of both our analytic expressions and the signal-flow graph of the circuit. Equation (5.10) is of little use from a design perspective because it is extremely large and cumbersome. To truly aid the design and optimization of the preamplifier, we need to derive a simplified set of equations. The next section demonstrates how DPI/SFG analysis can be used to achieve this goal.

5.2 DEVELOPING AN ANALYTIC CIRCUIT MODEL

The critical performance characteristics of any optical preamplifier are its bandwidth and sensitivity. The bandwidth is governed by the frequency response while the sensitivity is determined by the noise performance. As such, we will use DPI/SFG analysis to derive a set of simple, yet accurate, analytic expressions that capture the essence of the preamplifier's frequency response and noise characteristics. In the process, we will derive a simple schematic model of the preamplifier's input and output impedance. Upon demonstrating the accuracy of our analytic model using SPICE simulation results, we will use the design equations to optimize the design.

5.2.1 Modeling the Frequency Response

Due to the significant capacitance of the photodiode as well as the capacitance of the bond pad and IC package, the dominant pole is typically located at the input of the preamplifier. As such, we can estimate the bandwidth of the preamplifier by using a first-order approximation of the amplifier's input impedance.

Finding this approximation involves simplifying the circuit's SFG and identifying the dominant terms in each of the branches. Figure 5.6 shows the initial process of simplification. Here, the local feedback loop around v_{in} and i_{scin} has been collapsed. From Equation (5.11), we know that the transimpedance gain is proportional to $(g_{m3}R_f - 1)$, and so can expect that $g_{m3}R_f$ is significantly larger than one, or equivalently, that $g_{m3} \gg 1/R_f$; since C_f is typically small and significant only at high-frequencies, we can make the approximation that

$$-g_{m3} + Y_f = -g_{m3} + 1/R_f + sC_f \approx -g_{m3}$$

In addition, the two branches from i_{scout} to i_{scA} can be combined to make

$$(Y_f + Y_L)^{-1} \times Y_f \approx \frac{1}{R_f} \times \frac{R_f}{1 + sR_fC_L} = \frac{1}{1 + sR_fC_L}$$

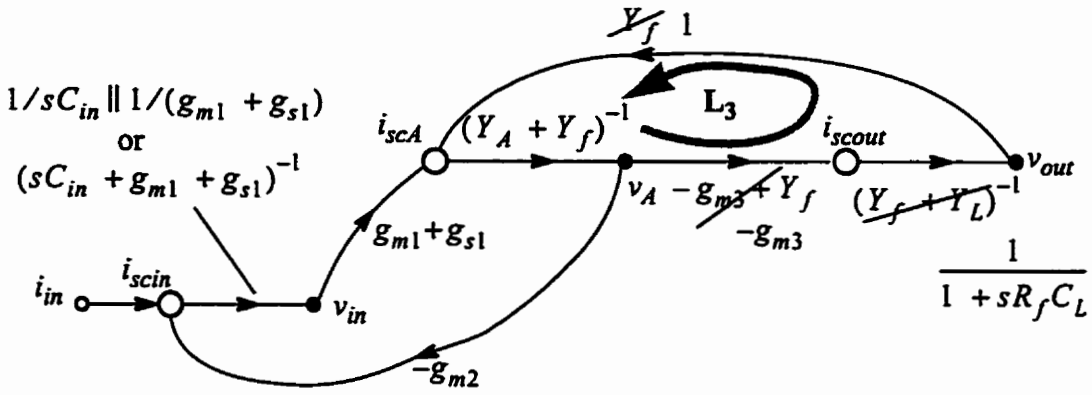


Figure 5.6 Simplified SFG from Figure 5.4

In order to simplify loop L_3, we determine its loop gain

$$L_3 \approx \frac{-g_{m3}}{(1 + sR_fC_L)(Y_f + Y_L)} = \frac{-g_{m3}R_f}{(1 + sR_fC_L)(1 + sR_fC_A)} \tag{5.12}$$

From our earlier assumption that $g_{m3}R_f \gg 1$, and assuming that the two pole frequencies of Equation (5.12) are significantly higher than the dominant pole, we can conclude that the loop gain L_3 is large. Thus, the overall transfer characteristic from i_{scA} to v_A is dominated by its feedback path, giving

$$\frac{v_A}{i_{scA}}(s) \approx \frac{1 + sR_fC_L}{g_{m3}}$$

As such, the entire SFG can be reduced to Figure 5.7, which when collapsed, can be represented schematically in Figure 5.8.

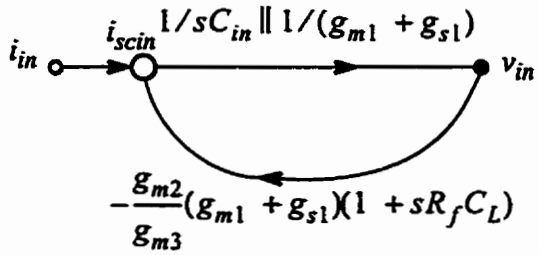


Figure 5.7 Simplified SFG from Figure 5.6

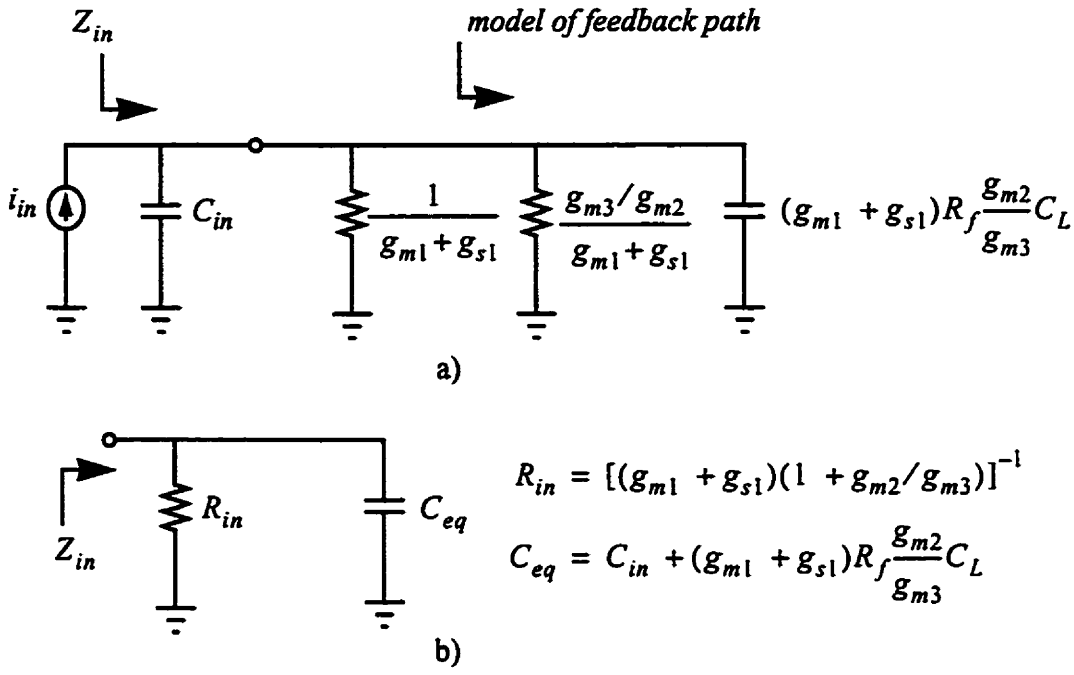


Figure 5.8 Schematic representation the SFG in Figure 5.6 a) complete b) lumped model.

Figure 5.8 is an important result because it shows us that the input of the preamplifier can be modelled by an RC network, and that the dominant pole is simply the inverse of the RC time constant,

$$\omega_{p1} = \frac{1}{R_{in}C_{eq}} = \frac{(g_{m1}+g_{s1})(1+g_{m2}/g_{m3})}{C_{in}+(g_{m1}+g_{s1})C_L R_f \frac{g_{m2}}{g_{m3}}} \tag{5.13}$$

where R_{in} is the input resistance of the preamplifier as obtained in Chapter 3 and given in Equation (3.15). The ratio g_{m3}/g_{m2} appears repeatedly in the equations we have derived. This ratio represents the gain of the current mirror. We will use the ratio as a design parameter in our investigation and denote it by the symbol K_{cm}.

To confirm the accuracy of our analytic expression for the dominant pole frequency, we can compare the bandwidth predicted from Equation (5.13) with that obtained through simulation using SPICE. The small-signal parameters used in the analytic expressions were extracted from the SPICE results. The analytical and

SPICE simulation results are plotted together in Figure 5.9 across a wide range of feedback resistance values and current mirror gains. The lower surface is a plot of ω_{p1} as defined by Equation (5.13) while the ringed meshed represents the extracted 3dB bandwidth of the preamplifier. For the most part, the dominant-pole accurately predicts the actual bandwidth. The agreement is slightly less accurate along the path marked by the arrow. From Equation (5.10) we know that the preamplifier exhibits a third-order frequency response, and that the higher-order poles can affect the overall bandwidth.

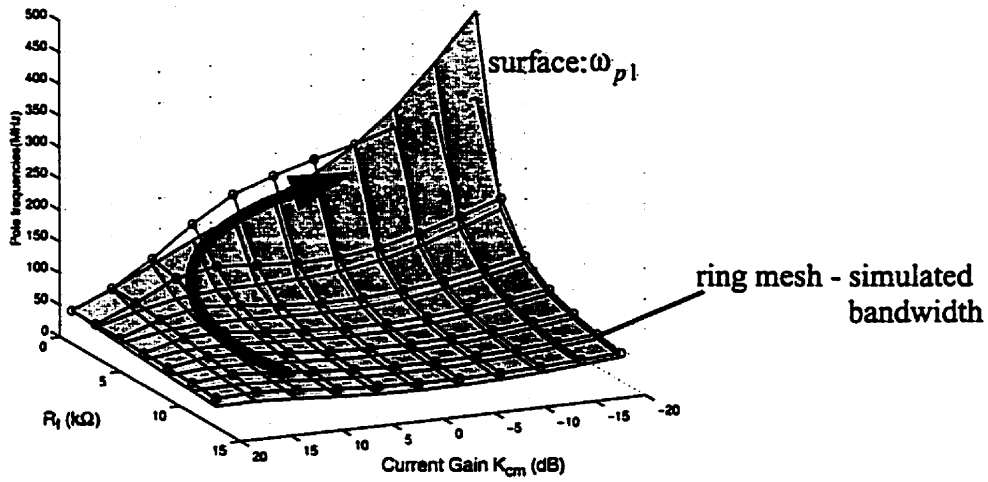


Figure 5.9 Plot of simulated bandwidth and ω_{p1} vs. feedback resistance and current mirror gain.

Equations (5.10) and (5.13) can be combined to derive the location of the higher order poles. Since the denominator of Equation (5.10) is third-order, if we assume the higher-order poles are complex, the denominator can be rewritten in factor form,

$$D(s) = K(s^3 + k_2 s^2 + k_1 s + k_0) = K(s + \omega_{p1})\left(s^2 + \frac{\omega_o}{Q}s + \omega_o{}^2\right) \qquad (5.14)$$

By equating the constant terms of Equations (5.10) and (5.14), we see that

$$\omega_{p1}\omega_o{}^2 = \frac{a_o}{a_3} \qquad (5.15)$$

Thus, the pole frequency, ω_o, of the complex-conjugate pair is given by

$$\omega_o^2 = \frac{g_{m3}}{R_f C_i} \times \frac{C_{in} + R_f C_L (g_{m2}/g_{m3})(g_{m1} + g_{s1})}{C_A C_L + C_f (C_A + C_L)} \tag{5.16}$$

Figure 5.10 shows a plot of ω_{p1} and ω_o as a function of R_f and the current mirror gain. For most of the design space, ω_o is significantly higher than ω_{p1}. However, along the path marked by the arrow, ω_o is closer to ω_{p1}. By adjusting the Q of the complex-conjugate pair, it is possible to provide some high-frequency boosting to help extend the bandwidth of the preamplifier.

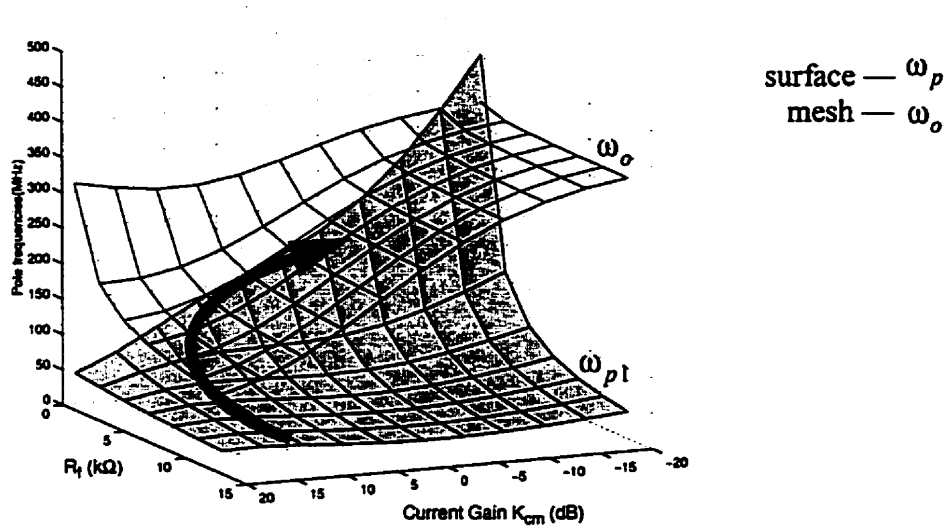


Figure 5.10 Plotting the preamplifier's pole frequencies vs. feedback resistance and current mirror gain.

5.2.2 Modeling the Amplifier Noise

The sensitivity of an optical preamplifier is limited by its noise performance. Figure 5.11 shows the thermal noise sources found within the low-voltage optical preamplifier. Although MOSFETs also produce flicker noise, flicker noise can be ignored in our design because the high bandwidth of the preamplifier makes thermal noise dominant. Figure 5.12 shows the preamplifier's SFG with the additional noise sources.

The thermal noise current generated by a resistor is given by

$$I_R^2(f) = \frac{4kT}{R} \tag{5.17}$$

in units of A^2/Hz where k is Boltzmann's constant ($1.38 \times 10^{-23} JK^{-1}$) and T is the absolute temperature in Kelvin. The thermal noise current of a MOSFET across its drain and source terminals is given by

$$I_d^2(f) = \gamma 4kTg_m \tag{5.18}$$

where γ is the excess noise factor and g_m is the transconductance of the device. Traditionally, an excess noise factor of 2/3 is used for long-channel devices, but for modern submicron MOSFETs, a higher value is necessary, the exact value of which is still under investigation [Abidi,1986].

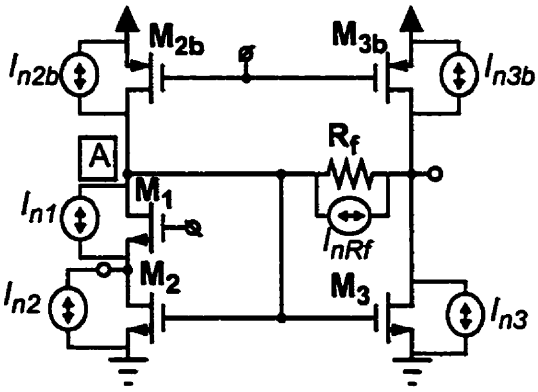


Figure 5.11 Noise sources within the low-voltage optical preamplifier.

Since the main objective is to compare the noise with the signal, we would like to refer all noise sources back to the input. This operation can be done by translating each noise component in the SFG back to the input node i_{scin} [Ochoa,1999].

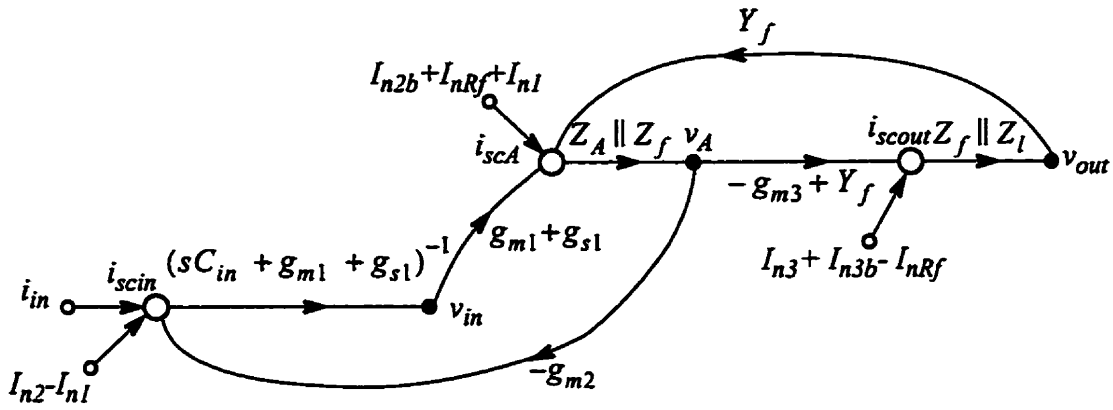


Figure 5.12 SFG of preamplifier with intrinsic noise sources.

I_{n1}:

Noise source I_{n1} provides two currents: a positive portion that is entering node A, and a negative portion that is leaving the input node. Since the negative portion is already input-referred, we only need to translate the positive portion of the noise source from node i_{scA} back to the input. The forward path from i_{scin} to i_{scA} is $(g_{m1}+g_{s1})/(sC_{in}+g_{m1}+g_{s1})$, and so we simply multiply by the inverse in order to translate backwards. Combining the positive and negative portions of I_{n1}, the net input-referred noise current is given by

$$\begin{aligned} I_{n1in}^2 &= \left| \frac{sC_{in}+g_{m1}+g_{s1}}{g_{m1}+g_{s1}} - 1 \right|^2 I_{n1}^2 \\ &= \left| \frac{sC_{in}}{g_{m1}+g_{s1}} \right|^2 I_{n1}^2 \end{aligned} \tag{5.19}$$

Essentially, Equation (5.19) tells us the noise contribution of I_{n1} is negligible at low frequencies and throughout most of the passband where $sC_{in} \ll (g_{m1}+g_{s1})$. We see from the SFG in Figure 5.12 that at dc, the two branches connected to node v_{in} precisely cancel each other. Consequently, a current that is injected into node A has the same effect as one injected at the input. As a result, the net noise contribution of I_{n1} is zero at dc, and practically negligible within the passband. Devices in cascode configuration such as M_1 generally do not contribute significant noise at

low frequencies. The effective cancellation of noise in this configuration has also been described in terms of a recirculation of the noise current within the cascode transistor [Buchwald,1995].

I_{n2}:

This noise source is already input-referred, so $I_{n2in}^2 = I_{n2}^2$.

I_{n2b}:

This noise current, like the positive component of I_{n1}, is injected into node i_{scA}, making its input-referred contribution

$$I_{n2bin}^2 = \left|\frac{sC_{in} + g_{m1} + g_{s1}}{g_{m1} + g_{s1}}\right|^2 I_{n2b}^2 = \left|1 + \frac{sC_{in}}{g_{m1} + g_{s1}}\right|^2 I_{n2b}^2 \qquad (5.20)$$

From the relation in Equation (5.20), we see that for much of the passband,

$$I_{n2bin}^2 \approx I_{n2b}^2$$

so that noise currents injected into node A are essentially input-referred. In other words, node A is practically identical to the input node from a noise perspective.

I_{n3} and I_{n3b}:

From a small-signal standpoint, current sources I_{n3} and I_{n3b} are identical, and we can analyze them together. Since these noise currents are injected directly into the output port, we can determine an expression for their input-referred equivalent values as a product of their effect on the output voltage and the transimpedance gain:

$$I_{n3(b)in}^2 = \left|\frac{i_{in}}{v_{out}} \times \frac{v_{out}}{i_{scout}}\right|^2 \times I_{n3(b)}^2 \approx \left|\left(\frac{v_{out}}{i_{in}}\right)^{-1}(s)\Big|_{s=0} \times Z_{out}(s)\right|^2 \times I_{n3(b)}^2 \qquad (5.21)$$

Our approximation of the transimpedance term using the dc value is justified because we are only interested in the input-referred noise spectrum within the pass-band where the transimpedance term lies within 3dB of the dc value. To determine the output impedance of the preamplifier, $Z_{out}(s)$, we can follow the same procedure that we used to derive a first-order model for the input impedance. The process of making successive approximations and collapsing the SFG is illustrated in Figure 5.13. Similar to our earlier analysis of the input impedance, we have been able to use DPI/SFG analysis to simplify the port impedance down to a simple RC network as shown in Figure 5.14. As expected, resistance component of the first-order model is simply the output resistance calculated in Chapter 3 and given in Equation (3.18).

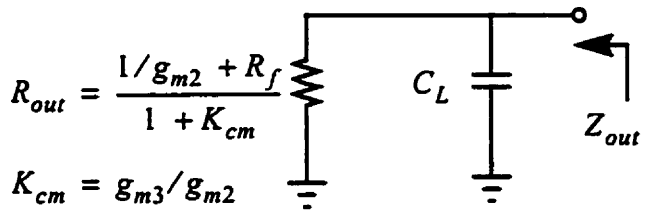
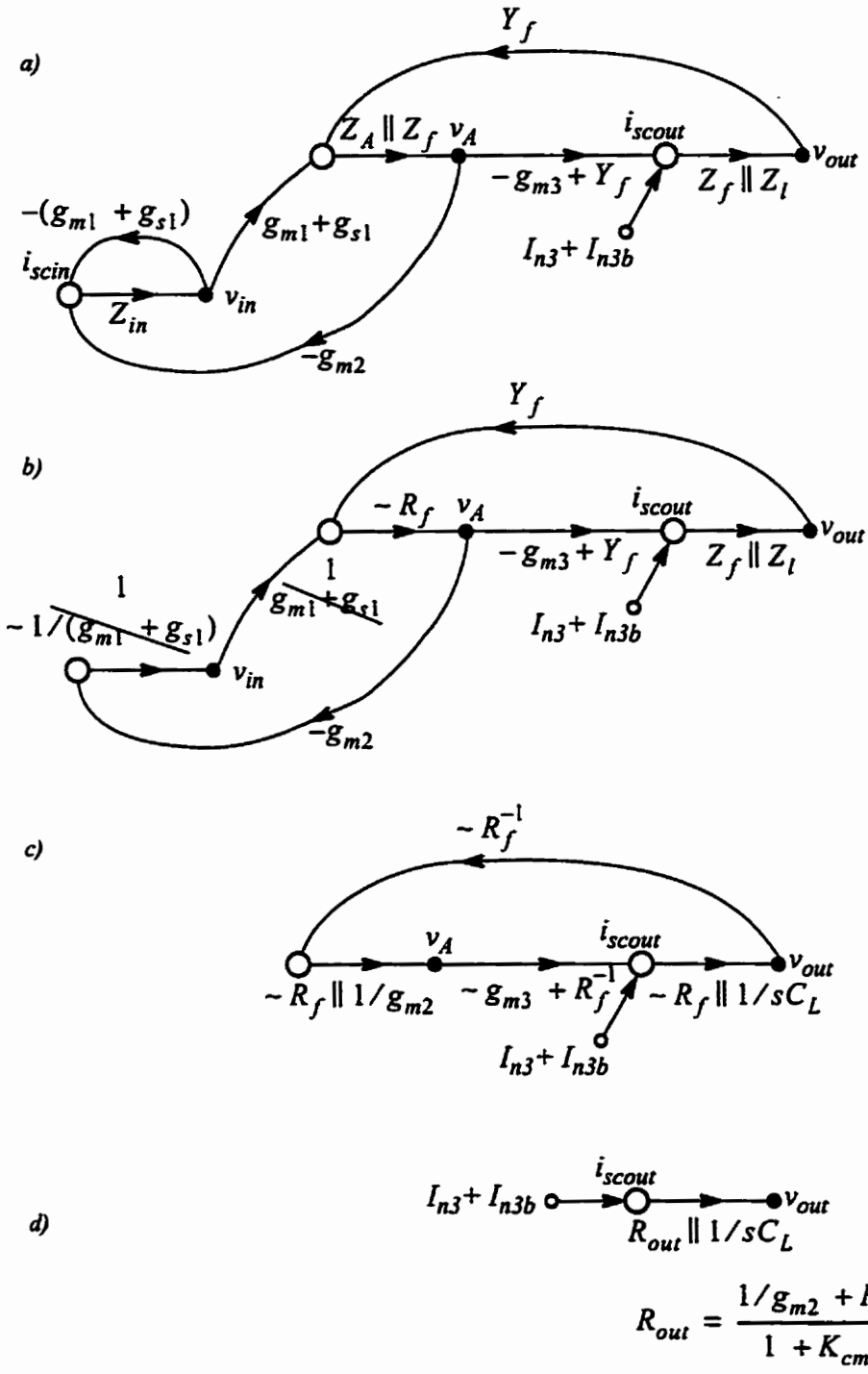


Figure 5.14 First-order model of the preamplifier output impedance.

We are now in a position to compute the input-referred equivalent of noise sources I_{n3} and I_{n3b}:

$$\begin{aligned} I^2_{n3(b)in} &= \left| \left(\frac{v_{out}}{i_{in}} \right)^{-1} \Bigg|_{s=0} \times Z_{out}(s) \right|^2 \times I^2_{n3(b)} \\ &= \left| \frac{\cancel{1 + K_{cm}}}{1/g_{m2} - K_{cm}R_f} \times \frac{1/g_{m2} + R_f}{\cancel{1 + K_{cm}}} \times \frac{1}{1 + sR_{out}C_L} \right|^2 \times I^2_{n3(b)} \qquad (5.22) \\ &= \left(\frac{1/g_{m2} + R_f}{1/g_{m2} - K_{cm}R_f} \right)^2 \times \left| \frac{1}{1 + sR_{out}C_L} \right|^2 \times I^2_{n3(b)} \end{aligned}$$



$$R_{out} = \frac{1/g_{m2} + R_f}{1 + K_{cm}}$$

Figure 5.13 Progressive approximation and collapsing of SFG in order to determine output impedance.

I_{nRf}:

Following the convention used in Figure 5.12, the noise current of the feedback resistor is injected into node A and drawn out of the output node. As such, the input-referred noise is the difference of the input-referred expressions for sources I_{n2b} and I_{n3b} given in Equations (5.20) and (5.22):

$$I_{nRfin}^2 = \left|\left(1 + \frac{sC_{in}}{g_{m1} + g_{s1}}\right) - \left(\frac{1/g_{m2} + R_f}{1/g_{m2} - K_{cm}R_f} \times \frac{1}{1 + sR_{out}C_L}\right)\right|^2 \times I_{nRf}^2$$

Total Input-Referred Noise

Combining the effects of all the independent noise components, we obtain the total input-referred noise current density of the optical preamplifier:

$$I_{ni}^2 = I_{n2in}^2 + I_{n2bin}^2 + I_{n3in}^2 + I_{n3bin}^2 + I_{nRfin}^2 \tag{5.23}$$

$$\begin{aligned} I_{ni}^2(s) = {} & I_{n2}^2 + \left|1 + s\frac{C_{in}}{g_{m1} + g_{s1}}\right|^2 \times I_{n2b}^2 \\ & + \left|\left(\frac{1/g_{m2} + R_f}{1/g_{m2} - K_{cm}R_f}\right) \times \frac{1}{1 + sR_{out}C_L}\right|^2 \times (I_{n3}{}^2 + I_{n3b}{}^2) \\ & + \left|1 + s\frac{C_{in}}{g_{m1} + g_{s1}} - \left(\frac{1/g_{m2} + R_f}{1/g_{m2} - K_{cm}R_f}\right) \times \frac{1}{1 + sR_{out}C_L}\right|^2 \times \end{aligned} \tag{5.24}$$

where

$$I_{n1}^2 = \gamma 4kTg_{m1} \qquad I_{n3(b)}^2 = \gamma 4kTg_{m3(b)}$$

$$I_{n2(b)}^2 = \gamma 4kTg_{m2(b)} \qquad I_{nRf}^2 = \frac{4kT}{R_f}$$

$$R_{out} = \frac{1/g_{m2} + R_f}{1 + K_{cm}}$$

are the constituent parameters.

To demonstrate the accuracy of Equation (5.24), we apply the equation to the same four preamplifier designs used earlier to verify the accuracy of our frequency response. Figure 5.15 plots the results obtained using Equation (5.24) together with the simulation results from SPICE. An excess noise factor of $\gamma = 2/3$ was used. The results are close within the passband of the designs, with the error increasing at high frequencies as expected because of our simplifying assumption that the transimpedance gain is flat. Within the passband, however, we confirm that our analytic results are no greater than 3dB off from the simulated results.

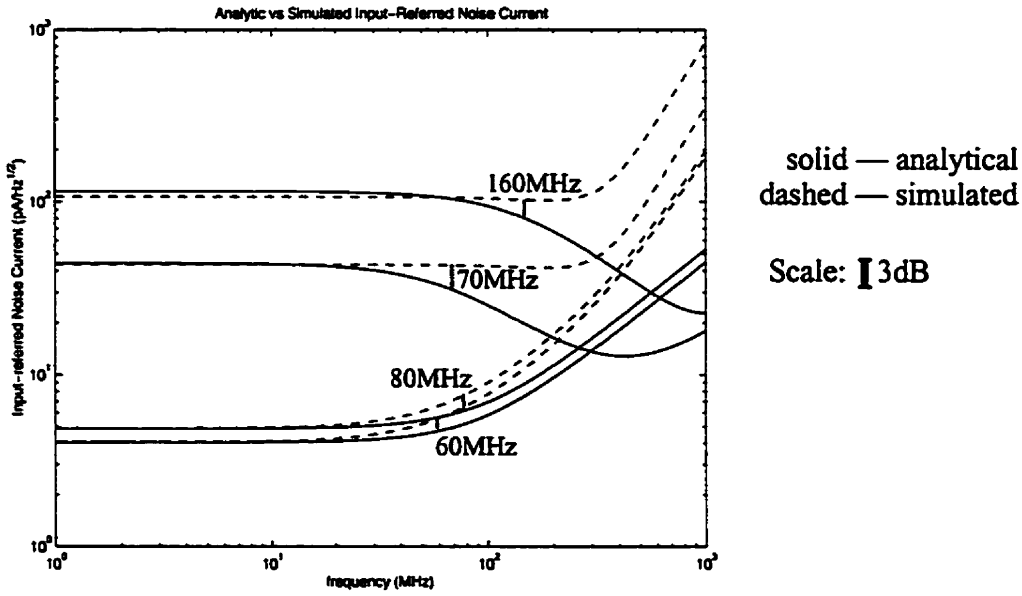


Figure 5.15 Plot of analytic vs. simulated input-referred noise of 4 designs. Vertical bars mark 3dB cut-off frequencies of preamplifiers.

5.2.3 Design Optimization

As is typical in analog circuits, the design of an optical preamplifier involves addressing conflicting goals and making trade-offs. Bandwidth, gain, and sensitivity are three important design specifications, and each is affected by circuit parameters such as the supply voltage and the input capacitance. Design trade-offs are often better understood with the aid of analytic models of the circuit. The following equations represent our analytic model of the preamplifier:

DC transimpedance gain:

$$gain = \frac{1/g_{m3} - R_f}{1 + 1/K_{cm}} \tag{5.25}$$

Pole locations:

$$\omega_{p1} = \frac{(g_{m1} + g_{s1})(1 + 1/K_{cm})}{C_{in} + (g_{m1} + g_{s1})(C_L + C_f)R_f/K_{cm}} \tag{5.26}$$

$$\omega_o{}^2 = \frac{g_{m3}}{R_f C_i} \times \frac{C_{in} + R_f(g_{m1} + g_{s1})(C_L + C_f)/K_{cm}}{C_A C_L + C_f(C_A + C_L)} \tag{5.27}$$

Input-referred noise current spectrum:

$$\begin{aligned} I_{ni}^2(s) = {} & I_{n2}^2 + \left|1 + s\frac{C_{in}}{g_{m1} + g_{s1}}\right|^2 \times I_{n2b}^2 \\ & + \left|\left(\frac{1/g_{m2} + R_f}{1/g_{m2} - K_{cm}R_f}\right) \times \frac{1}{1 + sR_{out}C_L}\right|^2 \times (I_{n3}{}^2 + I_{n3b}{}^2) \\ & + \left|1 + s\frac{C_{in}}{g_{m1} + g_{s1}} - \left(\frac{1/g_{m2} + R_f}{1/g_{m2} - K_{cm}R_f}\right) \times \frac{1}{1 + sR_{out}C_L}\right|^2 \end{aligned} \tag{5.28}$$

Input-referred noise level at dc:

$$\begin{aligned} I_{ni}^2(0) = {} & I_{n2}^2 + I_{n2b}^2 + \left(\frac{1/g_{m2} + R_f}{1/g_{m2} - K_{cm}R_f}\right)^2 \times (I_{n3}{}^2 + I_{n3b}{}^2) \\ & + \left|1 - \frac{1/g_{m2} + R_f}{1/g_{m2} - K_{cm}R_f}\right|^2 \times I_{nRf}^2 \end{aligned} \tag{5.29}$$

There are many insights that can be derived from studying this set of design equations. First, we see that the body effect of transistor M_1 has a positive effect on both the bandwidth and noise performance of the preamplifier by increasing the

effective transconductance of the transistor. Second, we can identify a region in the design space where the higher poles are in close enough proximity to the dominant-pole to have an effect on the overall preamplifier bandwidth. Figure 5.16 shows a plot of the simulated bandwidth from SPICE as well as the pole locations derived from the analytic expressions. The SPICE results merely indicate a path of slightly enhanced bandwidth that is marked by the arrow; the analytic results, however, provide us with the underlying reason for the observation. Third, although SPICE cannot predict the effect of power dissipation on bandwidth, Equation (5.26) points out that the power dissipation — as represented by the sum of transconductances g_{m2} and g_{m3} — is secondary to the *ratio* of g_{m2} and g_{m3}, represented by the current mirror gain K_{cm}, in determining the dominant pole frequency. Furthermore, we can infer from Equation (5.26) that the sensitivity of the bandwidth to K_{cm} is greatly affected by the capacitive load present at the input and output of the preamplifier. Fourth, in fiber-optic applications where the input capacitance is much smaller, and in cases where K_{cm} is greater than two (6 dB) or so, Equation (5.26) can be simplified to

$$\omega_{p1} \approx \frac{K_{cm}}{(C_L + C_f)R_f}.$$

We see in this situation that significant speed can be gained through increasing K_{cm}. This is illustrated in Figure 5.17 in which the input capacitance has been reduced from 2pF down to 100fF.[1] We see that surface contour has changed significantly from Figure 5.16. While this result can be inferred from studying Equation (5.22), there is no way to predict such changes from the original SPICE simulations.

The observations described above are but a few of the design insights that can be gleaned from the design equations, but not from numeric simulation results. The contribution of DPI/SFG analysis to this process is in giving the designer the ability to break down the dynamic feedback mechanisms of any circuit in order to make small, isolated decisions and simplifications which, taken as a whole, produce simplified analytic expressions that capture the essence of the circuit.

1. Note that the bandwidth improvement is not as dramatic due to the effect which K_{cm} has on C_L.

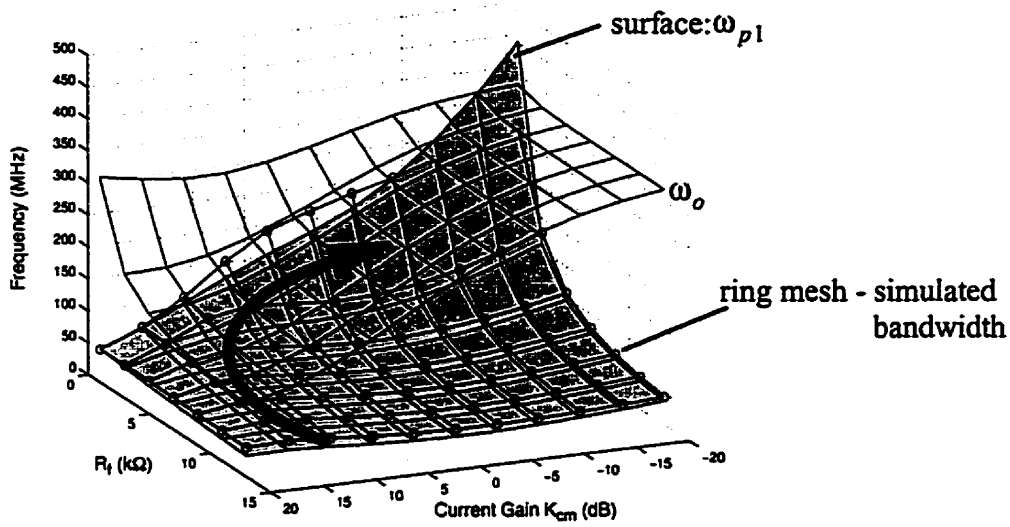


Figure 5.16 Plot of pole frequencies and simulated bandwidth vs. feedback resistance and current mirror gain.

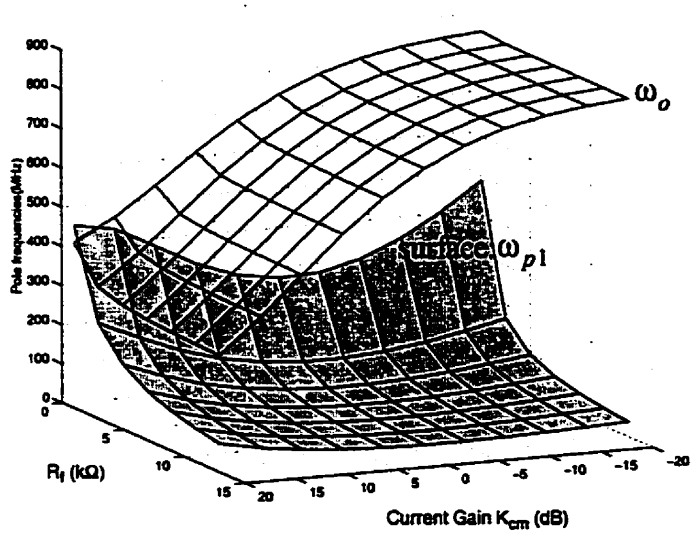


Figure 5.17 Plot of pole frequencies vs. feedback resistance and current mirror gain.

Optimizing Bandwidth and Gain

As with our variable-gain transimpedance amplifier, our target data rate is 100Mb/s with a preamplifier bandwidth of about 70MHz. For this low-voltage design, however, the supply voltage has been reduced to 1V, and the photodiode capacitance has been reduced to 1pF. Figure 5.18 plots ω_{p1} and ω_o over the design space, and Figure 5.19 shows two projection views along the R_f and K_{cm} axes. Recall from Figure 5.9 that the dominant pole, ω_{p1}, reliably predicts the bandwidth of the preamplifier. The sub-region bounded by the dashed line in Figures 5.18 and 5.19 represents that part of the design space capable of satisfying our bandwidth requirement.

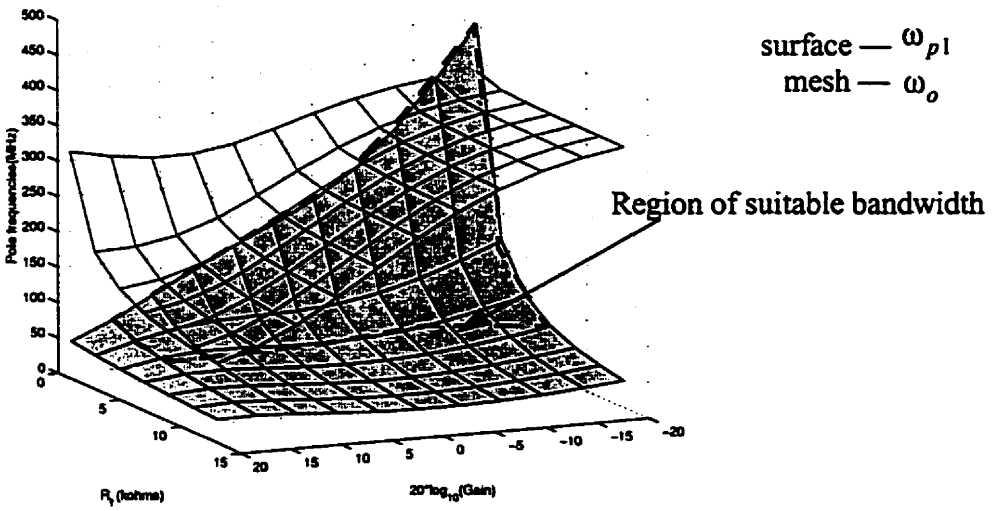


Figure 5.18 Plotting the preamplifier's pole frequencies vs. feedback resistance and current mirror gain.

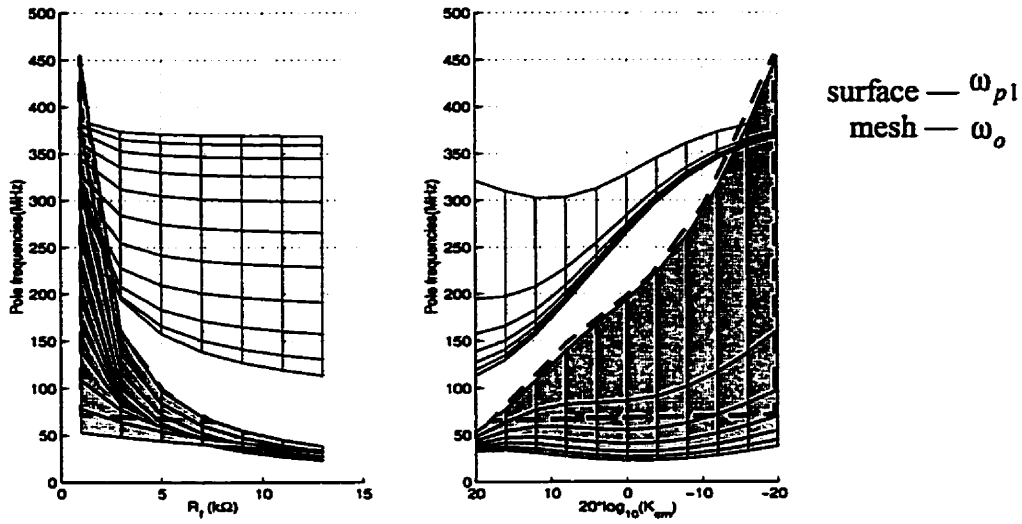


Figure 5.19 Two projections of the surface plot in Figure 5.18.

Since the process of optimizing the frequency response involves maximizing the gain for a desired bandwidth, the gain-bandwidth (GBW) product is a useful figure of merit because it combines gain and bandwidth into a single quantity. Although bandwidth and gain can be traded off with feedback, the product of the two is often fixed for a given topology, bias condition, etc. We can optimize our preamplifier design through maximizing the GBW. By approximating the bandwidth with ω_{p1}, we can obtain an analytic expression for the GBW from Equations (5.25) and (5.26):

$$GBW = \frac{(g_{m1} + g_{s1})(1 - g_{m3}R_f)}{C_{in} + (g_{m1} + g_{s1})(C_L + C_f)R_f/K_{cm}} \tag{5.30}$$

Figure 5.20 shows the resulting 3-dimensional plot of GBW versus R_f and K_{cm} while Figure 5.21 presents the same surface in two, 2-dimensional projections views. Across the design space, we see that the GBW can vary by over an order of magnitude. We can identify that portion of the design space which meets our bandwidth requirement by projecting the bounded region identified in Figure 5.18 onto the GBW plot. Within this region, we have marked in grey a sub-region that corresponds to an area with the highest GBW.

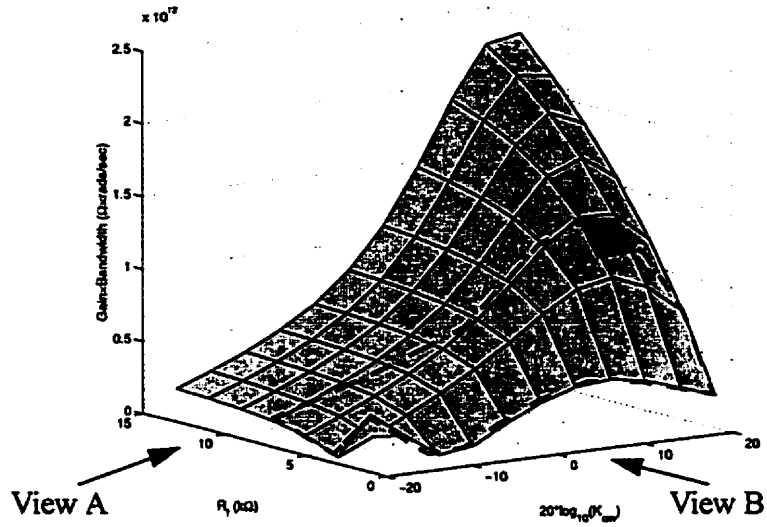


Figure 5.20 Plot of transimpedance gain-bandwidth product vs. feedback resistance and current mirror gain.

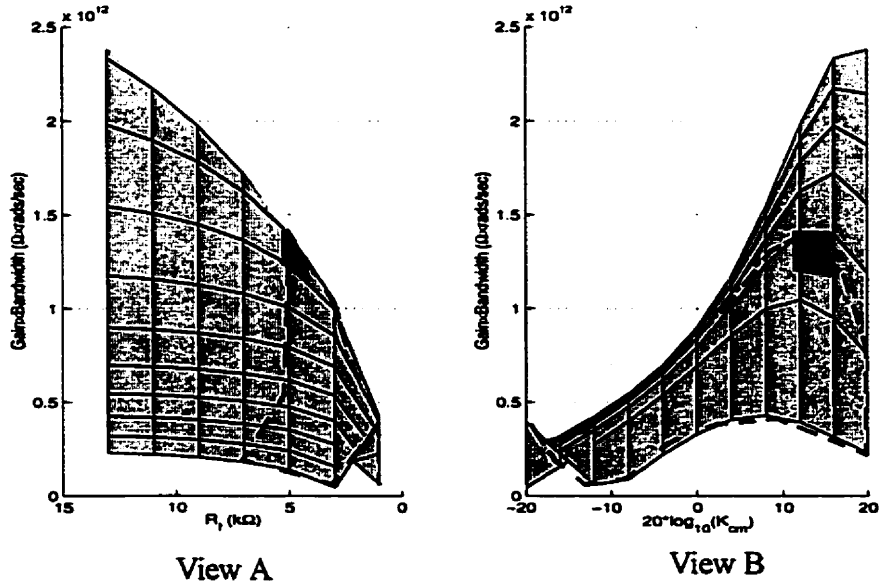


Figure 5.21 Two projections of the GBW plot in Figure 5.20.

Optimizing Sensitivity

Thus far, we have identified a region of the design space that provides maximum gain for a given bandwidth. We must now consider sensitivity. Using the expression for the input-referred dc noise current in Equation (5.29), we can plot the noise performance across the design space as shown in Figures 5.22 and 5.23. The vertical axis is in dB relative to $1 pA/\sqrt{Hz}$. We see here that within the optimized region projected from Figure 5.20 and marked in grey, the noise level within this region is about 16dB or $6 pA/\sqrt{Hz}$. The lowest noise performance is achieved by maximizing both R_f and K_{cm}. Hence, the optimum design choice is

$$R_f = 5k\Omega, K_{cm} = 16\text{dB}.$$

Notice, however, that the noise performance is rather insensitive around the optimum point, varying by only about 2dB in the grey region. This affords the designer greater flexibility to deviate from the optimum point without too much concern from a sensitivity standpoint.

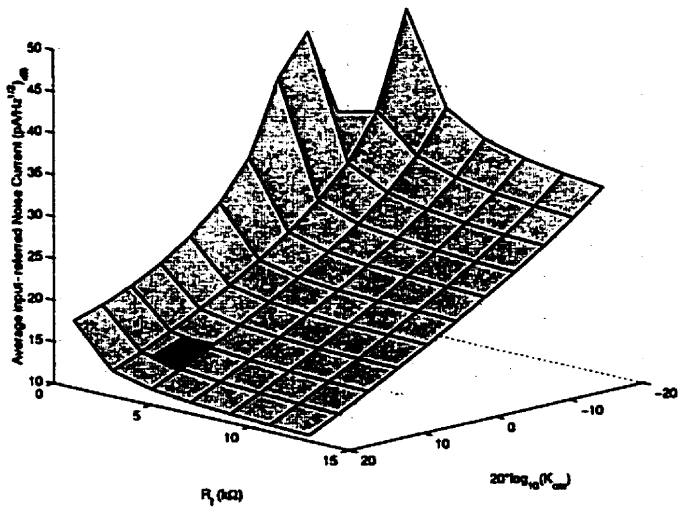


Figure 5.22 The dc input-referred noise current vs. R_f and K_{cm} in dB.

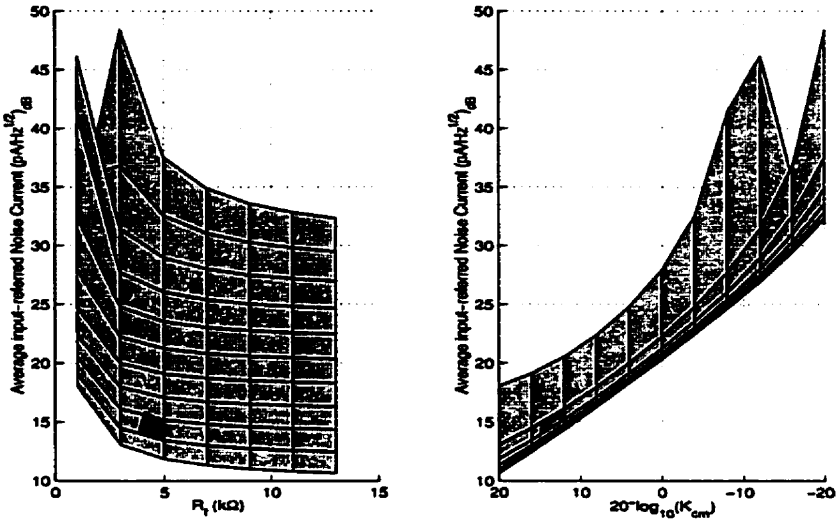


Figure 5.23 The dc input-referred noise current vs. R_f and K_{cm} in dB.

Final Design

We have completed our characterization of the preamplifier's bandwidth and sensitivity and are ready to finalize the design. To summarize, we have found the optimum feedback resistance to be in the range of $4-5k\Omega$ and the optimum current mirror gain to be in the range of $12-16\text{dB}$. A current-mirror gain of 12dB is desirable from a practical standpoint because the resulting 4:1 ratio between the sizes of transistors M_3 and M_2 allows for a common-centroid layout of the transistors which helps minimize offsets caused by device mismatch.

To determine the sizing of the transistors, we first considered our 1V system supply constraint. In order to operate down to 1V, we biased all transistors on the lower boundary of deep inversion with a saturation voltage of about 200mV. We verified our earlier observation that consuming greater power dissipation does not improve performance and so determined the bias currents based on the requirements of the photodiode. Given a nominal and maximum photocurrent signal of $1\ \mu A$ and $40\mu A$ respectively, we set the bias current at the input stage of the preamplifier to $64\mu A$, large enough to ensure that the photodiode reverse bias voltage does not change significantly over the signal range.

The optimized optical preamplifier circuit is shown in Figure 5.24. Resistor R_f is implemented using a MOSFET biased in the linear region. The cascode device M_4 was added to eliminate the systematic offset voltage generated by unequal drain-source voltages between M_2 and M_3. The additional device reduces the maximum output swing by about 200mV, but otherwise does not significantly affect the circuit performance.

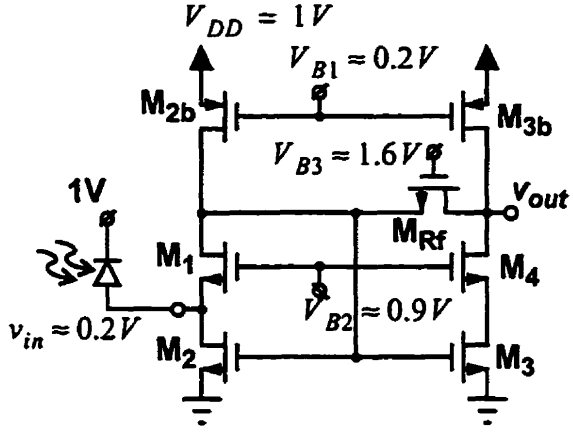


Figure 5.24 Optimized 1V optical preamplifier.

SPICE simulations of the optimized design resulted in a transimpedance gain of $3.5k\Omega$, an input-referred noise density of $6pA/\sqrt{Hz}$, and a bandwidth of 88MHz. Pole-zero analysis in SPICE gave a dominant-pole at 59MHz and the higher-order poles at 170MHz with $Q = 1.7$, confirming our analytic results of $\omega_{p1} = 59MHz$ and $\omega_o = 180MHz$. Although one could be tempted to increase R_f given the seemingly ample 88MHz bandwidth, the fact that the dominant-pole is only at 60MHz realistically limits us to a maximum of $5k\Omega$.

With our analytic expression of the noise current in Equation (5.28), we can plot the relative noise contributions of each of the devices in the optimized design as shown in Figure 5.25. Although transistors M_2 and M_{2b} have the largest contribution, we see that all the devices in the preamplifier except for M_1 are significant from a noise standpoint. This is commonly found in optimized designs which tend to equalize the noise contributions of different components in order to produce the lowest overall result.

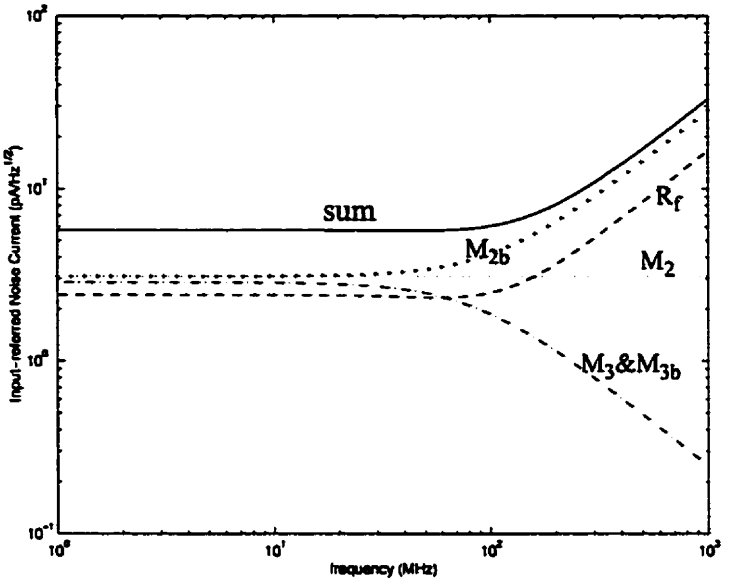


Figure 5.25 Plot of input-referred noise density of optimized preamplifier design and all the individual contributions from its internal devices.

As described in Chapter 3, the low-voltage preamplifier provides robust stability and a regulated bandwidth, making the circuit particularly suited for variable-gain designs. These properties are illustrated in Figure 5.26, where R_f is varied from $1\,k\Omega$ to $7\,k\Omega$. All four frequency responses are well-controlled and display no peaking. Although the transimpedance gain varies by 20 dB, the bandwidth only varies by a factor of two (i.e., from 65MHz to 126MHz). Figure 5.27 shows the corresponding pulse response of the optimized design for a 100Mb/s pulse stream.

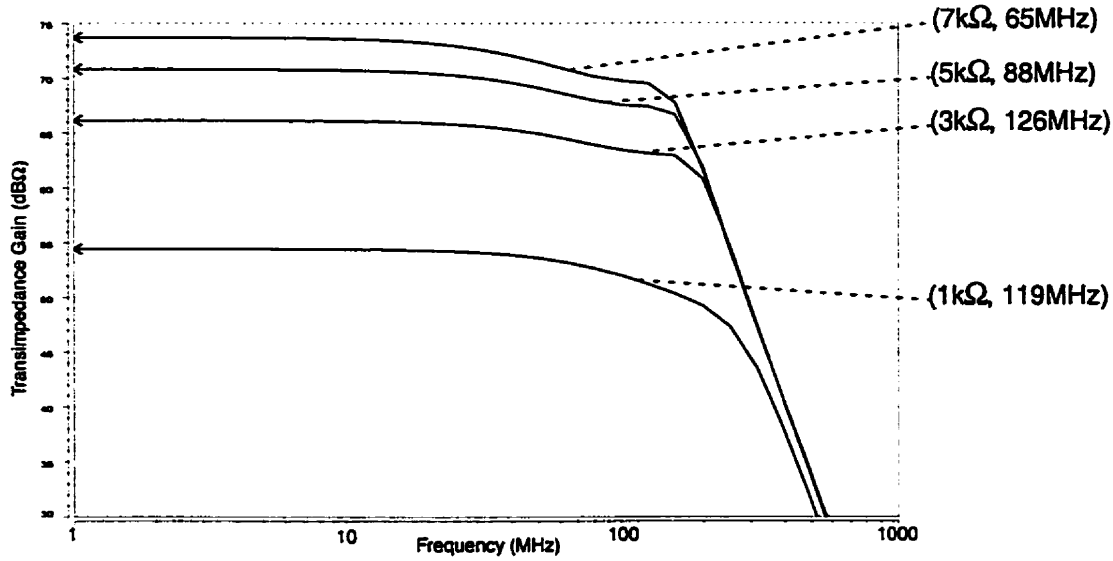


Figure 5.26 Simulated frequency response of low-voltage optical preamplifier for different feedback resistor values.

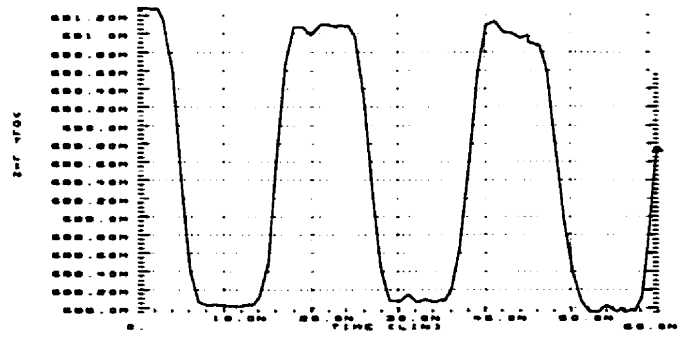


Figure 5.27 Simulated pulse response of optimized design.

5.3 SUMMARY

In this chapter, we optimized the design of a low-voltage transimpedance amplifier to provide maximum gain and sensitivity for a given bandwidth. In the process, we illustrated the use of DPI/SFG analysis for the synthesis and modelling of circuits. By developing a simplified set of design equations for the preamplifier, we gained insight into the operation of the circuit and its associated design trade-offs.

Admittedly, the presentation *of the development* of an optimized design can seem contrived. Many assumptions and approximations were involved in the development, but the presentation here included only those intuitive guesses that ultimately proved correct. In reality, the design process is a complex series of iterative approximations, derivations, and simulations. Designing using DPI/SFG analysis is no different. However, the DPI/SFG method does provide a framework for exploration, giving the designer the ability to break down the often complex interactions of signals within a circuit, and to make small, isolated decisions and simplifications which, taken as a whole, produce a better understanding of the design. Incorrect approximations will be made, but with DPI/SFG analysis, a designer can systematically backtrack and evolve his or her decisions until the appropriate trade-offs between model accuracy and simplicity have been achieved.

REFERENCES

A. A. Abidi, "High-Frequency Noise Measurements on FETs with Small Dimensions," *IEEE Trans. Electron Devices*, vol. 33, pp. 1801-1805, November 1986.

A. Buchwald and K. Martin, *Integrated Fiber-Optic Receivers*, Boston: Kluwer Academic Pub., pp. 368-370, 1995.

A. Ochoa, 1999. "Translating Noise Signals in Linear Circuits," *Proc. of IEEE Mid-West Symp. Circ. and Syst.*, Las Cruces, NM, pp. 51-55, August 1999.

CHAPTER

6 Implementation and Experimental Results

This chapter discusses the implementation details and presents the experimental results of two integrated circuits (IC) that were implemented to demonstrate the feasibility of the proposed optical preamplifier designs. We first present a 1V optical receiver front-end with on-chip dynamic gate biasing, followed by a wide dynamic range variable-gain transimpedance amplifier with ambient light rejection. Both ICs were implemented in a commercial, double-poly, triple-metal, 0.35μm CMOS process.

6.1 A 1V OPTICAL RECEIVER FRONT-END

A simplified diagram of the optical receiver front-end is shown in Figure 6.1. The signal path consists of the proposed low-voltage transimpedance preamplifier followed by two post gain stages that reuse the optimized transimpedance design in a transconductance-transimpedance topology. Additional circuitry using a 3V supply was incorporated on-chip only to aid testing. These circuits are represented by the shaded blocks in Figure 6.1. Passive RC filtering of the charge pump's output was used to reduce ripple due to charge injection and to isolate the gain stages.

6.1.1 Receiver Building Blocks

This section discusses the following additional circuits found on the test chip:

- Variable-gain post amplifiers
- Limiting amplifier
- Digital output driver
- Constant-g_m bias circuit
- Analog multiplexor (MUX) and output buffer
- Input test transconductor

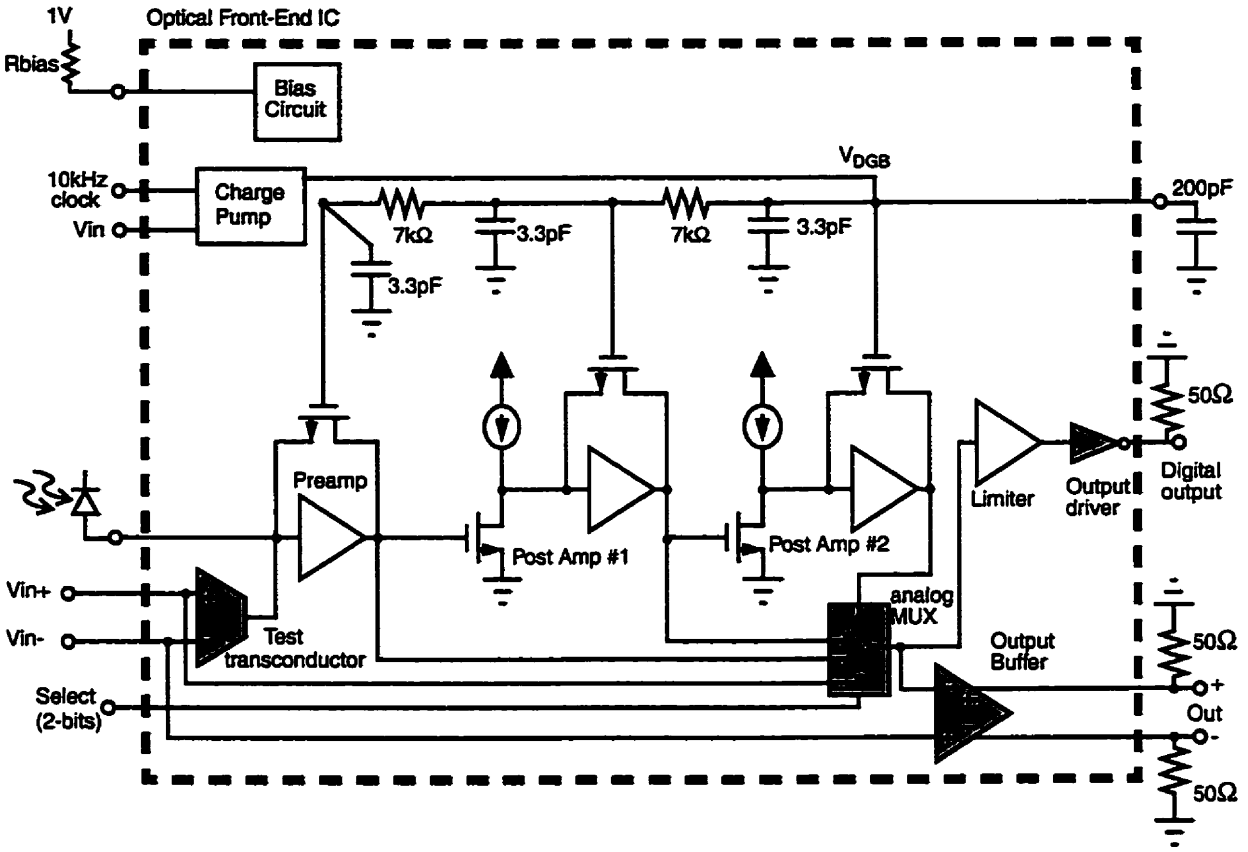


Figure 6.1 System-level block diagram of 1V optical receiver. Shaded blocks indicate the use of a 3V supply.

Variable-Gain Post Amplifiers

In the optical receiver, additional gain stages are required after the optical preamplifier to provide sufficient amplification for the final limiter stage. We can take advantage of our existing work on transimpedance amplifiers by adopting a transconductance-transimpedance topology [Cherry,1963], [Wang,1995]. A maximum gain of 40dB was achieved by cascading two stages, each with a variable gain up to 20dB. A variable gain is realized by either varying the transconductance [Gomez,1992] or the transimpedance. We chose the latter since our transimpedance design provides a variable gain with a well controlled bandwidth.

Figure 6.2 shows a schematic of a single variable-gain amplifier. The input transconductance stage is biased by the output level of the previous stage. The inter-

mediate current is then converted back to a voltage by the transimpedance stage. The transimpedance stage uses a standard current mirror without cascode devices in order to maximize signal swing. Variable gain is achieved by adjusting the central gate bias voltage generated by the voltage doubler, V_{DGB}.

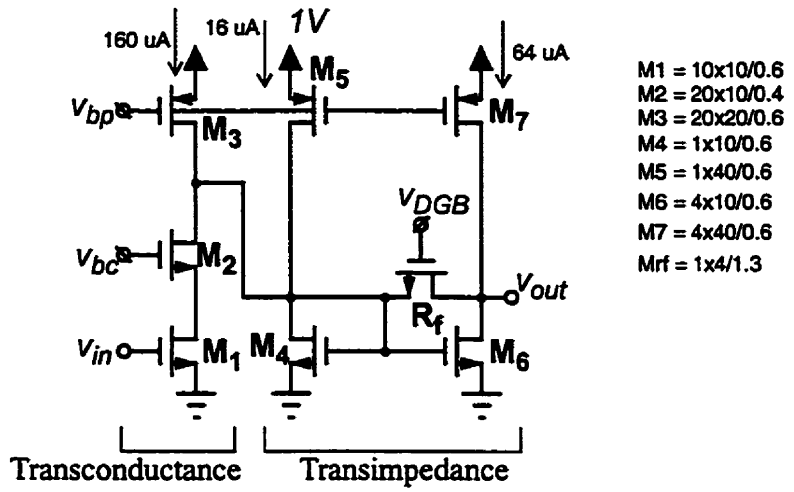


Figure 6.2 Variable-gain post amplifier stage. Transistor sizes as shown.

Limiting Amplifier and Digital Output Driver

The limiting amplifier is used to regenerate digital levels from an analog signal, and is shown in Figure 6.3. The circuit consists of a common-source input stage that is loaded by the diode-connected transistor M_3. Transistor M_3 biases the output of the common-source stage around the threshold voltage of the inverters. The inverters provide enough additional gain to regenerate the digital logic levels.

The output driver is used to drive the digital signal off-chip. It consists of a wide, open-drain NMOS device that is connected to an external 50Ω load. The nominal drive current is 4 mA which provides 200mV of output swing.

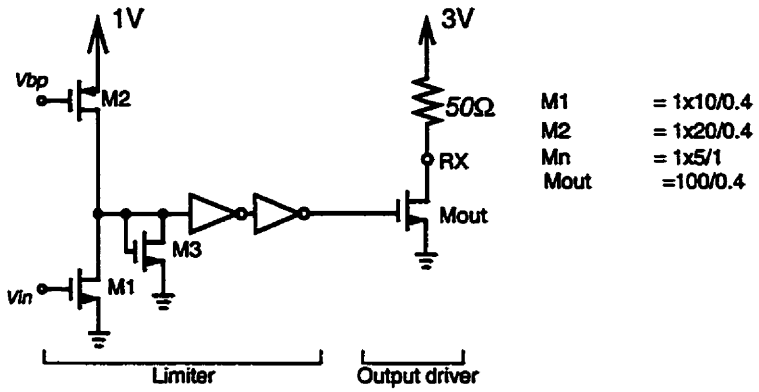


Figure 6.3 Final limiter stage. Transistor sizes as shown.

Constant-g_m Bias Circuit

The 1V bias circuit used in the receiver is shown in Figure 6.4. The circuit is commonly referred to as a constant-g_m bias circuit because it is designed to stabilized the transconductances of the transistors relative to the external resistor, R_{bias} [Steininger,1990]. The design is adopted from [Johns,1997], but the cascode devices associated with transistors M_2 and M_3 have been removed so that the drain-to-source voltages of transistors M_2 and M_3 are better matched to those of transistors M_1 and M_4 respectively. The start-up circuit shown on the right is required to prevent the circuit from remaining in an alternate stable state in which all the device currents are zero.

Analog Multiplexor and Output Buffer

The analog multiplexor (MUX) and output buffer together provide the crucial facility to observe high-speed signals along the signal path. The analog multiplexor connects four possible signals to the output buffer: a direct external input for characterizing the output buffer, the preamplifier output, the first post amplifier output, and the second post amplifier output. The multiplexor is made up of four source follower buffers that are all connected to the signal terminal of the output buffer while the other buffer input terminal is connected to an external bias voltage. The source

followers have an enable control as shown in Figure 6.5; when disabled, all bias currents are turned off, and the gate of M_1 is cut off from the input signal for improved isolation. Two external pins control a digital 4x1 decoder that is used to select the desired source follower while disabling the others.

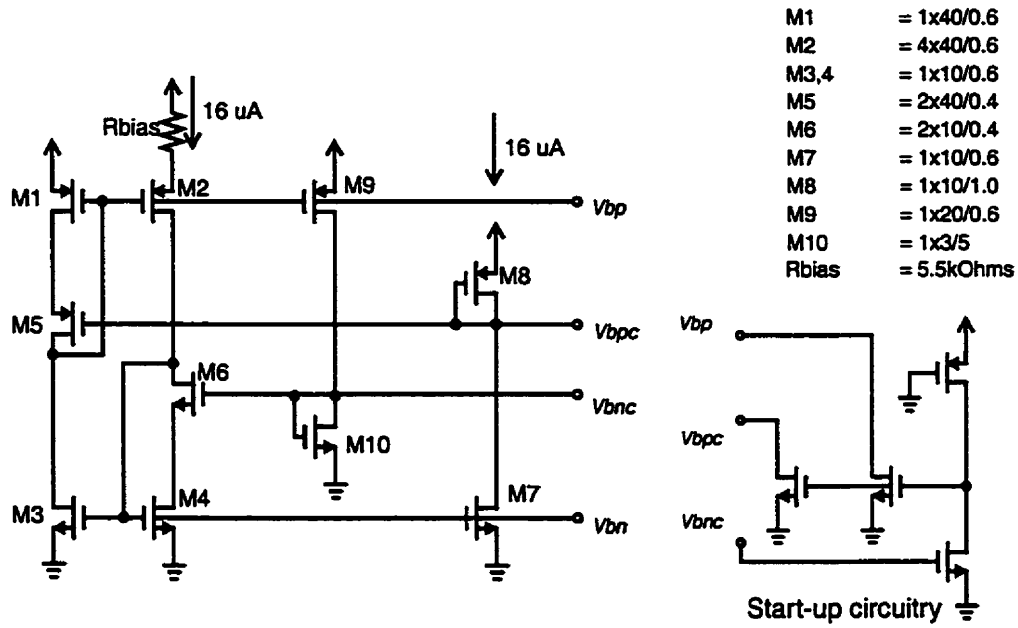


Figure 6.4 1V Constant-g_m bias circuit with start-up circuitry. Transistor sizes as shown.

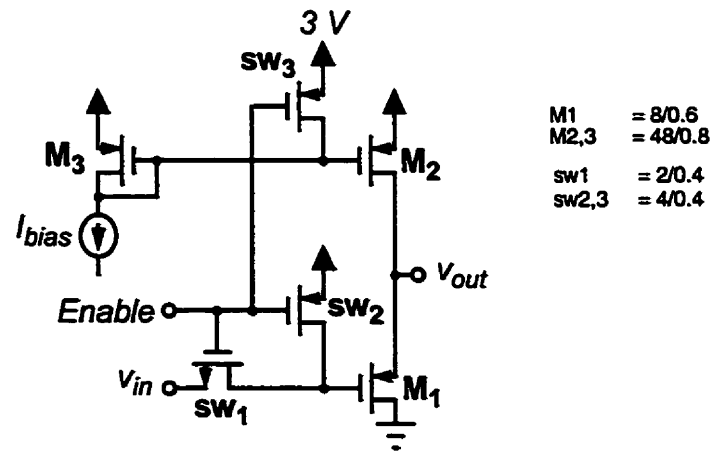


Figure 6.5 Source follower with enable control.

Figure 6.6 shows the differential output buffer that is designed to drive 50Ω loads. Transistor M_3 is very wide in order to decrease its saturation voltage so that the input common-mode range of the buffer is maximized. In contrast, transistors M_1 and M_2 are biased with a very high saturation voltage in order to maximize the bandwidth and the input linear range which is about 400mV (differential). The tail current is nominally 15 mA, and is controlled through a current mirror biased using an external resistor.

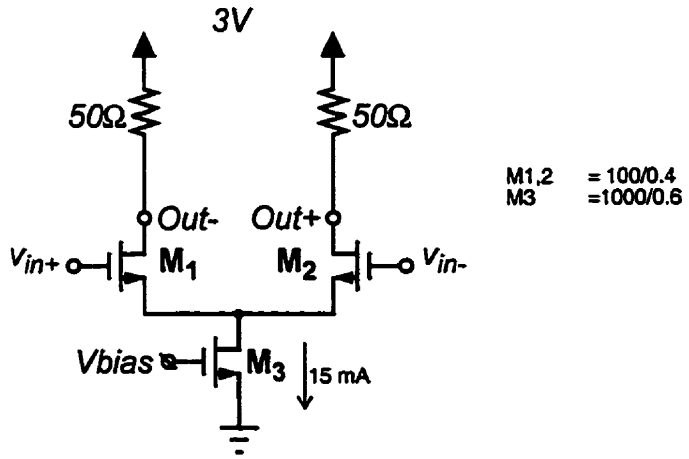


Figure 6.6 Output buffer shown with external 50Ω resistors.

Input Test Transconductor

The input test transconductor, shown in Figure 6.7, allows us to generate test currents on-chip. The transconductor has an linear input range of about 200mV (differential). The tail current is nominally 30μA, but is adjustable through an external bias resistor

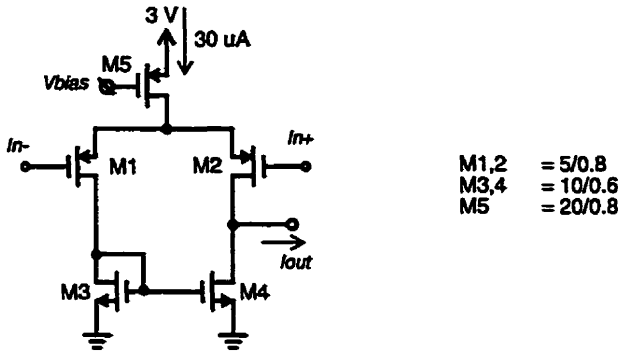


Figure 6.7 Input test transconductor circuit.

6.1.2 Experimental Results

A micrograph of the fabricated test chip is shown in Figure 6.8. The chip measures $1.0mm \times 1.6mm$ and occupies an active area of $0.13mm^2$. The main signal path runs through the centre of the chip, from left to right. The bias voltage doubler was placed in the far lower corner, away from the output buffer and output driver to minimize noise coupled through parasitics.

The power consumption of the 1V front-end circuit is 1mW. The power consumption of the 3V test circuitry is 45mW, and is essentially due to the output buffer. An external 1pF capacitor was used to model the photodiode during electrical testing, while a Mitel 1A354 PIN photodiode was used to construct the actual optical link. The typical capacitance of the photodiode is 1pF for a bias voltage of 1V or more.

Frequency Response Measurements

The measured frequency response of the output buffer with source follower is shown in Figure 6.9. The buffer has a loss of 4dB at the midband frequency of 20MHz, and its gain remains within +0.5dB and -3dB from 1MHz to 100MHz. The remaining frequency responses presented for this chip take into account the

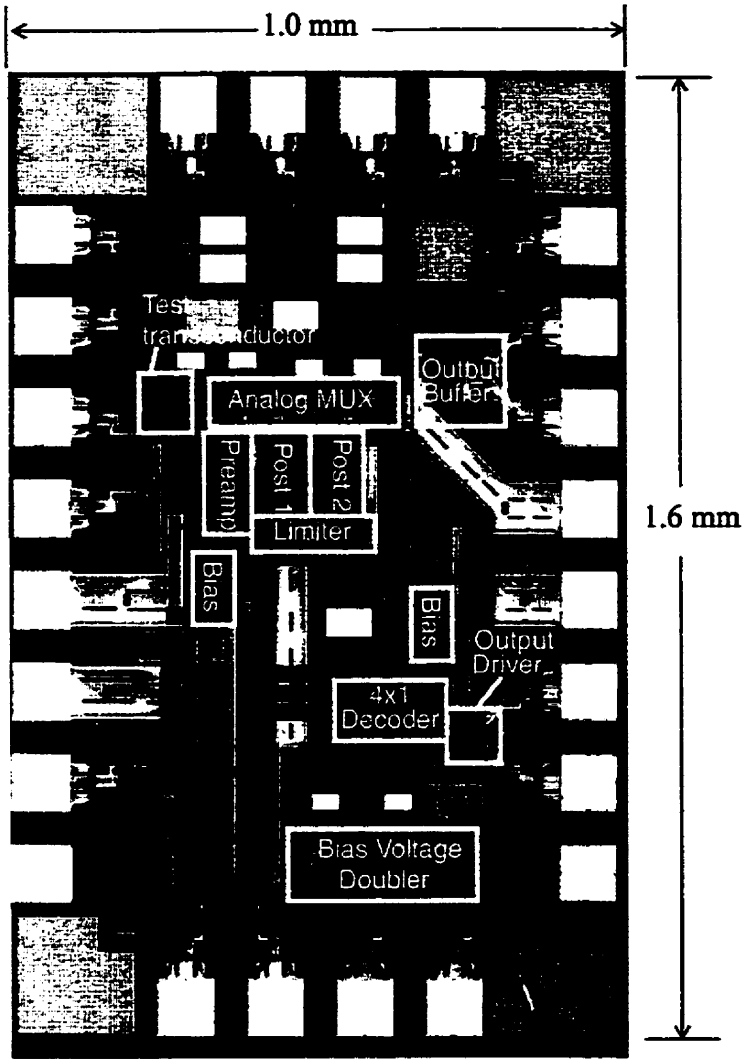


Figure 6.8 Micrograph of 1V optical receiver.

response of the buffer in order to present a true picture of the actual chip performance.

The measured frequency response along the signal path is shown in Figure 6.10. The preamplifier alone provides a nominal transimpedance gain of $2.4k\Omega$ over 45MHz, while the complete front-end provides a gain of $210k\Omega$ over 50MHz. The measured gain is consistent with our simulation results that predicted a total gain ranging from $200k\Omega$ up to $700k\Omega$ across process variations. The measured bandwidth, however, is slightly less than the 60MHz to 90MHz predicted in simulation. Unfortunately, these simulation results did not account for parasitics due to the layout or for temperature variations, and so likely overestimated the bandwidth.

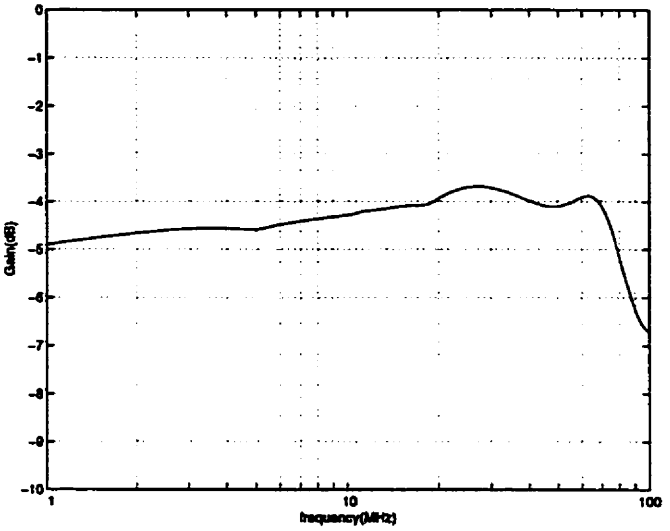


Figure 6.9 Measured frequency response of source follower (in analog MUX) and output buffer.

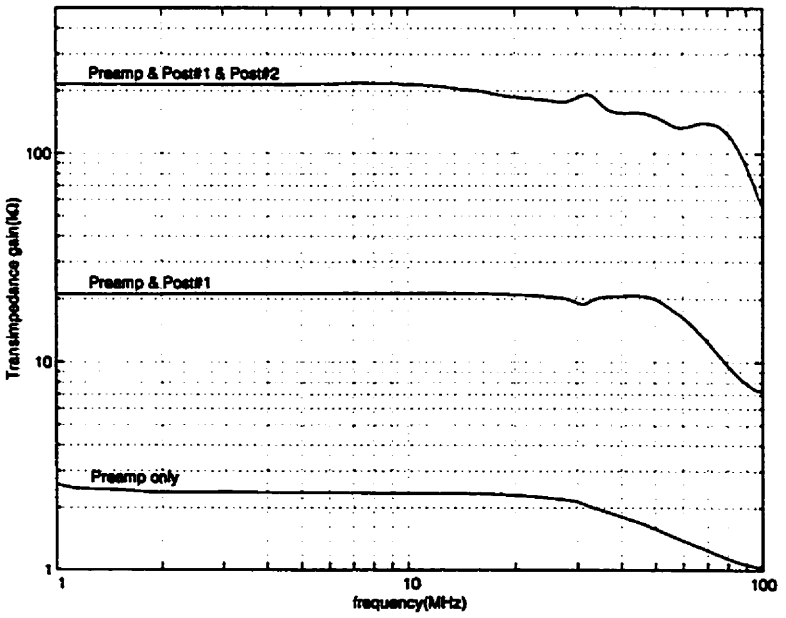


Figure 6.10 Measured frequency response along signal path.

The gain of the three transimpedance amplifiers can be controlled by varying the shared gate bias voltage, V_{DGB}. This is illustrated in Figure 6.11 which shows the frequency response for the combined preamplifier and first post gain stage for three different bias voltages. We see that the bandwidth remains well-controlled as the gain is varied. From the nominal bias voltage of 1.68V up to 2V, the gain of each

transimpedance stage can be varied by 7dB. As a result, the gain of the complete front-end can be varied by 21dB, from $210k\Omega$ down to $19k\Omega$.

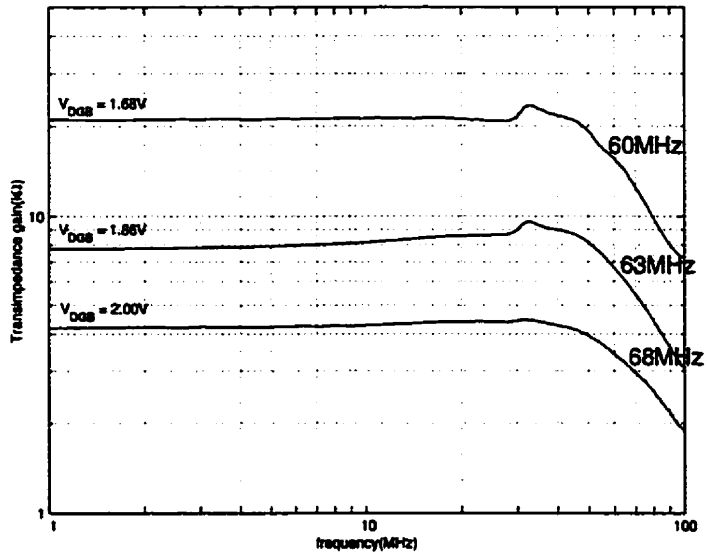


Figure 6.11 Transimpedance gain and bandwidths measured at the output of the first post amplifier for three different bias voltages.

Noise Measurements

The extracted input-referred noise current spectrum is shown in Figure 6.12. This plot was obtained in two steps. First, the combined frequency response of the preamplifier and first post amplifier was measured by driving the circuit with the spectrum analyzer's signal source through the test transconductor (measured gain = 80μA/V) to generate an electric current. Next, the signal source was turned off to obtain the output noise spectrum which is shown in Figure 6.13. The resolution bandwidth was set to 17kHz. Finally, the measured output noise spectrum was referred back to the input using the measured gain response from the first step.

The noise measurement in Figure 6.13 includes the frequency response of output buffer (see Figure 6.9) and the 3.7 dB loss due to the 180-degree phase splitter for combining differential output signals. The noise floor of the spectrum analyzer

at this resolution was observed to be 7.5μVrms, thus limiting our ability to accurately measure the output noise spectrum to 80 MHz as shown in Figure 6.13. This is not a major issue, however, since 80 MHz is still sufficiently beyond the 50MHz bandwidth of the prototype circuit.

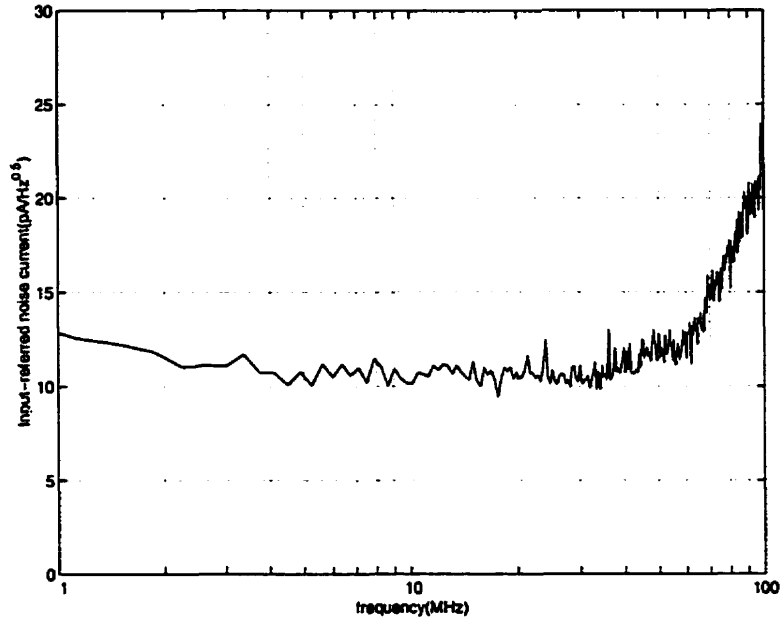


Figure 6.12 Extracted input-referred noise current spectrum.

Figure 6.12 indicates that the optical front-end has a noise density of $11\,pA/\sqrt{Hz}$ that is flat across the 50 MHz passband. This measured noise level is almost twice the $6\,pA/\sqrt{Hz}$ predicted by simulation. Similar discrepancies have been reported with other CMOS transimpedance amplifier designs [Razavi,2000], [Mohan,1999]. In both cases, the researchers suggest that the commonly used excess noise factor of 2/3 for MOSFETs is inaccurate to model the true noise behaviour of today's submicron devices, and have instead suggested excess noise factors as high as 2 [Mohan,1999]. A noise factor of 2 would increase the simulated noise level of our front-end to about $10\,pA/\sqrt{Hz}$ which would be consistent with our measured result.

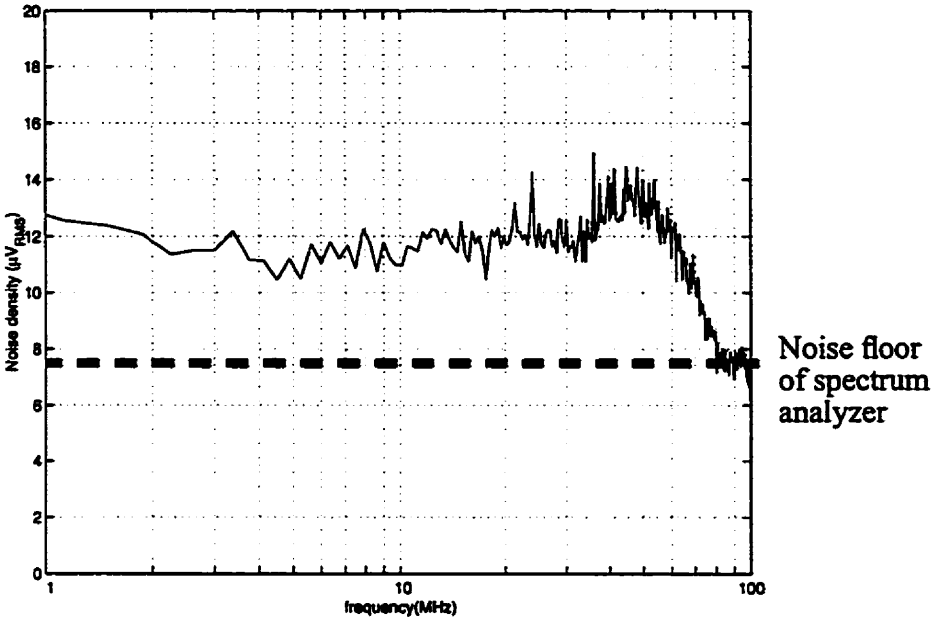


Figure 6.13 Measured voltage noise spectrum at output of first post amplifier with a 17kHz resolution bandwidth.

Experimental Optical Link

A free-space optical link was constructed using a Mitel 1A301 infrared LED, and a Mitel 1A354 Si-PIN photodiode. The link distance was approximately 2 cm and was largely limited by the short focal length (i.e., 1.5 mm) of the LED lens. The data pattern generator and LED driver were part of the second test chip that will be described in the next section. Because of the lower than expected bandwidth, we tested the circuit at a reduced the data rate of 75Mb/s instead of the original target rate of 100Mb/s. Figure 6.14 shows the eye diagram for a strong received signal with a peak current greater than 3μA. The differential signals of the output buffer were combined using a 180-degree phase splitter. The eye has a clean shape and is wide-open. The strength of the signal implies that soft-limiting and possibly slewing is occurring in the second post gain stage as well as at the output buffer. To better characterize the circuit's linear performance, we reduced the received signal to a peak current of about 1μA. The resulting eye diagram is shown in Figure 6.15 which was obtained by combining the differential buffer signals directly at the oscilloscope. Compared to Figure 6.14, the noise is proportionally larger due to the weaker input signal, but the eye remains open.

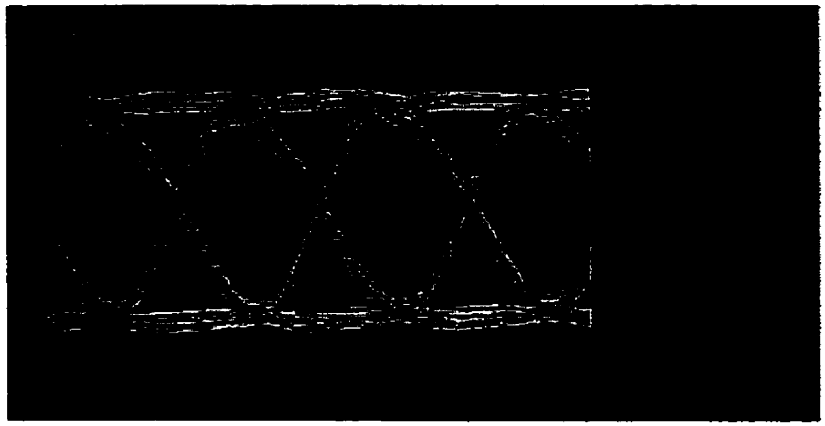


Figure 6.14 Eye diagram of free-space optical link at 75 Mb/s with an input signal greater than 3μA.

The on-chip analog multiplexor also allowed us to observe the eye diagrams at both the output of the first gain stage and the output of the preamplifier. Figure 6.16a shows the eye diagram of the preamplifier for a 3μA input signal. Although the eye is open, the eye diagram reveals a significant signal at high-frequencies. The bandwidth of the oscilloscope was 250MHz. To better gauge the actual eye diagram within the signal band, the output signals were filtered to 100MHz; the result is shown in Figure 6.16b. The eye diagram is clear as expected.

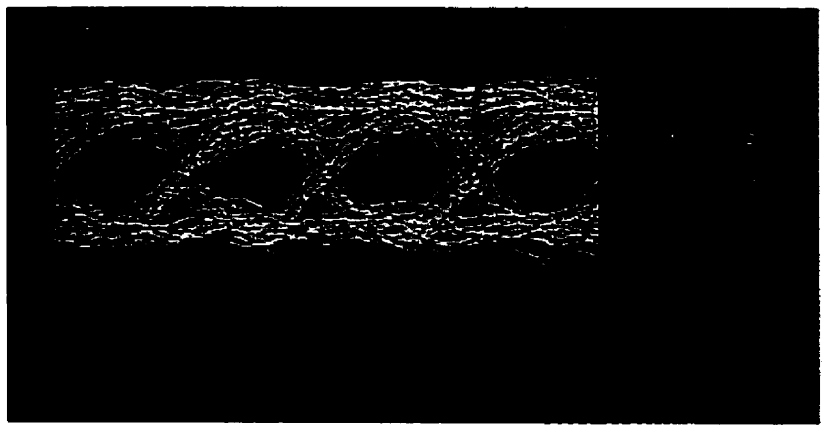
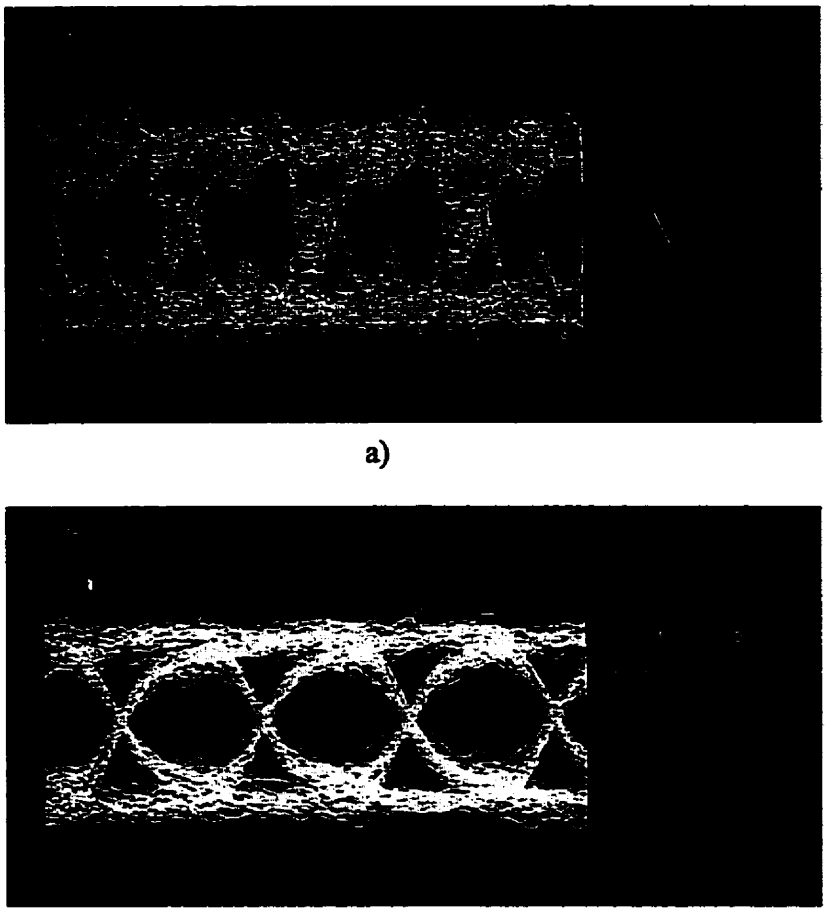


Figure 6.15 Eye diagram from free-space optical link at 75 Mb/s with input signal of about 1μA.



a)

b)

Figure 6.16 Eye diagram from preamplifier stage at 75 Mb/s with 3μA input signal: a) 250MHz bandwidth, b) 100MHz bandwidth.

Numerous measures were required to determine the cause of the high-frequency signal observed at the preamplifier. We first eliminated any external sources of electromagnetic interference by moving our testing into an EMC chamber. Doing so effectively removed some spectral peaks around 100MHz that were caused by FM radio transmissions. These peaks were present in some of our earlier measurements that are not included here. We then remeasured the noise spectrum and frequency responses of the signal path, this time from 1MHz up to 500MHz. The output noise spectrum did not show any peaks at high frequencies, thereby eliminating the possibility that the circuit was oscillating. The frequency responses at the three stages are shown in Figure 6.17. The figure clearly indicates a resonant peak near 200MHz. We resimulated the circuit using the extracted layout including parasitics, and found

a similar, albeit much smaller peak at 150MHz. This result suggests that the resonance is a result of our layout of the circuit. The extremely large gain of this circuit, together with the potential coupling of the gain stages through the common bias voltage or through the analog multiplexor, makes this design susceptible to resonance or oscillation. Although the numerous provisions incorporated in this design were sufficient to prevent oscillations, further isolation measures should be incorporated in future implementations. For instance, a separate charge pump could be used to bias each MOS resistor.

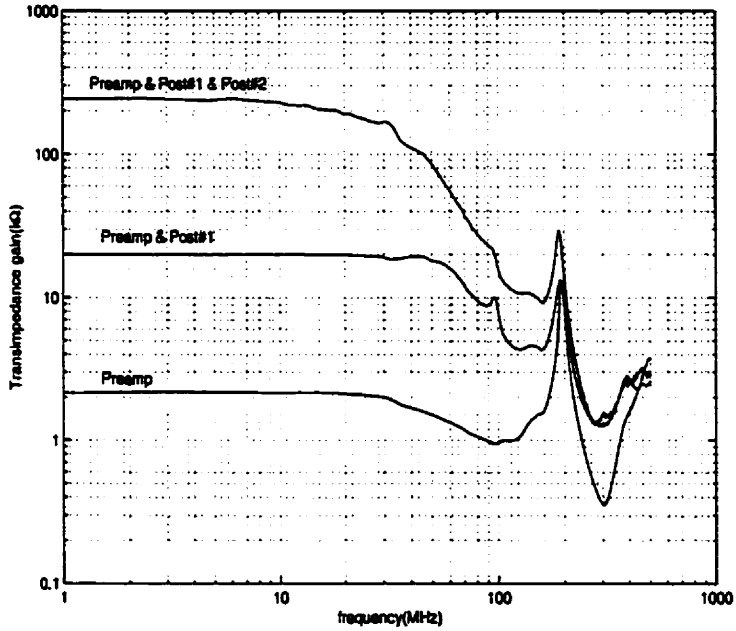


Figure 6.17 Frequency response of optical front-end characterized to 500MHz.

Experimental Results of the Voltage Doubler

The bias voltages used by the charge pump as well as the input voltage are generated on-chip using reference current sources and diode-connected NMOS transistors. To allow the external adjustment of the input voltage, the input terminal of the charge pump is directly connected to a pin on the packaged chip. Without adjustment, the input voltage was measured to be 0.862V, and the resulting output was

1.681V, just 43mV below the true doubling of the input voltage. Ideally, the output voltage should be sustained indefinitely. In reality, there is current leakage through the various pn junctions of the MOSFET switches that discharge the output capacitor over time. Relying only on the on-chip 10pF storage capacitor, the voltage doubler required a refresh period of 0.1msec or less to prevent any detectable change in bias voltage. Consequently, a 10 kHz voltage doubler clock was used for testing.

The demanding requirements placed on an optical receiver's front-end makes this test chip an excellent vehicle for evaluating the feasibility of dynamic gate biasing for low-voltage analog circuits. In addition to current leakage that causes the output voltage to droop, charge injection due to MOS switches must also be considered. Fortunately, in practice, the voltage fluctuations due to charge injection can be easily reduced by increasing the storage capacitance at the charge pump output. To illustrate this, consider Figures 6.18 and 6.19 that show the eye diagram of the optical link synchronized to the rising edge of the doubler clock. Figure 6.18 is the result obtained using only the on-chip 10 pF storage capacitor. We see there is a transient disturbance in the eye diagram at the clock edge caused by charge injection and its effect on the bias voltage. By placing an additional external 200 pF capacitor at the output of the voltage doubler, the bias voltage fluctuations are reduced to being insignificant as shown in Figure 6.19. Table 6.1 summarizes the performance results of the optical front-end.

Technology	0.35 μm CMOS (V_t:0.6 and -0.65V)
Supply voltage	1 V
Power dissipation	1 mW (1V front-end) 45mW (3V test circuitry)
Photodiode capacitance	1 pF
Transimpedance gain	210 ~ 19 kΩ
Bandwidth	50 MHz
Average input noise current	$11\,pA/\sqrt{Hz}$
Active area	$0.13\,mm^2$

Table 6.1 Performance Summary of 1V Optical Front-End.

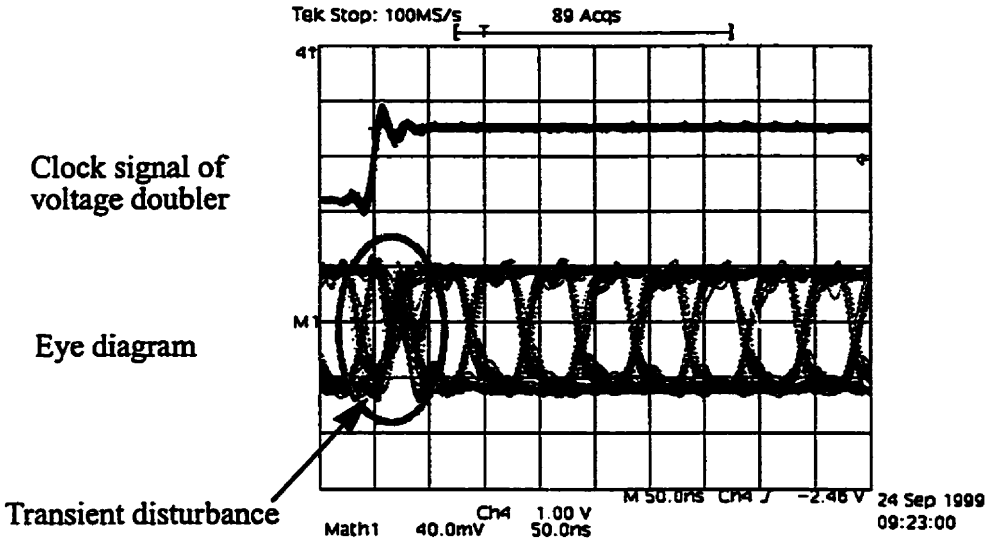


Figure 6.18 Eye diagram synchronized with rising edge of doubler clock, and no external storage capacitor at the charge pump output.

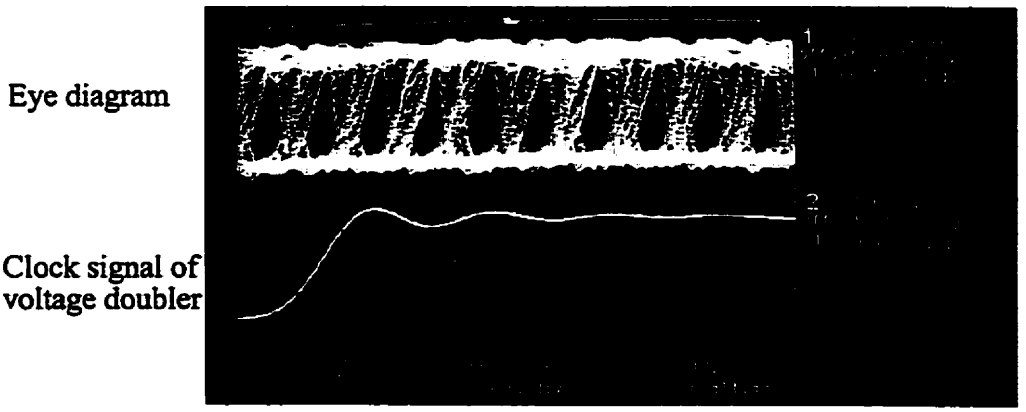


Figure 6.19 Eye diagram synchronized with rising edge of doubler clock, and a 200 pF external storage capacitor at the charge pump output.

6.2 VARIABLE-GAIN TRANSIMPEDANCE AMPLIFIER WITH AMBIENT LIGHT REJECTION

The second chip was implemented to test the proposed variable-gain transimpedance amplifier and ambient light rejection scheme. The system-level block diagram is shown in Figure 6.20. The design of the transimpedance amplifier and ambient light rejection feedback loop is detailed in Chapter 3. The four identical variable resistors used by the transimpedance amplifier are each implemented using an array of pass transistors. Three digital control pins set the resistance to one of five possible values. The chip also has a control pin for disabling the ambient light rejection feedback loop in order to test the transimpedance amplifier alone.

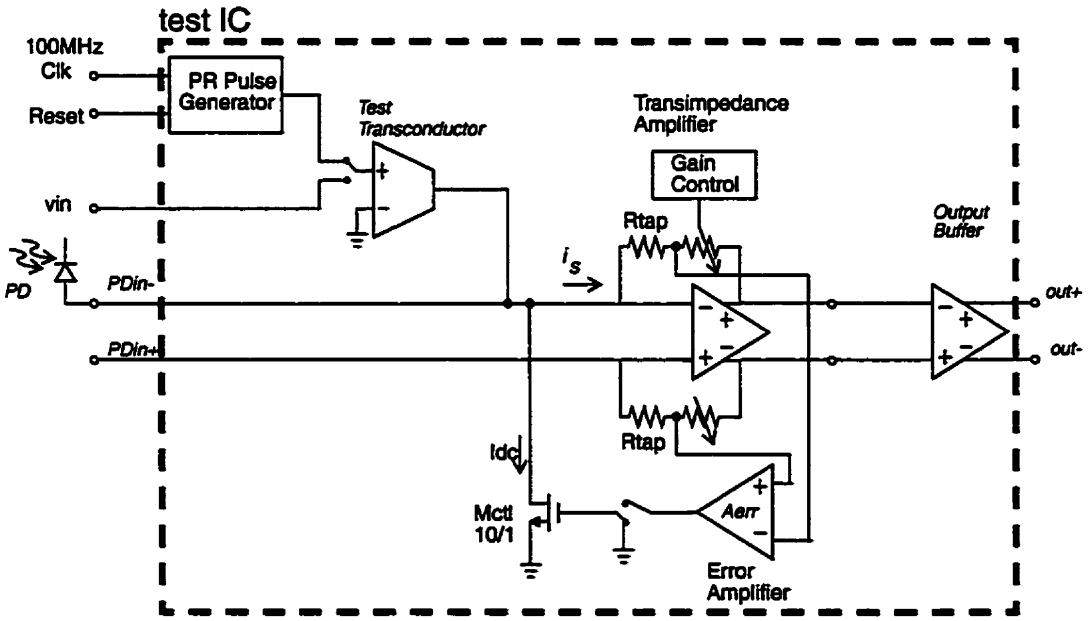


Figure 6.20 System-level block diagram of 3V optical preamplifier with ambient photocurrent rejection.

6.2.1 Implementation Details

For testing and characterization, the chip uses the same output buffer and test transconductor designs used on the first chip. A 5-bit, pseudo-random pattern generator is also included, and its schematic is shown in Figure 6.21. The pattern genera-

tor can be connected to the test transconductor in order to simulate a photocurrent signal. Alternately, the generator can be attached directly to the output buffer; when one of the outputs of the buffer is attached to an LED, the buffer functions as an LED driver with a nominal drive current of 15mA that is adjustable to 30mA. The pattern generator combined with the LED driver allows the chip to function as the optical signal source for an experimental optical link.

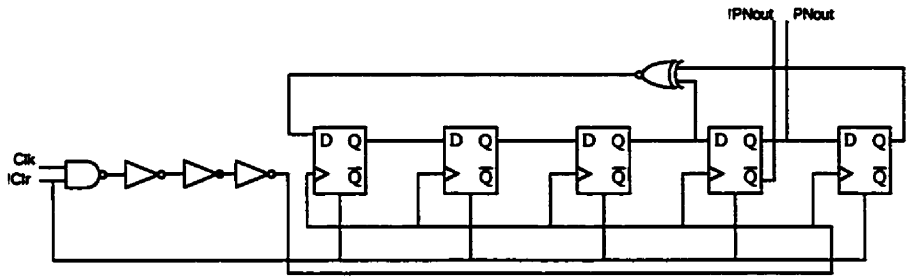


Figure 6.21 5-bit, pseudo-random pattern generator circuit.

On the test chip, the ambient photocurrent rejection circuit is designed to handle up to 30 μA of ambient photocurrent while keeping the high-pass cut-off frequency below 1MHz. The 30 μA specification corresponds to the ambient photocurrent generated by a typical 10 mm^2 Si-PIN photodiode under direct exposure to sunlight. The high-pass cut-off frequency of 1 MHz was determined to be sufficiently low for a 100 Mb/s NRZ (not return to zero) signal with some form of run length limiting to prevent the transmission of long strings of 1's or 0's. Since the design presented in Chapter 3 could not handle more than 5μA without exceeding the high-pass cut-off frequency requirement, a slight modification was made to the circuit. Instead of driving the error amplifier directly from the transimpedance amplifier's output, the error amplifier is instead driven from a middle tap off the feedback resistor as shown in Figure 6.20. Doing so effectively reduces the loop gain of the ambient photocurrent rejection circuit, thereby lowering the high-pass cut-off frequency. Simulations show that a resistance for R_{tap} of 500 Ω or less is required to keep the cut-off frequency below 1 MHz in the presence of a 30 μA average photocurrent.

A micrograph of the test chip is shown in Figure 6.22. The chip measures $1.2mm \times 1.2mm$ and occupies an active area of $0.14mm^2$. The pass transistor arrays are located beside the transimpedance amplifier (TIA), and are surrounded by a guard ring to minimize substrate noise coupling. The output buffer is also surrounded by a guard ring, but the ring's function in this case is to prevent noise generated by the buffer itself from reaching the rest of the circuit.

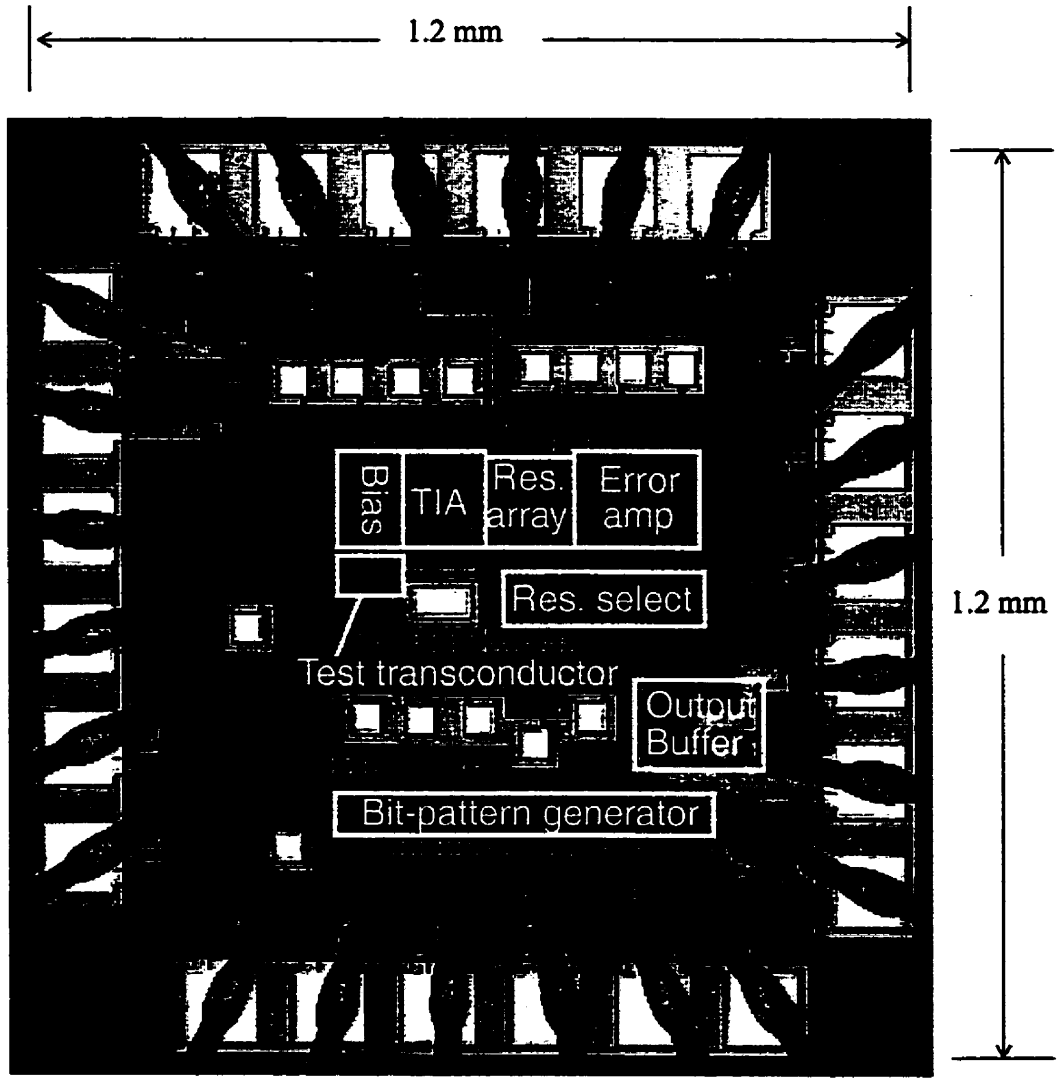


Figure 6.22 Micrograph of 3V variable-gain transimpedance amplifier with ambient photocurrent rejection.

6.2.2 Experimental Results

Figure 6.23 plots the measured frequency response of the variable-gain transimpedance amplifier together with typical simulation results. A sensitivity study using SPICE showed a ±10% bandwidth and ±25% gain deviation from nominal due to process and temperature variations. The measured results are consistent with the simulations within the passband. With a maximum gain of 19 kΩ or 85dBΩ, the preamplifier has a measured gain range of 31dB. Simulations results predict that, over the gain range, the bandwidth varies from 68 MHz up to 130 MHz while measured results show a tighter span from 85 MHz to 103 MHz. In either case, the bandwidth is still controlled to within a factor of two. At any gain setting, the transimpedance amplifier's response is well behaved, showing no significant peaking.

Compared with the 1V CMOS front-end, this transimpedance amplifier has better noise performance. The sensitivities of the available spectrum analyzers were not sufficient to obtain an output noise spectrum. Consequently, we decided to simply determine the average input-referred noise density. At the maximum gain setting of 19kΩ, the bandwidth of the preamplifier sample used for measuring the noise was 70MHz. Over this bandwidth, the chip produced an output noise of 319μV(rms) which translates to a total input-referred noise current of 56 nA(rms). This results in an average input-noise current density of $6.7 pA/\sqrt{Hz}$ which is about 30% higher than our simulated result of $5.3 pA/\sqrt{Hz}$. As with the 1V test chip, the discrepancy is likely due to a low estimate of the true excess noise factor in the modeling of the MOSFETs. If we define the preamplifier's dynamic range as the ratio of the preamplifier's noise floor of 56nA to its maximum input current handling of 400 μA, then the preamplifier has a dynamic range of 77 dB (38 dB optical).

Figure 6.24 shows the eye diagram for a 100 Mb/s optical link constructed from two test chips (one for transmit and the other for receive), a Mitel 1A301 infrared LED, and a Mitel 1A354 Si-PIN photodiode.[1] The input signal was approximately 15μA. The link distance was approximately 2 cm, and was largely limited by the

1. The 1A354 has a typical capacitance of only 1 pF so additional capacitance was added to increase the input capacitance to 5 pF. The original photodiode that we had designed for has a lower bandwidth than the data sheet would indicate.

short focal length (i.e., 1.5 mm) of the LED lens. Table 6.2 summarizes the performance of the transimpedance amplifier.

Technology	0.35 μm digital CMOS
Supply voltage	3 V
Bandwidth	70 MHz ±20 %
Transimpedance	19kΩ–500Ω
Input noise current density	6.7 $pA/\sqrt{Hz}$
Input capacitance	5 pF
Maximum signal current	400 μA
Preamplifier active area	0.04 mm^2
Power dissipation	8 mW (preamplifier) 43 mW (output buffer)

Table 6.2 Performance summary of the transimpedance amplifier.

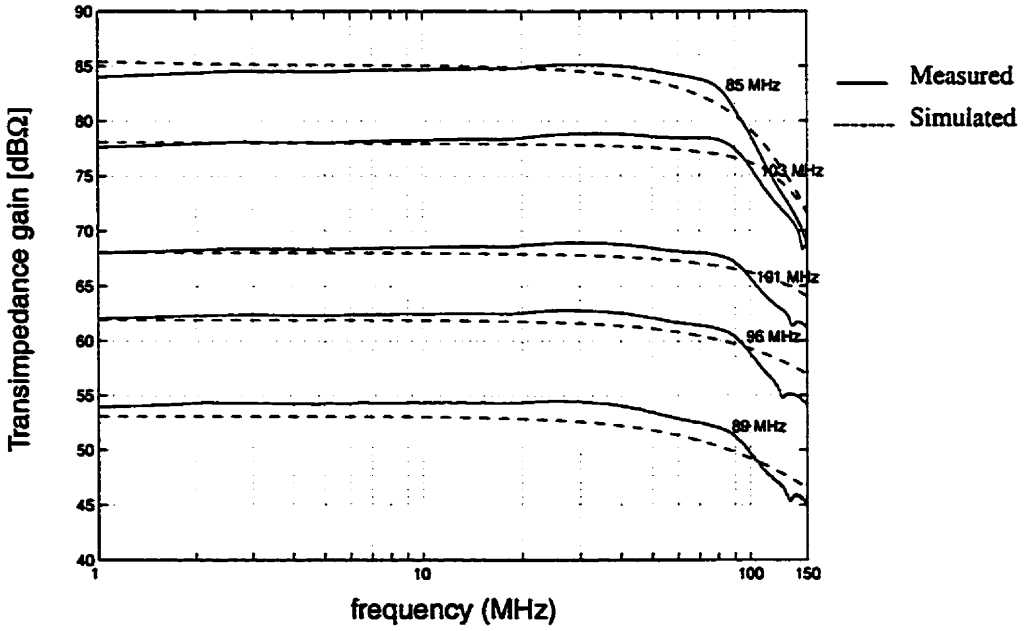


Figure 6.23 Simulated and measured frequency response of transimpedance amplifier.

The operation of the ambient light rejection feedback loop is illustrated in the step response shown in Figure 6.25. Here, a 10 μA dc current is injected into the preamplifier. The dc rejection loop is initially disabled, and then activated at the

indicated point on the graph. The total settling time is 6 μs which agrees with simulation.

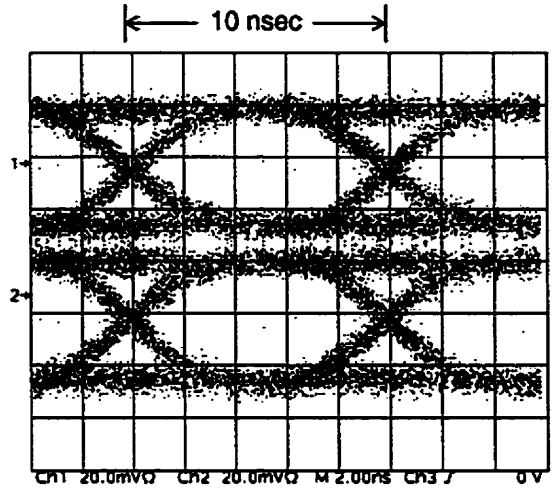


Figure 6.24 Eye diagram for 100 Mb/s optical link with 19kΩ transimpedance gain.

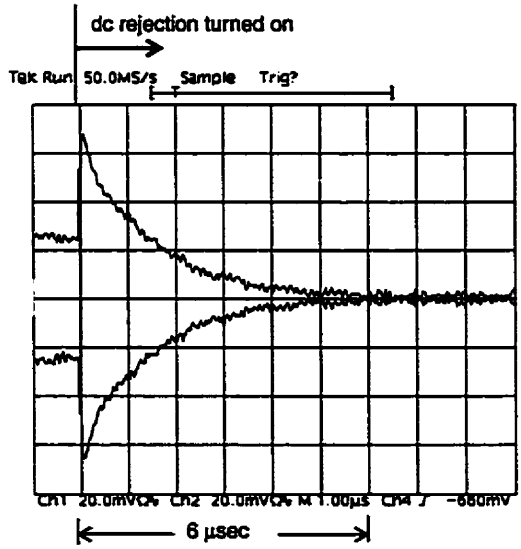


Figure 6.25 Measured step response of dc photocurrent rejection circuit to 10 μA dc input.

6.3 SUMMARY AND STATE-OF-THE-ART COMPARISON

Two optical preamplifier ICs fabricated in standard 0.35μm CMOS technology were presented in this chapter. The first was an optical receiver front-end consisting

of a transimpedance amplifier and two post amplifiers. The front-end consumed 1mW from a 1V supply, and did not require the use of low-threshold devices. It provided a transimpedance gain of 210kΩ at 75Mb/s, and incorporated an on-chip charge pump for the biasing and tuning of MOS resistors. The second IC was a fully-differential variable-gain transimpedance amplifier embedded in a larger feedback loop used to reject ambient light. The preamplifier consumed 8mW at 3V, and provided a 70MHz bandwidth over a 77dB dynamic range with a maximum transimpedance gain of 19kΩ. Both ICs displayed well-controlled bandwidths across their gain ranges, albeit through completely different mechanisms.

Table 6.3 places these two IC designs alongside other recent transimpedance amplifier designs. Our variable-gain transimpedance amplifier is the first reported fully-differential design. Other variable-gain transimpedance amplifiers reported to date have been single-ended designs fabricated in either bipolar or BiCMOS technology, and have not been designed for supply voltages lower than 5V. The differential CMOS transimpedance amplifier presented by Tanabe [Tanabe,1998] could be adapted to have variable gain; with only one gain stage, the circuit's stability is ensured, albeit possibly at the cost of reduced bandwidth. The transimpedance amplifier presented by Ingels [Ingels,1994] has varying gain, but the gain variations are uncontrolled, making the circuit more of a limiting amplifier rather than a true variable-gain design. Despite the large 5pF input capacitance, our 3V transimpedance amplifier achieves a bandwidth of 70 MHz that is sufficient for a 100 Mb/s data rate.

The 1V optical receiver front-end IC is significant in that it is the first reported design capable of 1V operation. At 1mW, it is also the lowest power optical front-end IC reported for use in high-speed data communications. In addition, this IC represents the first experimentally verified use of charge pumps for the stable biasing of MOSFETs. Despite its low power, the design still maintains a moderate bandwidth with moderate noise performance. With two post gain stages, this design has the second largest transimpedance gain of all the designs.

Reference	Outputs	Technology	Supply (V)	Power (mW)	Cin (pF)	Gain (kΩ)	Input Noise ($pA/\sqrt{Hz}$)	Dynamic Range (dB)	Band-width (MHz)	Data Rate (Mb/s)
[Meyer,1994]	single	0.8μm BiCMOS	5	110	1.0	98 ~ 0.16	1.17	107	128	--
[Khorrama-badi,1995]	single	1.0μm BiCMOS	5	>120	0.4	10.7 ~ 0.4	--	>80	600	1060
[van den Broeke,1993]	single	2.5GHz Bipolar	--	--	2.0	1	4.0	73	220	--
[Palojarvi,1997]	single	0.8μm BiCMOS	5	<250	6.7	260 ~ 1.1	6	80	170	--
[Mohan,1999]	differential	0.5μm CMOS	--	118	0.6	1.6	17.3*	64	1200	2125
[Ingels,1994]	single	0.8μm CMOS	5	20	1.0	150	1*	--	120	240
[Razavi,2000]	single	0.6μm CMOS	3	30	--	8.7	4.5	--	500	622
[Nakamura,1999]	--	0.35μm CMOS	1.2	< 35	--	--	--	--	--	50
[Tanabe,1998]	differential	0.15μm CMOS	2	22	0.3	0.89	9.75*	--	1900	2400
3V preamplifier	**differential**	**0.35μm CMOS**	**3**	**8**	**5.0**	**19 ~ 0.5**	**6.7**	**77**	**70**	**100**
1V Front-End	**single**	**0.35μm CMOS**	**1**	**1**	**1.0**	**210 ~ 19**	**11**	**54**	**50**	**75**

Table 6.3 A comparison of recent CMOS optical front-end designs. An asterisk (*) denotes a simulated result.

REFERENCES

E. M. Cherry and D. E. Hooper, "The design of wide-band transistor feedback amplifiers," *Inst. Elec. Eng. Proc.*, vol. 110, no. 2, pp. 375-389, February 1963.

R. Gomez and A. Abidi, "A 50MHz CMOS variable gain amplifier for magnetic data storage systems," *IEEE J. Solid-State Circuits*, vol. 27, pp. 935-939, December 1992.

M. Ingels, G. Van der Plas, J. Crols, and M. Steyaert, "A CMOS 18 THzΩ 240 Mb/s Transimpedance Amplifier and 155Mb/s LED-Driver for Low Cost Optical Fiber Links," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1552-1559, Dec. 1994.

D. A. Johns and K. W. Martin, *Analog Integrated Circuit Design*, New York: Wiley, pp. 246-250, 1997.

H. Khorramabadi, L. D. Tzeng, and M. J. Tarsia, "A 1.06 Gb/s -31 dBm to 0dBm BiCMOS Optical Preamplifier Featuring Adaptive Transimpedance," *IEEE ISSCC Digest of Tech. Papers*, pp. 54-55, Feb. 1995.

R. G. Meyer and W. D. Mack, "A Wideband Low-Noise Variable-Gain BiCMOS Transimpedance Amplifier," *IEEE J. Solid-State Circuits*, vol. 29, no. 6, pp. 701-706, June 1994.

S. S. Mohan, and T. H. Lee, "A 2.125Gbaud 1.6kohm Transimpedance Preamplifier in 0.5um CMOS," *IEEE Proc. CICC*, pp. 513-516, May 1999.

M. Nakamura and N. Ishihara, "1.2V, 35mW CMOS optical transceiver ICs for 50Mbit/s burst-mode communication," *Electronic Letters*, vol. 35, no. 5, pp. 394-395, 4 March 1999.

P. Palojarvi, T. Ruotsalainen, and J. Kostamovaara, "A Variable Gain Transimpedance Amplifier Channel with a Timing Discriminator for a Time-of-Flight Laser Radar," *Proc. European Solid-State Circuits Conf.*, pp. 384-387, Sept. 1997.

B. Razavi, "A 622Mb/s $4.5 pA/\sqrt{Hz}$ CMOS Transimpedance Amplifier," ISSCC Dig. of Tech. Papers, pp. 162-163, Feb. 2000.

J. M. Steininger, "Understanding Wide-Band MOS Transistors," *IEEE Circuits and Devices*, vol. 6, no. 3, pp. 26-31, May 1990.

A. Tanabe et al., "A Single Chip 2.4 Gb/s CMOS Optical Receiver IC with Low Substrate Crosstalk Preamplifier," *IEEE ISSCC Digest of Tech. Papers*, pp. 304-305, Feb. 1998.

L. A. D. van den Broeke and A. J. Nieuwkerk, "Wide-Band Integrated Optical Receiver with Improved Dynamic Range Using a Current Switch at the Input," *IEEE J. Solid-State Circuits*, vol. 28, no. 7, pp. 862-864, July 1993.

C. K. Wang, P. C. Huang and C. Y. Huang, "A Fully Differential CMOS Transconductance-Transimpedance Wideband Amplifier," *IEEE Trans. Circ. and Syst. II*, vol. 42, no. 11, pp. 745-748, November 1995.

CHAPTER

7 Conclusions

7.1 SUMMARY AND CONCLUSIONS

We have discussed the design of transimpedance amplifiers for use in optical receivers. Our approach to the discussion has been from two perspectives: that of the circuit and that of circuit's *design*.

From a circuit perspective, we have looked at specific topologies used to address the added requirements of wide dynamic range, ambient light rejection, and low-voltage operation. To achieve a wide dynamic range, we presented a fully-differential, variable-gain CMOS transimpedance amplifier. The design is significant because it overcomes the stability problems common in existing variable-gain implementations. The presented topology is simpler, and the stability of the circuit is ensured with the simple tracking of identical resistors. The implemented design consumed 8mW at 3V, and provided 70 MHz bandwidth with a dynamic range of 77dB, a maximum transimpedance gain of 19kΩ, and a gain range of 32dB.

To reject ambient light, we placed the transimpedance amplifier within an active feedback loop. In contrast with existing ac coupled designs, this topology eliminates the need for large passive devices and improves the regulation of the photodiode bias voltage. However, the lower-frequency limit of this topology is dependent on the ambient light level. The contributions of this thesis include identifying this characteristic and discussing its practical implications, experimentally verifying the technique, and analyzing the stability requirements of this topology.

To achieve low-voltage operation, we developed a transimpedance amplifier capable of 1V operation without the use of low-threshold devices. The design has a wide output swing and effectively maximizes the available bias voltage for the photodiode. The biasing of the MOS feedback resistor was performed using a charge

pump to generate a stable gate voltage, a technique called dynamic gate biasing (DGB). The proposed design was implemented as part of an optical receiver front-end which also included two post amplifiers. The resulting front-end consumed 1mW from a 1V supply and provided 210kΩ transimpedance gain for data rates up to 75Mb/s. This circuit is significant in three respects: it is the first reported transimpedance amplifier capable of 1V operation, it has the lowest power dissipation of any reported high-speed optical front-end, and it is the first reported experimental use of DGB for the stable biasing of transistors.

Beyond our discussion of specific circuits, we have also approached the question of *how* a circuit is designed, and have taken an introspective look at the analysis and design process itself. Our discussion has centred on a graphical circuit analysis technique called DPI/SFG analysis that is based on representing driving-point impedance (DPI) relationships using signal-flow graphs (SFG). The transimpedance amplifier serves as an excellent vehicle for this discussion because its demanding requirements and complex design trade-offs typify the challenges faced in analog circuit design.

In this thesis, we described DPI/SFG analysis and illustrated its application. Thus far, DPI/SFG analysis has been explained principally through specific circuit examples. Our contribution was to develop a general formulation of the method, first by justifying driving-point impedance analysis as a cause-and-effect interpretation of Kirchhoff's Current Law, and then by applying signal-flow graph theory. We illustrated the method on a range of circuits involving transistors and ideal building blocks. Our two particular contributions were in showing how circuits with floating voltage sources could be handled, and in using the method to derive Blackman's Impedance Formula.

Having described DPI/SFG analysis, we applied it to the design of the low-voltage transimpedance amplifier. We derived an analytic model of the circuit consisting of a simplified set of equations describing its bandwidth, pole locations, and noise, as well as a first-order schematic model of its input and output impedance. We then used this analytic model to optimize the circuit.

The significance of the DPI/SFG analysis method lies in its ability to visually represent the complex dynamics of a circuit. The signal-flow graph is complete with no simplifications, and yet it provides *a framework* for simplification by breaking down the complex interactions within a circuit into individual graph branches and nodes. This decomposition allows the designer to make small, isolated simplifications that progressively reduce the graph until only the essential features of the circuit are represented.

Design is as much an art as it is a science, and ultimately the question of what design method is best rests with the designer. We have strived here to present DPI/SFG analysis clearly, and to provide enough background for the reader to learn the method in order to draw his or her own conclusions.

7.2 FUTURE WORK

There are numerous directions for future work on transimpedance amplifiers. As mentioned in the discussion of the low-voltage design, an alternative topology exists in which the feedback resistor is placed directly across the input and output terminals of the current mirror as shown in Figure 7.1 [Martin,2000]. This topology was not initially not pursued because the circuit sets the bias voltage of the output to be equal to that of the input, resulting in almost no output swing. The advantage of this topology, however, is the much lower input impedance seen by the photodiode which may potentially improve speed provided the existing limitation in output swing can be overcome.

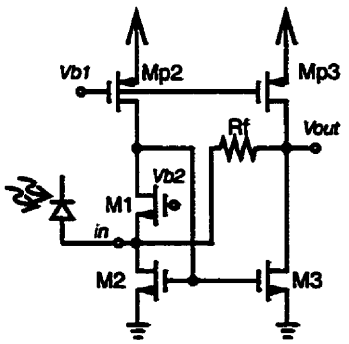


Figure 7.1 Alternative topology for low-voltage transimpedance amplifier.

For ambient light rejection, we have presented an alternative feedback topology that realizes differential photocurrent sensing, provides improved supply noise rejection, and eliminates the need for a dummy matching capacitor [Zand,1999]. A fully-differential implementation of the low-voltage transimpedance amplifier design could be implemented to improve supply noise rejection. Finally, work into optoelectronic integrated circuits (OEIC) could be initiated with the integration of a CMOS photodetector alongside one of the existing transimpedance amplifier designs.

As analog designers look for ways to meet the challenge of decreased supply voltages, dynamic gate biasing (DGB) has the potential to become a general technique for realizing low-voltage analog circuits. However, before DGB can be more widely applied, we need a better understanding of the effects of charge injection and clock feedthrough on circuit performance. Future work should focus on developing methods of reducing such transient effects. At the same time, additional applications of DGB need to be investigated. One example would be its use in tunable, low-voltage, continuous-time filters.

Future work on DPI/SFG analysis is likely to focus on automating the analysis process, and in investigating its use in computer-aided design (CAD) for analog circuits. In practice, the manipulation of signal-flow graphs by hand is limited to only the simplest of circuits. There is a need to develop a computer-aided analysis tool that can automate much of the generation and manipulation of signal-flow graphs in the same way today's math software has eliminated the need to perform cumbersome elimination of variables for sets of linear equations.

Recent published efforts such as [Spence,1999] and [Katzenelson,1999] show that CAD for analog circuits is entering a renaissance period with the emphasis shifting towards providing a greater understanding of circuit behaviour beyond simply determining performance characteristics. The continual trend towards greater integration, lower voltages, and lower power will drive the development of novel circuit techniques. Future circuit designers will require a greater ability to investigate circuit sensitivity to device parasitics, process variations, and noise from the

supply and substrate. DPI/SFG analysis can play an integral part in analog CAD by allowing the analysis and manipulation of circuits at a symbolic level with greater ease.

REFERENCES

J. Katzenelson and A. Unikovski, "Symbolic-Numeric Circuit Analysis or Symbolic Circuit Analysis with Online Approximations," *IEEE Trans. Circ. and Syst. I*, no. 1, pp. 197-207, Jan. 1999.

K. Martin, private communication, 2000.

R. Spence, "The Facilitation of Insight for Analog Design," *IEEE Trans. Circ. and Syst. II*, vol. 46, no. 5, pp. 540-548, May 1999.

B. Zand, K. Phang, and D.A. Johns, "Transimpedance Amplifier with Differential Photodiode Current Sensing," *IEEE Int. Symp. Circuits and Systems*, Orlando, FA, vol. 2, pp. 624-627, May 1999.

APPENDIX

A Analysis of Feedback Amplifier Using DPI/SFG

In this section, we illustrate how DPI/SFG analysis is applied to the two-stage transistor feedback amplifier example introduced in Chapter 2. The circuit is shown again in Figure A.1. This example also serves as a comparison of DPI/SFG analysis with traditional nodal and topology-based feedback analysis. Assuming $g_m = 100mA/V$, $\beta = 100$, and ignoring the Early effect for both transistors, let us determine the input and output resistance as well as the voltage gain of the amplifier.

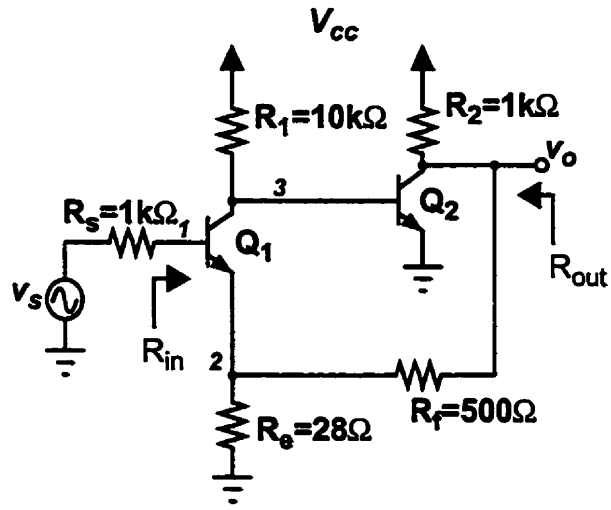


Figure A.1 Two-stage amplifier with feedback.

Having derived the signal-flow graph (SFG) for the bipolar transistor in Chapter 4, the SFG for this circuit can be obtained by simply connecting together the individual device SFGs as shown in Figure A.2. The superposition of the circuit schematic atop of the circuit SFG allows us to see the structural similarities between the two representations of the circuit. This superposition helps provide visual clues to the various feedback paths found in the circuit. We can simplify this graph by noting

that part of the SFG for Q_2 can be eliminated because of its common-emitter configuration. The final SFG including all the branch and node expressions is shown in Figure A.3. The various branch transmittances are calculated below:

$$\begin{array}{lll} a = 0.001S & b = 500\Omega & c = -0.1S \\ d = 909.09\Omega & e = -0.1S & f = 333.33\Omega \\ g = 0.002S & h = 0.101S & i = 7.209\Omega \\ j = 0.001S & k = 0.1S & l = 0.002S \end{array}$$

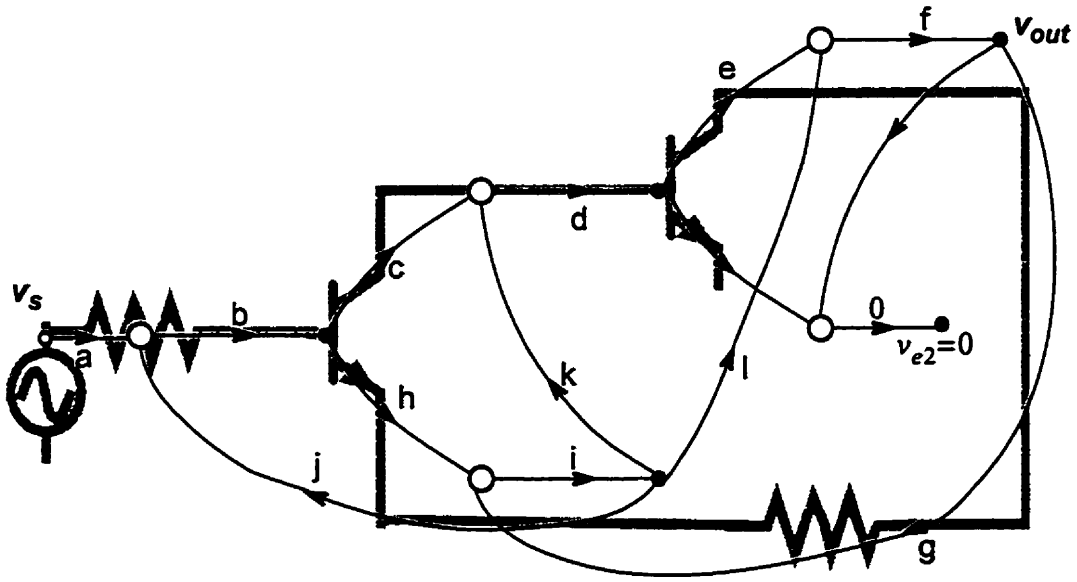


Figure A.2 SFG for wideband feedback amplifier.

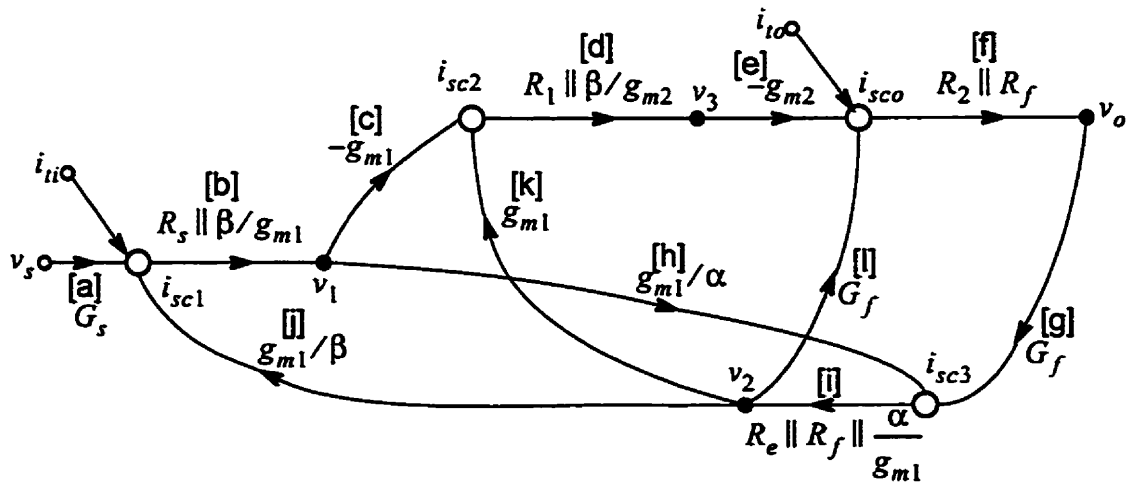


Figure A.3 Simplified SFG for wideband feedback amplifier.

Since this SFG is rather involved, we will use Mason's Direct Rule rather than manually manipulating the SFG. We observe that there are four distinct feedback loops in Figure A.3. In terms of their loop transmittances, they are

$$L_1 = bcdefgij = 21.8456$$
$$L_2 = defgik = -43.6913$$
$$L_3 = fgil = 0.0096$$
$$L_4 = bhij = 0.3641$$

Notice how the loop transmittances give us a sense of the relative strengths of the various feedback loops of the circuit; loops L_1 and L_2 represent the feedback paths across the two gain stages and back through feedback resistor R_f and they are the strongest while loop L_3 is by far the weakest, representing the reflection of the output signal through the feedback resistor R_f. Since all loops include branch transmittance *i*, there are no non-touching loops, thus

$$\Delta = 1 - (L_1 + L_2 + L_3 + L_4) = 22.472.$$

For the voltage gain, we can identify three forward transmission paths through the SFG:

$$P_1 = abcdef = 1515.2 \qquad \Delta_1 = 1$$
$$P_2 = abhikdef = -1103.2 \qquad \Delta_2 = 1$$
$$P_3 = abhilf = 0.2 \qquad \Delta_3 = 1$$

Again, from the SFG, we gain a sense of the relative strengths of the forward transmission, and confirm how insignificant the feedforward path through the feedback resistor R_f is relative to the main signal path through the two transistors. The final transfer function is

$$Gain = \frac{v_o}{v_s} = \frac{P_1\Delta_1 + P_2\Delta_2 + P_3\Delta_3}{\Delta} = 18.3.$$

Finding the input impedance is simple; having already determined Δ, we only need to determine the forward transmission path from i_{scI} to v_I:

$$P_1' = b = 500\Omega \qquad \Delta_1' = 1 - (L_2 + L_3) = 44.68.$$

Thus,

$$\frac{v_1}{i_{ti}} = \frac{P_1'\Delta_1'}{\Delta} = 994.16\Omega$$

To find the input resistance, we see that

$$\frac{v_1}{i_{ti}} = R_s \| R_{in}$$
$$994.16 = 1000 \| R_{in}$$
$$\therefore R_{in} = 170k\Omega$$

Finding the output resistance is done the same way, again reusing most of the previous calculations:

$$P_1'' = f = 333.33\Omega \qquad \Delta_1'' = 1 - L_4 = 0.6359 \ .$$

Thus,

$$R_{out} = \left.\frac{v_o}{i_{sc0}}\right|_{v_s = 0} = \frac{P_1''\Delta_1''}{\Delta} = 9.43\Omega$$

Comparison with Other Circuit Analysis Techniques

The analysis of this circuit using nodal analysis, topology-based feedback analysis, and feedback analysis using return ratios was presented in Chapter 2. Direct nodal analysis is both mathematically exact and straightforward to solve especially with the aid of calculators or computers capable of matrix operations. Unfortunately, this method is the least insightful as it reduces the circuit to a mere set of equations.

Greater insight into the role of feedback is obtained with topology-based feedback analysis. Here, the loop gain provides a measure of the amount of feedback in the circuit. Unfortunately, there are numerous limitations with this technique.

Firstly, we face the challenge of trying to make all circuits conform to the classical feedback structure. One consequence is that we must identify the topology that best describes the circuit. Often this is not altogether apparent. Secondly, for circuits which do not approximate the ideal case, all nonidealities such as loading effects must be accounted for by modifying the principle blocks. These parameters are obtained through a process of modifying the original circuit and measuring a variety of port parameters under short-circuit and open-circuit conditions. This process is involved, and prone to mistakes. Lastly, this analysis implicitly assumes that both the forward amplifier and feedback network are unilateral and that the signal traverses forward only through the amplifier and the output is fed back only through the feedback network. With many practical circuits, this is an assumption whose validity is difficult to ascertain, and should the underlying assumptions prove to be inaccurate, there is essentially no recourse. With this method, every analysis must be followed up by an exact analysis or computer simulation. As such, this method should not be considered a complete circuit analysis technique, but is best thought of as an intuitive aid to understanding feedback circuits.

The main advantage of feedback analysis using return ratios over topology-based analysis is that the technique neither requires the partitioning of the amplifier into two distinct components nor requires the identification of the sampling and mixing mechanisms. Beyond this, however, the analysis method shares many of the same limitations. Both methods require breaking the internal feedback and analyzing modified versions of the circuit. Determining port impedances involves measuring a variety of port parameters under short-circuit and open-circuit conditions. This process is involved, not at all intuitive, and so prone to mistakes. The concept of a return ratio is also, at best, a difficult concept when applied to real circuits. Finally, neither feedback analysis technique is suited to circuits with multiple or otherwise complex feedback mechanisms.

DPI/SFG analysis, on the other hand, requires no approximations, makes no assumptions, and is not limited to circuits with only a single feedback loop. Because of its use of signal-flow graphs, DPI/SFG analysis provides a designer with an intu-

itive representation of circuit dynamics that enhances his or her insight into a circuit's operation. One of the principal concerns that can be raised with DPI/SFG analysis, is its complexity. As much as the above example illustrates the power of DPI/SFG analysis, it also amply demonstrates the general complexity of analyzing signal-flow graphs. In practice, the manipulation of signal-flow graphs by hand is practically limited to small circuits. In the long run, computer-aided analysis tools need to be developed to help automate much of the generation and manipulation of signal-flow graphs much in the same way current matrix math software has eliminated the need to perform cumbersome elimination of variables by hand for sets of linear equations.

APPENDIX

B High-Frequency Transistor Models

The small-signal transistor models presented in Chapter 4 are sufficient for many applications. In instances where a more accurate representation of the high-frequency performance of a device is required, however, a more complex small-signal model such as the enhanced hybrid-π model shown in Figure B.1 is necessary. This model accounts for the base spreading resistance and the dominant parasitic capacitances of the bipolar transistor. The corresponding SFG is shown in Figure B.2. The high-frequency model for the MOS transistor is shown in Figure B.3, and the corresponding SFG is shown in Figure B.4. These SFGs have been included in the thesis for completeness, and to help highlight the complex interactions which are introduced by the presence of parasitic elements.

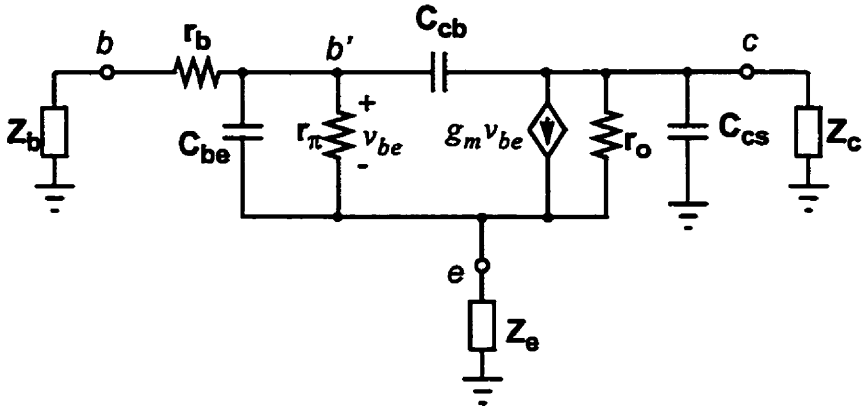


Figure B.1 High-frequency model of a bipolar transistor.

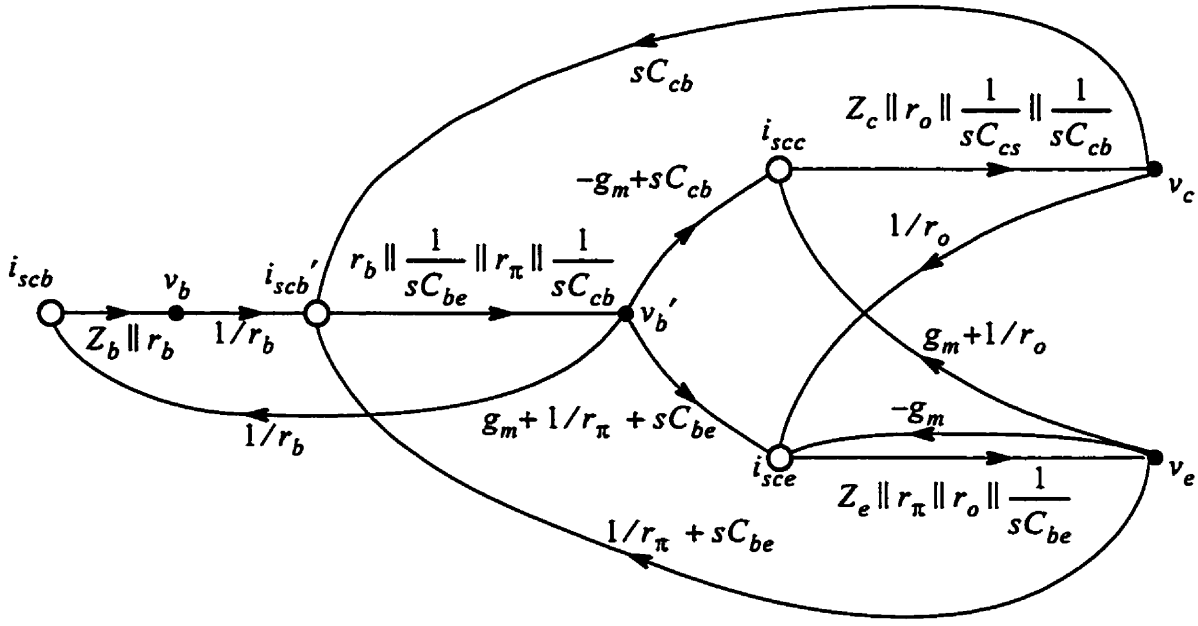


Figure B.2 SFG for the high-frequency bipolar transistor model shown in Figure B.1.

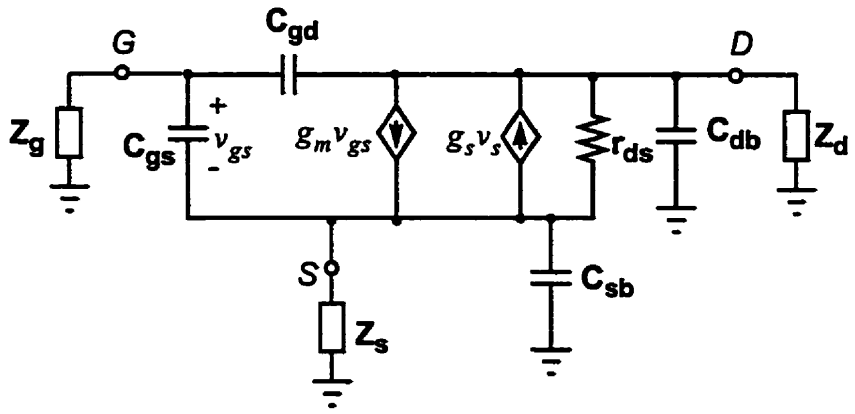


Figure B.3 High frequency model of a MOS transistor.

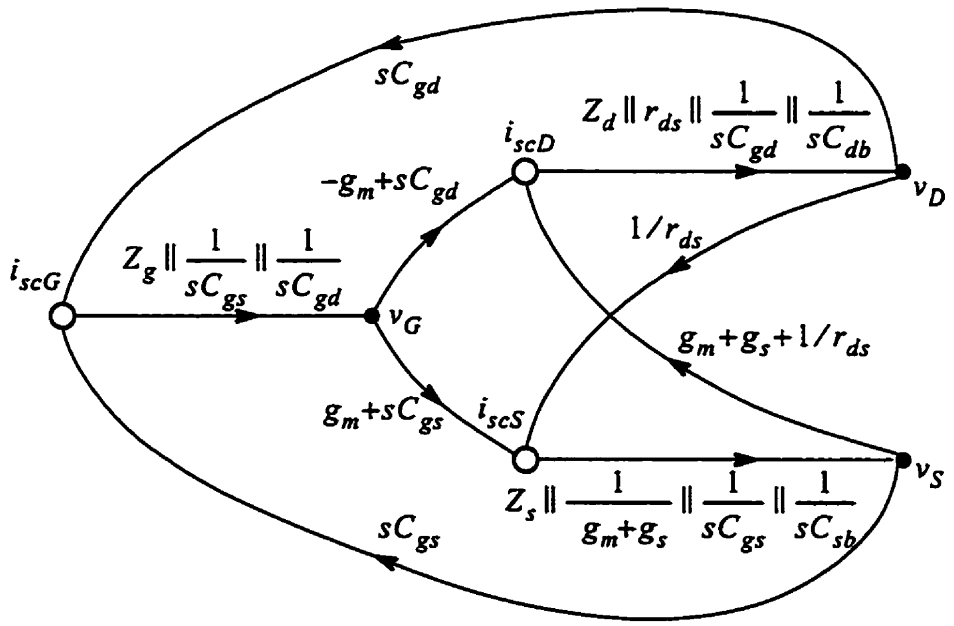


Figure B.4 SFG for the high-frequency MOS transistor model shown in Figure B.3.