

A power scaleable and low power pipeline ADC using power resettable opamps

By

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Abstract

A 10-bit pipeline Analog-to-Digital Converter (ADC) is designed such that its average power is scaleable with sampling rate over a large variation of sampling rates. Fabricated in CMOS 0.18 μm technology, while having an area of 1.21mm², the ADC uses a novel fast Power Resettable Opamp (PROamp), to achieve power scalability between sampling rates as high as 50Msps (35mW), and as low as 1ksps (15 μW), while having 54-56dB of SNDR (at Nyquist) for all sampling rates. A current modulation technique is used to avoid weakly inverted transistors for low bias currents, thus avoiding less accurate simulation, poorer matching, and increased bias sensitivity. The PROamp due to its short power on/off time also affords reduced power consumption in high speed pipeline ADCs, where opamps can be completely powered off when not required. Measured results show an ADC using PROamps has 20-30% less power than an ADC which does not use PROamps.

Acknowledgements

Researching a thesis is a unique proposition. One is forced to look into the depths of the unknown and find an answer to a question that does not necessarily have an answer. In some cases your answer fits the question – in some cases your answer fits the question like a square peg in a round hole. Regardless of the madness, the journey of developing a thesis from abstract ideas to ultimately a functional prototype is truly a unique and completely enriching experience - an experience that I for one am tremendously thankful for and very fortunate to have undergone. Acknowledging specific people in the development of an abstract piece of art as a thesis is somewhat partial, as undoubtedly every person one interacts with during the course of a thesis in some shape or form impacts the work. There are few however who have helped this piece of abstract art take form. Of course firstly I must thank my supervisor, Professor David Johns. No doubt without his aid in developing the focus of this work, and his invaluable suggestions and advice throughout the duration of this degree, this work would not have been possible. Next I am tremendously indebted to the aid and friendship of the ‘Master’s crew’, of Navid, Rob, and Trevor who in addition to helping me develop and refine my skills as a mixed-signal designer, have made my tenure as a Master’s student at U of T, truly enriching and thoroughly enjoyable. There are of course others who shall remain nameless, whose support and encouragement during the lows of lows and highs of highs was both welcome and much needed. Inspiration can come from surprising sources - a wise researcher should always be aware of this. Of course one cannot accomplish anything in life without the unquestioned pillar of support one’s family offers. To my family I dedicate this work, for whom without I would not be where I am today.

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List of abbreviations

ADC	Analog to Digital Converter
CMFB	Common Mode Feed Back
CMPS	Current Modulated Power Scale
DAC	Digital to Analog Converter
ENOB	Effective Number of Bits
FOM	Figure of Merit
IC	Inversion Coefficient
MDAC	Multiplying Digital to Analog converter
MIM	Metal-Insulator-Metal
NM	Nominal Mode
PRM	Power Reduction Mode
PROamp	Power Resettable Operational Amplifier
S&H	Sample and Hold
SFDR	Spurious Free Dynamic Range
SNR	Signal to Noise Ratio
SNDR	Signal to Noise plus Distortion Ratio
SRBO	Switched Replica Bias Opamps

CHAPTER ONE

Introduction

1.1: Overview

ADCs that have a power which reduces with sampling rate can significantly reduce manufacturer and customer costs. A single power scaleable ADC can be used by a manufacturer to target multiple applications with different performance requirements - saving development costs, and reducing time to market. Similarly a customer can purchase only a single ADC model to meet requirements for multiple applications. Low power applications requiring multiple operating speeds and multiple standard compliancy (e.g.: mobile, biomedical, etc.) also benefit from a single ADC with scaleable power

Conventional CMOS digital logic consumes mainly dynamic power during output transitions, thus power management in the digital domain can be easily achieved. In other words, if a CMOS digital block is clocked slower, less power is consumed as fewer output transitions occur. Thus digital sub-systems automatically adjust their power according to their operating speed. As ADCs are dominated by analog circuitry, ADCs do not have a power that optimally scales with operating speed. Analog power is dominated by static power, where fixed bias currents and fixed supply voltages are used for specific operation speeds (where $P=IV$). Thus analog power is scaled with operating speed if the bias current and/or supply voltage to the ADC are made functions of the operating speed. As extended voltage scaling degrades *Signal to Noise Ratios* (SNR), power is often scaled in ADCs by only scaling bias currents with operating speed (i.e. sampling rate, f_s). Since analog subsystems are carefully characterized and optimized by setting specific bias currents, a significant variation of bias currents to reduce power with speed, leads to lengthy design times, and costly post design verification to validate functionality over the multiple design corners. Furthermore, as bias currents are reduced, transistors shift from strong to weak-inversion operation. Current mirrors in weak inversion match substantially poorer, resulting

in sub-optimal power distribution, and are susceptible to significant performance degradation due to a high sensitivity of drain-source currents to bias voltages. As such designs in weak inversion have a poorer yield unless a conservative design approach is taken [1].

In this dissertation a 10-bit pipeline ADC is presented which uses pulse-width modulated currents to achieve power scaleability over ultra wide variations in sampling rate, without relying on excessive current scaling, thus avoids placing the ADC transistors deep in weak inversion for very low sampling rates. By sequencing the operation of each pipeline stage according to timing set by a digital controller that completely powers off the pipeline ADC between conversions, a power scaleable range which multiplies the power scaleable range of current scaling by over 1000x is shown to be achieved in a functional 0.18 μ m CMOS prototype. Although powering off the ADC between conversions is a technique used in industry to achieve scaleable power, such ADCs have been restricted to slower architectures (<500ksps). This work represents the first known ADC which using a pipeline architecture is capable of achieving power scaleability at sampling rates as high as 50Msps, and as low as less than 1ksps (i.e. power scaleable range of >50,000), without resorting to extensive current scaling (thus avoiding the problems of transistors biased deep in weak inversion).

To implement the power-scaleable architecture, a novel *Power Resettable Opamp* (PROamp) was developed which is capable of completely powering on/off in a very short time interval. The short on/off time of the novel opamp also allows for an improved ADC figure of merit, as opamps can be completely powered off when not required (e.g.) the sampling phase of a sample and hold or pipeline *Multiplying Digital to Analog Converter* (MDAC). As such, the pipeline ADC was designed such that the opamp is only powered on during hold phases in sample-and-hold and MDAC circuits. To quantify the reduction in power the ADC was designed with an additional mode of operation where when the pipeline ADC operates at full rate, the opamps always remain on (i.e. the ADC operates as a conventional pipeline ADC). Measured results show power is reduced from 44mW to 35mW when only powering the opamps during the hold phase, for $f_s=50$ Msps, while achieving an accuracy of ~ 55 dB SNDR (~ 1.6 pJ/step). As such the PROamp is shown to be a highly useful block to enable advanced power management in high-speed analog circuits.

1.2: Thesis outline

The dissertation details the development of an ADC that has power scalability over very wide range of sampling rate. Chapter two provides the reader with background information as to why ADCs are required in signal processing and how pipeline ADCs operate at the system level. Chapter three outlines common circuit implementations of key sub-blocks in the pipeline ADC, as well as addressing essential design trade-offs at the circuit level. Chapter four addresses the dependency of power with sampling rate, where issues associated with current scaling are elaborated. In chapter five the circuit implementation for this dissertation, including the digitally controlled pipeline architecture, and 50Msps Pipeline ADC with reduced power using the Power Resettable Opamp is described. Key simulation results and performance limitations are discussed and analyzed. Chapter six discusses the measured results of the fabricated 0.18 μ m CMOS Integrated Circuit, and chapter seven concludes the thesis, and briefly discusses potential future research directions.

CHAPTER TWO

ADC architectures

2.1: Overview

In this chapter a comparison of analog versus digital information is given, where the superior noise resilience of digital signals is shown to necessitate digital signaling for modern high-speed signaling environments. Non-idealities that are analog in nature are shown to necessitate ADCs in the digital signal path, which allow for signal recovery in the digital domain. A brief discussion of the Flash ADC is given, followed by a detailed analysis of the system level design of a 1.5 bit/stage pipeline ADC.

2.2: Analog vs. Digital Information

Analog signals have an infinite number of output states, whereas digital outputs have a finite number of states. Illustrations of analog and digital signals are given in Fig. 2-1, and Fig. 2-2 respectively.

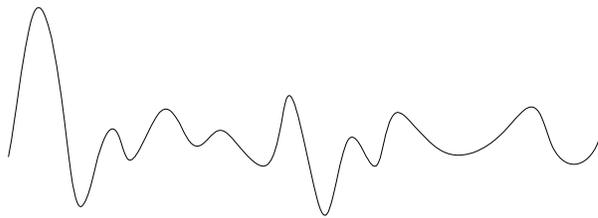


Fig. 2-1: Example of an analog signal

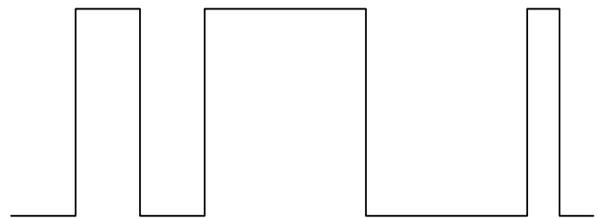


Fig. 2-2: Example of a digital binary signal

As digital signals have a finite symbol set, they are much easier to accurately recover at a receiver than analog signals. For example if a transmitted binary digital signal is distorted by a white noise source, it is still possible to precisely determine if a ‘1’ or ‘0’ was transmitted

so long as the noise source is sufficiently small (maximum noise limitations on digital signaling can be found in [2]). If a transmitted analog signal encounters the same noise source however, the received analog signal is permanently distorted as shown in Fig. 2-3, thus the transmitted signal cannot be accurately recovered (since an analog signal can be any value between maxima, the receiver cannot accurately distinguish the noise from the signal). With modern communication systems requiring fast and accurate signaling over noisy channels (E.g.: air, telephone wires, coaxial cables, power lines, etc.), digital transmission as shown in Fig. 2-4 is commonly used.

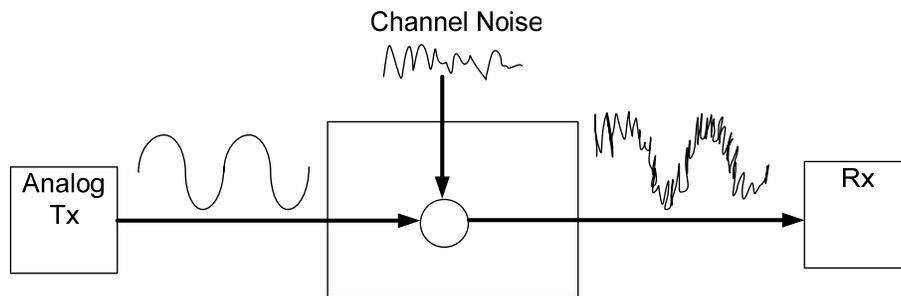


Fig. 2-3: Analog signal transmission

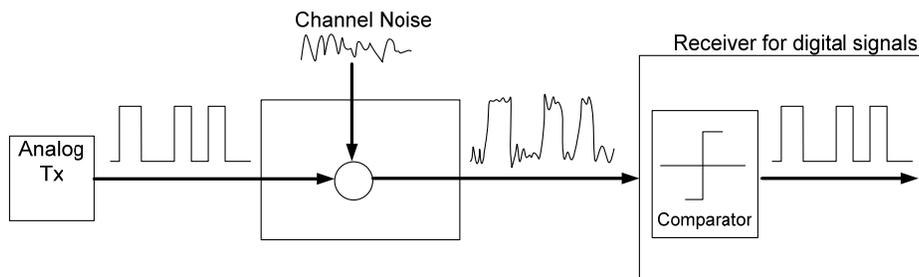


Fig. 2-4: Digital signal transmission of binary data

Although digital transmissions facilitate simpler receivers, channel distortion (e.g. echo, cross-talk, skin effect losses, etc.), which cannot be removed with a single comparison operation as shown in Fig. 2-4, necessitate more complicated receivers which perform a mathematical analysis to recover the transmitted signal. As a mathematical analysis can be easily performed in the digital domain, an ADC is required to convert the noisy receiver input to a digital representation for digital signal processing, as shown in Fig. 2-5.

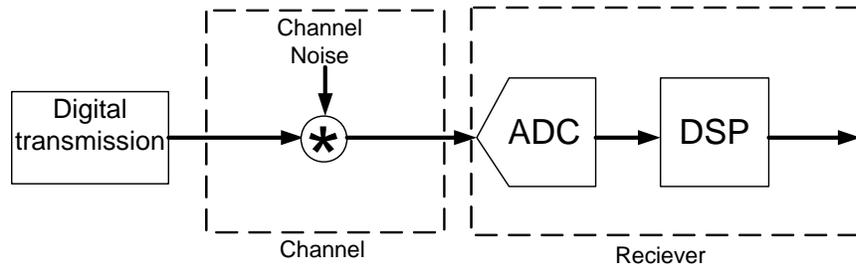


Fig. 2-5: ADC in signal path of a digital communication system

In general ADCs are required blocks when a digital system interfaces with an analog environment.

2.3: ADC architectures – Flash ADC

Various ADC architectures have been developed over the years, each with different tradeoffs with respect to power, speed, and accuracy (details in section 2.5). Most ADC architectures however are in some form a variant of the Flash ADC. Flash ADCs *measure* an analog signal into a digital signal by comparing an analog input to fixed reference values as shown in Fig. 2-6. The number of fixed references used determines the accuracy of the digital output (e.g.) 4-bit accuracy is obtained by comparing against $2^4=16$ reference values, 10-bit accuracy by comparing against $2^{10}=1024$ reference values. Determining which reference values the input is in-between forms a length 2^N bit (where N is the accuracy of the ADC) thermometer code representation of the analog input. Mapping the unique thermometer code to its binary equivalent forms a length N, binary representation of the analog input [3].

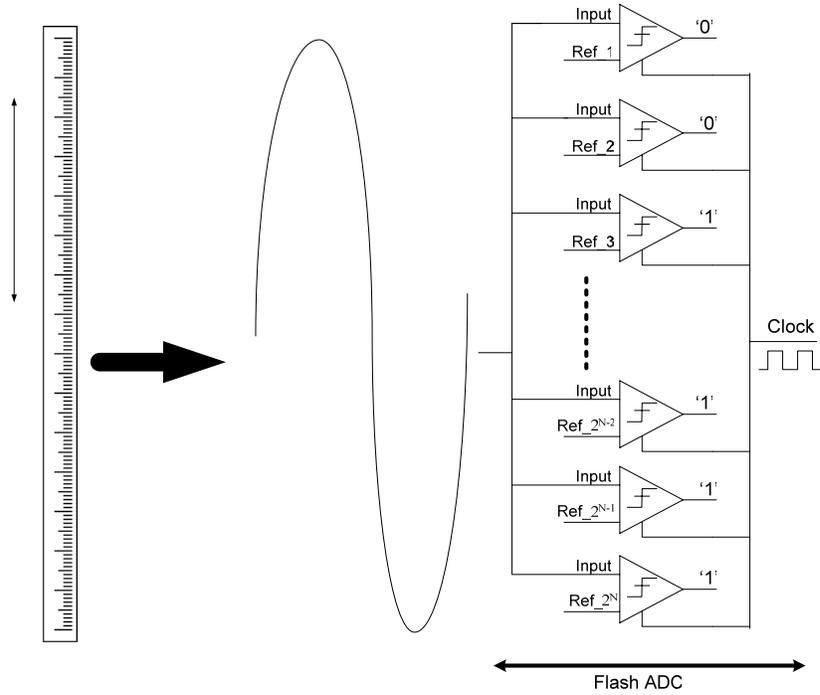


Fig. 2-6 Analogy between ruler and Flash ADC

2.4: Speed, Power, Accuracy trade-offs in ADCs

Note from Fig. 2-6 that the accuracy of the ADC is limited by the accuracy of the comparators, and reference values. Thus any offset or error in the comparators and reference voltages must be lower than the size of the least significant bit. For example, if the input has a maximum 1V signal swing, and 10-bit accuracy is required the total error must be less than $1V/2^{10} = 1V/1024 = 976\mu V$. The offset of a differential pair (which forms a simple comparator) consists of two key components: threshold voltage mismatch, and β mismatch ($\beta = \mu C_{ox} W/L$) [4]. Assuming the separation distance between the transistors is small, the offsets for a differential pair with width W and length L are given by Gaussian distributions, where the RMS values are given as

$$\sigma(\Delta V_t) = \frac{A_{V_t}}{\sqrt{WL}}, \quad (2.1)$$

$$\text{and } \sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_{\beta}}{\sqrt{WL}}, \quad (2.2)$$

where A_{V_t} , and A_{β} are process dependent values.

Typical values for the mismatch parameters are: $A_{Vt} = 5\text{mV}$, and $A_{\beta} = 1\%$, for a $0.18\mu\text{m}$ CMOS process. The input-referred RMS offset of the comparator is approximately given by

$$\sigma(\Delta V_{eff}) \approx \sqrt{\frac{1}{WL} \left[A_{Vt}^2 + \frac{A_{\beta}^2}{4} (V_{eff})^2 \right]} \quad [4] \quad (2.3)$$

where V_{eff} is the overdrive voltage of the transistor. The variation of comparator offset with gate overdrive (V_{eff}), and device sizing is shown in Fig. 2-7, where it is clear a higher precision, requires a larger WL product.

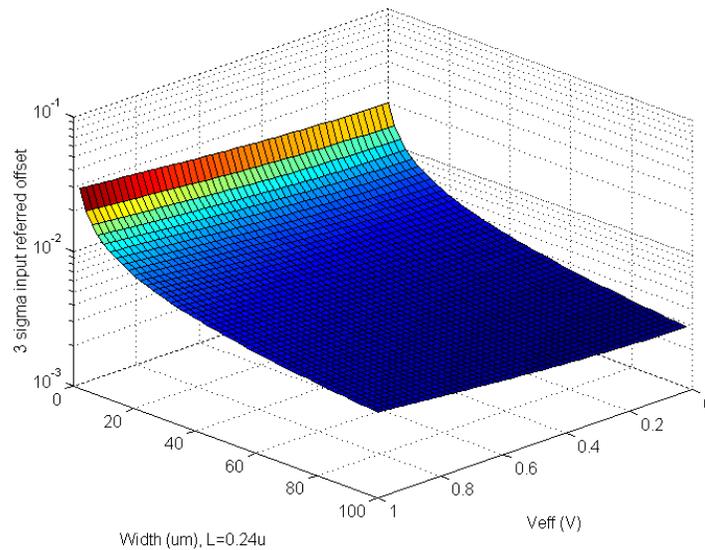


Fig. 2-7: Offset variation with V_{eff} and area

If 10-bit accuracy were required with a 1V signal swing, and 1V V_{eff} , for a successful yield of 99% (3σ of the random distribution), a W of over $1968\mu\text{m}$ would be required with $L=0.24\mu\text{m}$! Clearly the larger transistor area results in an increased parasitic gate/source/drain/bulk capacitance, requiring increased power to operate the comparator at a fixed speed. Thus a design tradeoff exists between speed, accuracy and power. Considering the gain-bandwidth of a differential pair, the speed of the differential pair to a first order [4] is given by

$$Speed \approx \frac{g_m}{2\pi C_{gs}} \approx \frac{2I}{2\pi WL(2/3)C_{ox}V_{eff}} \quad (2.4)$$

where square law relations are used, and drain-bulk capacitance ignored. Noting that $Power \approx I \cdot V_{DD}$, and defining accuracy [4] as

$$\frac{1}{Accuracy^2} \approx \frac{\sigma(\Delta V_{gs})}{V_{DD}^2} \approx \frac{A_{V_t}^2}{WL V_{DD}} \quad (2.5)$$

where β mismatch is ignored (from Fig. 2-7 offset is a weak function of V_{eff} , thus approximation is valid), the above equations are combined to yield the following relationship [4]:

$$\frac{Speed \times Accuracy^2}{Power} \approx \frac{1}{C_{ox} A_{V_t}^2} \quad (2.6)$$

Equation (2.6) is often used as a *Figure Of Merit* (FOM) for ADCs as it encapsulates three key performance metrics: speed, accuracy, and power, as well as their associated tradeoffs with respect to the associated technology. For example, if a designer has a fixed power and speed constraint, higher accuracy may only be achieved by migrating to a technology that has a smaller A_{V_t} and/or C_{ox} . FOMs also allow for easy comparisons between different ADC designs. (E.g.) if ADC ‘A’ reports twice the accuracy of ADC ‘B’, ‘A’ is expected to consume 4x the power of ‘B’. If ADC ‘C’ is twice as fast as ADC ‘D’, but ‘C’ consumes 3x more power than ‘D’, then ‘C’ is likely a poor design. (Assuming A, B, and C, D are in the same technology respectively).

Another popular FOM is

$$FOM = \frac{Power}{(2^{ENOB})(2f_{input-bandwidth})} (pJ/step) \quad (2.7)$$

where $2f_{input-bandwidth}$ is the sampling rate for Nyquist rate ADCs, f_s . This figure of merit is commonly used as the accuracy term is based on easily measured quantities, and calculates a value that has meaningful units (i.e. energy required per conversion step).

2.5: Alternative ADC architectures

Over the years different architectures optimal with respect to one or more of the performance metrics mentioned in section 2.4 have been developed. As a detailed overview of the most popular ADC architectures would require a lengthy discussion, only a table outlining the strengths of popular architectures is presented. The pipeline architecture however is discussed in detail, as it is the architecture used in this dissertation. A more detailed discussion of alternative ADC architectures can be found in [3].

Table 2-1: Comparison of ADC architectures

<i>ARCHITECTURE</i>	<i>LATENCY</i>	<i>SPEED</i>	<i>ACCURACY</i>	<i>AREA</i>
Flash	No	High	Low	High
Folding/Interpolating	No	Medium-High	Low-Medium	Medium-High
Delta-Sigma	Yes	Low	High	Medium
Successive Approximation (SAR)	Yes	Low	Medium-High	Low
Pipeline	Yes	Medium	Medium-High	Medium

2.6: Pipeline ADC – Architecture

In a Flash ADC, the digital outputs are realized almost immediately after the comparators are latched. The toll on the system is the number of comparators required is at least the number of unique outputs (e.g. 1023 for 10-bit accuracy). Recalling the accuracy-power tradeoff of section 2.4, a high accuracy implies high power consumption. Thus each of the 1023 comparators of a 10-bit flash would demand much power, making the total power of all 1023 comparators excessively large. If however the comparison operation is spread over several clock cycles, the number of comparators required per clock cycle can be significantly reduced. In Fig. 2-8, the comparison operation is spread over two clock phases in a two-stage Flash architecture. During the first clock phase the $N/2$ Most Significant Bits (MSBs) are resolved (where N is the number of bits in the final ADC output). During the second clock phase the resolved $N/2$ MSBs are removed from the input, the residue amplified to full scale (to maintain the dynamic range, and reuse reference voltages), and subsequently the remaining $N/2$ bits are resolved.

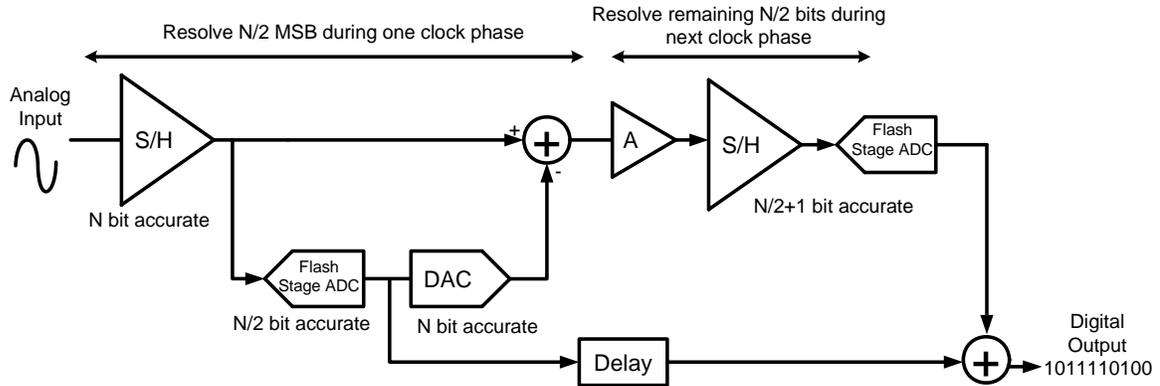


Fig. 2-8: Two stage N -bit accurate ADC

Thus the number of comparators required in the two-stage approach is $2^{N/2+1}$, which is lower than the Flash ADC for $N > 2$. Although speed is preserved by virtue of a queue structure, spreading the comparison operation over time comes at the penalty of increased conversion latency. Specifically, rather than the digital outputs being available one clock phase after the input is sampled as in the flash architecture, two clock phases are required for the two-step approach. Although the first stage of the two-stage approach resolves only the first $N/2$ MSBs, to allow for accurate resolution of the remaining $N/2$ LSBs, the *Digital to Analog Converter* (DAC), and subtraction blocks of the first stage must be precise to at least N -bits. The second sample and hold however requires only $N/2+1$ bits accuracy, thus has less stringent accuracy requirements. Section 2.7 introduces the concept of digital error correction to relax the requirements of the first stage ADC to $N/2$ bits.

The divide and conquer approach used in the two step ADC can be extended further, such that several clock phases are used, and only a few bits resolved per stage as illustrated in Fig. 2-9; this generalized approach forms the basis of a pipeline ADC [3].

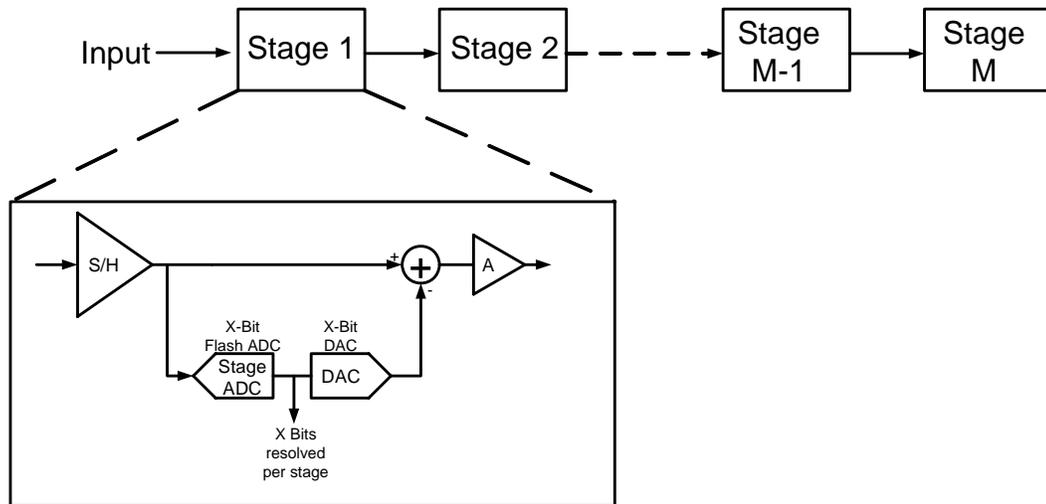


Fig. 2-9: Pipeline ADC architecture

Although several clock phases are required for an analog value to be digitized, a new digital output is available every clock phase. This is due to the sequential structure shown in Fig. 2-9, which by virtue of sample and holds in each stage, implements a queue or pipeline structure. Hence the throughput of the pipeline is limited by only the delay through a single stage [3]. Pipeline ADCs are useful in configurations where latency is not critical (e.g.) where the ADC is in an open loop signal path. For applications where latency is critical (e.g. where the ADC is in the critical path of a closed loop), one is restricted to using a Flash or variant ADC.

A design tradeoff which exists for pipeline ADCs is the choice between a larger number of bits resolved per stage (hence less latency, but more design complexity), or a fewer number of bits resolved per stage (hence increased latency, but simpler design). Although a proper discussion of which trade-off is superior is beyond the scope of this discussion, it is noted for high-speed applications with 10-bit accuracy, a longer pipeline with fewer bits/stage is preferred [5]. A longer pipeline allows for the implementation of fast switched-capacitor circuits with lower closed loop gains, thus smaller feedback factors (hence faster operation [3]), and a simple digital correction scheme to relax the precision requirements of the stage-ADCs [6].

The precision requirements of each pipeline stage decrease through the pipeline (i.e.) the first stage must be most precise, subsequent stages need only be as precise as the previous stage less the number of bits resolved previously. Thus analog design complexity can be reduced along the pipeline [7] as shown in Fig. 2-10 (less opamp gain and bandwidth for later stages – see section 3.4). Discussed in section 2.4, a relaxed precision implies a smaller area, thus lower power consumption. Hence it is possible to significantly reduce total power consumption by having many stages, where each subsequent stage in the pipeline is sized smaller than the previous stage.

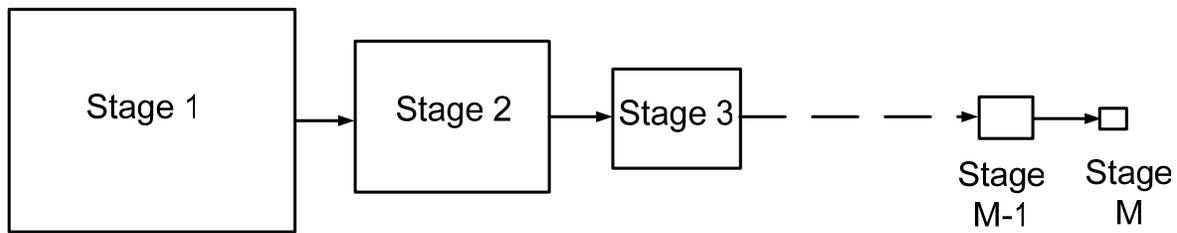


Fig. 2-10: Pipeline stage scaling – stages are sequentially smaller

2.7: Error correction – long division

The digitization of an analog signal in a pipeline ADC is very similar to the calculation of a quotient in long division, i.e.:

$$\begin{array}{r} \textit{Quotient} \\ \textit{Divisor} \overline{) \textit{Dividend}, \textit{remainder}} \end{array}$$

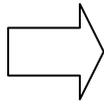
The divisor is similar to the analog input signal (relative to full scale), the dividend the full-scale voltage (i.e. the decimal representation of the largest 10-bit number - 1023), the quotient is the resolved digital output word, and the remainder the quantization error. By exploiting the long division structure of a pipeline ADC, the accuracy requirements of the stage ADC can be relaxed. Consider the long division of two numbers: x (divisor), and $y_n y_{n-1} y_{n-2} \dots y_1 y_0$ (dividend), in an arbitrary but common base β . Both x and y are of arbitrary length, where each digit of y is explicitly shown by the subscripts (most significant digit of y is y_n , least significant digit is y_1). Thus a correct long division of y by x is as follows:

$$\begin{array}{r}
\alpha_n \alpha_{n-1} \dots \alpha_1 \\
x \overline{) y_n y_{n-1} \dots y_1} \\
\underline{- x \alpha_n} \\
(y_n - x \alpha_n) \beta + y_{n-1} \\
\underline{- x \alpha_{n-1}} \\
r_1
\end{array}$$

* r_1 is the remainder after two lines of division

If however the divisor, x , is incorrectly divided into the dividend, y , an incorrect remainder results, yielding every subsequent digit in the quotient incorrect. This situation is analogous to a pipeline ADC where in a pipeline stage a comparator in the stage Flash ADC, due to an offset, incorrectly sets the stage DAC, leading to an incorrect value being subtracted from the stage input. An important observation is in long division the error is passed to the subsequent line of long division. Thus if a division error could be identified, the error could be eliminated in the subsequent line of long division by adjusting the quotient.

$$\begin{array}{r}
\alpha'_n \alpha'_{n-1} \dots \alpha'_1 \\
x \overline{) y_n y_{n-1} \dots y_1} \\
\underline{- x \alpha'_n} \\
(y_n - x \alpha'_n) \beta + y_{n-1} \\
\underline{- x \alpha'_{n-1}} \\
r_2
\end{array}$$



Thus if an incorrect division is made, such that α'_n is an incorrect digit in the quotient, the error can be eliminated by selecting α'_{n-1} such that $r_2=r_1$

Since the correct and corrected long division approaches yield the same remainder, the quotients in each approach are equal; despite the fact the latter approach included a division error.

The following example numerically illustrates the concepts discussed [8]:

Correct division example

Error in division, with correction example

	<u>7.142857</u>
	7)50.000000
subtracted reference	<u>- 49</u>
residue	1
amplified residue	10
subtracted reference	<u>- 7</u>
residue	3
amplified residue	30
subtracted reference	<u>- 28</u>
residue	2
amplified residue	20
subtracted reference	<u>- 14</u>
residue	6
amplified residue	60
subtracted reference	<u>- 56</u>
residue	4
amplified residue	40
subtracted reference	<u>- 35</u>
residue	5
amplified residue	50
subtracted reference	<u>- 49</u>
residue	1

	<u>7.143(-2)57</u>
	7)50.000000
subtracted reference	<u>- 49</u>
residue	1
amplified residue	10
subtracted reference	<u>- 7</u>
residue	3
amplified residue	30
subtracted reference	<u>- 28</u>
residue	2
amplified residue	20
subtracted reference	<u>- 21</u> ← error
residue	-1
amplified residue	-10
subtracted reference	<u>+14</u>
residue	4
amplified residue	40
subtracted reference	<u>- 35</u>
residue	5
amplified residue	50
subtracted reference	<u>- 49</u>
residue	1

** Note how error is allowed to pass on to subsequent line of division, and how error is corrected in subsequent line of division*

Correct division quotient:

$$7 \times 10^0 + 1 \times 10^{-1} + 4 \times 10^{-2} + 2 \times 10^{-3} + 8 \times 10^{-4} + 5 \times 10^{-5} + 7 \times 10^{-6} = 7.142857$$

Incorrect division with corrected quotient:

$$7 \times 10^0 + 1 \times 10^{-1} + 4 \times 10^{-2} + 3 \times 10^{-3} + (-2) \times 10^{-4} + 5 \times 10^{-5} + 7 \times 10^{-6} = 7.142857$$

2.7.2: Digital Error correction in pipeline ADCs using 1.5 bits/stage

From section 2.7, it is clear a finite error in long division can be tolerated so long as the error passes to the subsequent line of long division, and the occurrence of an error can be detected. Thus to apply the same error correction principle to a pipeline ADC, errors caused by

comparator offsets must be passed to the subsequent pipeline stage, and a logic implemented to recognize the occurrence of an error.

A simple pipeline topology is one that resolves two bits per stage as shown in Fig. 2-11, the transfer function of which is shown in Fig. 2-12.

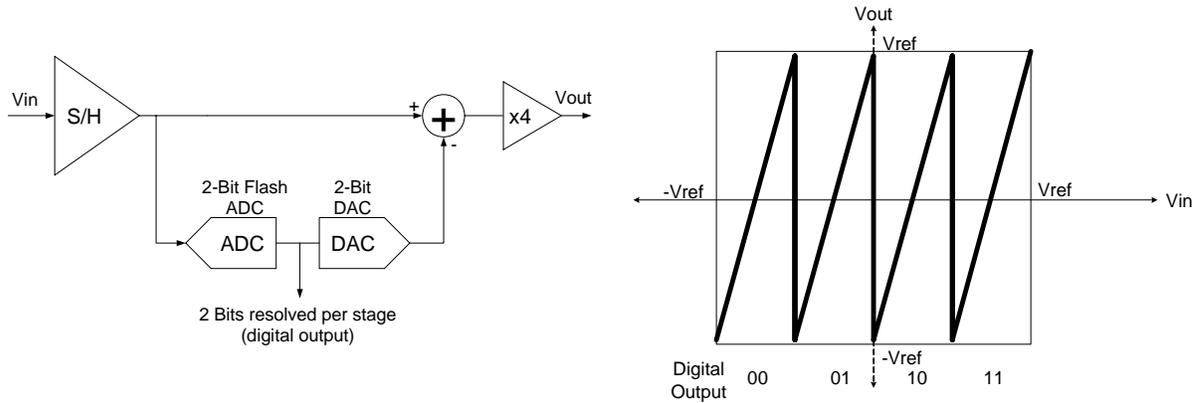


Fig. 2-11: Pipeline Stage detail

Fig. 2-12: Stage transfer function

The stage gain is 4x to maximize the dynamic range of the subsequent stage, and to allow for reuse of the reference voltages. An error in the stage ADC threshold (due to an offset) alters the transfer function as shown in Fig. 2-13.

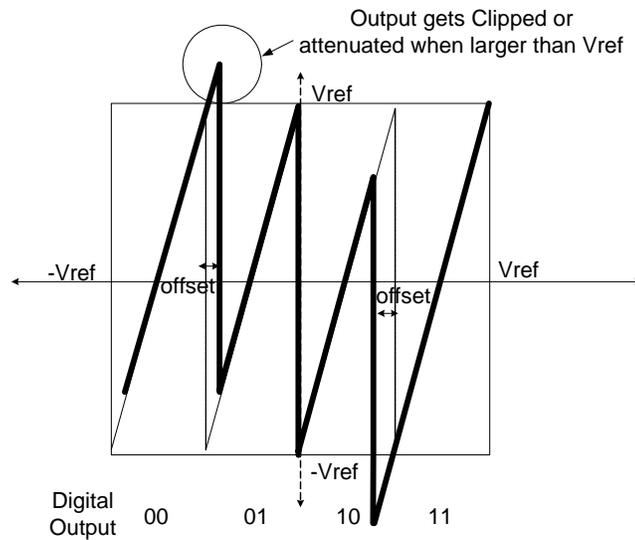


Fig. 2-13: Over-range error with pipeline stage

Thus threshold errors lead to stage outputs that exceed the full-scale input to the subsequent stage. As stage inputs that exceed full scale are attenuated or clipped, offset induced errors do not pass to the subsequent stage unaltered, and thus cannot be completely eliminated as described in section 2.7.2. If however the stage gain is reduced to $2x$ as shown in Fig. 2-14., the error is fully passed on to the subsequent stage, so long as the offset error does not exceed $V_{ref}/4$, as shown in Fig. 2-15.

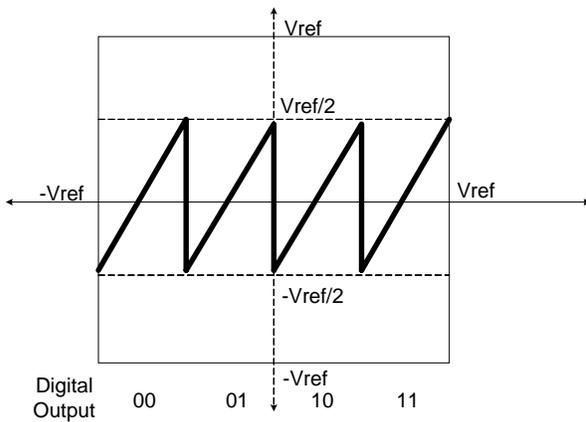


Fig. 2-14: Reduced gain stage transfer function

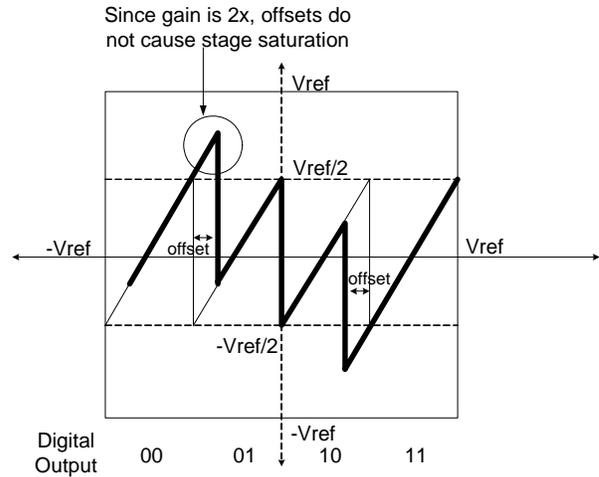


Fig. 2-15: Impact of errors on stage transfer function

Hence if the subsequent stage detects an over-range error, the error may be digitally eliminated by adding or subtracting a bit from the digital output (depending on whether the error was an over or under range error). Non-trivial digital subtraction is avoided by altering the transfer function of Fig. 2-14 by adding a $V_{ref}/4$ offset [5] as shown in Fig. 2-16:

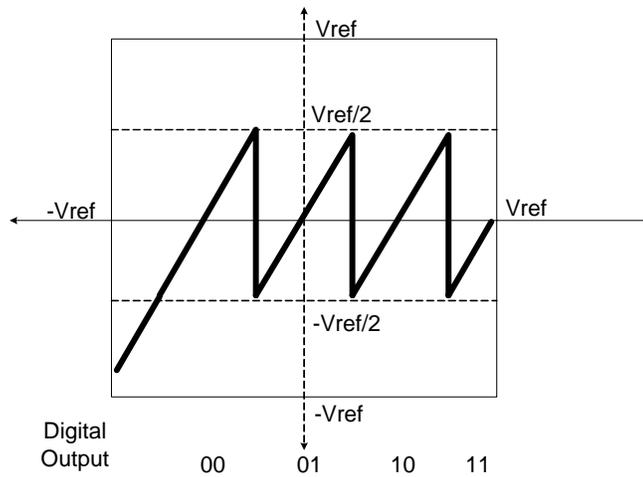


Fig. 2-16: $V_{ref}/4$ offset to eliminate digital subtraction

For error correction, each stage is required to only determine if an over/under range error has occurred, thus the comparator at $\frac{3}{4}V_{ref}$ can be eliminated, yielding the final transfer function shown in Fig. 2-17

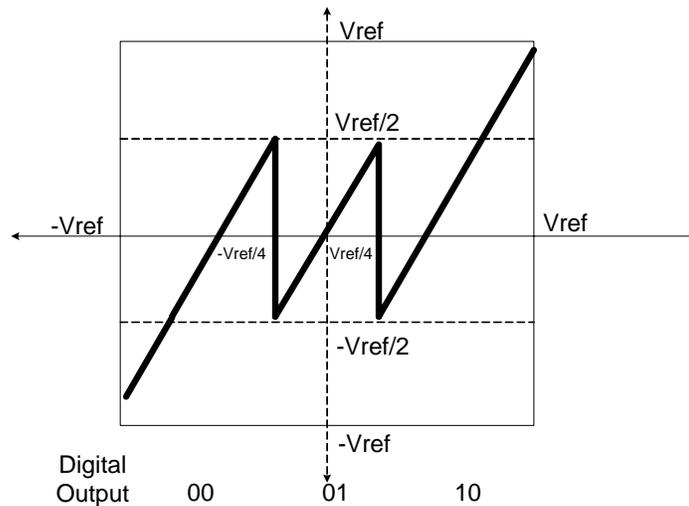


Fig. 2-17: 1.5bit/stage transfer function

With three unique digital outputs, the final transfer function is referred to as a 1.5 bit/stage architecture.

10-bits can be resolved using 1.5 bits/stage with eight such stages, followed by a 2-bit flash stage to resolve the final two bits (error correction cannot be used on the last stage since there

is no subsequent stage to correct the error – note the 2-bit flash has thresholds at $-V_{ref}/2$, 0 , $+V_{ref}/2$). The final 10-bit output code can be realized by digitally combining the outputs from each stage as described in [5]. A 1.5-bit/stage 10-bit pipeline ADC was the architecture used in the ADC of this dissertation. Fig. 2-18 illustrates the configuration of pipeline stages to yield a 10-bit output.

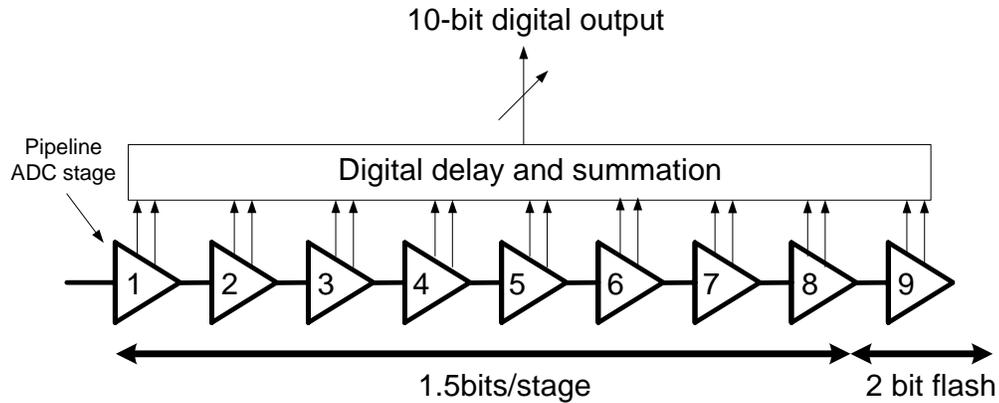


Fig. 2-18: 10-bit pipeline ADC using 1.5 bits/stage

2.8: Summary

This chapter discussed the fundamental differences between analog and digital signals, where the noise resilience of digital signaling was shown to be superior over analog signaling. Digital signal recovery in non-ideal channels was shown to require digital signal processing, where noise sources were shown to necessitate ADCs in the signal path. A brief review of Flash ADCs was given where various ADC tradeoffs between speed, power, and accuracy motivated the use of alternative ADC topologies. The pipeline ADC was detailed at a system level, including digital error correction, for a 1.5 bits/stage pipeline ADC.

CHAPTER THREE

Pipeline ADC Design

3.1: Overview

This chapter discusses circuit implementations and related design issues for 1.5 bit/stage pipeline ADCs. The key sub-blocks discussed are: the stage MDAC, the stage ADC, and the stage amplifier. The chapter concludes with a brief survey of recent 10-bit ADCs and their respective figure-of-merits.

3.2: Multiplying Digital-to-Analog Converter (MDAC)

As pipeline stages operate on discrete time signals (since each stage has a sample and hold), switched capacitor circuits are used for pipeline ADCs. With switch capacitor circuits it is possible to perform highly accurate mathematical operations such as addition, subtraction, and multiplication (by a constant), due to the availability of capacitors with a high degree of relative matching. Switch capacitor circuits also facilitate multiple, simultaneous signal manipulations with relatively simple architectures. It is possible to combine the functions of sample and hold, subtraction, DAC, and gain into a single switched capacitor circuit, referred to as the *Multiplying Digital-to-Analog Converter* (MDAC) as shown in Fig. 3-1.

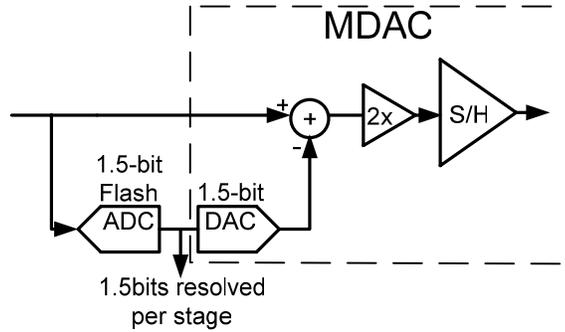


Fig. 3-1: MDAC functionality in dashes

Fig. 3-2 shows a single ended circuit implementation of the MDAC of Fig. 3-1, using a switched capacitor approach.

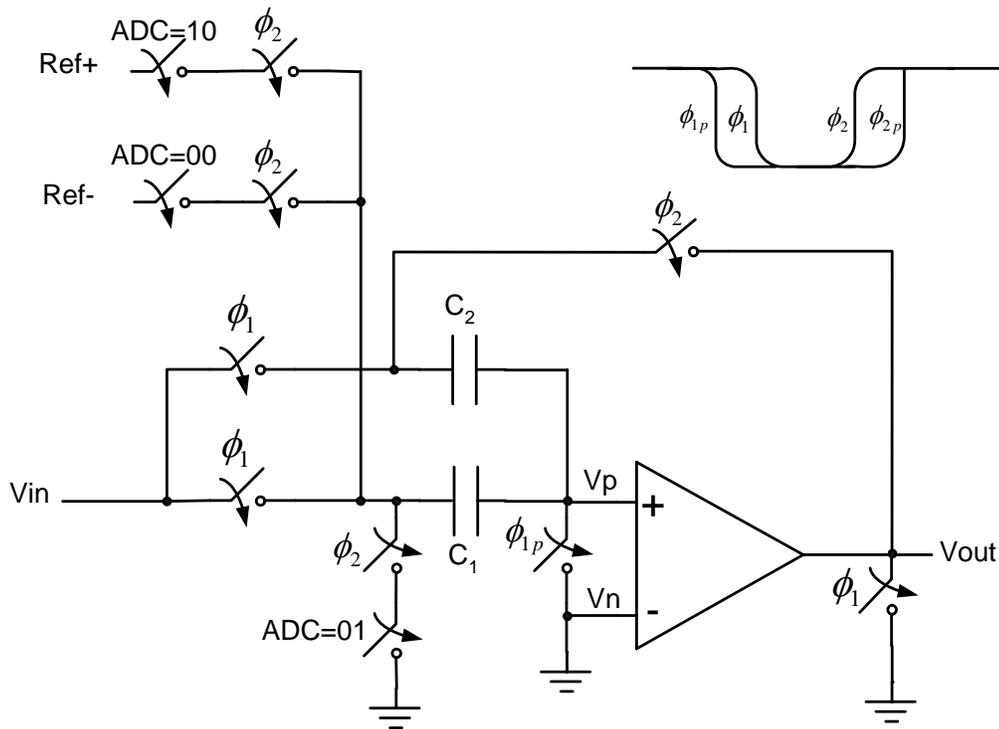


Fig. 3-2: stage MDAC

The MDAC of Fig. 3-2 is shown single ended for simplicity, although in practice fully differential circuitry is commonly used to suppress common-mode noise [9]. As described in section 2.7.2, a 1.5 bits/stage architecture has one of three digital outputs, thus the DAC has three operating modes according to Fig. 2-17:

ADC output = 01: No over range error (stage input is between $-V_{ref}/4$ and $V_{ref}/4$).

During ϕ_1 : $Q_{C1}=C_1V_{in}$, $Q_{C2}=C_2V_{in}$

During ϕ_2 : C_1 is discharged, thus by charge conservation: $C_1V_{in} + C_2V_{in} = C_2V_{out}$

(noting negative feedback forces node V_p to a virtual ground). Thus

$$V_{out} = \frac{C_1 + C_2}{C_2} V_{in} \rightarrow \text{if } C_1=C_2, \text{ then: } V_{out}=2V_{in} \quad (3.1)$$

ADC output = 10: Over range error – Input exceeds $V_{ref}/4$, thus subtract $V_{ref}/2$ from input

During ϕ_1 : $Q_{C1}=C_1V_{in}$, $Q_{C2}=C_2V_{in}$

During ϕ_2 : C_1 is charged to V_{ref} , thus by charge conservation

$$C_1V_{in} + C_2V_{in} = C_1V_{ref} + C_2V_{out}$$

$$\therefore V_{out} = \frac{C_1 + C_2}{C_2} V_{in} - \frac{C_1}{C_2} V_{ref} \rightarrow \text{if } C_1=C_2, \text{ then: } V_{out}=2V_{in}-V_{ref}=2(V_{in}-V_{ref}/2) \quad (3.2)$$

ADC output = 00: Under range error – Input below $-V_{ref}/4$, thus add $V_{ref}/2$ to input

During ϕ_1 : $Q_{C1}=C_1V_{in}$, $Q_{C2}=C_2V_{in}$

During ϕ_2 : C_1 is charged to $-V_{ref}$, thus by charge conservation

$$C_1V_{in} + C_2V_{in} = C_1(-V_{ref}) + C_2V_{out}$$

$$\therefore V_{out} = \frac{C_1 + C_2}{C_2} V_{in} + \frac{C_1}{C_2} V_{ref} \rightarrow \text{if } C_1=C_2, \text{ then: } V_{out}=2V_{in}+V_{ref}=2(V_{in}+V_{ref}/2) \quad (3.3)$$

Thus the switched capacitor circuit implements the stage sample-and-hold, stage gain, DAC, and subtraction blocks.

Signal dependent charge injection is minimized by using bottom plate sampling, where the use of an advanced clock ϕ_{1p} , makes charge injection signal independent [10]. A non-overlapping clock generator is thus required for the MDAC.

3.3: MDAC design considerations - Capacitor matching/linearity

From equations (3.1)-(3.3) it is clear stage gain is determined by the ratio of capacitors C_1 and C_2 . Thus to ensure a gain which is at least 10-bit accurate, C_1 and C_2 must match to at least 10-bit accuracy or within 0.1% for the first stage in the pipeline. To obtain at least 0.1% matching a high quality capacitor such as a *Metal-Insulator-Metal* (MIM) capacitor must be used. If properly designed in layout, MIM capacitors can achieve matching between 0.01-0.1% [11]. MIM capacitors however are often unavailable in purely digital processes, necessitating alternative capacitor structures. Alternatively metal-finger capacitors, which derive their capacitance from the combination of area and fringe capacitance between overlapping metal layers can be used in digital processes to achieve sub 0.1% matching. Metal-finger capacitors however can have large absolute variation (>20%), thus require a conservative design approach. Alternatively a digital calibration algorithm can be employed to significantly minimize mismatch-induced gain errors (and finite opamp gain errors) [12], [13], [14], [15]. Due to additional design complexity, calibration schemes are beyond the focus of this dissertation. We note however that calibration techniques are emerging as essential approaches for high-resolution pipeline ADCs due to the relaxed accuracy constraints afforded.

In addition to capacitor matching, it is essential the ratio of capacitors C_1 and C_2 be linear for the desired input range to minimize harmonic distortion. Thus non-linear parasitic gate capacitance (MOS-caps), or other active capacitors should be avoided for C_1 and C_2 in high precision pipeline ADCs. Passive MIM, and metal-finger capacitors are linear well beyond the 10-bit level, thus are typically used.

The MDAC shown in Fig. 3-2 is a popular MDAC architecture, as the capacitor sizes of C_1 and C_2 are equal. Since $C_1=C_2$, identical layouts can be used for C_1 and C_2 - maximizing layout symmetry and hence maximizing accuracy. As MIM capacitors only have a marginal matching for 10-bit accuracy, a high degree of capacitor matching is essential to minimize INL/DNL errors. Another advantage of the architecture of Fig. 3-2 is a high beta value (feedback factor), which maximizes the bandwidth of the closed loop system [16].

3.3.2: MDAC design considerations - Thermal noise

Although capacitors are ideally noiseless elements, in a sampled system, sample and hold capacitors capture noise generated by noisy elements such as switch resistors, opamps, etc. Consider the following noise analysis of a capacitor sampling resistor noise as shown in Fig. 3-3:

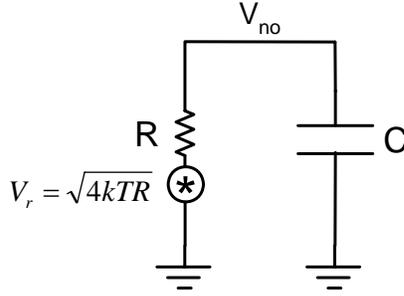


Fig. 3-3: RC noise model

from [3] it is shown equivalent noise bandwidth is $\frac{\pi}{2} f_0$,

$$\begin{aligned} \therefore V_{no-RMS}^2 &= \frac{\pi}{2} f_0 V_R^2(f) \quad [3] \\ \therefore f_0 &= \frac{1}{2\pi RC} \rightarrow V_{no-RMS}^2 = \frac{kT}{C} \end{aligned} \quad (3.4)$$

From the above example it is clear increasing the size of the sampling capacitor reduces the power of thermal noise. As thermal noise represents a dynamic noise source that reduces ADC SNR, a minimum capacitance (i.e. C_1 , C_2) must be driven to ensure a sufficient accuracy – thus thermal noise imposes a tradeoff between power and accuracy. For the MDAC of Fig. 3-2, the effective input referred thermal noise, which includes switch, and opamp noise is derived in [17] and found to be

$$\sigma_T^2 = \frac{kT(C_1 + C_2 + C_{opamp})}{(C_1 + C_2)^2} + \frac{2}{3} kT \frac{1}{\beta} \frac{1}{C_{LT}} \left(\frac{C_1}{C_1 + C_2} \right) \quad (3.5)$$

where $C_{LT} = C_2 + \beta(C_1 + C_{opamp})$ is the equivalent output load capacitance, and C_{opamp} the input capacitance to the opamp. The relationship between SNR and minimum capacitor size for a full scale signal swing of 0.8V, and $C_1=C_2=C_{opamp}=0.5\text{pF}$ is shown in Fig. 3-4.

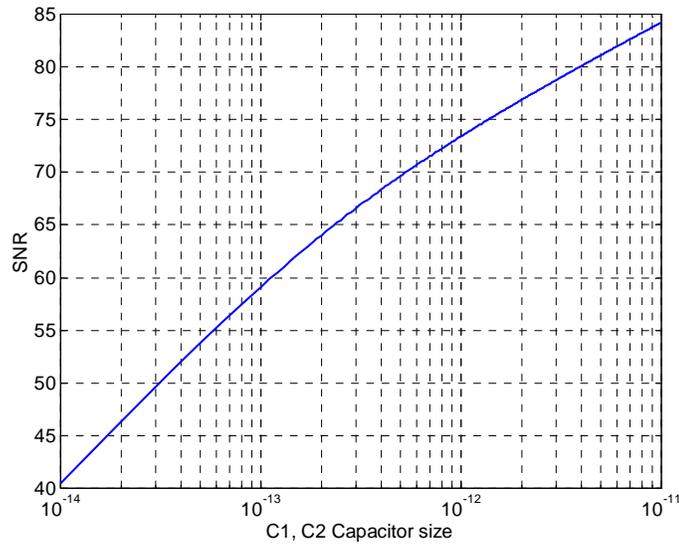


Fig. 3-4: Variation of SNR due to thermal noise (ignoring quantization error, full scale=0.8V, $C_1=C_2=C_{opamp}=0.5pF$)

From Fig. 3-4 it is clear thermal noise can alone limit accuracy to less than 10-bits (SNR=62dB) if capacitors are not sufficiently sized. As thermal noise represents only one of several precision limiting factors (others include: quantization noise, power supply noise, capacitor mismatch, etc.), it is desirable to place the noise floor beyond the 10-bit level (e.g.) for thermal noise less than 1/4 LSB \rightarrow thermal noise floor should be at least -72dB. Note from section 2.6, the stage accuracy requirements are relaxed for subsequent pipeline stages. Thus it is possible to increase the noise floor for subsequent stages by using smaller capacitors - maximizing opamp bandwidth and minimizing overall power.

3.3.3: MDAC design considerations - Switch sizing

When sizing a MOS switch two key issues should be considered: 1.) The desired RC time constant, and 2.) The maximum distortion tolerable through the switch.

As switched-capacitor circuits have a finite time to settle, it is essential the switches be sized large enough such that the sampled signal settle to the desired accuracy in the allotted time.

Since $r_{ds} = (\mu C_{ox} W L^{-1} V_{eff})^{-1}$, switch resistance can be minimized by increasing the MOS

switch W/L ratio. However an increased W/L ratio implies a larger area, which imparts a larger parasitic capacitance to the circuit. As described in [3], a sufficiently large parasitic capacitance can alter charge-sharing equations, and introduce harmonic distortion through charge injection. Thus switch transistors must be carefully sized, where switches should be large enough to ensure a sufficient RC time constant, but small enough to minimize parasitic induced errors.

A consequence of the switch's resistance dependency on V_{eff} is an RC time constant that is signal dependent, hence non-linear. A non-linear RC time constant can lead to significant distortion if the switch passes a continuous time signal, as is the case in front-end sample and hold inputs. Signal-dependent RC time constants also affect discrete time signals, as the MOS switch must be sized sufficiently such that the worst-case RC time constant (i.e. when V_{eff} is smallest) is sufficient for the desired sampling speed. Non-linear RC time constants can be significantly minimized however using a bootstrapping approach [10], which maintains a constant and maximal V_{eff} , thereby minimizing signal dependent variations.

3.4: Opamp design - Gain requirement

The charge transfer relations derived in equations (3.1)–(3.3) were based on the assumption of a perfect virtual ground at node V_p in Fig. 3-2, which only occurs when the opamp gain is infinite. In practice opamp gain is finite - introducing an error into the charge balance equations. As such opamp gain must be made sufficiently large to minimize finite gain error.

Consider the closed loop gain of a negative feedback system $H(s)$, as shown in Fig. 3-5:

$$H(s) = \frac{Y(s)}{X(s)} = \frac{A(s)}{1 + A(s)\beta} \quad (3.6)$$

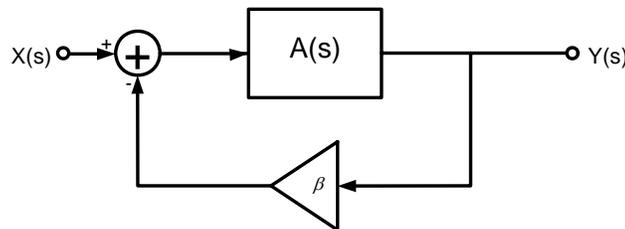


Fig. 3-5: basic linear feedback structure

Ideally as $A(s)$ tends to infinity, $H(s) \rightarrow 1/\beta$. Thus the relative error (Δ) is

$$\Delta = \frac{\frac{1}{\beta} - \frac{A(s)}{1 + A(s)\beta}}{\frac{1}{\beta}} \quad (3.7)$$

As switch capacitor circuits settle to DC values, DC gain affects charge transfer equations:

$$\therefore A > \frac{\frac{1}{\Delta} - 1}{\beta} \approx \frac{1}{\Delta\beta} \quad (3.8)$$

Hence for an error due to finite opamp gain to be less than $\frac{1}{4}$ LSB, i.e. $1/(4 \times 1024) = 1/4096$, with $\beta = 0.5$ implies $A > 8192$, or $A > 78\text{dB}$. Fig. 3-6 illustrates the variation of relative error with opamp gain.

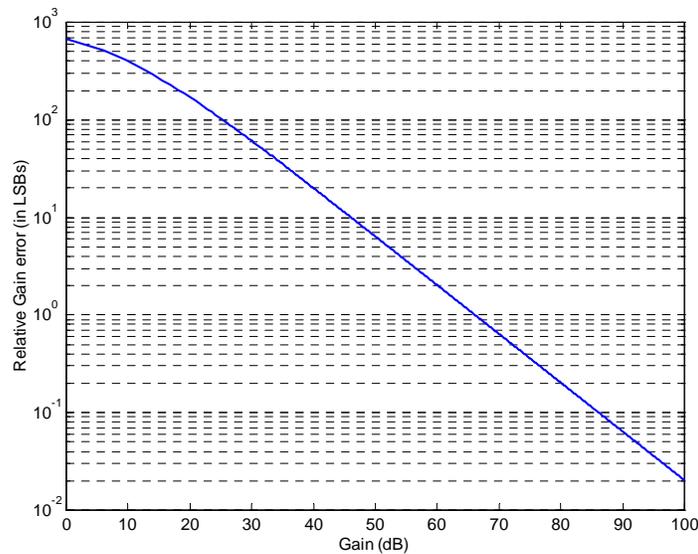


Fig. 3-6: gain error variation with opamp gain

Attaining 78dB of DC gain while maintaining a reasonable bandwidth is near impossible with a simple single stage configuration (e.g. differential pair) for sub-micron technologies. Thus two-stage or gain-booster configurations are necessitated for 10-bit pipeline ADCs (a detailed description of high gain opamps is given in [3], [18]). From section 2.6 it is noted that stage accuracy requirements decrease along the pipeline, thus latter stages may have less gain, allowing for simpler opamps (single stage, or no gain-boosting), thus reducing power.

It should be noted that alternative MDAC architectures exist which employ gain-error cancellation methods, facilitating much lower opamp gains [12], [13], [14], [15] than those required by (3.8). Such approaches however introduce a design overhead, and increase design time, thus are not considered in this dissertation.

3.4.2: Opamp design - Bandwidth requirement

Switched capacitor circuits have a finite time in which to settle, thus to ensure a minimum settling accuracy, opamp bandwidth must be optimized. If the opamp is modeled as a first order system, the opamp transfer function near the unity gain frequency is given

by: $A(s) = \frac{\omega_{ta}}{s}$ [3]. Thus the MDAC step response, during ϕ_2 is given by

$$H(s) \bullet \frac{1}{s} = \frac{A(s)}{1 + A(s)\beta} \bullet \frac{1}{s} = \frac{\frac{\omega_{ta}}{s}}{1 + \frac{\omega_{ta}}{s}\beta} \bullet \frac{1}{s} = \frac{\omega_{ta}}{s + \omega_{ta}\beta} \bullet \frac{1}{s} = \frac{1}{\beta} \left[\frac{1}{1 + \frac{s}{\omega_{ta}\beta}} \right] \bullet \frac{1}{s} \quad (3.9)$$

$$\therefore h_{step}(t) = \frac{1}{\beta} (1 - e^{-\frac{t}{\tau}})$$

where $\tau = \frac{1}{\omega_{ta}\beta}$, and slew rate is ignored. Since $e^{-\frac{t}{\tau}} = 2^{-x}$, where x is the settling accuracy

in bits, the available time to settle is

$$t = x \left(\frac{1}{\omega_{ta}\beta} \right) \ln 2 \quad (3.10)$$

As the available time t to settle is half the clock period, $t = \frac{1}{2f_s}$

$$\therefore f_u = \frac{x \ln 2 f_s}{\pi \beta}, \quad (3.11)$$

$$f_s = \frac{f_u \pi \beta}{x \ln 2} \quad (3.12)$$

where for settling within $\frac{1}{4}$ LSB, $x = 12$ for a 10-bit ADC. Figure Fig. 3-7 graphically illustrates the required opamp unity gain bandwidth to achieve a desired sampling rate and settling accuracy.

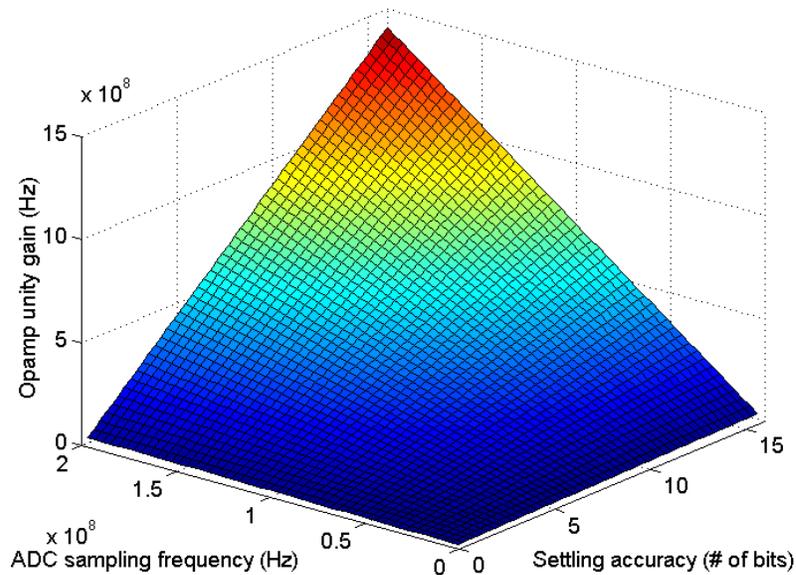


Fig. 3-7: required opamp unity gain frequency versus sampling frequency and settling accuracy

From Fig. 3-7 and equations (3.11)-(3.12), a unity gain frequency much larger than sampling frequency is required to obtain high accuracy settling. Since the MDAC opamps must drive large capacitive loads (to minimize thermal noise), much power is consumed by the opamps. As such, the power consumption of opamps in a pipeline ADC often consumes 60-80% of the total ADC power. It is noted from section 2.6 however, the accuracy requirements decrease along the pipeline, thus the unity gain frequency of subsequent stages along the pipeline can be reduced, minimizing total power [7].

3.5: Stage ADC design - Comparator

A flash architecture is commonly used for the stage ADCs, due to low accuracy required by the stage ADCs. As described in section 2.3, flash ADCs consist of comparators at the various thresholds of the ADC. For a 1.5-bit/stage pipeline architecture stage flash ADCs require comparators at thresholds of $\pm V_{ref}/4$ and 0. It was shown in section 2.7.2 that digital error correction could be used to relax the tolerable offset on stage-ADC comparators (up to $\pm V_{ref}/4$). For $V_{ref}=0.8V$, the comparator offset can be as high as 200mV, which allows for minimum size devices in the comparator (hence minimizing parasitic capacitance, thus minimizing power). The relaxed offset constrains also afford simpler dynamic comparator architectures, which do not require pre-amp gain stages, or static comparators (e.g.: as used in 6-bit flash ADCs [19], [20]). Like digital logic, dynamic comparators only consume power on clock edges according to fCV^2 thus have a power that scales linearly with sampling frequency. For pipeline ADCs one of two dynamic comparators are typically used [21]: the Lewis and Gray comparator [22] (Fig. 3-8), or the charge-distribution comparator (Fig. 3-9).

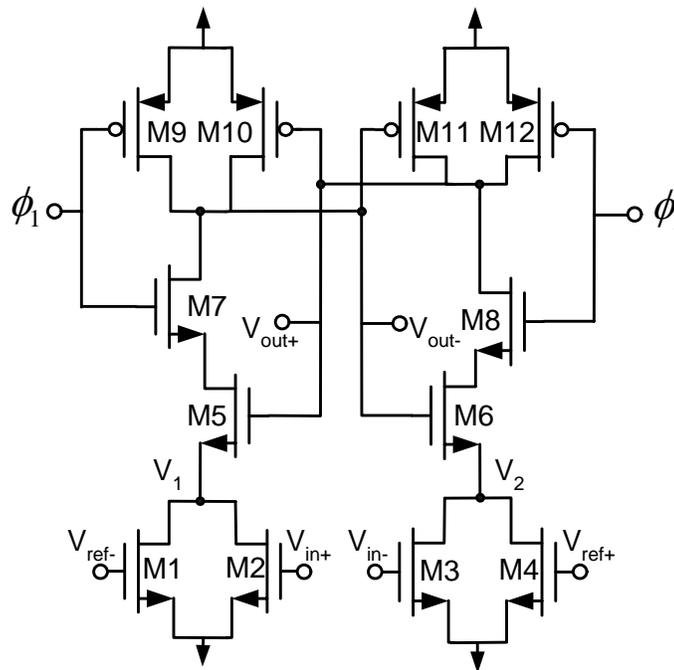


Fig. 3-8: Lewis and Gray comparator

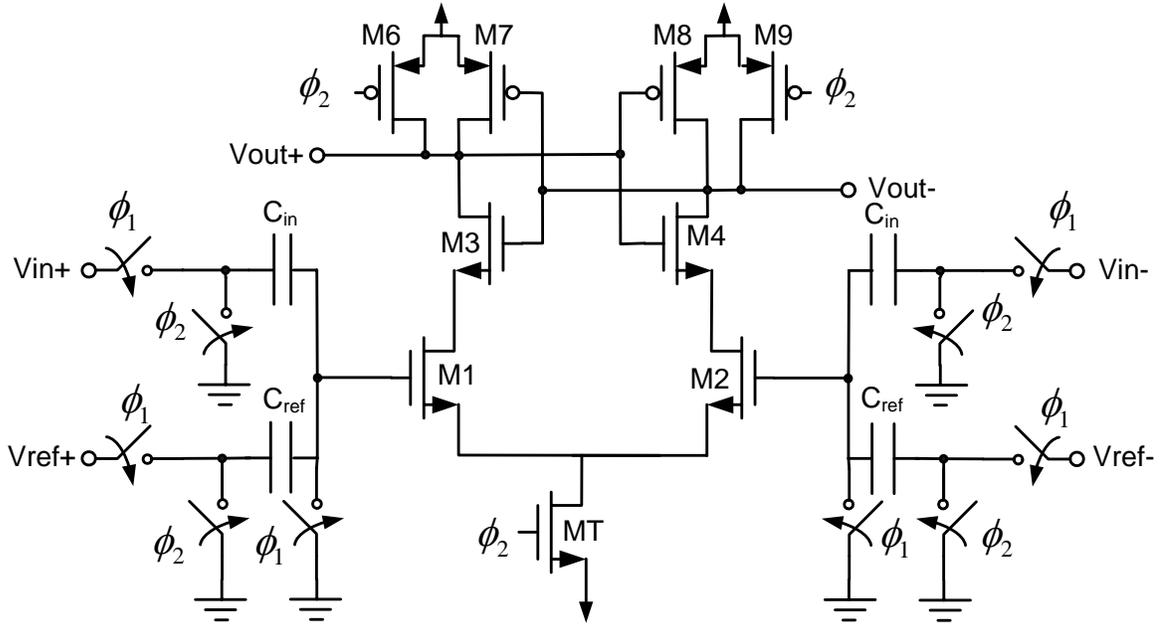


Fig. 3-9: switched capacitor/charge distribution comparator

The Lewis and Gray comparator compares two fully differential signals $V_{in+} - V_{in-}$, and $V_{ref+} - V_{ref-}$ (Fully differential comparators are highly desirable to reduce common-mode noise which can be large in digital environments). From section 2.7.2 comparators at $V_{ref}/4$ and $-V_{ref}/4$ are required to implement the 1.5bit/stage architecture, and comparators at $V_{ref}/2$, and $-V_{ref}/2$ for the 2-bit flash at the end of the pipeline. Rather than supply multiple reference voltages for each unique threshold, it is possible using the architecture of Fig. 3-8 to derive an arbitrary threshold by appropriate device sizing. Transistors M1-M4 operate in triode while the remaining transistors implement positive feedback to resolve the differential input [17]. The equivalent triode conductance of M1 and M2 from Fig. 3-8 are:

$$G_1 = \frac{1}{r_{ds-M1} \parallel r_{ds-M2}} = \mu C_{ox} \left[\frac{W_1}{L} (V_{ref-} - V_t) + \frac{W_2}{L} (V_{in+} - V_t) \right] \quad (3.13)$$

$$G_2 = \frac{1}{r_{ds-M3} \parallel r_{ds-M4}} = \mu C_{ox} \left[\frac{W_4}{L} (V_{ref+} - V_t) + \frac{W_3}{L} (V_{in-} - V_t) \right] \quad (3.14)$$

The comparator threshold occurs when the circuit is perfectly symmetric, i.e. when $G_1=G_2$, thus if $W_1=W_4$, and $W_2=W_3$

$$V_{in} |_{threshold} = \frac{W_1}{W_2} V_{ref} \quad (3.15)$$

where $V_{in} = V_{in+} - V_{in-}$, and $V_{ref} = V_{ref+} - V_{ref-}$.

Thus it is possible to achieve thresholds at $\pm V_{ref}/4$, and $\pm V_{ref}/2$ by providing a common differential reference voltage to each comparator in the pipeline, but sizing each comparator to yield the desired threshold (e.g.: $W_2 = 4W_1$ for a threshold of $V_{ref}/4$, $W_2 = 2W_1$ for a threshold of $V_{ref}/2$, etc.). As the comparator is fully differential, thresholds at $-V_{ref}/4$ and $-V_{ref}/2$ can be realized by reversing the polarity to the reference voltage. Thus all required thresholds for a 1.5 bit/stage pipeline can be realized by only supplying only one fully differential reference potential to the chip.

A drawback of the Lewis and Gray comparator is the threshold is a significant function of device symmetry. As the value resolved by the comparator operates by comparing the integral of the ratio of current to node capacitance at nodes V_1 and V_2 , circuit symmetry is crucial to reduce offset. Thus the layout of the Lewis and Gray comparator requires great care, and parasitic extraction for full characterization of input-referred offset. In [21] the Lewis and Gray comparator is shown to have an offset of $>200\text{mV}$ for a $0.35\mu\text{m}$ CMOS process,

Alternatively a charge distribution approach can be used to achieve a lower offset at the cost of increased power. As shown in Fig. 3-9, the charge distribution approach uses charge conservation to derive a comparator threshold, which depends on the ratio of capacitors rather than the ratio of device widths and parasitic capacitances. Using a two-phase clock (ϕ_1, ϕ_2), capacitors C_{in} and C_{ref} are charged to $V_{in+} - V_{in-}$ and $V_{ref+} - V_{ref-}$ respectively (in a differential sense) on the first clock phase. The charge is forced to redistribute between both capacitors during the second clock phase, where according to charge conservation the effective threshold of the comparator is found to be [21]

$$\frac{C_{ref}}{C_{in}}(V_{inp} - V_{inn}) \quad (3.16)$$

As the threshold is primarily a function of passive components and largely independent of parasitic capacitance, a lower offset can be achieved using the charge-distribution comparator. An analysis in [21] compares fabricated implementations (in 0.35 μ m CMOS) of the Lewis and Gray, and charge distribution comparators, where the following silicon measured results were obtained:

Table 3-1: Comparison of comparator area, offset, and power

<i>Comparator</i>	<i>Area</i>	<i>Power @ 100Msps</i>	<i>V_{offset-max}</i>
Lewis and Grey	1200 μ m	0.32mW	290mV
Charge distribution	2800 μ m	0.81mW	75mV

As other offsets besides device mismatch (e.g. noise) affect the stage transfer function, it is desirable to keep comparator offsets below $V_{ref}/4$. It should be noted the reduced offset of the charge distribution comparator comes at the cost of increased power (due to the dynamic charging of the sampling capacitors, and switches) and area. Thus the choice of which comparator architecture to use requires a tradeoff between tolerable offset, desired power consumption and area.

3.6: Survey of recently published 10-bit ADCs

A brief survey of recently published 10-bit ADCs (2000-2004) [9], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], is presented in Table 3-2, and in graphical form in Fig. 3-10 to Fig. 3-12. As a discussion of the approaches used in each publication would be prohibitively long, this section takes note of the key performance metrics for this dissertation, namely power, accuracy and speed in a tabular and graphical summary. The goal hence is to provide a basis upon which the power scaleable pipeline ADC of this dissertation can be compared against to show its merit.

Table 3-2: Survey of recently published (2000-2004) 10-bit pipeline ADCs

Published reports								
Author	ref.	Year	Speed (MSPs)	Power (mW)	SNDR (dB)	ENOB bits	FOM (pJ/step)	Power/MSPs mW/MSPs
J. Park et al	[31]	2000	0.5	1	56.1	9.0	3.8	2.0
Chang et al	[27]	2003	25	21	48.0	7.7	4.1	0.8
Miyazaki et al	[23]	2003	30	16	56.0	9.0	1.0	0.5
Mehr et al	[30]	2000	40	55	59.0	9.5	1.9	1.4
Hamedi-Hagh et al	[29]	2001	50	65	57.0	9.2	2.2	1.3
Stroeble et al	[35]	2004	80	33	56.0	9.0	0.8	0.4
Min et al	[26]	2003	80	69	58.0	9.3	1.3	0.9
Park et al	[9]	2001	80	80	55.7	9.0	2.0	1.0
Narin	[32]	2000	100	105	58.0	9.3	1.6	1.1
Li et al	[24]	2003	100	67	54.0	8.7	1.6	0.7
S. Yoo et al	[25]	2002	120	208	58.2	9.4	2.6	1.7
Jamal et al	[28]	2002	120	234	56.8	9.1	3.4	2.0
Yoo et al	[34]	2003	150	123	54.0	8.7	2.0	0.8
Hernes et al	[33]	2004	220	135	54.3	8.7	1.4	0.6

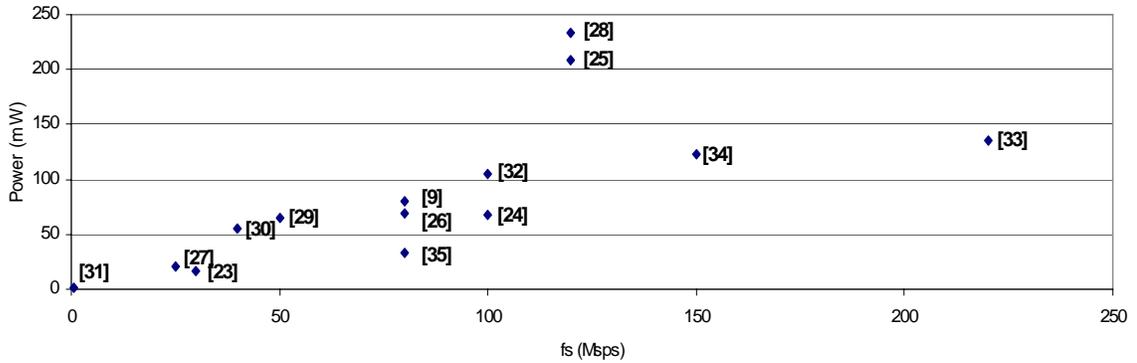


Fig. 3-10: Power vs. speed for recent publications

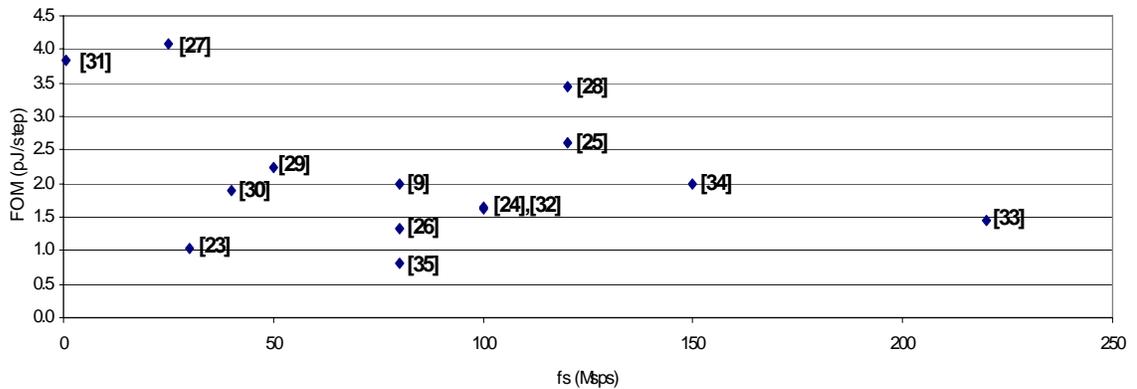


Fig. 3-11: FOM in pJ/step for recent publications (from equation 2.7)

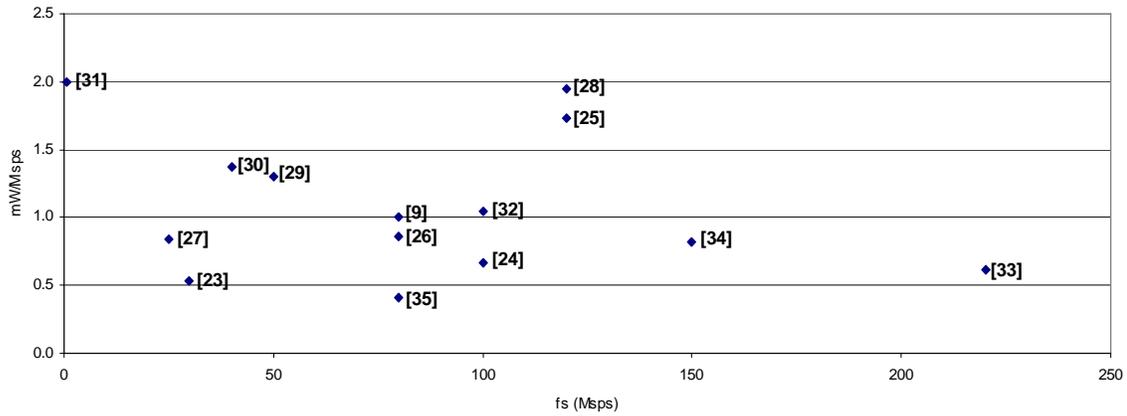


Fig. 3-12: Power per conversion step (power/speed) for recent publications

3.7: Summary

In this chapter circuit level implementation and design related issues were discussed for key components in a 1.5 bit/stage pipeline ADC: the stage MDAC and stage ADC comparators. It was shown for a desired settling accuracy, MDAC opamps require a minimum gain and unity gain bandwidth. Noise limitations due to thermal and opamp noise were shown limit minimum MDAC sampling and feedback capacitor sizes. Two popular dynamic comparators were examined: the Lewis and Gray comparator, and the charge distribution comparator, where it was shown the optimal comparator was a tradeoff between power and input referred offset. The chapter concluded with a brief survey of recently published, and industry 10-bit ADCs where the respective FOMs were compared in tabular and graphical form.

CHAPTER FOUR

Power Scaling: Design Issues

4.1: Overview

This chapter discusses approaches to scale power with sampling frequency. A comparison of digital versus analog power is given, where current scaling is shown as an analog power scaling technique. The consequences of extended power scaling using current scaling are emphasized where excessive current scaling is shown to increase design and simulation difficulty, and result in poorer yield due to larger mismatches, increased bias voltage sensitivity, and IR drops.

4.2: Motivation for power scaling

Total ADC power must scale with sampling rate, as from equation 2.7, the ADC figure of merit is a function of the ratio of power to sampling rate:

$$FOM = \frac{Power}{(2^{ENOB})(f_s)}$$

Thus to maintain a fixed figure of merit as the sampling rate is decreased, the power must also decrease. Analog power does not automatically scale with sampling rate as the product of supply voltage and net current consumed (which are not explicit functions of the sampling rate) determine analog power. Thus a power scaleable ADC requires techniques to make the analog power an explicit function of sampling rate.

4.3: Digital versus Analog power

Digital circuits primarily operate transistors in triode and cut-off regimes, whereas in analog circuits transistors primarily operate in the saturation regime. Steady state outputs in digital

circuits are realized by charging a load capacitance through a triode switch to a supply voltage as shown in Fig. 4-1.

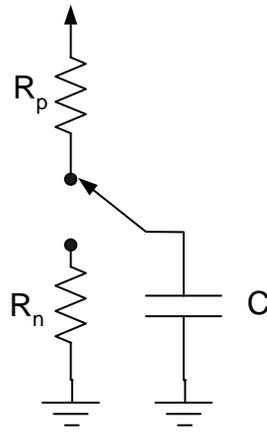


Fig. 4-1: RC model of digital switching

Thus digital circuits only require enough power to charge/discharge the load capacitance to the final logic level. For a full cycle from zero to one then back zero $Q = CV_{DD}$ is transferred from V_{DD} to ground in Fig. 4-1

$$\therefore E_{cycle} = QV_{DD} = CV_{DD}^2 \quad (4.1)$$

$$\therefore P = \frac{E}{T} = Ef \quad (4.2)$$

$$\therefore P = CV_{DD}^2 f \quad [36] \quad (4.3)$$

Thus, assuming the digital circuitry in an ADC is clocked by the sampling clock, the average digital power automatically scales with sampling frequency. In most ADCs however, the digital power consumes only a small fraction of the total power, thus if ADC power is to scale with sampling frequency, analog power must also scale with sampling frequency.

As analog circuits require static bias currents to bias transistors in the active region, analog power is given by the product of two static quantities: $P_{analog} = IV$. Thus if analog power is to scale with sampling frequency, voltage and/or current must be made functions of the sampling frequency (i.e.: $P(f_s) = i(f_s)V(f_s)$). Power scaling by supply voltage scaling is not a viable option as reducing the supply voltage reduces signal swing, possibly moving

saturated devices into the triode region, and/or significantly reducing the ADC SNR due to reduced signal swings. As minimum signal swings are required in analog circuits, power scaling by voltage reduction can only provide a minimal power-speed dependency. Analog power scaling is commonly achieved by making the bias currents a function of sampling frequency [33], [37]. In [33], total ADC power is scaleable between 3Msps-220Msps, and in [37] opamp bias currents are shown to be scaleable between 10kHz-10MHz; both implementations use current scaling to reduce bias currents with operating speed. Assuming a first order response of an opamp as shown in Fig. 4-2, opamp unity gain frequency is given by

$$\omega_{ta} = \frac{g_m}{C_{load}} \quad (4.4)$$

$$\therefore \omega_{ta} = \frac{1}{C_{load}} \sqrt{2\mu C_{ox} \frac{W}{L} I_D} \quad (4.5)$$

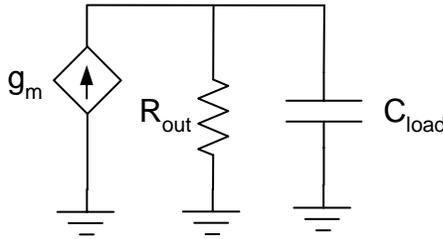


Fig. 4-2: simplified small signal opamp model

Thus reduction of bias currents with sampling frequency reduces the bandwidth of the opamp, which is consistent with the concept of maintaining a constant figure of merit, i.e.: since the sampling frequency is reduced, the opamps do not require as high a bandwidth as more settling time is available.

According to square law equations, as transistor drain-source currents are reduced, transistor $V_{GS} \rightarrow V_t$

$$\therefore V_{GS} = \sqrt{\frac{2I_D}{k \frac{W}{L}}} + V_t, \quad (4.6)$$

$$\therefore \lim_{I_D \rightarrow 0} V_{GS} = V_t \quad (4.7)$$

In actuality however as transistor V_{GS} tends to V_t , the channel region below the gate oxide becomes less inverted [38] (referred to as weak inversion), such that the inversion channel bridging the source and drain becomes diffusion carrier dominated, rather than drift carrier dominated as is the case in strong inversion. Thus like BJTs (which have a current dominated by diffusion), MOS transistors for low bias currents have a current that is exponentially related to the gate-source voltage [39]. Hence the I_{DS} - V_{GS} relation deviates from square law when $V_{GS} \rightarrow V_t$. In practice a current flows between drain and source for $V_{GS} < V_t$

An advantage of weak inversion operation is due to the exponential dependency of current on gate-source voltage, the g_m/I_D ratio (i.e. transistor gain) is a maximum in weak inversion [40]. Weak inversion operation is commonly used in analog circuits that require very low power consumption. A significant disadvantage of operation in the weak inversion region however is the lack of continuous, easy to manipulate models of transistor operation in weak inversion. As such design in weak inversion is often avoided where power requirements are not stringent, since careful design would require much background knowledge in weak inversion operation as well as patience to deal with complicated device parameters [1]. Furthermore as most ADCs are designed in digital or logic processes (which rarely operate transistors in weak inversion), transistor simulation models may not be well characterized in the weak inversion regime. Thus a functional ADC that relies on poor weak inversion models could take several fabrication iterations before all desired specifications are met [1].

4.4: Weak inversion model - EKV

This section briefly discusses a popular model (EKV) [1], [41], which describes transistor operation in both strong and weak inversion regions. In the EKV transistor model, drain-source current is given as the difference between a forward current, and a reverse current [41]:

$$I_{DS} = I_F - I_R \quad (4.8)$$

Where the forward current depends on gate and source voltages, and the reverse current depends on gate and drain voltages. For an NMOS transistor the current components can be expressed as [41]

$$I_{F(R)} = \frac{W}{L} I_s \log^2 \left(1 + e^{\frac{\kappa(V_G - V_{T0}) - V_{S(D)}}{2U_T}} \right) \quad (4.9)$$

where $\kappa \equiv \frac{C_{ox}}{C_{ox} + C_{dep}}$ is the reciprocal of the sub-threshold slope factor, V_{T0} is the zero-bias threshold voltage, and $U_T \equiv \frac{kT}{q}$ is the thermal voltage. I_s is the specific current which is roughly twice the threshold current of a square transistor (note I_s is NOT the source current) and is given as

$$I_s = \frac{2\mu C_{ox} U_T^2}{\kappa} \quad (4.10)$$

If the forward current is much larger than the reverse current, the channel current depends on V_{GS} , and becomes largely independent of the drain potential - hence the transistor is saturated. If I_F is comparable to I_R however, the channel current depends on drain and source potentials, hence the transistor is in the ohmic or triode region.

The *inversion coefficient* (IC) describes the level of channel inversion, and is given as

$$IC = \frac{I_D}{I_s} \quad (4.11)$$

A transistor is in strong inversion if $IC > 10$, moderate inversion if $IC \sim 1$, and in weak inversion if $IC < 0.1$ [42]. In terms of V_{eff} , this typically translates into strong inversion for $V_{eff} > 220\text{mV}$, weak inversion for $V_{eff} < -72\text{mV}$, and moderate inversion between weak and strong inversion, i.e. $V_{eff} \approx 40\text{mV}$ [42].

4.5: Weak inversion issues - mismatch

A major disadvantage of transistor operation in weak inversion is an increased current mismatch. The current mismatch of two transistors in weak inversion that have the same V_{GS} (e.g. a current mirror) is given by

$$\sigma_{I_D} = \sqrt{\sigma_{\beta}^2 + \left(\frac{g_{mg}}{I_D} \sigma_{V_t}\right)^2} \quad (4.12)$$

where $g_{mg} = \frac{I_D}{nU_T} \sqrt{\frac{1}{i_{f1} + \frac{1}{2}\sqrt{i_{f1} + 1}}}$, $i_{f1} = \frac{I_D}{2n\beta U_T^2}$, and n is a fitting factor between 1-2 [1].

The relationship between current mirror mismatch, area, and bias current is illustrated in Fig. 4-3.

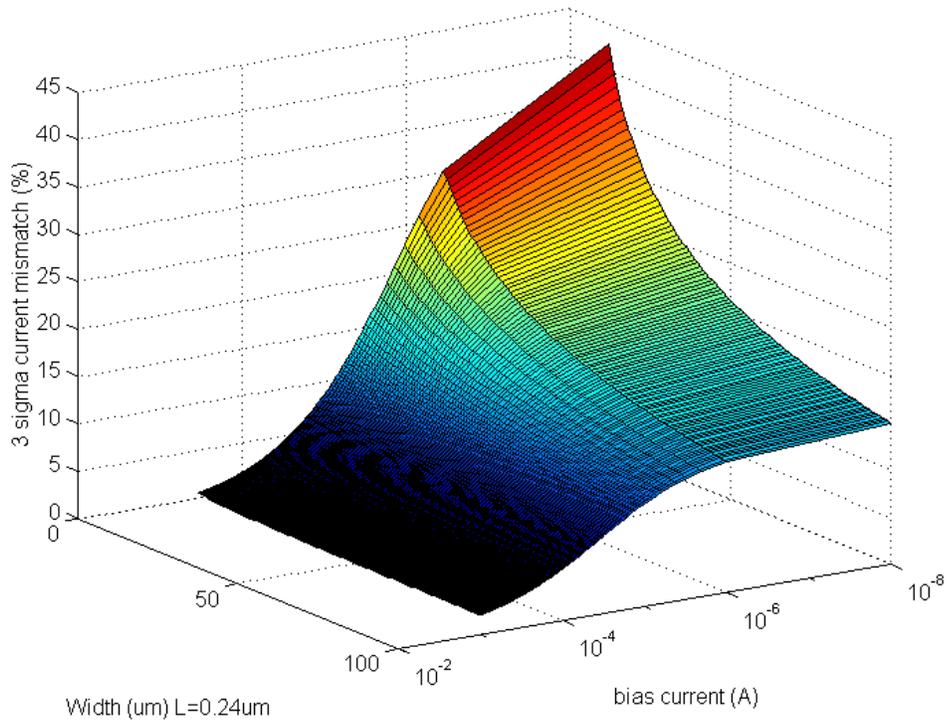


Fig. 4-3: 3 σ current mismatch versus device area and bias current

From Fig. 4-3 it is clear as the bias current decreases (placing the transistor deeper into weak inversion), the 3 σ mismatch of the mirror current increases significantly [1], [41]. One

consequence of the current mismatch is a sub optimal distribution of power in an ADC. For example, consider Fig. 4-4, where the opamps of several stages in a pipeline ADC are biased with a single current mirror, which has $3\sigma = 15\%$ mismatch in current (i.e. $\pm 7.5\%$ peak variation). Since a pipeline is limited by the slowest stage, potentially the power could have to be increased by over 15% to meet the desired bandwidth.

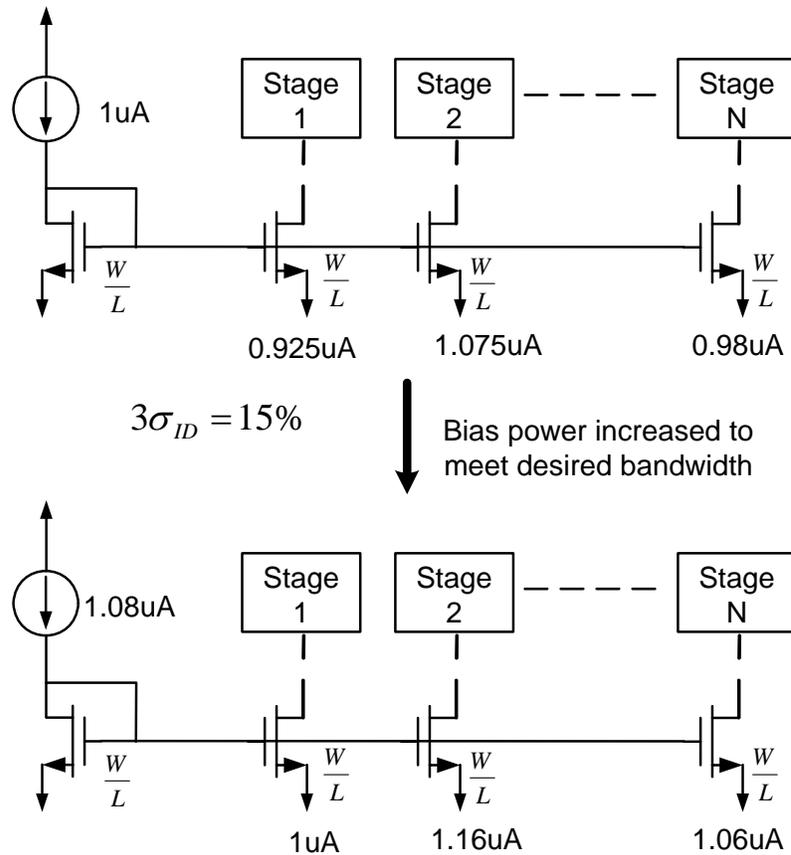


Fig. 4-4: illustration of impact of mismatched current sources

Clearly a 15%+ increase in power is not desirable - especially since much of the excess power is wasted. Often to avoid the high mismatch in current mirrors, mirror transistors are designed with a large area, but small W/L ratio so as to maintain strong inversion (e.g. $V_{\text{eff}} \sim 400\text{mV}$). Such an approach however requires a large area overhead to maintain strong inversion over large variations in bias current. (E.g.) in [43] to maintain a current mirror transistor in strong inversion for a bias current of 25nA in a $0.35\mu\text{m}$ process, a W/L ratio of $3\mu\text{m}/50\mu\text{m}$ is used for the current mirror transistors. Note that a current source transistor

sized at $3\mu\text{m}/50\mu\text{m}$ cannot be used for higher bias currents without V_{eff} becoming prohibitively large. Thus if the current source transistor were used to bias an opamp for various current scaled values (for different sampling rates), an array of different current mirrors must be used (to maintain strong inversion for different bias currents), thus consuming additional area.

For smaller length technologies (e.g. $0.09\mu\text{m}$) leakage current can become a significant issue if bias currents are on the order of nanoamps. With bias currents on the order of leakage currents, reliable analog circuit design can become difficult, as transistors cannot be accurately biased with desired drain-source currents. In other words, one cannot necessarily guarantee if a device is in active or triode.

4.6: Multiple design corners

Although simple to implement, current scaling has the disadvantage that it necessarily increases the number of design corners in the ADC. As the range of bias currents between minima and maxima are required to be verified over temperature and process corners, design/simulation time for an ADC using current scaling as a power scaleable technique can be excessive (and thus expensive). Multiple bias currents also increase post fabrication test time, hence increasing cost, as the ADC must be verified at all corners to ensure a working product is delivered to the customer.

4.7: Current scaling – Bias point sensitivity

Consider the differential $\frac{dI}{dV_{gs}}$ for a transistor in strong and weak inversion:

Current sensitivity (Strong Inversion)

$$\frac{dI}{dV_{GS}} \approx 2k(V_{GS} - V_t) \quad (4.13)$$

Current sensitivity (Weak Inversion)

$$\frac{dI}{dV_{GS}} \approx e^{\frac{V_G - V_t - V_s}{nU_T}} \quad (4.14)$$

In strong inversion the rate of change of drain-source current varies linearly with V_{GS} variation, whereas it is exponential in weak inversion. Thus if a transistor is acting as a current source to an opamp is in weak inversion, a small variation of gate-source voltage on

the transistor due to (e.g.) noise coupling from a nearby digital circuit, thermal fluctuations of a resistor acting as a reference current source, or threshold mismatch, will cause the unity gain frequency of the opamp, hence accuracy of the ADC to fluctuate significantly. An analogous problem manifests with the biasing of BJT transistors (which have an exponential relation between current and base-emitter voltage). To reduce current sensitivity, BJTs use emitter degeneration to reduce the transistor gain, at the cost of reduced signal swing and increased power. Although degeneration resistors could be switched in and out in a power scaleable ADC to reduce mismatch for different bias currents, multiple design corners still remain, thus a significant amount of time would be required to verify the ADC over all design corners.

Thus although it is possible to operate an opamp (hence a pipeline ADC) while deep in the weak inversion region, the high sensitivity of the bias nodes makes current scaling over large ranges (such that transistors are driven deep into weak inversion) an impractical approach to achieve lower power for low f_s . The high sensitivity to bias fluctuations could be significant if the ADC were part of a larger, noisier digital system, where fluctuations of a few mV could easily be induced on opamp bias nodes from (e.g.) substrate noise.

4.7.2: Current scaling – IR drops

In some cases an IR drop is required across a resistive load to provide a specific gain. If bias currents are reduced, the gain and signal swing also reduce since,

$$A \approx g_m R = R \sqrt{2\mu C_{ox} \frac{W}{L} I_D} \quad (4.15)$$

\therefore as current decreases, gain decreases. An example of resistor dependent gain is shown in Fig. 4-5, specifically a pre-amp which is commonly used in Flash ADC comparators, and multi-bit/stage pipeline ADCs comparators. Alternatively active loads can be used to provide gain, as shown in Fig. 4-6. Such configurations have a gain which increases with reduced bias currents since

$$A \approx g_m r_{ds} = \frac{\sqrt{2\mu C_{ox} \frac{W}{L} I_D}}{\lambda I_D} = \frac{1}{\lambda} \sqrt{\frac{2\mu C_{ox} \frac{W}{L}}{I_D}} \quad (4.16)$$

∴ as current decreases, gain increases. Active differential loads however require common-mode feedback to have a defined output common-mode.

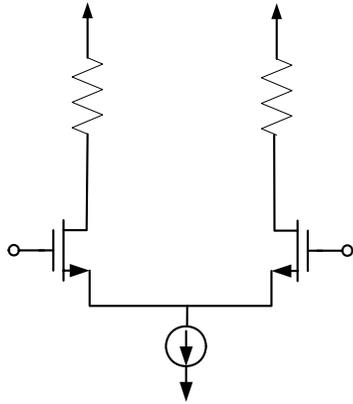


Fig. 4-5: differential pair with RC load

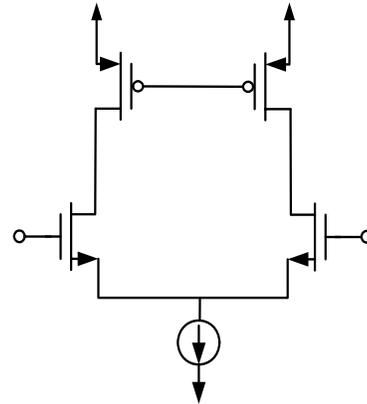


Fig. 4-6: differential pair with active load

IR drops across power supplies also pose a potentially significant design issue for weak inversion operation. As mentioned in section 4.7, current mirror transistors have a high sensitivity to bias node fluctuations, thus it is possible that even a small IR drop of a few mV between mirror transistor supply voltages (due to e.g. physical separation on a larger chip) could cause significant current mismatch hence potentially reduced performance (e.g.: Fig. 4-7).

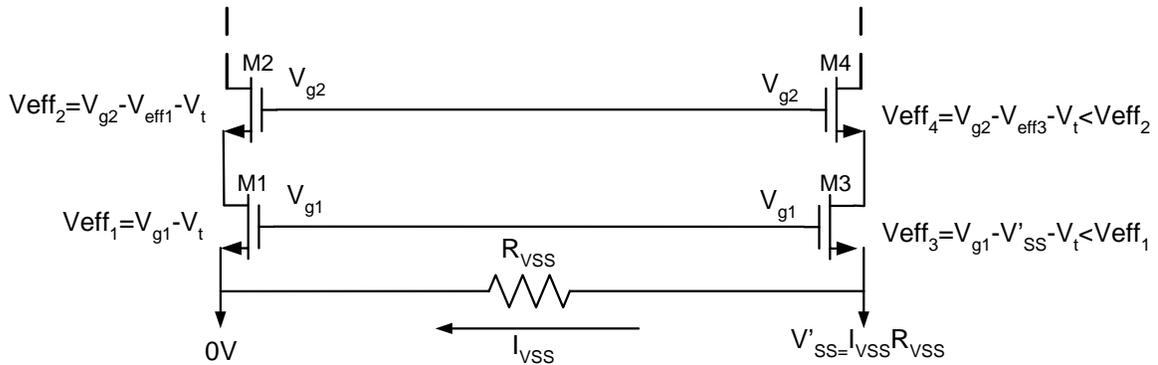


Fig. 4-7: impact of low currents on IR drops

If the transistors of Fig. 4-7 however are in strong inversion, the current is a much weaker function of V_{GS} , thus small V_{GS} variations due to IR drops have a much smaller impact on the desired bias current.

4.8: Survey of power scaleable ADCs

To date power scaleable ADCs have not been an active area of research, and as such there are very few publications which target a scaleable power over a large range of sampling rates [33], [37]. All published reports of ADCs with scaleable power use bias current scaling to reduce power with sampling rate. In industry however, several 10-bit ADCs have been developed which have a scalable power. High-speed architectures ($f_{s-max} > 10\text{Msps}$) achieve lower power for lower sampling rates using current scaling, and are shown in datasheets to have a small power scaleable range (<1:100), likely due to poorer yield at lower sampling rates as transistors are driven into weak inversion. Low-speed architectures (<500ksps) achieve power scaleability by powering off the ADC between conversion samples. Due to the slow power on/off times of ADCs however, the technique of powering off an ADC between conversions is limited to slower architectures, based on a survey of commercial 10-bit power scaleable ADCs. A survey of power scaleable ADCs in industry is given in Table 4-1.

Table 4-1: Survey of Power scaleable ADCs in Industry

<i>Power scaleable ADCs in industry</i>						
<i>Company</i>	<i>Model</i>	<i>Speed (MSPS)</i>	<i>Power (mW)</i>	<i>SNDR</i>	<i>ENOB</i>	<i>P. Scaling method*</i>
ADI	7467	0.05	0.48	61	9.84	A
ADI	7467	0.1	0.62	61	9.84	A
ADI	7811	0.001	0.0315	58	9.34	A
ADI	7811	0.01	0.315	58	9.34	A
ADI	7811	0.1	3.15	58	9.34	A
ADI	7811	0.35	10.5	58	9.34	A
ADI	9203	5	17	60	9.67	B
ADI	9203	40	75	59.3	9.56	B
Maxim	Max1086	0.001	0.00405	61	9.84	A
Maxim	Max1086	0.01	0.0351	61	9.84	A
Maxim	Max1086	0.05	0.1755	61	9.84	A
Maxim	Max1086	0.1	0.351	61	9.84	A
Maxim	Max1086	0.15	0.54	61	9.84	A
Nordic VLSI	nAD1050-18	10	8	59	9.51	B
Nordic VLSI	nAD1050-18	50	33	59	9.51	B
Fairchild Semi	SPT7883	10	20	60	9.67	B
Fairchild Semi	SPT7883	50	105	60	9.67	B
Fairchild Semi	SPT7883	70	129	57	9.18	B

*A is when ADC is powered off between conversions

*B is when current scaling is used to reduce power with sampling rate

4.9: Summary

This chapter discussed the dependency of power with sampling rate for analog and digital systems. Current scaling was shown as common technique to reduce analog power with sampling rate. It was shown that current scaling drives MOS transistors deep into the weak inversion region for extended reductions in sampling rate, where due to less accurate models, circuit design/fabrication could take several iterations to meet desired performance. Increased mismatch, bias point sensitivity, and IR drops were also shown as limiting factors to the extent to which current scaling can be used to reduce analog power.

CHAPTER FIVE

Power Scalable and Low Power ADC using Power Resettable Opamps

5.1: Overview

This chapter discusses the architecture of a power scaleable pipeline ADC, which has its power a function of sampling rate. A power scaleable range over a large range of sampling rates is achieved without resorting to extensive current scaling, thus avoiding the problems of MOS transistors biased in weak inversion as described in chapter four. A general architecture for power scaleable ADCs using a *Current Modulated Power Scale* (CMPS) approach is presented, where the application of CMPS to pipeline ADCs forms the focus of this work. Approaches to modulate current are presented, where a novel fast *Power Resettable Opamp* (PROamp) using a replica bias approach is shown to allow for CMPS to be used at high sampling rates in pipeline ADCs. The short on/off times of the PROamp are also shown to facilitate significant power reductions of opamp power in the MDACs of conventional pipeline ADCs, and more generally switched capacitor circuits, which have a clock phase that does not require a virtual ground. As such the MDAC stages are designed to power off during the sampling phase, and optionally remain on during the sampling phase so that a measure of the power savings afforded by powering off the opamp during the sampling phase can be measured. Design choices and justifications are presented, with simulation results in SPICE given to validate the architecture.

5.2: Power scaleable architecture

From chapter four it is clear the many design problems associated with current scaling make it an undesirable power scaleable approach for extended variations in f_s . Current scaling may be avoided however if the power scaleable constraint is relaxed to average power rather than instantaneous power - i.e. $P_{avg}(f)$. Since the instantaneous power of ICs often varies significantly (due to digital circuitry), relaxing the power scaleable constraint to average power is a valid compromise. The formula for power is altered to include average values as follows:

$$P_{avg} = \overline{P} \longrightarrow \overline{P} = \overline{IV} \quad (5.1)$$

As mentioned in section 4.3 voltage scaling is not a feasible approach, thus $\overline{V} = V_{DD}$,

$$\therefore \overline{P} = \overline{P(f)} = \overline{IV}_{DD} = \overline{I(f)}V_{DD} \quad (5.2)$$

Hence to obtain a power scaleable average power, the average current must be frequency dependent. Although current scaling satisfies equation (5.2), alternative current scaling methods can be found which also satisfy equation (5.2), yet do not impose the problems mentioned in chapter four. An alternative method can be derived by examining the ADC architecture, the settling requirements of the ADC, and the nature of digital circuits - which have their average power a function of frequency.

In digital circuits power is consumed only on output transitions where as described in section 4.3 only enough power is consumed to set the digital output to the desired logic level. A characteristic of an ADC which may be exploited is although ADCs are predominantly analog, the final output is digital. Thus per output sample, the ADC only requires enough power to set the output to the logic levels representing the analog input. When an ADC operates at full speed, just enough analog power is supplied to allow the analog circuits to settle to the desired accuracy, and thus provide the correct digital output. If the sampling rate is decreased while maintaining constant bias currents (hence constant analog power), the opamp settling time remains unchanged but the figure of merit is reduced as the sampling rate decreases whereas the power remains approximately constant. As the ADC output is digital however, only enough power is required to charge/discharge the digital output to the

correct logic levels, which as shown in Fig. 5-1, is achieved after $t_{ON} = t_{analog} + t_{digital}$ seconds.

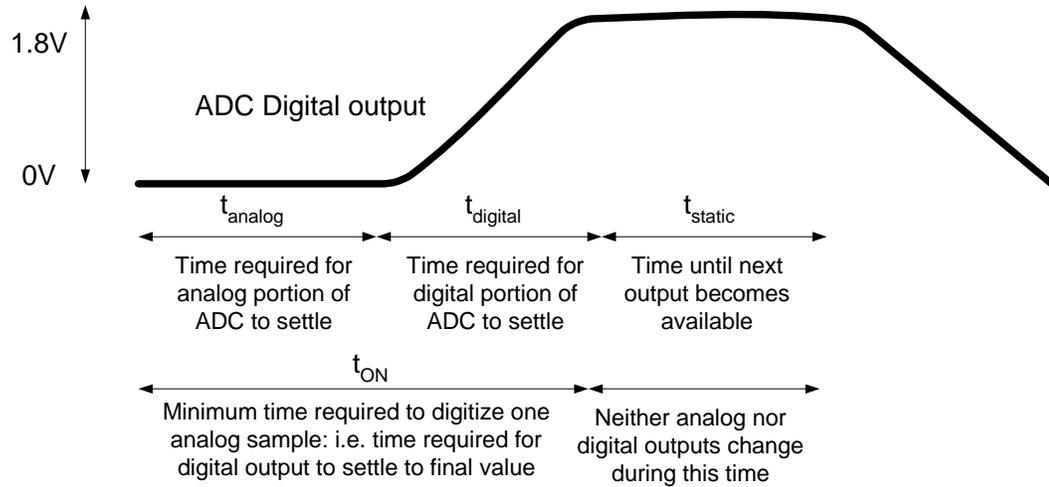


Fig. 5-1: setup times for a nominal ADC

Since the ADC is idle during t_{static} , if the digital output is latched from the ADC after t_{ON} , the analog portion of the ADC may be powered off after t_{ON} until the next sample is digitized as shown in Fig. 5-2.

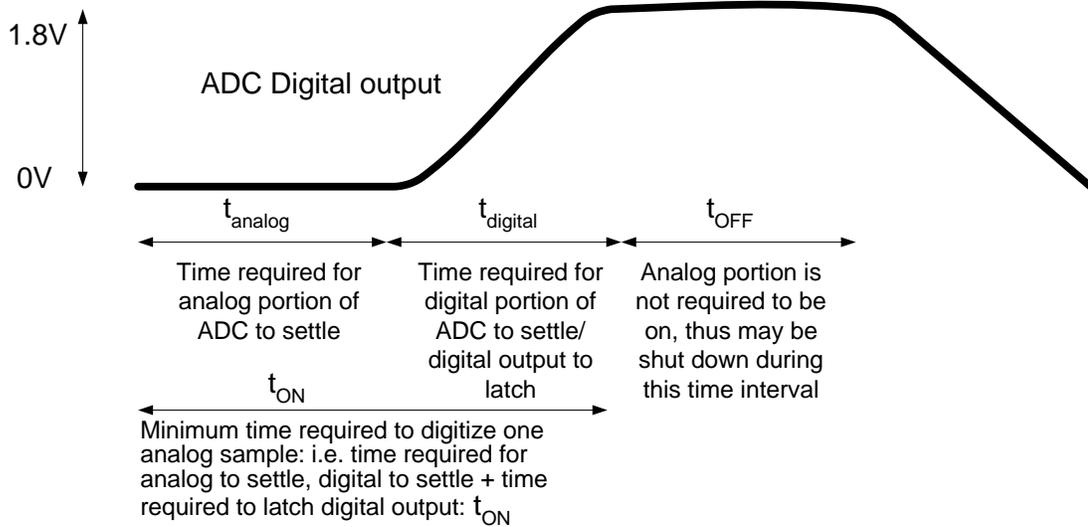


Fig. 5-2: setup times for a current modulated ADC

Thus by powering off the analog portion of the ADC during t_{static} (which is related to the sampling frequency – the larger t_{OFF} , the lower the sampling rate), the ADC power can be made a function of effective sampling rate, i.e.

$$P_{\text{avg}} = P_{\text{on}} \frac{t_{\text{on}}}{t_{\text{on}} + t_{\text{off}}} = P_{\text{on}} \frac{t_{\text{on}}}{T_{\text{effective}}} = P_{\text{on}} t_{\text{on}} f_{\text{effective}} \quad (5.3)$$

where $f_{\text{effective}}$ is the effective sampling rate, and P_{on} the average power consumed by the ADC during t_{on} . The variation of average power with sampling rate is shown in Fig. 5-3, and Fig. 5-4:

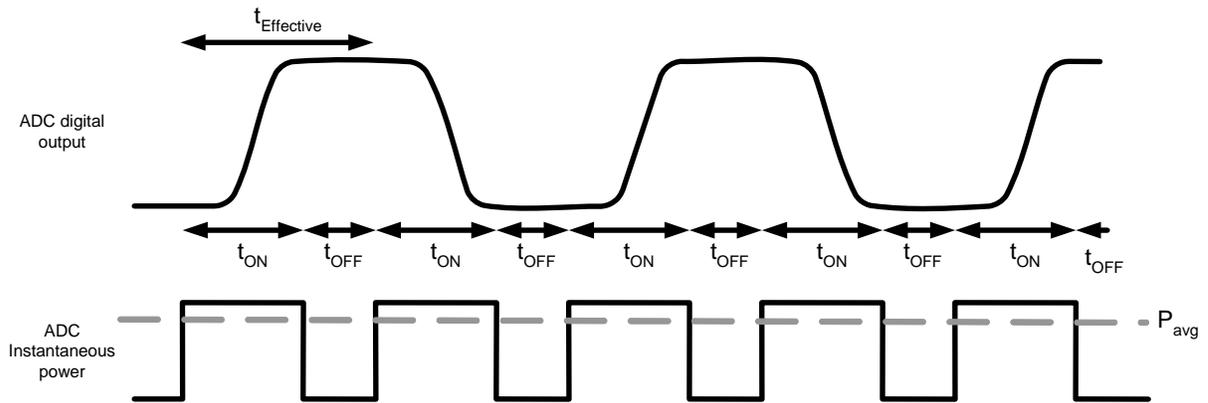


Fig. 5-3: illustration of a high average power with modulated current

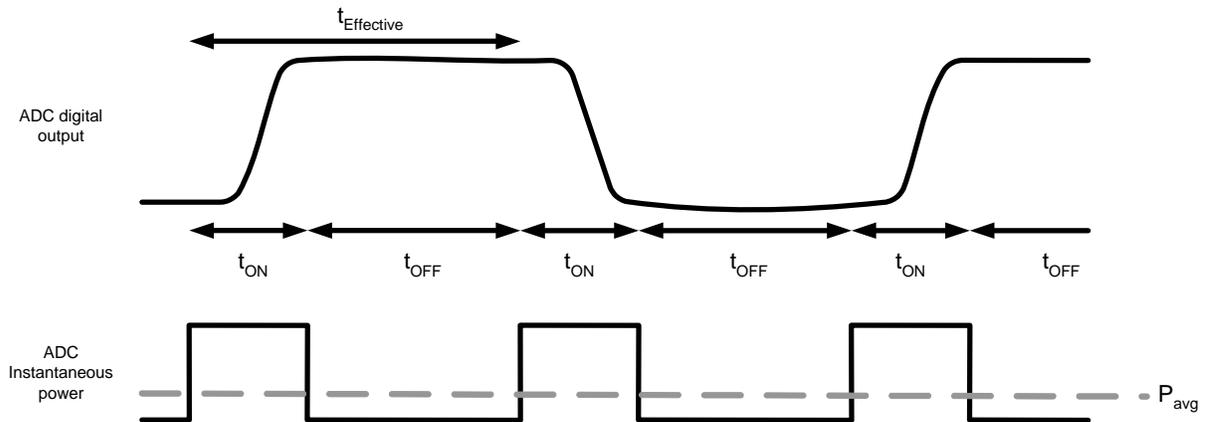


Fig. 5-4: illustration of low average power with modulated current

Thus as the effective sampling rate decreases, ADC power is reduced by time averaging, and since P_{on} remains constant between sampling rates, the bias currents in the ADC, and thus the

degree of channel inversion remain fixed. Hence the problems of poor device modeling, poor current matching, increased bias point sensitivity, and problems associated with IR drops of devices with low current biasing (hence weak inversion) are completely avoided. Since different power scaled sampling frequencies can be achieved while maintaining a constant on time (thus constant settling time), analog circuitry is minimally affected over frequency scaling. Thus the ADC characteristics for several sampling frequencies can be determined through simulating/testing only one sampling frequency, saving a significant amount of design, simulation, and test time over the current scaling method of chapter four. (E.g.) the *Effective Number Of Bits* (ENOB) at $f_s=10\text{Msps}$ is the same as $f_s=1\text{Msps}$, $f_s=100\text{ksps}$, $f_s=10\text{ksps}$, etc. as the bias current is unchanged between f_s - only the off time varies for different f_s .

It should be noted that if current scaling is used in addition to current modulation, the effective scaleable range is the product of the two scaleable ranges: (E.g.) If current scaling is used to scale the power between $f_s=50\text{MHz}$, and $f_s=5\text{MHz}$ (10x reduction in power), and the *Current Modulated Power Scale* (CMPS) technique allows for a 100x power scaleable reduction in f_s , application of CMPS to the current scaled sampling rate of 5MHz, allows for the sampling frequency to be reduced to $5\text{MHz}/100=50\text{kHz}$ without further reduction in bias currents. Thus, the scaleable range is $10 \times 100 \rightarrow 1:1000$, although the bias currents are only scaled 1:10. As a result, the current modulation technique improves on the maximum achievable power scaleable range possible with current scaling.

The CMPS technique described in this section, although independently derived for this dissertation, has been previously used to provide power scaleability in commercial ADCs (e.g.: ADI7811, Max1086). Although not fully explained, the datasheets of these commercial ADCs indicate that low power at low sampling rates can be achieved by placing the ADC in 'sleep mode' (i.e. all main blocks of ADC are powered off) between conversion samples. Commercial ADCs that achieve power scaleability by CMPS however are typically limited to slower architectures (e.g. serial, Successive Approximation, etc.), and thus slower maximum speeds (<500ksps). To the best of the author's knowledge, ADCs that have a scaleable power between very low sampling rates (e.g. <10ksps), and high sampling rates

(e.g. >10Msps), are not published, nor commercially available. Faster commercial ADCs (>10Msps) using faster pipeline architectures which have power scaleability (e.g.: Nordic nAD1080-18, Fairchild SPT7883), achieve power scaleability by current scaling, and are only shown to scale power with sampling rate over a small range of f_s (e.g. 1:10-100). As the goal of this work is to develop an ADC that can have a scaleable power between very high and very low sampling rates, this work represents the first investigation of power scaleability in ADCs over very wide variations in sampling rate

5.3: Current Modulated Power Scale (CMPS) in Pipeline ADCs

From Fig. 5-2 the maximum sampling rate of an ADC that uses the CMPS technique is limited by the time to completely digitize one analog sample t_{ON} - the latency of the ADC. As CMPS powers down the analog portion during t_{OFF} , the ADC cannot have analog memory (through sample and holds) between output samples. Thus the speed advantage gained by pipelining stages, namely a sampling rate that is only $1/t_{stage-max}$ (where $t_{stage-max}$ is the maximum delay through a pipeline stage), is effectively removed in a pipeline ADC using CMPS. Since input samples that do not fully traverse the pipeline are erased when the ADC is powered off, the maximum sampling rate for a pipeline ADC using CMPS is $1/(Nt_{stage-max})$, where N is the number of pipeline stages (each stage requires half a clock cycle to traverse). Although CMPS applied to pipeline ADCs limits the maximum sampling rate, the successive stage architecture of the pipeline ADC lends itself to easy adaptation of the CMPS technique.

From equation (5.3), due to the large latency (hence large t_{ON}) of pipeline ADCs, powering off the ADC after a single sample is digitized leads to large average power consumption. Analog power of a pipeline ADC using CMPS however, can be reduced by powering the minimum number of pipeline stages per output sample. Consider the example of Fig. 5-5: the sampled inputs between $0.5T \rightarrow 6.5T$ do not fully traverse the pipeline ADC before the pipeline is powered off (i.e. these samples are not digitized to 10-bit accuracy), and thus the samples between $0.5T \rightarrow 6.5T$ may be ignored all together. By only powering the pipeline

stages one at a time, as the input sample at $0T$ traverses the pipeline, P_{ON} of the pipeline ADC using CMPS can be significantly reduced.

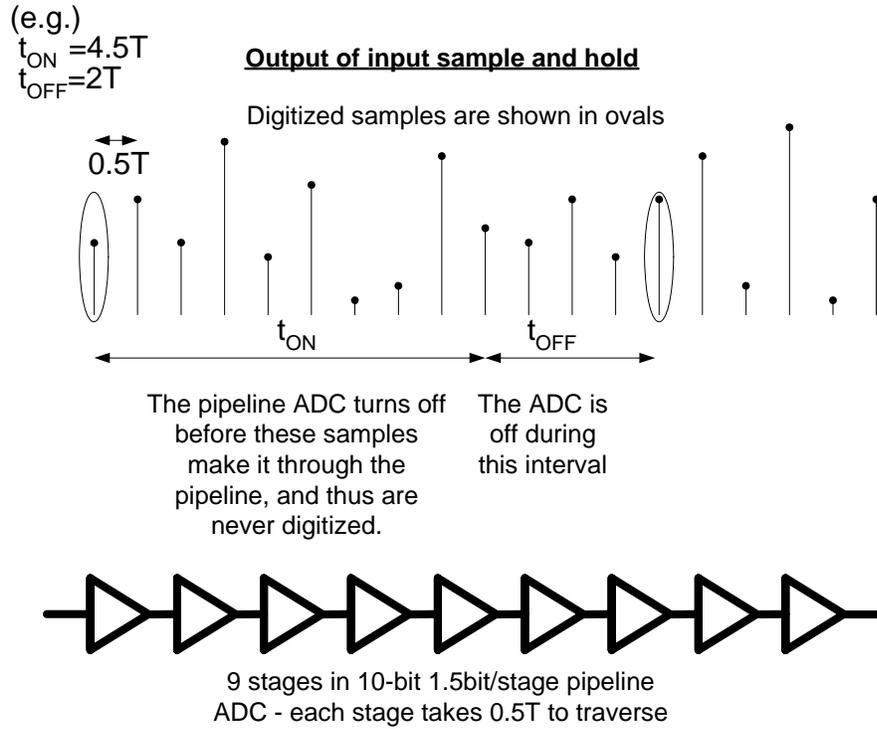


Fig. 5-5: example illustrating the valid inputs to a pipeline ADC

Therefore, by only powering a single stage at a time during digitization, the analog on power, P_{on} , can be reduced such that the average on power is the average power of a single stage. Fig. 5-6 illustrates this concept, where the average power is shown to be

$$P_{on-average} = average(P_{stage}) \quad (5.4)$$

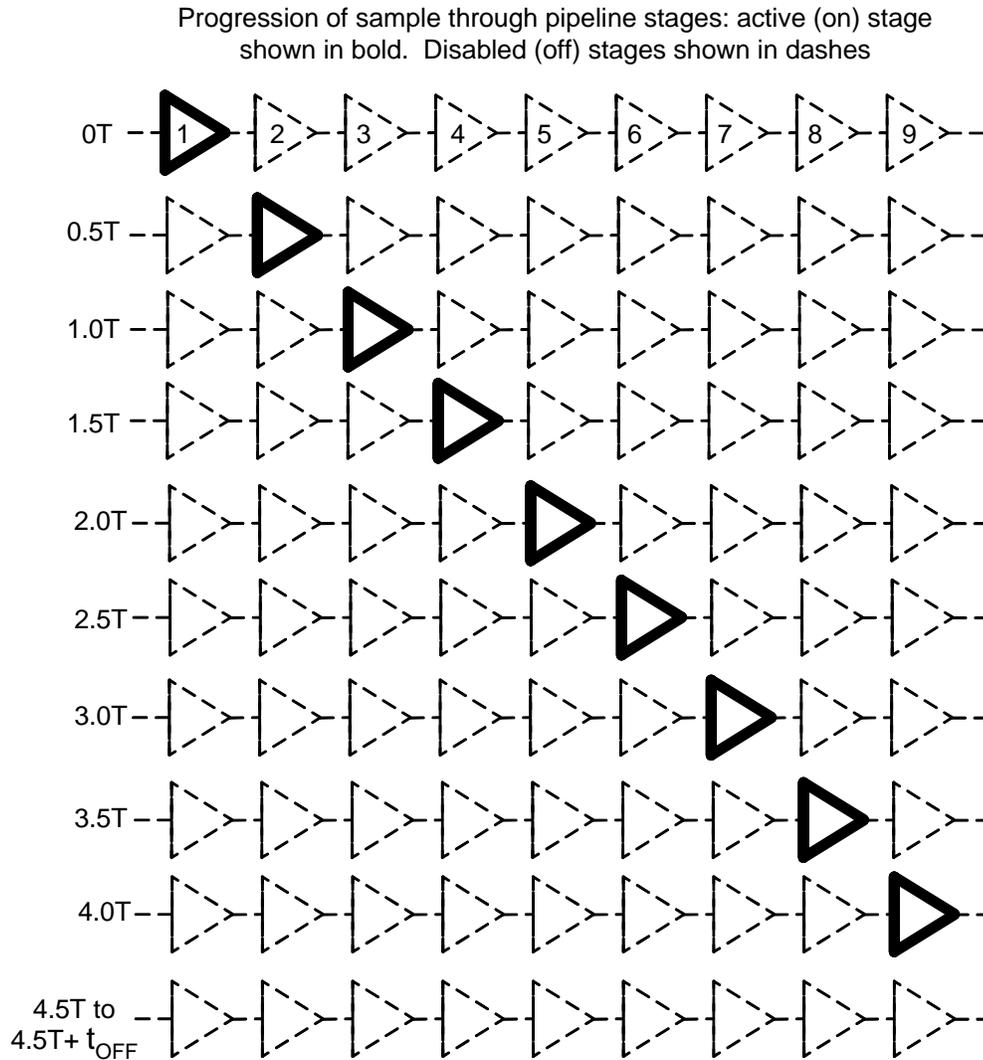


Fig. 5-6: on/off triggering sequence for a 10-bit pipeline ADC

In effect the pipeline ADC adapted to the CMPS technique operates as a Cyclic (Algorithmic) ADC, which operates successively in a special manner rather than a local manner. To adapt a high-speed pipeline ADC to use the CMPS technique to the following additional circuit blocks are required:

- 1.) Opamps that can completely power on and off very quickly with differential outputs that settle within one clock cycle after the opamp is powered on (need opamps similar to switched opamps [44], [45], [46], but at higher speeds to allow for high-speed

ADC operation, and such that the power goes to zero during the off phase), to facilitate the pipeline stages powering on/off as in Fig. 5-6.

- 2.) A digital state machine to generate control signals to power on/off the various pipeline stages in a sequential manner (can be easily hand designed or synthesized. Shown in section 5.7 to consume a small overhead power).

5.4: Current switching issues

From sections 5.2-5.3, analog power scaleability is shown to be possible by selectively powering on/off successive stages in a pipeline ADC. A consequence of powering analog blocks on/off is an increased power supply noise. When analog portions of the ADC are powered on/off the instantaneous current consumed by the power supplies changes a finite value in a very short time. As power supply noise is dominated by $L di/dt$ noise (ground bounce) [36], a large change in current over a short time interval leads to undesirable fluctuations in V_{DD} and V_{SS} . Although a fully differential architecture minimizes the impact of supply noise on sampled and held signals, unavoidable asymmetries in the layout and/or signal swings lead to a finite manifestation of power supply noise on sampled signals. Since supply noise is largely random (thus degrades the SNR), and 10-bit accuracy levels require very low noise floors (less than $780\mu\text{V}$ RMS noise for a 800mV signal swing), it is crucial to maintain as constant a power supply as possible. Supply voltages can be held constant through an on chip regulator [47], [48], which provides constant supply voltages regardless of current variation. On chip regulators however are often not feasible due to limited power and area constraints, as such alternative methods are typically required. Most integrated circuits use passive circuits to minimize AC supply noise. By placing a passive RC filter with a pole near DC (where resistance is used to reduce the quality of the LC tank formed by the package parasitics), supply noise (which is primarily high frequency) can be suppressed. A detailed analysis of power supply decoupling networks can be found in [36]

The RC filter of Fig. 5-7 was used for this dissertation to suppress power supply noise, where due to a low series resistance MIM caps ($\sim 40\text{pF}$) were used for C_1 , and due to a higher series resistance ([18], pg 622), MOS capacitors ($\sim 150\text{pF}$) used for the combination of C_2 and R .

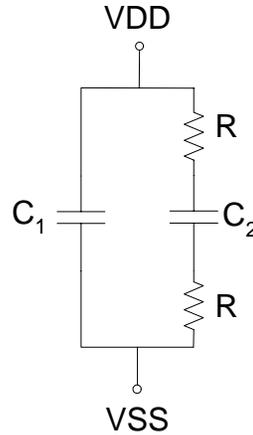


Fig. 5-7: power supply noise decoupling circuit

A significant advantage of applying CMPS to the pipeline architecture is on every clock transition there are at most two opamps powering on/off (while one opamp powers off another powers on). Thus the pipeline latency serves to reduce di/dt as less current is switched per clock cycle than (e.g.) a Flash ADC, which would switch a large current per clock edge to resolve all digital output bits in a single clock cycle (rather than just 1.5 as is the case in a 1.5bit/stage pipeline ADC). Thus a pipeline CMPS architecture generates less power supply noise.

5.5: Hybrid power scaling

As described in section 5.3, the CMPS technique applied to a pipeline ADC limits the maximum sampling rate to $1/t_{ON} = 1/t_{latency}$, which for a 10-bit, 1.5-bit/stage pipeline ADC limits the maximum sampling rate to at best $f_{fullrate}/4.5$ (nine pipeline stages requiring $\frac{1}{2}$ a clock cycle each to traverse). For example, applying the CMPS technique to a 50MSPs pipeline ADC limits the maximum sampling rate to $50\text{MHz}/4.5=11.1\text{MHz}$. Thus although the ADC is designed to run at 50MSPs if operated as a conventional pipeline ADC, CMPS cannot be used to achieve scaleable power between 11.1MHz-50MHz if 10-bit accuracy is

desired as shown in Fig. 5-8 (assuming the ADC is operated as a conventional pipeline ADC for 11.1MHz-50MHz).

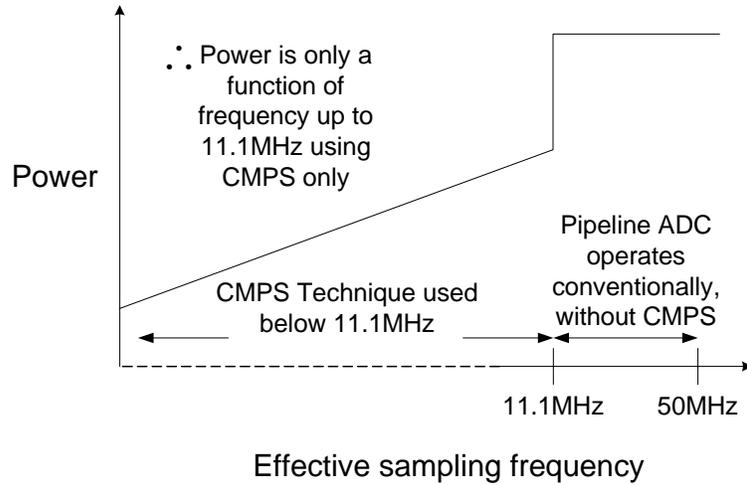


Fig. 5-8: CMPS limitations on power scaleable frequency range

Since the range of sampling frequencies not covered by CMPS is small (only 1:4.5 in the example), a hybrid approach that uses both CMPS and current scaling can be used. If current scaling is used to provide a scaleable power between the sampling rates not covered by the CMPS technique (i.e. 11.1MHz-50MHz) where the ADC operates as a conventional pipeline ADC, continuous power scaleability results as shown in Fig. 5-9.

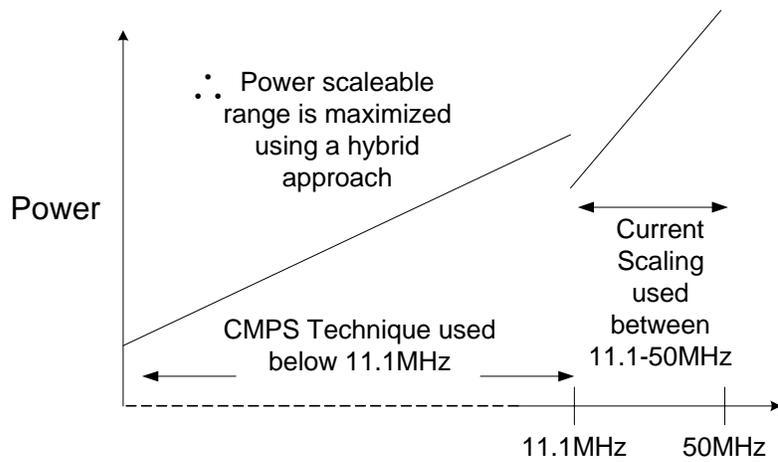


Fig. 5-9: continuous power scaleable range with hybrid power scaling

The problems of low current biasing (poor modeling, poor mismatch, increased bias sensitivity, and IR drops) are minimal with a hybrid approach as only a small current scaling range is required. Through careful design, the transistors can avoid operating in weak inversion over the narrow current scaling range. E.g.: $V_{eff} \propto \sqrt{I_{DS}}$ to a first order, thus a variation of bias currents by 10x reduces V_{eff} by ~ 3.3 . Thus if all current sources are designed to have a V_{eff} of 400mV for higher speeds, V_{eff} is only reduced to ~ 120 mV for the lowest current-scaled sampling rate, which according to section 4.4, places the device in moderate inversion.

In this dissertation a hybrid CMPS power scaling approach was taken where current scaling was used to achieve scaleable power for sampling rates not covered by CMPS. The hybrid CMPS approach was applied to a 10-bit 1.5-bit/stage pipeline ADC that was designed to have a maximum sampling rate of 50Msps.

5.6: Detailed Trigger Analysis

From Fig. 5-6, when using CMPS each stage opamp requires a trigger signal to power on/off the pipeline stages. In addition to the pipeline stages, other analog blocks must also be powered on/off, as equation (5.3) is based on the entire analog portion powering off during t_{OFF} . If certain circuit blocks are always on (i.e. are not powered off during t_{off} , and thus have a static power), the power scale formula of (5.3) is modified to

$$P_{avg} = P_{on} t_{on} f_{effective} + P_{static} \quad (5.5)$$

$$\therefore \lim_{f \rightarrow 0} P_{avg} = P_{static} \quad (5.6)$$

Thus as the sampling rate decreases, the power becomes less dependent on frequency, ultimately limited by P_{static} . Hence it is essential to minimize the number of blocks that are always powered on, so as to maximize the power scaleable range. A system level diagram of the showing each major block is shown in Fig. 5-10.

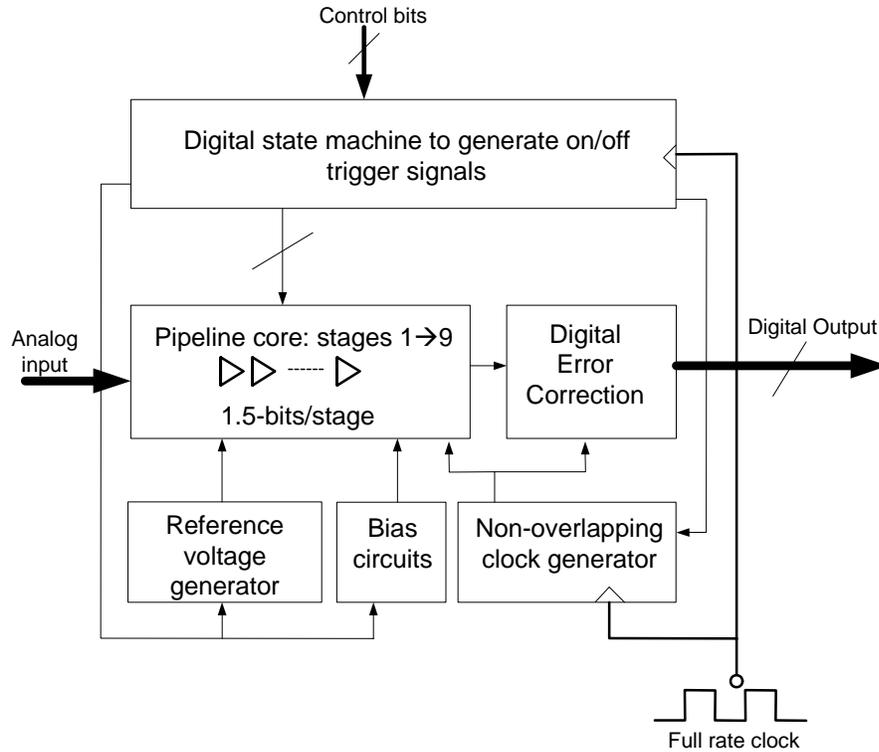


Fig. 5-10: major sub-blocks in a 1.5 bit/stage pipeline ADC using CMPS

In addition to the pipeline core (MDACs + stage ADCs), a power on/off scheme is required for the bias circuits, clock generator, reference generator, and digital error correction.

The digital state machine never powers down, as it is required to generate the on/off trigger signals for each block, thus contributes to P_{static} . As will be shown in section 5.7 however, the average power of the digital state machine can be made low, thus facilitating a large power scaleable range.

As each pipeline stage powers on/off according to Fig. 5-6, the bias circuit for each stage may also power on/off for the same time interval. However as bias nodes are often loaded with large capacitances, and set with low currents, the time required to power on/off a bias circuit to a minimum settling accuracy can be very large (relative to the on/off time of a pipeline stage – Fig. 5-12). Thus with the setup shown in Fig. 5-11 the bias circuit of stage X cannot be synchronously triggered with stage X, as the bias voltages do not settle quickly enough for proper operation of stage X.

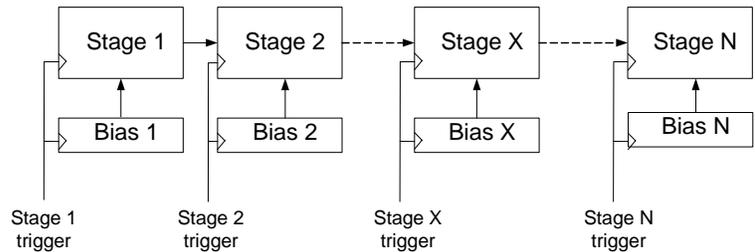


Fig. 5-11: 1 to 1 stage biasing arrangement

By powering on the bias circuit of stage X before stage X powers on however, the bias circuit of stage X can settle to a minimum accuracy before stage X is powered on as shown in Fig. 5-12.

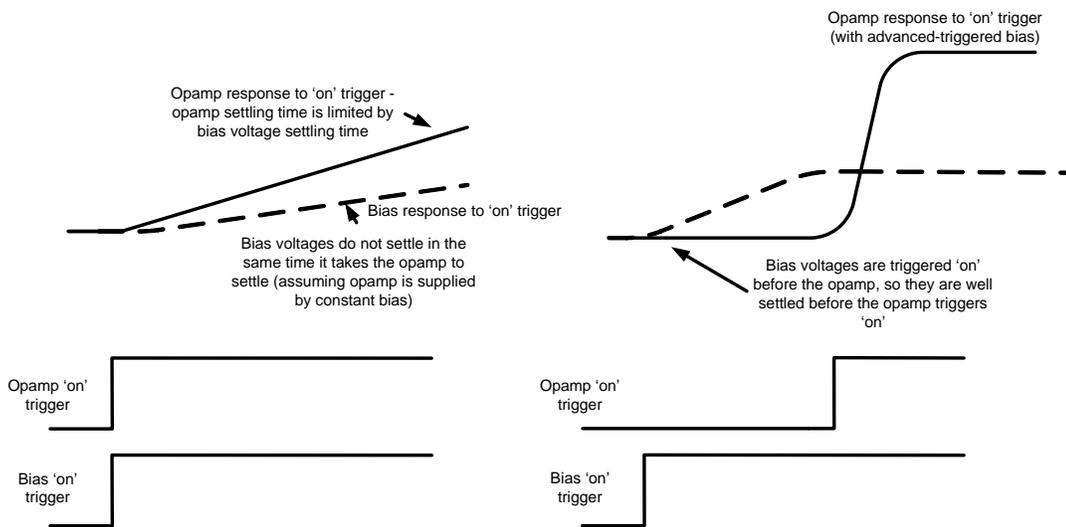


Fig. 5-12: illustration of different bias circuit on/off techniques

The additional setup time for the bias circuit however increases the minimum on time of the ADC, t_{ON} , as the bias for stage 1 is required before stage 1 becomes active.

In addition to the bias circuit, the ADC requires a clock generator and reference voltage generator. Although the digital state machine always requires a clock, the non-overlapping clocks required by the pipeline stages can be powered off during t_{OFF} . Turning off the clock generator during t_{OFF} can save a large amount of power as the non-overlapping clock

generator drives a large capacitive load, hence consumes a large average power when on (c.f. $P_{digital} \approx fCV^2$). To ensure the reference voltages have settled to a minimum accuracy, and the non-overlapping clock generator is fully powered on, the two blocks can be powered on a few clock cycles before the trigger to the first stage. As the digital error correction block only operates while the pipeline core outputs transitioning bits (i.e. is inherently a power scaleable block), an on/off trigger is unnecessary for the block.

Some analog blocks however cannot be powered on/off in a reasonable amount of time. One such block is a current mirror that receives an off-chip bias current as shown in Fig. 5-13 (I.e. constant current bias circuit – used in this dissertation to set on-chip bias currents).

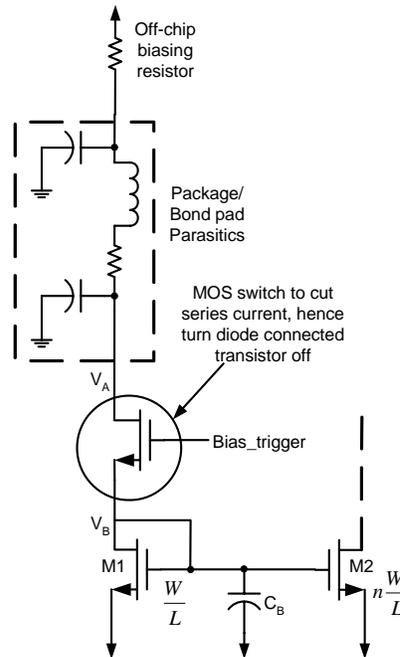


Fig. 5-13: An power on/off scheme for current mirror biased by off chip resistor

As node V_A in Fig. 5-13 has a large time constant, the settling time after an off to on transition can be excessive due to a large RC time constant/slew time from large bond pad capacitances and off chip resistance. To maintain stable on chip biases voltages, the diode-connected transistor must always remain on – which contributes to P_{static} thus limiting the maximum power scaleable range. The static power can be minimized however by supplying

only a small off chip current, where larger on chip currents can be generated on chip by appropriate mirror transistor sizing (e.g.: M2 in Fig. 5-13 has n times the drain-source current of M1) of current mirrors which can be powered on/off. The triggers signals for each major ADC block are shown in detail in Fig. 5-16. To simplify the bias on/off triggering, all bias circuits are activated on the same clock edge. A tradeoff of activating all bias circuits on the same clock edge is average power is increased. Future work could investigate optimizing the bias circuit timing such that a minimal power average is consumed. To save power and area, only three bias circuits have been designed for the ADC of this dissertation, such that one bias circuit serves three stages as shown in Fig. 5-14, where each bias circuit receives a reference current from a master current source set by an off chip current.

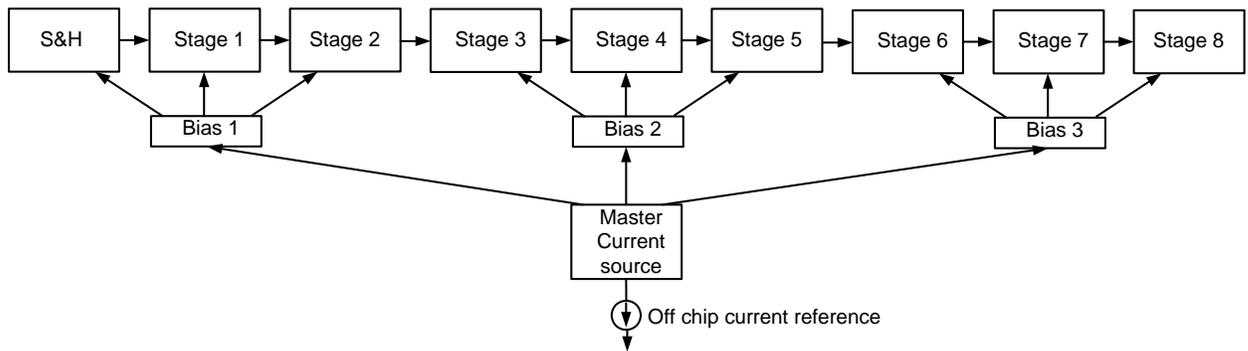


Fig. 5-14: Bias current routing for ADC in dissertation

The power of each bias circuit can be modulated by a series current switch (MS in Fig. 5-15), which cuts the DC current path between supplies.

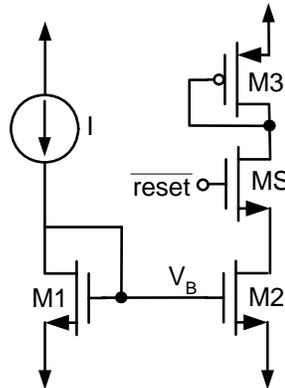


Fig. 5-15: Current switch 'MS' modulates bias circuit power

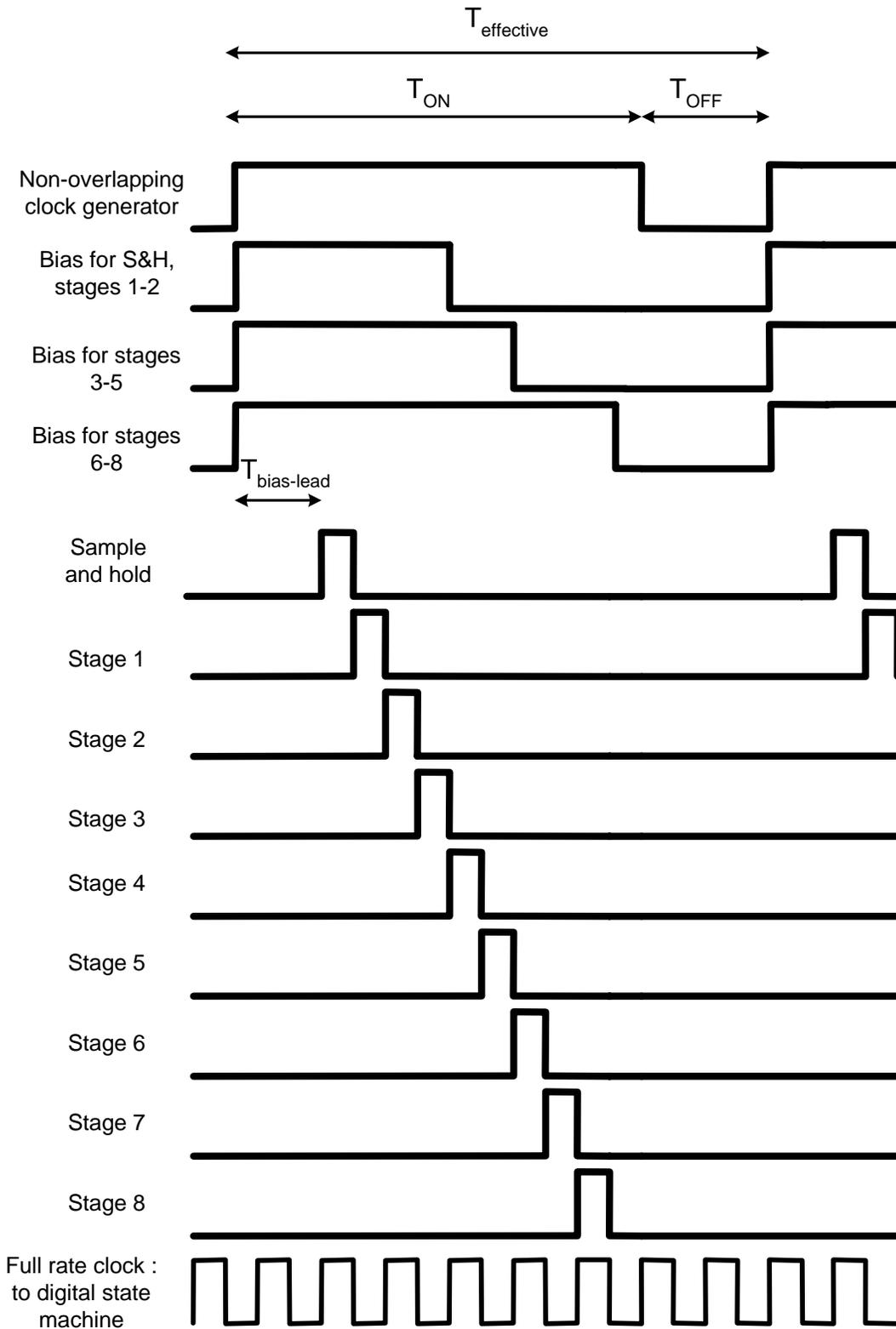


Fig. 5-16: detailed triggering diagram for pipeline ADC using CMPS (stage 9 does not require a power on/off trigger as it only consists of dynamic comparators)

5.7: Design of the digital state machine

A digital state machine is required to generate the control signals of Fig. 5-16, in uniform time intervals. By counting the number of clock edges of a full rate clock, precise timing of the control signals can be achieved. (E.g.): The on/off trigger for stage one is enabled when the counter counts to N, the on/off trigger for stage two is enabled when the counter reaches N+1, etc. Similarly the other control signals can be generated when the counter reaches a pre-programmed value. The effective sampling rate of the ADC can be controlled by resetting the counter after the counter has counted K clock cycles of the full rate clock. The effective sampling rate (the rate upon which the power scales with) is thus given by

$$f_{effective} = \frac{f_{fullrate}}{K}, \text{ i.e. } T_{effective} = KT_{fullrate} \quad (5.7)$$

Thus the effective sampling rate is not set by adjusting the off chip clock (full rate clock of Fig. 5-10), rather is digitally controlled by adjusting the value of ‘K’ in the state machine. For this dissertation the state machine was manually designed with a programmability, via serially loaded control bits, that allows for the adjustment of 1.) The effective sampling rate (i.e. the value of K), 2.) The lead setup time for the bias circuits, $t_{bias-lead}$ (as the exact bias lead time required is difficult to determine through simulation due to the many parasitic capacitors on the bias nodes in the layout). The counter used in the digital state machine was a synchronous 12-bit counter - limiting the lowest clock speed to $1/(2^{12}-1) = 1/4095$ the full-rate clock. For example, $50\text{MHz}/4095 = 12\text{kHz}$ if 50MHz provided to the state machine, $1\text{MHz}/4095 = 240\text{Hz}$ if 1MHz provided to the state machine. A system level diagram illustrating the state machine is shown in Fig. 5-17.

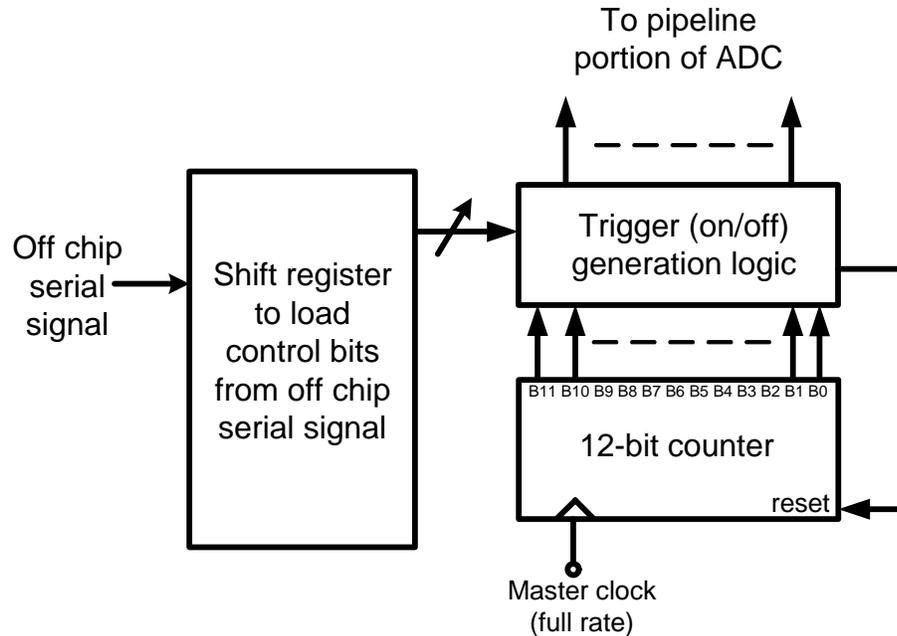


Fig. 5-17: system level diagram of on/off trigger generating digital state machine

The state machine power consumption at various full rate speeds is shown in Table 5-1. Since the state machine is always on, the power of the ADC is ultimately limited to at least the power of the state machine. However as the digital power consumed by the state machine is a function of the full rate clock in Fig. 5-17, if the clock rate is reduced, the state machine power can be reduced. Since the settling time of the MDACs in the pipeline is related to the period of the full-rate clock, for slower clocks supplied to the state machine, the bias currents supplied to the MDACs can be reduced to maintain an optimal figure-of-merit at the penalty of less inverted MOS transistor channels.

Table 5-1: Variation of digital state machine power with clock frequency

Frequency	Power
1MHz	~9.2 μ W
10MHz	~92 μ W
100MHz	~920 μ W

It should be noted that if the digital state machine were synthesized using commercial logic gates, the power could be significantly reduced (at least 2-5x), maximizing the power

scaleable range (A conservative digital design approach was taken to ensure functionality in this dissertation, where the state machine was manually designed).

5.8: Power resettable (on/off) opamps

As described in section 5.3, the CMPS technique requires an opamp that powers on and off in a short time interval (so as to maximize the sampling rate). Switched opamps, which short their differential outputs to a supply voltage, are similar in functionality to the desired power resettable opamp. Switched opamps are often used in low voltage applications [44], [45], [46], and are typically limited to less than 25Msps. To achieve fast settling times from when the outputs are reset, switched opamps typically do not completely power off. The techniques used in switched opamps to reset the output stage of an opamp however can be used to completely power on/off an opamp. The majority of switched opamps operate by switching bias voltages, or by series current switching. Sections 5.8.2-5.8.5 provide a brief overview of the implementation and design issues associated with each approach, as well as the replica bias approach used in this dissertation.

5.8.2: Switched bias opamp

Switching the bias voltages of current source transistors (M1 in Fig. 5-18) in opamps modulates the opamp current and hence power. The switched bias approach to power on/off (power reset) the opamp however has several design issues that lead to long power on/off times. Consider the schematic of Fig. 5-18, which shows the use of bias switching to achieve power on/off operation.

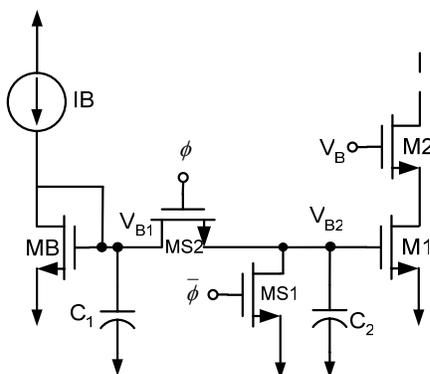


Fig. 5-18: switched bias approach to turn M2 on/off

The time required for the bias voltage (V_{B2}) to settle to the desired bias voltage (V_{B1}) is limited by the RC time constant of the switch network. Two key reasons keep the time constant large in the network of Fig. 5-18. Firstly as bias voltages are required to stay constant during nominal operation, large decoupling capacitors C_1 , and C_2 , are typically connected to V_{B1} and V_{B2} respectively. Furthermore as mirror transistors tend to be large in area (to minimize mismatch, or introduce a current gain), large parasitic capacitances exist on the bias nodes. The second design limitation is the inverse dependency of the switch resistance on V_{eff} (c.f: $r_{ds} = (\mu C W L^{-1} V_{eff})^{-1}$). If the bias voltage to be passed by the switch network is such that V_{eff} of the switch transistor (while it is on) is near zero, $r_{ds} \rightarrow \infty$, hence increasing the RC time constant which limits the maximum sampling rate.

When ϕ switches from low to high in Fig. 5-18, a discharged C_2 is placed in parallel with a charged C_1 , temporarily causing the voltage at V_{B1} to dip to $C_1/(C_1+C_2)V_{B1-steady\ state}$ due to charge sharing. For V_{B1} and V_{B2} to settle to $V_{B1-steady\ state}$, V_{B1} slews to the correct voltage according to the total capacitance of C_1+C_2 , and the difference in current of I_B and that drawn by M_B . The slewing current is small, and C_1+C_2 is large, thus the slew time can be very long (consider that for this work when CMPS is enabled at the highest operating speed the opamps have less than $1/50\text{MHz}/2=10\text{ns}$ to settle to at least 10-bit accuracy). Alternatively C_1 can be made very large (which consumes area) to minimize the amount V_{B1} dips when shorted to V_{B2} through MS_2 . However, if C_1 is made very large (e.g. 10's of pF),

the slew rate at V_{B1} becomes very low, and thus although the dip in V_{B1} becomes small, V_{B1} never settles as it continually slews during ϕ . With mismatches between positive and negative halves, and asymmetric parasitic capacitances in a fully differential opamp, if the bias voltages to it slew, the differential output of the opamp also never settles, thus affecting the settling accuracy of the switched capacitor circuit which is of paramount importance in a 10b pipeline ADC.

5.8.3: Replica bias based Power Resettable Opamp (PROamp)

The settling times of master bias voltages (the bias voltage generated by diode-connected transistors) have been shown to limit the minimum power on time of opamps when using a switched bias/bias reset scheme to modulate opamp power. If however the master bias voltages could be held constant while the opamp is powered on/off, the opamp power on/off time could be significantly reduced. A solution to this problem is achieved by utilizing replica biasing. With replica biasing it is possible to copy a bias voltage from one node to another as shown in Fig. 5-19.

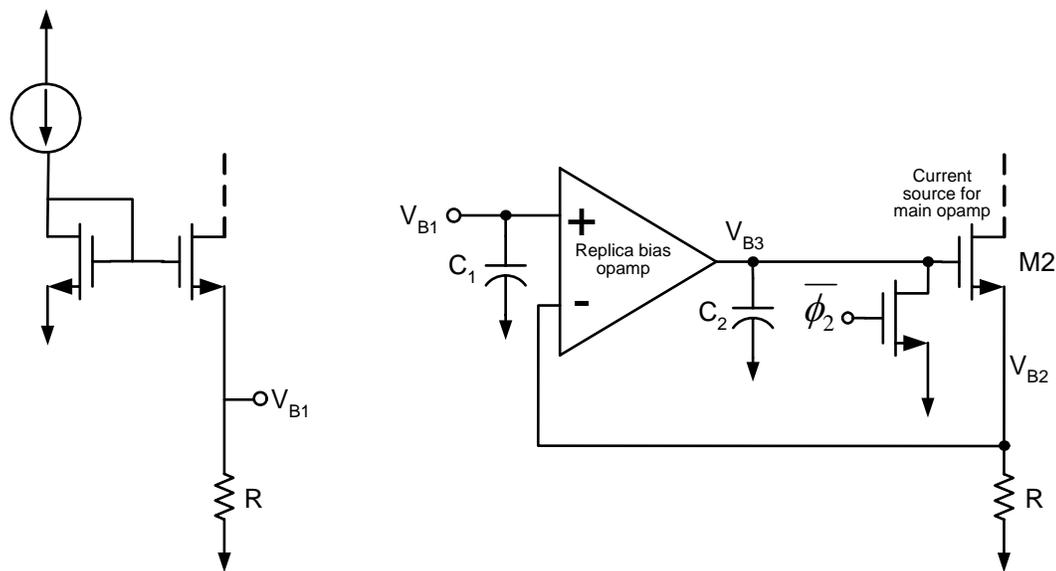


Fig. 5-19: replica bias switching

By virtue of negative feedback, $V_{B2} \approx V_{B1}$, and due to the large input impedance of the opamp, V_{B2} , and V_{B3} are well isolated from V_{B1} (and vice-versa). Thus switching V_{B3} to modulate the current of M2 minimally disturbs V_{B1} . Furthermore, as V_{B3} is isolated from V_{B1} , the RC time constant/slewing time at V_{B3} is minimal, as V_{B3} does not share any parasitic and decoupling capacitance with other bias nodes. Also charge sharing effects from switching at node V_{B3} do not affect the bias source (V_{B1}), thus avoiding excessive settling times as described in section 5.8.2. Thus, V_{B3} can be switched quickly without disturbing V_{B1} .

For the CMPS technique however, the entire analog core must power off for a fixed time interval, thus the replica bias opamp must also power off. On the surface using an opamp to shorten the on/off time of another opamp seems like a cyclical argument, however by exploiting the different performance requirements of the main opamp (i.e. the opamps used in the MDACs) and the replica bias opamp (the opamp used to shorten the power on time of the main opamp), a power reset (power on/off) mechanism for the replica bias opamp can be used without disturbing the bias voltages. Consider the switching scheme of Fig. 5-20 to power reset an opamp:

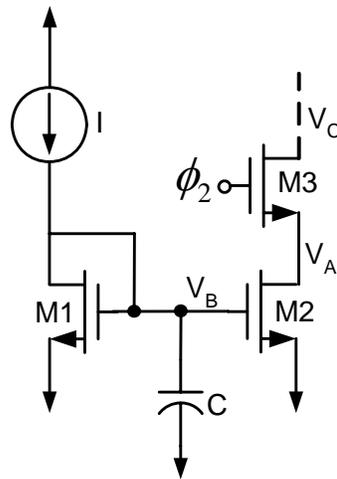


Fig. 5-20: series switching to turn M2 on/off

The series switch approach shown in Fig. 5-20 avoids perturbing the bias voltages, as the switch transistor $M3$ switches current rather than the bias voltage. Current switching is often

used for low power switched opamps [46]. Current switching only depends on the time required to toggle the switch transistor from cut-off to triode, thus is very fast and much faster than bias switching approaches, as the gate of the switch transistor requires no decoupling capacitance, thus has a small RC time constant. Current switching however reduces the available signal swing due to an IR drop across the switch transistor when in triode, which can be significant. (E.g.) a low triode resistance for a switch is 100Ω . If the current to be switched is 1mA, the IR drop is 100mV, which is excessive for a 1.8V supply, where signal swings tend to be 500mV-1000mV (single-ended). Thus the current switch method is not preferable in opamps where large bias currents are used and/or a large signal swing is required (i.e. the main MDAC opamp). Series current switches, which are designed with the intention of operating in the triode region, can shift to the active region for sufficient signal swings. For differential opamps where when one output is at a maximum the other is at a minimum, series current switches in the output stage of an opamp can lead to the switch being in active for only one half of the circuit, which leads to a degradation of circuit symmetry and thus power supply noise rejection. The replica bias opamps however, drive a much smaller load (in comparison to the main opamp) thus have lower bias currents, and only require a small output swing (since the output need only include the variation of the bias voltage - which is very small), hence can tolerate a reduction in available signal swing. Furthermore since the replica bias opamps are single ended, they do not require differential symmetry. Thus current switching can be applied to the replica bias opamps as shown in Fig. 5-21, where the trigger signal to power on/off the replica bias opamp are applied to node 'reset'.

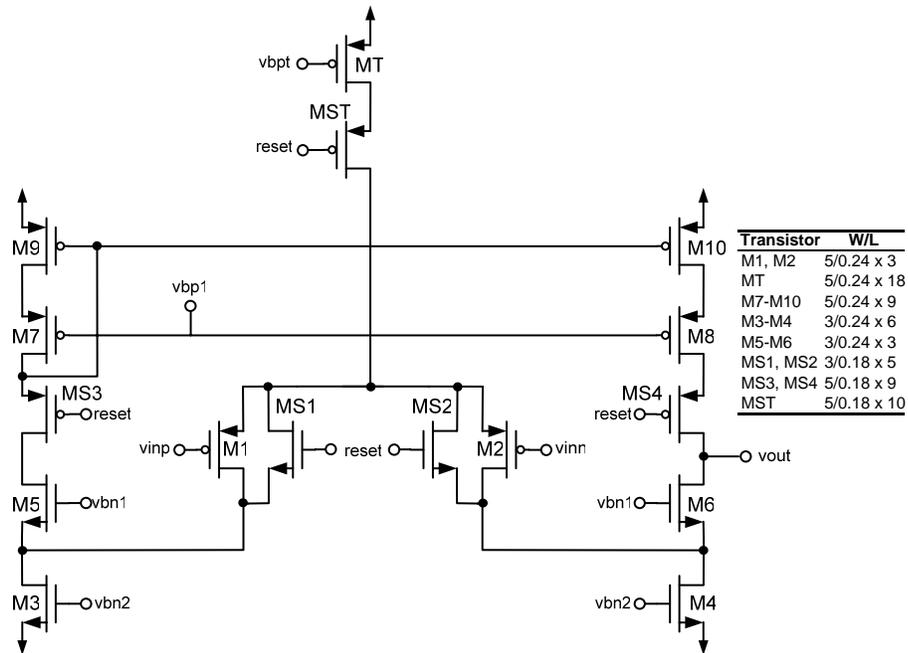


Fig. 5-21: replica bias opamp with current switching

The on/off time of the replica bias approach can be adjusted by minimizing the RC time constant at node V_{B3} in Fig. 5-19, and/or by increasing the bandwidth of the replica bias opamp. (c.f.: the time constant of a closed loop opamp is g_m/C_{load} , hence the settling time can be controlled by exchanging power for speed). Thus by combining different power on/off techniques - replica bias in the main opamp and current switching in the replica bias opamp, a short on/off time can be achieved. Furthermore as the main opamp power on/off time is very small, the opamp can be completely powered on/off very quickly as opposed to most switched opamp designs which only power a portion of the opamp off to achieve faster sampling rates [45], [46].

5.8.4: Benefits of replica biasing: Increased output resistance

A drawback of the replica bias approach is an increased power consumption to power the replica bias opamps. However, replica biasing serves to increase the output resistance of the opamp transistor as shown in Fig. 5-22:

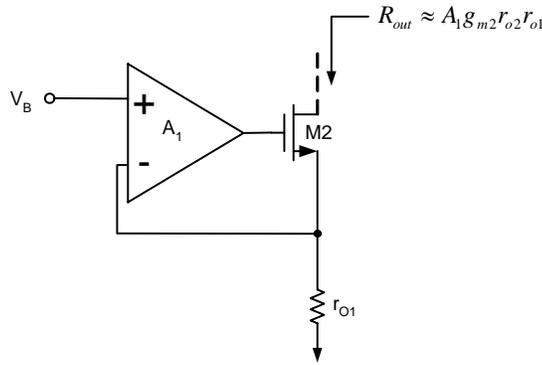


Fig. 5-22: increased output impedance through replica biasing

Replica biasing can be arranged in a gain-boosting configuration [49], such that a large gain can be achieved in the main opamp using only a single stage architecture. From section 3.4, a large gain is a necessary requirement for a 10-bit pipeline architecture, thus using a replica bias approach is doubly beneficial. By combining the replica bias switching approach with a folded cascode opamp, a gain-boosted single stage opamp with short power on/off times, and large DC gain results as shown in Fig. 5-24 (where signal *reset* powers on/off the opamp, and SRBO is the *Switched Replica Bias Opamp* of Fig. 5-21 for NMOS gain boosting, and the opamp of Fig. 5-23 for PMOS gain boosting.):

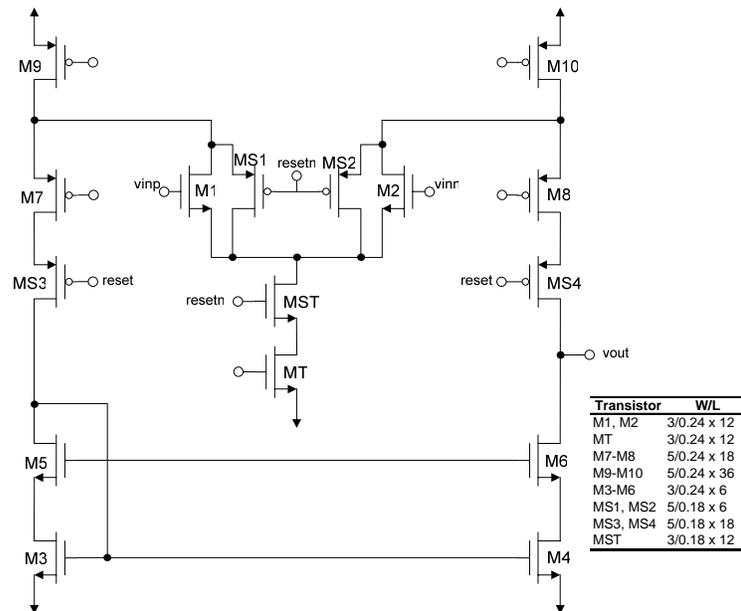


Fig. 5-23: PMOS gain boosting opamp

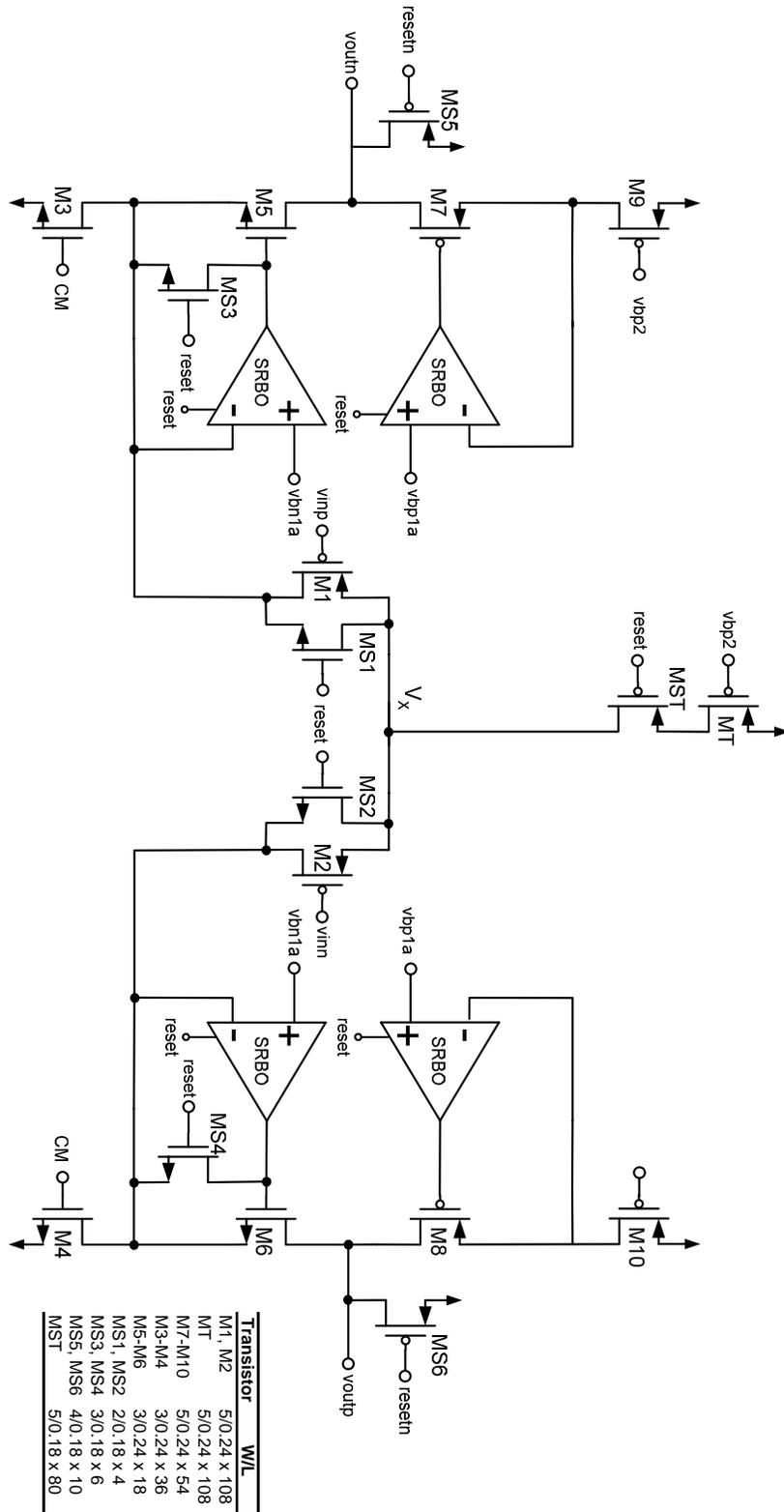


Fig. 5-24: high gain replica biased based switched opamp (note replica bias amps are switched)

As the replica bias opamps provide increased opamp gain, the additional power required to power the replica bias opamps is minimal as cascaded gain stages (thus more complicated compensation schemes) to achieve large gain are avoided.

A folded cascode architecture is beneficial as it allows the opamp input common mode to include ground. With an input common mode near ground, it is possible to use the current switch technique on the tail current transistors as a large IR drop can be tolerated across transistor MST (in Fig. 5-24) while maintaining the input differential pair in saturation. Transistors MS3 and MS4 are used in parallel with the replica bias opamp to shorten the off times of M5 and M6. MS1 and MS2 are used to set node V_X to a defined voltage during the power off state. MS5 & MS6 quicken the opamp-reset time, pulling the outputs to V_{DD} as required by the *Common Mode Feed Back* (CMFB) circuit (section 5.9). The opamp was biased such that the differential output swing was at least 1.6V with the maximum bias current (i.e. when ADC is operating at its maximum speed there is 0.8V signal swing available from each of voutp and voutn over process and temperature corners).

In Fig. 5-25, and Fig. 5-26 the transient responses of two approaches to power reset the opamp are compared. The simulation shows the transient response of an MDAC using the replica bias opamp of Fig. 5-24, and an MDAC using a folded cascode opamp where the bias voltages to the opamp are switched as shown in Fig. 5-18, with multiple opamps sharing the same master bias. From the figures it is clear the replica bias approach provides fast on/off times facilitating fast sampling rates.

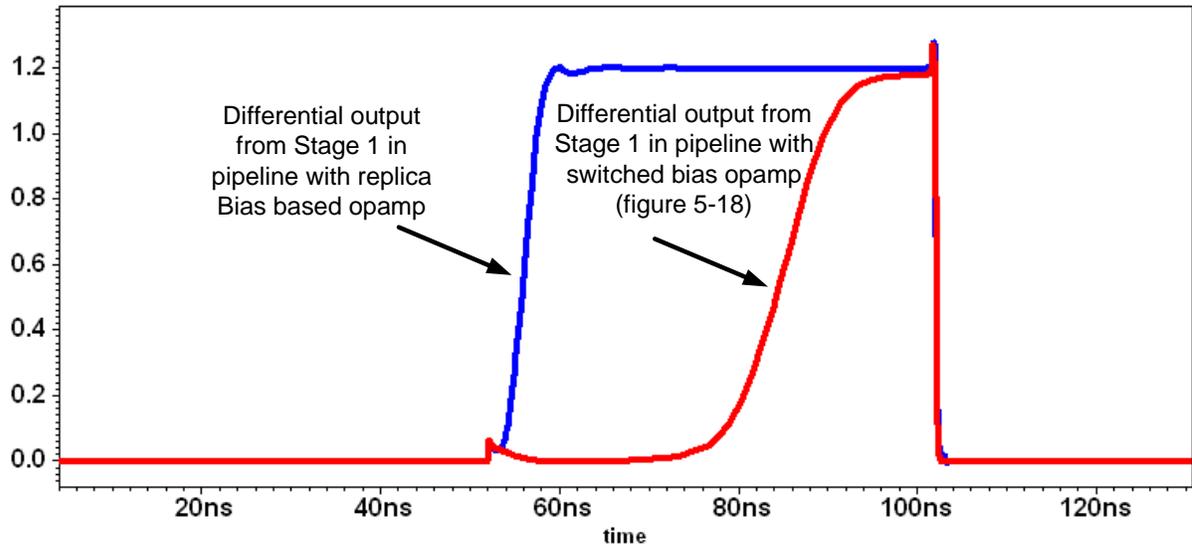


Fig. 5-25: SPICE simulation comparing different switching approaches

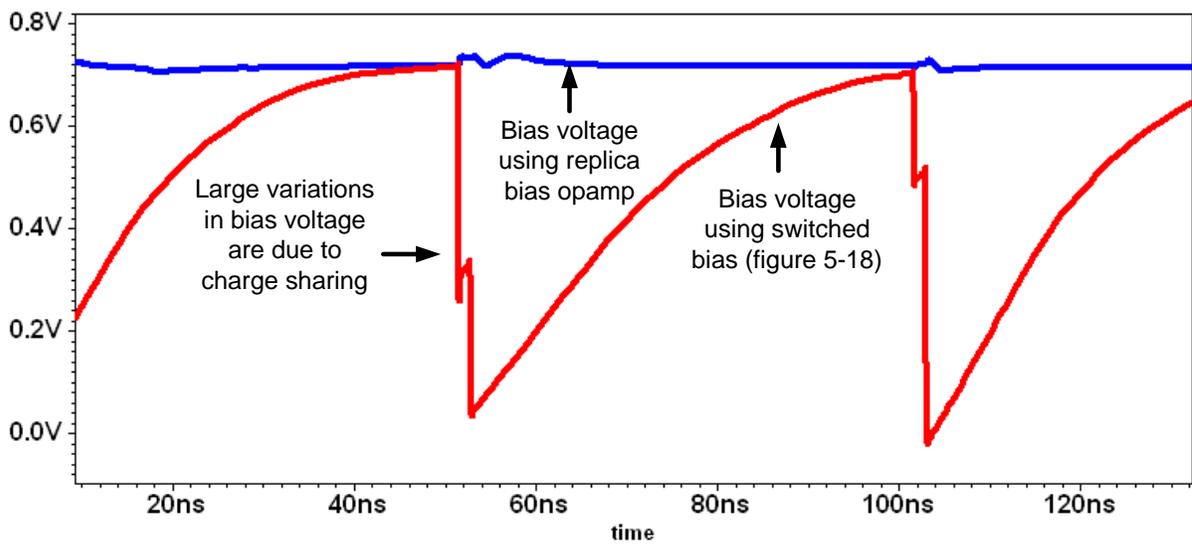


Fig. 5-26: SPICE simulation showing impact of switching architecture on bias voltages

5.8.5: Opamp specification/characterization

As described in sections 3.4-3.4.2, the opamps for each stage in the ADC pipeline require a minimum DC gain and bandwidth to achieve 10-bit accuracy. Ideally each stage would be

uniquely designed such that the required gain/bandwidth specifications are just met to minimize area and power. However, scaling each stage requires the design and layout of eight unique opamps for a 1.5-bit/stage 10-bit pipeline ADC. As the goals of this dissertation more favor proof-of-concept over absolute performance specifications, stage opamps were scaled in groups rather than individually as shown in Fig. 5-27.

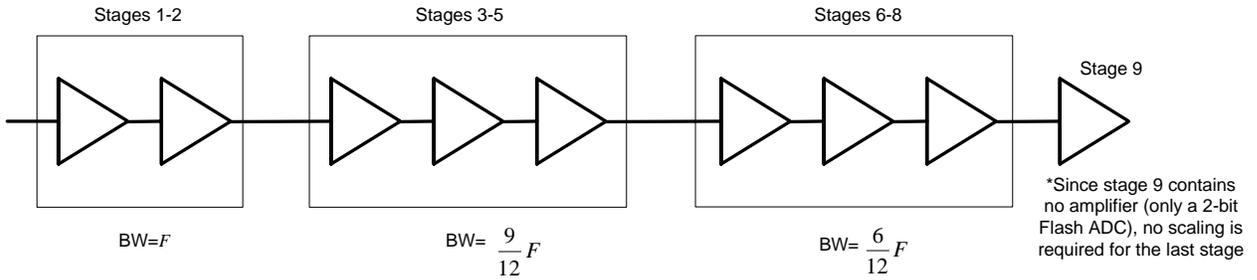


Fig. 5-27: stage grouping for scaling

To achieve 10-bit accuracy at a sampling rate of 50MSPs, the stage opamps were designed with the DC-gain and unity gain bandwidths shown in Table 5-2. From Fig. 4-6, as bias currents are reduced opamp gains increase. Thus for lower sampling rates where the bias currents are decreased (to allow for a hybrid CMPS technique as described in section 5.5), only the unity gain bandwidths are decreased. For lower sampling rates the minimum ADC power can be determined by decreasing the power until the ADC accuracy begins to reduce due to bandwidth limitations.

Table 5-2: MDAC Opamp DC gain and bandwidth for 50MSPs operation

Stages	DC Gain	Maximum Unity Gain	Desired Relative Unity Gain	Phase Margin	MDAC sampling/feedback capacitor	Effective opamp load	Opamp Power
1, 2	105dB	563MHz	f	75°	0.5pF	1.4pF	7.8mW
3, 4,5	73dB	515MHz	$\frac{9}{12}f$	62°	0.1pF	0.36pF	3.3mW
6, 7,8	52dB	297MHz	$\frac{6}{12}f$	80°	0.05pF	0.23pF	1.1mW

Reduced opamp gain for latter stages in the pipeline is achieved by removing the switched replica bias opamps as shown in Fig. 5-28, and Fig. 5-29. Note the stage opamps for stages 6 to 8 use series current switching, as the opamps in stages 6 to 8 require lower bias currents, and require less SNR, thus can tolerate a smaller signal swing.

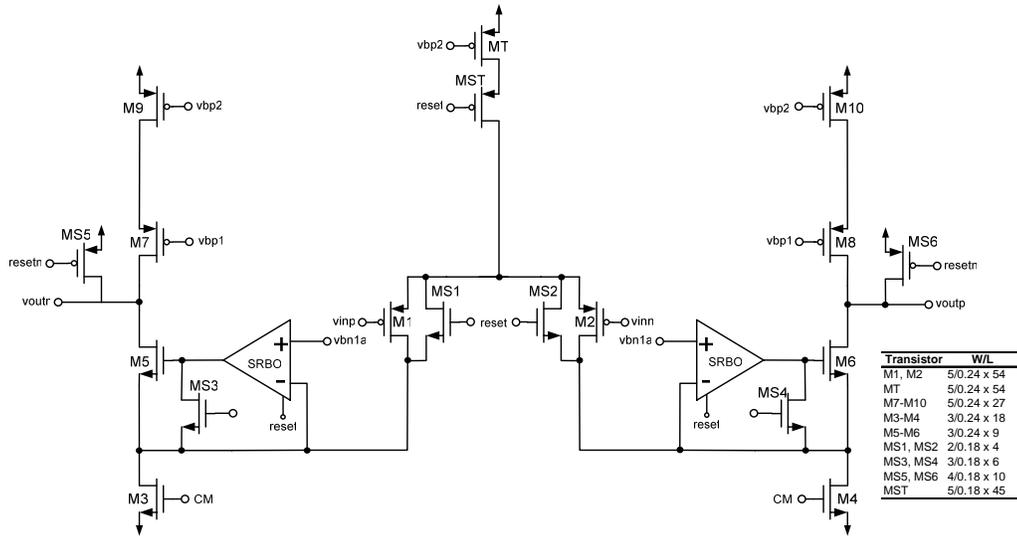


Fig. 5-28: opamp for stages 3-5

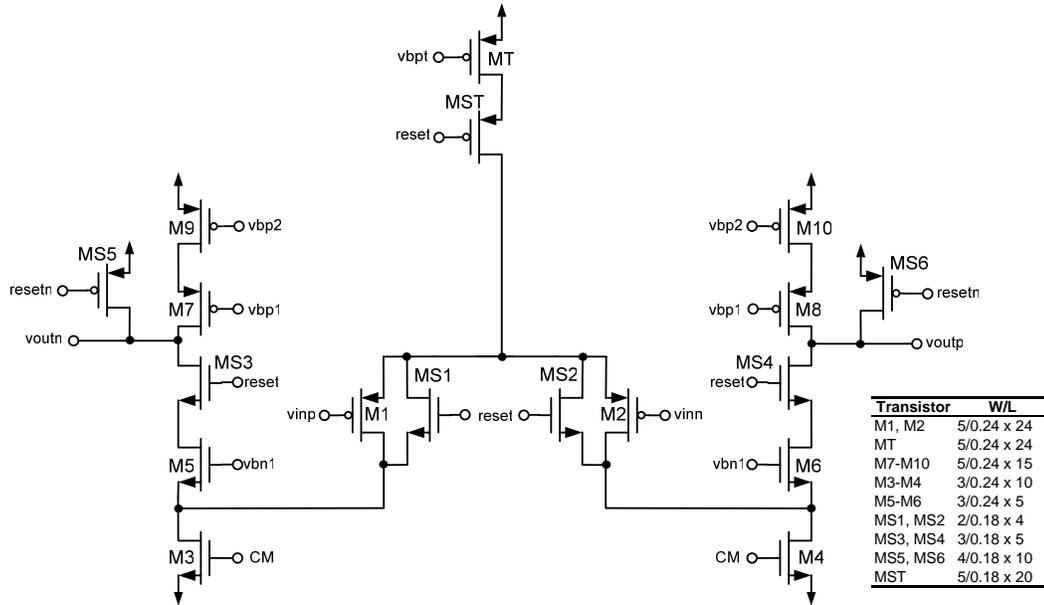


Fig. 5-29: opamp for stages 6-8

As mentioned in section 5.8.4, a benefit of the replica-bias/gain boosted architecture is the avoidance of complicated compensation structures. As the opamp has essentially a single stage architecture, simple load compensation can be used to achieve a minimum phase margin. An added benefit of load compensation is any additional parasitic capacitance that is not accounted for in simulation, but manifests in the layout process only serves to enhance the phase margin [18].

The bandwidths of the switched replica bias opamps have been tuned through simulation such that the closed loop response is stable and short settling times result. The replica bias opamps setting the bias voltage of the NMOS transistors are biased with $1/6^{\text{th}}$ the bias current of the main opamp and the PMOS replica bias opamp biased with $1/3^{\text{rd}}$ the bias current of the main opamp.

A Monte Carlo Analysis was performed in SPICE to determine opamp bandwidth variation as bias current is reduced. The relative variation ($3\sigma/\text{mean}$) bandwidth as the opamp tail current is decreased is shown in Fig. 5-30. The larger variation as current is decreased verifies the predicted poorer matching as the opamp is driven deeper into the weak inversion region of operation.

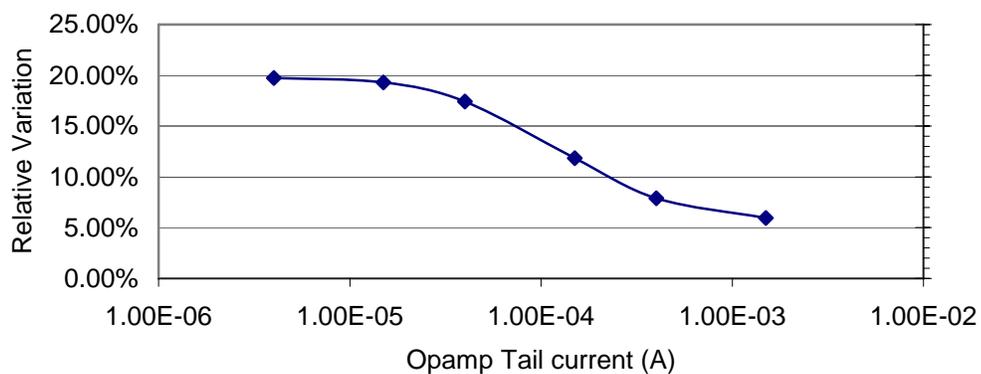


Fig. 5-30: relative variation ($3\sigma/\text{mean}$) of opamp bandwidth vs. tail current of opamp in Fig. 5-24

5.9: Common Mode Feed Back (CMFB) for PROamp

One of the requirements of CMPS (according to the triggering diagram of Fig. 5-16) is to have the MDAC output fully settled within one clock cycle after the stage trigger signal is enabled. Typically switched capacitor circuits use a switched capacitor CMFB (Fig. 5-31) circuit which takes several clock cycles to generate the correct common-mode in the output [3] - clearly not feasible for a pipeline ADC using CMPS.

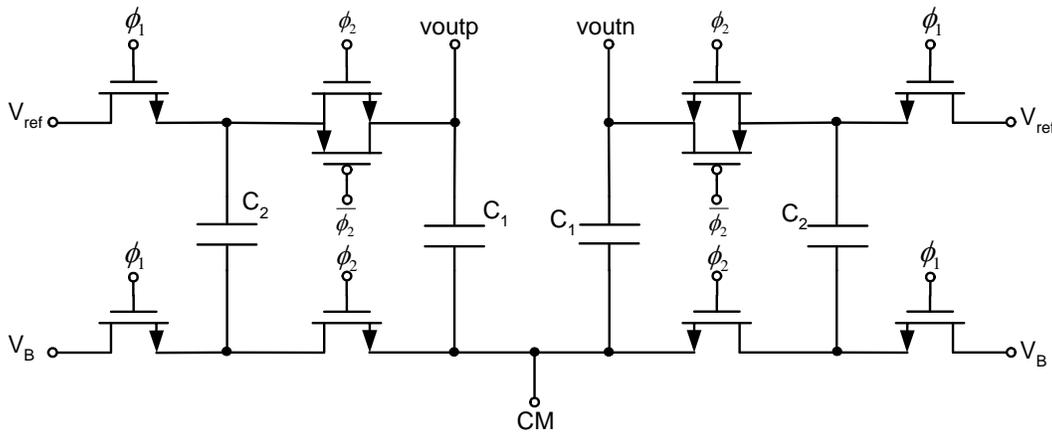


Fig. 5-31: conventional passive switched capacitor CMFB circuit

The CMFB circuits of switched opamps however, can be used as switched opamps have differential outputs, which settle within one clock cycle after a reset phase where the opamp outputs are shorted to a supply voltage. CMFB approaches for switched opamps fall into passive [46] and active [45], [50] categories. Active CMFB approaches have the advantage of settling to a common mode voltage defined by a known reference voltage, but have the penalty of additional power consumption to power the active circuitry. Passive approaches achieve the desired common-mode level by charge conservation, and thus have a common mode voltage that is sensitive to parasitic capacitances of the CMFB circuit. Passive CMFB however has the advantage of only consuming dynamic power as no active circuitry is used. In the interest of minimizing power, and avoiding the design of a power on/off mechanism for an active CMFB circuit, a passive CMFB approach has been taken for opamps of this dissertation. The passive CMFB approach used is shown in Fig. 5-32, and exploits charge conservation to set the output common mode to $V_{DD}/2$ [46].

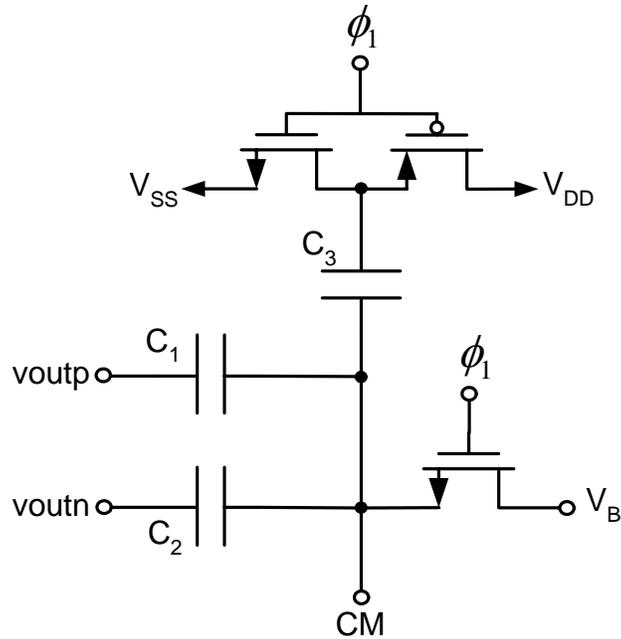


Fig. 5-32: passive switched capacitor circuit for switched opamps

For the circuit of Fig. 5-32, during ϕ_1 (reset phase: $v_{outp}=v_{outn}=V_{DD}$), assuming $C_1=C_2=C_3$:

$$Q_{C1} = Q_{C2} = C(V_{DD} - V_B) \quad (5.8)$$

$$Q_{C3} = -CV_B \quad (5.9)$$

and during $\overline{\phi_1}$:

$$Q_{C1} = C(V_{outp} - V_{CM}) \quad (5.10)$$

$$Q_{C2} = C(V_{outn} - V_{CM}) \quad (5.11)$$

$$Q_{C3} = C(V_{DD} - V_{CM}) \quad (5.12)$$

$$\therefore \text{Charge is conserved: } V_{DD} - 3V_B = (V_{outp} + V_{outn}) - 3V_{CM}$$

If V_B is set to approximately the intended value of V_{CM} (determined through desired bias

current): $\Rightarrow \frac{(V_{outp} + V_{outn})}{2} = V_{output=CM} = \frac{V_{DD}}{2}$

5.10: Power reduction through current modulation

As described in section 5.8, the PROamp developed for the power scaleable ADC has the advantage of short power on/off times due to a bias isolating-replica bias architecture. An application of the PROamp beyond the application to a power scaleable ADC using CMPS is in general using the PROamp in applications where analog blocks requiring opamps do not always need to be powered on. For example, in the case of a general 10-bit pipeline ADC (with 1.5 bits/stage), in the MDAC there are two operating modes, which depend on the clock phase. During one clock phase the MDAC samples the input, and during the following clock phase the MDAC holds a multiplied by two value of the input (see section 3.2). During the sampling phase a virtual ground is not required, hence the MDAC opamp is also not required during this clock phase. If the opamp is powered off during the sampling phase, the average MDAC power can be reduced by the fraction of time it is off over the total time the MDAC is operative. Ideally powering off the opamp for half a clock cycle affords a reduction in opamp power (which is a large portion of the entire ADC power) by 50%, thus allowing for substantial reductions in analog power consumption as shown in Fig. 5-33.

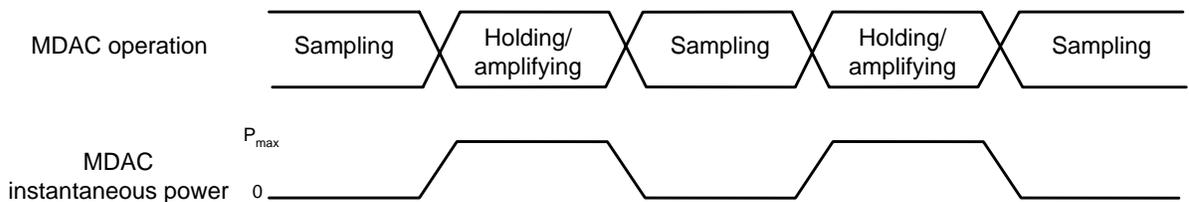


Fig. 5-33: Illustration of MDAC Power reduction using PROamp

Although powering off portions of opamps to reduce power is commonly used in low voltage applications using switched opamps, the approach is not typically used for higher voltage and higher speed applications. Furthermore as the opamp completely powers down, the power reduction is higher than publications where a portion of the opamp is kept on to allow for a short on/off time [45], [46]. Simulations show nearly identical *Signal to Noise + Distortion Ratio* (SNDR) performance of an MDAC with and without PROamps for sampling frequencies beyond 50Msps.

As the PROamp allows for reduced power consumption in pipeline ADCs, the MDACs of the pipeline in this dissertation have been designed to only power on during the hold phase, when using the hybrid CMPS power scale technique, thereby reducing power consumption. To evaluate the power reduction afforded by powering off the MDACs during the sampling phase, an additional mode of operation has been designed, where the opamps are never powered off, i.e. the ADC operates as a conventional pipeline ADC. Thus the ADC has three modes of operation:

Mode 1 (*power scaleable mode*): Pipeline ADC uses CMPS to allow for power to be scaled with sampling frequencies for low sampling rates, but has a maximum sampling rate limited by the pipeline latency as described in section 5.5. The MDAC opamps are only powered on during the hold phase

Mode 2 (*power reduction mode - PRM*): Pipeline ADC uses pipeline architecture to operate at maximum speed. Current scaling is used to reduce power with sampling frequency over a narrow range of sampling rates not covered by CMPS as described in section 5.5. To minimize power consumption the MDAC opamps are powered off during the sampling phase, exploiting the short on times of the PROamp.

Mode 3 (*nominal mode - NM*): Same as Mode 2, except the MDAC opamps are always powered on.

Thus by measuring the ADC power in power reduction mode and nominal mode, it is possible to determine the amount of power savings afforded by powering off the MDAC opamps during the sampling phase. It is not possible to compare the power of nominal mode with power scaleable mode as the power scaleable mode explicitly requires opamps to power off to achieve power scaleability.

The exact mode of ADC operation is set via off chip control bits. The MDAC opamps in power reduction and power scaleable modes are powered on at the same time the advanced sampling clock of the MDAC bottom plate samples, to ensure the opamp is powered on

before a virtual ground is required. Thus the opamps are on for larger than 50% of the period (i.e. $T/2 + t_{non-overlap}$). For higher sampling rates ($>50\text{Mps}$) where $t_{non-overlap}$ (shown in section 5.15 to be 1.4ns) is comparable to $T/2$, the effect of power reduction is less pronounced, as the opamps are powered off for a shorter portion of the clock period. A more aggressive design can significantly reduce $t_{non-overlap}$, thus allowing for near 50% reduction in opamp power for higher sampling rates.

It should be noted that in several high speed analog applications there exist idle time slots where opamps are not required (e.g. discrete time filters, sample and holds, etc.). By using PROamps in such applications it is possible to significantly reduce the analog power by completely powering off the opamps when not required.

5.10.2: Common Mode Feed Back (CMFB) for different opamp modes

As described in section 5.10, the ADC of this dissertation operates in three modes. As such the CMFB must facilitate the various constraints in each mode: in power scaleable and power reduction modes, the CMFB of Fig. 5-32 can be used, whereas in nominal mode, the opamps are always on, thus do not have a reset phase hence cannot use the CMFB of Fig. 5-32. For nominal mode operation, a conventional switched capacitor CMFB structure of Fig. 5-31 is required. To allow for a single CMFB circuit to work for all desired operating modes, a reconfigurable CMFB circuit can be used which changes its structure depending on the mode of ADC operation. In Fig. 5-34, ϕ_1 and ϕ_2 are connected to the non-overlapping clocks required for the MDAC via a mux, when the ADC operates in nominal mode. When the ADC operates in power scaleable and power reduction modes, ϕ_1 and ϕ_2 are connected to VSS, and ϕ_{1B} and ϕ_{2B} are connected to the non-overlapping clocks required for the MDAC via a mux.

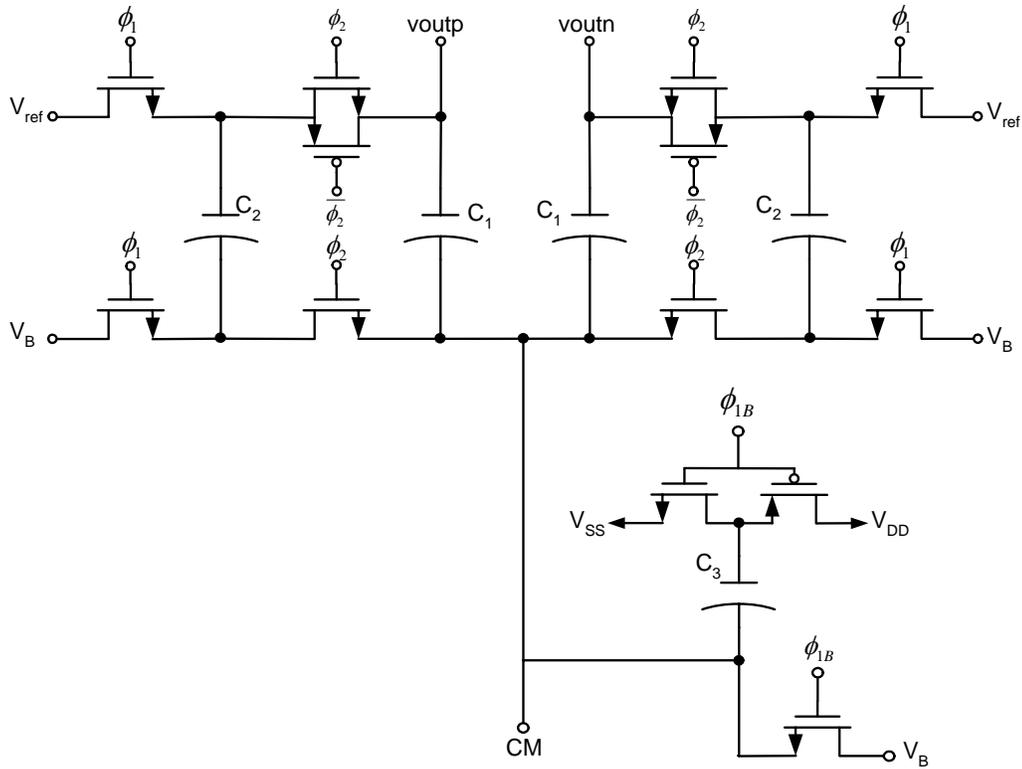


Fig. 5-34: hybrid switched capacitor CMFB circuit

5.11: Sample and Hold (S&H)

The ADC and MDAC of stage one must operate on the same input to correctly set stage two. For higher input frequencies a skew can manifest between the stage one MDAC and stage one ADC if the input is directly applied to the first stage. For higher sampling rates (as is the case in this dissertation), a *Sample and Hold* (S&H) should be used before the first stage to eliminate skew between the stage MDAC and ADC, as skew can cause the stage MDAC and ADC to operate on different values, resulting in accuracy degradation. Placing a sample and hold before stage one allows for the input to stage one in the pipeline to be a discrete time signal which guarantees the MDAC and ADC of stage one operate on the same value if enough time is given to allow the sample-and-hold output to settle to at least 10-bit accuracy. The architecture of the front-end S&H is similar to the MDAC S&H, except the gain is one and is shown in Fig. 5-35. Although it is shown single ended for simplicity, in the fabricated ADC a fully differential architecture has been used for the S&H.

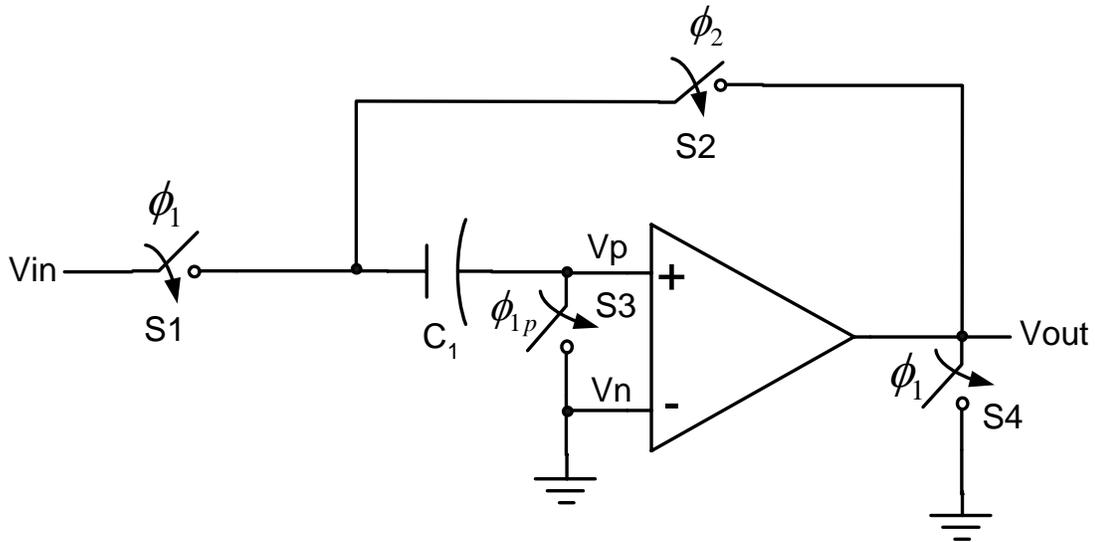


Fig. 5-35: input sample and hold (comes before stage 1)

As the S&H is the first stage in the pipeline, the S&H opamp bandwidth must be at least that of the first stage. To minimize the design/layout time, the opamp used in stage one is reused in the S&H. A transmission gate was used for S1, where the MOS switch sizes were sized to such that the S&H had an SNR > 72dB for input frequencies greater than 50MHz (NMOS W/L = 2/0.18 M=30, PMOS W/L=4/0.18 M=30). Simulations showed sufficient SNR using transmission gates for the input switch S1, thus more complicated gain-boosting techniques were not used.

5.12: MDAC

The MDAC of Fig. 3-2 (in fully differential form) was used for the pipeline ADC due to the large feedback factor, hence fast transient response, and good matching (due to the identical capacitor sizes). The sizes used for the sampling and feedback capacitors are listed in Table 5-2. To maximize capacitor matching, and minimize absolute variation, MIM capacitors were used. Switches for the MDAC were sized to meet the minimum RC time constant for the maximum sampling frequency (>50Mps), where transmission gates were used if the signal to be passed included $V_{DD}/2$.

5.13: Stage comparators

As digital error correction allows for less accurate comparators in pipeline stage ADCs, dynamic comparators were used in this dissertation. In addition to consuming less power than active comparators, dynamic comparators have the advantage of being inherently power scaleable, thus do not require power on/off trigger signals.

From section 2.7.2 the comparator offset must be less than $V_{ref}/4$, which for $V_{ref}=0.8V$ implies the comparators have an offset less than $0.8/4 = 200mV$. To ensure a high design yield, the lower-offset charge sharing comparators (Fig. 3-9) have been used for this dissertation. A Monte Carlo analysis of both comparator architectures discussed in section 3.5, verify the published results of [21] and is shown in Fig. 5-36-Fig. 5-37. The Lewis and Grey comparator was found to have an offset variation of $\sigma=94mV$ (i.e. $3\sigma=282mV$), whereas the charge sharing comparator was found to have an offset variation of only $18mV$ (i.e. $3\sigma=54mV$).

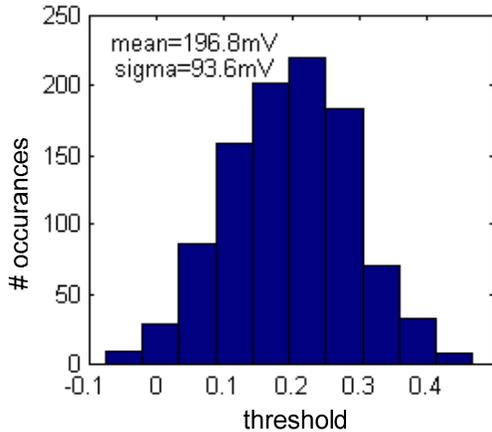


Fig. 5-36: Monte Carlo analysis of Lewis and Grey comparator

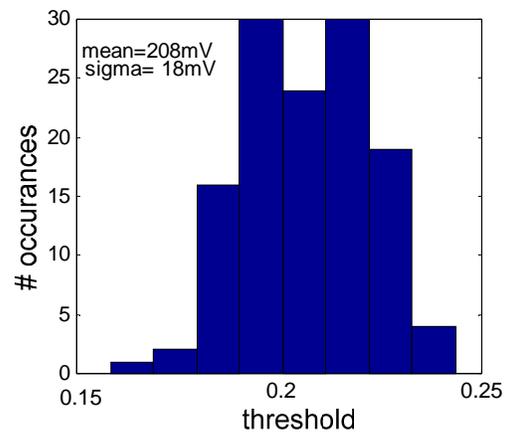


Fig. 5-37: Monte Carlo analysis of charge sharing comparator

From Fig. 3-9, C_{in} and C_{ref} were set to $64fF$ and $16fF$ (minimum sized MIM cap) respectively for comparators where a threshold of $\pm V_{ref}/4$ was required. $32fF$ and $16fF$ were used for C_{in} and C_{ref} when a threshold of $\pm V_{ref}/2$ was required (in the last stage of the pipeline: 2-bit flash).

5.14: Bias circuits

From Fig. 5-24 opamp bias circuits are required to provide a cascode bias to each opamp. Bias voltages for cascode opamps are typically derived from wide-swing cascode current mirrors [3]. As mentioned in section 5.5 however, a small amount of current scaling is used in this design so as to provide a continuous power scaleable range. The ADC should also be able to be biased deep in weak inversion so that the problems of increased bias-point sensitivity and mismatch can be empirically measured. As such the bias circuit must keep M2 and M3 in Fig. 5-38 in the active region regardless of the bias current (and thus level of channel inversion).

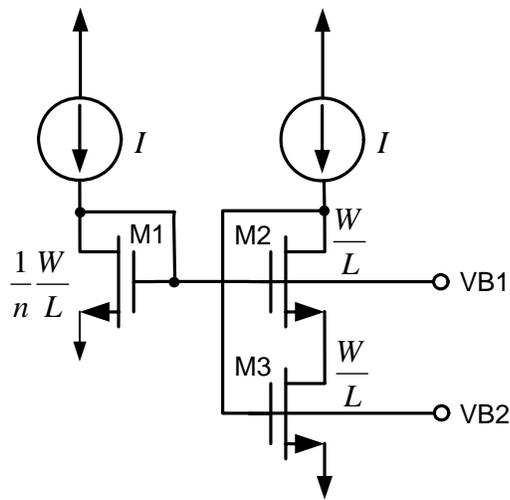


Fig. 5-38: Wide swing cascode current mirror(n is typically > 4)

In [1] a wide swing cascode bias circuit (Fig. 5-38) is shown to ensure the opamp cascode transistors remain active so long as one of M2 and M3 are in strong inversion. If both transistors fall into weak inversion however (which is inevitable for a sufficient current scaling), the required ratio of W_{M1}/W_{M2} to maintain both M2 and M3 in saturation would be prohibitive [1]. Subsequently rather than using a diode-connected transistor to bias M2, an alternative biasing network must be used to maintain active operation over wide variations in current. An alternative architecture that provides active cascode biasing that is independent of bias current is presented in [51], and illustrated in Fig. 5-39.

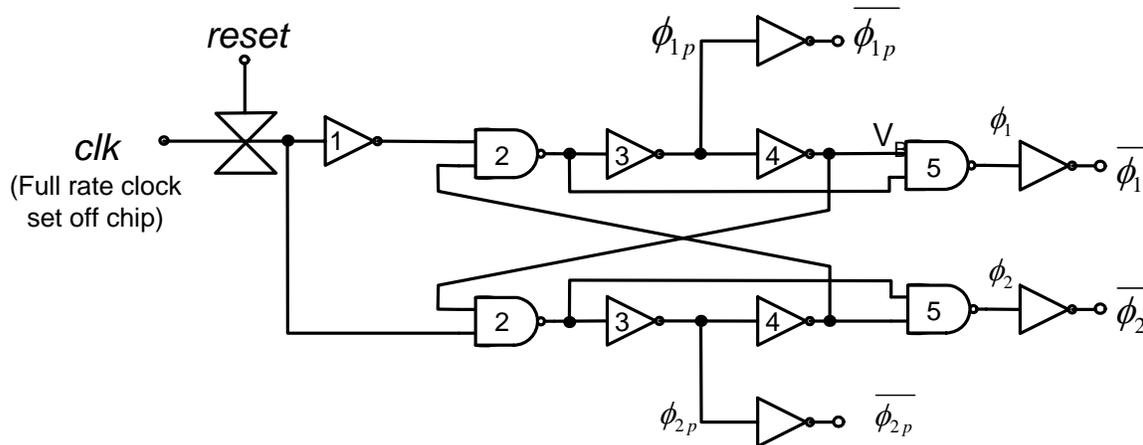


Fig. 5-40: non-overlapping clock generator

For this design, to improve the likelihood of design functionality (i.e. ensure enough time is given for clocks to fully swing rail to rail, and comparators to latch), a longer non-overlap time has been favored (shown in Fig. 5-41 to be 1.4ns). For higher sampling rates, where 1.4ns comprises a significant percentage of the settling time (e.g. for 50MHz, half pulse width is only 10ns), the settling time is reduced. In commercial designs, the non-overlap time can be carefully optimized to maximize the settling accuracy, such that a minimum power is required achieve the desired settled accuracy.

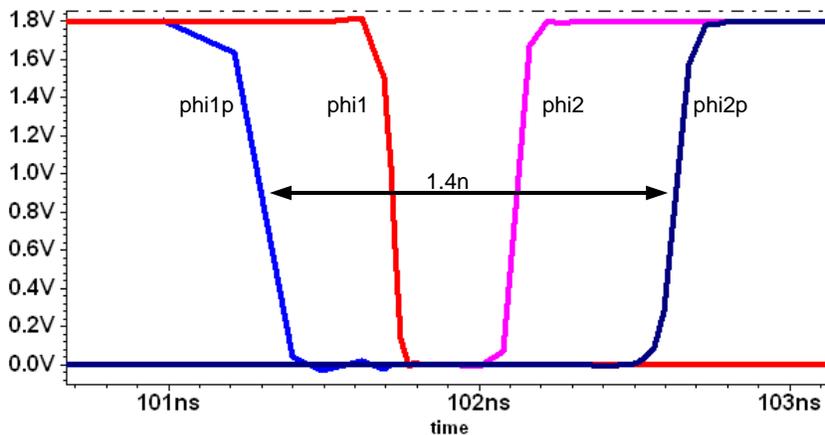


Fig. 5-41: illustration on non-overlapping time in SPICE simulation

The non-overlapping clock generator was powered on/off via transmission gate at the clock input, which is enabled or disabled according to Fig. 5-16 by 'reset'

5.16: Reference Voltages

A significant advantage of the pipeline ADC architecture is the minimal use of reference voltages. Only three reference voltages are required for the entire ADC: a differential reference for the stage ADCs ($v_{refp}=1.3V$, $v_{refn}=0.5V$), and a non-critical common mode reference ($v_{ref-cm}=0.9V$) for the CMFB circuit. In commercial designs the reference voltages are typically generated on chip through bandgap circuits, and/or resistor ladders. To enhance testability and minimize on chip complexity however, the three reference voltages are generated off chip for this dissertation. Thus the reference voltages are not controlled by the state machine, hence in the implementation of this dissertation not power scaleable. Future work could investigate power on/off schemes for the reference voltages using the various techniques described in this chapter thus far.

5.17: Digital error correction

In commercial designs the ADC must be self contained such that if an analog signal is input to the ADC chip, 10 digital bits should be output from the same chip. As the ADC of this dissertation is a prototype, testability takes precedence over form. Thus rather than performing an on chip digital error correction, the outputs of each stage have been routed off chip where error correction can be performed through a software post-processor (i.e. capture each stage digital output, and process it in Matlab to obtain the corrected 10-bit output). With the output of each stage available off chip, the design lends itself to more testability; if any errors are present in the design it is easier to debug where along the pipeline the problems are. As digital error correction typically consumes less than 5-10% of the total power budget, the exclusion of the block is not significant.

5.18: Simulation results

The power scaleable pipeline ADC with hybrid CMPS architecture was simulated at the top level using SPICE over process and temperature. This section presents a brief summary of key simulations and their results so as to provide a functional/performance reference for the fabricated chip.

From section 5.8.5, opamp bandwidths were designed such that the maximum sampling rate would be 50Msps. Simulated ENOB for various sampling rates while the ADC operates in power reduction mode are shown in Fig. 5-42 (ignoring thermal/opamp noise and power supply noise). The ENOB was measured such that the power was scaled for each sampling rate to have a minimal power for an accuracy near 10-bits. As mentioned in section 5.15, the non-overlap time of the clock generator was set fairly large to ensure design functionality, as such the ENOB performance at higher sampling frequencies is compromised. Furthermore, as the MDAC and sample and hold switches have been optimized for 50MHz operation, operation beyond 50MHz shows a degraded performance as expected.

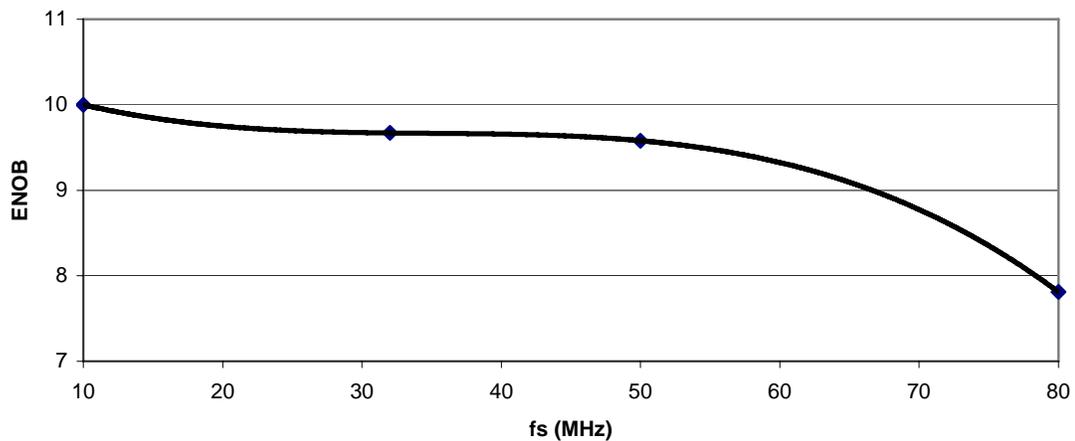


Fig. 5-42: SPICE simulated variation of ENOB with sampling frequency

The expected power in power reduction mode (PRM) and nominal modes (NM) of the ADC for various sampling rates is shown in Fig. 5-43:

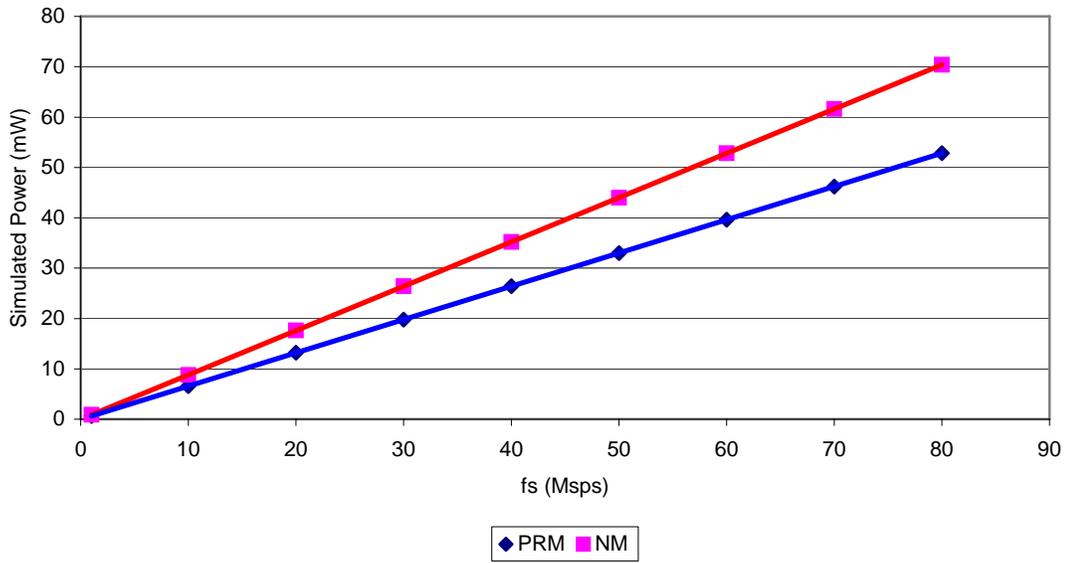


Fig. 5-43: Expected power based on simulation

As simulations in the digital power scale mode include a significant amount of digital logic, due to lengthy simulation times a minimal number of SPICE level simulations were performed to validate the power scaleable design in SPICE. A conservative simulation of the whole ADC in power scale mode was performed where the ADC state machine was operated at 10MHz (although the state machine and pipeline ADC were verified individually at higher and lower sampling rates). The state machine was programmed to have an effective sampling rate of ~1Msps, and the SNDR measured (i.e. digital state machine programmed to divide by 10: 10Msps/10=1Msps). A simulation was also performed with the ADC in power reduction mode at 10Msps, with the same supplied bias current, where the ENOB was found to be similar (~62dB) between sampling rates, verifying the hypothesis that ADC performance would be preserved between different sampling rates having the same bias current, thus saving the designer significant simulation time.

To determine the dependency of power on sampling rate, the power consumed during t_{on} for the analog circuitry was measured through simulation, as well as the estimated static power dissipation due to the digital state machine, and the current mirror set by an off chip resistor. Using equation (5.5) an estimate of the average power consumed by the ADC as a function

of effective sampling frequency was derived. The expected average analog power, and the expected analog + digital power as a function of sampling rate is shown in Fig. 5-44 for sampling rates covered by CMPS applied to the ADC with a 10MHz clock applied to the state machine. For frequencies not covered by CMPS (i.e. 1-10MHz), frequency dependent biasing can be used as described in section 5.5. As mentioned, simulations of the ADC operating in power scale mode at higher and lower clock rates supplied to the state machine were not performed due to lengthy simulation times, however the pipeline ADC and state machine were individually simulated at various sampling rates (1-80Msps) and found to be functional.

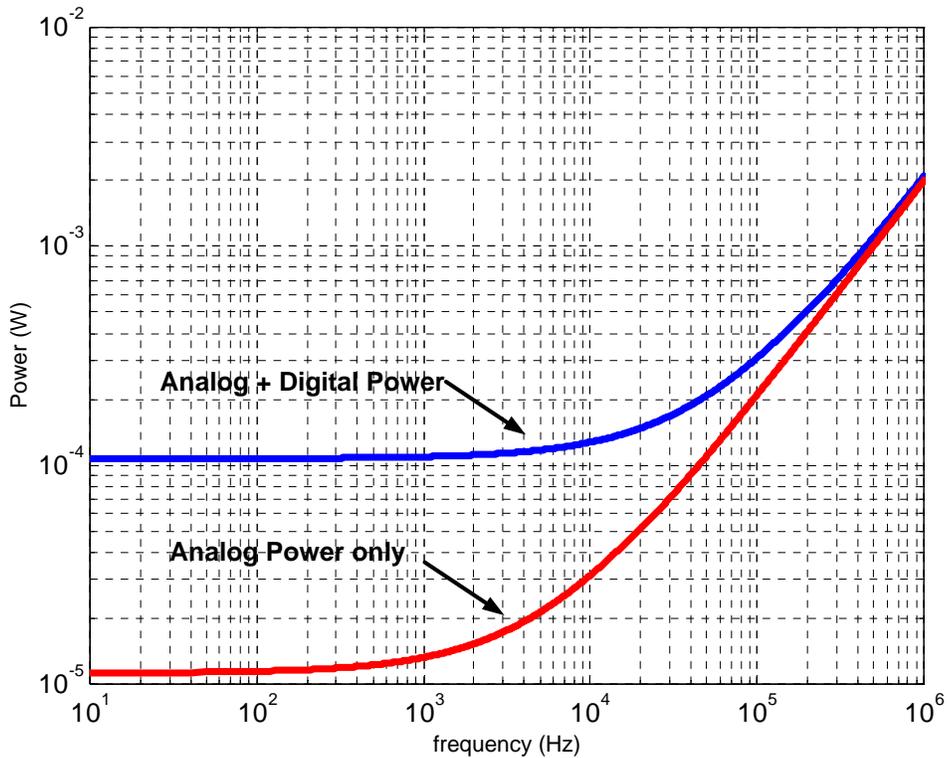


Fig. 5-44: SPICE simulated variation of Analog power and Analog+Digital power with effective sampling frequency with state machine clock = 10MHz

It is noted that the minimum power is limited by the power of the digital state machine. If the digital state machine were synthesized using a commercial standard cell library, the power scaleable range could easily be extended by at least 2-5x. As digital power scales with technology, the power scaleable range can be extended with smaller gate lengths.

5.19: Summary

In this chapter a general architecture for power scaleable ADCs, which scale their power by CMPS has been shown. A hybrid CMPS technique using a small current scaling range is shown to facilitate a large power scaleable range, including higher sampling rates not covered by previous power scaleable ADCs using a CMPS architecture. A fast power on/off Power Resettable Opamp (PROamp) has been developed, where by virtue of a replica bias structure, exhibits on/off times much shorter than previous attempts to power on/off opamps. The short on/off times of the PROamp have also been shown to be advantageous in general pipeline ADCs where by powering the MDAC opamps off during the sampling phase, it is possible to significantly reduce the opamp power consumed. The choices of circuits used in the fabricated integrated circuit for this dissertation were explained and justified. Simulation results validating the design were also presented.

CHAPTER SIX

Experimental Results

6.1: Overview

This chapter discusses experimental results of a pipeline ADC fabricated in $0.18\mu\text{m}$ CMOS, which as described chapter five, has three operating modes: 1.) Power scalability, 2.) Power reduction, and 3.) Nominal operation. Measured results show the hybrid CMPS technique as described in section 5.5, multiplies the power scaleable range of current scaling by over 1000x, where scaleable power can be achieved for f_s greater than 50Msps (35mW), and f_s lower than 1ksps ($16\mu\text{W}$). The application of the PROamp to reduce opamp power in pipeline ADCs is shown to reduce total ADC power 20-30%, where for $f_s=50\text{Msps}$, power is reduced from 44mW to 35mW. A peak ENOB of 9.1 bits is realized at $f_s=10\text{Msps}$, and an ENOB of 8.8 bits is realized at 50Msps, with Nyquist rate input. The problems of biasing the ADC deep in weak inversion are also empirically validated by performing a bias point analysis, where for lower bias currents the ADC is shown to have a substantial degradation in accuracy for small variations in bias voltages.

6.2: Experimental implementation – Integrated Circuit

The power scaleable pipeline ADC was implemented in a $0.18\mu\text{m}$ CMOS process (nominal $V_{\text{DD}}=1.8\text{V}$), and fabricated through the Canadian Microelectronics Corporation (CMC) in a single poly, 6-metal process, including MIM capacitor and Deep N-Well layer options. The core area was $1.1\text{mm} \times 1.1\text{mm}$ (1.21mm^2), and the total area including I/O drivers and bonding pads was $1.5\text{mm} \times 1.5\text{mm}$ (2.25mm^2). The integrated circuit was packaged in a 44-pin CQFP package. To minimize power supply related noise, analog pins were separated from digital pins on the power supply ring surrounding the ADC core. The layout of the

fabricated chip is shown in Fig. 6-1, where key circuit blocks of the pipeline ADC have been highlighted.

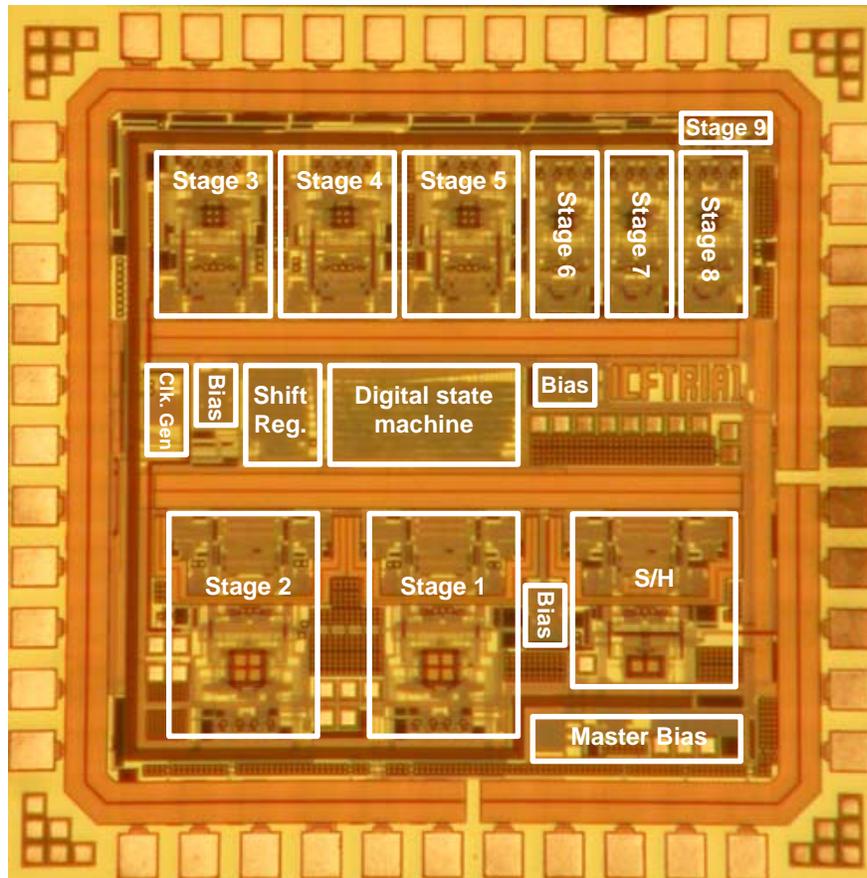


Fig. 6-1: Photograph of fabricated chip

As described in chapter five, the reference voltages and constant current bias source were generated off chip. Digital error correction was also performed off chip via a script written in Matlab.

6.2.2: Experimental implementation – PCB

A 4 layer FR4 dielectric PCB board with a minimum 6mil trace was designed and constructed for the device under test (Fig. 6-2). Separate Power planes were used to isolate the analog, digital, I/O, and board power supplies. A differential input was generated using a

1:1 turns ratio Minicircuits transformer matched to 50Ω . Reference voltages ($v_{refp}=1.3V$, $v_{refn}=0.5V$, and $v_{ref-cm}=0.9V$ as described in section 5.16) were generated by passing the output of a resistive voltage divider through an opamp (LM7301) in a unity gain buffer configuration. To maintain constant supply voltages, all voltage supplies for each power plane were generated through regulators (LM337, LM1117), and heavily decoupled with capacitors. As the ADC utilized a constant current biasing scheme, an off chip adjustable resistor was used as the master current source. The resistance was a series combination of $1k\Omega$, $10k\Omega$, $200k\Omega$, $1M\Omega$, and $3M\Omega$ potentiometers such that the biasing current could be accurately controlled over a wide range to facilitate the evaluation of wide range current scaling.

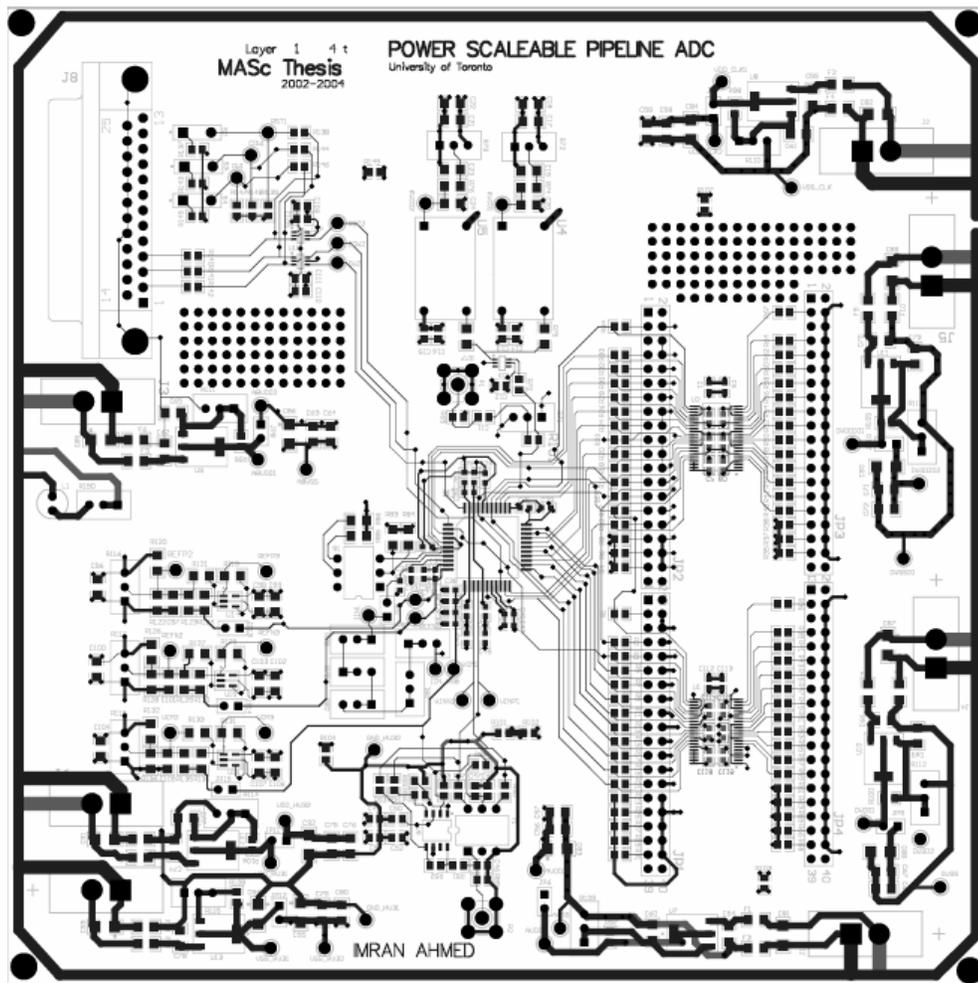


Fig. 6-2: Custom PCB layout

6.2.3: Experimental Implementation – Test setup

A test setup as shown in Fig. 6-3 was used. Sinusoidal inputs were generated using a Rohde & Schwarz SMT03 function generator. A Minicircuits low pass filter was used to minimize harmonic distortion from the function generator such that the sinusoidal input to the ADC had an SNDR of well over 62dB. An HP 81120A pulse/pattern generator was used to generate the clock to the ADC. The serial shift register was loaded via a parallel port connection to a PC, where a Matlab script was executed to load the appropriate bits. The output bits of each pipeline stage were captured using a Tektronix TLA714 logic analyzer, capable of capturing 65,536 points at a time. An Agilent E3620A Dual output DC power supply was used to provide positive and negative voltages to the voltage regulators on the PCB. The 10-bit output word from the 10-bit ADC was determined via a Matlab script written to emulate the operation of a digital error correction circuit.

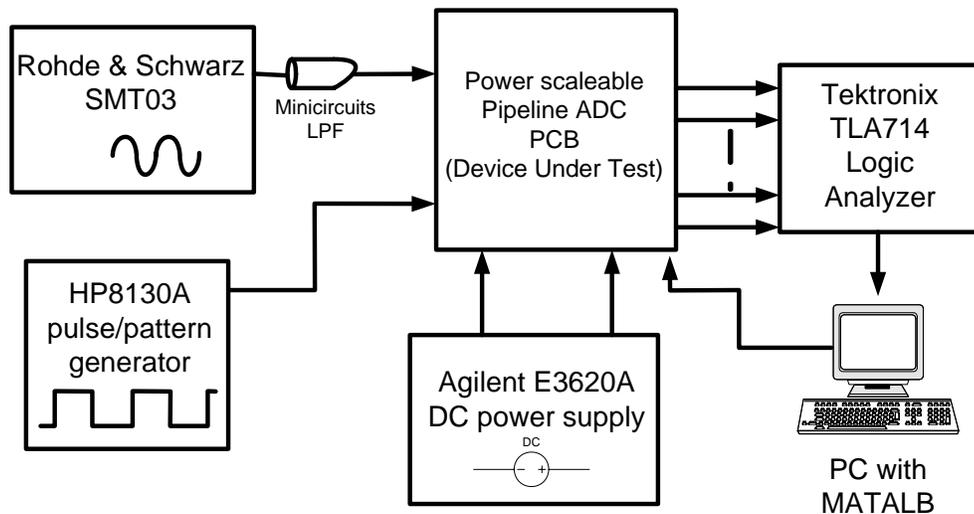


Fig. 6-3: Test setup for power scaleable pipeline ADC

6.3: Measured results

As described in section 5.5, the fabricated ADC achieves power scalability by using a hybrid CMPS technique, where current scaling is used to achieve power scalability for sampling rates not allowable with CMPS applied to a pipeline ADC. Since the CMPS technique provides power scalability by effectively multiplying the power scaleable range achievable

through current scaling while preserving the accuracy (as bias currents are unchanged when CMPS is enabled), the complete performance of the ADC can be quickly characterized by measuring the accuracy of the ADC for a narrow range of current scaled sampling rates. As such the measured results of the fabricated ADC are presented in two sections (6.4 and 6.5). Section 6.4 presents measured results of the ADC for a small range of sampling rates, where current scaling is used to achieve power scaleability. To evaluate the benefits of powering off the MDAC during the sampling phase, the power of the ADC in power reduction and nominal modes is also compared. The problems of extended power scaling using frequency dependent biasing are also elaborated with measured results in section 6.4.3. Section 6.5 presents measured results showing the achievable power scaleable range with CMPS applied to the current scaled sampling rates presented in section 6.4, thereby validating that the accuracy is indeed preserved when CMPS is used for lower sampling rates, and that an extended power scaleable range of sampling rates can be achieved without further reductions in bias currents.

6.4: Current scaling – Dynamic accuracy

The bias currents were scaled for f_s between 1-80Msps, where the current was set such that the figure-of-merit (see section 2.4) was optimal. For each f_s , a full scale (1.6Vpp) sinusoid near Nyquist was applied to the ADC input, where the SNDR, *Spurious Free Dynamic Range* (SFDR) and associated power were measured for each f_s .

The ENOB was measured as

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad (6.1)$$

To measure the benefit of the power reduction technique, the ADC was switched to nominal mode, and the accuracy and power were measured (without adjusting the bias currents, such that any additional power consumed was only due to the opamps being powered on all the time rather than just the hold phase as in the power reduction mode). The measured results of the ADC in power reduction (PRM) and nominal modes (NM) are shown in Table 6-1, where Fig. 6-4 to Fig. 6-6 graphically illustrate the differences in accuracy and power of the two operation modes. The 65,536 point FFTs of the digitized output are shown in Fig. 6-7 to

Fig. 6-12 for sampling rates of 50, 30 and 10Msps. Table 6-2 tabulates the figure of merit of the ADC for different current scaled sampling rates

Table 6-1: Measured ENOB and Power from fabricated ADC

<i>Accuracy and Power measurements of ADC</i>									
f_s (Msps)	f_{in} (MHz)	<i>SNDR (dB)</i>		<i>ENOB (bits)</i>		<i>SFDR (dB)</i>		<i>Power (mW)</i>	
		<i>PRM</i>	<i>NM</i>	<i>PRM</i>	<i>NM</i>	<i>PRM</i>	<i>NM</i>	<i>PRM</i>	<i>NM</i>
1	0.17	54.9	55.3	8.8	8.9	63	65	0.7	1.1
10	4.75	56.4	55.3	9.1	8.9	71	64	5.6	7.2
20	9.54	55.9	54.7	9.0	8.8	70	62	11.7	15.6
30	14.01	55.7	54.1	9.0	8.7	71	60	19.1	25.1
40	19.01	54.7	53.3	8.8	8.6	67	60	26.5	34.4
50	20.94	54.8	51.8	8.8	8.3	67	58	34.9	44.2
60	20.94	52.2	48.8	8.4	7.8	62	54	43.1	53.8
70	20.94	46.7	44.2	7.5	7.0	56	49	45.0	53.6
80	20.94	42.7	42.1	6.8	6.7	52	51	54.7	64.8

(PRM = Power reduction mode, NM=Nominal mode)

**Note power listed excludes I/O buffer, reference voltage, and digital error correction power*

Table 6-2: Fig. of merits for measured ADC at various f_s

<i>Accuracy and Power measurements of ADC</i>						
f_s (Msps)	f_{in} (MHz)	<i>FOM (pJ/step)</i>		<i>FOM (mW/Msps)</i>		<i>Power Reduction</i>
		<i>PRM</i>	<i>NM</i>	<i>PRM</i>	<i>NM</i>	
1	0.17	1.6	2.2	0.72	1.06	32.3%
10	4.75	1.0	1.5	0.56	0.72	22.0%
20	9.54	1.2	1.7	0.59	0.78	24.9%
30	14.01	1.3	2.0	0.64	0.84	23.9%
40	19.01	1.5	2.3	0.66	0.86	23.0%
50	20.94	1.6	2.8	0.70	0.88	21.1%
60	20.94	2.2	4.0	0.72	0.90	19.9%
70	20.94	3.6	5.8	0.64	0.77	16.1%
80	20.94	6.1	7.8	0.68	0.81	15.6%

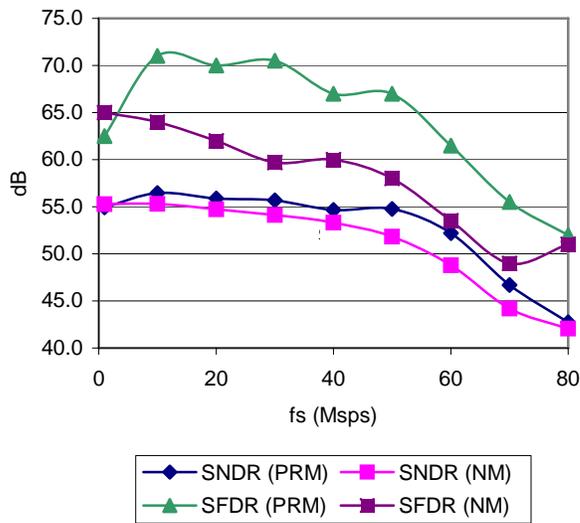


Fig. 6-4: SNDR, SFDR variation with sampling rate for PRM and NM

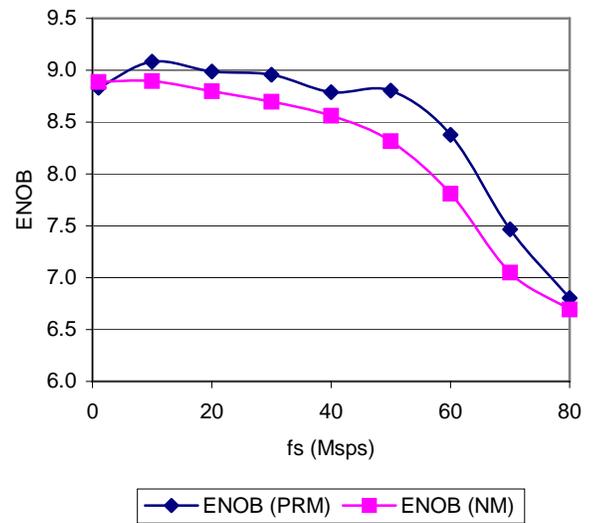


Fig. 6-5: ENOB variation with sampling rate for PRM and NM

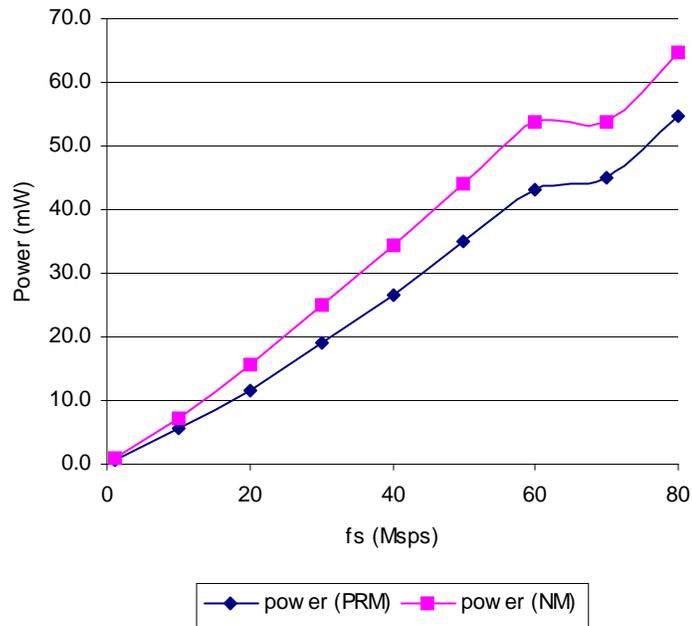


Fig. 6-6: Variation of power with sampling rate for PRM and NM

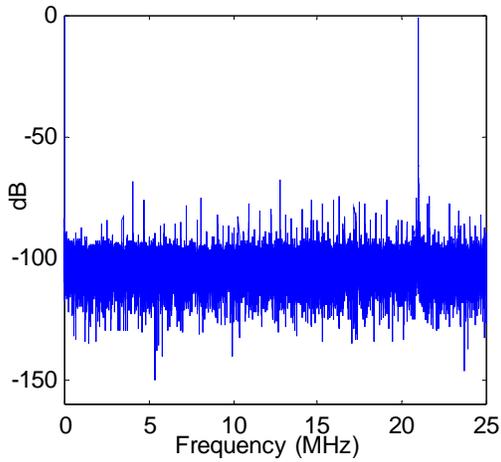


Fig. 6-7: $f_s=50\text{Msps}, f_{in}=20.9371\text{MHz}, \text{PRM}$

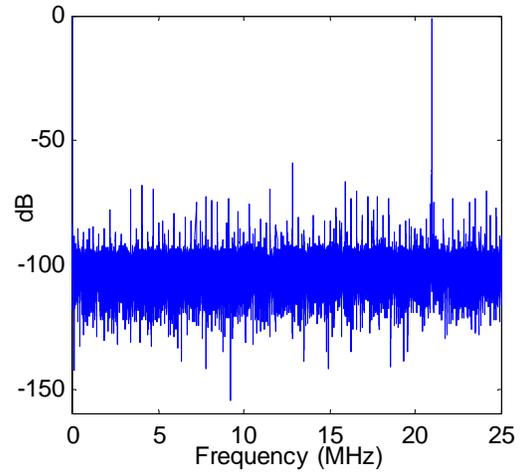


Fig. 6-8: $f_s=50\text{Msps}, f_{in}=20.9371\text{MHz}, \text{NM}$

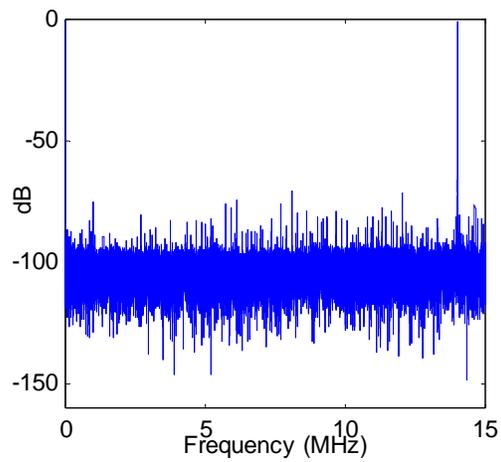


Fig. 6-9: $f_s=30\text{Msps}, f_{in}=14.013\text{MHz}, \text{PRM}$

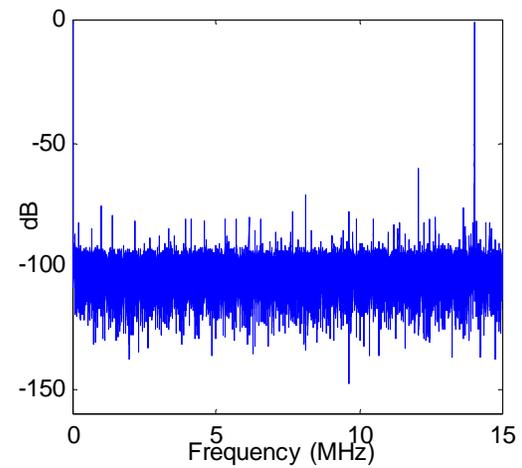


Fig. 6-10: $f_s=30\text{Msps}, f_{in}=14.013\text{MHz}, \text{NM}$

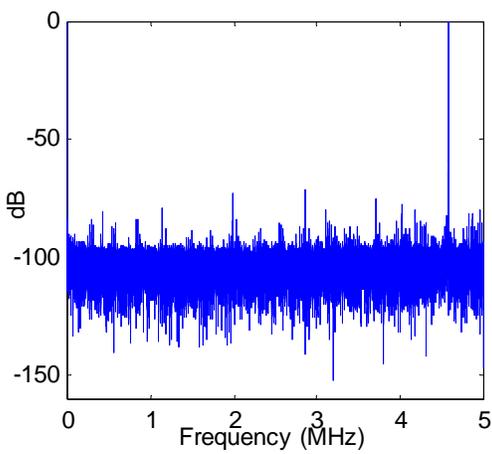


Fig. 6-11: $f_s=10\text{Msps}, f_{in}=4.571\text{MHz}, \text{PRM}$

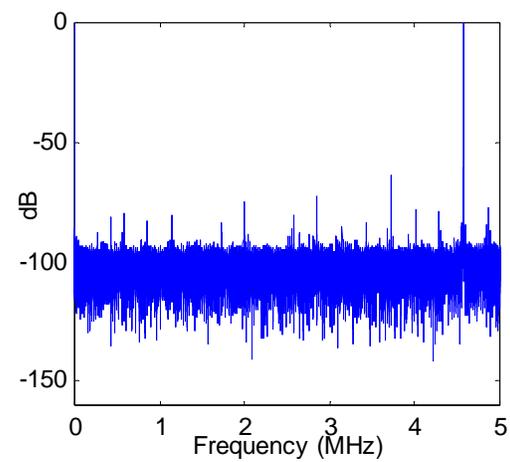


Fig. 6-12: $f_s=10\text{Msps}, f_{in}=4.571\text{MHz}, \text{NM}$

When the power reduction mode is enabled the power is reduced by as much as 30%. As described in section 5.10, the relative reduction of power in the power reduction mode is less for higher sampling rates as the opamp is off for a smaller percentage of the clock cycle. As the ADC maintains similar accuracy between power reduction and nominal modes for f_s up to 80Msps, it can be concluded the effect of increased power supply noise due to ground bounce (as described in section 5.4) is negligible. The low power supply noise is likely due to the use of large on chip supply-decoupling capacitors (section 5.4) and large off chip capacitors to maintain a constant power supply. The power reduction method shows a slightly higher ENOB for faster sampling rates as the CMFB circuit for the opamp in power reduction mode operates on an advanced clock ($\sim 1.4\text{ns}$ advanced from the clocks supplied to the CMFB in nominal mode, thereby increasing the settling time), which for higher frequencies is a large portion of the settling time. If however the ADC in nominal mode is supplied additional current, measured results show the ADC settles to the same accuracy in both cases. The similar accuracy and significantly reduced power in power reduction mode demonstrates the effectiveness of a Power Resettable Opamp to significantly reduce power in switched capacitor circuits at high sampling rates.

The ADC is further characterized in Fig. 6-13 to Fig. 6-19 at current scaled sampling rates of 50Msps, 30Msps, and 10Msps. Only results from power reduction mode are shown as the power reduction mode produces the best figure of merit. The plots include the variation of SNDR with supply voltage, and SNDR with input signal swing. As the input bandwidth of the ADC is limited by the layout and input switch sizes only (since a S&H is used on the front end of the ADC), the variation of SNDR with input frequency is only presented for $f_s=50\text{Msps}$. Of note as the highest bandwidth low pass filter available to filter distortion from the Rohde & Schwarz SMT-03 was 21.4MHz, the maximum input bandwidth could not be verified through measurement (i.e. the maximum input frequency where the ADC begins to loose accuracy due to distortion through the input sample and hold switch). For input frequencies below 200kHz, a Stanford Research Systems DS360 was used to provide the input sinusoid.

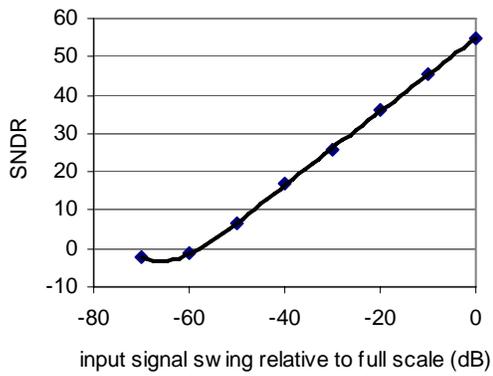


Fig. 6-13: input dynamic range, $f_s=50\text{MSPS}$, $f_{in}=20.371\text{MHz}$

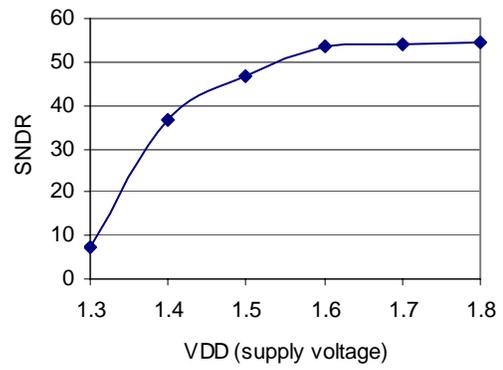


Fig. 6-14: SNDR vs. supply voltage for $f_s=50\text{MSPS}$, $f_{in}=20.173\text{MHz}$

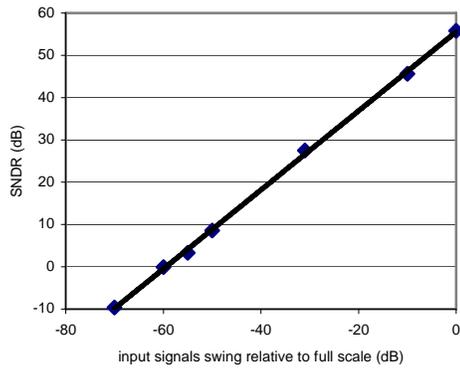


Fig. 6-15: input dynamic range, $f_s=30\text{MSPS}$, $f_{in}=14.317\text{MHz}$

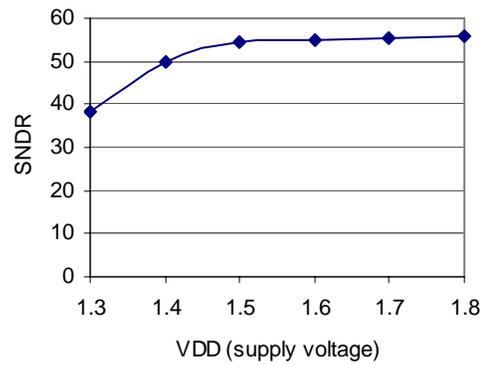


Fig. 6-16: SNDR vs. supply voltage for $f_s=30\text{MSPS}$, $f_{in}=20.173\text{MHz}$

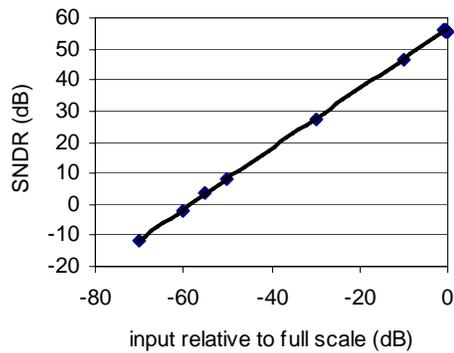


Fig. 6-17: input dynamic range, $f_s=10\text{MSPS}$, $f_{in}=4.571\text{MHz}$

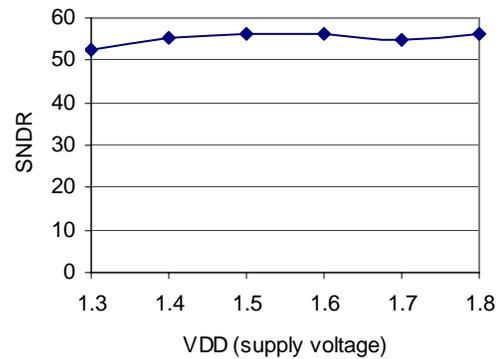


Fig. 6-18: SNDR vs. supply voltage for $f_s=10\text{MSPS}$, $f_{in}=4.571\text{MHz}$

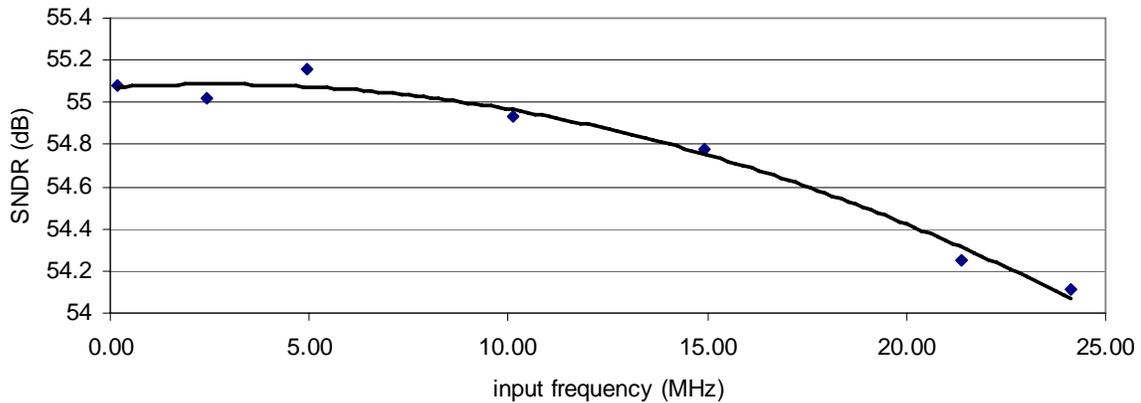


Fig. 6-19: SNDR vs input frequency for $f_s=50\text{Msps}$

Of note, when the supply voltage was reduced, the current was adjusted for each V_{DD} to be constant (if possible) to maintain fixed opamp bandwidths, and the reference voltages adjusted to maintain a fixed total V_{DS} across the opamp transistors of 800mV (i.e. input signal swing for $V_{DD}=1.8, 1.7, 1.6, 1.5, 1.4, 1.3$ was 1.6V, 1.6V, 1.6V, 1.4V, 1.2V, 1V peak-to-peak respectively). The input frequency was not adjusted between V_{DD} measurements for fixed f_s .

The power, FOM (pJ/step), and power per conversion step (mW/Msps) of this work (in power reduction mode only, as it has the best figure-of-merit) is compared to recently published ADCs (listed in section 3.6), for the current scaled sampling rates of Table 6-2 in Fig. 6-20 to Fig. 6-22. Previous publications include different ADCs fabricated in different technologies.

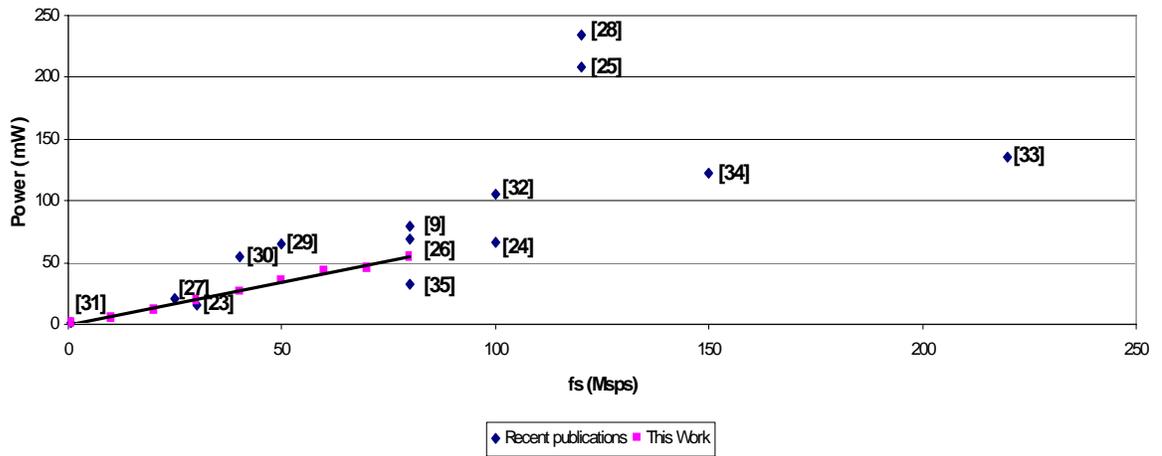


Fig. 6-20: Power vs. Speed comparison of this work (in Power reduction mode) with recent publications listed in section 3.6

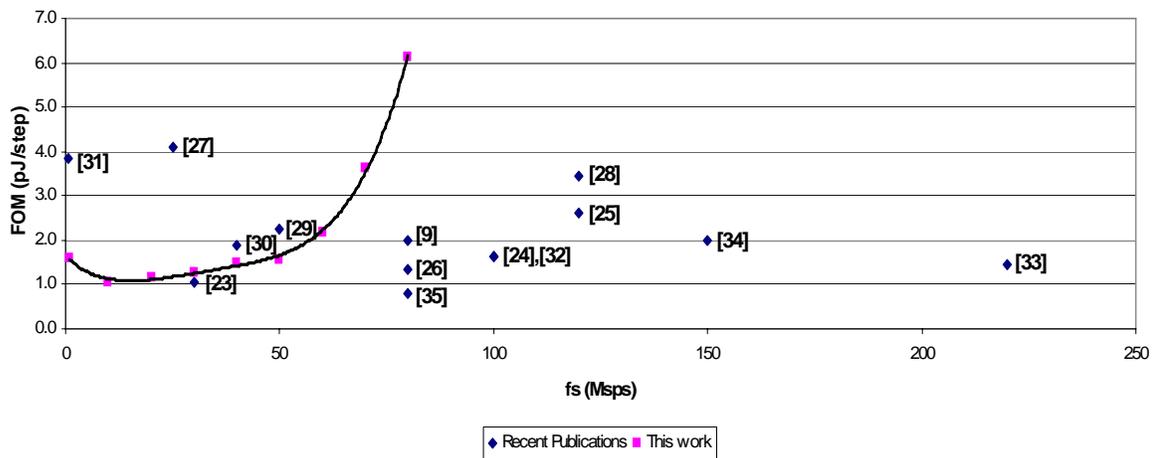


Fig. 6-21: Energy per conversion step comparison of this work (in power reduction mode) and publications listed in section 3.6

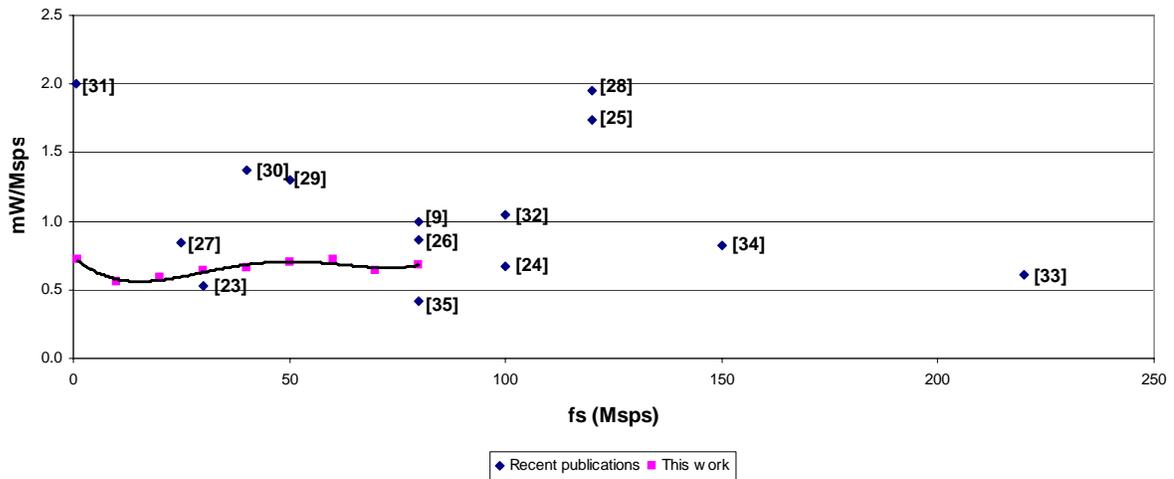


Fig. 6-22: power per conversion step comparison of this work (in power reduction mode) and publications listed in section 3.6

Although the goal of this dissertation favored proof-of-concept over absolute figure-of-merit, the ADC in power reduction mode exhibits good figure of merits – a testament to the benefits gained using the PROamp as a means to reduce power in high speed switched capacitor circuits.

6.4.2: Power reduction mode – Static accuracy

A histogram-based approach was taken to measure the INL and DNL of the ADC [52]. The histogram approach has the advantage of measuring ADC linearity without resorting to more time consuming DC approaches, which require several thousand different measurements, necessitating a more complicated automated testing routine. The histogram approach however has the disadvantage of requiring a significant amount of samples to measure the INL/DNL to at least 0.1LSB accuracy (>1,000,000 for 10-bit ADCs). As the Tektronix TLA714 logic analyzer only had a memory of 65,536 samples, to obtain an accuracy of at least 0.1LSB in the INL/DNL plots, several measurement captures of the logic analyzer were combined together to form a single measurement file, which had 1,048,576 output samples. A script written in MATLAB was used to derive the INL and DNL from the amalgamated data capture. The INL and DNL plots of the ADC in power reduction mode at sampling rates

of 10, 30 and 50Msps are shown in Fig. 6-23 to Fig. 6-28, where the maxima/minima are listed in Table 6-3.

Table 6-3: INL/DNL maxima and minima for $f_s=10, 30, 50$ Msps for current scaled f_s

f_s (Msps)	Max INL	Min INL	INL pp	Max DNL	Min DNL	DNL pp
10	+0.92	-0.92	1.84	+0.32	-0.52	0.84
30	+1.01	-1.17	2.18	+0.63	-0.70	1.33
50	+1.06	-1.19	2.25	+0.63	-0.91	1.54

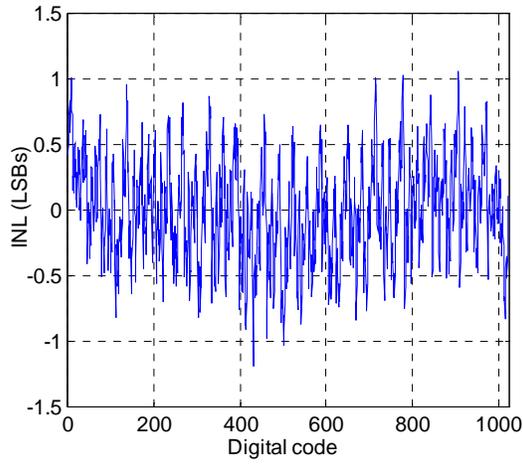


Fig. 6-23: INL @ 50Msps

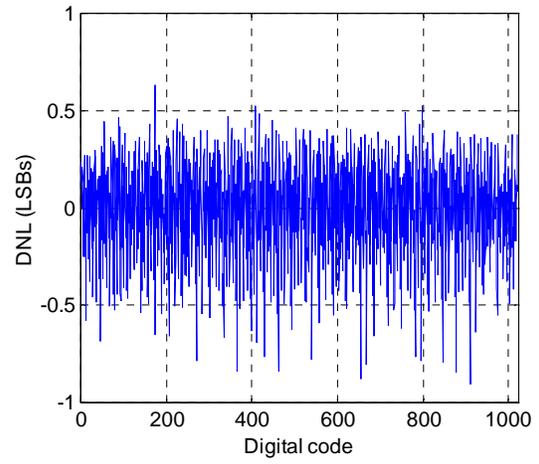


Fig. 6-24: DNL @ 50Msps

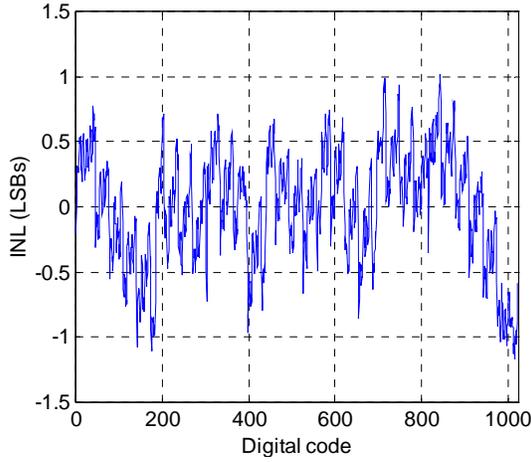


Fig. 6-25: INL @ 30Msps

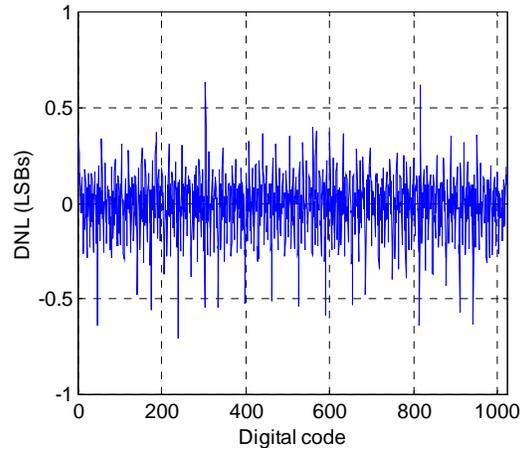


Fig. 6-26: DNL: @ 30Msps

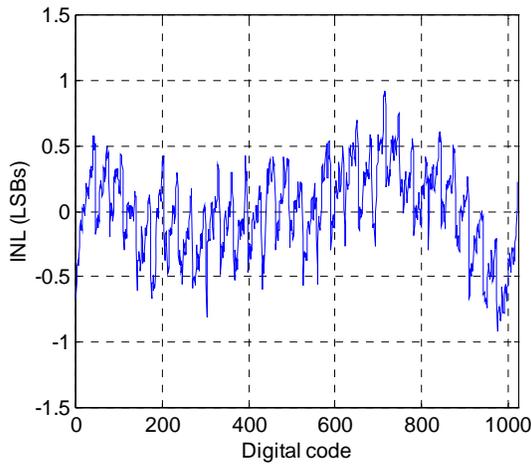


Fig. 6-27: INL @ 10Msps

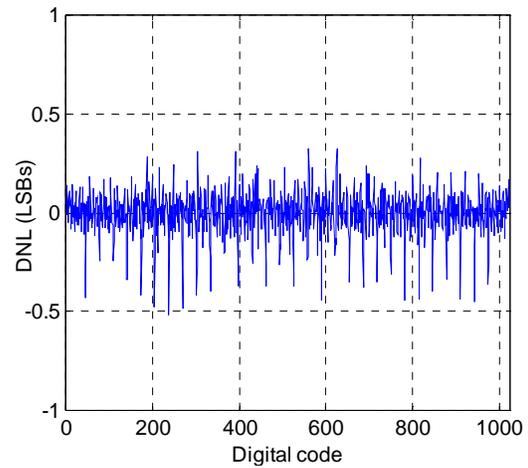


Fig. 6-28: DNL @ 10Msps

The INL plots exhibit sudden jumps in code error, indicating gain error in the pipeline stages. As mentioned in section 6.4 however, the power of the ADC was adjusted to achieve an optimal figure of merit. By providing a minimal power to the MDACs, some stages can be bandwidth limited to less than 10-bit accuracy, hence inducing gain error due to incomplete settling. If the ADC power is increased well beyond the optimal power, such that the stages are not bandwidth limited to less than 10-bit accuracy, it can be evaluated if in fact the larger linearity errors are due to insufficient opamp bandwidth, or capacitor mismatch/insufficient DC opamp gain. The INL/DNL plots of the ADC with maximum power are shown in Fig. 6-29 to Fig. 6-34, where the maxima/minima are listed in Table 6-4:

Table 6-4: INL/DNL maxima and minima for $f_s=10, 30, 50\text{MSPs}$ for maximum bandwidth

f_s (MSPs)	Max INL	Min INL	INL pp	Max DNL	Min DNL	DNL pp
10	+0.46	-0.45	0.91	+0.36	-0.15	0.51
30	+0.90	-0.64	1.54	+0.40	-0.23	0.63
50	+1.34	-1.13	2.47	+0.44	-0.67	1.11

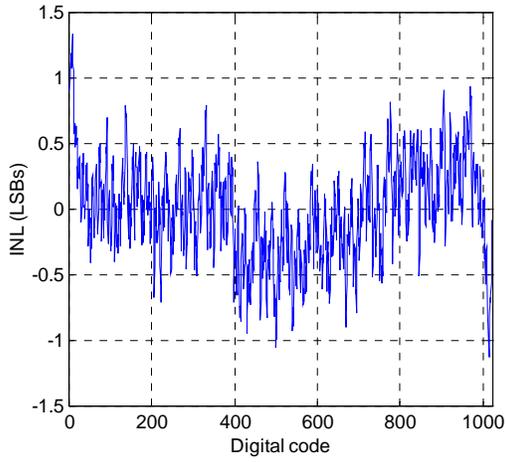


Fig. 6-29: INL @ 50MSPS (Max BW)

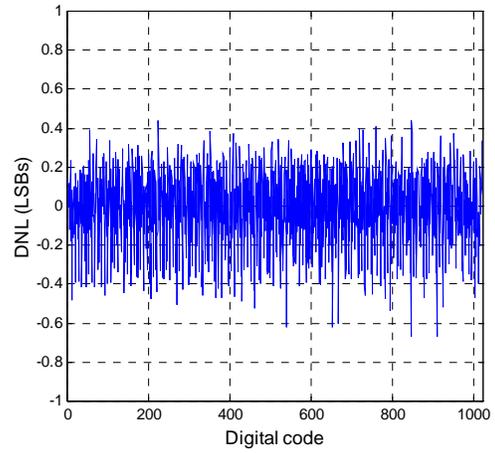


Fig. 6-30: DNL @ 50MSPS (Max BW)

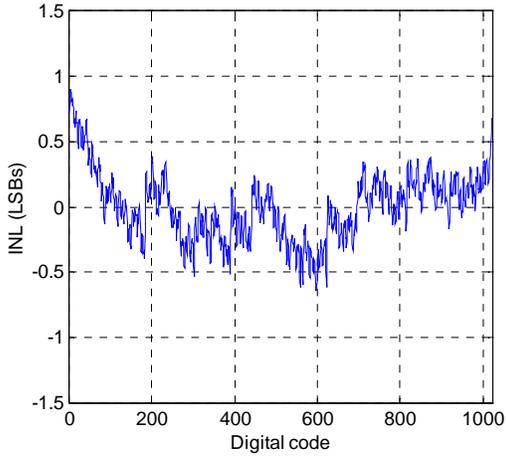


Fig. 6-31: INL @ 30MSPS (Max BW)

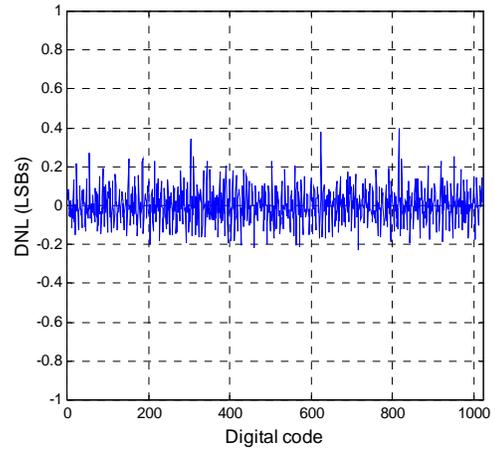


Fig. 6-32: DNL @ 30MSPS (Max BW)

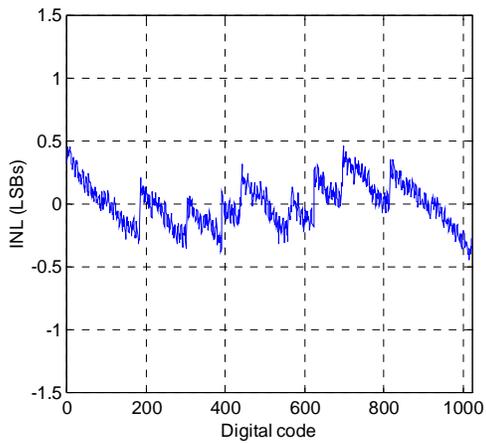


Fig. 6-33: INL @ 10MSPS (Max BW)

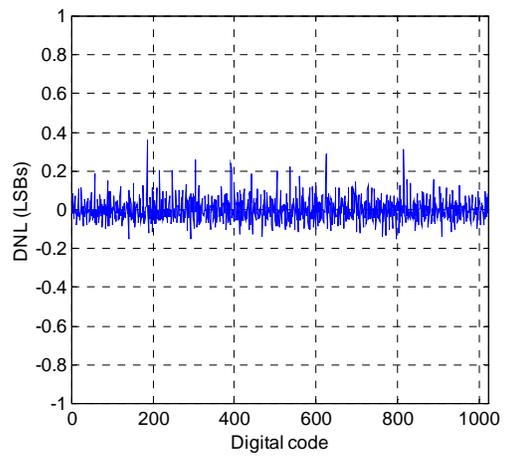


Fig. 6-34: DNL @ 10MSPS (Max BW)

As the ADC shows smaller linearity errors when not bandwidth limited, it can be inferred the larger linearity errors in Fig. 6-23 to Fig. 6-28 are due to some stages in the pipeline ADC being bandwidth limited when optimizing for figure-of-merit. Of note, the ADC displays less INL/DNL with lower sampling rates as more settling time is available for lower sampling rates. Thus although the ADC is not bandwidth limited to 10-bit accuracy with maximum power, the ADC is bandwidth limited to a higher accuracy (e.g. 12-bits), hence the improvement by $<1\text{LSB}$ in INL/DNL plots between 50 and 10Msps.

6.4.3: Power scaleable ADC – Current Scaling

As described in chapter four, there are several problems in using current scaling as a technique to scale power with sampling frequency over large sampling rates. The problems fall into two categories: pre-design and post-Design. Pre-design problems include increased design time due to multiple bias points, and more complicated and less reliable simulation models. Post-design problems include poorer yield, and increased bias point sensitivity. Only post-design problems may be empirically evaluated. For a proper yield analysis, the performance of the ADC biased deep in the weak inversion region must be measured for several hundred fabricated chips with identical setups (i.e. same input/clock frequency and supplied bias current). Such an analysis is not possible with the time, equipment, and number of chips fabricated available (only five packaged ICs are delivered) – thus a true yield analysis cannot be performed. Larger performance variations in weak inversion however, can be inferred from a bias point analysis of the ADC biased in weak inversion.

As described in section 5.14, a constant current biasing scheme set by an off chip resistor was used for the ADC of this dissertation. By using a digitally controlled voltage source (Agilent E3631A) rather than an off chip resistor, the V_{GS} of the on-chip current mirror shown in Fig. 6-35 can be precisely controlled. As such the impact of small variations of the bias voltage V_B (i.e. V_{GS} of M2 in Fig. 6-35) on ADC accuracy can be measured.

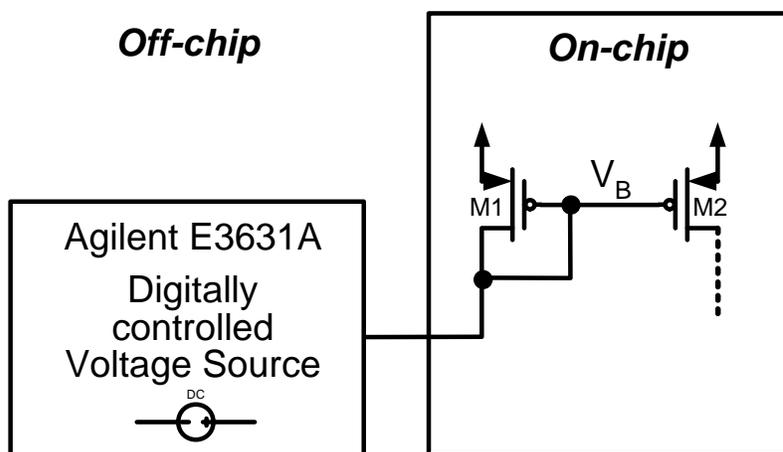


Fig. 6-35: Setup to perform bias point analysis

The theory of section 4.7 predicts the exponential dependency of drain-source current on gate-source voltages of devices in weak inversion cause the ADC to be more susceptible to bias fluctuations (i.e.) a larger reduction in performance for the same increment in bias voltage when the ADC is deeper into the weak inversion region. To verify the claim, the ADC was biased with the digitally controlled voltage source such that an ENOB of 7-8 bits was achieved at $f_s=100k$, 1Msps, 10Msps, 30Msps, and 50Msps (i.e. ADC was bandwidth limited, so that variations in bias currents directly impact settling time of ADC). The ENOB and power of the ADC were measured as the V_{GS} bias voltage of the on-chip current mirror was increased by 20mV in 2mV steps (thereby decreasing the on-chip V_{eff}). The measured ENOB reduction is shown graphically in Fig. 6-36.

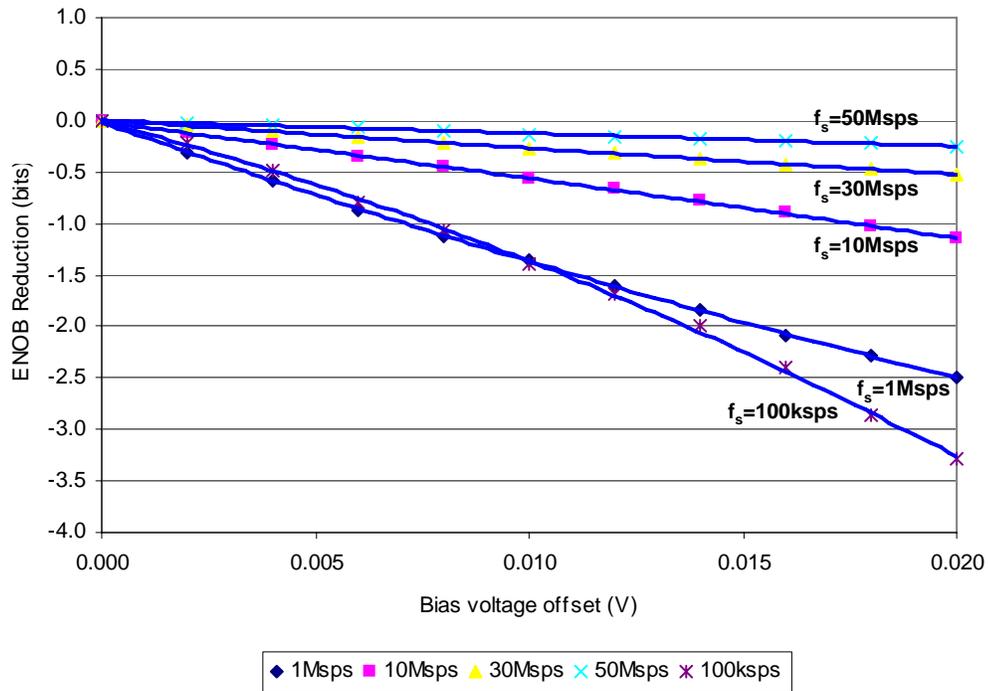


Fig. 6-36: Bias point sensitivity of ADC as current reduced with f_s

Thus, although it is possible to obtain a high accuracy as the ADC is driven into the weak inversion region (e.g. can achieve >8 bits even for very low bias currents), the ADC performance becomes highly sensitive to bias voltage variations. It may also be inferred that any offset incurred due to a threshold mismatch would similarly affect ADC performance (e.g.) the reduction in performance due to a 5mV threshold mismatch on the on-chip current mirror can be inferred from Fig. 6-36. Thus although it is possible to achieve a similar peak performance when current scaling is used to reduce analog power with sampling frequency, the increased bias sensitivity and poorer yield make current scaling over a large range impractical from a robustness standpoint.

6.5: Power scalable ADC – Power Scaling using CMPS

To evaluate the digitally controlled power scalable mode, clock frequencies between 1MHz and 50MHz were supplied to the state machine, where the ADC power was scaled (by adjusting the bias currents) according to Table 6-1. For each f_s between 1 and 50Msps the

state machine was programmed to various effective sampling rates (i.e. between $1/7^{\text{th}}$ and $1/3584^{\text{th}}$ the maximum f_s), and the power measured for each f_s . The measured power, SNDR, and SFDR of the ADC using CMPS at clocks of 50MHz, 30MHz, 10MHz and 1MHz supplied to the state machine (f_{sm}) are presented in Table 6-5 to Table 6-8, and in graphical form in to Fig. 6-44.

Table 6-5: ADC performance using CMPS with $f_{sm}=50\text{MHz}$

f_s (Hz)	f_{in} (Hz)	P_{analog} (mW)	$P_{digital}$ (mW)	P_{Total} (mW)	SNDR (dB)
5.55E+06	1.79E+06	9.72	1.05	10.77	54.3
3.12E+06	1.79E+06	5.45	0.84	6.29	54.3
1.67E+06	1.79E+06	2.88	0.71	3.59	54.1
8.62E+05	1.79E+06	1.58	0.64	2.22	54.3
4.38E+05	1.79E+06	0.84	0.60	1.43	54.4
2.21E+05	1.79E+06	0.46	0.59	1.04	54.2
1.11E+05	2.00E+05	0.27	0.57	0.84	54.5
5.56E+04	2.00E+05	0.17	0.57	0.74	53.8
2.77E+04	2.00E+05	0.12	0.57	0.69	53.7
1.39E+04	2.00E+05	0.10	0.57	0.67	53.5

Table 6-6: ADC performance using CMPS with $f_{sm}=30\text{MHz}$

f_s (Hz)	f_{in} (Hz)	P_{analog} (mW)	$P_{digital}$ (mW)	P_{Total} (mW)	SNDR (dB)
3.33E+06	1.79E+06	5.53	0.63	6.15	55.7
1.87E+06	1.79E+06	2.98	0.50	3.48	55.4
1.00E+06	1.79E+06	1.65	0.43	2.08	55.6
5.17E+05	1.79E+06	0.87	0.39	1.25	55.2
2.63E+05	1.79E+06	0.46	0.36	0.82	55.4
1.33E+05	2.00E+05	0.25	0.35	0.60	55.1
6.66E+04	2.00E+05	0.15	0.34	0.49	54.9
3.32E+04	2.00E+05	0.09	0.34	0.44	55.1
1.67E+04	2.00E+05	0.07	0.34	0.41	55.3
8.36E+03	2.00E+05	0.06	0.34	0.40	55.3

Table 6-7: ADC performance using CMPS with $f_{sm}=10\text{MHz}$

f_s (Hz)	f_{in} (Hz)	P_{analog} (mW)	$P_{digital}$ (mW)	P_{Total} (mW)	SNDR (dB)
1.11E+06	1.79E+06	1.710	0.19	1.90	56.1
6.25E+05	1.79E+06	0.941	0.17	1.11	55.9
3.33E+05	2.00E+05	0.503	0.14	0.65	55.0
1.72E+05	2.00E+05	0.264	0.13	0.39	55.8
8.77E+04	2.00E+05	0.140	0.12	0.26	55.5
4.42E+04	2.00E+05	0.076	0.12	0.19	55.5
2.21E+04	2.00E+05	0.044	0.11	0.16	55.2
1.12E+04	2.00E+05	0.028	0.11	0.14	55.3
5.58E+03	2.00E+05	0.022	0.11	0.14	55.6
2.79E+03	2.00E+05	0.016	0.11	0.13	55.9

Table 6-8: ADC performance using CMPS with $f_{sm}=1\text{MHz}$

f_s (Hz)	f_{in} (Hz)	P_{analog} (mW)	$P_{digital}$ (mW)	P_{Total} (mW)	SNDR (dB)
1.11E+05	2.00E+05	0.2086	0.021	0.230	55.5
6.25E+04	2.00E+05	0.1172	0.017	0.134	55.5
3.34E+04	2.00E+05	0.0628	0.015	0.077	55.6
1.72E+04	2.00E+05	0.0333	0.013	0.046	55.6
8.77E+03	2.00E+05	0.0176	0.012	0.030	55.5
4.42E+03	2.00E+05	0.0095	0.012	0.021	55.6
2.22E+03	2.00E+05	0.0054	0.012	0.017	55.4
1.12E+03	2.00E+05	0.0035	0.012	0.015	55.6
5.58E+02	2.00E+05	0.0041	0.012	0.016	55.5

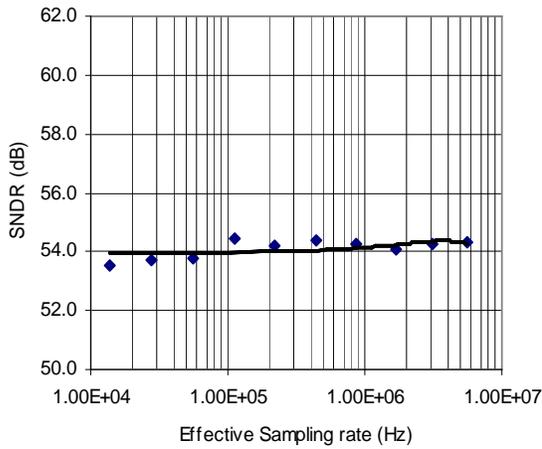


Fig. 6-37: SNDR variation with effective sampling rate for $f_{sm}=50\text{MHz}$

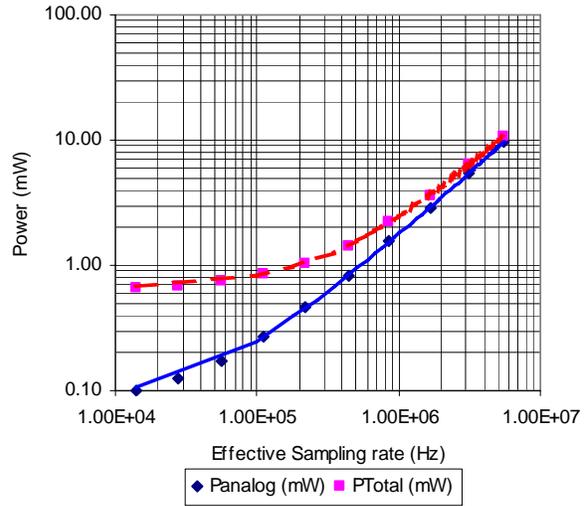


Fig. 6-38: Analog and Total ADC power variation with effective sampling rate for $f_{sm}=50\text{MHz}$

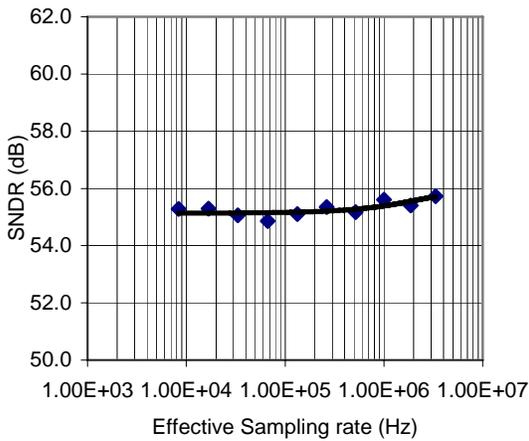


Fig. 6-39: SNDR variation with effective sampling rate for $f_{sm}=30\text{MHz}$

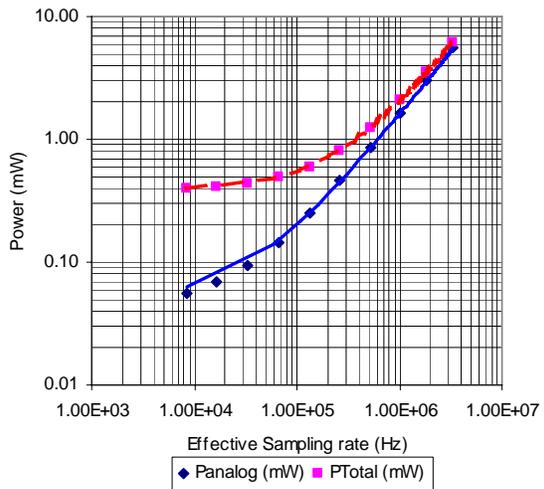


Fig. 6-40: Analog and Total ADC power variation with effective sampling rate for $f_{sm}=30\text{MHz}$

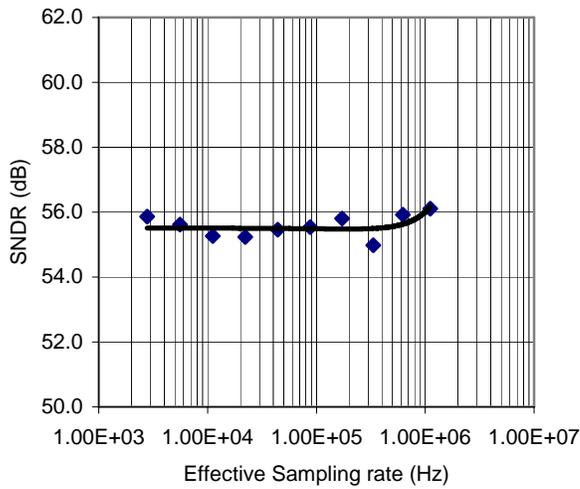


Fig. 6-41: SNDR variation with effective sampling rate for $f_{sm}=10\text{MHz}$

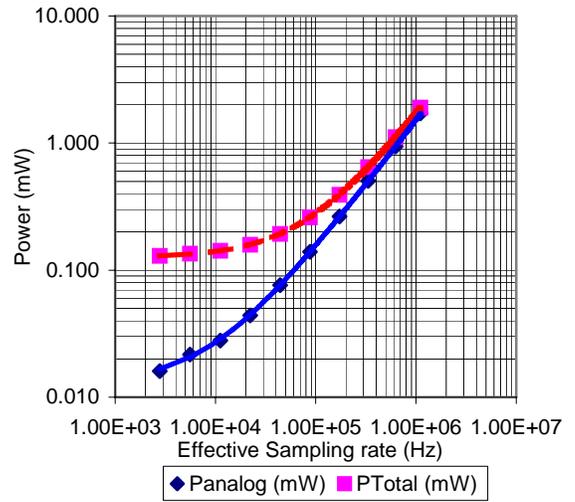


Fig. 6-42: Analog and Total ADC power variation with effective sampling rate for $f_{sm}=10\text{MHz}$

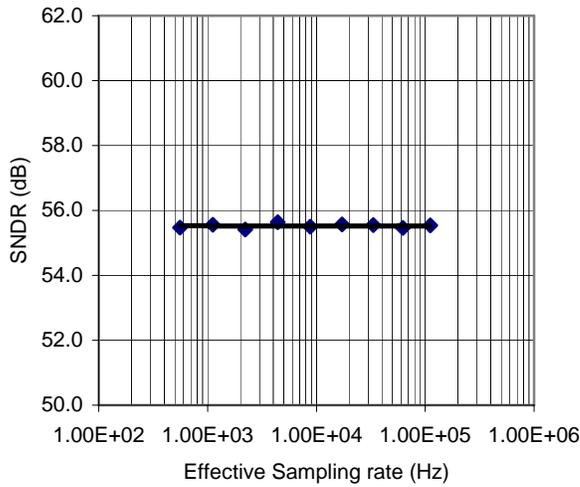


Fig. 6-43: SNDR variation with effective sampling rate for $f_{sm}=1\text{MHz}$

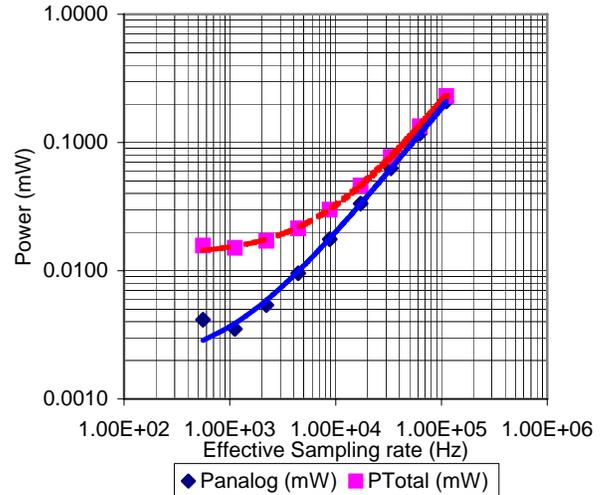


Fig. 6-44: Analog and Total ADC power variation with effective sampling rate for $f_{sm}=1\text{MHz}$

As predicted, the SNDR changes minimally over effective sampling rate, since the bias currents remain constant between sampling rates (only the off time changes, as described in section 5.2). From the above figures, the ADC power is shown to scale with sampling frequency, where for lower sampling rates for a particular f_{sm} , the power scaleable range is ultimately limited by the power of the digital state machine. As shown in Table 6-5 to Table 6-8, the state machine power can be reduced by reducing the state machine clock speed, thereby lowering the lowest power scaleable sampling rate. If the analog power is scaled with the clock supplied to the state machine so as to minimize analog power however, the lowest possible sampling rate achievable is limited by the sensitivity of the application in question to the problems of devices biased deep in weak inversion (as described in chapter four). (E.g.): if the yield, and bias point sensitivity of the ADC with bias currents adjusted to 1Msps were tolerable; the lowest sampling rate achievable from Table 6-8 is 580Hz (~100,000x power scaleable range). However if the desired yield and bias point sensitivity required the bias current to be scaled by no more than 1:5 (i.e. 50MHz-10MHz), the lowest power scaleable sampling rate is 2.8kHz (~20,000x power scaleable range). Thus the limiting factor of the CMPS approach is ultimately the limits of transistor performance in weak inversion – however as CMPS multiplies the power scaleable range of current scaling by a large factor (>1000x in the fabricated chip), much lower effective sampling rates with scaled power can be achieved than if the current scaling method were alone used to make power a function of sampling rate.

From the measured results, the ADC requires a higher mW/Msps when using CMPS compared to current scaling. The increased power when using CMPS is only due to a sub-optimal power-triggering scheme. As mentioned in chapter five, to simplify the logic of the state machine, all bias circuits were activated at the same time. If the state machine were redesigned to include more programmability, the timing for each bias circuit could be optimized such that the individual bias circuits are powered on for the minimum time required. As the power of all bias circuits is comparable to single pipeline stage, a significant power reduction can be realized through careful power timing optimization.

The complete power scaleable range showing the use of current scaling over a narrow range of sampling rates (1-50Msps), and CMPS applied to the narrow range of current scaled sampling rates is shown in Fig. 6-45.

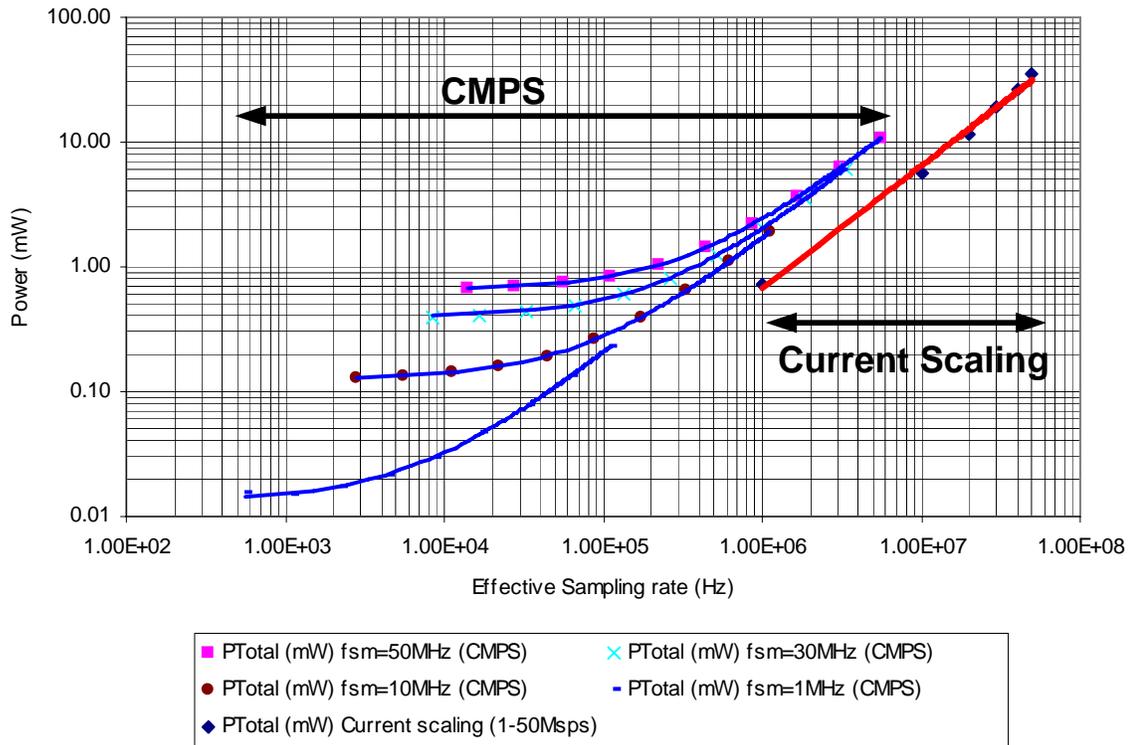


Fig. 6-45: Power scaleable range of ADC with CMPS applied to current scaled sampling rates of 1-50Msps

Thus from Fig. 6-45, with CMPS applied to current scaled sampling rates between 1-50Msps, it is possible to achieve a power scaleable power for sampling frequencies as low as 580Hz (16 μ W), and as high as 50MHz (35mW).

As the bias currents remain fixed between sampling rates when using CMPS, the advantages of transistors biased in strong inversion can be preserved for low sampling rates, where if current scaling were used, the transistors would be in weak inversion. A specific example displaying strong inversion performance at low sampling rates is the bias sensitivity of the ADC. As shown in Fig. 6-36, for lower sampling rates where current is scaled to achieve

lower power for lower sampling rates, the variation of ENOB with bias voltage becomes much larger when the ADC is biased in weak inversion. In Fig. 6-46, the variation of ENOB with bias voltage is shown for $f_s=1\text{Msps}$ and $f_s=100\text{kps}$ when the CMPS is used to power scale (with $f_{sm}=50\text{MHz}$), and when current scaling is used to power scale.

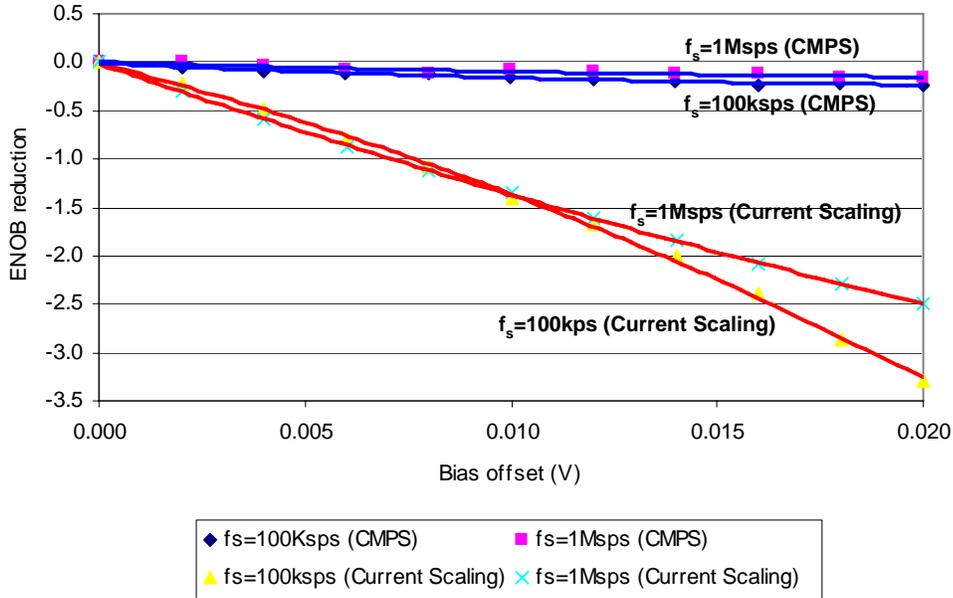


Fig. 6-46: Bias point variation of ADC using CMPS and current scaling for $f_s=1\text{Msps}$, and $f_s=100\text{kps}$

As expected, the ADC maintains strong inversion performance when CMPS is used, as evident from the small reduction in ENOB with bias voltage variation. Thus for lower sampling rates where CMPS is used, performance and yield degradation associated with weak inversion are minimized.

6.6: Simulated vs. Measured results

Simulated and measured SNDR for $f_s=1\text{--}80\text{Msps}$ of the ADC is shown in Fig. 6-47.

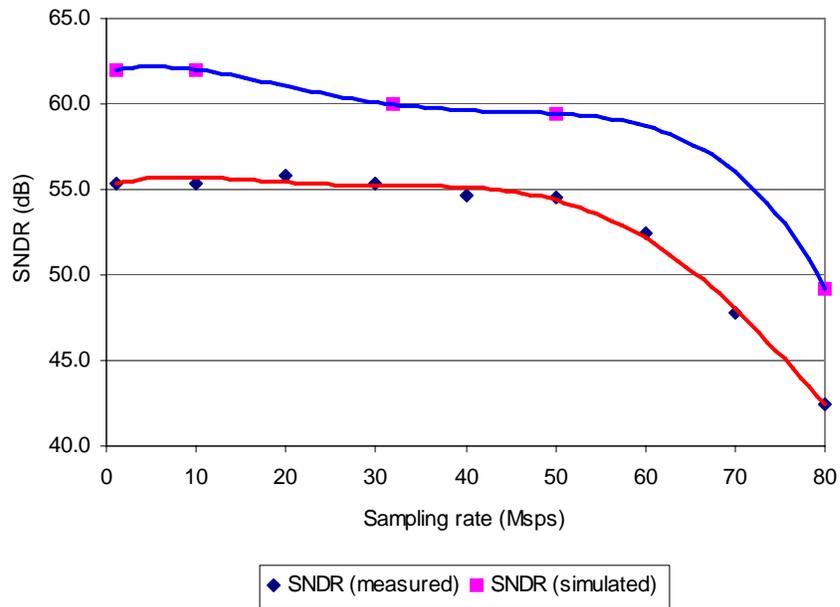


Fig. 6-47: Expected and measured SNDR of ADC for $f_s=1-80\text{Msps}$

Measured results show a loss of 5-6dB in SNDR between simulated and measured results. One possible reason for the performance degradation is noise coupling from the digital circuitry (on-chip I/O pad drivers, clock buffers) into the sample and held signals of each pipeline stage. This can be seen in output spectrums for $f_s=50-10\text{Msps}$ in Fig. 6-7→Fig. 6-12. For the higher sampling rates several spurs at frequencies not multiples of the input (i.e. not second, third, fourth, etc. harmonics) appear in the spectrum, which likely are due to noise the I/O drivers for each pipeline stage's digital output. For lower sampling rates (e.g. 10Msps), fewer spurs are present in the output spectrum likely due to the higher AC impedance from capacitive coupling between I/O pads and the analog core.

Although fewer spurs are present in the output spectrum for $f_s=10\text{Msps}$, the measured results still show an SNDR ~5dB below simulated results. Some of the performance degradation at 10Msps can be attributed to noise from the I/O pads, however as the measured SNDR peaks at ~56-57dB for f_s below 10Msps, the performance limitation must be white in nature. As described in section 3.3.2, white noise sources included capacitor and opamp noise. One problem with the formula used to derive the minimum capacitor size (equation 3.5) is that it depended on an approximation of opamp noise, and opamp input capacitance. It is possible

that due to process variation/layout parasitics, the expected opamp input capacitance varied significantly from the expected input capacitance used in the calculations. For latter stages in the pipeline where the feedback capacitors are on the order of tens of femto Farads, a small absolute variation in opamp input capacitance can easily occur, increasing the uncertainty of the LSB. As mentioned in section 5.18, transient simulations including thermal noise were not performed due to limited computing power, thus it is possible that if a transient simulation including thermal and opamp noise were performed, the 5-6dB loss of performance could be accounted for.

6.7: Conclusion

This chapter presented measured results of fabricated ADC in 0.18 μ m CMOS, which has its power a function of sampling rate. Power scalability was shown to be achieved for sampling rates greater than 50Msps (35mW), and lower than 1ksps (15 μ W), while maintaining ~55dB of SNDR. The benefits of powering off the MDAC opamps during the sampling phase were quantified, where a reduction of power by 20-30% was measured. Increased bias voltage sensitivity as the ADC is driven into weak inversion operation was empirically quantified. The benefit of strong inversion design for low sampling rates using CMPS was shown where bias voltage sensitivity was compared for the ADC using current scaling and CMPS, where in CMPS the ADC shows minimal accuracy degradation with bias voltage fluctuation.

CHAPTER SEVEN

Conclusions

7.1: Summary

In this dissertation a pipeline ADC that has its power as a function of a wide range of sampling rates was presented. The ADC was shown to achieve power scalability without driving the ADC deep into the weak inversion region, thereby avoiding the problems of less accurate simulation, poorer matching, increased bias voltage sensitivity, and poorer yield. Although used in industry, the Current Modulated Power Scale technique independently developed for this dissertation had previously not been applied to ADCs faster than a few hundred ksp/s. As such previous power scaleable ADCs were relegated to slower architectures (e.g. SAR, cyclic, etc.), due to the lack of available circuits which can power on/off in short time intervals. The key to power scalability at high sampling rates in this dissertation was the development of a Power Resettable Opamp (PROamp), which by virtue of a replica bias technique, is able to completely and quickly power on/off. The application of the PROamp to a high speed pipeline architecture in parallel with current scaling over a relatively small range (1:50) was shown to result in an ADC which had its analog power a function of frequency for frequencies lower than 1ksp/s (15 μ W), and higher than 50Msp/s (35mW) while maintaining an SNDR of 54-56dB over the entire power scaleable range. The development of the PROamp was also shown to be highly useful in reducing power of pipeline ADCs, by completely powering off the MDAC opamp during the sampling phase. Measured results showed a 20-30% decrease in overall ADC power between $f_s=1-50$ Msp/s when MDAC opamps were powered off during the sampling phase. The use of the PROamp to reduce opamp power in high speed and precision circuits is of great use, as opamp power typically constitutes the majority of power consumed in analog circuits. Sampling rate and associated power for f_s between 1ksp/s and 50Msp/s for the power scaleable ADC of this dissertation are summarized in Table 7-1.

Table 7-1: Sampling rates and power for $f_s=580-50\text{Msp}$ s

f_s	P_{total}	$SNDR$ (dB)
50Msp	35mW	55
30Msp	19mW	56
10Msp	5.6mW	56
1Msp	700uW	55
111ksps	230uW	56
8.7ksps	87uW	56
1ksps	15uW	56
580sps	16uW	56

7.2: Future research

As the goal of this work was proof-of-concept, rather than absolute figure-of-merit, future research could involve using the ideas developed in this thesis to design a power scaleable ADC, or conventional ADC which targets figure-of-merit. For example, from Table 3-2 the state of the art pipeline ADC is shown have a FOM of 0.8pJ/step [35]. It is conceivable that the application of the PROamp to the design approach of [35] could reduce the FOM by over 30%. Furthermore, the PROamp could be used to develop other switched capacitor circuits with reduced power (e.g.: discrete-time-filters/integrators, sample and holds, etc.)

The focus of this dissertation has been reconfigurable power, however the techniques used to achieve power scalability also allow for bit-reconfigurability. For example, if a 6-bit ADC were required, only the first six stages could be triggered on/off in power scale mode (as opposed to eight), where the bias current to the ADC could be reduced such that the first pipeline stage is bandwidth limited to ~6-bit accuracy, thus minimizing ADC power according to the desired accuracy. To maximize bandwidth, the sampling/feedback capacitors could be switched in according to the desired accuracy. Through the design of a state machine with greater programmability, the on/off timing of each analog block in the ADC could be fine tuned, potentially significantly reducing the power of the ADC while using CMPS. Future developments of the CMPS architecture could also include power on/off triggering on-chip reference voltages.

A significant advantage of the CMPS technique is the ability to design very low power ADCs using conventional design techniques with transistors biased in strong inversion with large bias currents. As low power design presents a significant design challenge for low speed/low power applications (e.g. biomedical, mobile), the techniques developed in this dissertation could be used to develop new ultra low power ADCs without resorting to the difficult design of transistors biased in weak inversion and/or with very low bias currents. Furthermore as CMPS avoids biasing transistors with small currents, future work could entail developing low power ADCs in smaller technologies (e.g. $L=0.09\mu\text{m}$), where biasing transistors with small currents to achieve low power would be difficult due to the bias currents being on the order of significant leakage currents.

7.3: Key developments of this work

- 1.) The development a technique to achieve scaleable power in ADCs, using a Current Modulated Power Scale (CMPS) technique, which can enable low power ADC design without biasing transistors with small currents and/or operating transistors deep in weak inversion.
- 2.) The application of CMPS to a pipeline ADC to achieve power scalability over wide variations in sampling rate for frequencies greater than 50Msps (35mW) and lower than 1ksps (15 μ W).
- 3.) The development of an opamp that can completely power on/off in a short time period – the Power Resettable Opamp (PROamp).
- 4.) The demonstration of opamp power reduction at high sampling rates by completely powering off MDAC opamps during the sampling phase for f_s between 1-50Msps.

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