Design of a Wideband Quadrature Continuous-Time Delta-Sigma ADC

by

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Abstract

Delta-sigma (ΔΣ) modulation is a popular technique for making high resolution analog to digital and digital to analog converters (ADC and DAC). This thesis outlines a design procedure for a low power, wide bandwidth, 4^{th} order continuous-time complex bandpass ΔΣ ADC. System level simulations of the modulator are used to examine the behavior of the modulator in presence of moderate circuit imperfections. The modulator was designed and fabricated in TSMC's 0.18μm CMOS technology. The ADC achieves 68.8dB SNDR in a 23MHz signal bandwidth while consuming 42.6mW from a 1.8V supply. The core area of the IC is $0.95mm^2$. This work demonstrates the feasibility of implementing a high-resolution high-speed ΔΣ ADC suitable for a low-IF receiver in deep sub-micron technology using low-gain opamps.

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CHAPTER 1 *Introduction*

Advances in VLSI technology allow the realization of high speed, densely packed digital circuits. To take advantage of this fact, it is highly desirable in telecommunication and signal processing applications to implement as much of the functionality as possible in the digital domain. However, real world signals are inherently analog, so analog to digital and digital to analog converters (ADCs and DACs) are required to interface the analog world with the digital world.

One technique for realizing high resolution ADCs and DACs is delta-sigma ($\Delta\Sigma$) modulation. The significant advantage of this scheme is that signals are converted using a low resolution quantizer and the precision of much of the analog circuitry is usually less than the resolution of the overall converter. The cost of this gain in resolution is that the signal must be sampled faster than necessary.

The most common application of these types of ADC is in the audio field where they are used to digitize narrowband signals with very high accuracy [4]. However there are many applications such the 802.11 wireless LAN standard which require a wideband ADC. For these applications pipeline ADCs are typically employed, however a lower power consumption can be achieved by using $\Delta\Sigma$ ADCs for the same given resolution and signal bandwidth.

In a typical low-IF wireless receiver, downconversion to a non-zero IF is accomplished using quadrature or image reject mixers. The use of an image reject mixer in the signal path relaxes the off-chip filtering requirements of the receiver. A quadrature bandpass $\Delta\Sigma$ ADC can digitize the signal band accurately while simultaneously the image band is only coarsely quantized. This can lead to a significant power saving as power is not wasted to perform accurate A/D conversion on the image band. This thesis covers the design of a low power, wideband continuous-time 4^{th} order quadrature bandpass $\Delta\Sigma$ modulator.

1.1 Thesis Outline

An overview of Nyquist and oversampling converters is given in chapter 2. A brief background on low-pass modulator theory is presented. A description of complex signals and complex filters is followed by a description of quadrature bandpass ΔΣ ADC. The desired modulator specifications are described in chapter 3 and two different modulator topologies are examined. Chapter 4 uses system level simulations to quantify the amount of tolerable component imperfection. Circuit specifications are also found in chapter 4. In chapter 5 the design of the modulator is presented. It is implemented in TSMC's 0.18μm CMOS process. Transistor level simulations of the circuits are used to verify functionality of the modulator. Measured results are presented in chapter 6. Chapter 7 concludes the thesis and makes suggestions for future work.

CHAPTER 2

Delta-Sigma Background

This chapter presents an overview of analog to digital conversion. The ideal SNR performance of Nyquist rate and oversampling converters is examined. A brief background on low-pass modulator theory is presented. The advantages and disadvantages of using a continuous-time loop filter as well as multi-bit feedback DAC are discussed. A simple and fast algorithm for reducing the effects of DAC mismatch is also discussed. Complex signals and complex filters are reviewed and the performance of complex filters in presence of filter mismatches is examined.

Quadrature bandpass ΔΣ ADC is presented as the generalization of real ΔΣ modulators. The performance of quadrature modulators in presence of filter mismatches is examined and is shown to give rise to two image transfer functions that are not present in a real modulator. An algorithm for reducing the effects of the image transfer functions is also discussed.

2.1 Analog to Digital Conversion

An analog to digital converter (ADC) is a device that converts a continuous-time analog signal, such as voltage or current into a discrete-time signal, with finite precision. In order to flawlessly reconstruct the continuous-time signal from its sampled values, Nyquist's sampling theorem states that the minimum sampling rate (f_S) must be at least twice the signal bandwidth (f_B). The bandlimit criteria can be strictly enforced by inserting a filter with a cut-off frequency of less than $f_S/2$ before the sampling operation to bandlimit the signal and avoid aliasing effects.

An ideal *n*-bit linear ADC has 2^n quantization steps. Assuming an input signal with a range of ±1, the quantizer step size is

$$\Delta = 2/2^n \qquad (2.1)$$

Assuming Δ is small, the error introduced due to the quantization process is a random variable uniformly distributed over $[-\Delta/2,\Delta/2]$. Under these assumptions, the power of the error signal, is

$$\sigma_e^2 = \Delta^2/12 \qquad (2.2)$$

The largest sine-wave signal that does not overload the ADC has an amplitude of 1 and a power of -3dB relative to a DC input with an amplitude of 1. A simple calculation shows that the maximum signal-to-noise ratio (SNR) of an ideal *n*-bit linear ADC with a sinusoidal input is 6.02*n* + 1.76dB [3]. A more general definition of resolution that takes into account the non-linearity of the ADC is based on the signal to noise and distortion ratio (SNDR) measurement. The effective number of bits (ENOB) is a measure that compares an ADC's actual SNDR to that of an ideal n bit ADC and is defined as

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{2.3}$$

For example, an ADC with a 98dB SNDR achieves 16 ENOB.

In a conventional Nyquist rate ADC, higher SNR is achieved by reducing Δ. However small steps require precisely-matched analog components. This increases the cost of the ADC as it usually requires trimming or a process with better matching characteristics.

Another technique for increasing the SNR of an ADC is to oversample the signal followed by decimation. A decimator is a low pass filter combined with a down-sampler. Oversampling is simply sampling the input faster than the Nyquist criterion requires. The oversampling ratio (*OSR*) is defined as the ratio of the sampling rate over the Nyquist sampling rate of the desired signal

$$OSR = f_s / 2f_B \tag{2.4}$$

Increasing *OSR* has the effect of decreasing the in-band quantization noise and thereby improving SNR, since quantization noise is fixed and independent of sampling frequency. Assuming that the quantization noise has a white spectrum, it is easy to show that for every octave increase in *OSR*, the resolution of the ADC is increased by 0.5bit (i.e. 3dB decrease in quantization noise power).

Note that in this scheme we are trading speed for resolution. The higher resolution is obtained at the expense of faster sampling rate. Analog circuit complexity has also been traded for digital circuit complexity in the form of a decimator. The analog circuitry has been simplified because we require a quantizer with lower number of levels to achieve the required resolution. Another benefit, which is a direct consequence of oversampling is that the anti-alias filter does not need a very sharp cutoff. The transition band of the anti-alias filter can be from f_B to f_s - f_B, which for large *OSR* can be quite wide. The following section will briefly explain how $\Delta\Sigma$ modulation can improve on the resolution-sampling rate trade-off.

2.2 Delta Sigma Modulator Theory

The basic principal behind ΔΣ modulation is that of feedback and filtering around a low-resolution quantizer [1]. Fig. 2.1 shows a general block diagram of a ΔΣ modulator. The loop transfer functions L_1 and L_0 have very high gain in a narrowband (ideally infinite gain at frequencies for which $H(z) = 0$). Due to the negative feedback action of the loop, the actual resolution after filtering is much better than the resolution of the quantizer. This is accomplished by oversampling the input and feeding back the output from the quantizer to a resonator circuit. Assuming that the system is stable, the error at the loop filter's resonant frequency must be small. Therefore the output closely represents the input around a narrow frequency band for which the loop filter possesses high gain. Note that the poles of L_1 correspond to the zeros of the $H(z)$.

The modulator consists of two sections: a linear block (the loop filter) and a nonlinear block (the quantizer). Assuming for now that the loop filter is a discrete-time filter, the output of the linear block can be written as

$$Y(z) = L_0(z)U(z) + L_1(z)V(z) \qquad (2.5)$$

Modeling the quantizer in Fig. 2.1 as an additive white noise source $E(z)$, (i.e. $V(z) = Y(z) + E(z)$), Eq. (2.5) can be rearranged to give the output of the modulator in terms of its input and the error signal

$$V(z) = G(z)U(z) + H(z)E(z) \qquad (2.6)$$

With appropriate choice of the loop filters, $G(z)$, the signal transfer function (STF) will pass signals in a certain frequency band, while $H(z)$, the noise transfer function (NTF) will attenuate the quantization errors in that band, and so the signal can be separated from the noise by digital filtering. Thus the output can faithfully represent the input in a narrowband where $H(z)$ is small. The loop filter can be implemented using either discrete-time filters such as switched-capacitors

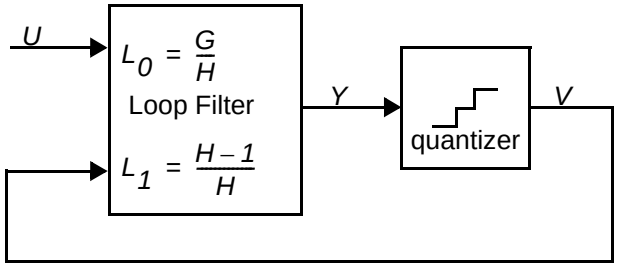

Fig. 2.1 A general block diagram of a ΔΣ modulator.

(SC) or it can be implemented using continuous-time filters, for example LC tanks, g_m-C or active-RC filters or even a combination [21].

Oversampling increases SNR by spreading a fixed quantization noise power over a bandwidth that is larger than the signal bandwidth. Noise shaping or modulation further attenuates this noise in the band-of-interest and amplifies it outside the passband. This process can be viewed as pushing quantization noise power from the signal band to other frequencies. Note, a similar equation to Eq. (2.6) can be used to describe the output of a Nyquist rate converter, where the NTF is $H(z) = 1$ (i.e. no noise shaping).

The three most important parameters in determining the performance of a ΔΣ modulator are its OSR, NTF and the number of quantization levels. By increasing *OSR*, in-band noise is reduced and hence SNR is increased. The number of levels in the quantizer determines the amount of quantization noise that is to be suppressed by the NTF. The NTF determines the in-band quantization noise attenuation, thus the maximum SNR that the modulator can achieve for a given value of *OSR*. $H(z)$ must be designed to minimize the in-band noise under two constraints: one for causality and one for stability. The loop around the quantizer cannot be delay-free, so $H(z) - 1$ must be strictly causal (i.e. first impulse-response coefficient zero). This constraint forces

$$\lim_{z \to \infty} H(z) = 1 \qquad (2.7)$$

which indicates that $H(z)$ can not be set to zero everywhere. Making $H(z)$ small in-band forces it to be greater than unity out-of-band [1].

The stability of a ΔΣ modulator is a much less understood problem [1], [4]. Ensuring that $H(z)$ is stable does not guarantee that the modulator will be stable. However, according to Lee's rule-of-thumb [2], for binary modulators, stability is ensured if the following constraint is met

$$\left|H(e^{j\omega})\right| < 2 \qquad (2.8)$$

This rule is approximate in nature and it is possible to find stable modulators for which Lee's rule is violated. Since stability of a ΔΣ modulator is an unsolved problem, transient simulation of the non-linear model with large inputs is the only way to verify that the modulator will be stable.

To illustrate the properties discussed, consider the simple first order low-pass ADC, MOD1 (Fig. 2.2a) [4]. The quantizer used in this modulator is a single bit comparator. The quantizer may be "linearized" by modeling it as a device that only adds white noise to the output (Fig. 2.2b). The output of the modulator is then

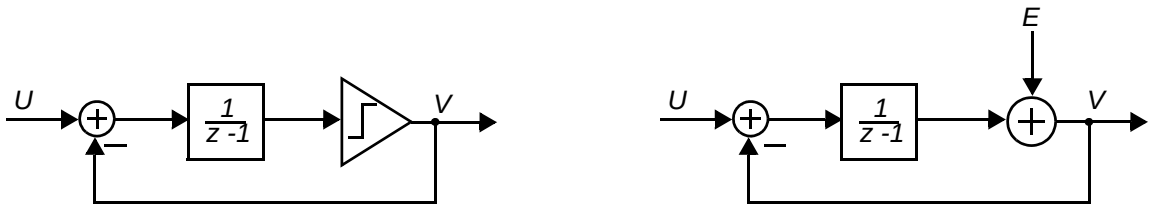

Fig. 2.2 (a) MOD1: A first order ΔΣ ADC (b) linearized MOD1.

$$V(z) = z^{-1}U(z) + (1 - z^{-1})E(z) \tag{2.9}$$

The STF of this modulator is z^{-1}, which is simply the input delayed by one clock period. The magnitude of the NTF is given by

$$\left|H(e^{j\omega})\right| = 2\sin(\omega/2) \approx \omega \text{ for large } OSR \tag{2.10}$$

It has been shown in [3] that for a binary 1st order modulator, the SNR is given by

$$SNR = 10\log(\sigma_s^2) - 10\log\left(\frac{\pi^2}{9OSR^3}\right) = 10\log(\sigma_s^2) - 0.4 + 30\log(OSR) \tag{2.11}$$

where σ_s^2 is the signal power. According to the linear model, for every octave increase in *OSR*, SNR will improve by 9dB or 1.5 bits. For systems with higher-order NTFs the increase in SNR with increase in *OSR* is even greater. In general, the resolution of a ΔΣ modulator is increased by clocking faster and increasing the NTF order. SNR may also be improved by increasing the maximum out of band gain of the NTF ($\|H(z)\|_\infty$). However according to Lee's rule of thumb, a binary modulator is likely to be become unstable if $\|H(z)\|_\infty$ is larger than 2.

A low-pass modulator is one in which the NTF zeros have been placed at or very close to DC and so the output accurately represents the input in a narrow band around DC. A bandpass modulator shifts the zeros away from DC to a non-zero frequency f_0. Quantization noise is suppressed at f_0 and therefore the output accurately represents the input in a narrow band around f_0. The primary advantage of a bandpass ΔΣ modulator is that the oversampling ratio is no longer f_s/f_0 but rather f_s/f_B where f_B is the signal bandwidth. Therefore *OSR* can be made quite large without having to sample the signal much faster than its Nyquist rate. The second major advantage of a bandpass modulator is that it avoids DC related problems that are normally associated with downconversion to DC such as DC offset and flicker (1/*f*) noise.

However this comes at the expense of a faster loop filter since the resonant frequency of the filter is shifted to a higher frequency. The zeros of a real NTF must also occur in conjugate pairs and so for a given NTF order, the amount of noise suppression that a bandpass NTF can achieve is approximately half of what a low-pass NTF can achieve. Consequently, for a given signal band-

width and resolution, bandpass modulators tend to consume more power compared to their lowpass counterparts.

To shift the NTF zeros to a non-zero frequency, the loop filter is modified so that its resonant frequency is somewhere other than DC. This may be implemented with either discrete-time or continuous-time circuitry. The main advantages of a continuous-time loop filter is that because the sampling operation is done at the output of a continuous-time loop filter, alias frequencies are suppressed by the loop filter [8]. To illustrate this point, consider the following: suppose a signal at an alias frequency of f_0 (e.g. $f_s + f_0$) is applied at the input. Now if this system had no anti-alias properties, that signal would be aliased back to f_0 at the feedback DACs (the quantizer is clocked) and because the filter has very high gain at f_0, the system would become unstable. Therefore if the system is to be stable then no aliased signal can be fed back through the feedback DACs. Furthermore, the sampling errors are noise-shaped along with the quantization errors and thus the requirements of the sample and hold block are reduced. However the disadvantage of a continuous-time modulator is that it is sensitive to the DAC output over the entire feedback period, unlike a discrete time implementation which relies only on the final settled output value of the feedback DAC. For example clock jitter will corrupt the output of the feedback DACs. Non-complementary DAC rise and fall times are an additional source of error. The first feedback DAC is especially critical since noise introduced at the first stage resonator will not be shaped by the loop filter.

2.3 Multi-Bit Modulators

One method of increasing the SNR of the modulator without increasing the order of the modulator or its sampling rate is to replace the binary feedback DAC with a multi-bit DAC. A multi-bit DAC improves the SNR in two ways. The first improvement is due to the lower quantization noise level of a multi-bit DAC. For every extra bit of resolution, the SNR is improved by 6dB. The second significant advantage is that a multi-bit modulator is more likely to be stable than a single-bit modulator. This is because the assumption that the quantizer can be modeled as additive white noise will be much more accurate with a multi-bit quantizer in the feedback path. Therefore the linear model can more accurately predict the stability of the modulator. Thus NTFs with higher out-of-band gain and therefore lower in-band gain can be used. However the major disadvantage of using a multi-bit feedback DAC is that the linearity of the overall modulator may be determined

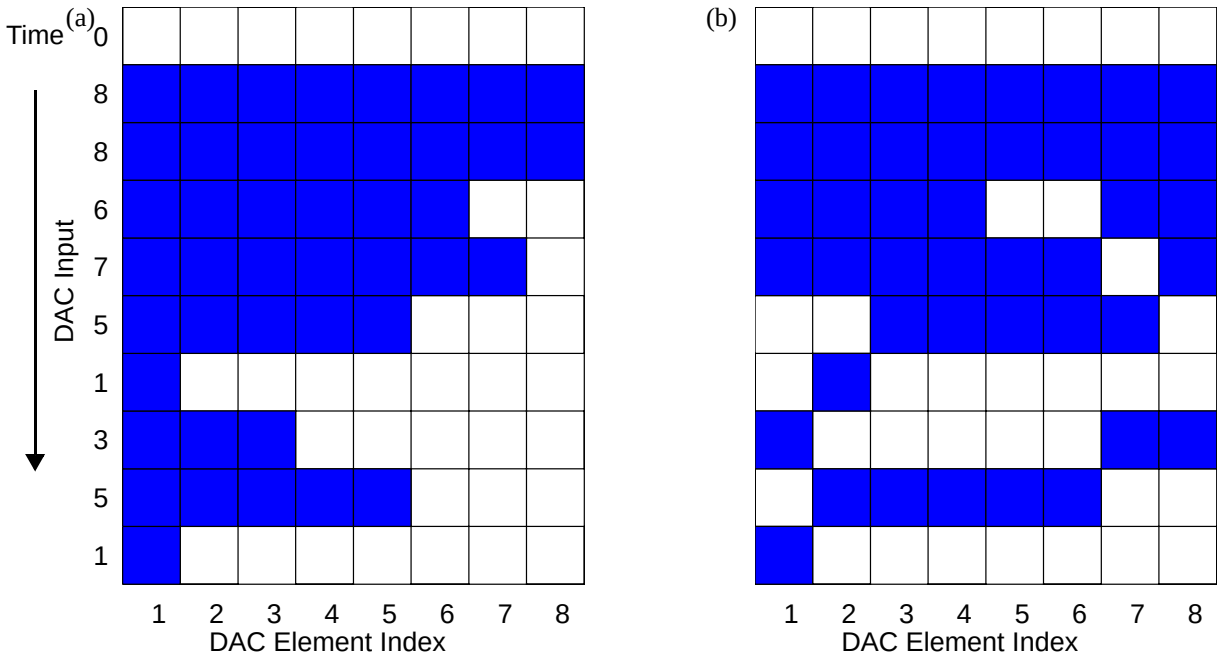

Fig. 2.3 (a) Example of a DAC usage pattern with no mismatch shaping. (b) Example of a DAC usage patter with a DWA algorithm. Note: each filled box represents a unit element of a thermometer coded DAC that is to be turned on. The output is the sum of all the elements turned on.

by the feedback DAC, since any noise or non-linearity at the output of the first DAC will appear directly at the input of the ADC [4].

A simple, fast and effective method of linearizing the feedback DAC is to use the data-weighted averaging scheme [19]. In this scheme the individual DAC elements are chosen in a rotating fashion which results in a first order shaping of the DAC errors. A DAC using a DWA rotation scheme can be conceptually thought of as integration and a differentiation operation. Since the error due to DAC element mismatch is introduced after the integration operation, the errors will be shaped by a lowpass transfer function. This implies that the spectrum of the error signal at low frequency will be small, hence the DAC will be "linear" at low frequencies. A plot of a typical DAC usage pattern is shown in Fig. 2.3. The following section provides background information on complex signals and filters.

2.4 Brief Background on Complex Signals and Complex Filters

A complex signal is essentially a baseband representation of a bandpass signal. A complex signal can be thought of as a convenient representation of two real signals, $m_1(t)$, $m_2(t)$. The complex

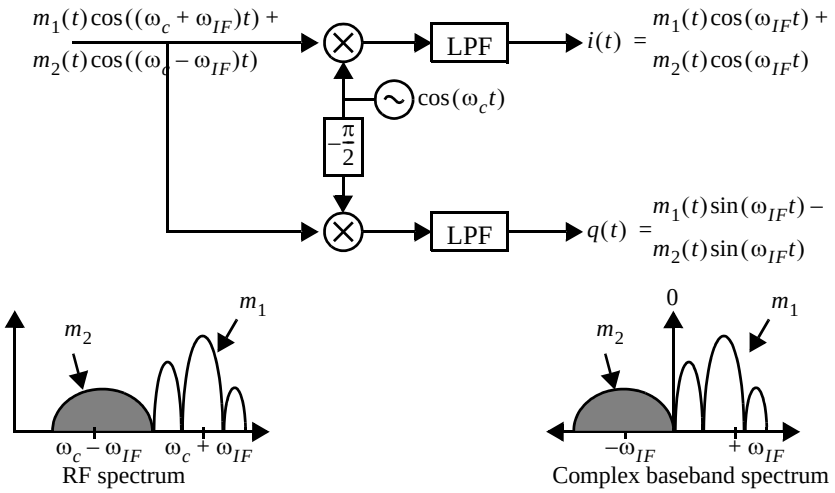

Fig. 2.4 Low-IF down conversion using an image reject mixer.

valued signal is interpreted as $m(t) = m_1(t) + jm_2(t)$. One of the most important characteristics of a complex signal is that its spectrum does not have to exhibit any symmetry about DC. One way of generating a complex signal from a set of two real signal sources (e.g. a signal from an antenna in a radio receiver) is by multiplying the real signal by $e^{j\omega_c t} = \cos(\omega_c t) + j\sin(\omega_c t)$. Suppose that a modulated signal is present at a carrier frequency of $\omega_c + \omega_{IF}$ in addition with an unwanted signal at $\omega_c - \omega_{IF}$. The output of the system shown in Fig. 2.4 when treated as a single complex quantity is proportional to

$$y(t) = i(t) + jq(t) = m_1(t)e^{j\omega_c t} + m_2(t)e^{-j\omega_c t} \qquad (2.12)$$

Note that, the spectrum of the $y(t)$ contains two distinct signals. One at the positive frequency band ($+\omega_{IF}$) and another at the negative frequency band ($-\omega_{IF}$). Note this result was arrived by assuming that the I and Q channel are perfectly matched (both in terms of phase and magnitude) and furthermore the phase shifter changes the phase of the local oscillator (LO) by exactly 90°. In practice none of these assumptions will be perfectly true. When the assumptions are violated, some of the energy in the positive frequency band will leak into the negative band and vice versa. In other words the unwanted signal at $\omega_c - \omega_{IF}$ will interfere with the signal present at $\omega_c + \omega_{IF}$ and cause the image signal to alias in-band.

In a direct-conversion architecture, the intermediary frequency (IF) is zero (i.e $\omega_{IF} = 0$). The interfering signal, is the desired signal itself and so very little attenuation of the image signal is necessary [1]. However this type of receiver suffers from DC-offset and $1/f$ noise problems. This limits the usefulness of the direct-conversion receiver to modulation schemes that do not contain much

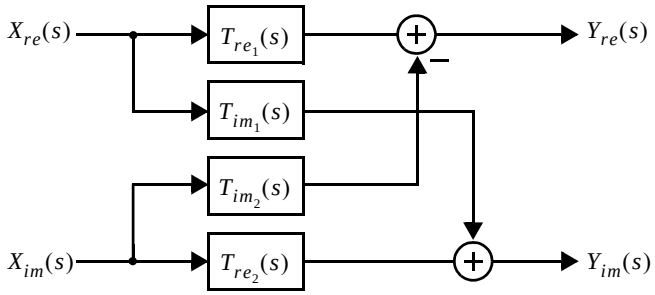

Fig. 2.5 Block diagram of a generalized complex filter.

energy at low frequencies [6]. A non-zero IF is used in a low-IF type receivers to avoid low frequencies noise. However, since the signal at the positive frequency band ($\omega_c + \omega_{IF}$) is unrelated to the signal at the negative frequency band ($\omega_c - \omega_{IF}$), the interfering signal can be much larger than the desired signal. It is the job of the image-reject filter to attenuate the image signal at $\omega_c - \omega_{IF}$ before it gets to the mixer. Using a single IF stage requires a very sharp RF filter (high Q) to block the image signal. This filter can not be implemented efficiently on-chip. However with the use of an image-reject mixer, the attenuation requirements of the image-reject filter can be relaxed.

A complex filter is simply a filter that operates on complex signals, such as that from an image-reject mixer. It is a two input, two output system with the inputs and outputs being treated as complex quantities. The filter may conceptually be thought of as several cross-coupled real filters. A block diagram of a generalized complex filter is shown in Fig. 2.5. The input and output of the system are treated as $X(s) = X_{re}(s) + jX_{im}(s)$ and $Y(s) = Y_{re}(s) + jY_{im}(s)$ respectively. Assuming $T_{re_{nom}}(s) = T_{re_1}(s) = T_{re_2}(s)$ and $T_{im_{nom}}(s) = T_{im_1}(s) = T_{im_2}(s)$ then it is easy to show that the transfer function of the filter is

$$T_{nom}(s) = T_{re_{nom}}(s) + jT_{im_{nom}}(s) \qquad (2.13)$$

However, due to coefficient mismatches the real and imaginary paths will not be identical and so the system will not realize a pure complex transfer function. It has been shown that the output of a mismatched complex filter can be written as sum of two terms [5]: one operating on the complex input and the other operating on its conjugate. The output of the filter is then written as

$$Y(s) = T(s)X(s) + T_{img}(s)X^*(s) \qquad (2.14)$$

where $X^*(s)$ denotes the complex conjugate of the input,

$$T(s) = \frac{T_{re_1}(s) + T_{re_2}(s)}{2} + j\frac{T_{im_1}(s) + T_{im_2}(s)}{2} \qquad (2.15)$$

and

$$T_{img}(s) = \frac{T_{re_1}(s) - T_{re_2}(s)}{2} + j\frac{T_{im_1}(s) - T_{im_2}(s)}{2} \quad (2.16)$$

The image transfer function, $T_{img}(s)$ will cause signals present in the image band to leak into the band of interest. Image rejection ratio (IRR) defines the effectiveness of a complex filter in passing in-band signals while rejecting signals in the image-band. For example, a filter that passes the desired signal with a 0dB gain and passes an image signal with 40dB attenuation has an IRR of 40dB.

2.5 Quadrature Modulator and Effect of Filter Mismatch on Noise-Shaping

A quadrature ΔΣ ADC is a ΔΣ modulator which has a complex NTF and STF. A complex bandpass NTF can achieve better noise suppression than a real bandpass NTF because the zeros are not constrained to being realized in conjugate pairs [1]. It is possible to place all available NTF zeros in the band of interest, much like a low-pass modulator. A complex STF is also desirable because digitizing a complex input such as that from an image-reject mixer can reduce the filtering requirements of a radio receiver. However, in terms of complexity, a quadrature modulator is similar to its real counterpart in converting complex signals. For example a second order complex modulator would require four integrators; two second-order real modulators would also require four integrators (two integrators each).

The output of a real ΔΣ modulator is usually described in terms of its NTF and STF. Likewise, the output of an ideal quadrature ΔΣ modulator can also be described in terms of only its NTF and STF. However due to component mismatches in the loop filter, the loop transfer function will also have image terms. The effect of the image transfer functions will be to alias out-of-band signals and quantization noise at around the image frequency band into the desired band. In the presence of filter mismatches, the output of the modulator must be augmented by two additional transfer functions. The output of a mismatched complex modulator is written as

$$V(z) = G(z)U(z) + G_{img}(z)U^*(z) + H(z)E(z) + H_{img}(z)E^*(z) \quad (2.17)$$

The image noise transfer function (INTF), $H_{img}(z)$ relates the output with respect to the image of the quantization noise. The image signal transfer function (ISTF), $G_{img}(z)$ describes the output with respect to an image input. See Appendix A for derivation of the various transfer functions as a function of loop filter transfer functions. In the presence of quadrature filter imperfections, the

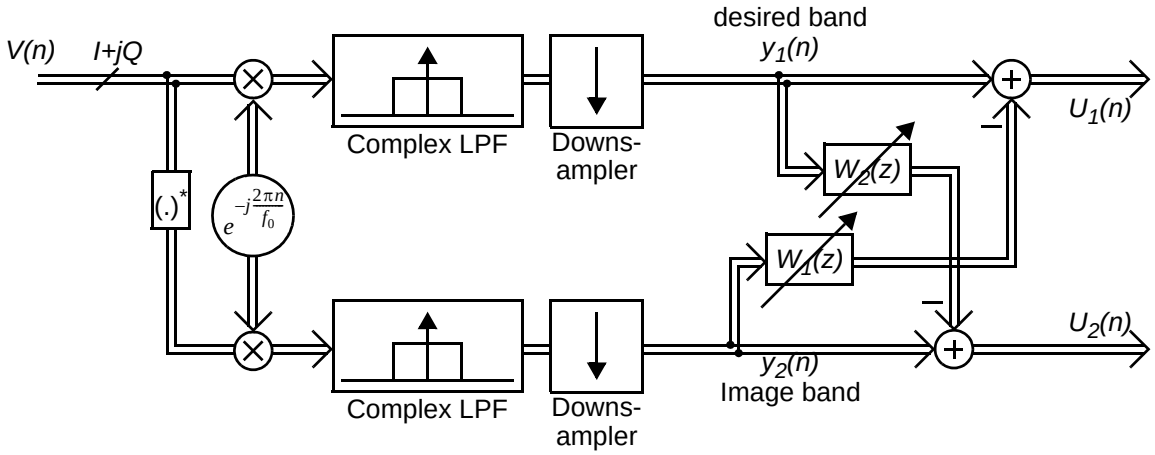

Fig. 2.6 Block diagram of the mismatch cancellation system.

in-band noise can be dominated by the INTF. One technique for reducing the effects of the INTF is to introduce a zero in the NTF's own image band [1]. Although this technique reduces the effect of INTF in the presence of I and Q path mismatch, it does not reduce the magnitude of the ISTF! Large interferes present at the image band will still alias in-band, decreasing the dynamic range of the modulator. The IRR of the modulator will be defined as the maximum of the ratio between $G(j\omega)$ and $G_{img}(s)$:

$$IRR = max\left(20\log\left\{\left|\frac{G(j\omega)}{G_{img}(j\omega)}\right|\right\}\right) \text{ for } 2\pi\left(f_0-\frac{f_B}{2}\right)<\omega<2\pi\left(f_0+\frac{f_B}{2}\right) \qquad (2.18)$$

2.6 Adaptive mismatch cancellation techniques

One method of reducing the degradation caused by I and Q path mismatch in a complex ADC or filter is to use an adaptive filter to subtract the aliased image signal [20]. A block diagram of such a system is shown in Fig. 2.6. In this scheme a decimation filter is used to obtain both the signal band and the image band. A complex least mean square (LMS) algorithm is then used to compensate for mismatch between the I and Q paths by using an adaptive filter to subtract the aliased image signal from the desired band. Using this type of approach, it is possible to improve the IRR performance of the modulator by digitally post processing the output data stream. Fig. 2.7a shows the output spectrum of a mismatched modulator. As a result of the mismatches, a fraction of the image signal has aliased in-band through the ADC's ISTF, thereby SNR of the modulator has been degraded. The output spectra before and after applying the adaptive mismatch cancellation system described in [20] is shown in Fig. 2.7b and Fig. 2.7c respectively. There is clearly at least 30dB

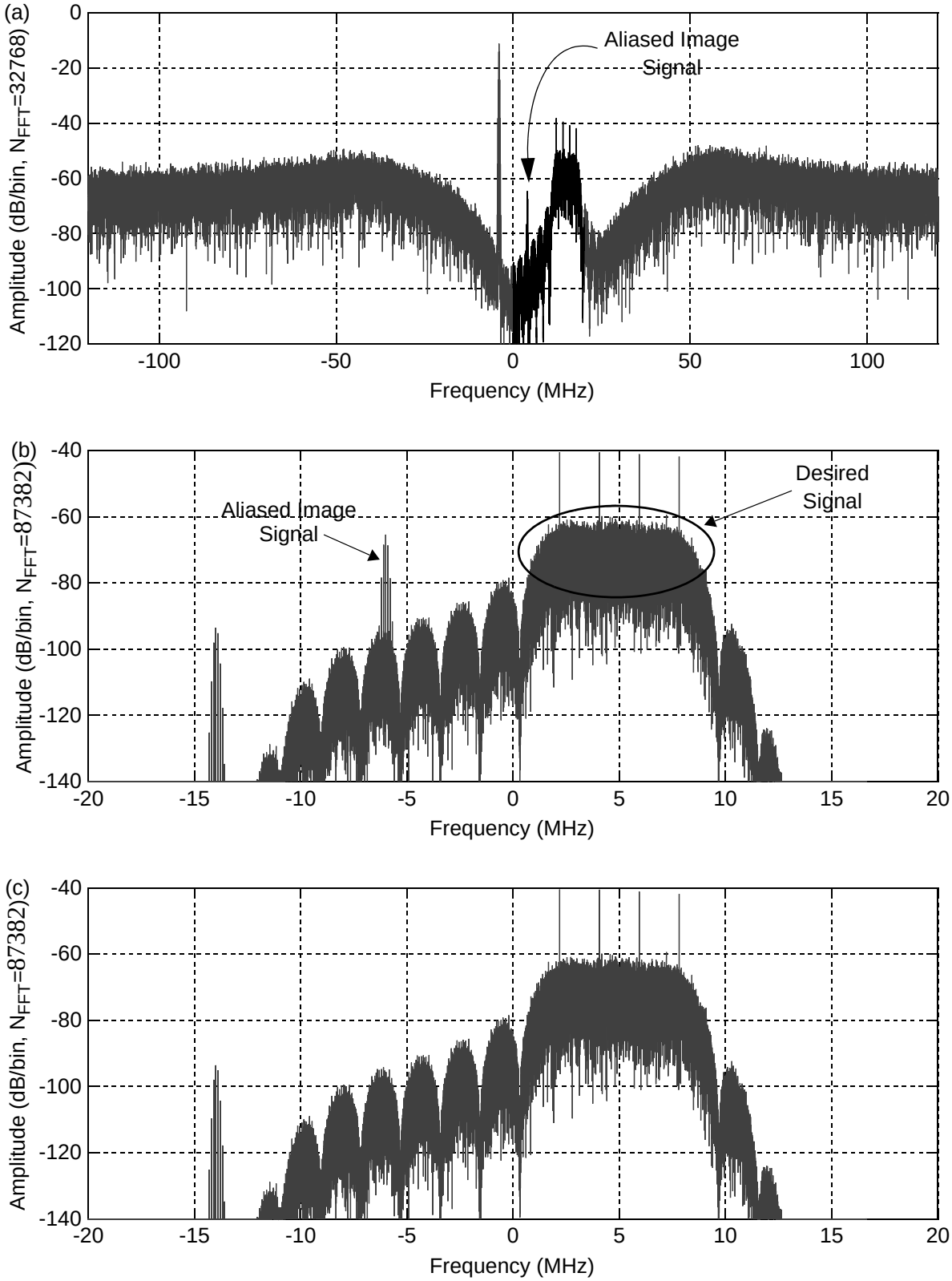

Fig. 2.7 (a) Undecimated output spectrum of the modulator, *V(n)*. (b) In-band signal after down-conversion and decimation $y_1(n)$. (c) In-band signal after downconversion, decimation and the adaptive filter $u_1(n)$.

improvement in IRR of the modulatory, which shows that it is possible to improve the IRR of ADC by digitally post processing the data stream.

2.7 Summary

Lowpass and bandpass ΔΣ modulators were discussed and shown to perform high resolution A/D conversion on narrowband signals using only a coarse quantizer. The key parameters in determining the performance of a ΔΣ ADC were shown to be its NTF and oversampling ratio. The advantages and disadvantages of using a continuous-time loop filter were briefly discussed.

Complex signals and filters were introduced. The performance of complex filters in the presence of filter mismatches was shown to result in an aliasing effect in which signals in the image-band fold into the band-of-interest, thus corrupting the output. Quadrature modulators were discussed and their performance in presence of filter mismatches was examined. It was shown that filter mismatches give rise to two additional image transfer functions that have no equivalents in real modulators. An adaptive LMS algorithm for improving the performance of the modulator in the presence of I and Q path mismatch was also discussed.

CHAPTER 3

NTF Design and Modulator Architecture

This chapter provides the motivation for the desired modulator specifications. The procedure for designing a complex NTF is described. The advantages and disadvantages of two different modulator topologies for implementing the same NTF are discussed. Ideal system level simulations of the modulator are presented and an appropriate architecture is chosen for further study. The dynamic range of the modulator is also scaled to a suitable level.

3.1 Desired Design Specifications

The goal of this thesis is to demonstrate a wide-band, low power continuous-time bandpass complex ΔΣ ADC suitable for a low-IF receiver architecture as shown in Fig. 3.1. In a low-IF receiver, it does not make much sense to digitize the image-band accurately since it will be rejected by the baseband digital filters. A bandpass complex ΔΣ ADC is ideally suited for this purpose. A lower power consumption can be achieved by taking advantage of this fact since a complex bandpass ΔΣ ADC only digitizes the in-band signal accurately, while the image-band is only coarsely digitized. A continuous-time modulator has a further advantage which is that it will have built-in anti-aliasing properties. This can simplify or even eliminate an anti-alias filter in the signal path. Furthermore, if the ADC has sufficient dynamic range, it is possible to remove the baseband variable gain amplifiers, further simplifying the receiver design. The target ADC specification are list-

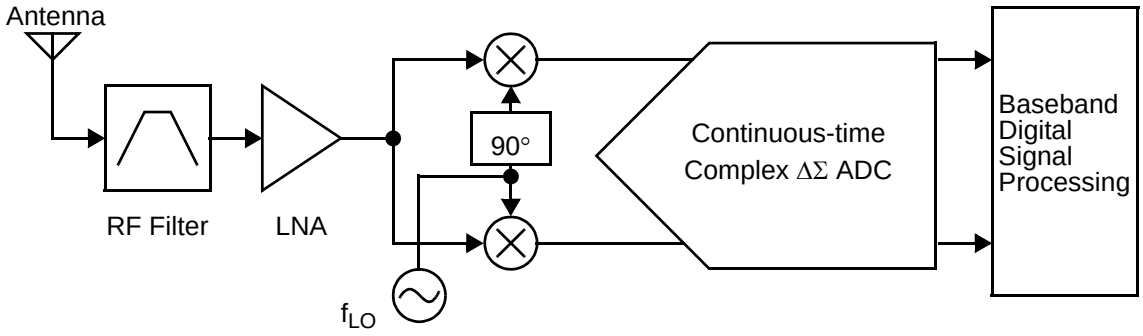

Fig. 3.1 Block diagram of a low-IF architecture.

ed in Table 3.1. The specifications listed in the table should make this ADC suitable for an 802.11g receiver [14]. The required bandwidth and oversampling ratio are dictated by the bandwidth of a single 802.11g channel, which is approximately 16.67MHz with a channel spacing of 20MHz. The center frequency of the modulator is chosen such that the edge of the pass-band is just at DC and therefore DC offset and 1/f noise from the preceding stages in the signal chain can be removed with a high pass filter. The order and number of quantization levels are chosen such that quantization noise of the modulator becomes negligible for the required dynamic range. The target power consumption of the ADC is found by scaling the power consumption of recently published state-of-the-art ΔΣ ADC [12], [13] such that a similar figure of merit (FOM) is achieved by the target modulator. A commonly used FOM is

$$FOM = \frac{POWER}{2^{ENOB} BW} \tag{3.1}$$

where ENOB is the effective number of bits and BW is the signal bandwidth achieved by the ADC. The following sections will elaborate on the design procedure.

3.2 NTF Selection

The three most important parameters in determining the performance of ΔΣ modulator are its OSR, NTF and the number of quantization levels used in the feedback DACs. The NTF determines

Parameter	Desired Specification
ΔΣ Topology	Complex Continuous-Time Feedforward Architecture
Sampling Frequency	>240MHz
Signal Bandwidth	>20MHz
Center Frequency	$f_s/24$
Oversampling Ratio	12
Number of Quantization Levels	17
Dynamic Range	>72dB
Image Rejection	>40dB
Maximum Input Voltage (diff.)	~600mV$_{rms}$
Power Consumption	<50mW

Table 3.1: Target ADC performance.

the in-band quantization noise attenuation, thus the maximum SNR that the modulator can achieve for a given value of *OSR*. The number of quantization levels determines the amount of the quantization noise that is to be suppressed in-band by the NTF. The following procedure was followed to design a prototype NTF.

A 4^{th} order lowpass NTF with optimally spread zeros and a maximum out-of-band gain of 2.8 ($\|H(z)\|_\infty = 2.8$) was designed using the $\Delta\Sigma$ toolbox [7] in Matlab. The poles and zeros of the modulator were then shifted to $\frac{\pi}{12}$ by multiplying them by $e^{j\frac{\pi}{12}}$. This method works because the target NTF has a symmetrical spectrum about the modulator's center frequency. Typically, a zero is also placed in the image band to suppress the quantization noise in the image-band from leaking in-band [1]. However, since the separation between the image-band and desired band is relatively small for this type of low f_0 bandpass ADC, it was not necessary to insert a zero into the NTF in the image-band. The pole-zero plot as well as the frequency response are shown in Fig. 3.2. The desired NTF is

$$\frac{(z-0.9851-j0.1719)(z-0.9391-j0.3437)(z-1)(z-0.8836-j0.4682)}{(z-0.6438+j0.3315)(z-0.3918-j0.6090)(z-0.4857+j0.0111)(z-0.4151-j0.2525)} \qquad (3.2)$$

Note that following the above procedure will result in an NTF zero that is very close to DC. For ease of implementation, the NTF's near DC zero was replaced with a zero at exactly DC. This resulted in only a minor degradation in SNR and a slightly asymmetrical NTF about the modulator's center frequency.

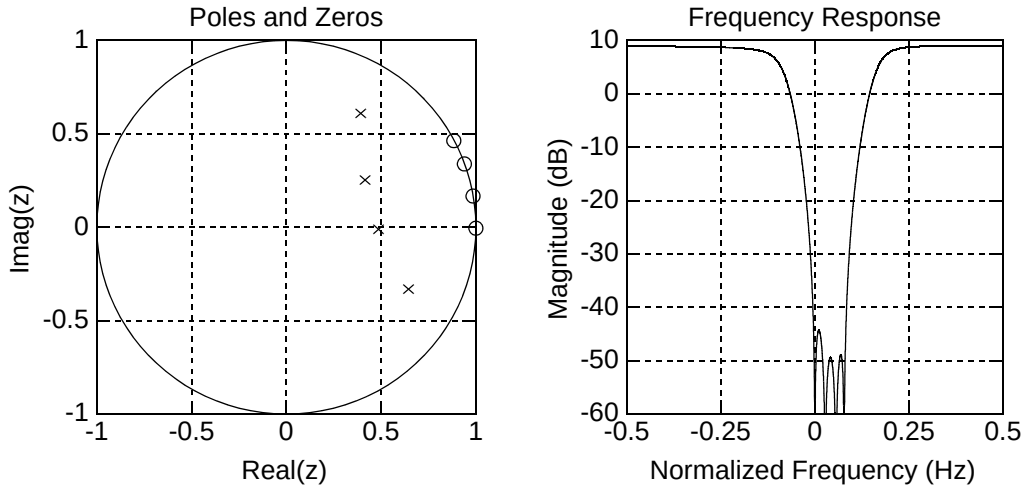

Fig. 3.2 Pole-zero and frequency response plot of the desired NTF.

3.3 Realizing Complex Poles

Fig. 3.3 shows a continuous-time complex resonator using two cross-coupled integrators. This filter will form the basic building block of the quadrature ΣΔ ADC. The transfer function of the ideal filter is

$$T(s) = \frac{k_r + jk_i}{s - j\omega_0} \tag{3.3}$$

Note that to realize a single pole requires 2 integrators. Thus to realize a 4^{th} order NTF requires 8 integrators or 8 opamps.

3.4 Modulator Topology

Once a suitable NTF has been chosen, it is necessary to map it to a specific topology. The two topologies that were considered in this thesis are the feedback and the feedforward topology as shown in Fig. 3.4 and Fig. 3.5. Note that the double lines represent complex signals, i.e. two real signals that are interpreted as $I+jQ$.

Each topology has its own unique set of advantages and disadvantages. The feedforward structure (shown in Fig. 3.5) drives the quantizer with a weighted sum of the output of the resonators. The obvious advantage of this structure is that only a single DAC is used to drive the resonators and so the full-scale of the modulator can be changed simply by adjusting the full-scale of a single DAC. The second advantage is that all the resonator stages except the first one contain almost no signal component [4]. This can ease the dynamic range requirement of the resonators compared

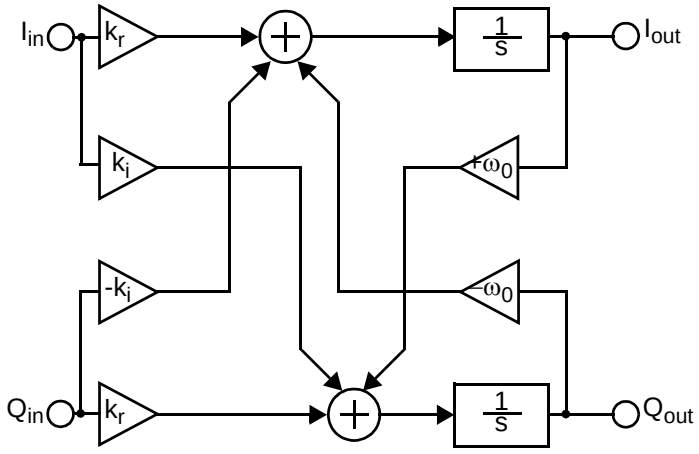

Fig. 3.3 Block diagram of a complex resonator using two cross coupled integrators.

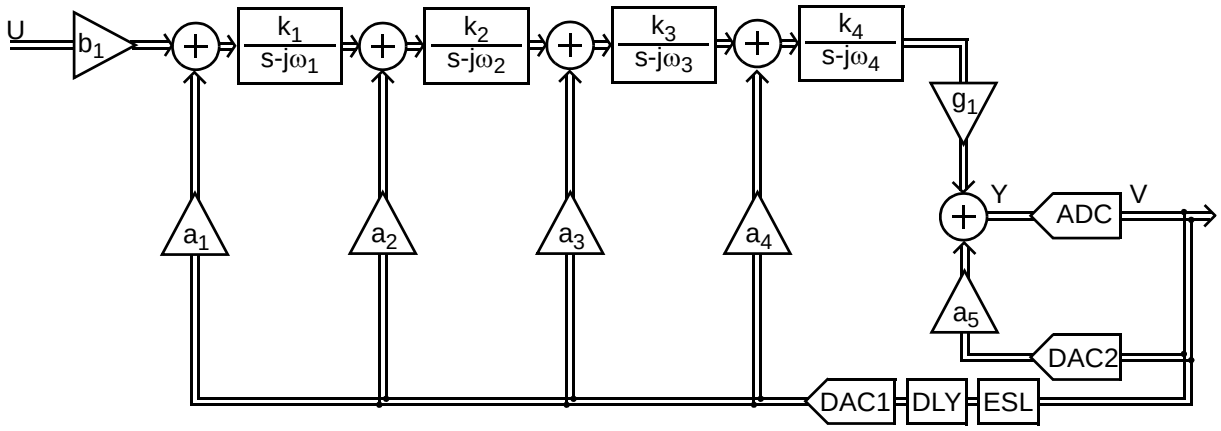

Fig. 3.4 General feedback structure for implementing any arbitrary 4th order modulator.

with the feedback structure and hence a lower power consumption can be achieved with this topology. Note that both [12] and [13] employ a feedforward loop filter structure to achieve very low power consumption. However, the disadvantage of this architecture is that the STF will have out-of-band peaking and will be slightly non-flat in-band [4]. Peaking in the STF is undesirable since it means that the modulator is more likely to be driven into instability by large out-of-band interferers. The second feedforward term, b_2 is used to reduce the out-of-band peaking of the STF. The STF has an out-of-band peaking of 13.2dB without and 6.6dB with the b_2 term.

The advantage of feedback structure (shown in Fig. 3.4) is that the STF will be flat in-band and will have low-pass characteristics out-of-band using only a single feed-in. The disadvantage is that the dynamic range of the resonators is increased as each resonator will contain some signal component at its output which needs to be cancelled by the next stage DAC. The increased dynamic

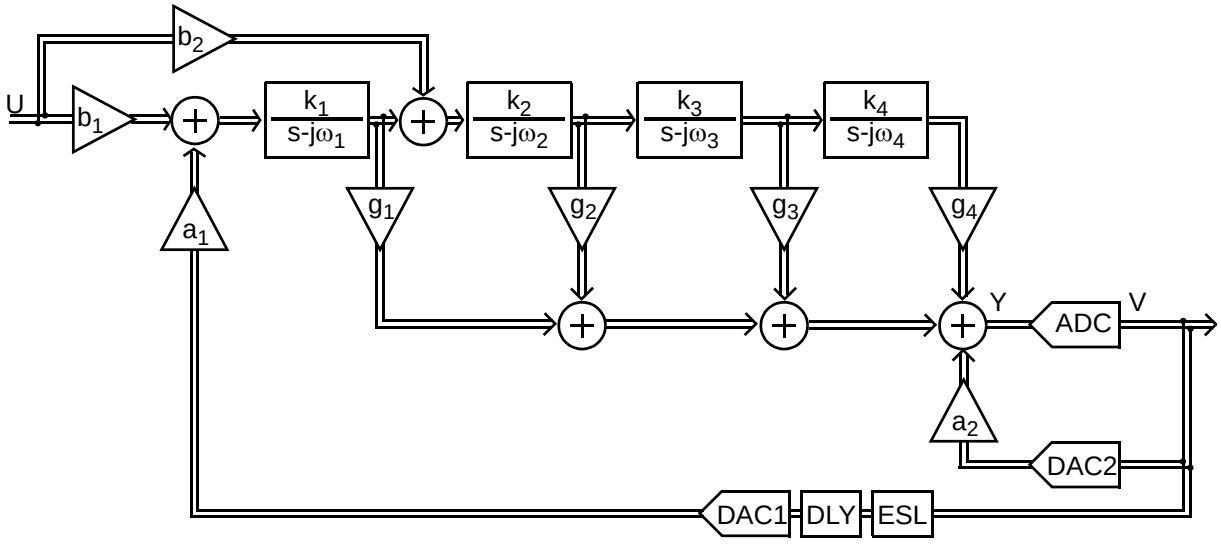

Fig. 3.5 General feedforward structure for implementing any arbitrary 4th order modulator.

range requirement of the first stage resonator is especially troublesome as it can dramatically increase the power consumption of the first stage resonators. There are also several feedback DACs which lead to an increased die size.

In both topologies, the NTF zeros determine the center frequency of the resonators. Both structures contain enough adjustable parameters to accommodate any arbitrary 4^{th} order NTF with a DAC delay of less than one clock period. Note that $a_1 \ldots a_5$, $b_1 ... b_2$ and $g_1 ... g_4$ are complex gains. Both structures use continuous-time complex resonators, and so the modulator will have inherent anti-aliasing properties. However the alias attenuation ability of the feedback architecture will be much greater. This is because in the feedback structure, the transfer function from the input U to the input of the quantizer (i.e L_0) is a 4^{th} order lowpass transfer function. However in the feedforward architecture, L_0 contains components that only have a first order characteristics (the path through $b_1 \rightarrow \frac{k_1}{s - j\omega_1} \rightarrow g_1$), therefore there is less attenuation of the signal at the input of the quantizer at an alias frequency of the modulator. This degrades the alias attenuation capability of the feedforward modulator.

An intentional $\frac{1}{2}$ clock period delay is introduced to allow for latency in the feedback path, including the flash, the feedback DACs and the element selection logic block (ESL) to shuffle the unit DAC elements. Due to the extra delay, it is necessary to add an extra degree of freedom to the system, hence the need for the feedback DAC2 [42]. Other methods of compensating for excess loop delay are described in [43].

3.5 Coefficient Selection

To fully specify the systems shown in Fig. 3.4 and Fig. 3.5 requires 14 parameters. The parameters $\omega_1 \ldots \omega_4$ determine the center frequency of the modulator and are fixed by the zeros of the NTF. The feedback coefficients $a_1 \ldots a_5$ determine the poles of the NTF in by the feedback topology. Coefficient $k_1 ... k_4$ and g_1 were added to allow arbitrary scaling of the integrator outputs. For the purposes of choosing the coefficients for a given NTF, they can all be set to unity. Similarly, the coefficients $g_1 ... g_4$ and a_2 determine the poles of the NTF in the feedforward architecture. The full-scale of the first DAC (i.e. a_1) and $k_1 ... k_4$ can arbitrarily be set to unity for initial coefficient calculations. In both topologies b_i determines the STF of the modulator and is chosen to give unity gain at around f_0.

The ordering of the zeros is important. In order to minimize the input-referred thermal noise of later stages, ω_1 should be chosen so that it is near center of the signal band. To choose the coefficients that will give the desired NTF, the sampled pulse response from the quantizer output to the quantizer input was "matched" with the impulse response of the prototype NTF (see Appendix B for details). This ensures that the equivalent discrete-time transfer function from the output of the quantizer to the input of the quantizer is equal to the desired transfer function that will result in the target NTF, i.e. the sampled loop filter pulse response is matched to the impulse response of $\frac{H-1}{H}$, where H is the desired NTF. Note that in the absence of any mismatch between the real and imaginary paths, it is only necessary to match the pulse response in one channel only. Due to the symmetry of the I and Q channels, the impulse response from the Q channel to the input of the quantizer will be exactly the same as the response from the I channel to the quantizer input multiplied by *j*.

3.6 Ideal Modulator Performance

The modulators were simulated in Simulink for various input amplitude to obtain the SNR vs. input amplitude plots that are shown in Fig. 3.6. The output spectra as well as the NTF and STF of the two topologies with a -2dBFS is shown in Fig. 3.7. Note that the two topologies implement exactly the same NTF, therefore the expected ideal SNR is the same. However the STF is different for each topology. Also note that the spectrum is not symmetric about DC. This is a characteristic of a complex system. In absence of non-idealities, both topologies achieve over 84dB SNR at an oversampling ratio of 12 with a 17 level quantizer.

3.7 Coefficient Scaling

Both modulator structures were simulated in Simulink for 2^{20} clock cycles with a single complex sinusoid tone at f_0 with an input amplitude of 0.85 to find the peak value of each state. A 10% margin of safety was added to the simulated peak values. The states were then scaled such that the output of the first integrator does not exceed ±1.1. Subsequent stages were scaled for a maximum swing of ±0.6. Table 3.2 and Table 3.3 show the scaled and un-scaled coefficient values for the feedback and feedforward topologies respectively.

Note that a much larger gain can be used in the first stage resonator of a feedforward modulator

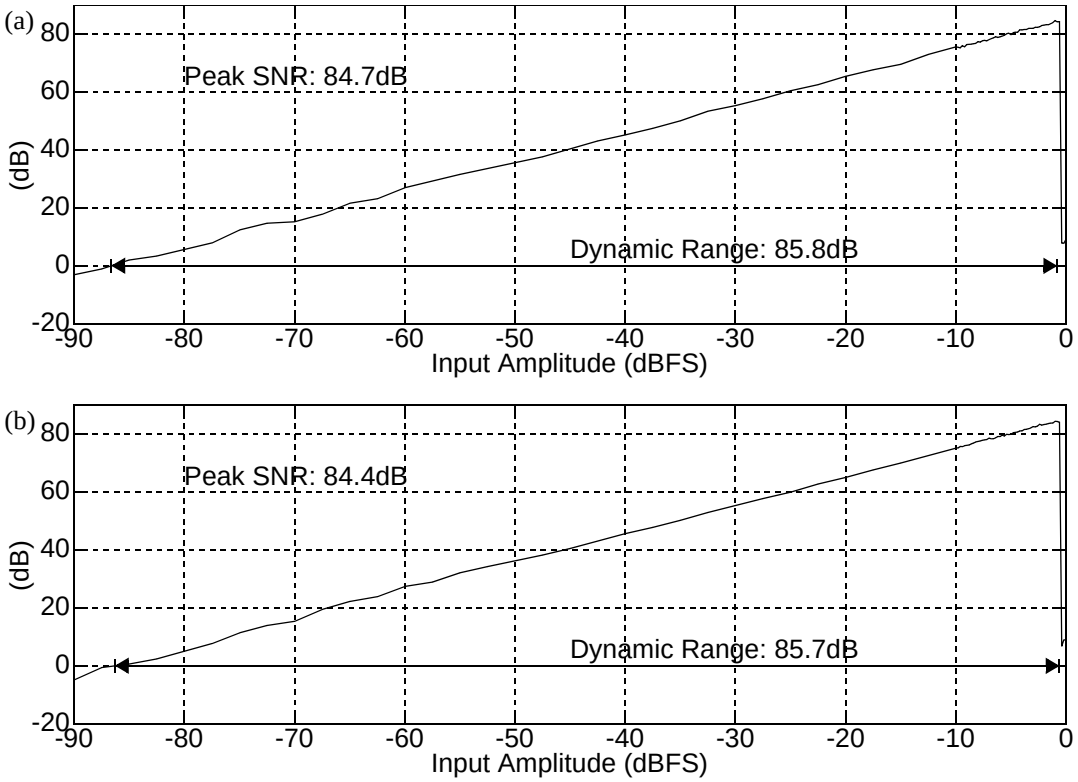

Fig. 3.6 In-band SNR vs. input level for (a) feedback structure (b) feedforward structure.

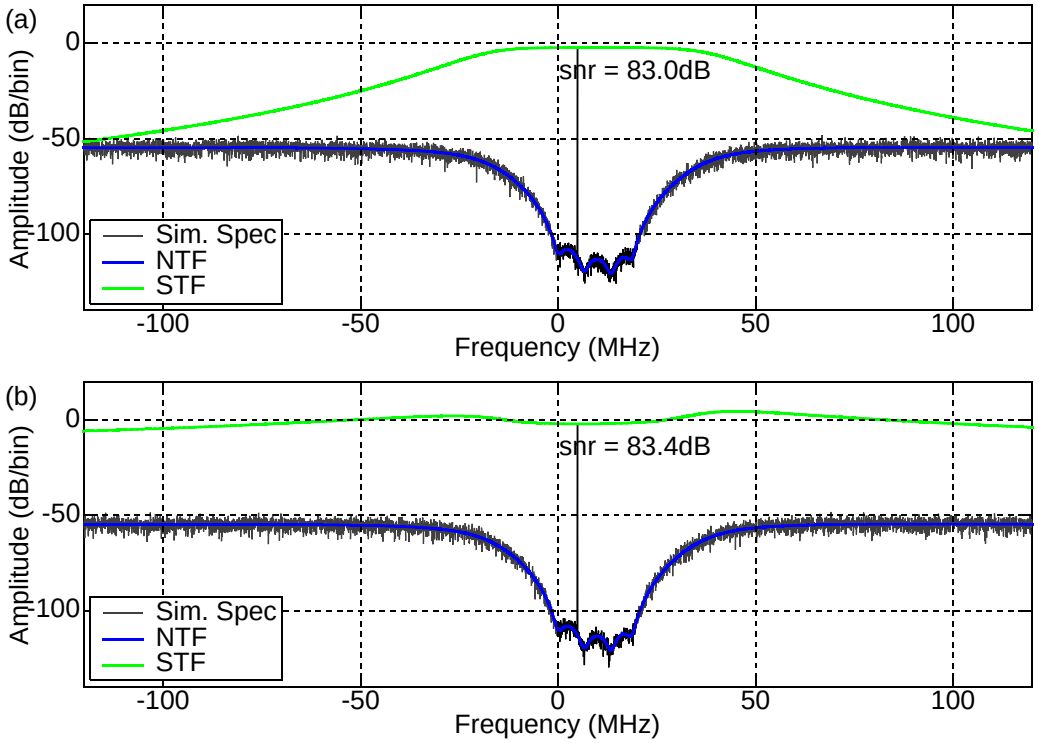

Fig. 3.7 4 Averaged output Spectra, N_{FFT} = 8192 (a) feedback structure (b) feedforward struc-

Coefficient	Un-Scaled Value	Scaled Value
b_1	0.1554	0.2586
a_1	-0.1377+j0.0135	-0.2290+j0.0225
a_2	-0.6060-j0.2005	-1.0080-j0.3336
a_3	-1.4630+j0.1084	-0.5488+j0.0406
a_4	-2.0607-j0.5759	-0.5174-j0.1446
a_5	-1.1262-j0.2213	-1.1262-j0.2213
g_1	1.0000	1.0000
k_1	1.0000	0.2255
k_2	1.0000	0.6694
k_3	1.0000	0.9745
k_4	1.0000	4.0870

Table 3.2: Un-scaled and scaled coefficient values for the feedback structure.

than can be used in a feedback modulator (b_{1ff}=0.8846 vs. b_{1fb}=0.2586). The effect of this is that a) thermal noise of subsequent stages becomes much more negligible and b) a smaller capacitor can be used for same given thermal noise level. The effect of this is that the resonators can use smaller integrating capacitors for a given input-referred noise requirements which reduces the

Coefficient	Un-Scaled Value	Scaled Value
b_1	1.0234	0.8846
b_2	-1.0234	-0.8846
a_1	1.0000	0.8644
a_2	-1.1262-j0.2213	-1.1262-j0.2213
g_1	-2.0607-j0.5759	-2.3840-j0.6663
g_2	-1.2819-j0.5396	-0.7878-j0.3316
g_3	-0.5137-j0.1226	-0.4605-j0.1099
g_4	-0.0239-j0.1386	-0.0797-j0.4629
k_1	1.0000	1.0000
k_2	1.0000	1.8826
k_3	1.0000	0.6855
k_4	1.0000	0.2685

Table 3.3: Un-scaled and scaled coefficient values for the feedforward structure.

power consumption of the first stage resonator. For these reasons, only the feedforward modulator was chosen for further investigation. The reason for this is that in a feedforward architecture, the resonators do not process much of the signal, therefore dynamic range requirements of the resonators can be reduced. For an intuitive understanding of this phenomenon, consider the following: there are no feedback DACs to cancel signal components at the input of any of the resonators except for the first one. Hence, the input and outputs of the resonators cannot have a large signal component present since that would saturate the next stage. Therefore the input of the resonators contains mostly quantization noise and so the dynamic range of the resonators should be small.

3.8 Summary

The desired modulator specifications were presented in this chapter. The procedure for designing a complex NTF was described. The desired NTF was mapped onto two different topologies. The advantages of each topology was discussed. The feedforward architecture was chosen for further study because of it can lead to lower power consumption. The modulator was also scaled for maximum integrator output level of ±1.1 in the first stage and a ±0.6 in subsequent stages.

CHAPTER 4

Effects of Non-Idealities on Modulator Performance

This chapter discusses the performance of the modulator in the presence of non-idealities. Minimum required opamp specifications are also found. The modulator performance in terms of both SNR and IRR is discussed in presence of component mismatch. The required matching tolerance are found using sensitivity analysis and Monte Carlo simulations. The modulator is also simulated in presence of clock jitter and timing errors. Errors due to DAC element mismatch are discussed and matching requirements are also found.

4.1 Effect of Non-Ideal Opamp

The effect of finite opamp gain and bandwidth is to move the NTF zeros inside the unit circle. This reduces the noise attenuation capability of the NTF and thus reduces the maximum SNR that the modulator can achieve. To study the effect of finite opamp gain and bandwidth on modulator performance, first the modulator was simulated in Simulink assuming that the opamp used in the integrator is ideal except for finite gain, i.e. the ideal integrator transfer function was changed from $\frac{1}{s}$ to $\frac{1}{s + 1/A}$, where A is the gain of the opamp. A plot of SNR vs. opamp gain is shown in Fig. 4.1. Based on these simulations, an opamp with a gain of 35dB is sufficient to ensure that SNR degradation due to finite opamp gain is negligible.

To study the effect of finite opamp bandwidth, the modulator was simulated with a simple 1-pole opamp model in the integrator. To reduce the required opamp bandwidth requirements, the impulse response from the quantizer output to the quantizer input was matched to that of the ideal NTF taking into account the non-idealities of the loop filter, such as finite gain and bandwidth of

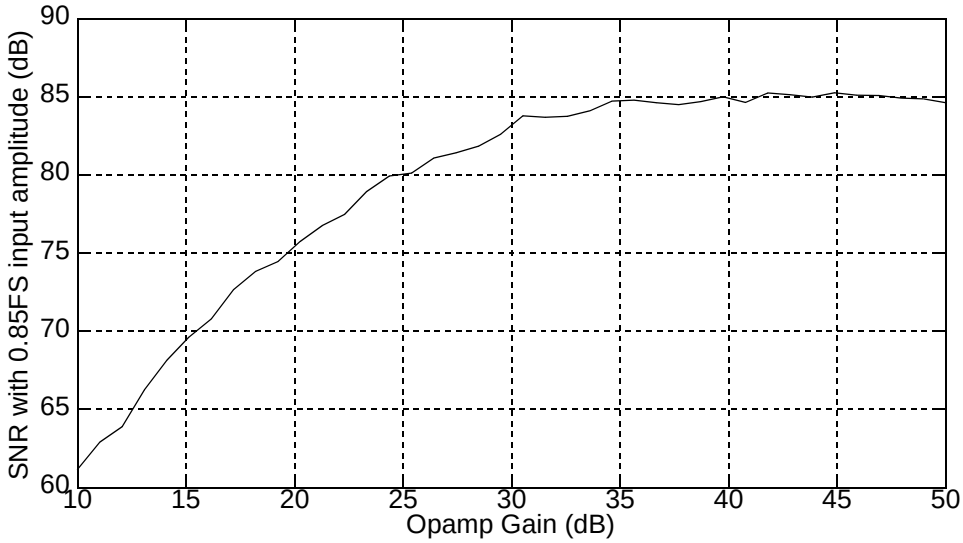

Fig. 4.1 SNR vs. finite opamp gain.

the opamp. The procedure is similar to the method described in chapter 3 where the feedforward coefficients are calculated using ideal integrators (See Appendix B).

A plot showing SNR vs. opamp unity gain frequency (relative to f_s) is shown in Fig. 4.2. Based on these simulations, using an opamp with a gain of 40dB and unity gain frequency of around $2.5f_s$ or 600MHz is sufficient to achieve over 82dB SNR.

For comparison's sake, to achieve the same SNR, without adjusting the filter coefficients to take into account finite gain and bandwidth of the opamp, requires an opamp with unity gain frequency of greater than 2.4GHz. A plot showing SNR vs. opamp bandwidth for the non-adjusted loop filter coefficients is also shown in Fig. 4.2.

The opamp slew rate requirements are found by simulating the modulator with a rate limiting block at the output of each opamp and a single complex tone at f_0 as the input stimulus. The opamp gain and unity gain frequency were set to 40dB and 600MHz respectively. The opamp slew rate requirements for each stage, in order to achieve at least 82dB SNR is summarized in Table 4.1. To verify that the ADC is able to achieve over 80dB SNR in the presence of process variations, the modulator was also simulated with the opamp unity gain frequency varied by ±20% about 750MHz.

Resonator Stage	Minimum Slew Rate (v/μs)
1	160
2	160
3	200
4	160
Feedforward Opamp	320

Table 4.1: Required opamp slew rate to achieve over 82dB SNR.

4.2 Coefficient Errors

The following sections study the effect of coefficient errors on modulator performance. In order to avoid time-consuming simulations of the non-linear model, predictions are made based on the linearized model of the modulator. The ideal nominal rms in-band gain of the NTF is about -60dB. The quantization noise power generated by each quantizer is $-\{6.02n + 1.76 - 3\}$ and the total noise power generated by the pair of quantizers is $-\{6.02n + 1.76\}$ thus the modulator can achieve SNR of approximately 84dB with a -2.0dBFS input and a 17 level quantizer

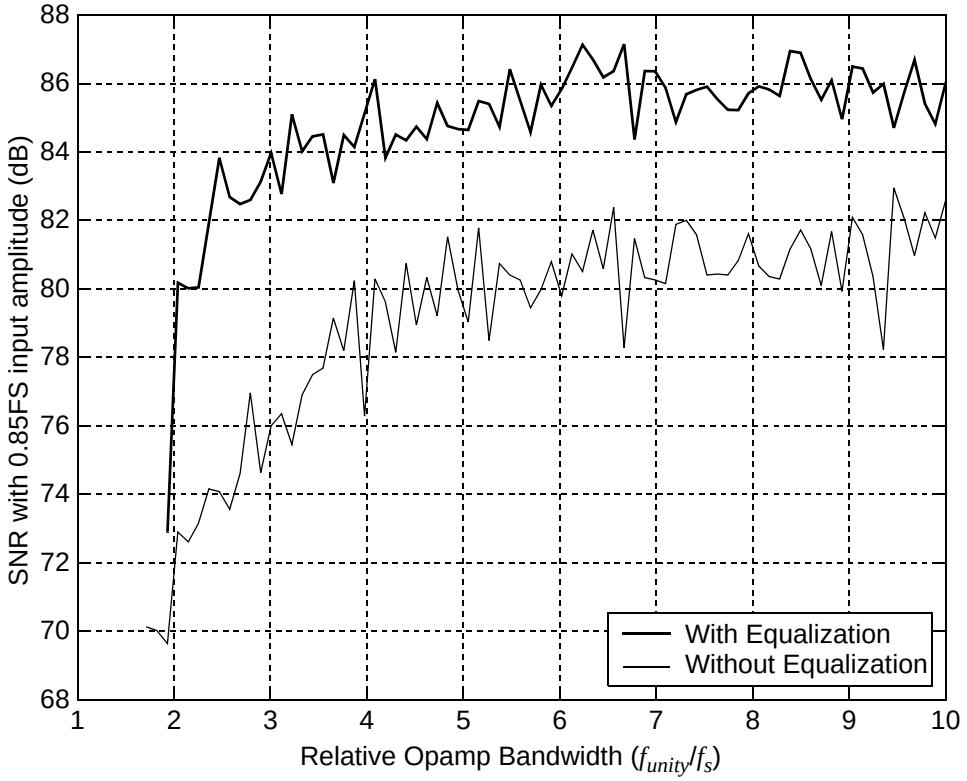

Fig. 4.2 SNR vs. Opamp bandwidth with/without impulse matching.

$(-2\text{dBFS} - ([-\{6.02\log 2(17) + 1.76\}] \approx 84\text{dB}))$. In order for SNR degradation caused by component tolerances to be negligible, the combined rms in-band gain of the NTF and INTF of the perturbed modulator should be less that -54dB (or about 78dB SNR at -2.0dBFS input level). To determine, the amount of SNR degradation caused by variations in each parameter, the in-band gain of the NTF was calculated for small changes in each parameter. The results of these sensitivity calculations are shown in Appendix D. Note that these plots only show the in-band NTF gain with respect to change in a single parameter. These plots are useful in determining which parameters will dominate the SNR degradation due to parameter shifts/mismatch. However, the cumulative effect of several simultaneous parameter shifts can not accurately be predicted from these plots. The effects of multiple parameter shifts were studied using Monte Carlo simulations.

4.2.1 Effect of Symmetric Coefficient Errors on SNR

Shifts in parameter values cause two kinds of error in a complex system. The first type of error causes a change in the complex transfer function and occurs as a result of symmetrical shifts in the real and imaginary paths (i.e. the coefficients are perturbed about their nominal values but the real and imaginary paths remain identical). The effect of symmetrical error is to cause the poles and zeros of the NTF to change. Movement of the NTF poles should not cause much SNR degradation as poles only determine the out-of-band gain and location of the transition bands of the NTF. Similarly, change in the location of the NTF zeros does not result in large SNR degradation since the center frequency of this particular modulator is relatively low ($f_s/24$) compared to the sampling rate, thus accurate tuning of the resonant frequency is not necessary.

According to calculations based on the linear model of the modulator, 5% drift in the NTF zeros relative to their nominal frequency, will result in less than 1dB increase in NTF gain (see Fig. C.3). Thus, tuning the resonant frequency of there resonators to within 5% of its nominal value will result in negligible degradation in ADC performance. Since absolute capacitor and resistor values can vary by as much as 20% independently, frequency tuning will be necessary to cope with process variations. For example, a resonator circuit with 600fF integrator capacitor requires tuning capacitors with a maximum capacitor step size of 60fF. Similarly, 5% symmetrical variation in other parameters such as inter-stage gain, full-scale value of DAC1 and feedforward coefficients (k_i, a_1 and g_i) results in negligible degradation in ADC performance (see Fig. C.1 and Fig. C.2).

In conclusion, symmetric variations in coefficient values do not degrade SNR by much, as long as what changes the I path affects the Q path equally. This is expected since symmetrical errors do not give rise to an image transfer function and so coefficient errors result only in slight perturbation of the poles and zeros of the modulator, which do not greatly degrade system performance.

4.2.2 Effect of Quadrature Coefficient Error on SNR

The second kind of error is much more serious and is the result of mismatches in the I and Q paths. This type of error will be referred to as quadrature error. As discussed in chapter 2, mismatch between the real and imaginary channels of the loop filter will result in a non-zero INTF and ISTF. The INTF will alias quantization noise at the image frequency, in-band. The effect of quadrature coefficient error on modulator performance is also studied with sensitivity calculations (See Appendix C). The in-band noise of the NTF and INTF is calculated with respect to changes in parameters of the real channel only. Fig. 4.3 shows the output spectrum of a modulator with 1% mismatch in all its coefficient values. The cumulative in-band quantization noise is partly due to the NTF and partly due to INTF.

Based on sensitivity analysis, mismatches in the a_i and k_i coefficients can be considered to be negligible, (less than 6dB increase in the in-band NTF gain), if the mismatch in the real and imaginary channel is less than 1% (see Fig. C.4 and Fig. C.5). Similarly, Fig. C.6 shows that 1% mismatch in cross coupling term ω_i causes negligible degradation in SNR performance. From these plots it is obvious that the critical parameters are those that are associated with the first and second resonators (a_1, k_2, ω_1 and ω_2).

4.2.3 Effect of Quadrature Coefficient Error on IRR

IRR was defined as the ratio of maximum ISTF gain in the band of interest over the STF gain at ω_0. Fig. C.7, Fig. C.8 and Fig. C.9 show the sensitivity of the modulator to each coefficient parameter. Most of IRR degradation is caused by mismatches in the first and second stage resonators. According to the sensitivity plots, in order to achieve 40dB IRR, b_1, b_2 and a_1 of the real channel must be at least within 1% of the imaginary channel.

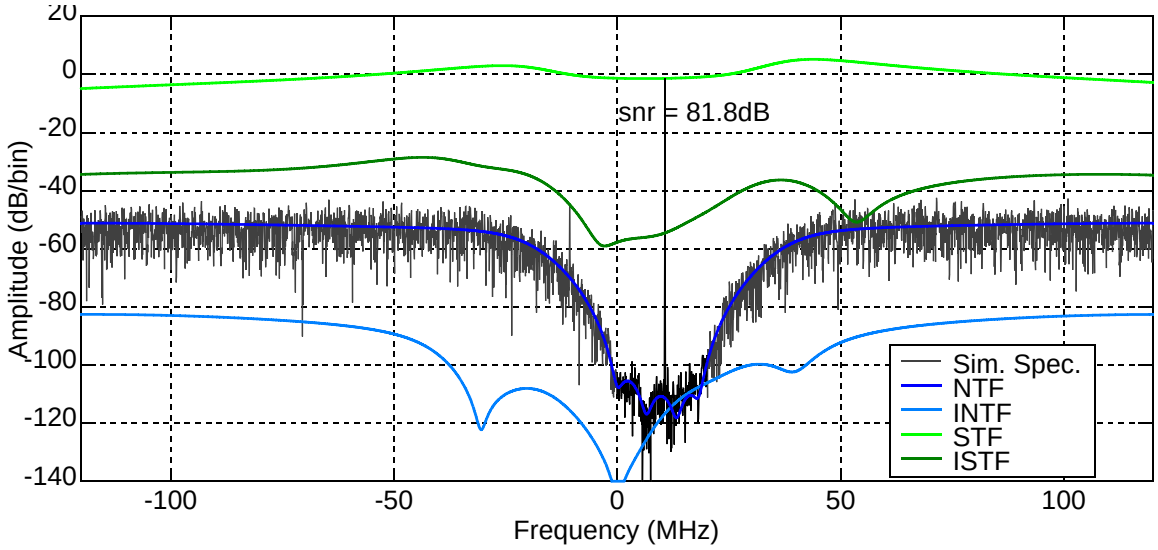

Fig. 4.3 Output spectrum of the modulator with 1.0% quadrature mismatch in coefficient values.

4.2.4 Random Coefficient Errors

The effect of multiple coefficient errors on ADC performance was studied by Monte Carlo simulations of the linear model. Assuming that modulator coefficients will be tuned to within 5% of their nominal value, all modulator coefficients were subject to a globally random 5%-peak shift.

All coefficients were also subject to random symmetric coefficient variation with a standard deviation of 1%. Furthermore, a_1, $b_{1\text{-}2}$, ω_1, and $k_{1\text{-}2}$ coefficients were given a random 0.5%-Gaussian distribution. All other coefficients were subject to a 1%-Gaussian distribution. The result of the Monte Carlo simulations of 10000 perturbed modulator are shown in Fig. 4.4. According to the simulation, 95% of the modulators achieve an in-band NTF gain of less than -56dB or greater than 80dB SNR with -2dBFS input. Furthermore, 95% of the perturbed modulators also achieve greater than 40dB of IRR. To verify the results based on the linear model, Monte Carlo simulations were also ran on the the non-linear model of the modulator. The resulting histograms are shown in Fig. 4.5. Simulations of the non-linear model verify that the predictions made with the non-linear model are accurate.

4.3 DAC Element Mismatch

A major disadvantage of a multi-bit ΔΣ modulator is that any errors in the feedback DAC will translate directly into errors for the overall converter [4]. To illustrate this consider the modulator

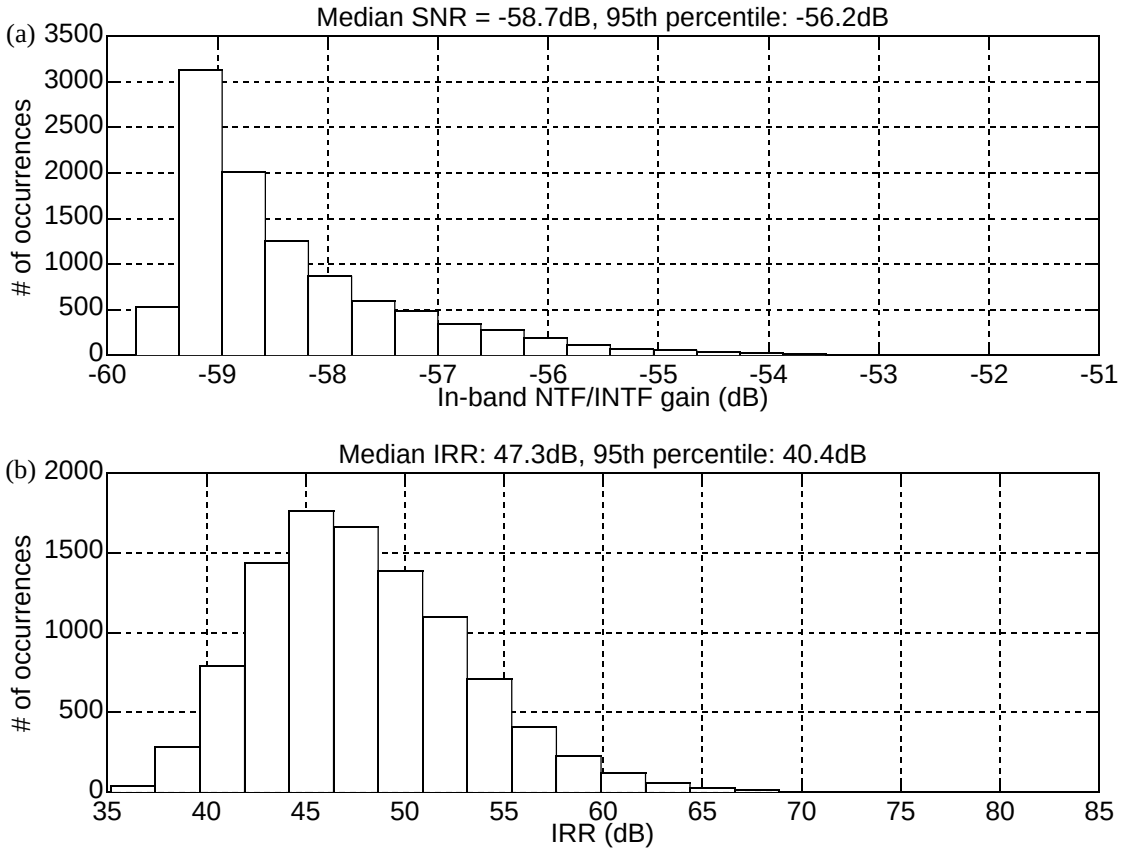

Fig. 4.4 (a) In-band NTF/INTF gain and (b) IRR histogram of 10000 perturbed modulators.

shown in Fig. 4.6. Assuming the error introduced by element mismatches in the feedback DAC can be modeled as additive white noise, the linear model of a multi-bit ΔΣ modulator is

$$V = GU + HE + (H-1)E_{DAC} \qquad (4.1)$$

where $(H-1)E_{DAC} \approx -E_{DAC}$ in the band-of-interest. Thus, in-band noise will be dominated by the DAC noise if nothing is done. An effective way to reduce the effects of E_{DAC} is through the use of mismatch shaping [4], [10]. First order mismatch shaping is equivalent to element rotation or DWA. In this scheme DAC elements are chosen in a circular fashion, and therefore the average of the DAC mismatch errors will be zero. Noise generated by the DAC is filtered by $1 - z^{-1}$ mismatch

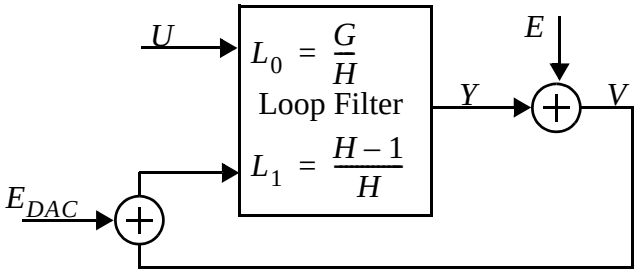

Fig. 4.6 A general block diagram of a ΔΣ modulator with DAC.

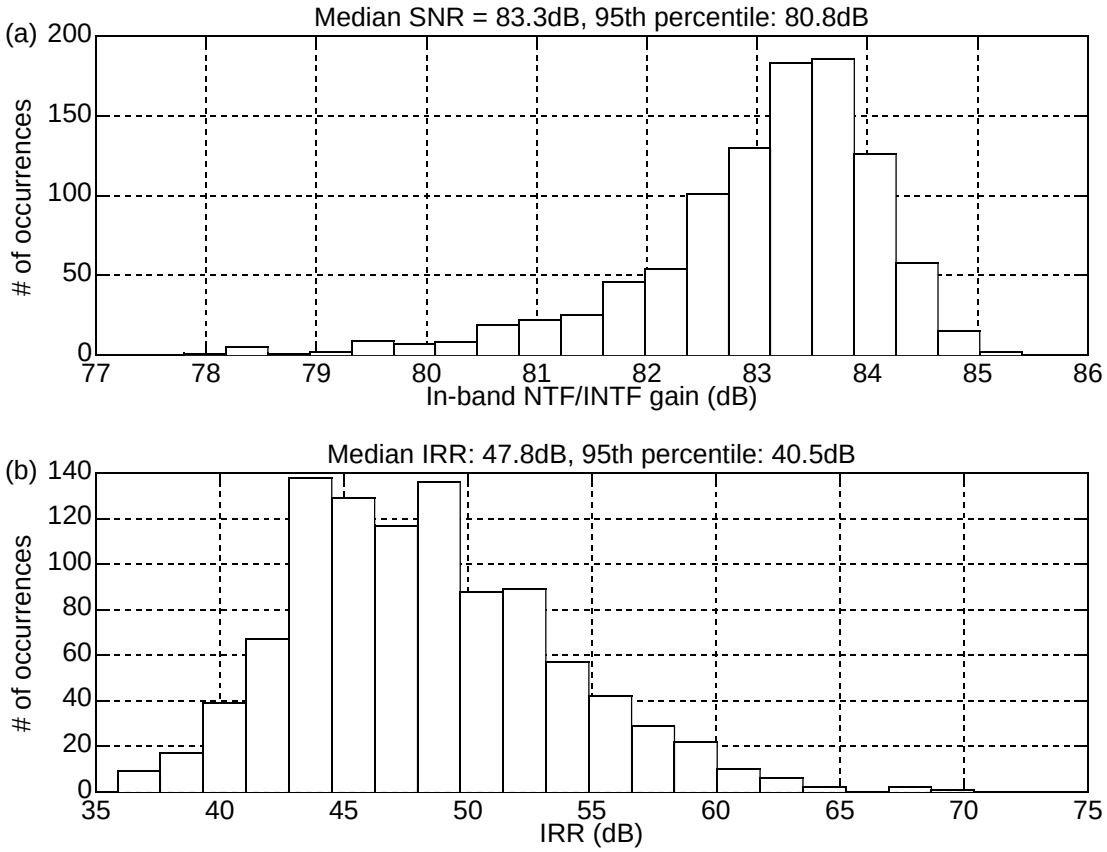

Fig. 4.5 (a) In-band SNR and (b) IRR histogram of 1000 perturbed modulators.

transfer function (MTF). Although algorithms do exist that provide second order noise shaping (e.g. [22] and [23]), (i.e. E_{DAC} is reduced by $(1-z^{-1})^2$ MTF), they are too slow to be useful in high speed applications. The maximum time that can be allocated to the DAC shuffler is less than a clock period. Thus the algorithm must be fast and simple. Any algorithm that requires complex logic cannot be used as it may require more than one clock period. Second order noise shaping algorithms, tend to be too slow as they require a great deal of combinatorial logic. Furthermore, the advantage of second-order noise shaping is greatly reduced at low oversampling ratios, which is the case for this particular ADC.

Among the first order noise shaping algorithms, DWA provides the most aggressive attenuation of the DAC mismatch errors, but is likely to suffer from tonal behavior. The DWA algorithm produces tones when its input signal is periodic. However, for higher order $\Delta\Sigma$ modulators, the correlation between the quantization noise and the input signal is much less, thus DWA will produce less tones [15]. For the above mentioned reasons, DWA was chosen as the algorithm for shuffling the DAC elements.

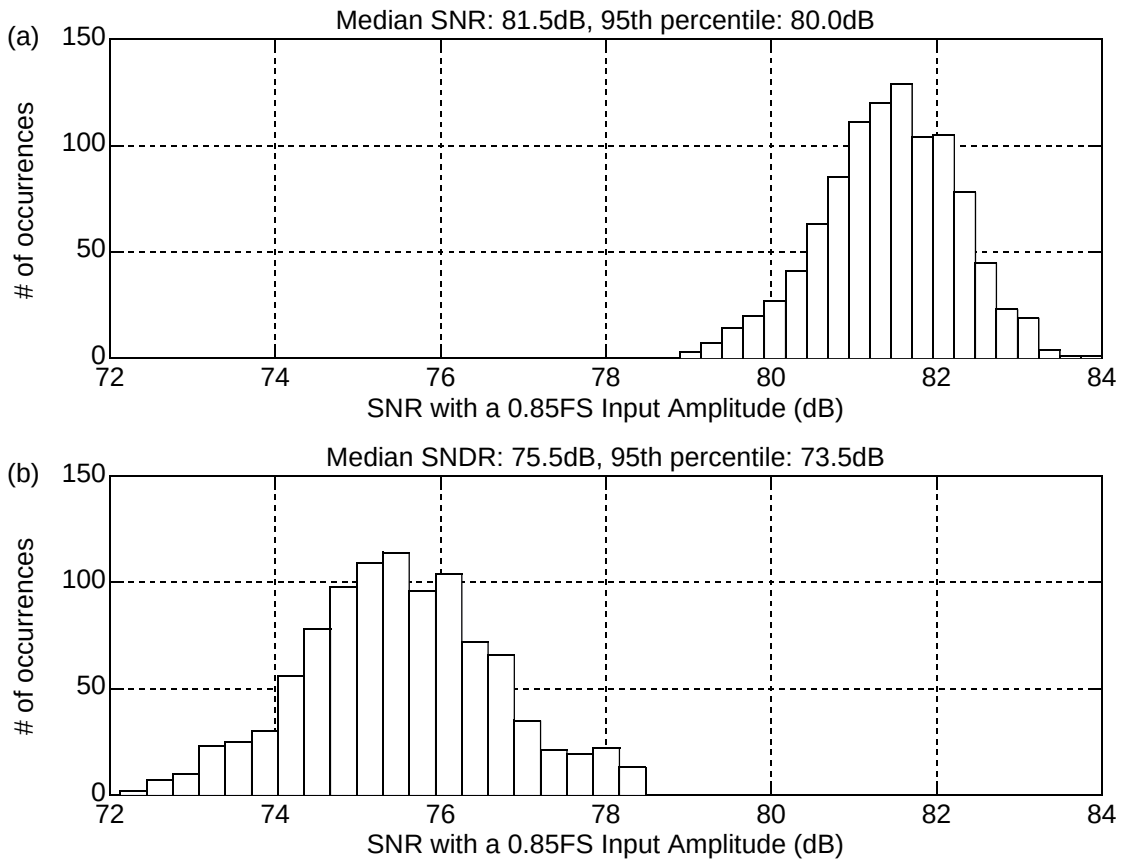

Fig. 4.7 Histogram of 1000 modulators with 0.5% mismatch in DAC1 and 1% mismatch in DAC2 with (a) DWA turned on and (b) DWA turned off.

To achieve greater than 80dB SNDR, the element sizes in the first DAC should be matched to within 0.5% of each other with the DWA turned on. However, with the DWA turned off the performance degrades to about 73.5dB peak SNDR (see Fig. 4.7). The effect of the second DAC on system performance is negligible, since it is connected to the input of the 17-level quantizer. The elements sizes in the second DAC were given a 1% Gaussian random distribution, in the above simulation.

4.4 Static Timing Errors

The modulator was simulated in Simulink with the DAC delay varying by ±5% of the clock period. This did not result in much SNR degradation (less than 1dB, with a 0.85FS input) although the out-of-band gain of the NTF did change due to the timing changes. The out-of-band gain of the NTF changed from 2.8 to 3.9. Large out-of-band NTF gain is not an issue, since a multi-bit modulator is able to tolerate large out-of-band NTF gain.

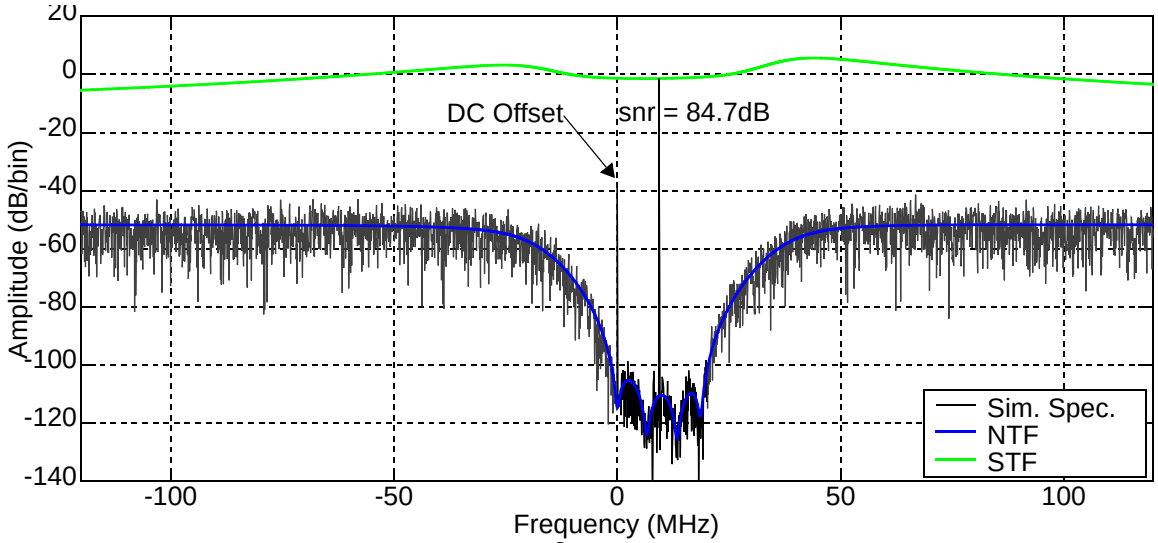

Fig. 4.8 Spectrum of the modulator with 10^{-2} integrator offset and an input level of -6.0dBFS (N_{FFT} = 4096).

4.5 Timing Jitter

A major disadvantage of a continuous-time modulator is that it is sensitive to the DAC output over the entire feedback period, unlike a discrete-time implementation which relies only on the final settled output value. DAC timing jitter corrupts the output of the feedback pulse and is often the main error source in high resolution continuous-time delta-sigma modulator [4], [9]. The output of the first feedback DAC is especially critical since any noise introduced there will not be shaped by the loop filter. To quantify the effects of clock jitter, the modulator was simulated with a normally distributed jittered clock signal. According to Simulink simulations, in order to achieve over 78dB peak SNR, clock jitter must be less than 0.09% of the clock period. At 240MHz sampling rate this corresponds to about 3.8ps of of random jitter on the clock signal.

4.6 DC Offset

DC offset in the feedback DACs and integrators and the quantizer is not expected to be a big problem since DC and low frequency content will be ignored in a low-IF type receiver. To verify that DC offsets do not cause instability, the scaled modulator was simulated in Simulink with a small DC offset at the input of each integrator (10mV). No degradation in performance was ob-

served with the addition of the small offset. The spectrum of the modulator with the specified integrator offset is shown in Fig. 4.8.

Source of Error	Main Assumption	Expected SNDR
Coefficient shift/mismatch	0.5% mismatch in the first 2 resonator coefficients and 1% elsewhere	80dB
Clock jitter	3.8ps rms and completely uncorrelated with the input signal	78dB
Unit DAC element mismatch	0.5% purely random mismatch between individual DAC elements (i.e no gradient present)	80dB
Thermal Noise	---	78dB
Total	All above sources of SNR degradation add in rms sense	73dB

Table 4.2: A summary of several sources of SNR degradation.

4.7 Summary

According to calculations based on the linear model of the modulator, an opamp with a gain of 40dB and a minimum unity gain frequency of 600MHz is sufficient to achieve the desired ADC performance target. Based on sensitivity analysis and Monte Carlo simulations, up to 5% symmetrical shifts in coefficients and 0.5% mismatch in the real and imaginary channels can cause little degradation in SNR. The matching tolerances can be relaxed to 1% matching after the second stage resonator. A feedback DAC clock with less than 3.8ps of random jitter and a duty cycle of 45-50% is enough to ensure a stable operation with negligible degradation in performance. DC offset was also shown to be a completely insignificant in determining the performance of the modulator. Table 4.2 summarizes the expected SNR with each source of non-ideality present and the cumulative effect of all the noise sources.

CHAPTER 5

Integrated Circuit Implementation

This chapter describes the design procedure to realize a 0.18μm CMOS implementation of the quadrature modulator described in the previous chapters using a 1.8V supply. The key blocks are described in detail followed by layout considerations. Spice level simulations results of all the key blocks as well as the complete modulator are presented and discussed.

5.1 Block diagram of the ADC

A complete block diagram of the ADC is shown in Fig. 3.5. The modulator consists of several key blocks: A loop filter, a quantizer, a DAC shuffler and feedback DACs. The loop filter is made up of four complex resonators and four feedforward adders. The resonators are realized using poly resistors, metal-insulator-metal (MIM) capacitors and opamps. The feedforward coefficients are realized using resistors and opamps. The quantizer is made up of two 4-bit flash ADCs which consists of a reference voltage generator using resistor ladders, preamplifiers, dynamic comparators and latches. The element selection logic (ESL) consists of combinatorial logic, digital adders and several flip-flops. The feedback DACs are implemented as switched current sources. The following sections discuss design considerations and details of each block.

5.2 ADC Loop Filter

5.2.1 Overview

A circuit level diagram of the loop filter is shown in Fig. 5.1. The resonator stages are implemented as active-RC filters. This was done so that the voltage swing of both the inputs and outputs of the first stage complex resonator could be maximized. For a fixed SNR, a higher input swing allows for a higher thermal noise level at the input. A higher swing at the output of the resonators also allows for the use of higher gain in the integrators (i.e. higher value of b_1). This leads to small-

er integrating capacitor size which lowers the power consumption of the first stage. Another major advantage of an active-RC implementation is that due to the feedback of the opamps, the resonators will be highly linear, compared to G_m-C filters which employ open loop transconductors.

5.2.2 Resonator Design

The resonators consist of four active-RC biquad filters, where the input and output are interpreted as complex quantities. The complex transfer function of the filter is given by

$$H(s) = -\frac{1}{R_i C} \times \frac{1}{\left(s - j\frac{1}{R_\omega C}\right)} \qquad (5.1)$$

A sign change can easily be realized in a fully-differential implementation by reversing the input connections. The products $R_\omega C$ and $R_i C$ sets the center frequency and the gain of the complex resonators. An adjustable capacitor is used in the integrator to account for variations in the RC time-constants due to changes in absolute resistor and capacitor values as a result of process variations.

The first step in designing the resonator was to determine the capacitor and resistor values so that opamp loads can be known. In order to do this, noise caused by resistors and opamps in the resonators must be known. To estimate the equivalent input referred noise (IRN) of the first stage resonator, consider the circuit shown in Fig. 5.2. V_n represents a single opamp's equivalent IRN.

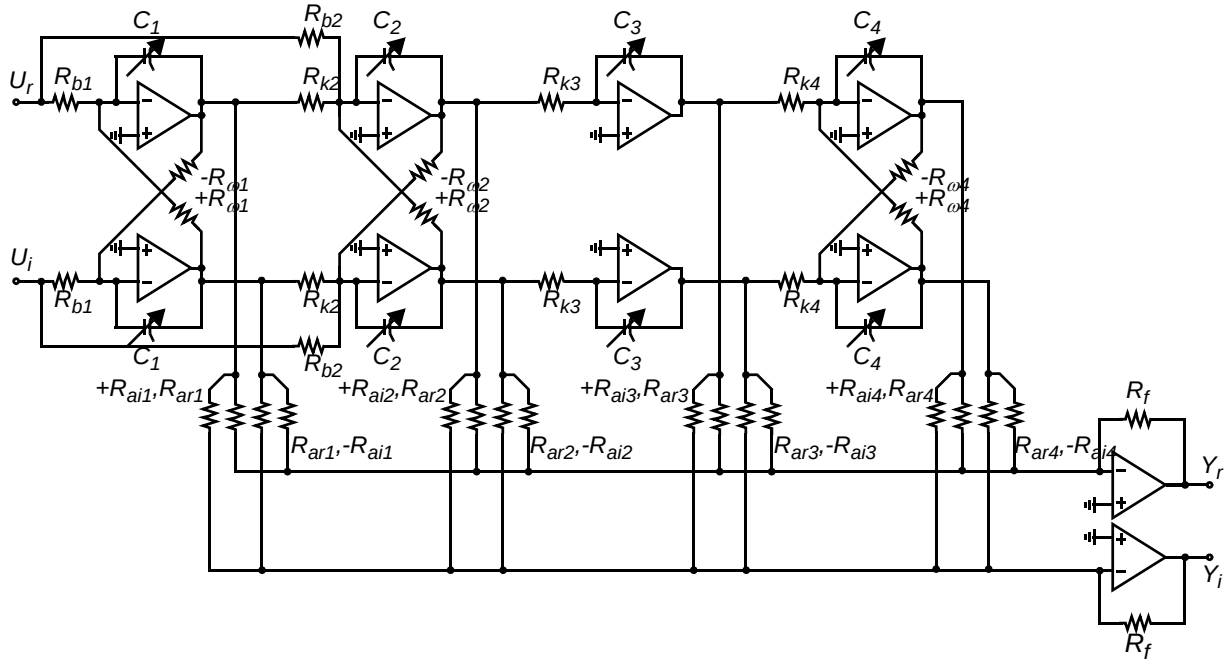

Fig. 5.1 Single-ended representation of the ADC loop filter.

Noise due to the finite on-resistance of the switched capacitors is modeled by V_{sw}. V_{R_i} and V_{R_f} represent the thermal noise of the resistors. Thermal noise of the feedback DACs is modeled with I_{DACn}. All noise sources are assumed to be uncorrelated and white. Referring half of the noise sources to the input of the real channel and the other half to the imaginary channel results in the following equivalent IRN in each channel:

$$V_{ni}^2(f) = V_{R_i}^2 + V_{R_\omega}^2\left(\frac{R_i}{R_\omega}\right)^2 + I_{DACn}^2(R_i)^2 + V_n^2\left|1 + R_i\left(\frac{1}{R_\omega} + j2\pi fC + \frac{1}{R_{sw} + 1/j2\pi C_{sw}}\right)\right|^2 + V_{sw}^2\left|\frac{j2\pi fC_{sw}R_i}{1 + j2\pi fC_{sw}R_{sw}}\right|^2 \quad (5.2)$$

Assuming the tuning capacitors, C_{sw} are small, the resonant frequency is largely determined by the product of R_ω and C, therefore noise due to the switches can be ignored since R_iC_{sw} will be small. Value of C and R_ω are fixed by the modulator parameters and are given by

$$C = \frac{1}{f_sR_ib_1}, R_\omega = \frac{b_1}{2\pi(f_1/f_s)}R_i \quad (5.3)$$

where f_1 is the resonant frequency of the first stage resonator and b_1 is gain of the first stage resonator. Since this is a filter with an asymmetric frequency response about DC, the resistor noise power spectrum density is given by 2*KTR*. The thermal noise of the feedback DAC current source is given by

$$I_{DACn} = 2KT\left(\frac{2}{3}\right)\frac{2(I_{DAC}/2)}{V_{eff}} = 2KT\left(\frac{2}{3}\right)\left(\frac{a_1}{b_1}\frac{1}{R_i}\right)\frac{1}{V_{eff}} \quad (5.4)$$

where I_{DAC} is the full scale current of the first feedback DAC and V_{eff} is the gate-to-source overdrive voltage $V_{GS} - V_{th}$ of the current sources. Eq. (5.2) can be further simplified by calculating the mean-squared value of the term that is due to the opamp noise, in the band of interest (DC to +20MHz).

$$\begin{aligned} V_{ni}^2 &= 2KTR_i + 2KTR_\omega\left(\frac{R_i}{R_\omega}\right)^2 + 2KT\frac{2}{3}\frac{a_1}{b_1R_iV_{eff}}(R_i)^2 + \frac{V_n^2\int_0^{2\pi\times f_{BW}}\left|1 + R_i\left(\frac{1}{R_\omega} + j\omega C\right)\right|^2 d\omega}{2\pi f_{BW}} \\ &= 2KTR_i\left(1 + \left(\frac{R_i}{R_\omega}\right) + \frac{2}{3}\frac{a_1}{b_1}\frac{1}{V_{eff}}\right) + V_n^2\left(\left(\frac{R_i + R_\omega}{R_\omega}\right)^2 + \frac{1}{3}(R_iC\times 2\pi f_{BW})^2\right) \\ &= 2KTR_i\left(1 + \frac{2\pi(f_1/f_s)}{b_1} + \frac{2}{3}\frac{a_1}{b_1}\frac{1}{V_{eff}}\right) + V_n^2\left(\left(1 + \frac{2\pi(f_1/f_s)}{b_1}\right)^2 + \frac{1}{3}\left(\frac{1}{b_1}\frac{2\pi}{OSR}\right)^2\right) \end{aligned} \quad (5.5)$$

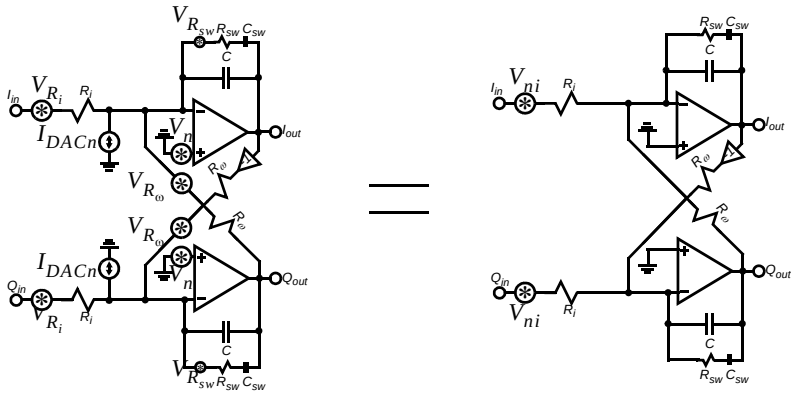

Fig. 5.2 Equivalent noise model of the complex resonator and with all noise sources referred to the input.

With a maximum stable input amplitude of $600\text{mV}_{\text{rms}}$ ($300\text{mV}_{\text{rms}}$ single-ended) and a desired SNR of 78dB due to thermal noise alone, the total IRN density in each channel must be less than

$$\frac{10^{-78/20}(600\text{ mV})}{\sqrt{20\times10^6}} \approx 17\text{nV}/\sqrt{\text{Hz}}. \qquad (5.6)$$

Assuming that the noise contribution of the resistors/DAC and opamp noise should be equal and and an operating temperature of 80C, then

$$\frac{1}{2}\left(\frac{10^{-78/20}(0.6)}{\sqrt{20\times10^6}}\right)^2 = 2KTR_i\left(1+\frac{2\pi(f_1/f_s)}{b_1}+\frac{2}{3}\frac{a_1}{b_1}\frac{1}{V_{eff}}\right)$$

$$\Rightarrow R_i \le 5.11\text{k}\Omega,\ R_\omega \le 27.86\text{k}\Omega,\ C \ge 0.87\text{pF}$$

Similarly solving for V_n for half the total in-band noise results in

$$\frac{1}{2}\left(\frac{10^{-78/20}(0.6)}{\sqrt{20\times10^6}}\right)^2 = V_n^2\left(\left(1+\frac{2\pi(f_1/f_s)}{b_1}\right)^2+\frac{1}{3}\left(\frac{1}{b_1}\frac{2\pi}{OSR}\right)^2\right)$$

$$V_n \le 10\text{nV}/\sqrt{\text{Hz}}$$

In order to achieve the same SNR in a fully differential implementation, the sum of resistance values in the positive and negative paths should be less than or equal to the above found resistance values. Similarly the parallel combination of the two integrating capacitors should be greater than or equal to the *C* value found above. The noise of the circuitry proceeding the first stage is referred back to the input of the ADC through the gain of the first resonator. Assuming the complex resonator has an infinite Q, then its attenuation function is given by

$$A(\omega) = \frac{j(\omega-\omega_1)}{b_1} \qquad (5.7)$$

Therefore, the root mean-square attenuation is

$$\frac{\sqrt{\int_0^{2\pi f_{BW}} \left|A(\omega_0+\omega)\right|^2 d\omega}}{2\pi f_{BW}} = \frac{\sqrt{\int_0^{2\pi f_{BW}} \frac{(\omega-\omega_1)^2}{\left|b_1\right|^2} d\omega}}{2\pi f_{BW}} = \frac{1}{\sqrt{3}b_1} \times \frac{\sqrt{(\omega_1)^3 + (2\pi f_{BW}-\omega_1)^3}}{2\pi f_{BW}} \qquad (5.8)$$

Thus, the rms value of the attenuation is 0.2571 in the band of interest. Thus the total noise of subsequent stages should be much less then $66\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ to be considered negligible. Therefore the noise of the second stage resonator can be ignored if the second stage opamp has an IRN density of less then $40\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, the input resistor that is much less than 46kΩ and an integrating capacitor that is much larger than 0.1pF. Table 5.1 summarizes the nominal resistor and capacitor values used in the resonator circuits. Note that the capacitor size used in the first stage is slightly larger than the

Parameter	Stage 1	Stage 2	Stage 3	Stage 4
Desired resonator center frequency for f_s=240MHz	6.6MHz	13.4MHz	DC	18.6MHz
Nominal integrating capacitor value (C_i)	1.92pF	0.450pF	0.450pF	0.450pF
Input resistor (R_{bi})	2.1kΩ	5.2kΩ	---	---
Inter-stage resistor (R_{ki})	---	7.6kΩ	10.1kΩ	29.1kΩ
Zero-setting resistor (R_ω)	11.2kΩ	23.2kΩ	---	16.3kΩ

Table 5.1: Capacitor and resistor values used in the ADC loop filter.

calculated value. This was done to add some margin of safety to the design. The second stage integrating capacitor is also much larger than the minimum required value for a similar reason.

5.2.3 Feedforward Adder

The feedforward terms in the block diagram (g_i) are implemented using an opamp in an opamp circuit in a R-R configuration. The major advantage of this circuit is that it is able to tolerate large voltage swings at its input without degradation in linearity. In order to choose the resistor values such that the non-idealities of the opamp are taken into account, the pulse response from the quantizer output to the quantizer input was matched to that of the desired NTF using Spice to simulate the loop filter's pulsed response.

5.2.4 Tuning Capacitor

To tune for absolute change in capacitor and resistor values, a large fixed capacitor and several switched capacitors were used in parallel to make the integrating capacitor. Resistors and capacitors can vary by as much as ±20% independently. This results in -30% to +56% shift in the center frequency of the resonators. Based on the results of chapter 4, sufficient performance can be attained by tuning the resonance frequency to within ±5% of the nominal value. Thus, using 11 fixed capacitor and 16 switched capacitors provides sufficient accuracy in tuning the center frequency. For noise consideration, the nominal value of the first stage integrating capacitor was set to 1.92pF which results in a unit capacitor size of 120fF. the subsequent resonator stages use a 28fF unit capacitor size.

To minimize loading the input of the opamp with parasitic bottom-plate capacitance where it can be more susceptible to substrate noise, the bottom plate of the capacitor was connected to the output of the opamp. To reduce large variation in V_{GS} of the switching transistors, the switches were connected to the input terminal side of the capacitors where voltage variation is small.

To facilitate tuning, the inputs of the switches were connected to a series of D-flip-flops to form shift registers. The correct tuning code could then be serially loaded into the flip-flops. Although, automatic tuning was not provided on chip, it can easily be implemented by using a slave resonator stage configured as an oscillator. By measuring the oscillation frequency of the oscillator relative to the clock frequency, it is possible to calculate the correct tuning code. A reset switch was also placed in parallel with the capacitors to reset the integrators to a known state during the code loading phase.

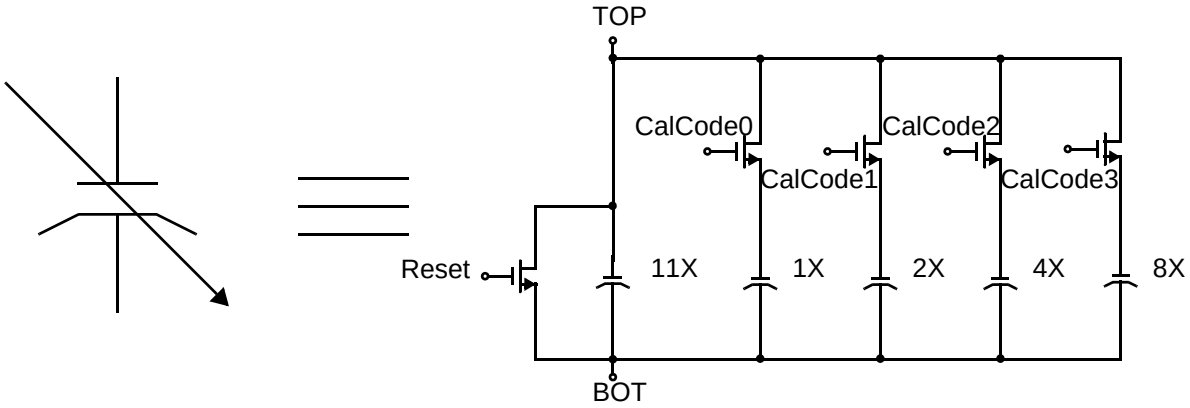

Fig. 5.3 Circuit used to tune for variations in RC time constant due to process variations.

5.2.5 Opamp Design

There are several issues that need to be considered in the opamp design. The opamp has to meet a certain criteria for voltage swing, gain, noise, and bandwidth. The opamp should be a) capable of driving small resistive loads, b) have a minimum gain of at least 40dB, c) IRN of the first stage opamp should be less than $10\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and d) the output voltage swing should be large (1.1V for the first stage opamp and 0.6V for subsequent stages). Requirement a) precludes the use of single stage opamp topologies such as folded or telescopic cascode as small resistive loads would greatly reduce the gain of the opamp. Therefore the opamp must either be a two stage or a single stage followed by a source follower. The use of source follower at the output is not very attractive since the output voltage swing will be limited by the source follower unless low-threshold devices are used. Low-threshold devices require an extra mask layer, and the minimum gate length of these types of devices is 2.5 times larger than the minimum drawn length of a regular device, which results in poor frequency response. Since the opamp gain requirement is not very large, it is possible to use a simple two stage, Miller-compensated opamp to meet all the above design criteria.

A circuit diagram of the opamp is shown in Fig. 5.4. The first stage is biased such that it met the majority of the gain and noise requirements, while the second stage is biased to meet the voltage swing requirements. Fig. 5.5 shows the continuous-time common-mode feedback (CMFB) used in the opamp. The average output voltage of the opamp is sensed across the resistors, R_{CMFB}. The average value of the output is then compared against the desired CM level, V_{cmin}. A signal that is proportional to the difference of the two voltages is then used to control V_{ctrl} which due to feedback will force the output to the desired CM level of V_{cmin}=0.8V. A relatively low CM level is chosen because the input differential pair are PMOS devices. Since the output is sensed across two linear poly resistors, this type of CMFB circuit will be highly linear.

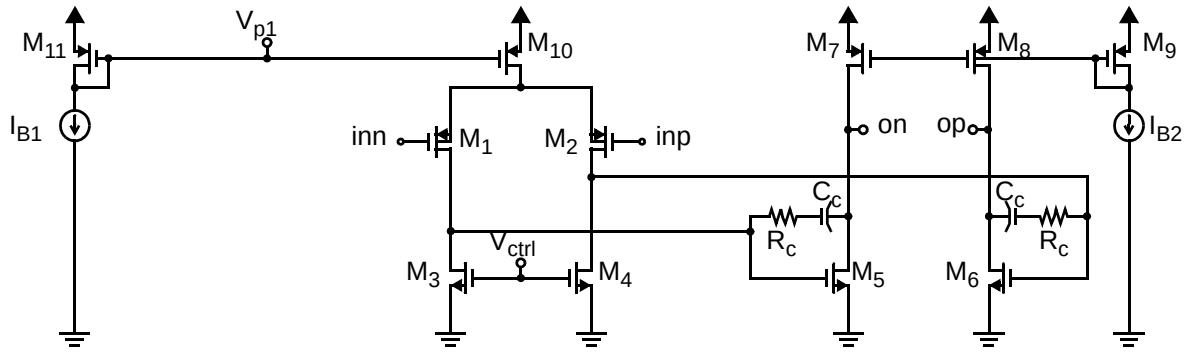

Fig. 5.4 A simple two stage Miller compensated opamp.

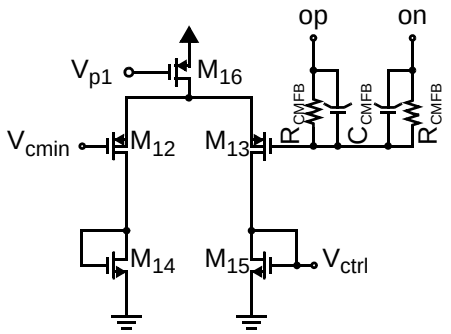

Fig. 5.5 CMFB circuit used in opamp shown in Fig. 5.4.

The second opamp design requirement is that the equivalent opamp IRN must be less than $10\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The IRN of the opamp will be dominated by the input stage and is approximately given by

$$V_n^2 = 2KT\left(\frac{2}{3}\right)\frac{1}{g_{m_{1,2}}} + 2KT\left(\frac{2}{3}\right)\frac{g_{m_{3,4}}}{g_{m_{1,2}}} \qquad (5.9)$$

In order to minimize the IRN of the opamp, the input differential pair g_m ($M_{1\text{-}2}$) must be maximized while the g_m of the active load devices ($M_{3\text{-}4}$) should be minimized. Thus, minimum length transistors are used in the input differential pair, while large length devices are used in the active loads. The output stage is used drive the resistive loads, therefore minimum length transistors are used at the output so that transconductance of the output transistors ($M_{5\text{-}6}$) can be maximized. The reason for using a PMOS input differential pair is so that the output stage can use NMOS devices which have higher g_m for a given W/L ratio. PMOS devices also tend to have lower 1/f noise [3].

The stability of the opamps were verified with both AC and transient simulations. For transient simulations, the opamps were configured as integrators in the resonator circuit and a sharp pulse was applied at the input of the resonators. The output was then checked for any signs of high frequency oscillation, which would be a sign of possible instability. The simulations were performed in the best/worst process corner, high/low temperature and supply voltage. The opamp device sizes are summarized in Table 5.2.

Component	Stage 1 opamp	Stage 2-4 opamp	Feedforward opamp
$M_{1,2}$	80/0.18	64/0.24	64/0.18
$M_{3,4}$	20/1.0	8/0.36	8/0.18
$M_{5,6}$	32/0.18	12/0.18	24/0.18
$M_{7,8}$	128/0.18	48/0.18	96/0.18
M_9	8/0.18	8/0.18	8/0.18
M_{10}	160/0.36	64/0.36	128/0.36
M_{11}	16/0.36	8/0.36	16/0.36
I_{B1}	60μA	30μA	60μA
I_{B2}	60μA	60μA	90μA
R_c	0.5kΩ	1.0kΩ	1.5kΩ
C_c	600fF	250fF	300fF
$M_{12,13}$	16/0.24	16/0.24	4/0.24
$M_{14,15}$	4/1.0	2/0.36	2/0.18
M_{16}	32/0.36	16/0.36	32/0.36
R_{CMFB}	20kΩ	40kΩ	40kΩ
C_{CMFB}	50fF	50fF	50fF

Table 5.2: Summary of opamp device sizes. Sizes are given in μm, as width divided by length, unless otherwise labelled.

5.3 Current Steering DAC Design

5.3.6 1st Stage Current Source Feedback DACs

One of the most critical blocks in any ΔΣ ADC is the first feedback DAC, DAC1. As discussed in chapter 4, any noise introduced by DAC1 will not be shaped by the loop filter and hence will appear directly at the input of the ADC. It is critical that the first feedback DAC be properly designed and laid out.

The feedback DAC that is used in this design is based on a current steering DAC architecture. In this type of DAC, an array of matched current sources are connected to the load, which in this

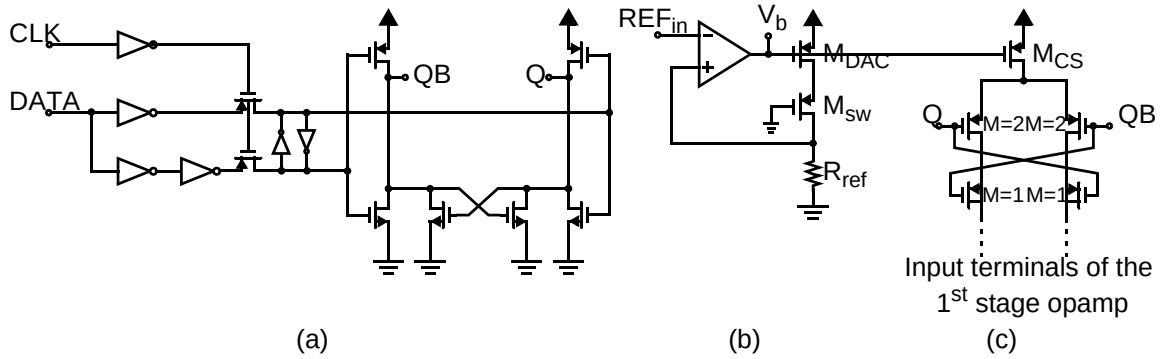

Fig. 5.6 (a) Switch driver for DAC1 (b) Biasing circuit for DAC1. (c) Single current cell of DAC1.

design is the input of the first stage resonator. Switches connected in series with the current sources steer the current from one side to the other based on the digital input code. This type of DAC can operate at frequencies above 1GHz [17], [24] and is ideally suited as a feedback DAC for a high speed ΔΣ ADC.

The input pair of the opamps are PMOS devices with a low CM voltage, therefore the ideal current source to drive the input of the opamp is PMOS current sources. This is because the low CM voltage allows for larger drain-to-source voltage across the current sources, which in turn allows one to use larger V_{eff} in the current sources. Large V_{eff} voltage improves the matching characteristics of the current source array. Random mismatch between two current sources is approximately inversely proportional to the V_{eff} voltage and is given by [16]

$$\frac{\Delta I_D}{I_D} = \frac{A_{VT}}{\sqrt{WL}} \cdot \frac{2}{V_{GS} - |V_{tp}|} + \frac{A_\beta}{\sqrt{WL}} \qquad (5.10)$$

where A_{VT}, A_β are the threshold voltage mismatch an the β mismatch coefficients respectively.

A circuit diagram of a single cell of DAC1 is shown in Fig. 5.6. The DAC current source M_{CS} is sized such that in the worse corner (FF, low temperature and +20% R), the mismatch will be less than 0.5%. The DAC current sources are biased using the circuit shown in Fig. 5.6b. In this circuit, the full scale current of the DAC will track variations in absolute resistor values and hence the time-constant created by the DAC current sources should track RC time-constant variations elsewhere in the modulator.

Another important block in a current steering DAC design is the switch driver. The task of the switch drive is to latch the incoming DAC code and to perform final synchronization. Another function of the switch driver is to shift the crossing point of the switch transistors' differential control signals (Q and QB) in such a way that the switches are never simultaneously in the off

state [17]. This ensures that V_{DS} of the current source device stays relatively constant. The switch driver used is shown in Fig. 5.6a. It is based on a design described in [17]. The crossing point of QB and Q was made low so that the current source M_{CS} device is always in saturation. Charge cancellation transistors are also used in the switches to reduce the effect of charge injection and clock feed through.

5.3.7 2nd feedback DAC

A circuit diagram of the 2nd feedback DAC, DAC2 is shown in Fig. 5.7. The matching characteristics of the second DAC current sources are not very critical as the output is connected directly to the input of a coarse quantizer. Therefore the current sources are sized for only 1% matching of the drain-to-source current. Synchronization of the incoming DAC code is also redundant as the flash input is sampled by a clock signal already. Hence, only a simple non-clocked latch is used for the switch driver. The function of the latch is to ensure that the crossing point of the Q and QB signals remain low.

To increase the full-scale current of DAC2, a current divider is used at the output of DAC2. Also, since the matching requirement of DAC2 is not critical, extra settling time can be given to DAC2 by connecting the input of DAC directly to the output of the flash, without going through the ESL block.

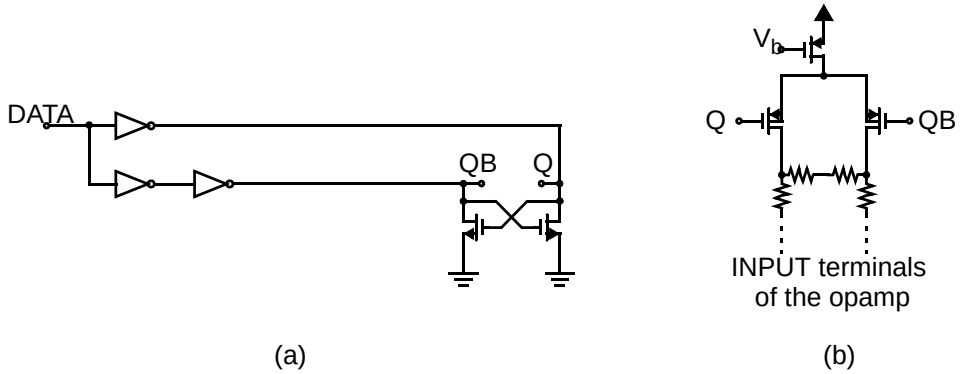

Fig. 5.7 (a) Switch driver for DAC2. (b) Single current cell of DAC2.

5.4 Flash ADC Design

One of the least critical blocks in a ΔΣ ADC is the flash. This is because any noise or error generated by the flash is subject to the same attenuation as the quantization noise. Hence errors in the flash will result in only a small degradation in performance.

The 17-level flash is made up of 16 comparators. A single cell of the comparator circuit is shown in Fig. 5.9. It consists of a preamplifier stage, a dynamic comparator and an SR latch. The role of the resistively loaded preamplifier is to compare the differential input signal to a differential reference signal and amplify the difference. The input pairs of the preamplifier were sized such that the input referred offset of the preamplifier would be less than 8mV. The gain of the preamplifier is 5V/V and a unity gain frequency is 1400MHz. The role of the preamplifier is to reduce the input-referred offset of the dynamic comparator. It also isolates the relatively noisy dynamic comparator from the input nodes of the flash. This is critical since large voltage swings at the internal nodes of the dynamic comparator will generate large kickback signals. The reference signals for the flash are generated on chip using a resistor ladder. MOS capacitors are placed on the *refp* and *refn* nodes, to stabilize the reference voltage. Note that one major disadvantage of this type of preamplifier design, is that any difference in the CM level of the input and the reference signal will reduce the gain of the preamplifier, which increases the input-referred offset of the dynamic comparator. The gain of the preamplifier is proportional to the g_m of the input pairs $M_{1,4}$. A lower CM level at the reference will reduce the amount of current that will flow in the input pair transistors near the trip point of the comparators. Hence, the g_m of the input pair $M_{1,4}$ will be reduced which in turn reduces the gain of the amplifier. Fig. 5.8 shows the simulated DC gain of the preamplifier vs. input and reference CM level difference. According to these simulations, the CM level of the reference and the input should be kept within 100mV of each other.

To reduce power consumption, dynamic comparators are used in the flash. The dynamic comparator is based on a design described in [18]. During the reset phase, when latch signal is low, M_{13} is off and there is no DC path to ground. Simultaneously, $M_{11\text{-}12}$ reset the output of the dynamic comparator high to VDD while $M_{7\text{-}8}$ pull the drain of $M_{5\text{-}6}$ high. When the latch signal is turned high, transistors M_{13} enters saturation and begin to conduct current. The switching direction of the

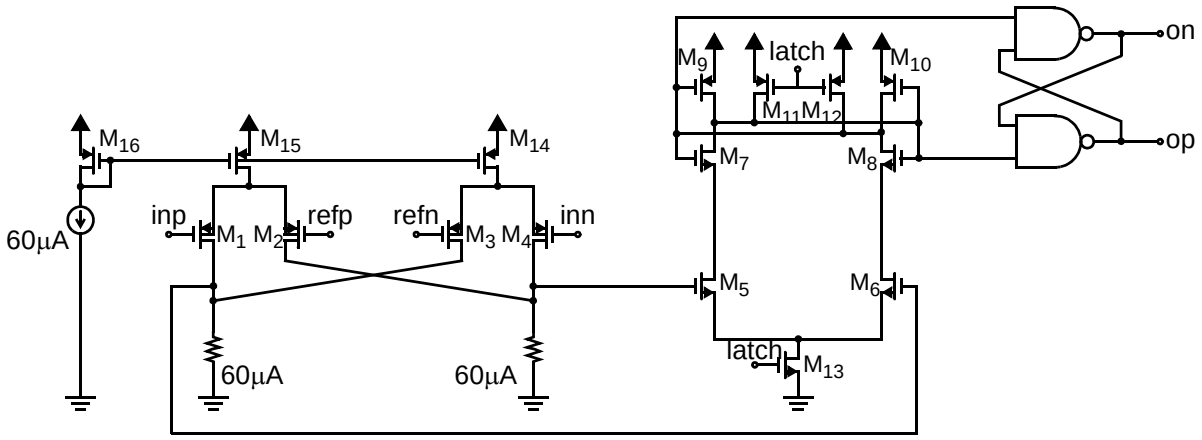

Fig. 5.9 CMOS comparator.

comparator is then determined by current division in the input differential pairs $M_{5\text{-}6}$. The input-referred offset is approximately determined by the the offset of the input differential pair.

A simple SR latch is used to latch the output of the comparators. When the dynamic comparator is in reset phase, the output is held high and so the cross-coupled NAND gates will hold their previous value. During the compare phase, when the latch signal goes low and the comparator makes a decision, the SR latch will change to its new state. Monte-Carlo simulation of a single comparator cell were performed to ensure the standard deviation of the offset is less than 8mV with device sizes chosen.

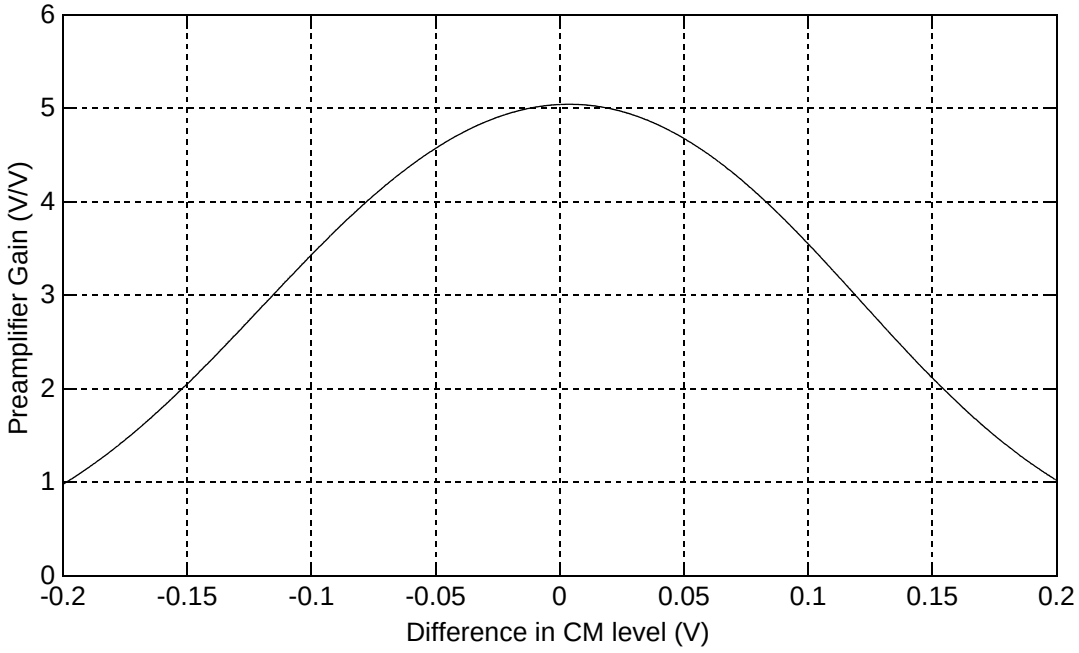

Fig. 5.8 Preamplifier gain vs. difference in CM level.

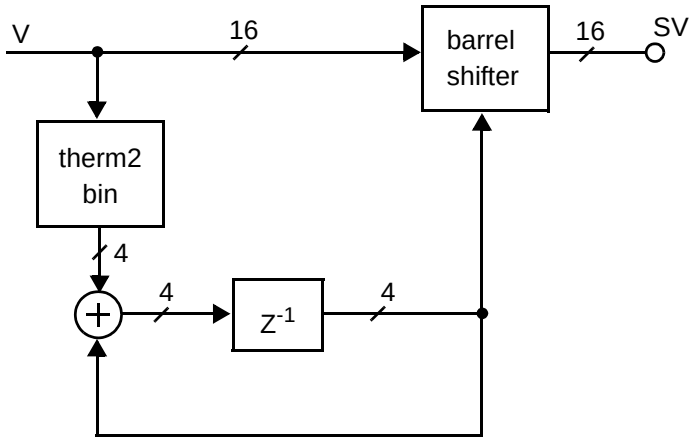

Fig. 5.10 Block diagram of the DWA circuit.

5.5 Element Selection Logic

A block diagram of the DWA block is shown in Fig. 5.10. The incoming signal from the flash, V, is converted from thermometer to binary format. The binary value is then fed into a 4-bit digital accumulator, which drives the control signal of a barrel shifter. The barrel shifter then rotates the incoming thermometer coded values by the amount specified by the control signal. The output of the barrel shifter, the selection vector (SV) is connected to the input of DAC1 which is also thermometer coded.

The DWA block was described in Verilog at the behavioral level. The circuit was then synthesized using Synopsis' Design Compiler. In the worst process corner (high temperature, SS and low supply voltage) the circuit has a maximum critical path delay of 1.4ns (maximum allowable delay is approximately 2ns). Finally, place and route tools were used to generate the layout from the synthesized Verilog code using CMC provided standard cells.

5.6 Transistor Level Simulation

The complete transistor level schematic of the ADC was simulated in Spice. The clock duty cycle was then adjusted until the output spectrum spectrum matched more closely the desired NTF. The difference between the simulated duty cycle and the desired duty cycle of the clock provided an estimate of latency in the flash. Finally the pulse response of the loop filter from the quantizer

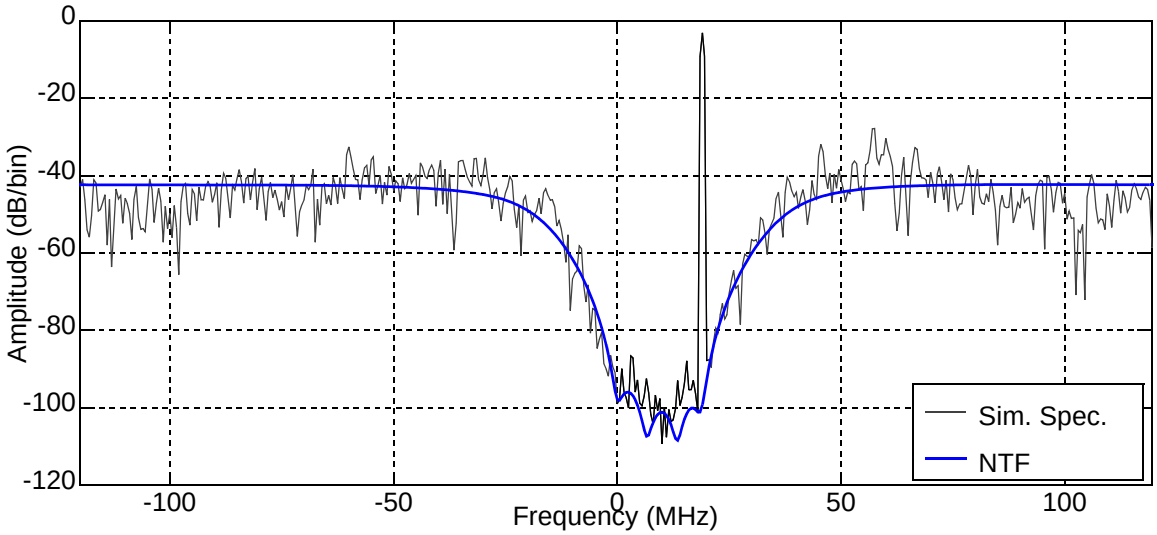

Fig. 5.11 Simulated spectrum of the ADC using initial values of g_i.

output to the quantizer input was matched to that of the target NTF, with the sampling instance moved to take in to account the latency of the flash.

Fig. 5.11 shows the results of simulation with a 50% duty cycle clock using the initial resistor values in the feedforward amplifier. Note that the desired NTF and simulated spectrum match well however there is some out-of-band peaking of the simulated spectrum. This is due to the extra latency introduced by the flash. Fig. 5.12 shows the output spectrum with the DAC clock advanced by 700ps, to cancel the extra loop delay caused by the flash. Note that the simulated spectrum and the NTF are now much more closely matched. To take into account the extra 700ps of delay in the feedback loop, the feedforward coefficients were adjusted to take into account the latency of the flash. This was done by matching in the pulse response of the loop filter to the NTF at a sampling

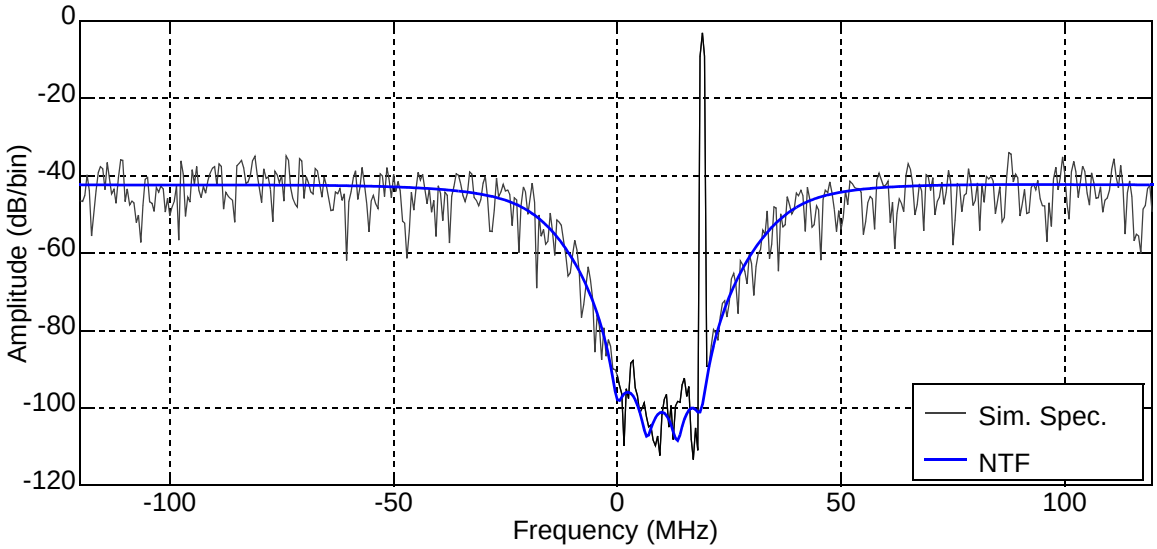

Fig. 5.12 Simulated spectrum of the ADC with the DAC clock advanced by 700ps.

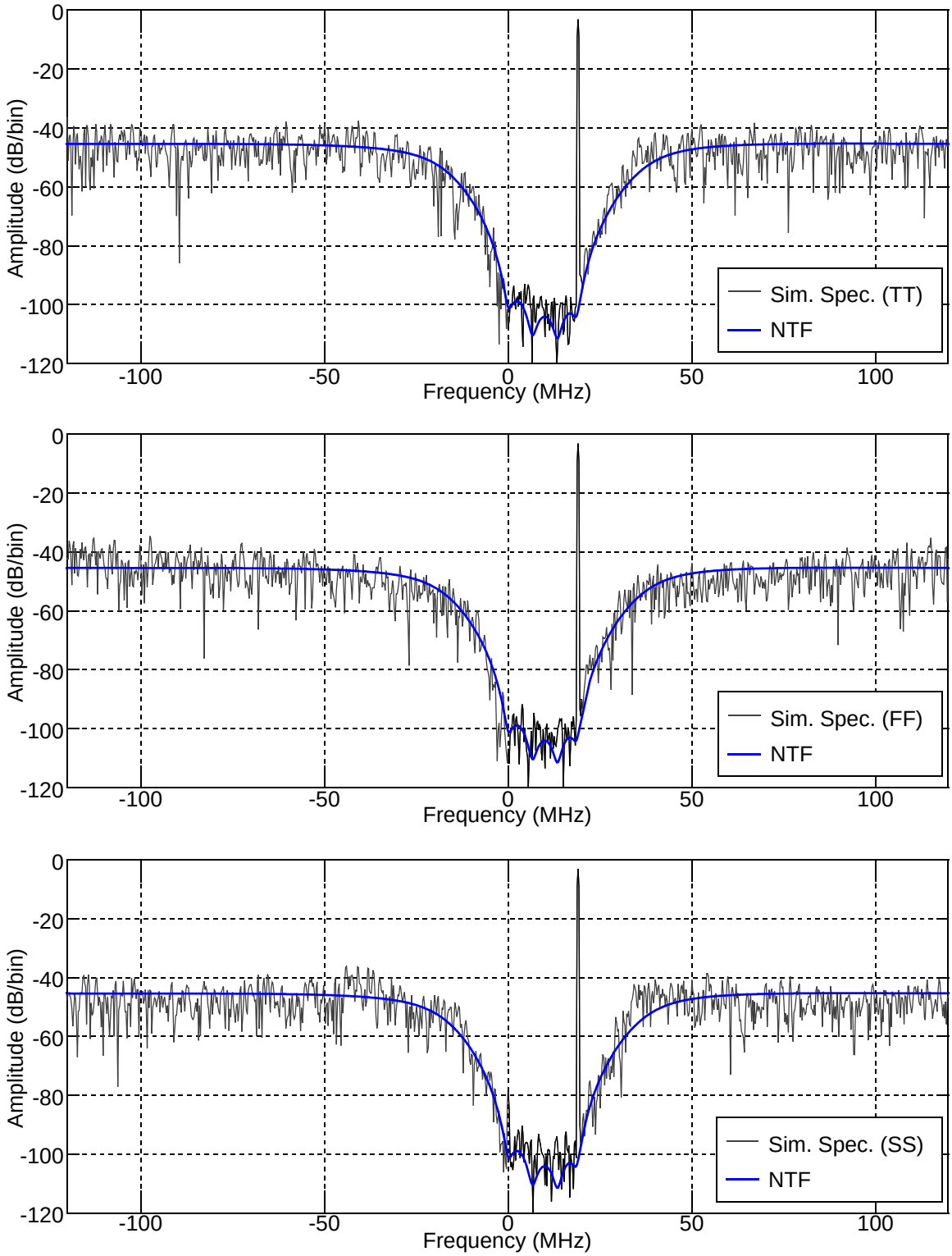

Fig. 5.13 Simulated spectrum of the ADC with the new coefficients. (a) Spice simulation results using the typical library, 60C and typical absolute resistor and capacitor values. (b) Spice simulation results using the fast-fast library, 0C and -20% resistors and capacitor values. (c) Spice simulation results using the slow-slow library, 80C and +20% resistors and capacitor values. N_{FFT}=960

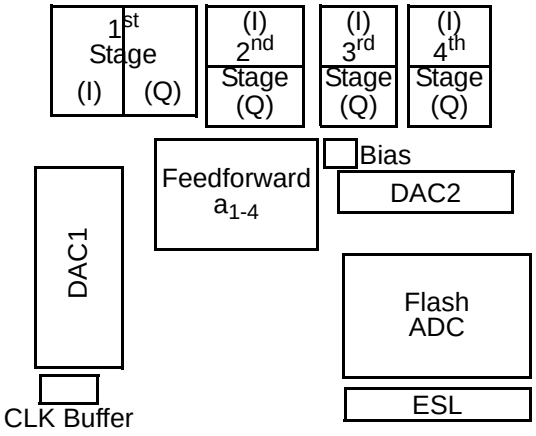

Fig. 5.14 Modulator floor-plan.

point that was delayed by 700ps. To verify that the modulator is fully functional in the presence of process variation, the ADC circuit was also simulated in the fast-fast corner at low temperature with the absolute value of the resistors and capacitors scaled by -20% each. Note that a different capacitor tuning code was used to set the correct center frequency of the resonators. Similarly the modulator was simulated in the slow-slow corner at high temperature (80C) with the absolute value of the resistors and capacitors scaled by +20%. A correct capacitor tuning code was again used to account for the increase in the RC time-constant. The results of these simulations are shown in Fig. 5.13.

5.7 Layout Issues

Layout is very important in high performance mixed-signal circuits. A good IC layout starts with a good floorplan. Fig. 5.14 shows the floorplan of the chip. Note that the first stage resonator and DAC were placed as far away as possible from the ESL and flash. This was done to minimize any noise being injected from the digital circuitry into the sensitive first stage through the substrate. The analog and digital power supplies are connected to their own separate pads to further improve isolation. MIM capacitors were placed in blank areas and connected to the closest power supply to act as on-chip decoupling capacitors.

Dummy devices were placed on the edges to improve the matching characteristic of capacitors and resistors. The transistors that are required to be well matched such as transistors in a differential pair are laid out in an interdigitated fashion. Care is taken to match the length and the environment of the interconnect wires in differential paths and the real and imaginary paths. Critical high im-

pedance nodes such as voltage references are shielded from the substrate by surrounding the wires inside a grounded metal shield. Common-centroid layout technique is used in the DAC current source array to reduce gradient effects. The NMOS devices in the DAC1's switch drivers were placed in a deep NWell tub to improve isolation from the substrate. In order to minimize power supply induced jitter on the clock signal of DAC1, its switch driver and clock buffer are connected to separate power supply pin.

To improve isolation of the analog circuit from the noisy digital circuit such as the output drivers, the digital pads are placed as far away from the first stage resonator as possible. In high resolution ADCs, the output pad drivers can be a major source of substrate and power supply noise. In order to minimize this source of noise, ideally the output of ADC should be taken off chip using a differential signaling schemes such as LVDS. However due to lack of silicon area, the output drivers had to use full CMOS level logic signals. To reduce the amount of noise generated by the output drivers, the inverters' NMOS devices are placed in a deep N-wells to improve isolation from the substrate. Complete layout of the IC is shown in Fig. 5.15.

5.8 Post-Layout Simulation

The parasitic capacitance of each individual block was separately extracted and simulated to verify correct operation. The complete layout was also extracted and simulated. The simulated

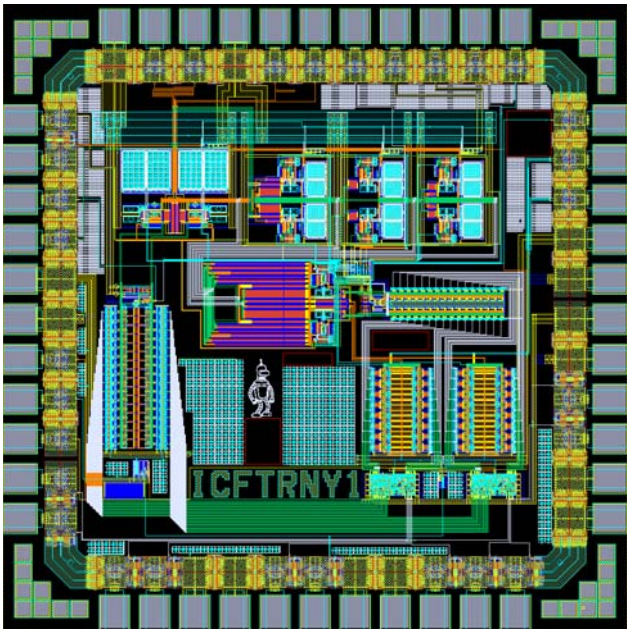

Fig. 5.15 Modulator layout

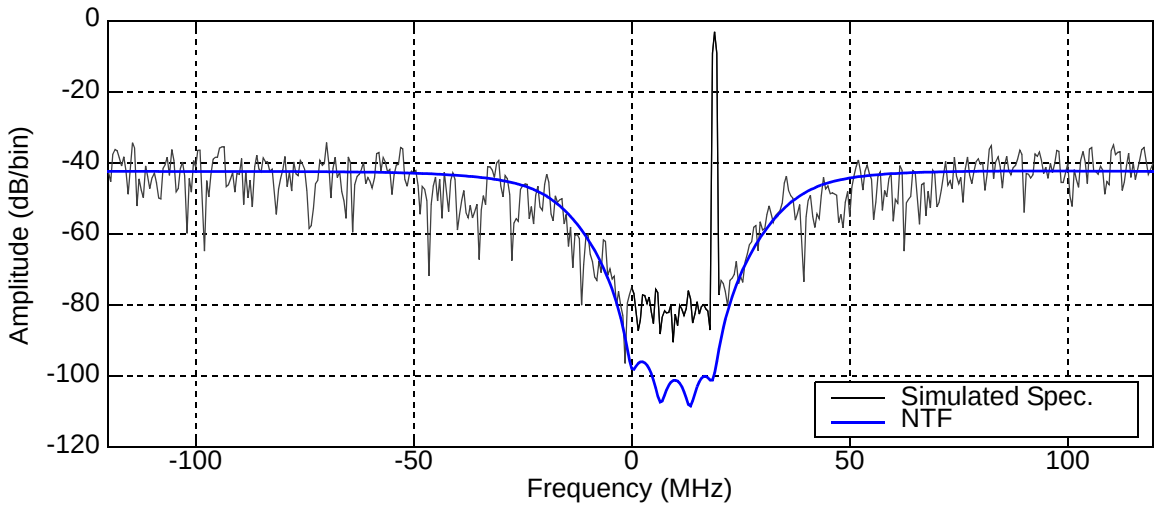

Fig. 5.16 Simulated spectrum of the extracted using the typical library, 60C and typical absolute resistor and capacitor values. N_{FFT}=480.

spectrum of the post layout netlist is shown in Fig. 5.16. Post-layout simulations of the modulator showed a peak SNR of only 62dB. Removing all the parasitic capacitors from the extracted netlist resulted in only 2dB improvement in SNR. One possible reason for this could be the accuracy/tolerances of the simulator. The number devices in the extracted netlist is much larger than the number of devices in the schematic netlist. This is because large transistors are made with several smaller devices in parallel. This increases the number of devices in the netlist which increases the complexity of the circuit by an order of magnitude. It is possible that the accuracy of the simulation is affected as a result of this.

5.9 Summary

The design procedure for realizing the desired modulator in a standard 0.18μm CMOS process was discussed. The key blocks such as the loop filter, flash, DAC and ESL block were described in detail. Spice level simulations of the modulator was used to improve the robustness of the design by taking in to account some non-idealities of the circuit implementation of the modulator. Some layout issues was also discussed.

CHAPTER 6

Experimental Results and Conclusions

This chapter describes the experimental testing of the ADC designed in the previous chapters. A description of the test board is followed by presentation of experimental results. The measured performance of the chip is discussed and compared with previously published works.

6.1 The Silicon Integrated IC

A die micrograph of the modulator implemented in a 0.18μm 1-poly 6-metal CMOS process is shown in Fig. 6.1. The IC was fabricated by TSMC via CMC. All the major blocks discussed in the previous chapter are highlighted with an overlay. The core area without the output pads is $0.95mm^2$.

6.2 Test Setup

A four layer printed circuit board (PCB) was designed to test the chip. The two internal board layers were dedicated to the power supplies. The analog, digital and digital I/O power supplies were isolated from each other by using separate voltage regulators and separate planes for each supply. In addition to providing decoupling capacitor at the output of the voltage regulator, local decoupling capacitors were also placed at each power supply pin near the IC.

The clock signal was provided either by an Epson EG-2101CA surface acoustic wave (SAW) oscillator or an Agilent 8130A pulse generator. To convert the ECL level signal of the SAW oscillator to a 1.8V CMOS level signal, first the signal was convert from ECL to 3.3V CMOS level signal. The signal was then converted from 3.3V level signal to 1.8V signal using another chip.

The input signal came from two synchronized Rhode & Schwarz SMT03 signal generators. The output of the generators was first low-pass filtered using external Mini-Circuits filters. To generate a single complex tone, the phase of one of the signals was adjusted until 90° phase shift be-

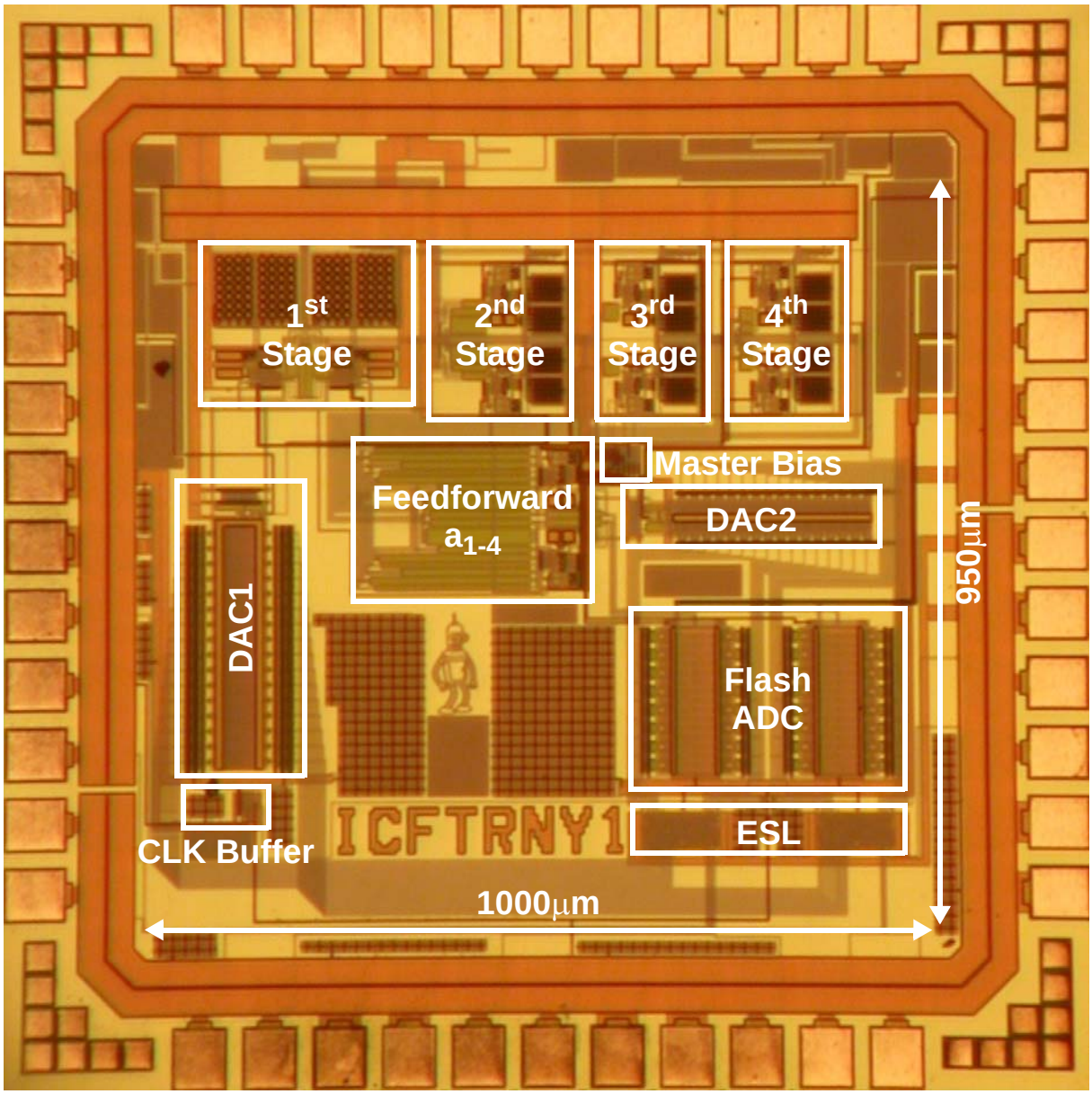

Fig. 6.1 Micrograph of the IC

tween the two signals was obtained as observed on an oscilloscope. For the two tone tests, shown later in this chapter, a quadrature signal was obtained from a Mini-Circuits 90° phase shifter. Single-ended to differential conversion was done using Mini-Circuits RF transformers, with the center tap connected to the CM of the chip.

The off-chip reference signals such as the bias current and common-mode level were generated using potentiometers configured as voltage dividers. The IC output data was captured using a Tektronix TLA704 logic analyzer. The maximum synchronous data capture rate of this logic analyzer is only around 200MHz. In order to capture data at a faster rate, the output of the chip was muxed

using several off-chip flip-flops. The acquired data was then demuxed and the digital signals I and Q signals were combined as I+jQ in Matlab. The FFT of the data was taken using a Hann window. SNDR measurements are calculated by comparing the total in-band signal power to the total power of in-band noise plus distortion and spurs. For SNR measurements, the first 5 harmonic of the signal were ignored.

6.3 Experimental Measurements

The first step in testing the modulator is to tune the resonator circuits to the correct center frequency. Since the unit capacitor size is different in stage 1, a slightly different code was used for that stage. However stage 2-4 share the same tuning code. To find the correct calibration code for the capacitor array, the input of the modulator was nulled. The reason for this is because the modulator is more likely to be stable even with an incorrect tuning code if the there is no signal present. The correct tuning code was then found by finding the tuning code which resulted in the best match between the measured spectrum and the desired NTF.

Fig. 6.2 shows the output spectra of the ADC at various sampling rates with the DWA block turned on and input signal frequency of 5.0MHz. Fig. 6.3 shows the output spectra with the DWA block turned off and the same input signal. Note that the performance of the modulator is much better with the DWA turned off. Fig. 6.4 and Fig. 6.5 show measured SNR/SNDR vs. input power for different clock frequencies with the DWA turned on and off respectively. Notice again that the peak SNDR is much larger with the DWA block turned off, whereas SNR is roughly the same. This is because there is more harmonic distortion with the DWA block turned on. A plot of peak SFDR/SNDR/SNR vs. input signal frequency at several clock frequencies is shown with and without DWA turned on in Fig. 6.6 and Fig. 6.6. Fig. 6.8 shows the two-tone intermodulation test. The two frequencies are such that the intermodulation products fall at just the edge of the passband of the ADC. The measured signal transfer function is shown in Fig. 6.9. A plot of the ADCs measured IRR as a function of input frequency is shown in Fig. 6.11 at 250MHz sampling rate. Measured IRR was greater than 45dB. A summary of the measurement results is shown in Table 6.1.

One possible explanation for the degradation in ADC performance with the DWA block turned on could be that the errors generated by the DAC's rise/fall time mismatch being greater than the DAC's static mismatch. Although, the feedback DAC used in this design is fully differential and

hence the rise and fall times should ideally be the same, there will still be some asymmetry due to random mismatch of the switching and the latch transistors. According to Monte-Carlo Spice simulations of the DAC circuit, the expected mismatch is about 10ps and the expected static mismatch assuming that the PMOS transistors have a nominal V_{eff} is about 0.25%.

The noise generated by dynamic errors is roughly proportional to the number of DAC elements that are switched per clock period. DWA algorithm increases the switching activity of the DAC elements since at every clock period a new set of DAC elements need to be turned on, even if the input code is changing very slowly (i.e. a high *OSR* modulator). Hence it is reasonable to expect that DWA degrades the performance of the modulator if DAC mismatch is dominated by dynamic mismatch. In [25] it is shown that asymmetrical switching errors introduce even harmonic distortion in the differential output signal of a current-steering non-return-to-zero DAC. Furthermore, it is shown that the amplitude of the even order harmonics increases with the DWA algorithm enabled.

To verify that DAC mismatch as a possible culprit of SNDR degradation, the modulator was simulated in Matlab with 15ps rms of random mismatch in the DAC1's rise and fall times. An extra mismatch of 5ps is reasonable and could be the result of non-symmetrical layout of the DAC cell. A histogram of the resulting modulator SNDR is shown in Fig. 6.10. Note that the mean SNDR value with and without DWA is very close to the SNDR measurements done in the lab. Hence it is reasonable to assume that the slight degradation in modulator performance is due to mismatched DAC rise/fall times.

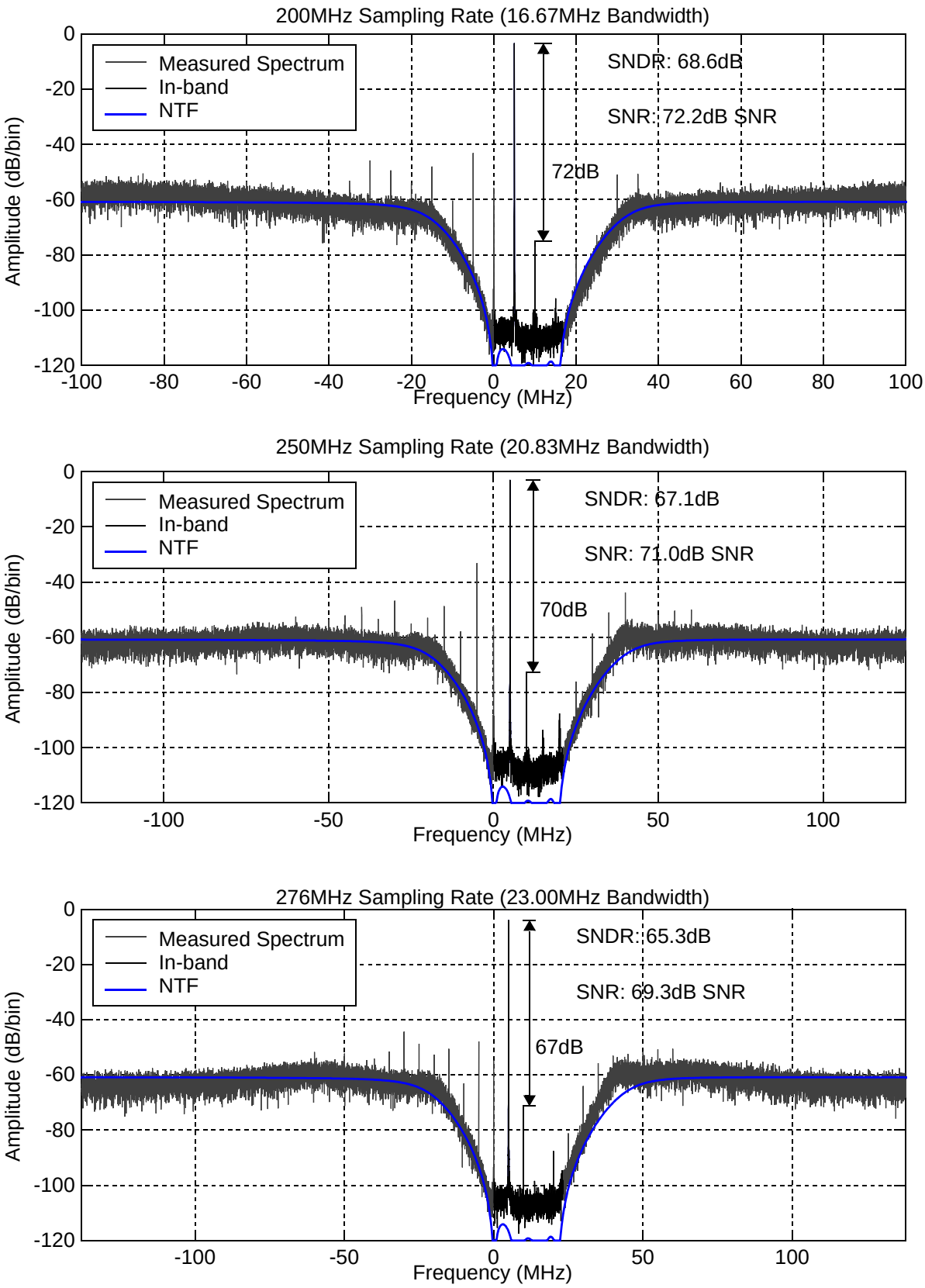

Fig. 6.2 Measured spectra at different clock frequency with an input signal frequency of 5.0MHz (DWA turned on, N_{FFT}=32768).

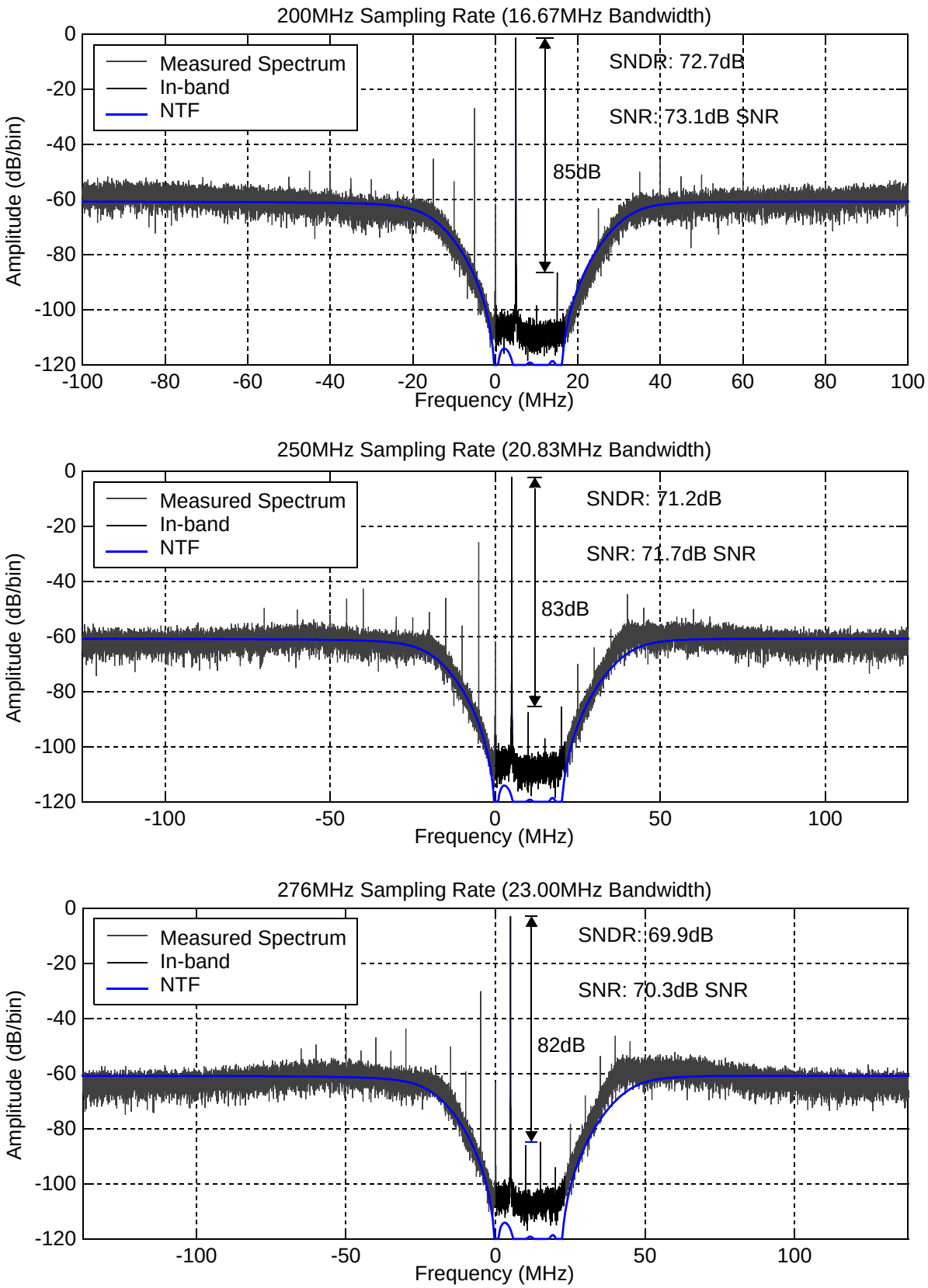

Fig. 6.3 Measured spectra at different clock frequency with an input signal frequency of 5.0MHz (DWA turned off, N_{FFT}=32768).

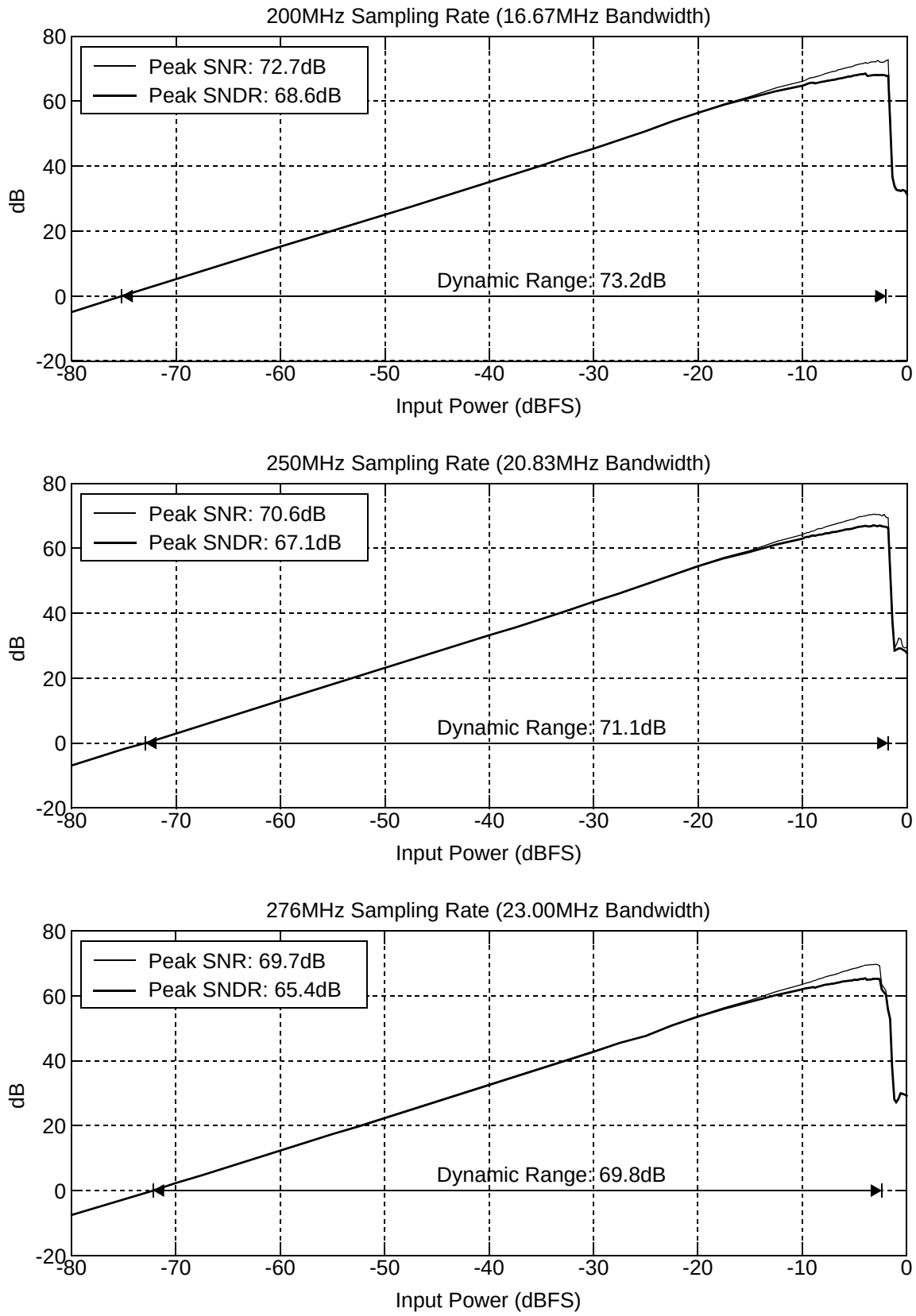

Fig. 6.4 Measured SNR/SNDR vs. input signal power at different clock frequency with an input signal frequency of 5.0MHz. (DWA turned on).

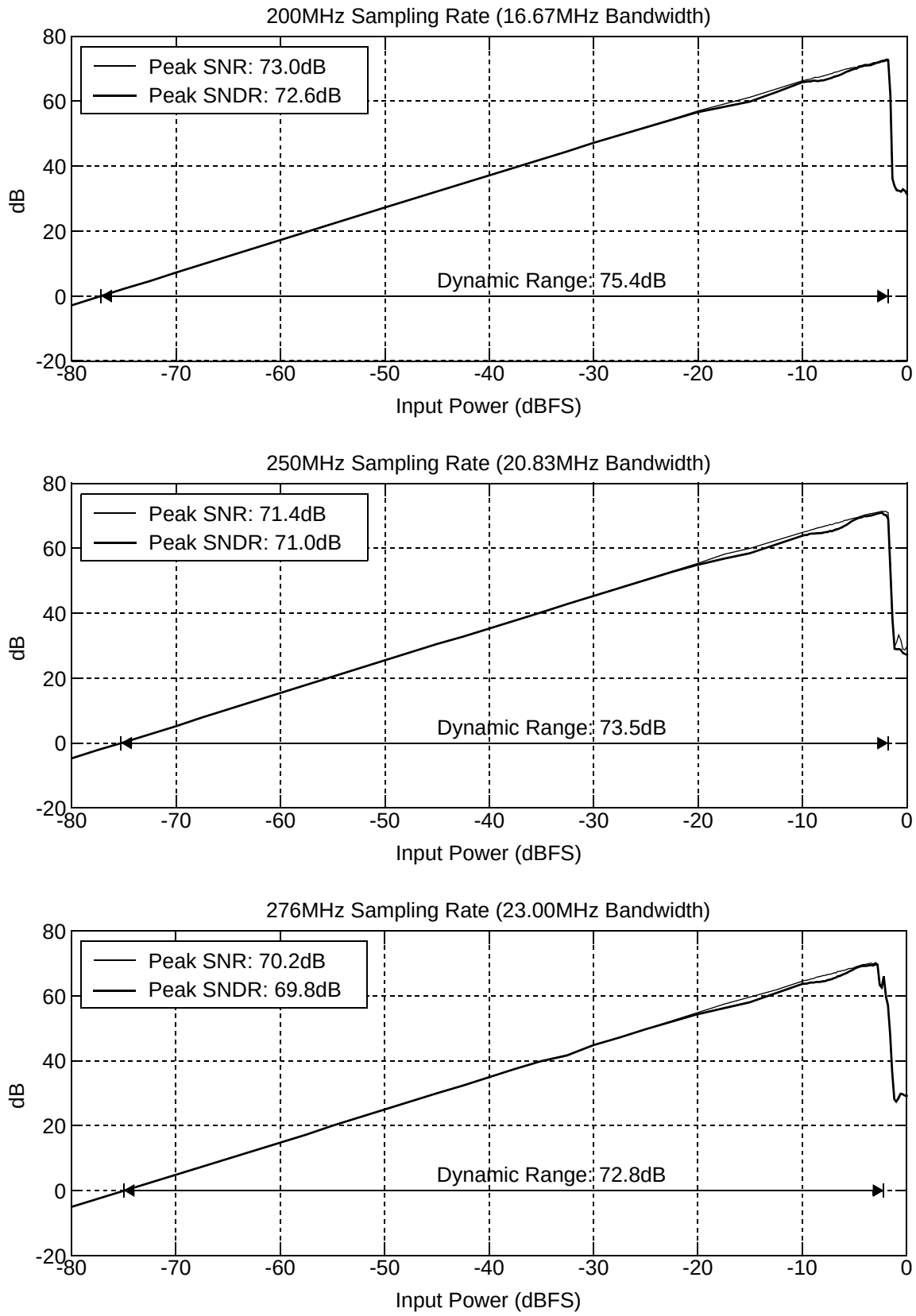

Fig. 6.5 Measured SNR/SNDR vs. input signal power at different clock frequency with an input signal frequency of 5.0MHz. (DWA turned off).

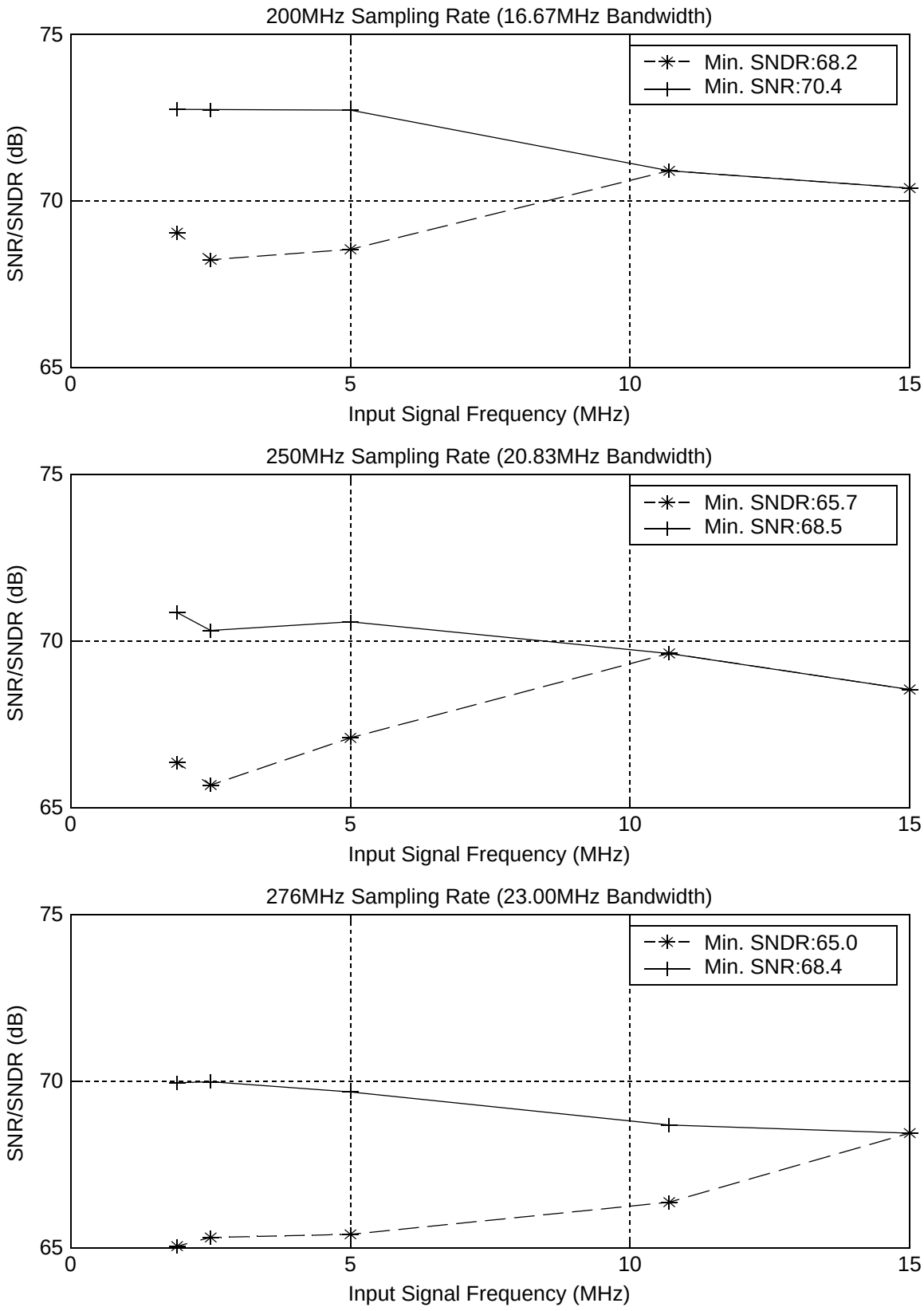

Fig. 6.6 Measured SNR/SNDR vs. input signal frequency at different clock frequency (DWA turned on).

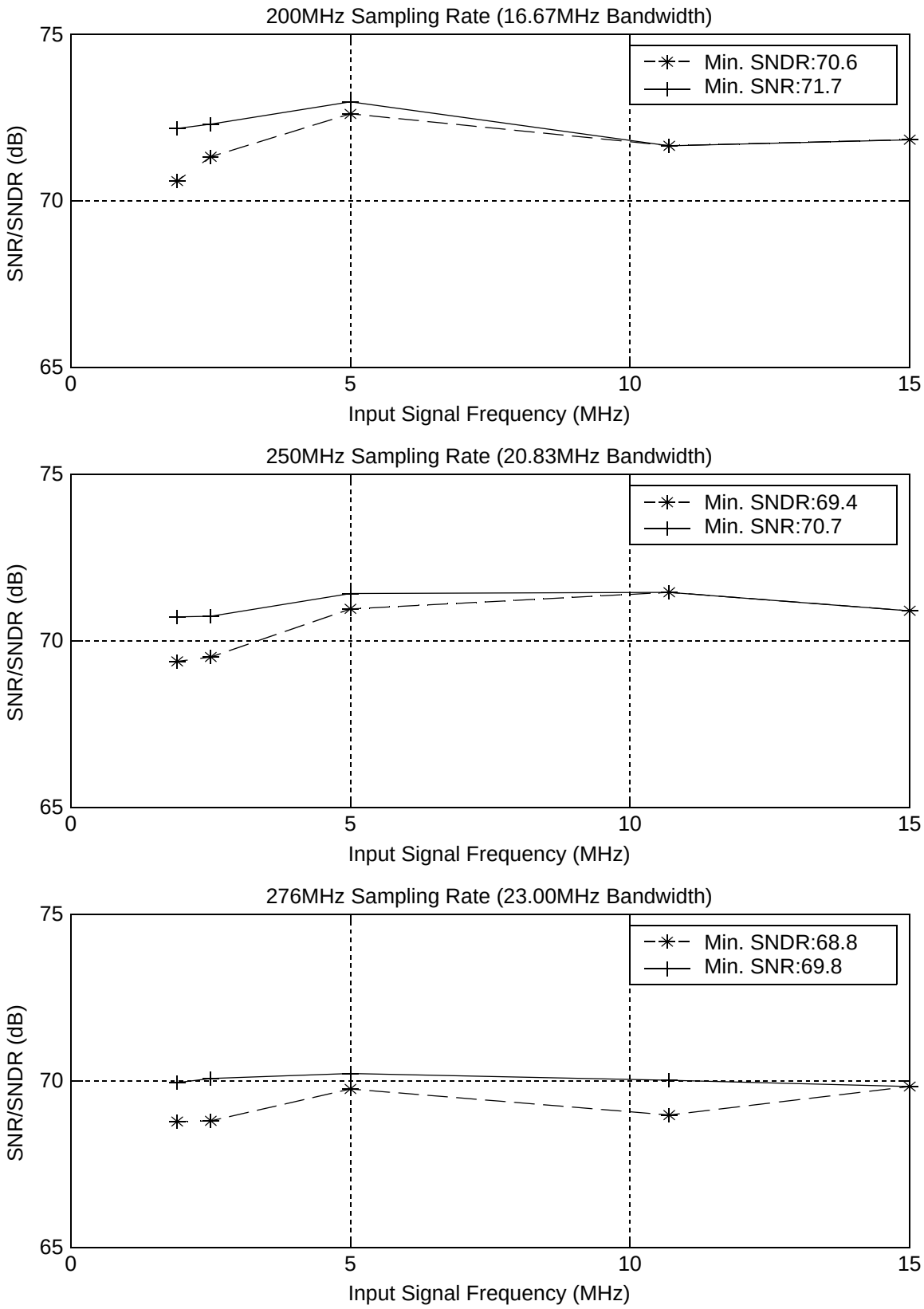

Fig. 6.7 Measured SNR/SNDR vs. input signal frequency at different clock frequency (DWA turned off).

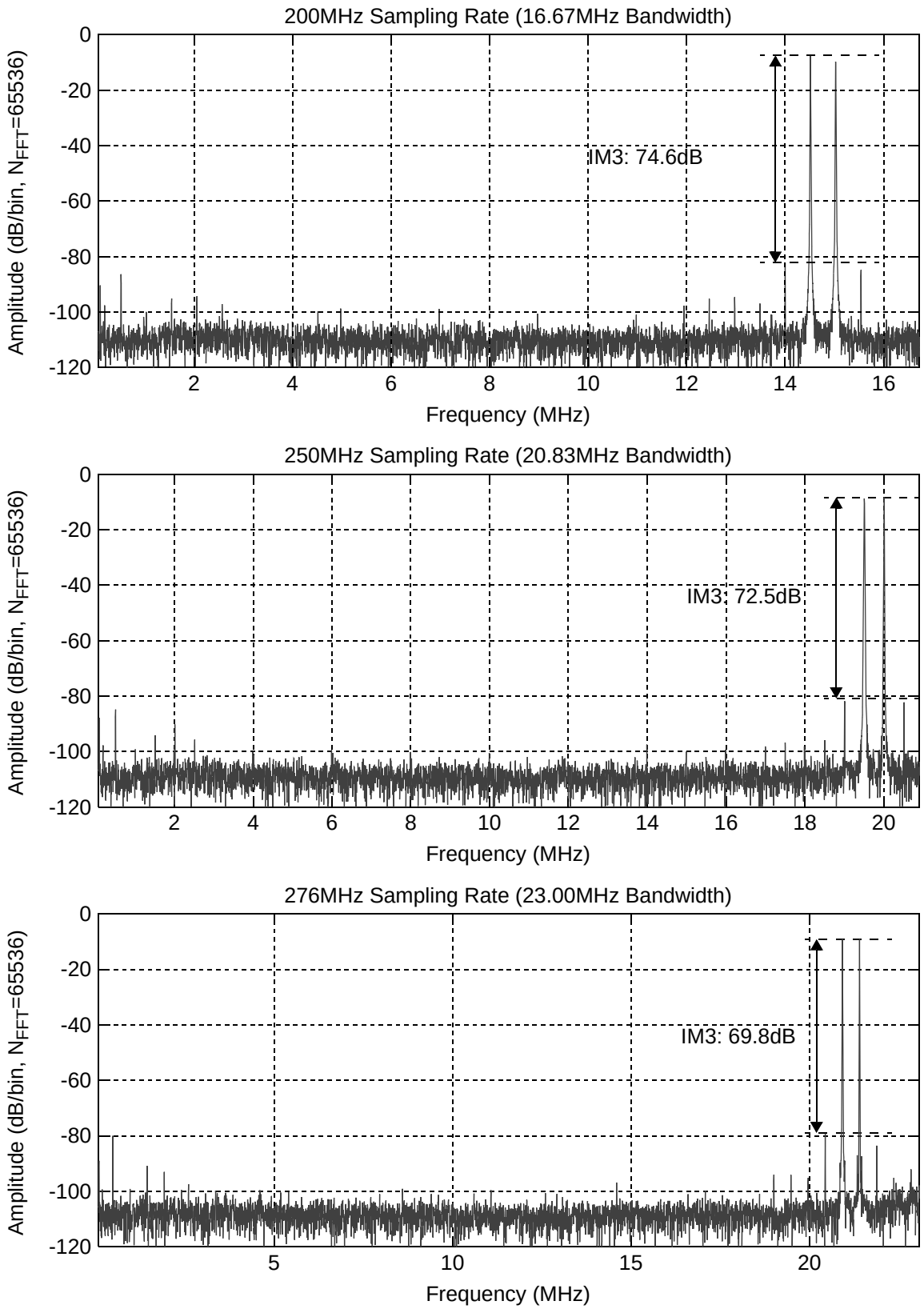

Fig. 6.8 Output spectra of two-tone intermodulation distortion test. Peak-to-peak signal amplitude is same as the signal amplitude which produces peak SNDR with a single tone at 5.0MHz (DWA turned off).

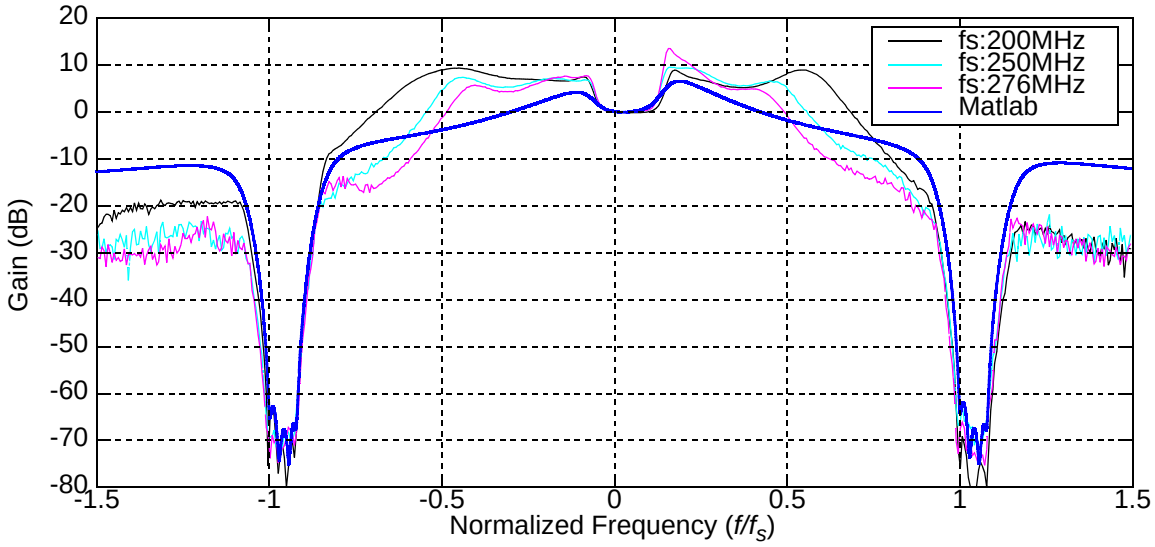

Fig. 6.9 Measured signal transfer function at various clock frequencies. DWA turned off.

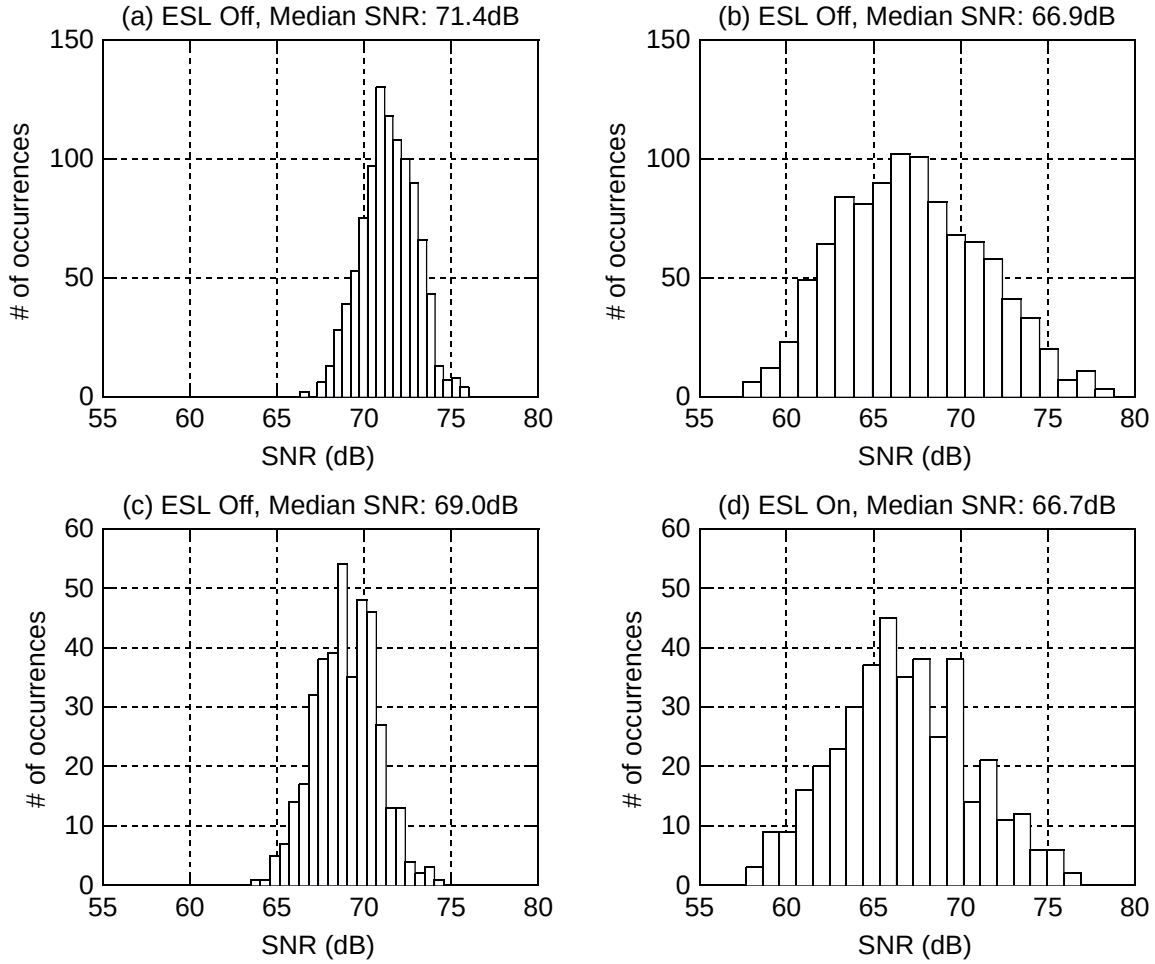

Fig. 6.10 Matlab Monte-Carlo simulations of the modulator with 15ps of random DAC rise/fall time mismatch with (a) Dynamic mismatch only and DWA turned off, (b) Dynamic mismatch only and DWA turned on, (c) Dynamic and static DAC mismatch, coefficient mismatch, 3ps of clock jitter with the DWA turned off, (d) Dynamic and static DAC mismatch, coefficient mismatch, 3ps of clock jitter with the DWA turned on

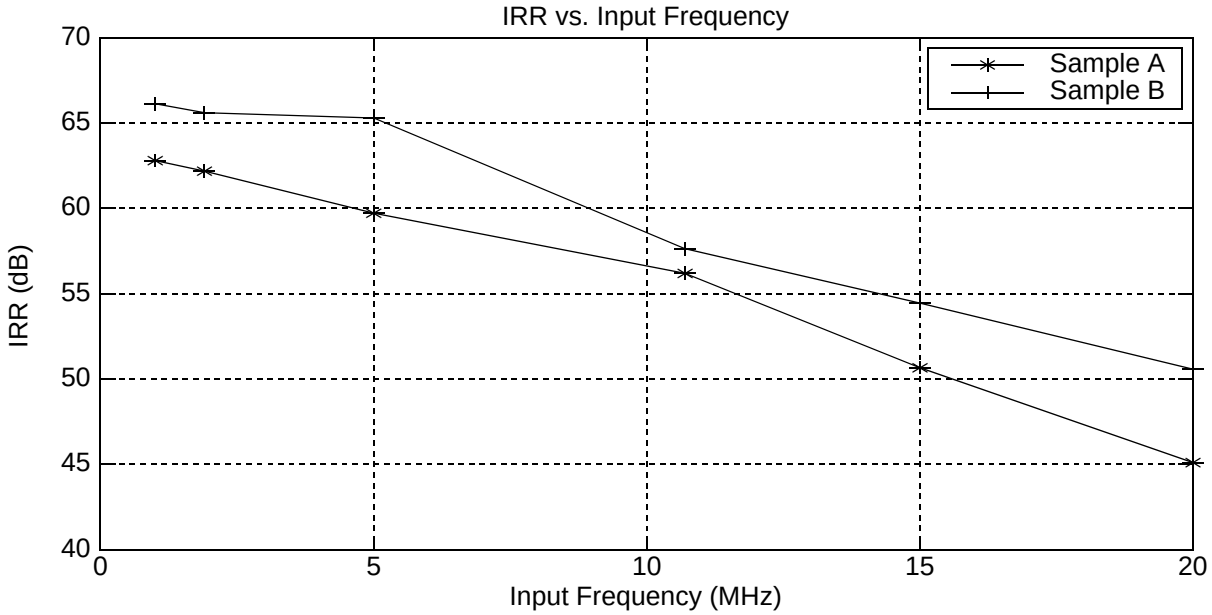

Fig. 6.11 Measured image rejection vs. input frequency at fs=250MHz for two different samples.

Technology	0.18μm 1P6M CMOS		
Architecture	4th Order Continuous-Time Bandpass Complex ΔΣ		
Sampling Frequency	276MHz	250MHz	200MHz
Signal Bandwidth	23.0MHz	20.8MHz	16.7MHz
IF	11.5MHz	10.4MHz	8.3MHz
Maximum Stable Input Voltage	$550mV_{rms}$ (differential)		
Dynamic Range	72.5dB	73.5dB	75.4dB
Peak SNDR (worst input frequency)	68.8dB	69.4dB	70.6dB
Peak SNR (worst input frequency)	69.9dB	70.7dB	71.3dB
Image Rejection		>45dB	
Alias Attenuation	>66dB	>68dB	>62B
Power Supply Voltage	1.8V		
Power Dissipation	42.6mW	42.3mW	41.3mW
Chip Core Area	$0.95mm^2$		

Table 6.1: Summary of IC performance.

6.4 Comparison of This Work with other State-of-the-Art ΔΣ ADC designs

Table 6.2 compares the achieved specifications of this modulator with previously published state-of-the-art ΔΣ ADC designs. In terms of signal bandwidth, this ADC has one of the highest reported signal bandwidth in a CMOS only process.

Figure of merit (FOM) is a commonly used method to evaluate the performance of different ADCs taking in to account power consumption, bandwidth and achieved resolution. The most commonly used FOM for ADC designs is

$$FOM1 = \frac{POWER}{2^{ENOB} \times 2BW} \qquad (6.1)$$

This figure of merit was originally developed to evaluate the performance of flash converters, hence for every extra bit of resolution, power can be doubled. FOM1 makes sense for a flash convertor since a 1-bit increase in resolution doubles the number of comparators in this type of architecture, hence doubling of the power consumption. However for higher resolution ADCs, where the ADC is limited more by thermal noise, every extra bit of resolution requires the sampling capacitor size to be increased by a factor of four (noise power is proportional to $\frac{KT}{C}$), hence the power consumption has to be increased by a factor of four. For these types of ADCs a figure of merit equation that makes more sense is one where 2^{ENOB} term is squared. To take this fact in to account a second FOM can be used

$$FOM2 = DR - 10\log 10\left(\frac{POWER}{BW}\right) \text{ where DR is dynamic range} \qquad (6.2)$$

Note for FOM1, a lower number is better, whereas for FOM2 a higher number is better. Based on the summary provided in Table 6.2 and using either FOM equation, this ADC's FOM is comparable to previously published work and it achieves one of the highest signal bandwidth for a ΔΣ ADC.

Reference	Power (mW)	SNDR/ [SNR] (dB)	Dynamic Range (dB)	2*BW (MHz)	FOM1 (pJ/Conv. Step)	FOM2 (dB)
This Work	42.6	68.8	72.5	46	0.41	160
[26]	70	63.7	67	30	1.87	150
[27]	122	63	67	20	5.28	146
[28]	200	72	84	25	2.46	162

Table 6.2: Comparison of this design and some previously published work.

Reference	Power (mW)	SNDR/ [SNR] (dB)	Dynamic Range (dB)	2*BW (MHz)	FOM1 (pJ/Conv. Step)	FOM2 (dB)
[29]	6	[77.3]	77.3	2	0.52	160
[30]	1.5	50.9		3.84	1.36	
[31]	15	76	82	2.2	1.32	161
[32]	2	59	89	2	1.37	176
[33]	149	81.6	83	4	3.8	154
[34]	62	83	88	2.2	2.44	160
[35]	4.5	72	74	3.84	0.36	160
[36]	180	88	90	2.2	3.98	158
[37]	2.2	[64]	68	2	0.85	155
[12]	4.4	75.5	76	2	0.45	160
[38]	87.5	50	53	40	8.47	136
[39]	24	79	86	2	0.82	162
[40]	150	87	95	4	2.05	166

Table 6.2: Comparison of this design and some previously published work.

6.5 Summary

This chapter described the PCB and the test setup used to characterize the ADC designed in the previous chapter. Measurement results were presented and the performance of the ADC was compared with previously published ΔΣ ADC designs. The modulator achieved a peak SNDR of 68.8dB at a signal bandwidth of 23MHz using only 42.6mW. The ADC achieved a FoM of 0.41pJ/Conv. step. The overall measured performance of the modulator for the given signal bandwidth and power was shown to be be comparable with current state-of-the-art ADC designs in standard CMOS process.

CHAPTER 7 *Conclusions and Future Work*

This chapter summarizes the thesis and offers possible areas of research which can potentially be used to further improve the performance of the modulator.

7.1 Thesis Summary

An overview of Nyquist and oversampling converters was given in chapter 2. A brief background on low-pass modulator theory was also presented in chapter 2. A description of complex signals and complex filters was followed by a description of quadrature bandpass ΔΣ ADCs. The desired modulator specifications were described in chapter 3 and two different modulator topologies were examined. Chapter 4 used system level simulations to quantify the amount of tolerable component imperfection and circuit specifications were found. Chapter 5 presented the design of the modulator and it was implemented in TSMC's 0.18μm CMOS process. Transistor level simulations of the circuits were used to verify functionality of the modulator. Measured results and comparison with previous works were presented in chapter 6. The IC was shown to achieve a peak SNDR of 68.8dB at a signal bandwidth of 23MHz using 42.6mW from a 1.8V supply. The measured results demonstrates that it is possible to achieve a low power consumption and wide bandwidth using a single loop quadrature ΔΣ ADC.

7.2 Suggestions for Future Work

In this thesis, a high resolution wide bandwidth complex bandpass ΔΣ ADC was fabricated in a standard 0.18μm CMOS only process. However, there are still more issues that need to be resolved. To make a fair comparison of the power consumption of this modulator with that of a Nyquist rate converters such as pipeline ADCs, requires an estimate of the decimation filter's power consumption. Future work is also needed to investigate the possibility of using a DAC shuffling

algorithms which take in to account NRZ DAC's rise/fall mismatch. One such algorithm is described in [11]. In this scheme, the element selection logic block tries to keep the number of switching activities constant at every clock period, hence dynamic errors will appear at harmonics of the clock frequency and will be out of the band of interest. Another possibility is to use a constant switching DAC scheme such as the one described in [41], [24]. Two additional switches are used to ensure that there is constant switching activity regardless of input code. Again, constant DAC switching activity ensures that dynamic errors due to rise/fall time asymmetry are repeated every clock cycle and hence the distortions will not fall in the band of interest. Improving the first feedback DAC's dynamic performance will be critical to achieving higher SNDR performance at high input frequencies.

APPENDIX A

NTF and STF Derivation

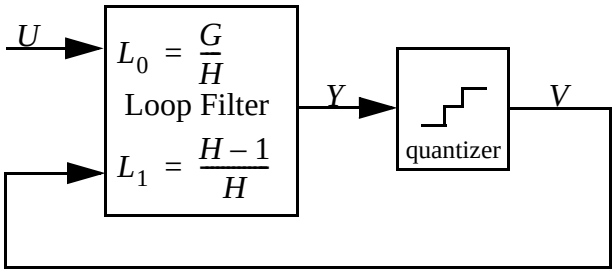

Fig. A.1 A general block diagram of a ΔΣ modulator.

This appendix summarizes the equations that were used to derive the signal and noise transfer functions of modulators described in this thesis. A block diagram of general delta-sigma modulator is shown in Fig. A.1 Note that *U, V, Y, L_0, L_1* and the quantizer are complex objects. The loop transfer function is described by a 2-by-2 matrix that describes the input-output relationship between the real and imaginary channel. note that $\underline{L}_0$ is a continuous-time TF and $\underline{L}_1$ is a discrete-time TF. A_{re1}, A_{re2}, B_{re1},... are real transfer functions. The transformation from continuous-time TF to discrete-time TF were performed using the method described in [8].

$$\underline{L}_0 = \begin{bmatrix} B_{re1}(s) & -B_{im2}(s) \\ B_{im1}(s) & B_{re2}(s) \end{bmatrix} \text{ and } \underline{L}_1 = \begin{bmatrix} A_{re1}(z) & -A_{im2}(z) \\ A_{im1}(z) & A_{re2}(z) \end{bmatrix} \text{ where } z = e^s$$

Replacing the quantizer by a random noise source and solving for V

$$\underline{V} = \underline{L}_0\underline{U} + \underline{L}_1\underline{V} + \underline{E}$$

$$\begin{bmatrix} V_{re} \\ V_{im} \end{bmatrix} = \begin{bmatrix} B_{re1} & -B_{im2} \\ B_{im1} & B_{re2} \end{bmatrix}\begin{bmatrix} U_{re} \\ U_{im} \end{bmatrix} + \begin{bmatrix} A_{re1} & -A_{im2} \\ A_{im1} & A_{re2} \end{bmatrix}\begin{bmatrix} V_{re} \\ V_{im} \end{bmatrix} + \begin{bmatrix} E_{re} \\ E_{im} \end{bmatrix}$$

$$= \begin{bmatrix} 1-A_{re1} & A_{im2} \\ -A_{im1} & 1-A_{re2} \end{bmatrix}^{-1}\left\{\begin{bmatrix} B_{re1} & -B_{im2} \\ B_{im1} & B_{re2} \end{bmatrix}\begin{bmatrix} U_{re} \\ U_{im} \end{bmatrix} + \begin{bmatrix} E_{re} \\ E_{im} \end{bmatrix}\right\}$$

$$= \frac{1}{(1-A_{re1})(1-A_{re2}) + A_{im1}A_{im2}}\begin{bmatrix} 1-A_{re2} & -A_{im2} \\ A_{im1} & 1-A_{re1} \end{bmatrix}\left\{\begin{bmatrix} B_{re1} & -B_{im2} \\ B_{im1} & B_{re2} \end{bmatrix}\begin{bmatrix} U_{re} \\ U_{im} \end{bmatrix} + \begin{bmatrix} E_{re} \\ E_{im} \end{bmatrix}\right\}$$

$$= \frac{1}{(1-A_{re1})(1-A_{re2})+A_{im1}A_{im2}}\begin{bmatrix}(1-A_{re2})B_{re1}-A_{im2}B_{im1} & -\{(1-A_{re2})B_{im2}+A_{im2}B_{re2}\}\\ (1-A_{re1})B_{im1}+A_{im1}B_{re1} & (1-A_{re1})B_{re2}-A_{im1}B_{im2}\end{bmatrix}\begin{bmatrix}U_{re}\\ U_{im}\end{bmatrix} +$$

$$\frac{1}{(1-A_{re1})(1-A_{re2})+A_{im1}A_{im2}}\begin{bmatrix}1-A_{re2} & -A_{im2}\\ A_{im1} & 1-A_{re1}\end{bmatrix}\begin{bmatrix}E_{re}\\ E_{im}\end{bmatrix}$$

NTF and STF are given by the following equations:

$$H = \frac{1}{2}\frac{\{2-(A_{re1}+A_{re2})\}+j\{A_{im1}+A_{im2}\}}{(1-A_{re1})(1-A_{re2})+A_{im1}A_{im2}}$$

$$H_{img} = \frac{1}{2}\frac{\{A_{re1}-A_{re2}\}+j\{A_{im1}-A_{im2}\}}{(1-A_{re1})(1-A_{re2})+A_{im1}A_{im}}$$

$$G = \frac{1}{2}\frac{\{(1-A_{re2})B_{re1}-A_{im2}B_{im1}+(1-A_{re1})B_{re2}-A_{im1}B_{im2}\}+j\{(1-A_{re2})B_{im2}+A_{im2}B_{re2}+(1-A_{re1})B_{im1}+A_{im1}B_{re1}\}}{(1-A_{re1})(1-A_{re2})+A_{im1}A_{im2}}$$

$$G_{img} = \frac{1}{2}\frac{\{(1-A_{re2})B_{re1}-A_{im2}B_{im1}-((1-A_{re1})B_{re2}-A_{im1}B_{im2})\}+j\{(1-A_{re2})B_{im2}+A_{im2}B_{re2}-((1-A_{re1})B_{im1}+A_{im1}B_{re1})\}}{(1-A_{re1})(1-A_{re2})+A_{im1}A_{im2}}$$

If the real and imaginary signal paths are identical (i.e. $A_{re} = A_{re1} = A_{re2}$ and $A_{im} = A_{im1} = A_{im2}$ and etc....) then

$$H = \frac{1}{1-(A_{re}+jA_{im})} = \frac{1}{1-L_1} = \frac{1}{1-(H-1)/H} = H$$

$$H_{img} = 0$$

$$G = \frac{B_{re}+jB_{im}}{1-(A_{re}+jA_{im})} = \frac{L_0}{1-L_1} = \frac{G/H}{1-(H-1)/H} = G$$

$$G_{img} = 0$$

APPENDIX B *Impulse Matching*

One way of ensuring that a loop filter will implement a desired NTF is to guarantee that the open loop (feedback loop broken at the quantizer) impulse response from v to y (i.e impulse response of L_1 TF, see Fig. A.1) is the same as the impulse response of $\frac{H-1}{H}$, where H is desired NTF. To implement an arbitrary NTF, design parameters may be adjusted such that the two impulse responses are equal. This method can be generalized to a continuous-time modulator by "matching" the pulse response of L_{1c} TF with the $\frac{H-1}{H}$ impulse response. The design parameters a_i are then adjusted such that at each sampling instance the continuous-time output $y(nT_s)$ is equal to the desired impulse response at that time.

To find a "good match" between the two responses the following system of equations can solved for the matrix A:

$$\underline{B} = \underline{X}\underline{A} \tag{B.1}$$

$\underline{B} = \left[y(0)\ y(1)\ \ldots\ y(N)\right]$ where $y(i)$ is the i^{th} sample of the impulse response of the desired NTF.

$\underline{X_j} = \left[y_j(0)\ y_j(1)\ \ldots\ y_j(N)\right]$ $y_j(i)$ is the i^{th} sample of the pulse response of the continuous-time system with only j^{th} DAC turned on and $\underline{X} = \left[\underline{X_1}\ \underline{X_2}\ \ldots\ \underline{X_n}\right]^T$

$\underline{A} = \left[a_1\ a_2\ \ldots\ a_n\right]$ where a_i is the i^{th} feedback DAC coefficient.

$(\underline{B} = \underline{X}\underline{A}) \Rightarrow \underline{A} = \underline{B}/\underline{X}$

$\underline{A}$ is the solution in the least squares sense to the system of equations. i.e

$$\sum_{i=0}^{N}\left(y(i)-\left(\sum_{j=1}^{n}a_j y_j(i)\right)\right)^2 \tag{B.2}$$

is a minimum. Therefore the columns of $\underline{A}$ correspond to DAC feedback coefficients such that the impulse response of the NTF and the pulse response of the system are a "good match" to each other. The above procedure ensures that the NTF of the continuous-time system is same as the prototype.

APPENDIX C

Sensitivity Calculation

The following plots were obtained by calculating the relevant measure of merit (such as in-band NTF gain) with respect to small shifts in a single modulator parameter. In case of symmetrical errors, the same amount of parameter variation was applied to the real channel and imaginary channel. Note that this kind of error does not give rise to either an INTF or ISTF. For asymmetrical errors, the parameter variation was applied only to the real channel. Note, in the context of this thesis, symmetrical change means that the variations effect the real and imaginary path equally. asymmetrical variations are those that effect only a single channel.

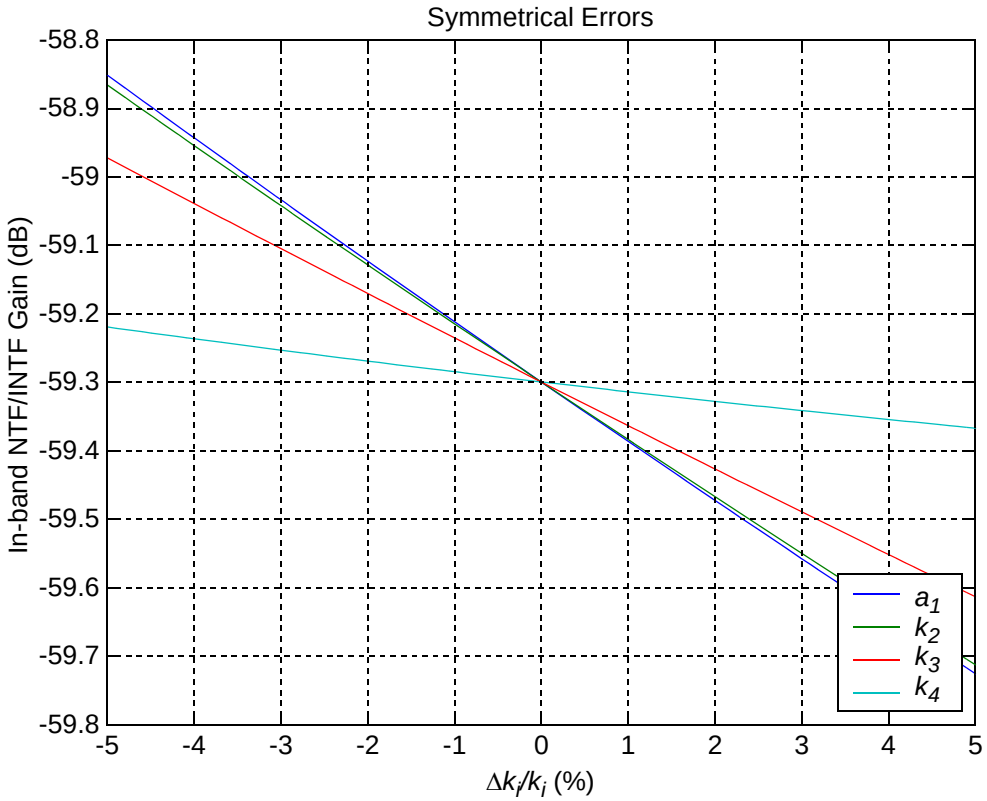

Fig. C.1 Variation of in-band NTF gain due to symmetrical shifts in inter-stage gain coefficients.

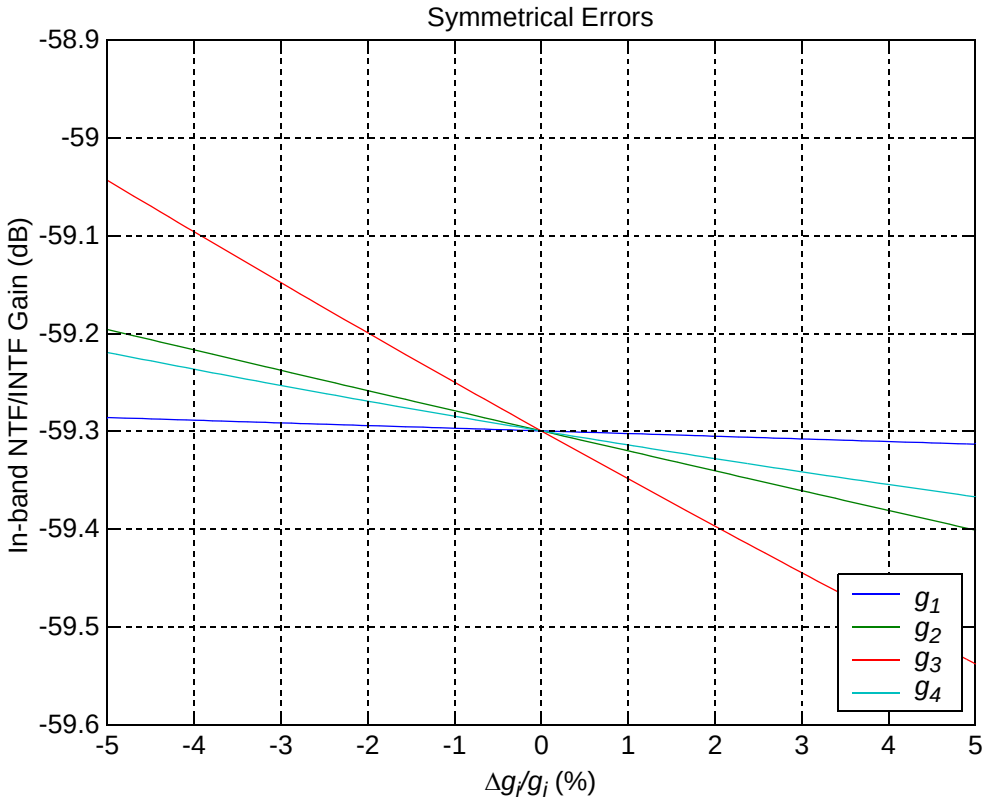

Fig. C.2 Variation of in-band NTF gain due to symmetrical shifts in feedforward gain coefficients.

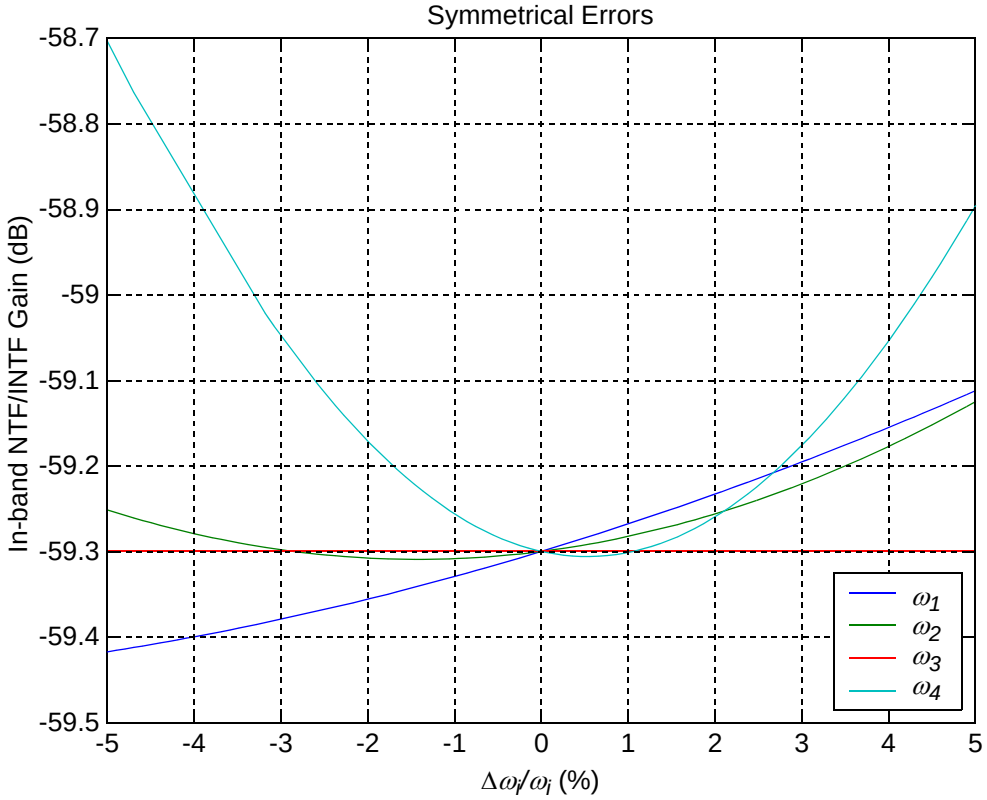

Fig. C.3 Variation of in-band NTF gain due to symmetrical shifts in NTF zeros.

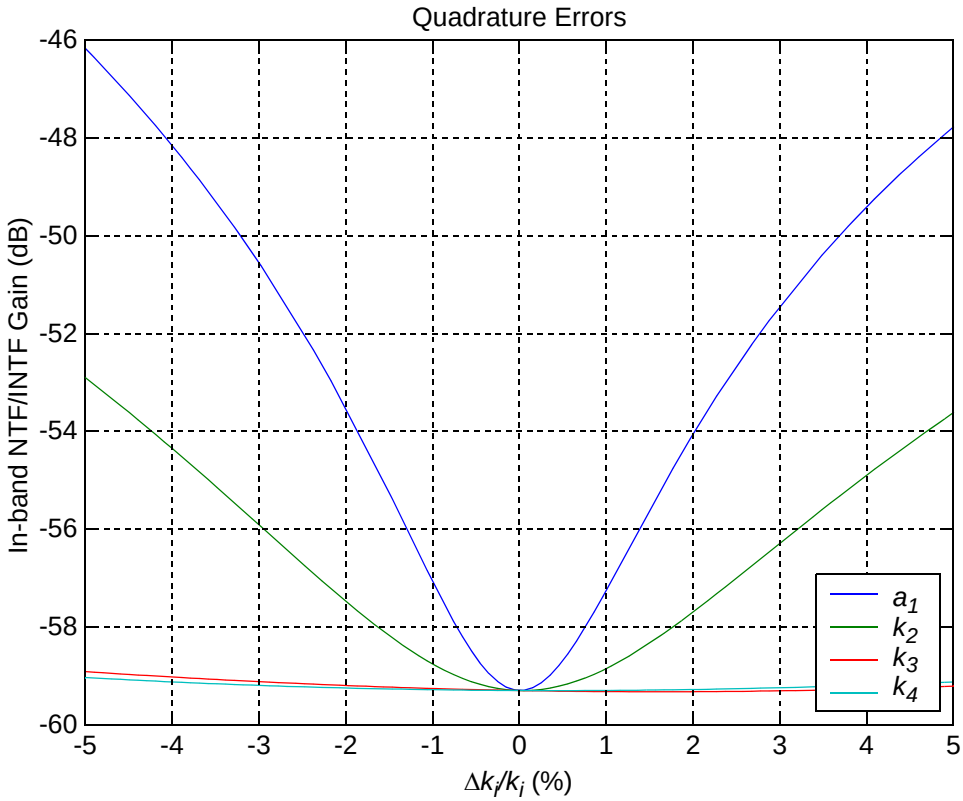

Fig. C.4 Variation of in-band NTF gain due to asymmetrical shifts in inter-stage gain coefficients.

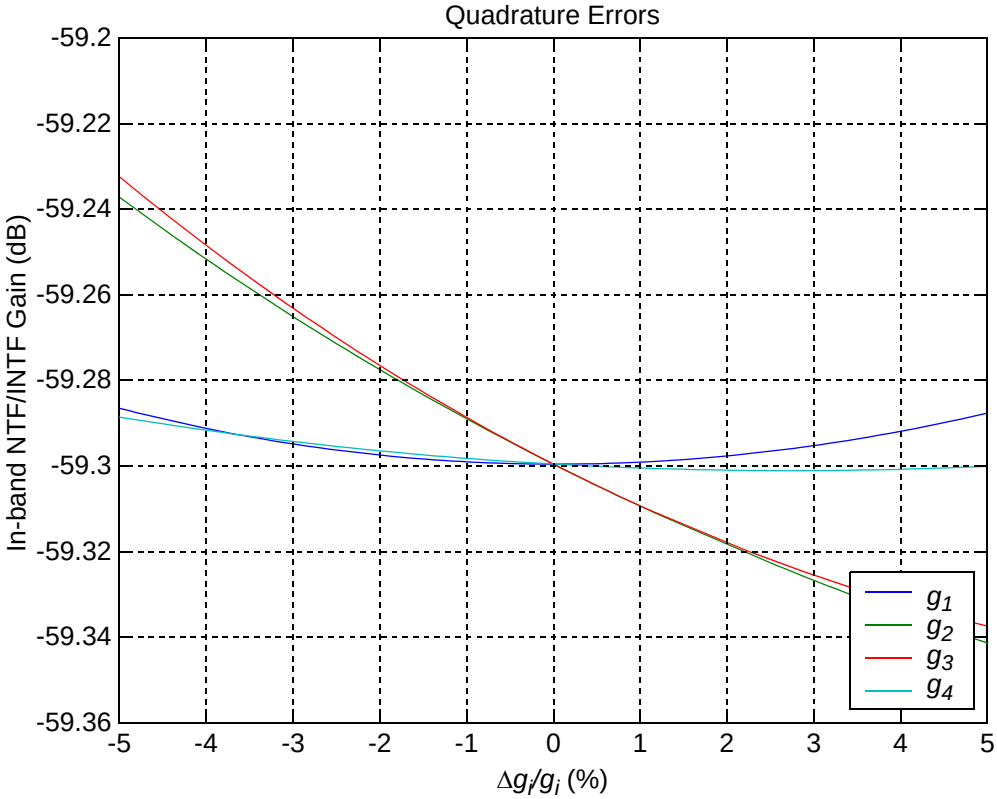

Fig. C.5 Variation of in-band NTF gain due to asymmetrical shifts in feedforward gain coefficients.

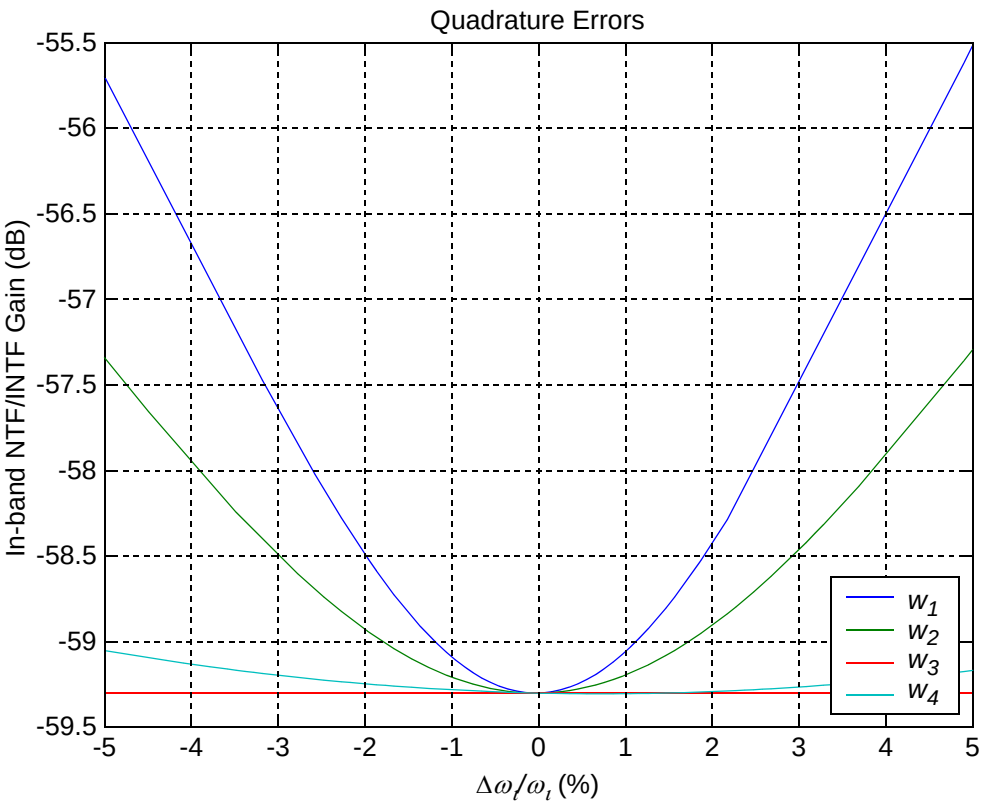

Fig. C.6 Variation of in-band NTF gain due to asymmetrical shifts in NTF zeros.

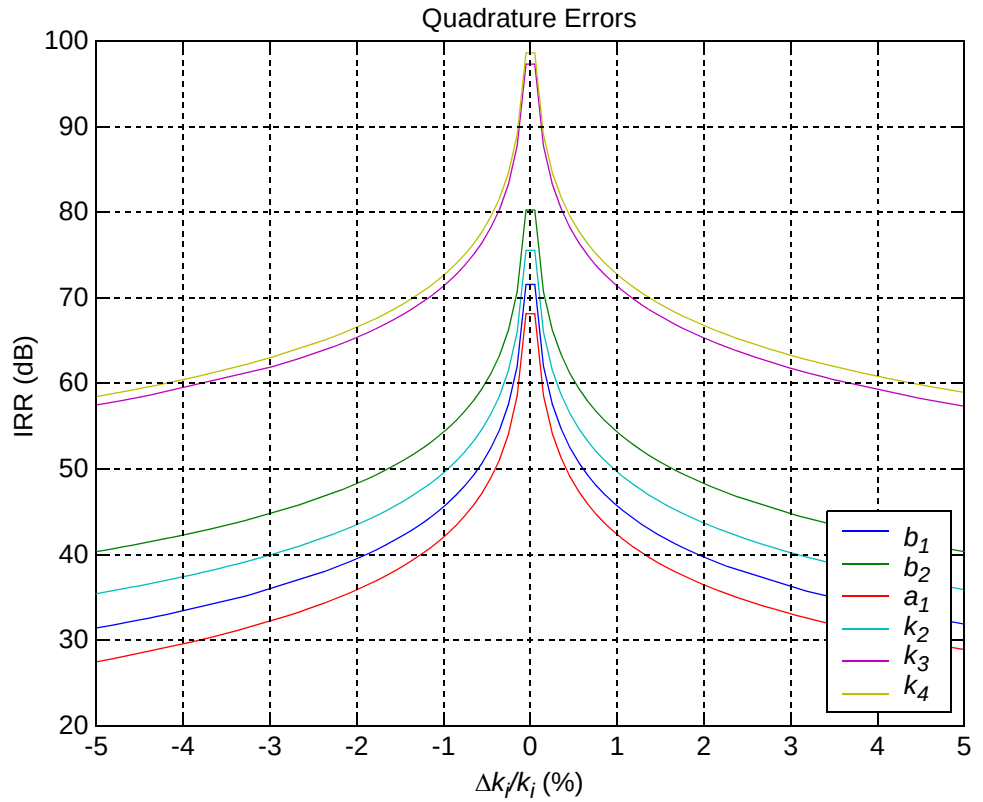

Fig. C.7 Variation of IRR due to changes in inter-stage gain and input coefficients.

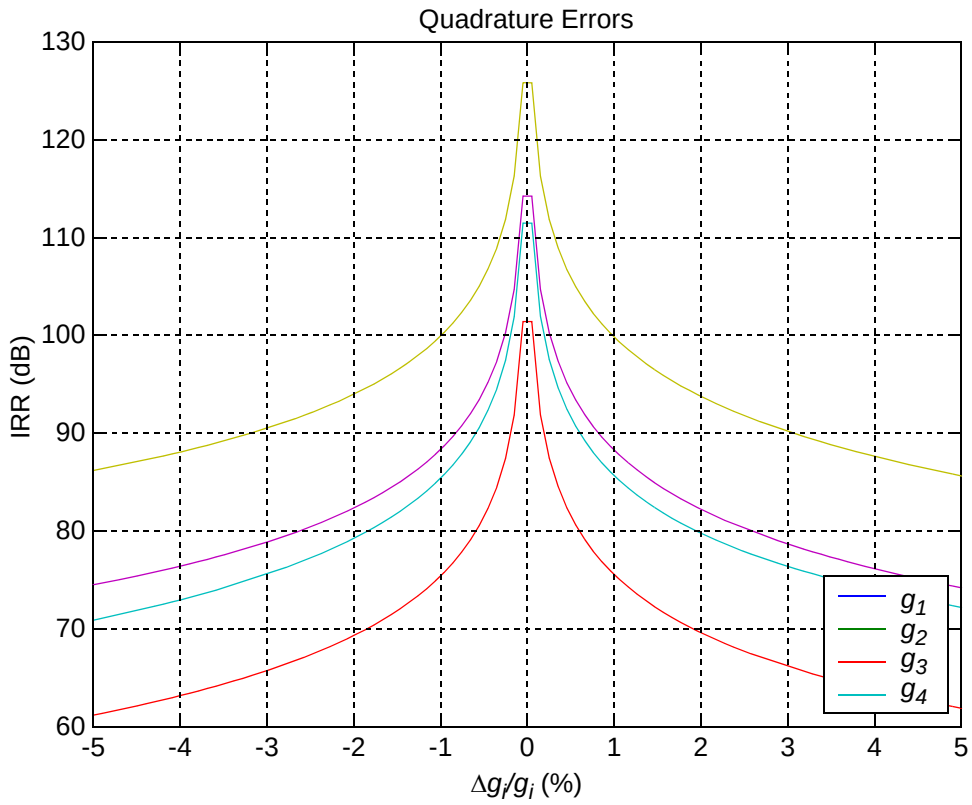

Fig. C.8 Variation of IRR due to change in feedforward gain coefficients.

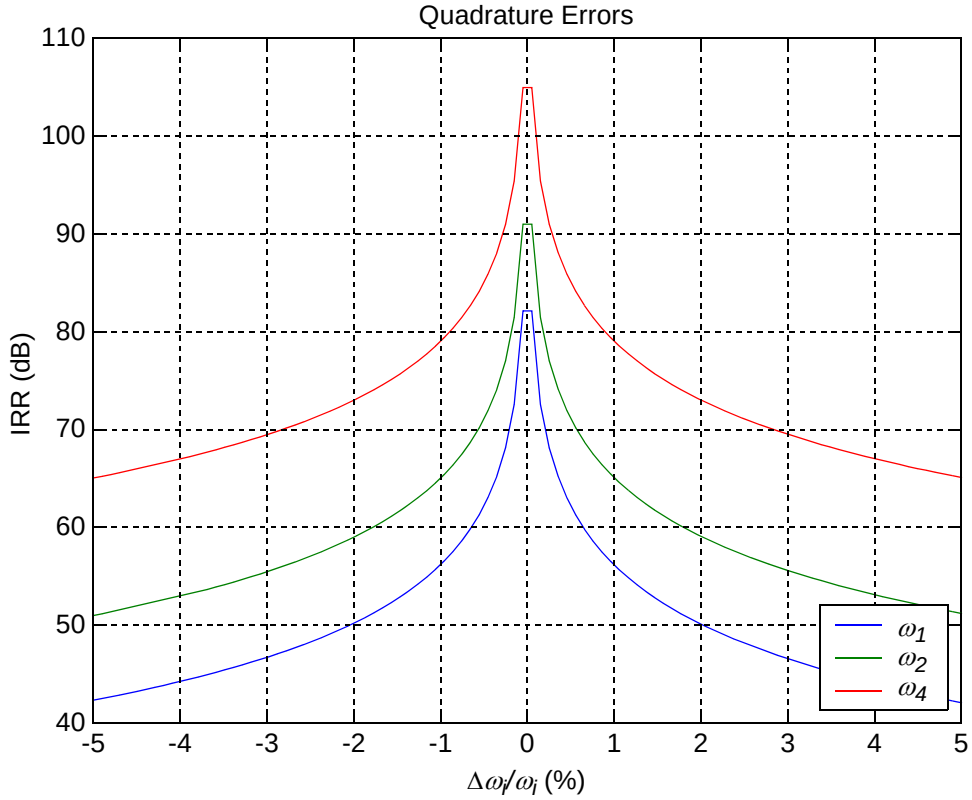

Fig. C.9 Variation of IRR due to change in NTF zeros.

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