ARCHITECTURE ALTERNATIVES FOR TIME-INTERLEAVED AND INPUT-FEEDFORWARD DELTA-SIGMA MODULATORS

by

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Abstract

This thesis provides architecture alternatives for delta-sigma modulators in two areas: high-speed operation based on time-interleaving and low-voltage environment by exploiting the input-feedforward concept.

Parallelism based on time-interleaving can be used to increase the speed of delta-sigma modulators. A novel single-path time-interleaved architecture is derived and analyzed. Finite opamp gain and bandwidth result in a mismatch between the noise transfer functions of the internal quantizers which degrades the performance of the new modulator. Two techniques are presented to mitigate the mismatch problem: a hybrid topology where the first stage uses multiple integrators while the rest of the modulator uses a single path of integrators and a digital calibration method.

The input-feedforward technique removes the input-signal component from the internal nodes of delta-sigma modulators. The removal of the signal component reduces the signal swing and distortion requirements for the opamps. These characteristics enable the reliable implementation of delta-sigma modulators in modern CMOS technology. Two implementation issues for modulators with input-feedforward are considered. First, the drawback of the analog adder at the quantizer input is identified and the capacitive input feedforward technique is

introduced to eliminate the adder. Second, the double sampled input technique is proposed to remove the critical path generate by the input feedforward path.

Novel input-feedforward delta-sigma architecture is proposed. The new digital input feedforward (DIFF) modulator maintains the low swing and low distortion requirements of the input feedforward technique, it eliminates the analog adder at the quantizer input, and it improves the achievable resolution. To demonstrate these advantages, a configurable delta-sigma modulator which can operate as a feedback topology or in DIFF mode is implemented in 0.18μm CMOS technology. Both modulators operate at 20MHz clock with an oversampling ratio of 8. The power consumption in the DIFF mode is 22mW and in feedback mode is 19mW. However, the DIFF mode achieves a peak SNDR of 73.7dB (77.1dB peak SNR) while the feedback mode achieves a peak SNDR of 64.3dB (65.9dB peak SNR). Therefore, the energy required per conversion step for the DIFF architecture (2.2 pJ/step) is less than half of that required by the feedback architecture (5.7 pJ/step).

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ADC ..... Analog-to-Digital Converter
CDM..... Code Division Multiplexing
CIFB ..... Cascade of Integrators with distributed FeedBack
CIFB-CIF..... CIFB with Capacitive Input-Feedforward
CIFB-IF ..... CIFB with Input-Feedforward
CIFF ..... Cascade of Integrators with weighted FeedForward summation
CIFF-CIF ..... CIFF with Capacitive Input-Feedforward
CIFF-IF..... CIFF with Input-Feedforward
CMC ..... Canadian Microelectronics Corporation
CQFP..... Ceramic Quad Flat Pack
DAC ..... Digital-to-Analog Converter
dBFS..... DeciBel with respect to Full-Scale
DDA ..... Differential Difference Amplifier
DEM ..... Dynamic Element Matching
DIFF ..... Digital Input-FeedForward
DSP..... Digital Signal Processing
DUT..... Device Under Test
DWA ..... Data Weighted Averaging
FDM ..... Frequency Division Multiplexing
FOM ..... Figure of Merit
LSB..... Least Significant Bit
LTI..... Linear Time Invariant
MASH ..... Multi-stAge noise SHaping
MIM ..... Metal-Insulator-Metal
MPSPTI ..... mixed Multi-Path Single-Path Time-Interleaved
MPTI ..... Multi-Path Time-Interleaved
NTF ..... Noise Transfer Function

PCB ..... Printed Circuit Board

SISO ..... Single Input Single Output

SNDR ..... Signal to Noise plus Distortion Ratio

SNR ..... Signal to Noise Ratio

SPMPTI ..... mixed Single-Path Multi-Path Time-Interleaved

SPTI..... Single-Path Time-Interleaved

SQNR ..... Signal to Quantization Noise Ratio

STF ..... Signal Transfer Function

TDM ..... Time Division Multiplexing

TI ..... Time-Interleaving

ZITI ..... Zero-Insertion Time-Interleaved

Chapter 1:

Introduction

1.1 Motivation

THE phenomenal advances in CMOS integrated circuit technology coupled with the development of sophisticated *digital signal processing* (DSP) algorithms have shifted more of the signal processing from the analog to the digital domain, and have fueled the development of a wide range of new applications. In many applications, digital circuits still need to communicate with the real world, which is inherently analog. Therefore, the links between the analog and digital domains are of great importance. The analog information coming from the real world is filtered and converted into digital bits by an *analog-to-digital converter* (ADC). The data processed in the digital domain is fed back to the analog world using a *digital-to-analog converter* (DAC) and an analog post filter.

The technological advances in CMOS allow digital circuits to run faster and to consume less power. Also, the increase in integration allows an entire system to be fabricated on a single chip. Therefore, digital circuits are benefiting tremendously from advances in CMOS technology. Conversely, these advances make it more difficult to design analog circuits due to diminishing voltage supplies and smaller transistor intrinsic gain; moreover, many of the new DSP algorithms have placed more stringent requirements on the analog-digital interface. Therefore, the interface between the digital world and the analog world is becoming the bottleneck in the achievable performance of modern systems.

In this thesis, a specific part of the analog-digital interface is investigated, namely the ADC. Although there are a number of methods to design an ADC, delta-sigma ($\Delta\Sigma$) converters have many advantages that make them great candidates for such environments. Their tolerance to component mismatches and circuit non-idealities relaxes the requirements placed on the analog building blocks. Furthermore, they simplify the anti-aliasing filter design requirements by potentially moving most of the filtering operations into the digital domain. Therefore, $\Delta\Sigma$ modulators are widely used for high-resolution and low-bandwidth analog-to-digital converters.

Their dominance in such applications stems from the inherent trade-off in the way they operate. They sample the input-signal at a rate much higher than the Nyquist rate. Then, they process the high-speed low-resolution digital signal to generate a high-resolution low-speed representation of the analog input. The intensive digital post-processing makes CMOS a great technology for implementing ΔΣ converters, however, the low voltage environment of modern CMOS makes the design of the analog part more challenging.

The challenge today is to develop new architectures and circuits for implementing the ADCs under the increasing technological difficulties and rising demands from DSP algorithms. Specifically, increasing the speed of ΔΣ modulators and enabling the reliable operation in low-voltage environments are investigated.

Parallelism can be exploited as a method to increase the speed of ΔΣ modulators. Parallelism by time-interleaving, based on the block filtering theory, is a candidate to achieve higher speeds [1]. In this thesis, new time-interleaved topologies are introduced and evaluated.

The idea of controlling the internal states of ΔΣ modulators to reduce the signal swing and linearity requirements is a significant development [2]. It makes the design of ΔΣ based ADCs in low-voltage environments reliable, and sets it farther apart from other ADC techniques. Therefore, the state control achieved by the input-feedforward is investigated thoroughly. Furthermore, the capacitive-input feedforward and the double sampled input are proposed to simplify input-feedforward modulators. Finally, a new input-feedforward technique is proposed and a prototype chip is implemented in CMOS technology.

1.2 Thesis Outline

This dissertation is organized in six chapters including this introduction. Chapter 2 provides a brief overview of ΔΣ modulators. It discuses the most common single-loop topologies and analyzes the tradeoffs involved in their design. Next, multi-stage noise shaping modulators are discussed. Finally, time-interleaved ΔΣ modulators are reviewed.

Chapter 3 introduces a new time-interleaved ΔΣ modulator topology. The proposed architecture requires a single modulator with extra quantizers and interconnects to achieve an arbitrary time-interleaving factor. Finite opamp gain and bandwidth result in a mismatch between the noise transfer functions of the internal quantizers which degrades the performance of the new modulator. Two techniques are presented to mitigate the mismatch problem. First, a hybrid topology where the first stage uses multiple integrators while the rest of the modulator uses a single path of integrators is presented. Second, a digital calibration method reduces the mismatch

and relaxes the requirements on the analog components. The issue of multi-bit digital-to-analog nonlinearity is discussed for the new topology and a method to minimize its effect is proposed.

Chapter 4 analyzes the input-feedforward modulator's advantages and complications. It introduces the double sampling input as a method of mitigating the timing constraint due to the critical path of the input-feedforward path. The capacitive-input-feedforward is introduced to eliminate the problematic adder at the quantizer input. Finally, a new digital input-feedforward ΔΣ modulator is proposed and evaluated in this chapter.

Chapter 5 discusses the design of a configurable ΔΣ modulator. The configurability allows the modulator to operate in the single-loop mode or in the digital input-feedforward mode. The implementation of the modulator in 0.18μm CMOS technology is discussed. Finally, the test chip and the test set-up are described and measured results are provided.

Chapter 6 summarizes the thesis, highlights its research contributions, and suggests areas of research for future exploration.

Chapter 2:

Fundamentals of ΔΣ Modulators

DELTA-SIGMA modulation is a popular method for achieving high-resolution data converters. Their popularity is due to the relaxed requirements they place on analog circuits. Furthermore, the evolution of new ΔΣ architectures reduces the analog complexity and makes their implementation in nano-scale CMOS technology feasible.

This chapter is not intended to be a comprehensive background to ΔΣ modulation, instead, it provides the important aspects necessary to understand the subsequent chapters. The technical literature contains a wealth of information on ΔΣ modulation, the most thorough and up to date is presented in [3].

The outline of this chapter is as follows: Section 2.1 reviews single-loop ΔΣ modulators. Section 2.2 provides an overview of the multistage noise shaping architectures. In Section 2.3, time-interleaving ΔΣ modulators are reviewed.

2.1 Single Loop ΔΣ Modulators

The architectural level development of ΔΣ modulators involves the design of three components: the *noise transfer function* (NTF), the *signal transfer function* (STF), and the internal states of the modulator.

Traditionally, designers concentrated on the design of the NTF because it determines the achievable *signal to quantization noise ratio* (SQNR). Topologies suitable for ADC applications which evolved from the early days can be classified in two categories based on their loop filter implementation: feedback ΔΣ modulators and feedforward ΔΣ modulators [4]. The feedback and feedforward topologies provide the designer with one degree of freedom. Therefore, the STF and the states are fixed by the choice of the NTF.

Recently, the input-feedforward concept is used to control the states of the modulator [2]. The input-feedforward path alleviated some of the drawbacks of the feedback and feedforward topologies, however, it has added a few complications. These issues are discussed later in this chapter.

In general, the design of the STF is not of significant concern as long as it does not degrade the modulator stability. In some circumstances however, the control of the STF could be of interest. For example, an ADC at a receiver input with large channel interference requires significant continuous-time analog filtering. This can be relaxed if the STF is designed to attenuate the out of band spectrum [5].

To keep the scope of the analysis focused; this discussion is limited to ΔΣ modulators with pure differentiator type NTFs that employ internal quantizers with a sufficient number of levels to keep the modulator stable for any NTF out of band gain. The relation of the topologies to their integrated circuit implementation is emphasized.

2.1.1 Feedback ΔΣ modulators

The simplest method to construct high order ΔΣ modulators is to cascade several integrators in the forward path, with each integrator receiving feedback from the quantizer to ensure stability. Such a structure is called the *cascade of integrators with distributed feedback* (CIFB). The CIFB topology is illustrated for a second-order modulator in Fig. 2.1.

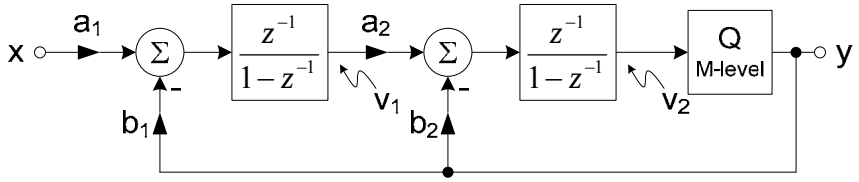

Fig. 2.1: Second-order CIFB modulator

Analysis of the linearized system with $a_1 = a_2 = b_1 = 1, b_2 = 2$ leads to the following results:

$$STF = \frac{y}{x} = z^{-2} \tag{2-1}$$

$$NTF = \frac{y}{q} = \left(1 - z^{-1}\right)^2 \tag{2-2}$$

$$v_1 = z^{-1}\left(1 + z^{-1}\right)x - z^{-1}\left(1 - z^{-1}\right)q \tag{2-3}$$

$$v_2 = z^{-2}x - z^{-1}\left(2 - z^{-1}\right)q \tag{2-4}$$

where q is the quantization noise from the internal quantizer, and v_1 and v_2 are the signals at the outputs of the first and second integrators, respectively. The STF exhibits an all-pass response and the NTF provides a second-order pure differentiator type high-pass response.

The main advantage of the CIFB topology is that it is easy to implement with low sensitivity to component variations. The main disadvantage of this topology is that the signals at the output of the integrators are a function of the input-signal as given in Eqs. (2-3) and (2-4), resulting in two effects. First, the signal swing at the output of the opamps is large which makes their implementation in the low-voltage, nano-scale CMOS technology difficult. Second, opamp nonlinearities generate distortion that is a function of the input-signal. The opamp distortion can severely limit the achievable SNDR. Another disadvantage of the CIFB topology is that the NTF, STF, and states cannot be set independently. Therefore, if we pick a certain NTF, then the STF and states are fixed.

The CIFB topology is simulated using Matlab and Simulink. The probability density function of integrator outputs and a sample output spectrum including opamp third-order distortion are shown in Fig. 2.2 for a sinusoidal input signal which parameters are specified in the figure. The third-order distortion is modelled as a power series with the third-order term corresponding to 1% third-order harmonic distortion for a full scale signal.

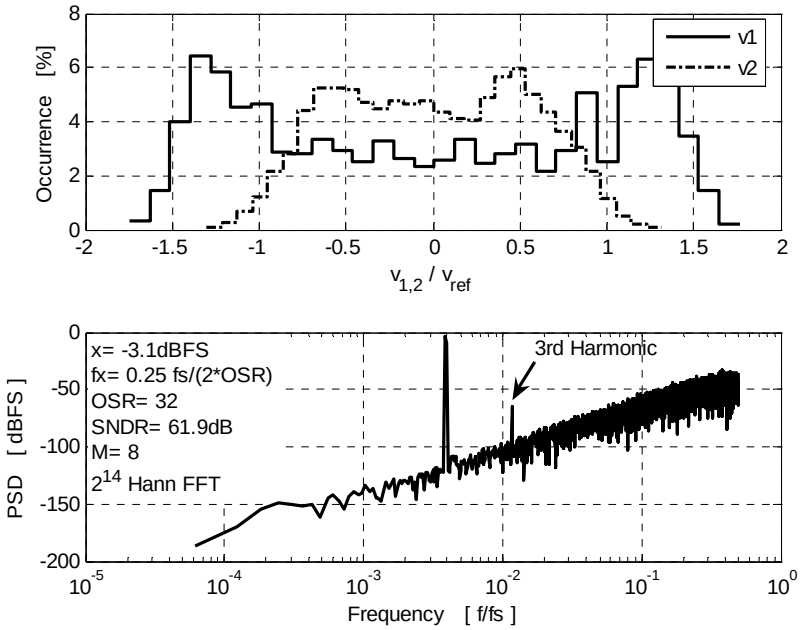

Fig. 2.2: Signal swing at Opamp outputs and sample output spectrum for CIFB

Simulations indicate that the signal swings at the internal nodes can be over 1.5 times larger than the internal quantizer reference voltage. On the other hand, the input-signal range is from 50 to 80% of the quantizer reference voltage and depends on the loop order and number of bits in the quantizer [4]. Therefore, the input-signal is going to be relatively small when compared

to other topologies, and to meet thermal noise requirements the capacitor sizes must be larger, leading to greater power dissipation. The third harmonic generated by the opamp nonlinearity is clear in the output spectrum shown in Fig. 2.2. Distortion severely reduces the SNDR of the CIFB topology from the ideal 76 dB to 62 dB for the example shown in Fig. 2.2.

The CIFB is the most commonly used topology for ΔΣ modulators. An example of the CIFB topology is implemented as a third-order CIFB ΔΣ modulator using a 4-bit internal quantizer and operating with a sampling frequency of 100 MHz at an OSR of 8 [6]. The modulator achieves a *signal to noise plus distortion ratio* (SNDR) of 67 dB and a peak *signal to noise ratio* (SNR) of 68 dB with a 12.5 MS/s conversion rate. The modulator is implemented in 0.65μm technology and powered with 5 V supply while consuming 380mW.

2.1.2 Feedforward ΔΣ modulators

Distributed feedback is used to ensure stability of the cascade of integrators in the forward path of the CIFB topology. Alternatively, weighted feedforward paths can be used to establish stability. Such a structure is called the *cascade of integrators with weighted feedforward summation* (CIFF). The resulting CIFF topology for a second-order modulator is shown in Fig. 2.3.

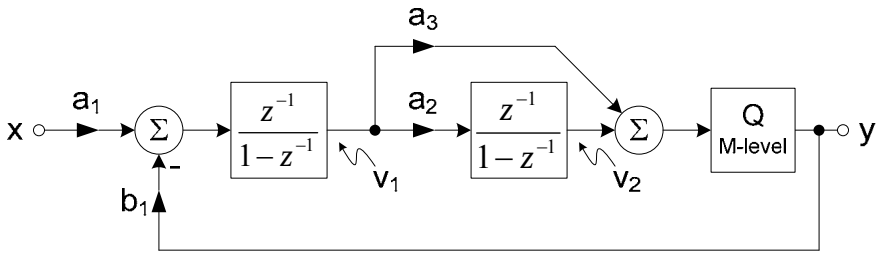

Fig. 2.3: Second-order CIFF modulator

Analysis of the linearized system with $a_1 = a_2 = b_1 = 1, a_3 = 2$ leads to the following results:

$$STF = \frac{y}{x} = z^{-1}\left(2 - z^{-1}\right) \tag{2-5}$$

$$NTF = \frac{y}{q} = \left(1 - z^{-1}\right)^2 \tag{2-6}$$

$$v_1 = z^{-1}\left(1 - z^{-1}\right)x - z^{-1}\left(1 - z^{-1}\right)q \tag{2-7}$$

$$v_2 = z^{-2}x - z^{-2}q \tag{2-8}$$

where q is the quantization noise from the internal quantizer, and v_1 and v_2 are the signals at the outputs of the first and second integrators, respectively.

The CIFF improves the performance of CIFB in terms of the signals at the output of the integrators. As can be seen from Eq. (2-7), the signal at the output of the first opamp contains a first-order noise shaped input-signal component in addition to shaped quantization noise. This reduces signal swing and reduces dependence of the distortion on the input-signal. Both of these benefits are illustrated in Fig. 2.4 for a sinusoidal input signal which parameters are specified in the figure. The signal swing at the output of the first opamp is significantly reduced and the output spectrum does not show harmonic distortion. The second opamp output still contains an input-signal component as can be seen from Eq. (2-8); however, nonlinearities at this stage are not as important since they are second-order noise shaped when referred back to the input.

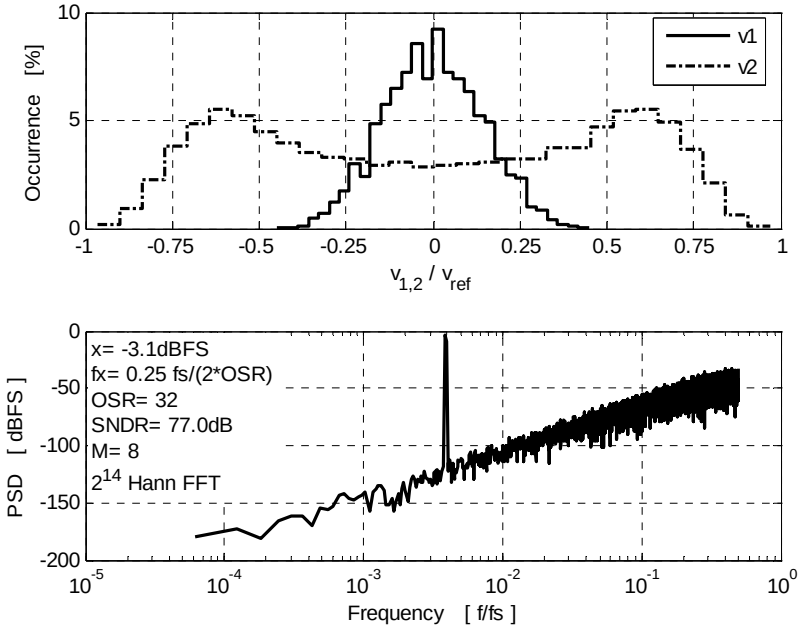

Fig. 2.4: Signal swing at Opamp outputs and sample output spectrum for CIFF

The main disadvantage of the CIFF topology can be seen by investigating its STF given in Eq. (2-5). The STF has a high frequency boost with a gain of one at low frequencies and a gain of three at half the sampling frequency. The amplification of the out-of-band frequencies due to the high frequency boost can overload the quantizer and drive the modulator into instability. Unfortunately, the NTF, STF, and modulator states are not independent. Selection of the NTF fixes the magnitude of the high frequency boost in the STF.

One of the fastest CMOS ΔΣ modulators reported in literature is implemented using the CIFF topology where a fifth-order CIFF ΔΣ modulator uses a 4-bit internal quantizer and operates at a 200 MHz sampling frequency at an OSR of 8 [7]. The modulator achieves an SNDR of 72 dB with a peak SNR of 82 dB at a conversion rate of 25 MS/s. The differential input signal range is 1.6 $V_{pp,diff}$. This performance is achieved in 0.18μm CMOS technology and powered with 1.8 V supply while consuming 200mW.

2.1.3 Feedback ΔΣ modulators with input-feedforward

The input-signal component at the opamp outputs in the CIFB topology can be eliminated by feeding the input-signal forward such that the input-signal components cancel out. The resulting *CIFB with input feedforward* (CIFB-IF) topology is illustrated for a second-order modulator in Fig. 2.5.

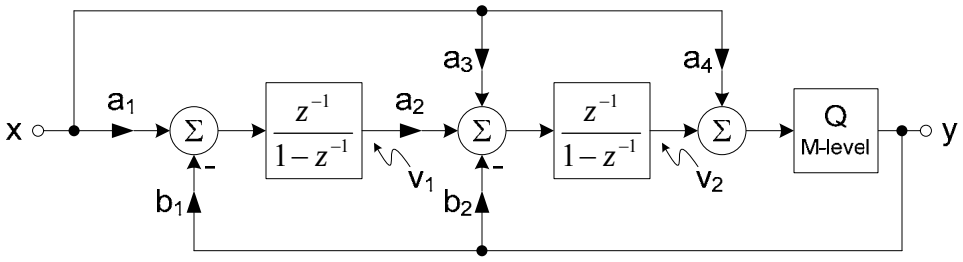

Fig. 2.5: Second-order CIFB-IF modulator

Analysis of the linearized system with $a_1 = a_2 = a_4 = b_1 = 1, a_3 = b_2 = 2$ leads to the following results:

$$STF = \frac{y}{x} = 1 \tag{2-9}$$

$$NTF = \frac{y}{q} = \left(1 - z^{-1}\right)^2 \tag{2-10}$$

$$v_1 = -z^{-1}\left(1 - z^{-1}\right)q \tag{2-11}$$

$$v_2 = -z^{-1}\left(2 - z^{-1}\right)q \tag{2-12}$$

where q is the quantization noise from the internal quantizer, and v_1 and v_2 are the signals at the outputs of the first and second integrators, respectively.

The input-feedforward modifies v_1, v_2, and the STF without affecting the NTF. The signals v_1 and v_2 are free of the input-signal component. Therefore, the signal swings are smaller and the distortion generated by the opamp is independent of the input-signal. These advantages

are illustrated in Fig. 2.6 for a sinusoidal input signal which parameters are specified in the figure. The STF magnitude response maintains its all pass response, however, its phase response changes.

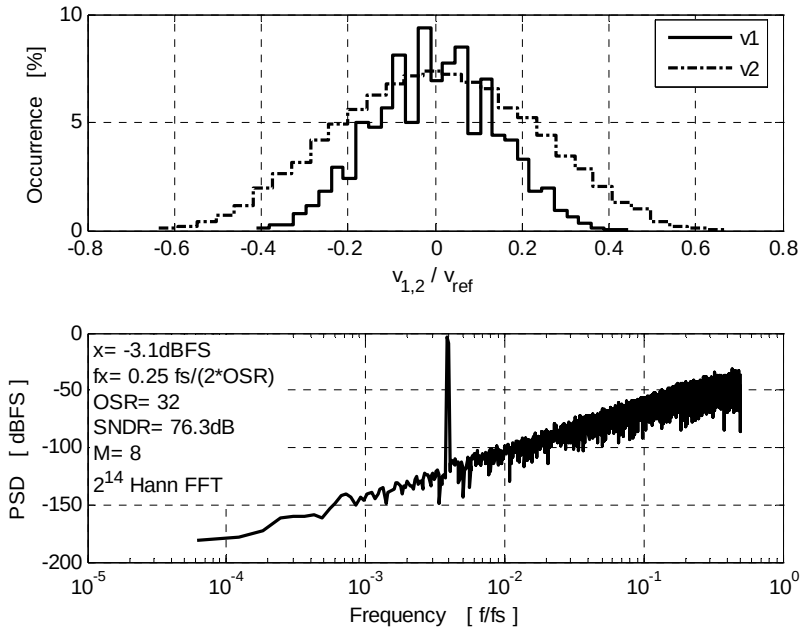

Fig. 2.6: Signal swing at Opamp outputs and sample output spectrum for CIFB-IF

The disadvantage of the CIFB-IF topology is the increased loading that the input has to drive, which can be particularly large for higher order modulators. This is because of the distributed feedforward paths that are needed to achieve the input-signal cancellation. In the second-order case, for example, there is the main sampling capacitor at the input as well as two extra sampling capacitors to feed the input-signal forward. It should be mentioned that the extra capacitors are usually smaller than the input sampling capacitor because the thermal noise on these capacitors is noise shaped when referred back to the input and therefore, their size can be smaller. Another disadvantage of the CIFB-IF topology is the delay-free path from the input, through the quantizer, and back to the modulator input. This delay-free path imposes implementation complications that are significant for high speed modulators. This problem and a possible solution are investigated thoroughly in Chapter 4.

An example of the CIFB-IF topology is demonstrated in [8] for a second-order modulator using a single-bit internal quantizer and operating with a sampling frequency of 105 MHz. For a signal bandwidth of 300 kHz (1.1 MHz), the modulator achieves an SNDR of 80 dB (78 dB) with a peak SNR of 82 dB (76 dB). The differential input signal range is 1.4 $V_{pp,diff}$. The modulator is

implemented in 0.13μm CMOS technology and powered with a 1.5 V supply while consuming only 8mW of power.

2.1.4 Feedforward ΔΣ modulators with input-feedforward

The input-feedforward concept can be used to modify the STF of the CIFF topology without affecting its NTF. Therefore, the high frequency boost in the STF of the CIFF topology can be eliminated. The resulting *CIFF with input feedforward* (CIFF-IF) topology is illustrated in Fig. 2.7 for a second-order modulator [2].

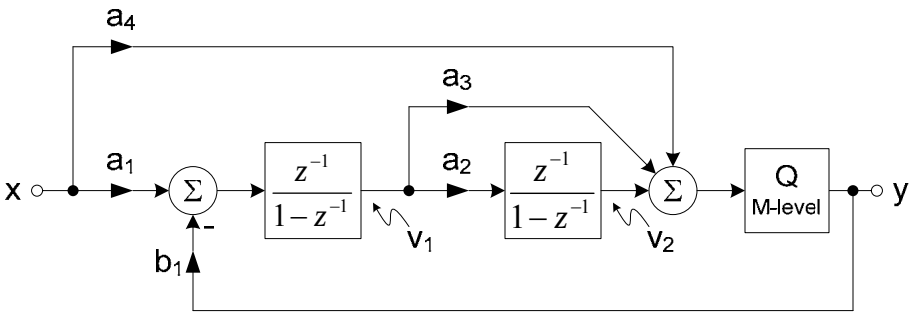

Fig. 2.7: Second-order CIFF-IF modulator

Analysis of the linearized system with $a_1 = a_2 = a_4 = b_1 = 1, a_3 = 2$ leads to the following results:

$$STF = \frac{y}{x} = 1 \tag{2-13}$$

$$NTF = \frac{y}{q} = \left(1 - z^{-1}\right)^2 \tag{2-14}$$

$$v_1 = -z^{-1}\left(1 - z^{-1}\right)q \tag{2-15}$$

$$v_2 = -z^{-2}q \tag{2-16}$$

where q is the quantization noise from the internal quantizer, and v_1 and v_2 are the signals at the outputs of the first and second integrators respectively.

The input-feedforward changes the problematic high frequency boost in the STF of the CIFF topology to an all-pass STF in the CIFF-IF topology with no effect on the NTF. In addition the signals v_1 and v_2 are free of the input-signal component. It is interesting to note that this modulator achieves the smallest signal swings at the output of the opamps among the topologies discussed, as seen in Fig. 2.8 for a sinusoidal input signal which parameters are specified in the

figure. Specifically, comparing the CIFF-IF and the CIFB-IF topologies, v_1 is similar. However, v_2 is smaller in the CIFF-IF topology since it contains quantization noise only in contrast to the CIFB-IF topology where v_2 contains shaped quantization noise.

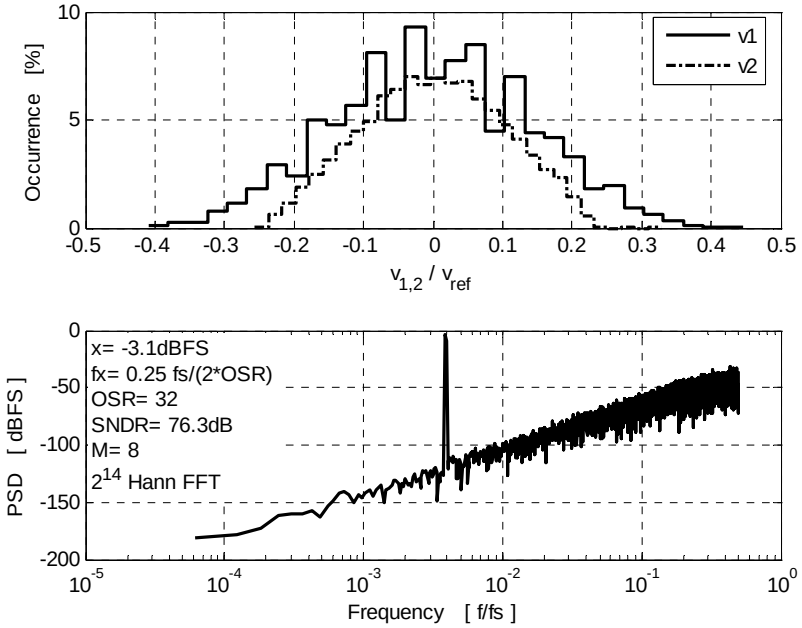

Fig. 2.8: Signal swing at Opamp outputs and sample output spectrum for CIFF-IF

The disadvantage of the CIFF-IF is the delay-free path from the input, through the quantizer, and back to the modulator input. This is the same problem as the CIFB-IF and is discussed further in Chapter 4.

2.2 Multistage Noise Shaping Modulators

The single loop topologies presented in the previous section operate on the principle of filtering the quantization noise out of the signal band and are called noise shapers. Another useful method for reducing quantization noise depends on noise cancellation, in addition to noise shaping. *Multistage noise shaping* (MASH) modulators fall under the noise cancellers category.

Multistage modulators allow the designer to build high order structures by cascading low order modulators. They have two advantages: using first and second-order modulators in each stage ensure stability of the overall modulator and they are more attractive for low OSR implementation. The low OSR advantage stems from the fact that in single-loop topologies the marginal improvement of the SQNR diminishes as the OSR decreases. The diminishing return makes the high-order single-loop topologies less attractive for high speed applications. The

drawback of MASH is that noise cancellation requires good matching between the analog and the digital circuits. Matching can be achieved by imposing higher requirements on the analog blocks to make them more ideal. Alternatively, digital circuits can be calibrated to match the analog ones and hence maintain the relaxed requirements on the analog components.

The multistage topology is illustrated using a cascade of two stages as shown in Fig. 2.9. The first stage is a general ΔΣ modulator of order L and the second stage is a general static (i.e. zero-order) ADC, hence, the name of this modulator is L-0 (also commonly known as the Leslie-Singh structure). In general, the multistage modulator can include any number of stages and each stage can be of different order. In the L-0 modulator, the second stage processes the quantization noise from the first stage (q_1). Then, the output from both stages is processed by the digital filters H_1 and H_2 and finally subtracted to produce the final output. H_1 is simply unit delays equal to the latency of the second stage while H_2 is equal to the NTF of the first stage.

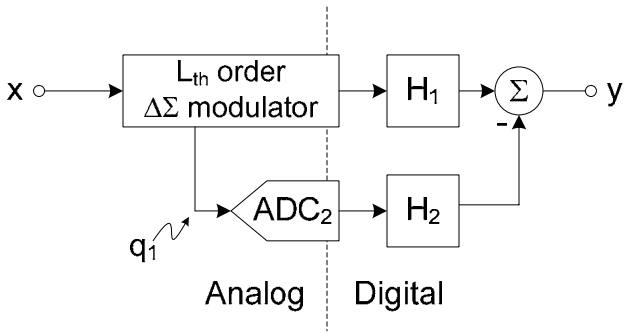

Fig. 2.9: The L-0 multistage modulator

Analysis of the linearized system leads to the following results assuming no latency in ADC_2:

$$y = STF_1\ x - NTF_1\ q_2 \tag{2-17}$$

where q_2 is the quantization noise from ADC_2, and STF_1 and NTF_1 are the signal and noise transfer functions of the first stage.

The difference between the L-0 multistage and a single loop modulator of order L is that the output contains the shaped quantization noise from the second stage instead of the first stage. Therefore, the quantization noise from the first stage is completely cancelled at the output. By making q_2 smaller than q_1, the SQNR is improved.

An example of the multistage topology is presented in [9] where a 2-0 structure is used operating at 20 MHz clock rate. The first stage is a second-order modulator with a five-bit internal quantizer and the second stage is a four-stage 12 bit pipeline ADC. The modulator

achieves a SNR of 89 dB at an OSR of 8 (1.25 MHz signal bandwidth) and 82 dB at an OSR of 4 (2.5 MHz signal bandwidth). The modulator is implemented in 0.6μm CMOS technology and powered with a 5 V analog supply and 3 V digital supply while consuming 550mW of power.

2.3 Time-Interleaved ΔΣ Modulators

The usual system level design parameters for ΔΣ modulators are the shape and order of the loop-filter, the OSR, and the number of bits in the internal quantizer. High-speed applications require low OSRs thereby limiting the choices available for the designer. One way of adding another degree of freedom is to use parallel ΔΣ structures. The simplest method of making parallel converters is through the use of *time-interleaving* (TI) which is simply a time-division multiplexing scheme where an array of individual converters are clocked at different instants in time. Unfortunately, exploiting simple time-interleaved parallelism is not a straightforward process for ΔΣ modulators due to their recursive nature. Straightforward TI adaptation to ΔΣ modulators results in a 3 dB improvement in the SNR for each doubling of converters regardless of the order of the modulator. To overcome this problem, different schemes of parallel modulators have been devised. They can be classified in one of three main categories: *frequency division multiplexing* (FDM) [10], *code division multiplexing* (CDM) [11], and *time division multiplexing* (TDM) [1].

TDM can be implemented by deploying the theory of block digital filtering. The principle of block digital filtering is based on transforming a *linear time-invariant* (LTI) *single-input single-output* (SISO) system with transfer function $H(z)$ to an equivalent multi-input multi-output system with transfer function $\overline{H}(z)$, as shown in Fig. 2.10.

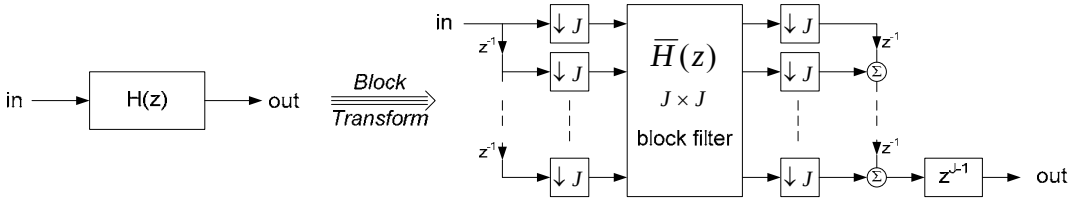

Fig. 2.10: H(z) and its blocked version with block length J

The internal circuitry of the block filter operates in parallel and at a reduced rate by the factor J. For example, using this transformation for a ΔΣ modulator with J=2 allows the internal modulators to either operate at half-speed for the same resolution, or at enhanced resolution for the same speed. This improvement is significant in wide bandwidth applications where the sampling speed is limited by the technology and resolution requirements.

The block digital filtering has facilitated the design and construction of a true TI ΔΣ modulator [1]. A second-order, time-interleaved by 2 (J=2), CIFB ΔΣ modulator is shown in Fig. 2.11 as an example of the technique.

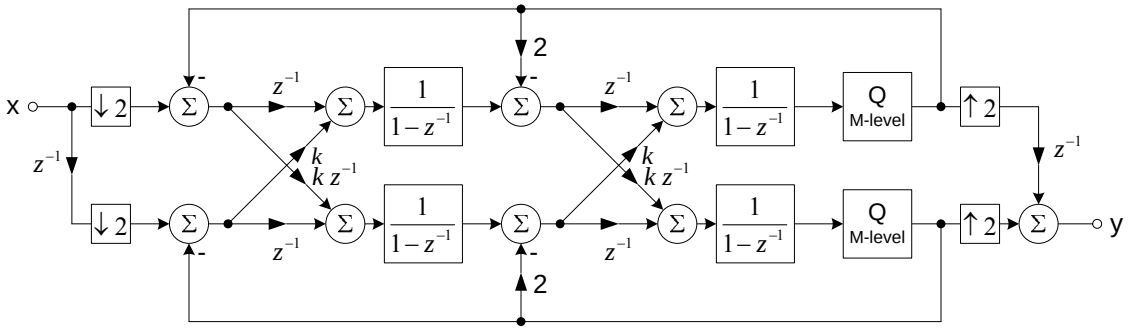

Fig. 2.11: Second-order time-interleaved by 2 CIFB ΔΣ modulator

The k-factor shown in Fig. 2.11 is used to deal with the issue of opamp DC offsets [1]. DC offsets are problematic in time-interleaved modulators because the difference in offset between the two branches drives the modulator to instability. Reducing the cross-coupling coefficients gives more control to each parallel ΔΣ modulator, thus enabling the negative feedback loop to adjust, which maintains DC stability. However, reducing k from unity modifies the STF and results in an increase of the quantization noise in the signal band, thereby reducing the SNDR. The choice of k is a tradeoff between the offset value that the modulator can tolerate and the achievable SNR. A significant advantage of the k-factor is the creation of a notch at half the sampling frequency. This notch attenuates the aliasing that occurs due to component mismatches [1]. There are two potential limiting factors in the time-interleaving modulators especially for an interleaving factor larger than two. First, the analog demux at the modulator input. This limitation is discussed in more detail below and in Chapter 3. Second, the critical path created due to the lack of delays between the output of a quantizer and the input of another.

A high-speed demux is needed at the input of the modulator to sample the input-signal and distribute it to the individual internal modulators. The demux operates at the full speed of the overall TI structure. For example, for a time-interleaving factor of 4, the demux operates at four times the speed of the individual ΔΣ modulators. The high-speed demux can become the limiting factor in the performance especially for higher-order TI structures (J>2). A solution to the demux problem for J=2 is to sample each branch at a different phase of the two non-overlapping clocks [1]. Therefore, the demux is inherent in the operation of the modulator. Another more general solution that can be used for any J is called the zero-insertion interpolation technique [12], which

is shown in Fig. 2.12 for J=2 second-order CIFB topology. The *zero-insertion time-interleaved* (ZITI) ΔΣ samples the input-signal at the operating frequency of the individual ΔΣ modulator and applies these samples to one branch only with the inputs to the others grounded.

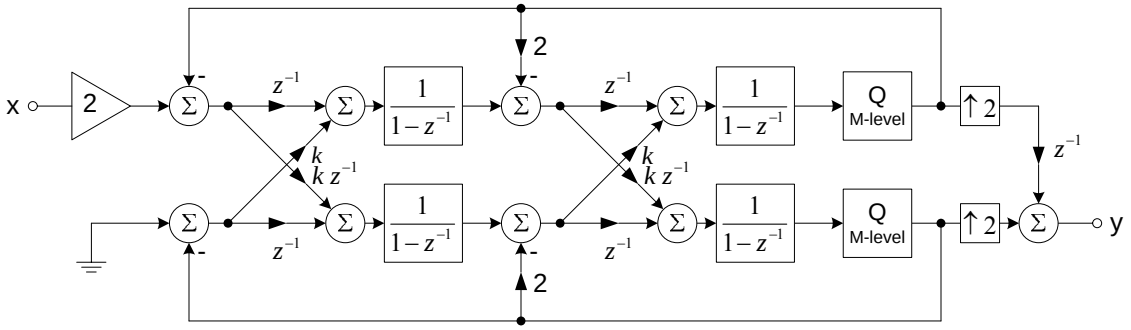

Fig. 2.12: Second-order ZITI with J=2 CIFB ΔΣ modulator

The sampled input must be amplified (by J) to compensate for the lost signal power resulting from supplying zero input instead of the input-signal to the other branches. However, the input signal amplification causes the ZITI modulator to become unstable at smaller input levels than the traditional TI modulator. In addition, The ZITI modulator still suffers from DC offsets and therefore the cross-coupling coefficient k must be set appropriately.

2.4 Summary

The design of ΔΣ modulators involves tradeoffs between the NTF, STF, and internal states. Different topologies provide different degrees of freedom in the determination of these three parameters. The NTF determines the achievable SNDR for a given modulator. The internal states are significant from the analog circuit standpoint; therefore, the design of the states is critical for the reliable implementation of ΔΣ modulators in the nano-scale CMOS technology.

ΔΣ modulators can be classified in two broad categories: noise shapers and noise cancellers. Multi-stage ΔΣ modulators are noise cancellers. For the noise cancellation to work properly, good matching between the analog part and the digital part is required.

Parallelism can be used to improve the speed of oversampled modulators. Specifically, time-interleaving based on the block filtering theory can increase the attainable bandwidth of a given modulator.

Appendix A: Modeling Non-Idealities in Switched-Capacitor ΔΣ Modulators

Behavioral simulations provide a convenient way to understand the operation of systems and offer a quick method to evaluate the tradeoffs involved in their design. High-level simulations are particularly useful in the design of ΔΣ modulators because of the strong non-linear nature of these modulators. Since linearized models provide a qualitative understanding of ΔΣ modulators only, a full time-domain simulation of the modulators is necessary to verify their operation. Matlab and Simulink is the tool of choice for performing system level simulations due to its extensive number of toolboxes and ease of use.

This appendix focuses on the simulation of non-idealities in switched-capacitor circuits that are critical to the operation of ΔΣ modulators. In particular, the settling behavior of switched-capacitor integrators is studied to assist in the development of a Simulink model that takes settling errors into account. With this model, initial estimates of the required opamp specifications can be determined and used in the circuit level design.

There are two strategies for determining the opamp requirements in the design of ΔΣ modulators. The first strategy is to design the integrators to settle to the full accuracy of the overall modulator. In this case, analytical methods can be used to determine the opamp specifications directly. In the second strategy, the integrators are allowed to settle to less than the full accuracy, however, their settling must be linear. The incomplete linear settling changes the coefficient value of the integrators which alters the NTF and the STF. The changes in the transfer functions have an insignificant effect on the performance of ΔΣ modulators, especially for single loop topologies. Consequently, if slewing in the opamp is guaranteed not to occur, a more power efficient modulators can be obtained by following the second design strategy. Therefore, the non-linear nature of ΔΣ modulators in addition to its relaxed settling requirements makes system level time-domain simulations a desirable step in the design process.

The settling behavior of a switched-capacitor integrator can be divided into static settling and dynamic settling. The static settling is determined by the finite gain of the opamp and is independent of time. The dynamic settling is a function of the speed of the modulator and is limited by the finite unity-gain frequency and the slew rate of the opamp.

Consider the parasitic-insensitive switched-capacitor delaying integrator shown in Fig. A.1 where C_S is the sampling capacitor, C_I is the integrating capacitor, C_O is the total capacitor connected at the integrator output, and C_P is the total parasitic capacitor at the opamp input.

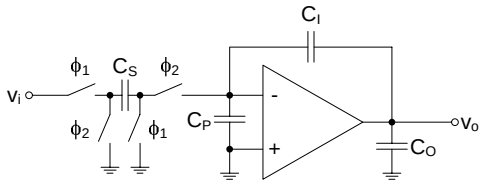

Fig. A.1: Switched-capacitor delaying integrator

With infinite opamp gain, bandwidth, and slew rate, the integrator has the following transfer function assuming ideal switches and with the output taken at the end of phase 1:

$$\frac{v_o}{v_i} = \frac{a\, z^{-1}}{1 - z^{-1}}$$

where a is the integrator coefficient (C_S/C_I).

Finite opamp gain (A) introduces a gain error (ε_a) and a phase error (ε_θ) which modifies the integrator transfer function as following:

$$\frac{v_o}{v_i} = \frac{a\left(1-\varepsilon_a\right) z^{-1}}{1-\left(1-\varepsilon_\theta\right) z^{-1}}$$

where:

$$\varepsilon_a = \frac{C_I + C_S + C_P}{\left(A+1\right) C_I + C_S + C_P} \approx \frac{1}{A\beta}$$

$$\varepsilon_\theta = \frac{C_S}{\left(A+1\right) C_I + C_S + C_P} \approx \frac{a}{A}$$

and β is the feedback factor $C_I/(C_I+C_S+C_P)$.

Next, consider finite opamp unity-gain frequency for a single stage opamp. A gain error (ε_u) is introduced in response to a step input:

$$\frac{v_o}{v_i} = \frac{a\left(1-\varepsilon_u\right) z^{-1}}{1 - z^{-1}}$$

where:

$$\varepsilon_u = \left(1 + \frac{\tau_z}{\tau}\right) e^{-t_{settle}/\tau} \approx e^{-t_{settle}/\tau}$$

and:

$$\tau = 1/\omega_{-3dB}$$

$$\omega_{-3dB} = \beta\, \omega_u = \beta\, g_m / C_L$$

$$C_L = C_O + \beta\left(C_S + C_P\right)$$

$$\tau_z = C_I / g_m$$

where t_{settle} is the available settling time which is approximately half the period, g_m and ω_u are the transconductance and the unity-gain frequency of the opamp respectively, ω_{-3dB} is the integrator closed-loop bandwidth, and τ_z is the time constant of the feedforward zero.

The phase error due to finite opamp gain and the gain error due to dynamic linear settling and static settling can be incorporated into the Simulink model for system level simulations. Circuit level design should make sure that slewing does not occur. Modern ΔΣ modulators usually employ multi-bit internal quantizers, therefore, they are much less prone to get into slew limited region. Therefore, the incomplete linear settling strategy works well with multi-bit modulators. Furthermore, input-feedforward topologies have the least slew-rate requirement due to their small signal swings at the integrator outputs.

Chapter 3:

Time-Interleaved ΔΣ Modulators

TIME-INTERLEAVING is discussed in Chapter 2 as a method to add another degree of freedom to the design of ΔΣ modulators. In this chapter a modified time-interleaved ΔΣ modulator is introduced. The new modulator requires the same number of opamps used by traditional modulators but with more quantizers and interconnects paths. Since the new topology requires the same number of opamps regardless of the interleaving order, it is called the *single-path time-interleaved* (SPTI) ΔΣ modulator. In contrast, traditional time-interleaved modulators require J-paths for an interleaving factor of J; therefore, they are referred to as the *multi-path time-interleaved* (MPTI) ΔΣ modulators.

The SPTI modulator eliminates some of the problems the MPTI topology suffered from which are discussed in chapter 2. Specifically, the opamp DC offsets problem and the high speed demux at the modulator input are not present in the SPTI architecture. However, the critical path created due to the lack of delays between the output of a quantizer and the input of another is still present. A prediction technique to deal with the critical path in time-interleaved modulators was presented in [13]. This technique can be utilized in conjunction with the topologies in this chapter to alleviate the critical path problem.

The outline of this chapter is as follows: Section 3.1 introduces the derivation of the new time-interleaved modulator. Section 3.2 discusses the consequences of removing the analog demux at the input. Section 3.3 evaluates the new modulator. Section 3.4 investigates the mixed multi-path and single-path time-interleaved modulator as a possibility to alleviate some issues in the SPTI topology. Section 3.5 investigates a partial calibration scheme for the SPTI ΔΣ modulator. Section 3.6 analyzes mismatch shaping in multi-bit SPTI modulators. Finally, the timing constraint in the SPTI is discussed in Section 3.7 and a possible solution is proposed.

3.1 Single-Path Time-Interleaved ΔΣ Modulator Concept

The first SPTI modulator was reported in [14] where the concept of removing the high-speed input demux and feeding the input to all paths in the time-interleaved modulator was proposed. It

was shown later that removing the demux modifies the STF of the SPTI architecture [15]. More recently, a discrete-time SPTI modulator was reported in [13]. In addition to the single-path feature, some of the analog processing was transferred into the digital domain. This transfer eliminated the critical path issue discussed later in this chapter at the expense of requiring finer resolution quantizers.

In this section, new SPTI discrete-time ΔΣ modulators are presented. First-order SPTI modulators with an interleaving factor of 2 are developed as an illustration of the derivation procedure. The starting point of the derivation is the MPTI modulator [1] with the input demux removed and the input signal fed to both branches of the modulator [14] as shown in Fig. 3.1.

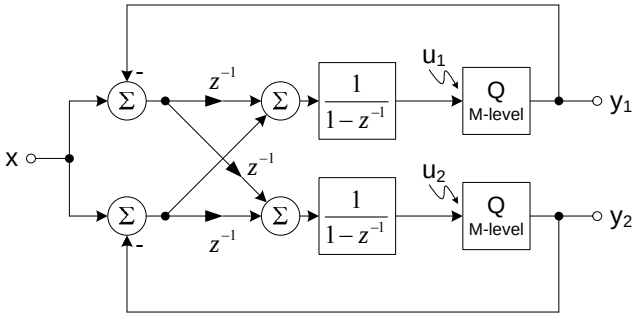

Fig. 3.1: MPTI ΔΣ modulator without input demux

The inputs to the quantizers are needed later in the derivation process. They can be determined directly from the block diagram in Fig. 3.1:

$$u_1 = \frac{1}{1-z^{-1}}\left[\left(1+z^{-1}\right)x - z^{-1}y_1 - y_2\right] \tag{3-1}$$

$$u_2 = \frac{1}{1-z^{-1}}\left[2z^{-1}x - z^{-1}y_1 - z^{-1}y_2\right] \tag{3-2}$$

The next step is to combine the two adders in the top path into a single adder as well as combining the two adders in the bottom path. With the combined adders, the modulator can be redrawn as shown in Fig. 3.2a. The rearranged modulator is split into two separate entities as shown in Fig. 3.2b. Therefore, if we can generate y_2 from x, y_1, and u_1, the top branch can operate as a stand alone time-interleaved modulator. Similarly, if we can generate y_1 from x, y_2, and u_2, the bottom branch can operate as a stand alone time-interleaved modulator.

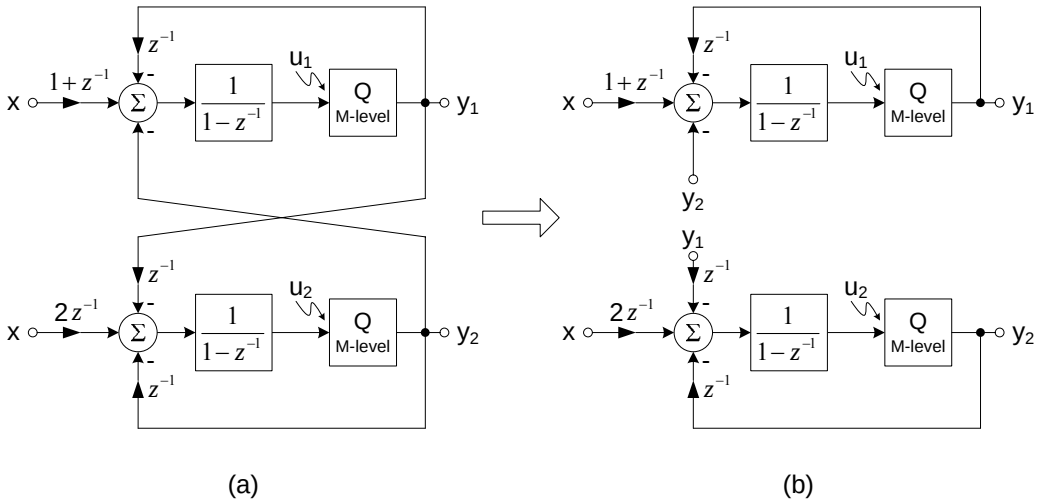

Fig. 3.2: (a) MPTI ΔΣ modulator without input demux rearranged (b) with top and bottom paths split

To generate a SPTI modulator from the bottom path, we can manipulate Eqs. (3-1) and (3-2). First, Solve Eq. (3-2) for y_1:

$$y_1 = z\left(2z^{-1}x - z^{-1}y_2 - \left(1-z^{-1}\right)u_2\right)$$

Next, substitute y_1 into Eq. (3-1):

$$u_1 = x - y_2 + u_2$$

Since y_1 is the quantized value of u_1: y_1 can be generated from x, y_2, and u_2 as desired. Therefore, the bottom path of Fig. 3.2b can be used as a time-interleaved modulator as shown in Fig. 3.3.

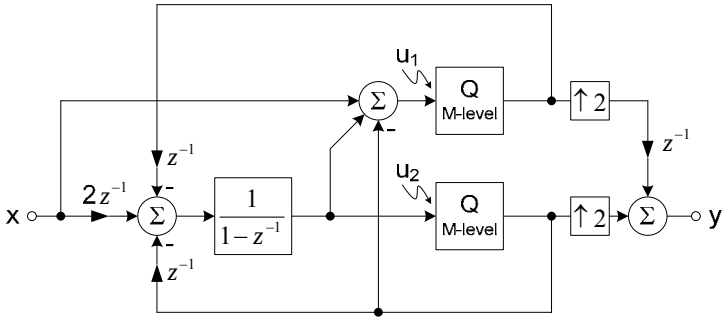

Fig. 3.3: SPTI ΔΣ modulator with an interleaving factor of 2

Similarly, to generate a SPTI modulator from the top path, we solve Eq. (3-1) for y_2 and substitute it into Eq. (3-2) to obtain:

$$u_2 = z^{-1}x - z^{-1}y_1 + z^{-1}u_1$$

Since y_2 is the quantized value of u_2: y_2 can be generated from x, y_1, and u_1 as desired. Therefore, the top path of Fig. 3.2b can be used as a time-interleaved modulator as shown in Fig. 3.4.

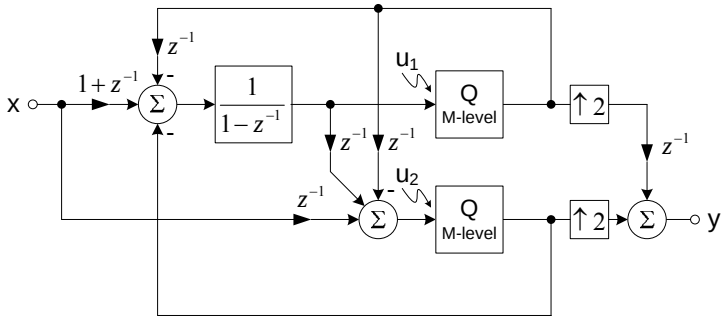

Fig. 3.4: SPTI ΔΣ modulator with an interleaving factor of 2

The input of the SPTI modulator in Fig. 3.4 can be simplified further by modifying the bilinear discrete-integrator to a delaying discrete-integrator. This means a loss of half the input signal and therefore must be compensated by increasing the input gain to 2. Using extensive Matlab simulations, the modulators in Fig. 3.3 and Fig. 3.4 have similar performance with and without non-idealities in their building blocks.

Additional SPTI discrete-time ΔΣ modulators can be developed using the method presented above. The starting point of the derivation is the MPTI modulator [1] with the zero-insertion concept [12]. First-order SPTI modulators with an interleaving factor of 2 are derived as shown in Fig. 3.5 and Fig. 3.6. As discussed in chapter 2 however, the stable input-signal level is smaller for modulators with zero-insertion due to the amplification at the input by the interleaving factor.

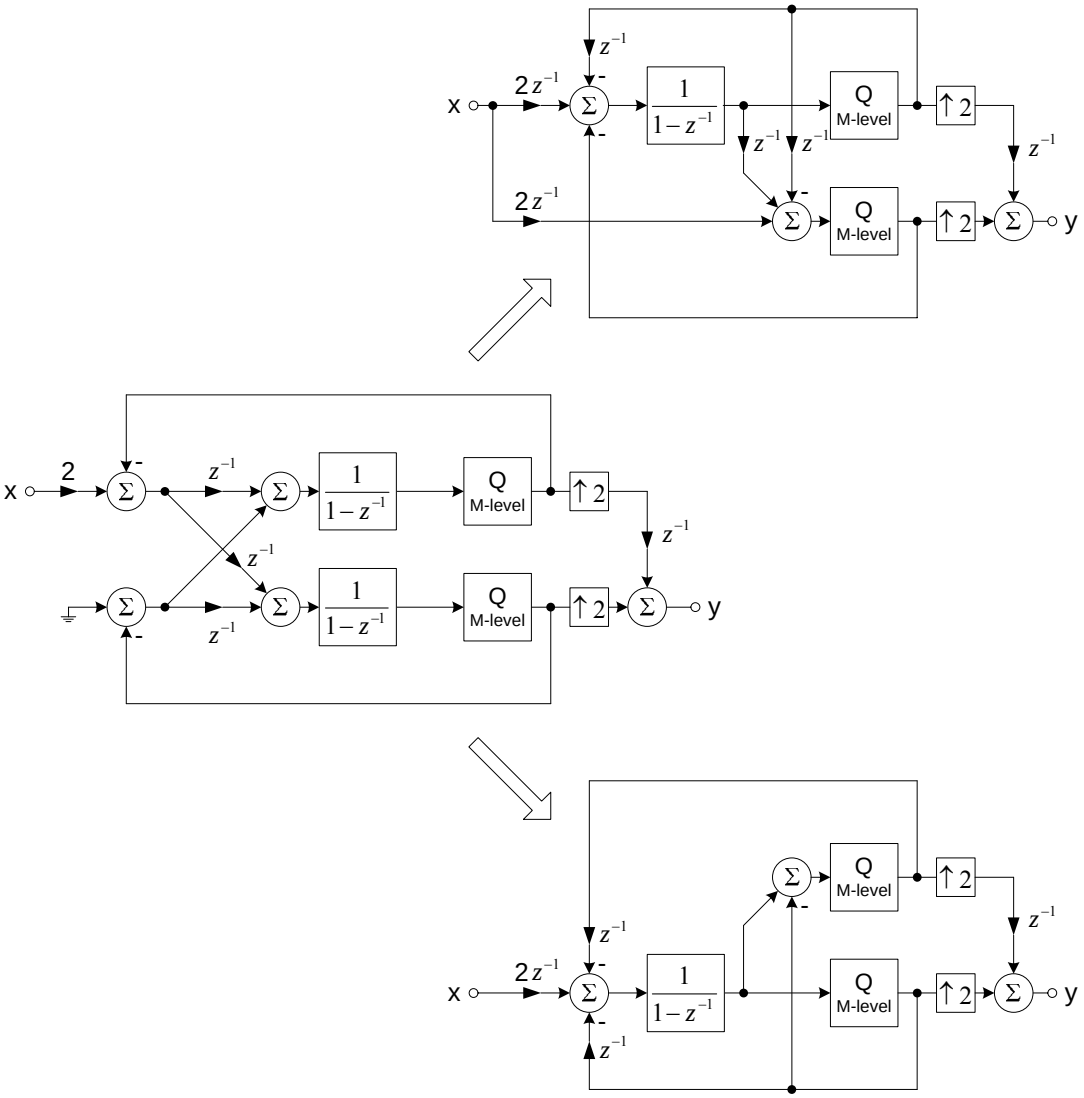

Fig. 3.5: SPTI ΔΣ modulators with an interleaving factor of 2

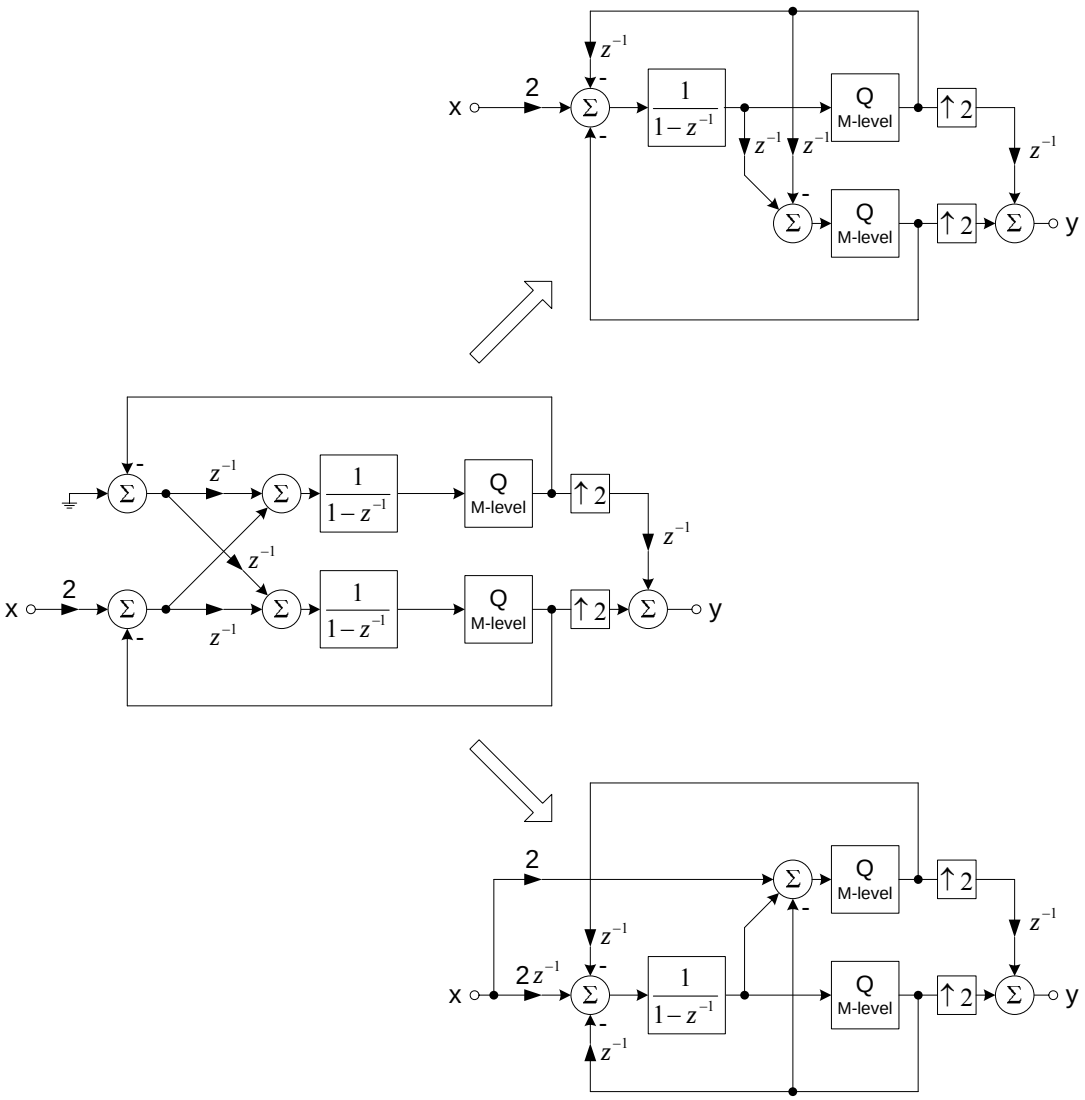

Fig. 3.6: SPTI ΔΣ modulators with an interleaving factor of 2

The SPTI modulator has several advantages when compared to the MPTI modulator. First, it does not suffer from the DC offset problem like the traditional time-interleaved ΔΣ modulator. In addition, the SPTI eliminates the high-speed analog demux at the input of the modulator while also using fewer opamps.

3.2 Effects of Removing the Demux

Removing the analog demux at the input has some consequences [15]. Analysis of the linearized system of Fig. 3.3 leads to the following results:

$$y = z^{-1}\left(1+z^{-1}\right)x + z^{-1}\left(1-z^{-1}\right)q_1 + \left(1-z^{-1}\right)q_2$$

where q_1 and q_2 are the quantization noise from the top and bottom quantizers respectively. Due to the output mux, the quantization noise q_1 is only added to the output once for every two samples, which is also true for q_2. Therefore, the overall noise contribution can be rewritten as:

$$NTF = \frac{y}{q} = \left(1 - z^{-1}\right)$$

which is simply first-order noise shaped. Clearly, the removal of the demux does not affect the NTF, however the STF is affected. The first term in the STF is z^{-1}, which is the expected STF of a first-order CIFB modulator. The second term $\left(1 + z^{-1}\right)$ resulted from the removal of the input demux. The extra term adds a notch at half the sampling frequency and filters the amplitude response of the STF as shown in Fig. 3.7. Due to oversampling, the frequency variation is not significant within the signal band.

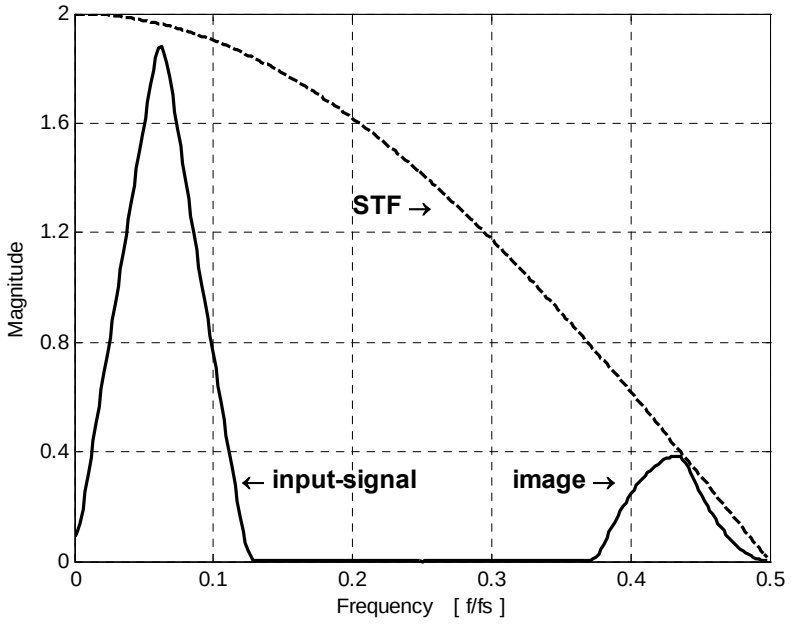

Fig. 3.7: STF and imaging issue for SPTI

Another effect of removing the demux is that the signal is under the influence of the upsamplers only. The effect of upsampling by J is J-fold compression and repetition of the frequency-domain magnitude response [16]. The process generates images shaped by the STF at frequencies less than half the sampling frequency as shown in Fig. 3.7.

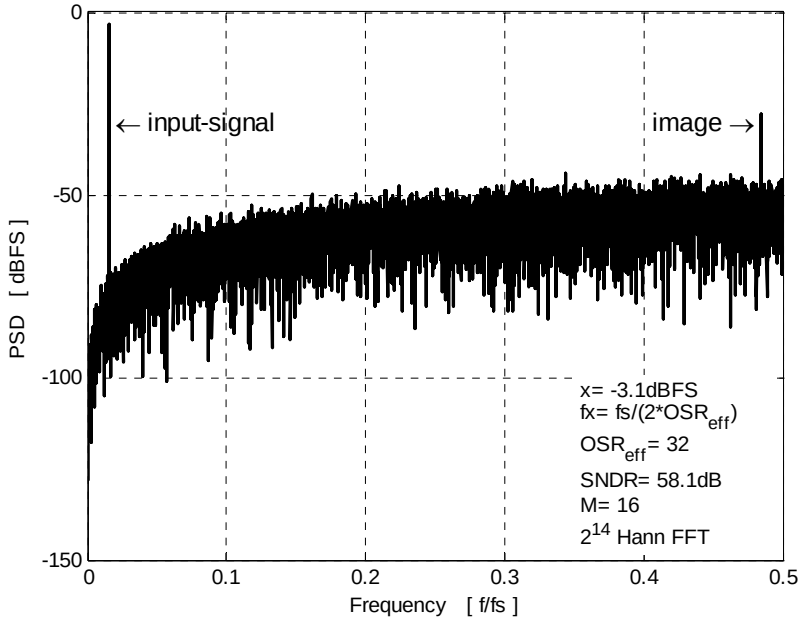

Fig. 3.8: Sample output spectrum for the SPTI of Fig. 3.3

A sample output spectrum of the SPTI modulator in Fig. 3.3 is shown in Fig. 3.8. It also highlights the shaped image of the input-signal.

3.3 Evaluation of the SPTI ΔΣ Modulator

Several simulations using Matlab and Simulink are used to evaluate the performance of the new SPTI modulator and to compare it to traditional structures. The simulations use the second-order SPTI modulator shown in Fig. 3.9, the MPTI modulator shown in Fig. 2.11 with a k-factor of 1, and the traditional CIFB modulator shown in Fig. 2.1. The time-interleaved by 2 modulators are clocked at half the rate of the CIFB modulator. In other words, the oversampling ratio of the CIFB (OSR) and the effective oversampling ratio of the SPTI and MPTI (OSR_{eff}) are equal, hence, their expected SNDR is the same.

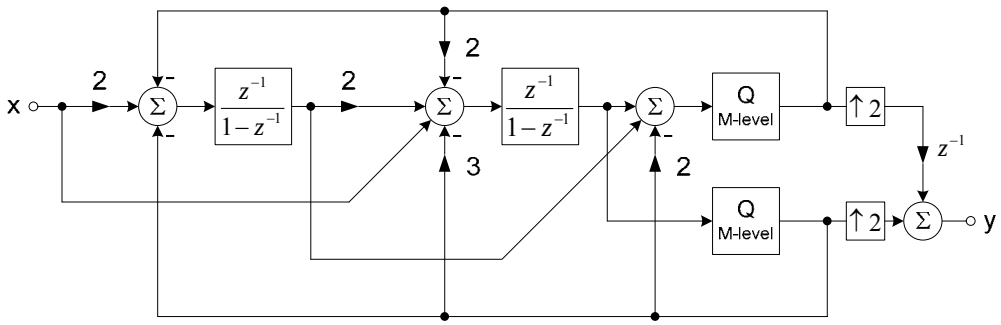

Fig. 3.9: Second-order SPTI ΔΣ modulator with interleaving factor of 2

The modulators are simulated taking into account the effects of finite gain and bandwidth in the opamps. The second stage integrator opamp has 5% less gain and bandwidth than those in the first stage. In addition, a 2% mismatch between the two paths of the MPTI modulator is considered. The results are summarized in Fig. 3.10 where f_{-3dB} is the closed-loop -3 dB bandwidth of the opamp.

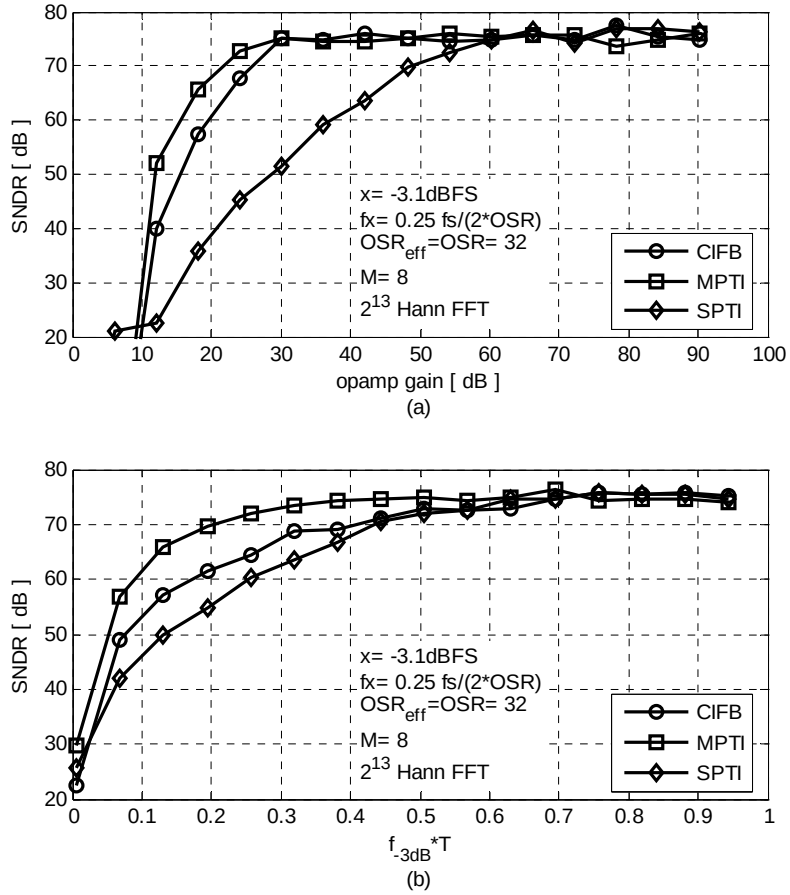

Fig. 3.10: SNDR versus (a) opamp gain (b) normalized bandwidth

We can observe that the MPTI requires less opamp gain and bandwidth than the CIFB which is close to the prediction in [1]. On the other hand, the SPTI requires much larger opamp gain and bandwidth to achieve the same SNDR as the CIFB even though it is clocked at half the clock speed.

To identify the cause of the large gain and bandwidth requirements in the SPTI, the error introduced by the finite gain and bandwidth into the modulator transfer functions should be understood. First, the limited bandwidth will cause an error in the integrator coefficient, which is simply an error in the numerator of the integrator transfer function. Second, finite gain will introduce both gain and phase errors in the integrators transfer function, which is an error in the numerator and the denominator. Therefore, gain error and phase error factors are added into the SPTI model in Fig. 3.9 and the STF, NTF_1, and NTF_2 transfer functions are derived. The resulting formulas are complicated and no intuitive understanding can be gained from them (see Table 3.1 in section 3.5). Therefore, the equations are solved numerically with 50 dB opamp gain and a

bandwidth of 3 time constants. It is found that the modification in any of the transfer functions is not significant on its own. However, the difference between NTF_1 and NTF_2 is significant as can be seen in Fig. 3.11c. Since the overall NTF is a combination of NTF_1 and NTF_2, the mismatch introduces an error in the final NTF and degrades the achievable SNDR.

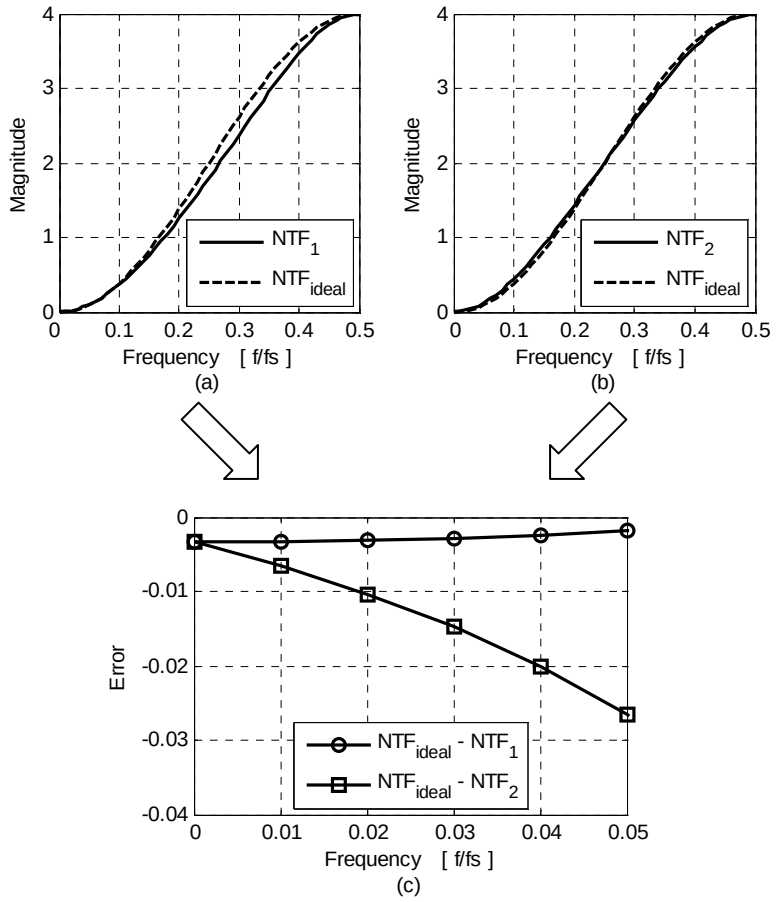

Fig. 3.11: NTFs of the SPTI with gain and phase errors (a) ideal NTF and modified NTF_1 (b) ideal NTF and modified NTF_2 (c) NTF_1 and NTF_2 error at low frequencies

Fig. 3.11a-b) show NTF_1 and NTF_2 with typical integrator gain and phase errors and the NTFs with no errors. Fig. 3.11c show the difference between NTF_1 and NTF_2 with non-idealities and their ideal behavior for low frequencies which represents typical signal bands for ΔΣ modulators. It can be observed that the error in NTF_1 is much less than the error in NTF_2. This NTF mismatch due to finite gain and bandwidth is the reason for the large requirement from the SPTI modulator. Therefore, by increasing the gain and bandwidth, the analog integrators become more ideal and the NTF matching improves. Unfortunately, the NTF mismatch can not be calibrated easily which makes it a significant issue. On the other hand, the MPTI modulator does

not suffer from the NTF mismatch problem. This is because each NTF is modified by the errors in a separate path. Thus, assuming the opamps have similar gains and bandwidths, the errors in the different paths are similar. Therefore, the mismatch between the NTFs is small. Consequently, the gain and bandwidth requirements of the MPTI are less than SPTI.

3.4 Mixed Multi-Path and Single-Path Time-Interleaved ΔΣ Modulator

In an attempt to overcome the NTF mismatch problem encountered in the SPTI modulator, a hybrid of multi-path and single-path time-interleaved modulator is derived. The hypothesis here is that the first stage will not suffer from the NTF mismatch because it is multi-path. Therefore, NTF mismatch errors from the single-path in later stages are attenuated when referred back to the input.

The derivation of the mixed *multi-path single-path time-interleaved* (MPSPTI) discrete-time ΔΣ modulators is illustrated for a second-order modulator with an interleaving factor of 2 using the method presented in section 3.1. The derivation procedure is applied to the second stage of the MPTI modulator shown in Fig. 3.12 only. The input to the top quantizer (u_1) after eliminating its dependency on y_1 is:

$$u_1 = w_2 - 2y_2 + u_2$$

Which can be used to build the bottom MPSPTI modulator in Fig. 3.12. Similarly, the top MPSPTI modulator can be constructed by eliminating y_2 from u_2:

$$u_2 = z^{-1}w_1 - 2z^{-1}y_1 + z^{-1}u_1$$

Since the first stage of the modulator is multi-path, the input signal can be applied in different forms. For example, an analog input demux can be used, the input demux can be removed and the input is supplied to both paths, or the zero-insertion concept can be used.

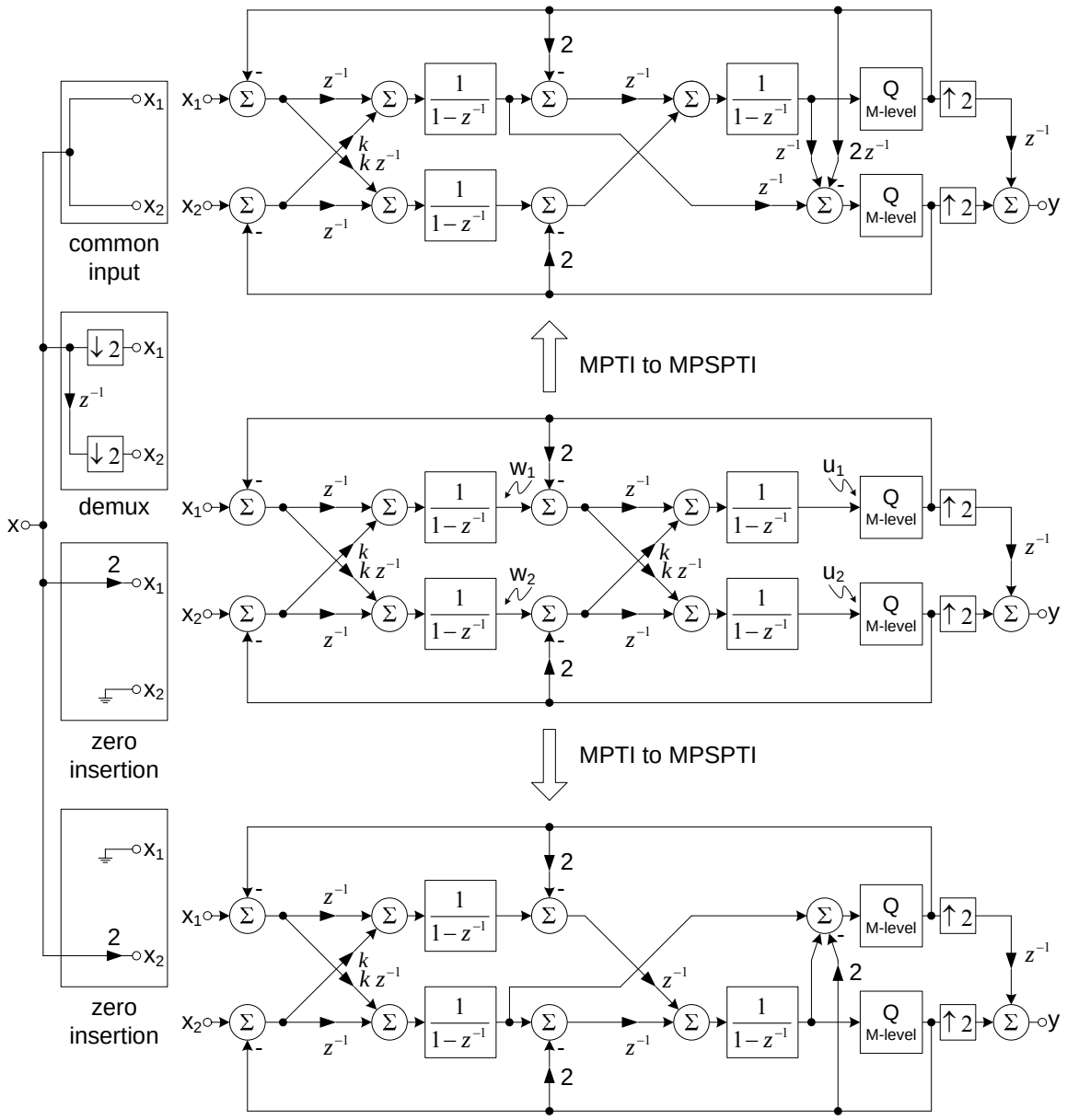

Fig. 3.12: MPTI and MPSPTI modulators

Both MPSPTI modulators have similar performance with and without non-idealities for the common input and demux front end. However, the SNDR is less for the zero-insertion front end due to stability reasons as mentioned in chapter 2. Therefore, the zero-insertion is excluded from the following discussion. As shown in Fig. 3.13, the MPSPTI modulator requires slightly more opamp gain than the CIFB counterpart, however, it relaxes the bandwidth requirements. The simulations take into account the effects of finite gain and bandwidth in the opamps. The second stage integrator opamp has 5% less gain and bandwidth than those in the first stage. In addition, a

2% mismatch between the two paths in the first stage of the MPSPTI modulator is considered. The MPSPTI first stage uses a demux for the input signal and a unity cross coupling factor.

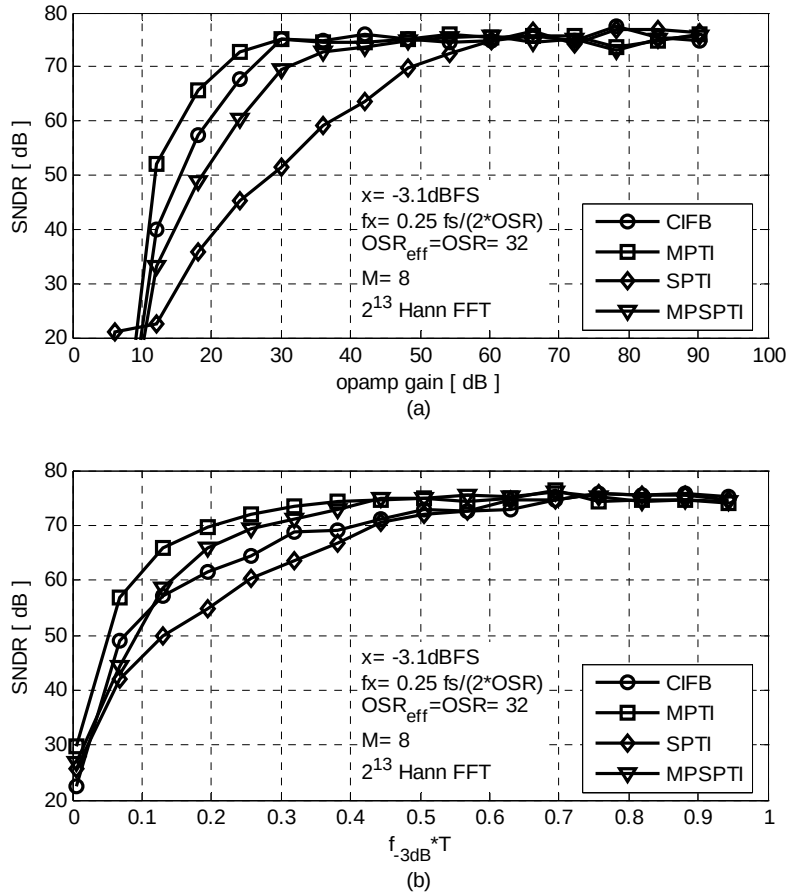

Fig. 3.13: SNDR versus (a) opamp gain (b) normalized bandwidth

To verify the hypothesis further, a modulator with single-path first stage and multi-path second stage is derived. The mixed *single-path multi-path time-interleaved* (SPMPTI) ΔΣ modulator should suffer from the NTF mismatch problem. Applying the method of section 3.1 to the first stage of the MPTI modulator only, the SPMPTI topology can be developed as shown in Fig. 3.14.

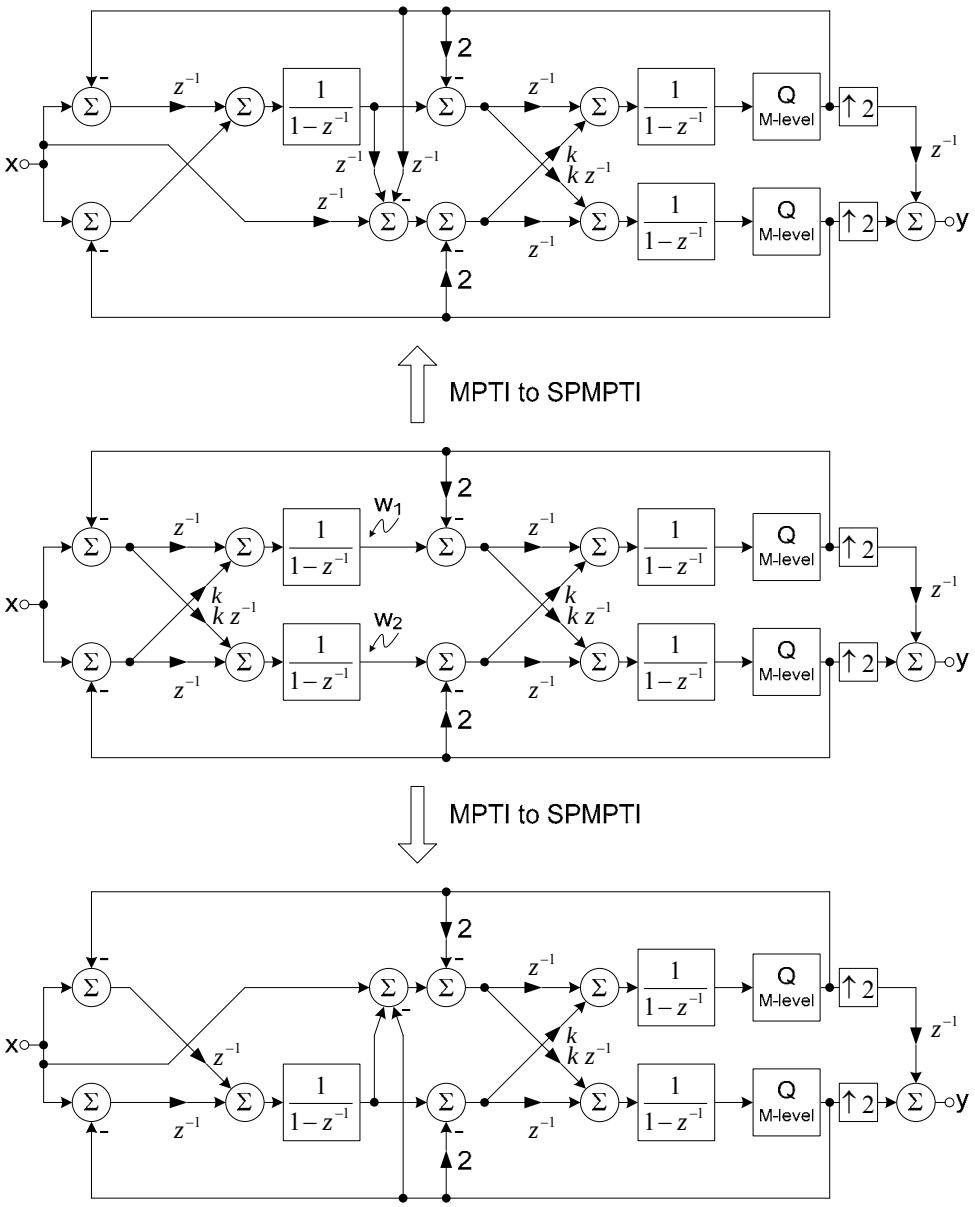

Fig. 3.14: MPTI and SPMPTI modulators

Both SPMPTI modulators have similar performance with and without non-idealities. The SPMPTI modulator performance is closer to the SPTI topology as shown in Fig. 3.15. The simulations take into account the effects of finite gain and bandwidth in the opamps. The results further verify the advantages of the MPSPTI topology over the SPTI when finite opamp gain and bandwidth are considered.

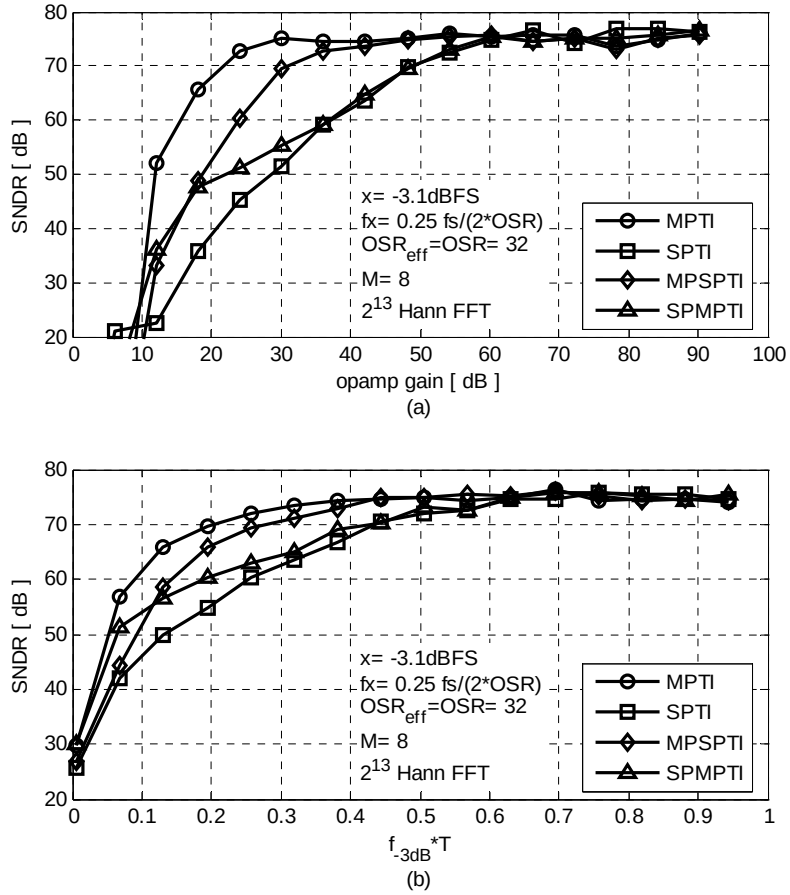

Fig. 3.15: SNDR versus (a) opamp gain (b) normalized bandwidth

The second stage integrator opamp has 5% less gain and bandwidth than those in the first stage. In addition, a 2% mismatch between the two paths in the second stage of the SPMPTI modulator is considered and a unity cross coupling factor is used.

3.5 Calibration of the SPTI ΔΣ Modulator

It is desirable to relax the constraints imposed on the circuits of the SPTI modulator. Calibration can be used to achieve this goal. However, calibration in the analog domain is needed to match the two analog NTFs. Analog domain calibration is less attractive than their digital counterpart especially in the nano-scale CMOS technology. In this section, a partial calibration scheme is investigated to decrease but not eliminate the difference between the NTFs. The main goal of this calibration is to operate in the digital domain. For this purpose, the linearized model of the SPTI modulator is shown in Fig. 3.16 with integrator gain errors (a and c) and phase errors (b and d). Also, two digital filters H_1 and H_2 are inserted after the quantizers for calibration purposes. The

modulator has three inputs and two outputs (before the mux), therefore, six transfer functions. The non-ideal transfer functions due to gain and phase errors relating the inputs and outputs are summarized in Table 3.1. The ideal transfer functions are also included.

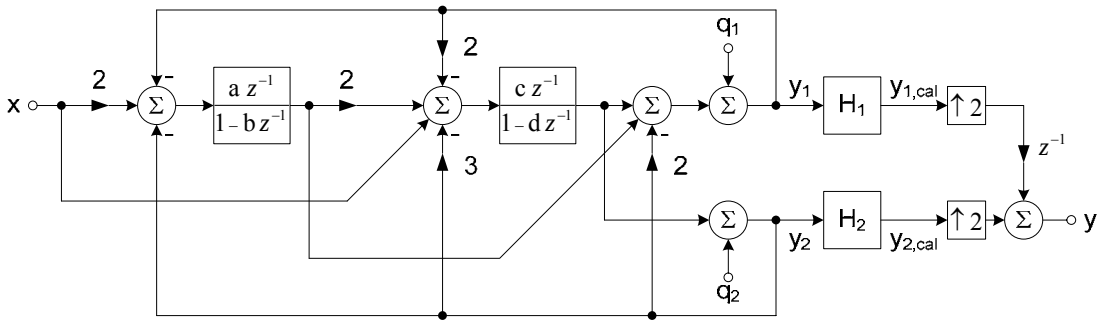

Fig. 3.16: SPTI modulator linearized model with gain and phase errors

Table 3.1: Non-ideal and ideal transfer functions of the SPTI modulator

With gain and phase error	Ideal (a=b=c=d=1)
$\frac{y_1}{x} = \frac{(2a\text{-}c)z + (\text{-}2ad\text{+}ac\text{+}cb)}{(b\text{-}a\text{-}z)(d\text{-}c\text{-}z)}$	$\frac{y_1}{x} = \frac{1}{z}$
$\frac{y_1}{q_1} = \frac{z^2\text{+}(3c\text{-}b\text{-}d)z\text{+}(2ac\text{-}3cb\text{+}bd)}{(b\text{-}a\text{-}z)(d\text{-}c\text{-}z)}$	$\frac{y_1}{q_1} = \frac{z^2+z}{z^2}$
$\frac{y_1}{q_2} = \frac{\text{-}2z^2\text{+}(\text{-}a\text{-}3c\text{+}2b\text{+}2d)z\text{+}(ad\text{-}2ac\text{+}3cb\text{-}2bd)}{(b\text{-}a\text{-}z)(d\text{-}c\text{-}z)}$	$\frac{y_1}{q_2} = -2$
$\frac{y_2}{x} = \frac{\text{-}c}{(d-c-z)}$	$\frac{y_2}{x} = \frac{1}{z}$
$\frac{y_2}{q_1} = \frac{2c}{(d-c-z)}$	$\frac{y_2}{q_1} = -\frac{2}{z}$
$\frac{y_2}{q_2} = \frac{\text{-}2c+d\text{-}z}{(d-c-z)}$	$\frac{y_2}{q_2} = \frac{1+z}{z}$

The objective is to find the two digital transfer functions H_1 and H_2 such that the outputs $y_{1,cal}$ and $y_{2,cal}$ are equal to their ideal values in Table 3.1. Unfortunately, since y_1 and y_2 are functions of three inputs x, q_1, and q_2, it is not possible to compensate for all of them. However, as stated earlier and illustrated in Fig. 3.11, NTF_2 is worse than NTF_1 with respect to its ideal behavior. Since NTF_2 is the transfer function of the final output as a function of q_2, the calibration should attempt to reduce the error in y_1 and y_2 due to q_2. Therefore, if H_1 and H_2 are chosen to be the ideal transfer function of y_1 and y_2 with respect to q_2 divided by the non-ideal one:

$$H_1 = -2 \Big/ \frac{-2z^2+(-a-3c+2b+2d)z+(ad-2ac+3cb-2bd)}{(b-a-z)(d-c-z)}$$

$$H_2 = \frac{1+z}{z} \Big/ \frac{-2c+d-z}{(d-c-z)}$$

the errors in $y_{1,cal}$ and $y_{2,cal}$ due to the non-idealities in the q_2 transfer functions are eliminated.

Matlab and Simulink were used to evaluate the calibration scheme. As shown in Fig. 3.17, calibration reduces the opamp requirements significantly. The bandwidth requirement is similar to the MPTI and the gain requirement is slightly larger than the MPTI. In addition, the SPTI modulator does not suffer from the offset problem of the MPTI and uses fewer opamps.

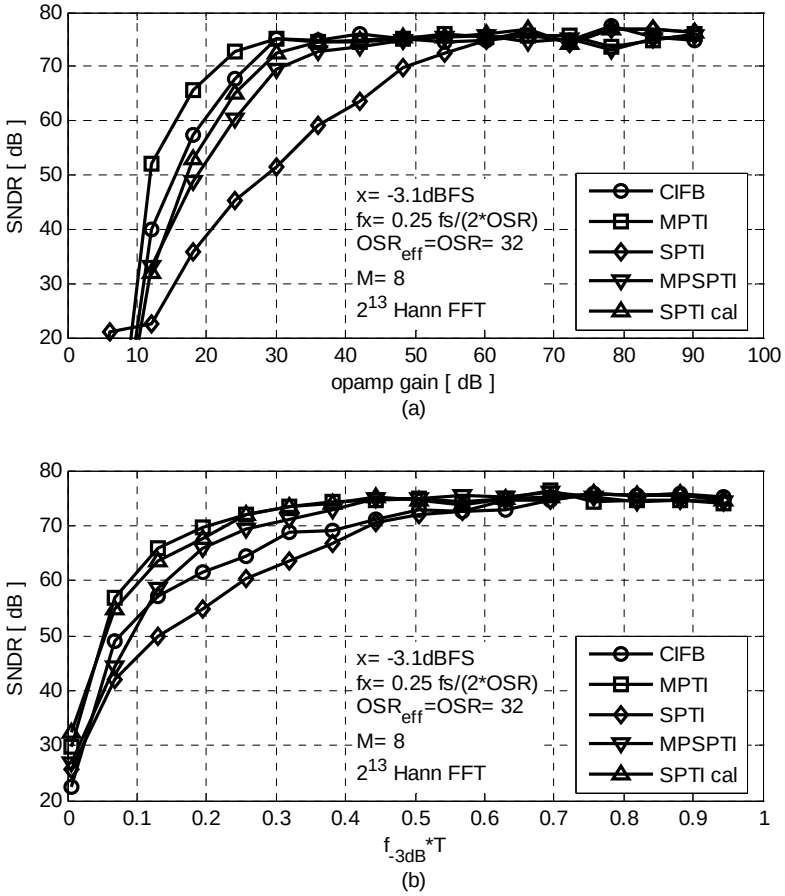

Fig. 3.17: SNDR versus (a) opamp gain (b) normalized bandwidth

A sample output spectrum with non-ideal opamps for the SPTI and the calibrated SPTI are shown in Fig. 3.18. The first integrator in the modulator has 50 dB opamp gain and a closed

loop bandwidth of 0.4/T, furthermore, the second integrator has 5% less gain and bandwidth than the first one.

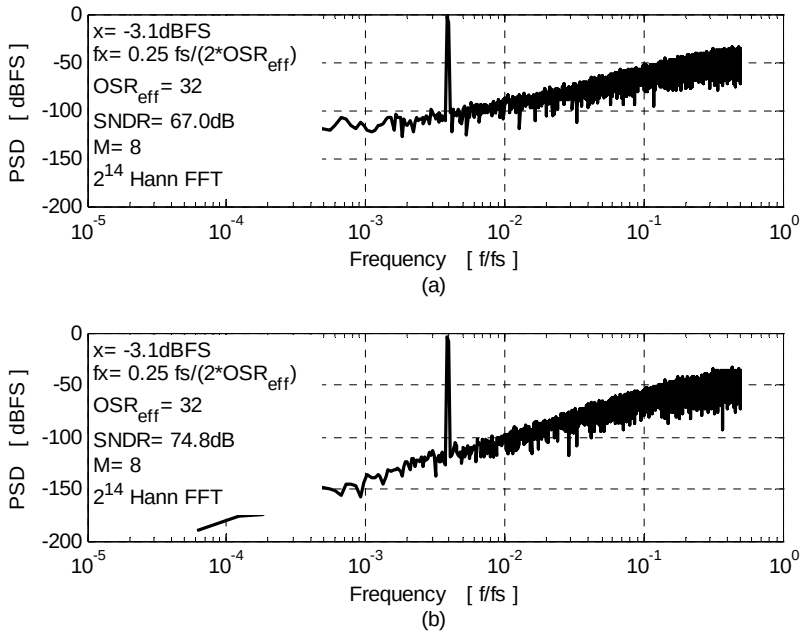

Fig. 3.18: Sample output spectrum (a) without calibration (b) with calibration

Calibration can be carried out in the background. A possible background calibration scheme is to inject a pseudo-random signal at the input of the second quantizer (q_2) [17]. The correlation between the output signals (y_1 and y_2) and the pseudo-random input is measured. An adaptive algorithm is used to modify the coefficients of digital filters such that the power of the pseudo-random signal is minimized at the outputs (y_1 and y_2). The modified digital filters represent the non-ideal transfer functions y_1/q_2 and y_2/q_2, which can be used in the calibration filters.

3.6 Mismatch Shaping for Multi-Bit DAC in SPTI ΔΣ Modulator

Unit element mismatch in multi-bit DACs is inevitable. Therefore, dealing with the mismatches in high resolution multi-bit modulators is critical. *Dynamic element matching* (DEM) is the most common method to achieve DAC linearization for high speed ΔΣ modulators [18] and one DEM approach is *Data weighted averaging* (DWA). For an interleaving factor of 2, the SPTI modulator has two feedback paths feeding into the input as shown in Fig. 3.9. Therefore, two DWA circuits are needed. Unfortunately, using two DACs and two DWA circuits degrades the SNR as shown in Fig. 3.19a. An intuitive explanation for the cause of the problem can be stated as follows:

DWA causes each DAC element to be used equally. Therefore, the effective unit capacitor size is simply the average of all the unit elements. Since there are two DACs feeding into each integrator of the SPTI modulator, a mismatch between the averages of the unit elements in the two DACs degrades the SNR.

The problem can be solved by adding the two feedback signals in the digital domain and feeding the sum back to the integrator through a finer resolution single DAC. Moving the addition from the analog to the digital domain can be done for all or some of the integrators, however, it is essential for the first integrator. Fig. 3.20 shows a second-order SPTI modulator with digital domain addition of the feedback signal in the first integrator only. Assuming that the DAC reference voltages are the same (i.e., the step size is smaller for the increased number of levels), the coefficient for the feedback path is 2. Fig. 3.19b shows a sample output spectrum for the SPTI with a single feedback path which achieves the ideal SNDR. The disadvantage of the addition in the digital domain is that the DWA has to process twice the number of levels, increasing the latency in the DWA block.

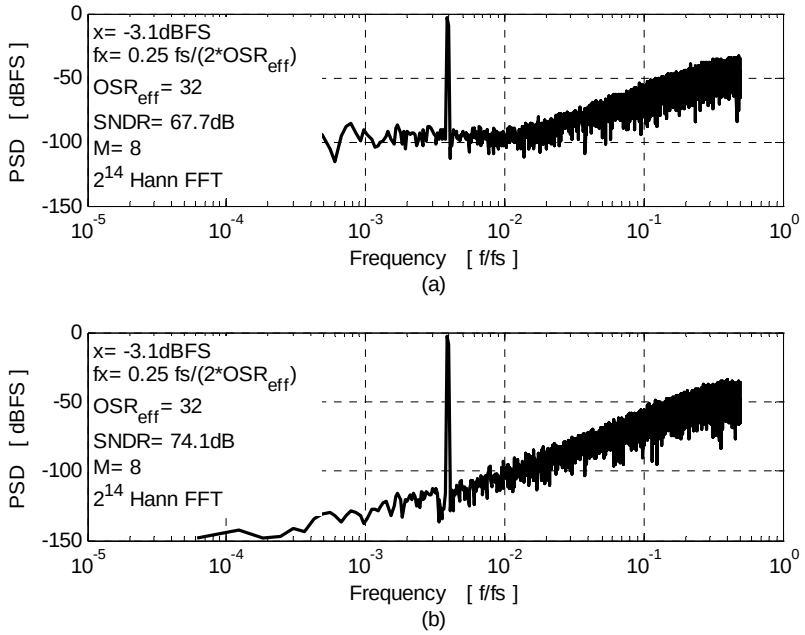

Fig. 3.19: Sample output spectrum with σ=0.5% DAC mismatch (a) two 7-level DWA (b) one 14-level DWA

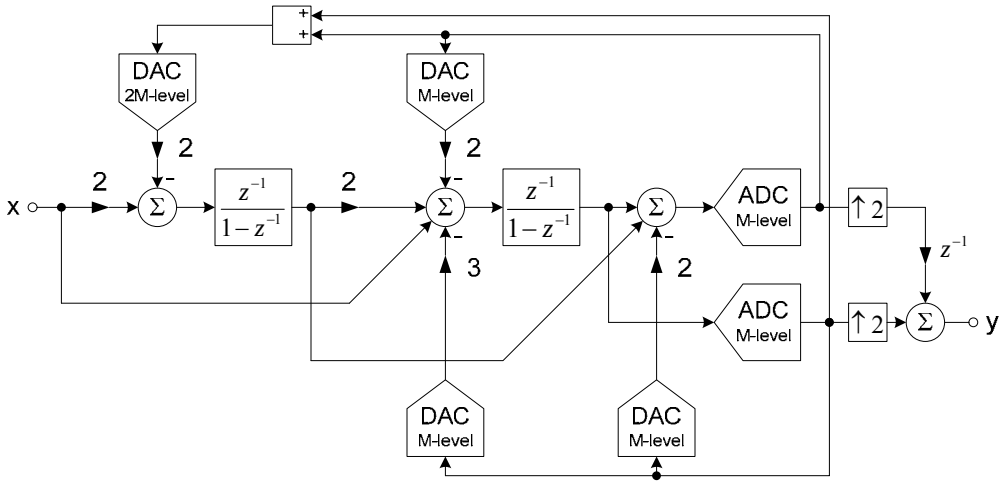

Fig. 3.20: SPTI modulator with digital domain addition of the feedback signal in the first integrator

3.7 Summary

New discrete-time single-path time-interleaved ΔΣ modulators are derived. The SPTI modulator does not suffer from the DC offset problem as the multi-path time-interleaved ΔΣ modulator. On the other hand, the SPTI requires good matching between the NTFs seen by the quantizers. The NTF mismatch is a significant limitation on the achievable performance of the modulator. To mitigate the problem, the first stage of the modulator can use multi-path of integrators while the later stages can use a single path. Alternatively, a digital-calibration technique is proposed to alleviate the NTF mismatch problem. With calibration, the SPTI ΔΣ modulator can operate faster than the single-loop ΔΣ modulator.

Appendix A: A Mathematical Approach for the SPTI Derivation

In this appendix, a systematic mathematical method is presented to derive the SPTI discrete-time ΔΣ modulator. The derivation method is based on the procedure presented in [12]. A first-order CIFB ΔΣ modulator shown in Fig. A.1 is used to illustrate the derivation steps. Note that the integrator is expanded to clearly show the internal states. Also, an interleaving factor of 2 is used in the derivation.

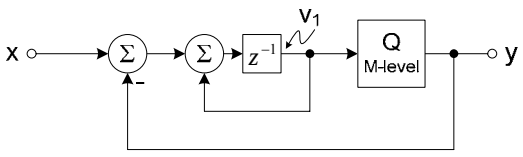

Fig. A.1: First-order CIFB ΔΣ modulator

Step 1: The difference equations describing the first-order CIFB ΔΣ modulator (shown in Fig. A.1) are found:

$$v_1(n) = x(n-1) - y(n-1) + v_1(n-1)$$
$$y(n) = Q[v_1(n)]$$

where Q[ ] is the quantization operation. Since an interleaving factor of 2 is desired, two consecutive iterations of the difference equations are required. The first is generated by replacing the index (n) with (2n) and the second is generated by replacing the index (n) with (2n+1), therefore:

$$\text{Iteration 1:}$$
$$v_1(2n) = x(2n-1) - y(2n-1) + v_1(2n-1)$$
$$y(2n) = Q[v_1(2n)]$$
$$\text{Iteration 2:}$$
$$v_1(2n+1) = x(2n) - y(2n) + v_1(2n)$$
$$y(2n+1) = Q[v_1(2n+1)]$$

Step 2: New labels for the input, outputs, quantizers, and states are defined to simplify the two iterations:

$$x_{1\_2}(n) = x(2n) = x(2n-1)$$
$$v_{1,1}(n) = v_1(2n)$$
$$v_{1,2}(n) = v_1(2n-1)$$
$$y_1(n) = y(2n)$$
$$y_2(n) = y(2n-1)$$

Note that the first label describing the input signal implies the removal of the input demux since both iterations are using the same input. Next, the new labels are substituted back into the difference equations describing the two iterations:

$$\text{Iteration 1:}$$
$$v_{1,1}(n) = x_{1\_2}(n) - y_2(n) + v_{1,2}(n)$$
$$y_1(n) = Q[v_{1,1}(n)]$$
$$\text{Iteration 2:}$$
$$v_{1,2}(n+1) = x_{1\_2}(n) - y_1(n) + v_{1,1}(n)$$
$$y_2(n+1) = Q[v_{1,2}(n+1)]$$

Step 3: The equations are rewritten to describe a single time period:

Iteration 1:

$$v_{1,1}(n) = x_{1\_2}(n) - y_2(n) + v_{1,2}(n)$$
$$y_1(n) = Q\left[v_{1,1}(n)\right]$$

Iteration 2:

$$v_{1,2}(n) = x_{1\_2}(n-1) - y_1(n-1) + v_{1,1}(n-1)$$
$$y_2(n) = Q\left[v_{1,2}(n)\right]$$

Step 4: The equations derived in the previous step include two states for the first-order time-interleaved modulator with an interleaving factor of 2 and no demux at the input. For the single path modulator, only one state is required. Therefore, one state is eliminated from the equations. This means that there are two possible solutions: the first is for $v_{1,2}$ ($v_{1,1}$ is eliminated) and the second is for $v_{1,1}$ ($v_{1,2}$ is eliminated).

For the first case, substitute $v_{1,1}$ into y_1 and $v_{1,2}$, the resulting state and modulator outputs can be derived:

$$v_{1,2}(n) - v_{1,2}(n-1) = 2x_{1\_2}(n-1) - y_1(n-1) - y_2(n-1)$$
$$y_1(n) = Q\left[x_{1\_2}(n) - y_2(n) + v_{1,2}(n)\right]$$
$$y_2(n) = Q\left[v_{1,2}(n)\right]$$

Then, using the z-transform, the following results are obtained:

$$v_{1,2} = \frac{z^{-1}}{1-z^{-1}}\left(2x_{1\_2} - y_1 - y_2\right)$$
$$y_1 = Q\left[x_{1\_2} - y_2 + v_{1,2}\right]$$
$$y_2 = Q\left[v_{1,2}\right]$$

The block diagram that describes the above equations can be easily derived and is shown in Fig. A.2.

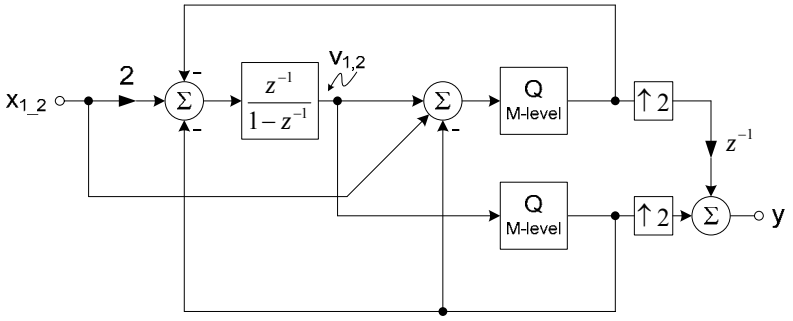

Fig. A.2: First-order time-interleaved by 2 SPTI ΔΣ modulator

For the second case, the resulting state and modulator outputs can be derived. Then, using the z-transform, the following results are obtained:

$$v_{1,1} = \frac{1}{1-z^{-1}}\left(\left(1+z^{-1}\right)x_{1\_2} - z^{-1}y_1 - y_2\right)$$
$$y_1 = Q\left[v_{1,1}\right]$$
$$y_2 = Q\left[z^{-1}\left(x_{1\_2} - y_1 + v_{1,1}\right)\right]$$

The block diagram that describes the above equations can be easily derived and is shown in Fig. A.3.

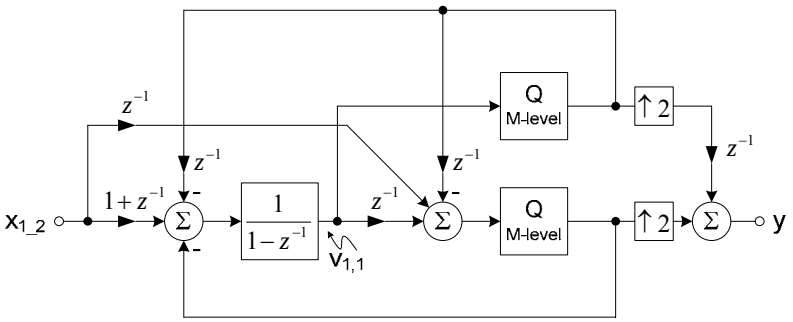

Fig. A.3: First-order time-interleaved by 2 SPTI ΔΣ modulator

Chapter 4:

Input-Feedforward ΔΣ Modulators

THE input-feedforward principle is discussed in Chapter 2 as a method to overcome some of the limitations of the classical architectures. It is shown that its main advantage is removing the input-signal component from the loop filter which relaxes the analog requirements. The delay-free path it introduced into the modulator is pointed out as its main disadvantage. In this chapter, a more detailed treatment of the input-feedforward principle is provided. Furthermore, its drawbacks are analyzed and possible solutions are proposed. Specifically, the double-sampled input concept is proposed to overcome the timing issue. Also, the disadvantage of the adder at the quantizer input is discussed and the capacitive input-feedforward is proposed as a method to overcome the problem.

Up to this point, all input-feedforward architectures can be classified as analog input-feedforward since the implementation is done completely in the analog domain. More advanced input-feedforward architectures including mixed-mode and digital input-feedforward are discussed in this chapter.

The outline of this chapter is as follows: Section 4.1 analyzes the input-feedforward architecture and proposes solutions to overcome their limitations. Section 4.2 introduces the proposed digital input-feedforward modulator.

4.1 Input-Feedforward ΔΣ Modulators

The input-feedforward path in ΔΣ modulators relaxes the requirements of the analog blocks [2]. It is illustrated in Fig. 4.1 for a general loop filter H(z).

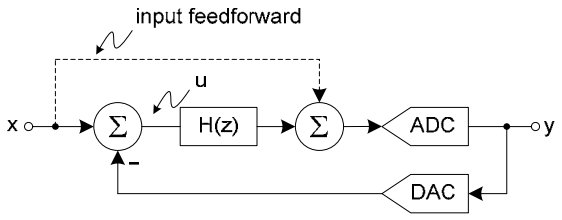

Fig. 4.1: General input-feedforward ΔΣ modulator

Analysis of the linearized system shows that the ΔΣ modulator with the input-feedforward path has the following STF and NTF assuming an ideal DAC:

$$STF = \frac{y}{x} = 1 \tag{4-1}$$

$$NTF = \frac{y}{q} = \frac{1}{1 + H(z)} \tag{4-2}$$

where q is the quantization noise from the ADC. Also, the input to the loop filter is:

$$u = -\frac{1}{1 + H(z)} q \tag{4-3}$$

Note that the loop filter H(z) has to process the quantization noise only. On the other hand, without the input-feedforward, the loop filter has to process the quantization noise in addition to the input signal. The removal of the input signal component reduces the swing at the internal nodes of the modulator which relaxes the headroom requirements, and allows for more efficient opamp architectures to be used. Also, distortion becomes independent of the input signal, which relaxes linearity requirements [2]. However, the input-feedforward path presents a couple of complications, namely the reduced processing time and the analog adder at the quantizer input.

In the ΔΣ modulator without the input-feedforward path, the input-signal and the quantization noise are processed by the loop filter and feed to the quantizer. On the other hand, the input feedforward path provides an alternate route for the input-signal. The processed quantization noise and the input-signal are then added just before the quantizer. Therefore, the quantizer input for both cases are similar. Furthermore, the loop filter is exactly the same for both cases. Therefore, there is no inherent tradeoff between distortion and noise performance in the modulator. The adder at the quantizer input adds thermal noise into the loop. However, noise injected at this point is greatly attenuated when referred back to the input and is therefore insignificant.

4.1.1 Input-feedforward timing issues

The input-feedforward path imposes a timing constraint that complicates its implementation, especially for high speed multi-bit modulators [20] and [21]. The constraint is due to the delay-free loop starting from the input, through the input-feedforward path to the quantizer, and finally through the DAC back to the input of the loop filter. Although it is still possible to implement using switched-capacitor circuits [2], it limits the speed of the modulator. The problem becomes worse with the use of a multi-bit quantizer with DEM algorithms. To understand where the speed

limitation comes from, a typical first-order switched-capacitor ΔΣ modulator implementation (without input-feedforward) and its timing diagram are shown in Fig. 4.2.

Also, a typical first-order switched-capacitor ΔΣ modulator implementation with input-feedforward and its timing diagram are shown in Fig. 4.3. The figure references a process operation which refers to the subtraction and integration functions in the modulator, this can not start before the beginning of phase 2. This is not explicitly indicated in the timing diagram to emphasize the fact that quantization, DEM, and DAC can extend into phase 2.

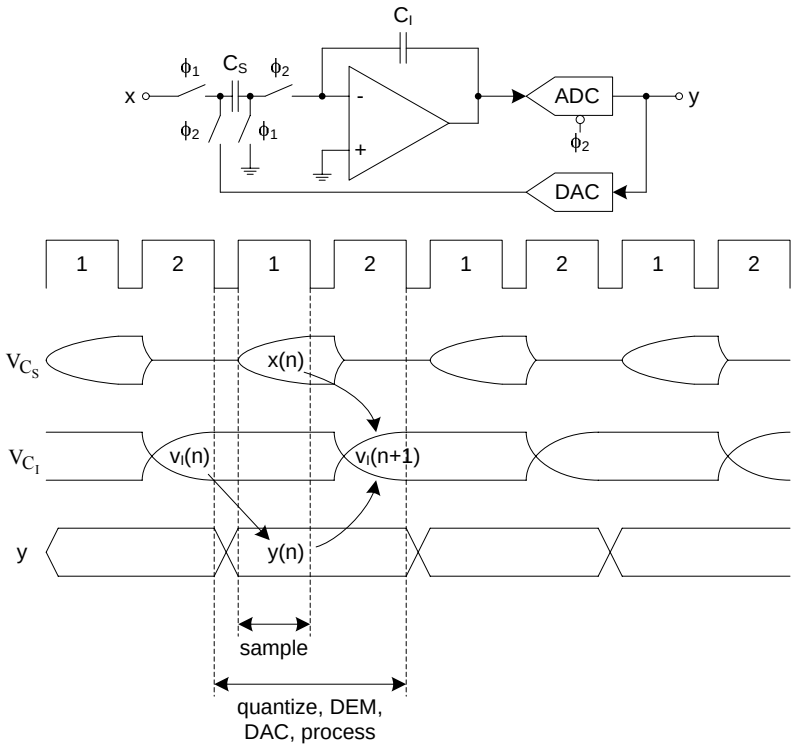

Fig. 4.2: A first-order switched-capacitor ΔΣ modulator without input-feedforward and its timing diagram

Without input-feedforward, the quantizer only needs $v_I(n)$ to generate the output y(n), where $v_I(n)$ is the voltage at the integrator output. Since $v_I(n)$ is available at the end of the previous ϕ_2 and held by the integrator throughout ϕ_1, there is an entire phase (ϕ_1) to perform quantization, DEM, and DAC. Therefore, the entire ϕ_2 can be allocated for the integrator to settle to the required accuracy as shown in Fig. 4.2.

On the other hand, with input-feedforward, the quantizer needs $v_I(n)$ and x(n) to generate y(n), where y(n) is needed during the same period by the integrator. Since x(n) is only available at the end of ϕ_1, there is about one phase to perform quantization, DEM, DAC, and processing as

shown in Fig. 4.3. This reduces the time available for the opamp to settle to the required accuracy. For example, consider a ΔΣ modulator with a 4-bit internal quantizer and 100 MHz sampling frequency. This gives the input-feedforward modulator about 5ns to perform quantization, DEM, DAC, and processing. Most high speed ΔΣ modulators utilize data weighted averaging (DWA) to linearize their DAC [18]. Also, a well designed DWA only adds a shifter into the modulator loop; and the pointer update logic is done outside the loop [22]. A typical 4-bit barrel shifter in 0.18μm CMOS technology requires 0.9ns. Therefore, DWA alone requires about 20% of the available time, implying the opamp requires more power to settle to the same accuracy.

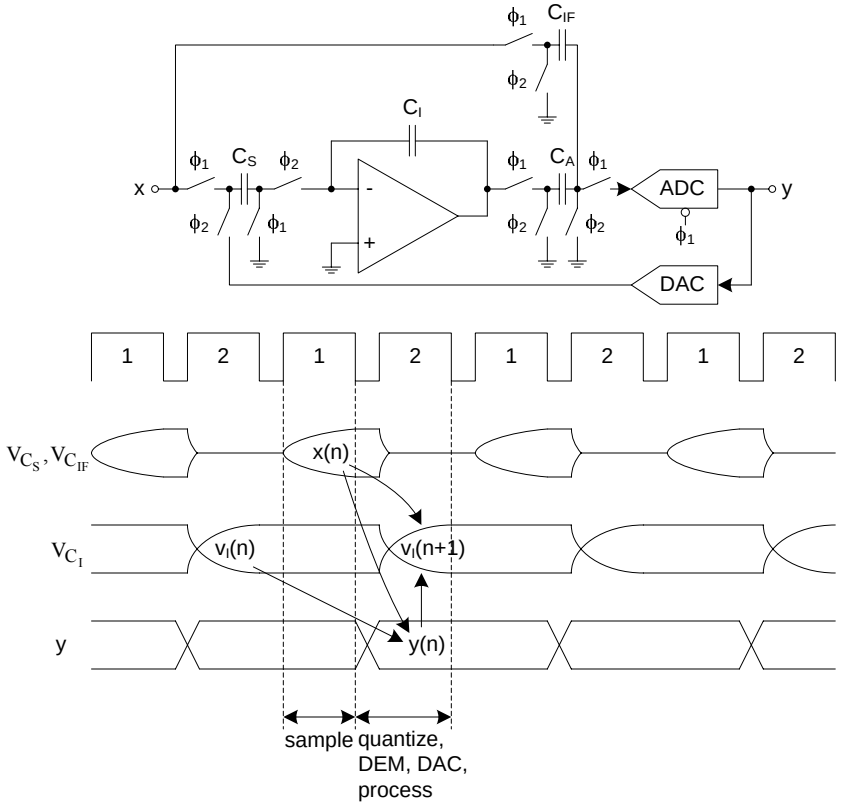

Fig. 4.3: A first-order switched-capacitor ΔΣ modulator with input-feedforward and its timing diagram

One method to relax the timing constraint is to sample the input on the feedforward capacitor C_{IF} one phase earlier than the sampling capacitor C_S. Therefore, the quantizer inputs are available at the end of the previous ϕ_2. This gives the topology of Fig. 4.3 a full period to perform the required operations just like the topology of Fig. 4.2. Mathematically, sampling C_{IF} one phase earlier than C_S is equivalent to multiplying the feedforward coefficient by half a unit delay. To

investigate the effect of this delay on the modulator, the linearized system of Fig. 4.1 (with $z^{-1/2}$ in the feedforward path) for a pure differentiator type NTF of order L is used, and the analysis reveals the following results:

$$\begin{aligned} H(z) &= NTF^{-1} - 1 \\ &= \left(1 - z^{-1}\right)^{-L} - 1 \end{aligned} \tag{4-4}$$

$$\begin{aligned} y &= \left(1 - \left(1 - z^{-1/2}\right) NTF\right) x + NTF\ q \\ &= \left(1 - \left(1 - z^{-1/2}\right)\left(1 - z^{-1}\right)^{L}\right) x + \left(1 - z^{-1}\right)^{L}\ q \end{aligned} \tag{4-5}$$

$$\begin{aligned} u &= \left(\left(1 - z^{-1/2}\right) NTF\right) x - NTF\ q \\ &= \left(\left(1 - z^{-1/2}\right)\left(1 - z^{-1}\right)^{L}\right) x - \left(1 - z^{-1}\right)^{L}\ q \end{aligned} \tag{4-6}$$

There are two important observations: there is a signal component at the input of the loop filter and the STF is modified. The input signal component into the loop filter is noise shaped. Therefore, the signal component at the output of the integrators is small and usually not a problem. This means that headroom and linearity requirements are still relaxed. The modified STF has a unity gain at DC and larger gain at half the sampling frequency. The high frequency boost makes this solution undesirable because it represents a potential instability problem.

4.1.2 Relaxed timing input-feedforward architecture

To relax the timing constraint presented by the input-feedforward path, it is desirable to extend the time available for quantization, DEM, and DAC. A method to accomplish this is to sample the input one phase earlier than required, hold it for another phase, and process it during the third phase [23] and [21]. During the holding phase, the quantizer can be strobed since both inputs x(n) and $v_I(n)$ are available for the duration of the phase. The process implies that the sampling capacitor is busy for three phases; on the other hand, one sample must be taken per period. This conflict can be resolved by introducing another sampling capacitor. Effectively, there are two sampling capacitors and each one samples the input once every two periods. One capacitor (C_{S1}) samples during odd phases (ϕ_{1o}) and another capacitor (C_{S2}) samples during even phases (ϕ_{1e}) as shown in Fig. 4.4. Note that the process (subtract and integrate) operation can not start before the beginning of phase 1.

The cost of the proposed solution is an increase in area due to the second sampling capacitor. The proposed implementation in Fig. 4.4 uses a separate capacitor (C_{DAC}) to feedback the quantized signal. It is also possible to use the sampling capacitors to feedback the quantized signal as shown in Fig. 4.5. The implementation of Fig. 4.4 allows easy scaling of the feedback

signal relative to the input signal and it draws signal independent current from the voltage reference supply [24]. The implementation of Fig. 4.5 saves power because there is less kT/C noise and a larger feedback factor. Another important issue to consider when comparing the two implementations is the sampling capacitors mismatch.

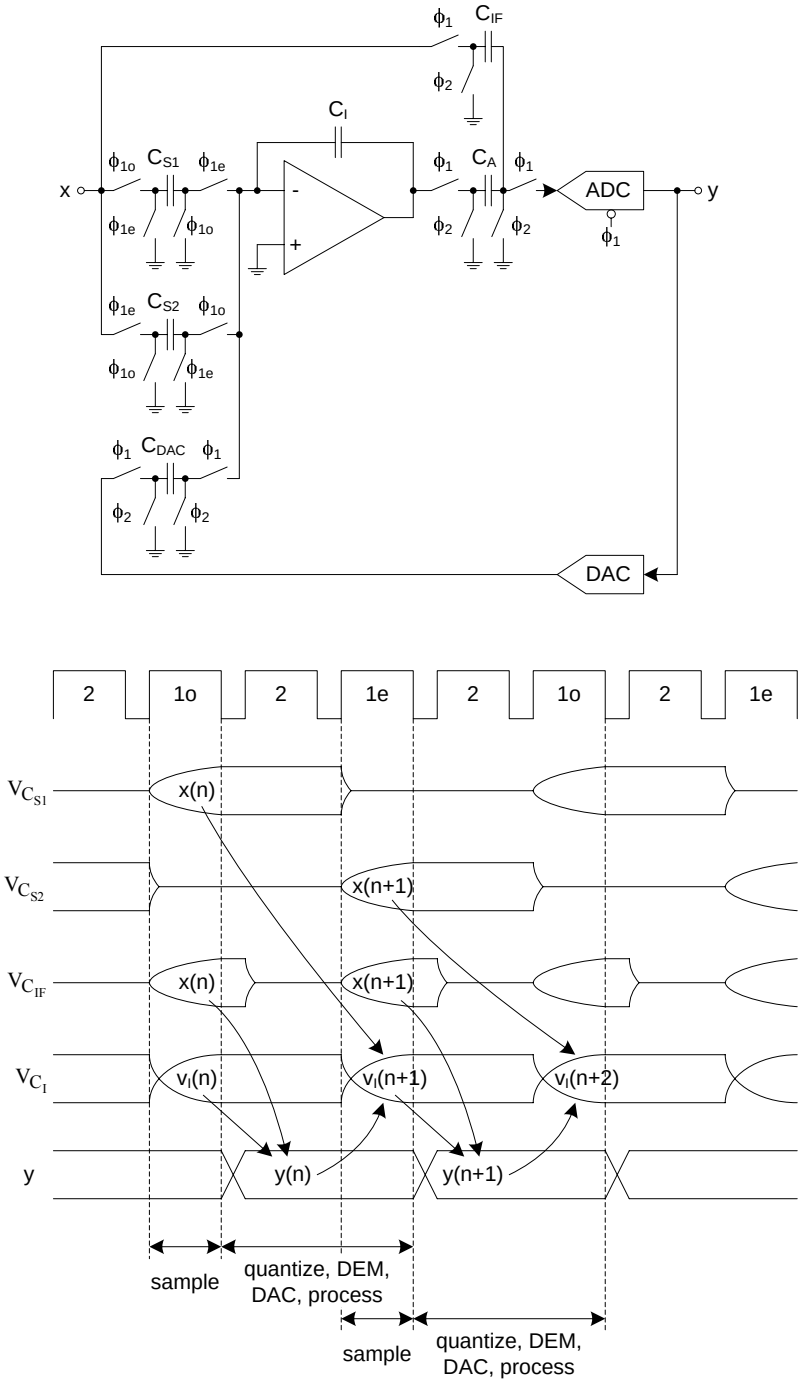

Fig. 4.4: Proposed relaxed timing input-feedforward architecture and its timing diagram

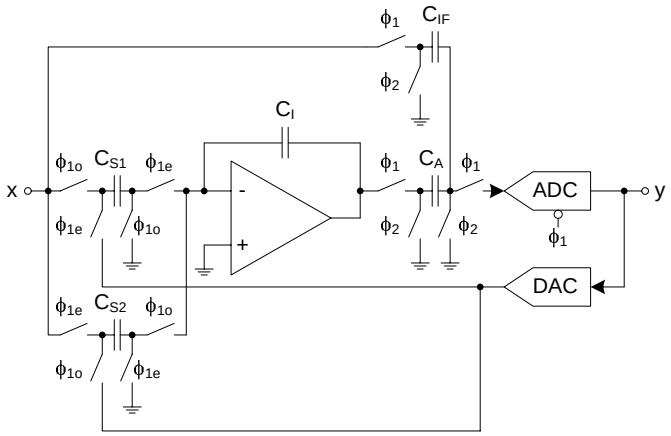

Fig. 4.5: Relaxed timing input-feedforward architecture using only the sampling capacitors

The mismatch issue is investigated using ideal building blocks in Spectre and the simulations do not include thermal noise. A third-order input-feedforward ΔΣ modulator with a 3-bit internal quantizer and an OSR of 64 is used for the investigation. The traditional implementation (Fig. 4.3) achieves a SNR of 119 dB but as mentioned above, has a difficult timing requirement. With ideal capacitor matching, the implementations of Fig. 4.4 and Fig. 4.5 also both achieve 119 dB performance but have much relaxed timing requirements. However, when capacitor mismatch of 0.1% is introduced, the implementation of Fig. 4.4 maintains a performance of 118 dB while that of Fig. 4.5 reduces significantly to only 81 dB. The reason for the large degradation in SNR for the circuit of Fig. 4.5 is due to large out-of-band quantization noise near fs/2 being aliased back in band which is a similar problem that occurs in double sampled modulators [25]. This effect does not occur in the circuit of Fig. 4.4 since only the input signal is double sampled and the input signal likely has little signal energy near fs/2. However, since the circuit of Fig. 4.5 does have better kT/C noise performance than that of Fig. 4.4, if one chooses to make use of the Fig. 4.5 circuit, the noise folding problem can be mitigated by adding an extra zero at fs/2 into the noise transfer function [26]. In addition, capacitor mismatch in the circuits of Fig. 4.4 and Fig. 4.5 results in an out of band tone to occur near fs/2. Fortunately, this tone is of little consequence as it will be removed by the decimation filter.

4.1.3 Input-feedforward topologies without the adder at the quantizer input

The summation at the quantizer input creates another complication for input-feedforward ΔΣ modulators. The disadvantage is the increased circuit complexity and power dissipation. In some

implementations, this adder is done passively. However this approach reduces the signal level into the quantizer which can also result in a power increase since smaller quantization levels must now be resolved.

The cascade of integrators with distributed feedback topology (CIFB) can be modified to eliminate the adder at the quantizer input [21]. Fig. 4.6 illustrates the proposed *CIFB with capacitive input-feedforward* (CIFB-CIF) as shown for a second-order modulator. The $(1\text{-}z^{-1})$ term in the feedforward path can be implemented by a simple capacitor.

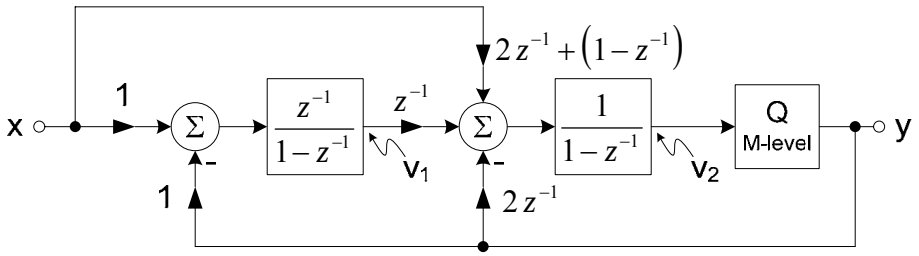

Fig. 4.6: Proposed CIFB-CIF topology

Analysis of the linearized system leads to the following results:

$$STF = \frac{y}{x} = 1 \tag{4-7}$$

$$NTF = \frac{y}{q} = \left(1 - z^{-1}\right)^2 \tag{4-8}$$

$$v_1 = -z^{-1}\left(1 - z^{-1}\right)q \tag{4-9}$$

$$v_2 = x - z^{-1}\left(2 - z^{-1}\right)q \tag{4-10}$$

where q is the quantization noise from the ADC. The STF exhibits an all pass response and the NTF provides a second-order pure differentiator type high pass response. Signal v_1 is free of the input signal while v_2 contains a signal component. Therefore, unlike the CIFB topology, when input-feedforward is used, the output of the second integrator contains input signal. However, any non-idealities at this point are second-order noise shaped when referred back to the input and their effects are less important. The reduced sensitivity to non-idealities in the final integrator is more significant if a higher order modulator is used.

The CIFB-CIF model in Fig. 4.6 can be implemented using switched-capacitor circuits as shown in Fig. 4.7 in the single ended form for simplicity. The negative capacitor can be easily implemented in a fully differential circuit.

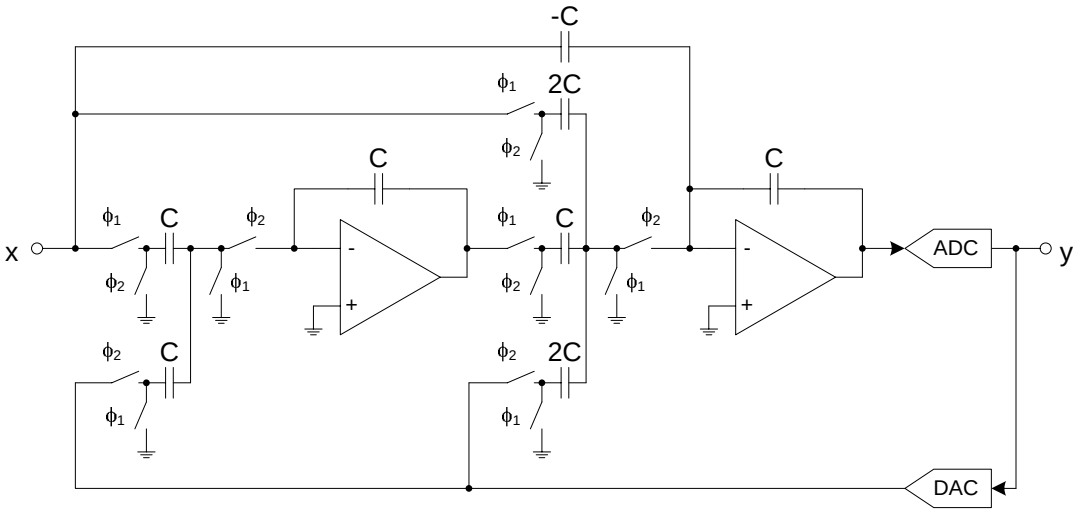

Fig. 4.7: Switched-capacitor implementation of CIFB-CIF

The CIFB-CIF topology is simulated using Matlab and Simulink. A sample output spectrum including opamp third-order distortion in both opamps corresponding to 1% third-order harmonic distortion for a full scale signal is shown in Fig. 4.8. There are no harmonic components in the output spectrum with the input-feedforward path ($2z^{-1}+(1-z^{-1})$) as shown in (a). However, with the input-feedforward path removed, the third harmonic of the signal appears at the output as shown in (b).

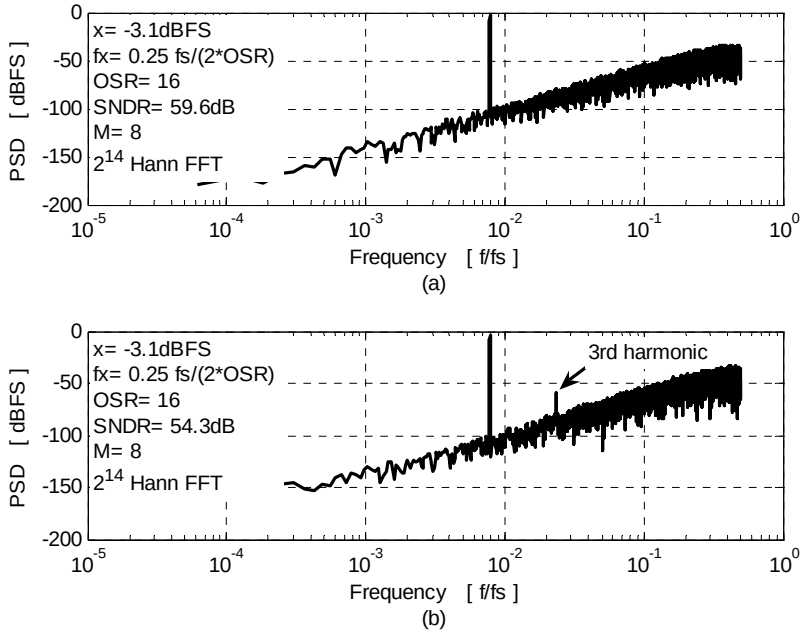

Fig. 4.8: Sample output spectrum (a) with input-feedforward (b) without input-feedforward

The effect of capacitor mismatch in the CIFB-CIF topology is investigated using Monte Carlo analysis in Matlab. Mismatches have the same effect on the SNR for both CIFB and CIFB-CIF topologies. Therefore, the new topology has the same sensitivity to component mismatches as the CIFB.

The input to the quantizer of CIFB-CIF topology is a continuous-time signal (assuming the quantizer is not switched-capacitor based). Therefore, the effect of timing skew between the front-end sampling capacitor and the internal quantizer is investigated. The model of Fig. 4.7 is used in Spectre for the evaluation with an OSR of 16 and an input signal at -3.1dBFS. The effect of the skew is insignificant on the achievable SQNR and the output of the integrators as long as the quantizer is strobed during the sampling phase (ϕ_1). However, if the skew is large enough to move the quantization into the integrating phase, then the SQNR degrades which is the case in any ΔΣ architecture.

The continuous-time nature of the signal at the input of the quantizer in the CIFB-CIF topology does not have an effect on metastability. A metastabile state happens when the latch fails to produce the desired output voltage (ΔV) within a specific time period. Consider a typical regenerative latch shown in Fig. 4.9, the time required for the latch to amplify the initial voltage difference (ΔV_{init}) is given by [27]:

$$t = \frac{\tau_0}{A_0 - 1} \ln\left(\frac{\Delta V}{\Delta V_{init}}\right)$$

This indicates that the only parameter of importance in the input signal is its swing (ΔV_{init}). Therefore, metastability is not affected by the moving signal at the quantizer input.

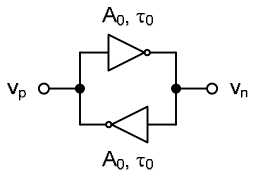

Fig. 4.9: Regenerative latch with back-to-back amplifiers of gain A_0 and time constant τ_0

The capacitive feedforward concept can be extended to the cascade of integrators with weighted feedforward summation topology (CIFF). Unfortunately, the classical CIFF topology requires an adder before the quantizer to perform the weighted feedforward summation. Therefore, using the capacitive feedforward technique is not very helpful. However, a modified CIFF topology that eliminates this adder, except for the input-feedforward adder, was presented

in [18]. The modified *CIFF with capacitive input-feedforward* (CIFF-CIF) is shown for a third-order modulator in Fig. 4.10 [21].

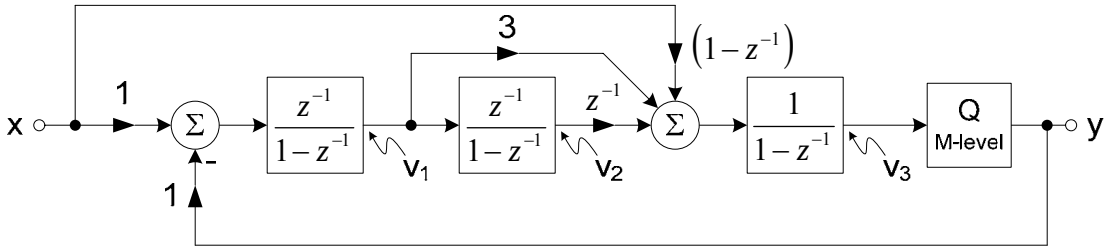

Fig. 4.10: Proposed CIFF CIF topology

The STF exhibits an all pass response and the NTF provides a third-order pure differentiator type high pass response. Signals v_1 and v_2 are free of the input signal while v_3 contains a signal component. As mentioned earlier, non-idealities at the output of the third integrator are unimportant because they are third-order noise shaped when referred back to the input.

4.2 Digital Input-Feedforward ΔΣ Modulators

The input-feedforward structures presented thus far are analog domain implementations, but researchers have been trying to move the input-feedforward path either partially or completely into the digital domain. To the author's knowledge, the first attempt at implementing the input-feedforward path in the digital domain was presented in [28] and is shown in Fig. 4.11.

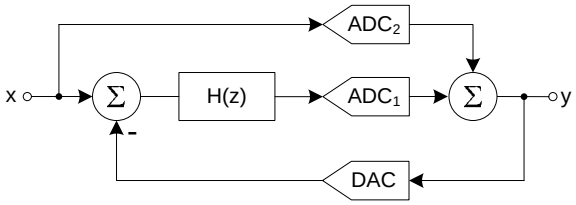

Fig. 4.11: Digital input-feedforward ΔΣ modulator

The objective of this architecture is to eliminate the analog adder at the quantizer input. However, this advantage comes at a great cost. The quantization noise is increased due to the extra quantizer in the feedforward path. The increase in quantization noise reduces the achievable SNDR compared to the analog implementation.

The next attempt was a mixed-mode approach where the input-feedforward path was implemented in both the analog and the digital domains as shown in Fig. 4.12 [29]. This topology

eliminated the adder at the quantizer input without degradation in the SNDR. It achieved this by cancelling the quantization noise from the extra quantizer at the output of the modulator. Another characteristic of the topology is the elimination of the delay-free path; therefore, it does not suffer from the timing constraint presented earlier. However, the elimination of the delay-free path has some consequences. First, the signals at the output of the opamps contain a first-order shaped input-signal component. Although swing and linearity requirements are still relaxed, the existence of the input-signal represents a problem at low OSR. Second, the STF has high frequency boost which is undesirable from a stability standpoint.

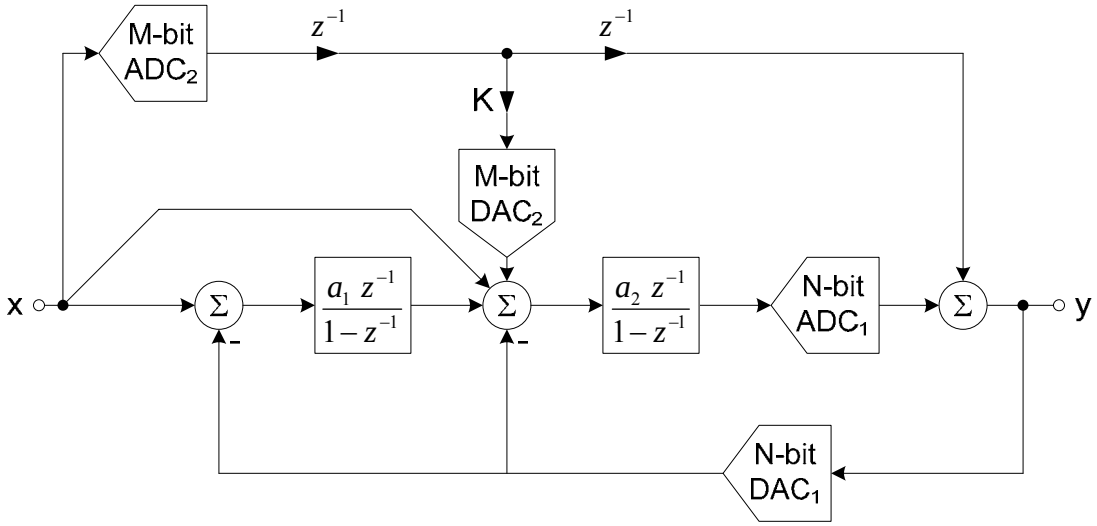

Fig. 4.12: Mixed-mode input-feedforward ΔΣ modulator

Another mixed-mode modulator was presented in [30]. The input-signal component and high frequency boost problems were eliminated at the expense of having a delay-free path.

4.2.1 Digital input-feedforward ΔΣ modulator concept

The proposed *digital input-feedforward* (DIFF) structure is illustrated for a first-order modulator as shown in Fig. 4.13 [31]. The feedforward path (dashed line) consists of an additional quantizer (Q_2) with a reference voltage $V_{ref, Q2}$ which can be different than the main quantizer (Q_1) reference voltage $V_{ref, Q1}$. In addition, the number of quantization levels in Q_2 can be different than that of Q_1.

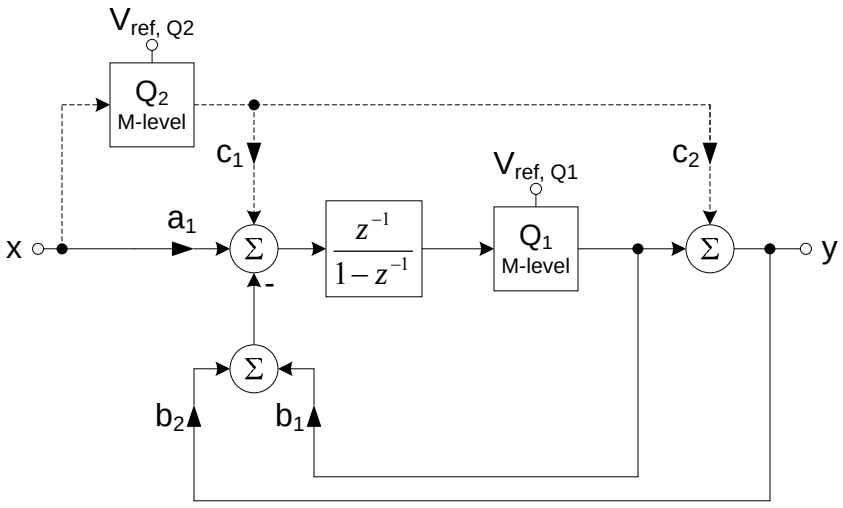

Fig. 4.13: First-order Digital input-feedforward ΔΣ modulator

The modulator can be simplified further as shown in Fig. 4.14. As will be shown shortly, the coefficient values feeding to the integrator are equal; therefore, the signal processing does not involve any multiplications, only additions are required.

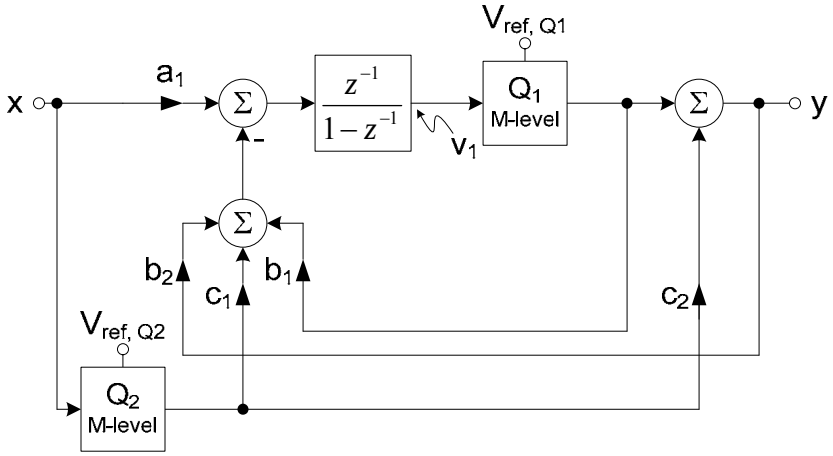

Fig. 4.14: Modified first-order DIFF ΔΣ modulator

The noise transfer function of Q_1 is not affected and is first-order noise shaped. Quantization noise from Q_2 is completely cancelled and does not appear at the output of the modulator, however, it appears at the output of the integrator. The signal at the output of the integrator does not contain any input-signal component, only quantization noise. A linear analysis of the system leads to the following results:

$$y = z^{-1}x + \left(1 - z^{-1}\right)q_1 \tag{4-11}$$

$$v_1 = -z^{-1}q_1 - z^{-1}q_2 \tag{4-12}$$

for the following choice of coefficients: $a_1 = 1, b_1 = 1-\alpha, b_2 = \alpha, c_1 = 1-\alpha\, z^{-1}, c_2 = z^{-1}$, where q_1 is the quantization noise from Q_1, q_2 is the quantization noise from Q_2, and α is a constant. If α is chosen to be zero, the modulator can be simplified further as shown in Fig. 4.15.

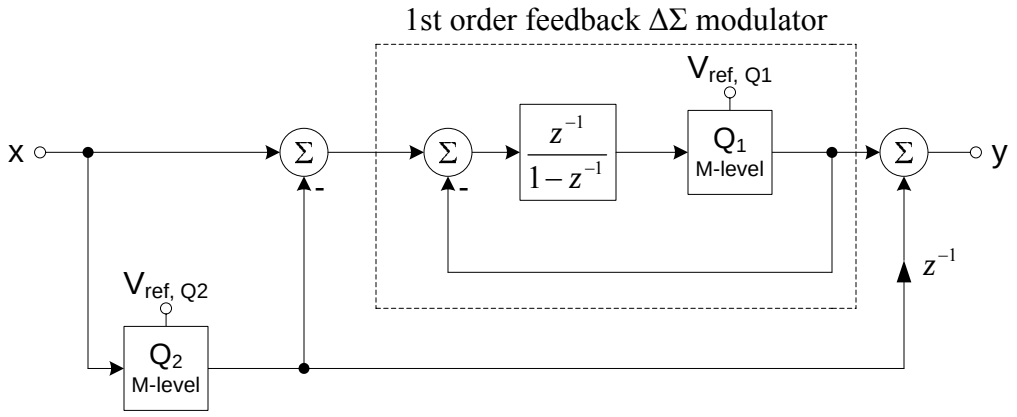

Fig. 4.15: DIFF ΔΣ modulator with the blocks rearranged

4.2.2 Generalized DIFF ΔΣ modulator

A simpler and more general DIFF modulator shown in Fig. 4.16 can be devised by generalizing the structure in Fig. 4.15 [31]. It is interesting to note that the DIFF topology in Fig. 4.16 can be classified as a 0-L MASH.

The simplified DIFF consists of an input stage (Q_2 and a subtractor), a digital filter T(z), and an internal ΔΣ modulator that can be made of any traditional topology. The inter-stage gain factor "a" does not map directly from Fig. 4.15, but it offers another degree of freedom in the design of the DIFF modulator.

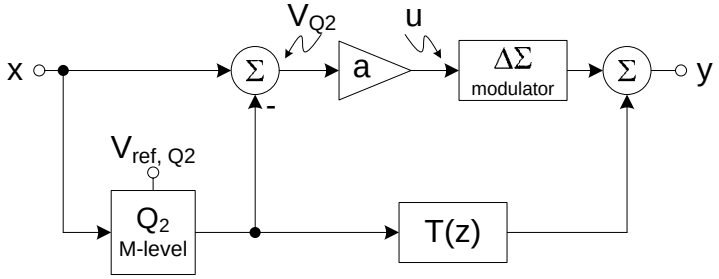

Fig. 4.16: Generalized DIFF ΔΣ modulator

Linear analysis of the generalized DIFF ΔΣ modulator where the quantizers are replaced with additive noise sources leads to the following result:

$$y = T(z)\, x + NTF_{\Delta\Sigma}\, q_1 + \left(T(z) - a\, STF_{\Delta\Sigma}\right) q_2 \tag{4-13}$$

where $STF_{\Delta\Sigma}$ and $NTF_{\Delta\Sigma}$ are the internal ΔΣ modulator transfer functions. Therefore, to cancel q_2 at the output of the modulator, T(z) must equal $\left(a\, STF_{\Delta\Sigma}\right)$, hence:

$$y = a\, STF_{\Delta\Sigma}\, x + NTF_{\Delta\Sigma}\, q_1 \tag{4-14}$$

Since the DIFF modulator works on the principle of noise cancellation, it requires analog-digital matching. The matching can be obtained by making the analog path match the digital path which imposes higher requirements on the analog components. Alternatively, the digital transfer function can be calibrated to match the analog one and hence maintain the relaxed requirements on the analog components.

The characteristics of the input to the internal ΔΣ modulator changes depending on the input-signal level and the external quantizer reference voltage. The internal ΔΣ input can be viewed graphically as shown in Fig. 4.17 for a sinusoidal input and 8 levels in Q_2 and expressed mathematically as:

$$u = \begin{cases} a\, V_{Q2} & x < V_{\text{ref, Q2}} \\ a\left(V_{\text{LSB2}} + \left(x - V_{\text{ref, Q2}}\right)\right) & x \geq V_{\text{ref, Q2}} \end{cases} \tag{4-15}$$

where V_{Q2} in the quantization signal of the first stage. As long as the input-signal does not overload the external quantizer, the input to the ΔΣ is the quantization noise of the first stage. Once the input-signal exceeds $V_{\text{ref, Q2}}$, the signal into the ΔΣ includes an input-signal component.

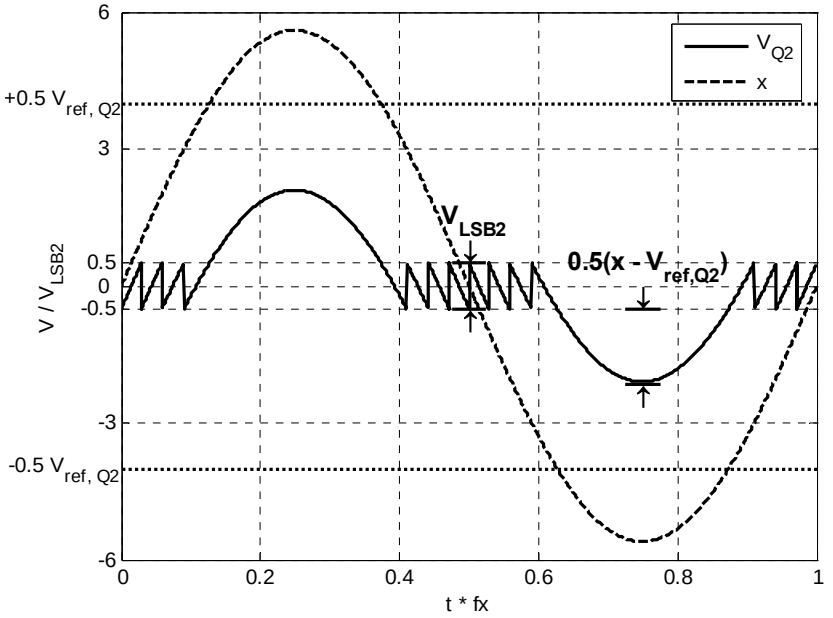

Fig. 4.17: Input and output waveforms of the first stage in the DIFF ΔΣ modulator

Two parameters of the DIFF topology are derived next: the maximum inter-stage gain and the limit of the input-signal level. To determine the inter-stage gain analytically, consider the maximum input into the traditional internal ΔΣ modulator which is given by:

$$u_{\max} = k\, V_{\text{ref, Q1}} \tag{4-16}$$

where k is a constant ranging from 50 to 80% [4] and depends on the loop order and number of bits in the quantizer Q_1. Also, assuming Q_2 is not saturated, the output of the first stage amplified by the inter-stage gain is given by:

$$u = a\, V_{\text{Q2}} \tag{4-17}$$

The maximum value of V_{Q2} is one LSB, therefore, for the maximum quantization voltage, Eq. (4-17) becomes:

$$u_{\max} = a\, V_{\text{LSB2}} = a\, \frac{V_{\text{ref, Q2}}}{M_2} \tag{4-18}$$

From Eqs. (4-16) and (4-18), the maximum inter-stage gain can be determined:

$$a \le k\, \frac{V_{\text{ref, Q1}}}{V_{\text{ref, Q2}}} M_2 \tag{4-19}$$

If the inter-stage gain is set to less than its maximum value, the dynamic range of the internal ΔΣ modulator is not fully utilized. Therefore, the input-signal level can exceed the external quantizer reference. In this case, the maximum input into the internal ΔΣ modulator is given by:

$$\begin{aligned} u_{\max} &= a\left(V_{\text{LSB2}} + \left(x_{\max} - V_{\text{ref, Q2}}\right)\right) \\ &= a\left(\frac{V_{\text{ref, Q2}}}{M_2} + \left(x_{\max} - V_{\text{ref, Q2}}\right)\right) \end{aligned} \tag{4-20}$$

From Eqs. (4-16) and (4-20), the maximum input-signal level is:

$$x_{\max} = k\, \frac{V_{\text{ref, Q1}}}{a} + V_{\text{ref, Q2}}\left(1 - \frac{1}{M_2}\right) \tag{4-21}$$

Eq. 4-21 holds as long as the inter-stage gain is bound by Eq. 4-19.

Consider the following two special cases of Eq. 4-21. First, for maximum inter-stage gain, substituting Eq. 4-19 into Eq. 4-21 yields:

$$x_{\max} = V_{\text{ref, Q2}} \tag{4-22}$$

In other words, with maximum inter-stage gain, the input to the internal ΔΣ modulator is set at the edge of the stable region, hence, the modulator becomes unstable if the external quantizer

saturates. Therefore, the maximum input-signal is limited to the reference of the external quantizer. Furthermore, note that Eq. 4-22 is equal to 4-18 since u_{max} attenuated by the inter-stage gain and amplified by the number of levels in the external quantizer is simply x_{max}.

In the second case, the external quantizer is removed, hence, M_2 becomes unity. Furthermore, removing the external quantizer necessitates setting the inter-stage gain to unity. Eq. 4-21 reduces to:

$$x_{\max} = k\, V_{\text{ref, Q1}}$$

which is equivalent to a traditional ΔΣ modulator as expected.

The advantages of the DIFF ΔΣ modulator are:

- It maintains the low swing and low distortion characteristics of traditional input-feedforward topologies for input-signals limited to $V_{ref,\ Q2}$. These benefits can be maintained after the saturation of the external quantizer if an input-feedforward topology is used for the internal ΔΣ in the DIFF modulator.
- It eliminates the adder at the internal quantizer (Q_1) input which is required for most input feedforward topologies. Therefore, the additional circuitry used to implement the DIFF does not necessarily increase the power consumption and it is simpler to implement.
- It provides an improvement in the achievable SNDR. This is done via the utilization of the inter-stage gain and the appropriate choice of the levels and reference voltage of the external quantizer.

There are two complications with the DIFF ΔΣ modulator:

- The delay-free path from the input through Q_2 back to the input. This path results in a timing problem for high speed modulators. The timing issue is a common characteristic of input-feedforward architectures that achieve complete cancellation of the input-signal component from the loop filter. However, the double sampled input concept presented earlier can be used here to alleviate the problem. In addition, an architectural level solution is presented in section 4.2.4.
- Matching between the analog and the digital domains is required for the quantization noise from the external quantizer to be cancelled at the output. This is not a significant issue for modern CMOS technology where digital calibration is an effective way to achieve the matching.

4.2.3 Evaluation of the DIFF ΔΣ Modulator

There are tradeoffs between the maximum input-signal, the inter-stage gain, the signal swings at the output of the integrators, and the references and number of levels in the quantizers. To illustrate these tradeoffs, a second-order DIFF ΔΣ modulator is used as shown in Fig. 4.18 and compared to a second-order CIFB topology, which is the internal ΔΣ modulator in Fig. 4.18. The following are used for simulations: an OSR of 32, 8 levels in both quantizers, a quantizer reference voltage $V_{ref, Q1} = \pm 0.5 = V_{ref, Q2}$.

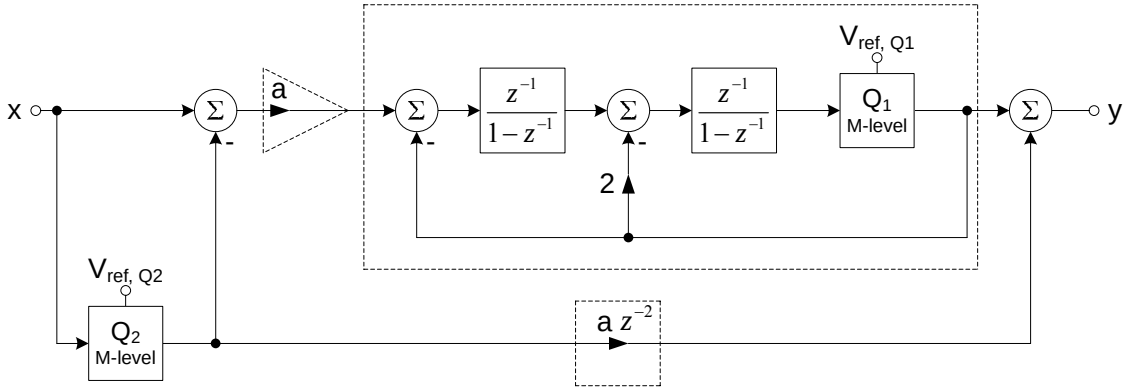

Fig. 4.18: Second-order DIFF ΔΣ modulator

The achievable SNDR versus the input-signal level is shown in Fig. 4.19. The graphs illustrate the improvement in the SNDR of the DIFF ΔΣ modulator over the CIFB topology. For example, with an inter-stage gain of 4, the SNDR improvement is 17 dB at maximum SNDR points. In addition, Fig. 4.19 shows the achievable SNDR for various inter-stage gains for the DIFF ΔΣ. The SNDR is improved as the inter-stage gain is increased for a given input level while the maximum input-signal is decreased. There is a 6 dB improvement in SNDR for every doubling of inter-stage gain. However, larger gain causes the internal quantizer to overload at a smaller input level.

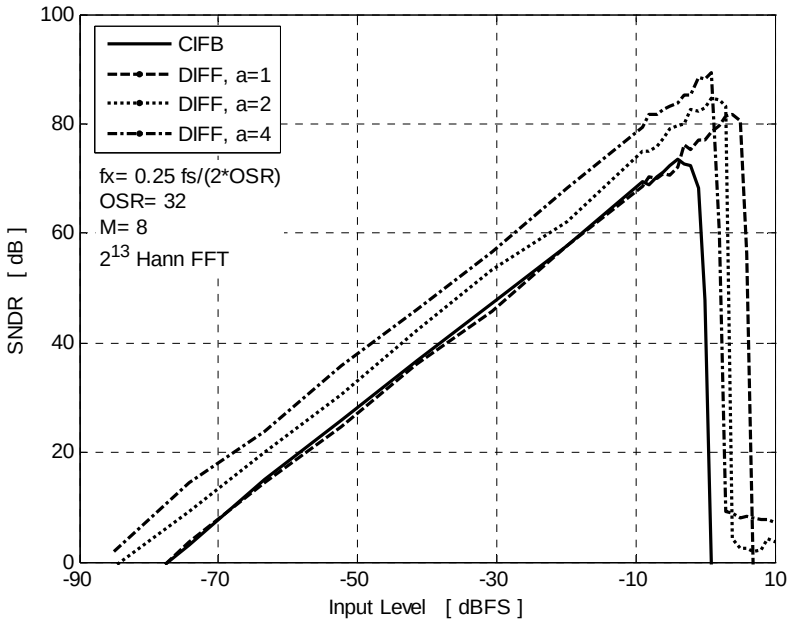

Fig. 4.19 SNDR versus input-signal amplitude for various inter-stage gains

The CIFB ΔΣ states contain input-signal component, therefore, they have a larger swing than the DIFF ΔΣ where only quantization noise is processed as shown in Fig. 4.20 for a sinusoidal input signal which parameters are specified in the figure. The DIFF topology maintains this low swing as long as the external quantizer is not saturated. After Q_2 saturation, the state swing in the DIFF becomes a function of the internal ΔΣ modulator topology. Larger inter-stage gain increases the signal swings at the integrators outputs. Since this signal is still quantization noise only, the linearity requirements are still relaxed.

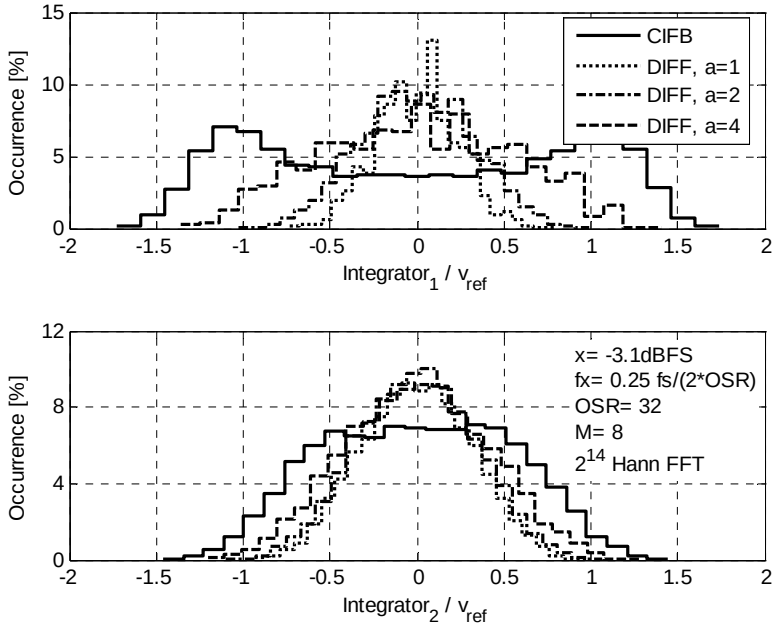

Fig. 4.20: Output probability densities for the first and second integrators with sinusoidal input and for various inter-stage gains

A sample output spectrum of the modulator is illustrated in Fig. 4.21 for unity inter-stage gain before and after overloading the external quantizer (Q_2). The opamp in the simulations has a 70 dB gain and a closed loop bandwidth f_{-3dB} equals twice the sampling frequency $f_{sampling}$. The second stage integrator opamp has 5% less gain and bandwidth than those in the first stage. In addition, third-order distortion in the first integrator and variations of σ=5% in the reference levels of Q_2 are considered.

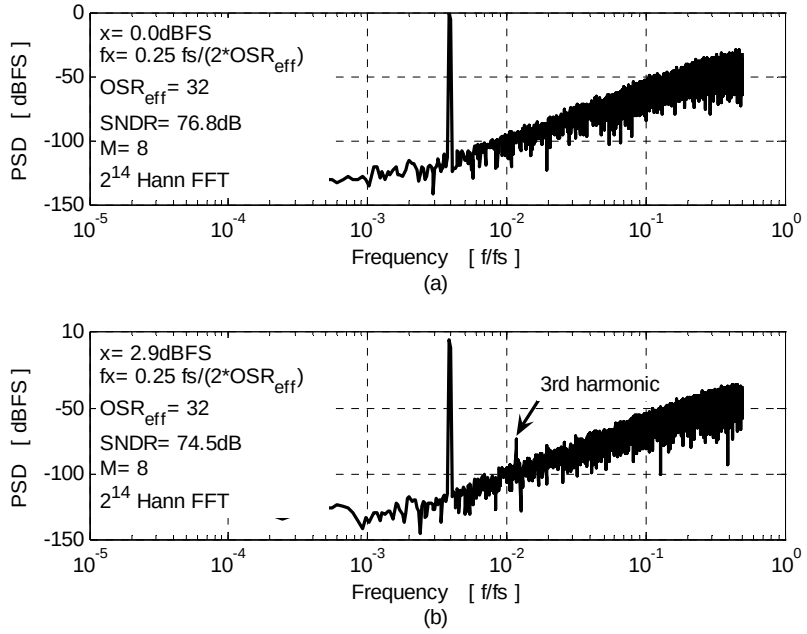

Fig. 4.21: Output spectrum for second-order ΔΣ modulator (a) before Q_2 saturates (b) after Q_2 saturates

Before overloading Q_2, the spectrum does not show distortion as expected from input-feedforward structures. After overloading Q_2, the spectrum shows third-order distortion component. Alternatively, a traditional input-feedforward structure can be used in conjunction with the DIFF concept to achieve low-swing and low-distortion through the entire input range.

4.2.4 Practical Considerations

Two practical issues for the implementation of a DIFF ΔΣ modulator are considered. The effect of timing skew between Q_2 and the analog signal path is studied. In addition, the options and tradeoffs for the realization of the subtractor in the first stage are analyzed.

Timing skew at the input of the DIFF modulator is inevitable without adding a sample and hold circuit at the front end, therefore, understanding its effect is important. To explore this matter, the DIFF model can be redrawn as shown in Fig. 4.22 with an explicit delay in the quantizer path.

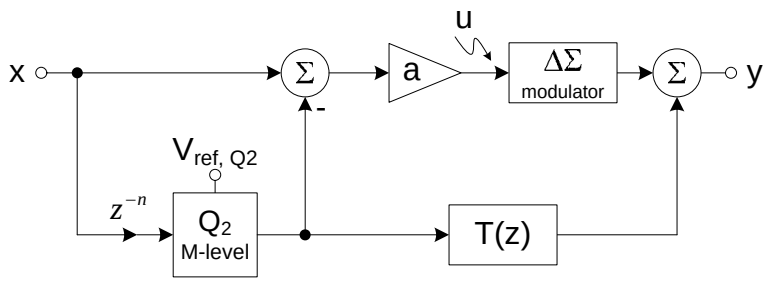

Fig. 4.22: Generalized DIFF ΔΣ modulator with delay in ADC_2 path

Analysis of the linearized system for the modulator in Fig. 4.22 leads to the following results:

$$y = \left[a\ STF_{\Delta\Sigma} + z^{-n}\left(T(z) - a\ STF_{\Delta\Sigma}\right)\right]x + NTF_{\Delta\Sigma}\ q_1 + \left(T(z) - a\ STF_{\Delta\Sigma}\right)q_2$$

for $T(z) = a\ STF_{\Delta\Sigma}$:

$$y = a\ STF_{\Delta\Sigma}\ x + NTF_{\Delta\Sigma}\ q_1$$

In addition, the input to the internal ΔΣ modulator is:

$$u = a\left(\left(1 - z^{-n}\right)x - q_2\right)$$

Therefore, the input of the internal ΔΣ modulator contains the quantization noise from ADC_2 and an input-signal component shaped by $(1-z^{-n})$ which has an insignificant effect. For example, a 2% skew in the period results in a negligible signal component at the output of the first stage as illustrated in Fig. 4.23. Therefore, the timing skew is not critical. This also suggests a method to overcome the timing issue at the expense of having a noise shaped input-signal. A practical choice to relax the timing requirements is to use $z^{-1/2}$ delay in the quantizer path. The resultant frequency shaping is shown in Fig. 4.23. However, the high frequency boost is undesirable from the stability standpoint. Note that a $z^{-1/3}$ in the quantizer path is the maximum delay for no boost in the quantization noise.

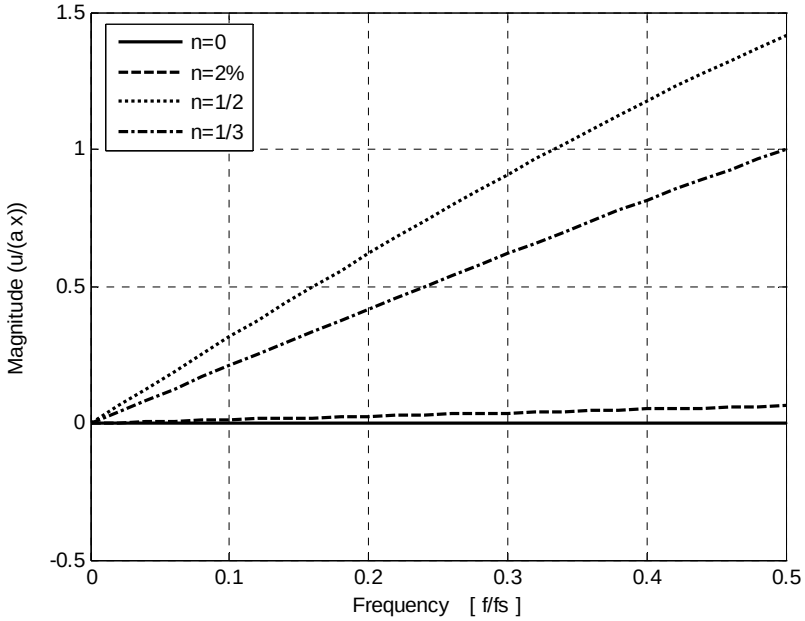

Fig. 4.23: Frequency shaping of the input-signal at the output of first stage for different skew values

There are two possibilities for the implementation of the subtractor in the first stage. One option is to add the feedback signal from the ΔΣ modulator to the output of the first stage ADC digitally and feed the sum back to the first integrator through a single DAC. The digital processing concept is illustrated conceptually at the top of Fig. 4.24. The other option is to subtract the signal in the analog domain. To do so, two separate DACs connected to the virtual ground of the first integrator feed the output of the internal and external ADCs to the first integrator. The analog processing option is illustrated conceptually at the bottom of Fig. 4.24.

Adopting the digital option increases latency due to the digital processing of the signal and the increasing complexity of DEM due to the larger feedback digital signal. However, the analog option is more sensitive to coefficient mismatch. Using Monte-Carlo simulations on the modulator of section 4.2.3 (as shown in Fig. 4.25), the expected SNDR mean and lower 3σ variations due to mismatch are illustrated in Fig. 4.26. The Monte-Carlo model in Fig. 4.25 multiplies each integrator coefficient with a normally distributed random number with unity mean (α_n). Since the same variance is used to generate α_n, the larger capacitors (larger coefficients) suffer from worse mismatch than the smaller ones. This represents worst case condition and could happen if bad layout is followed. However, if good layout practices are used, larger capacitors will have better matching than small ones.

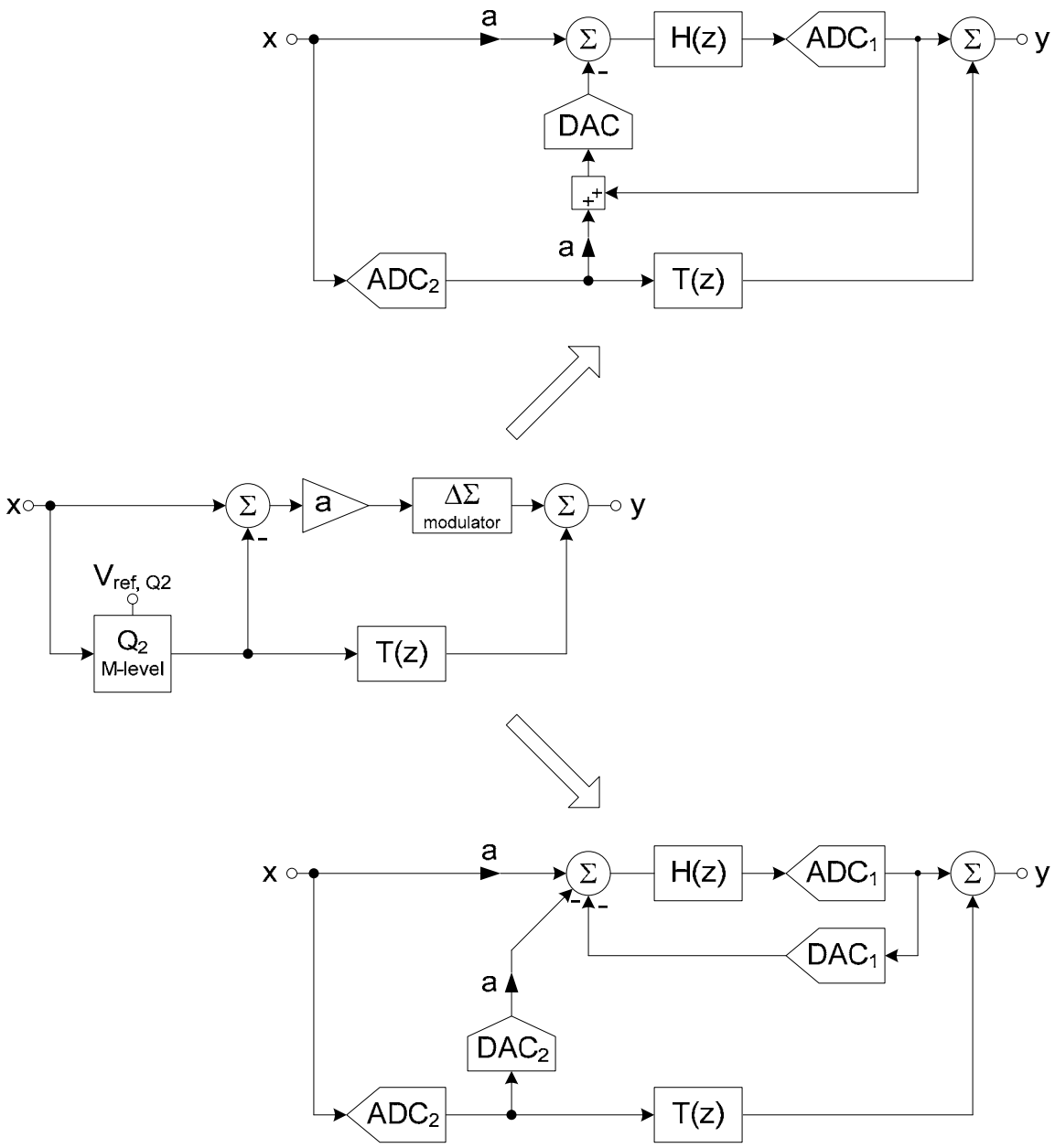

Fig. 4.24: Generalized DIFF ΔΣ modulator with two possible implementations

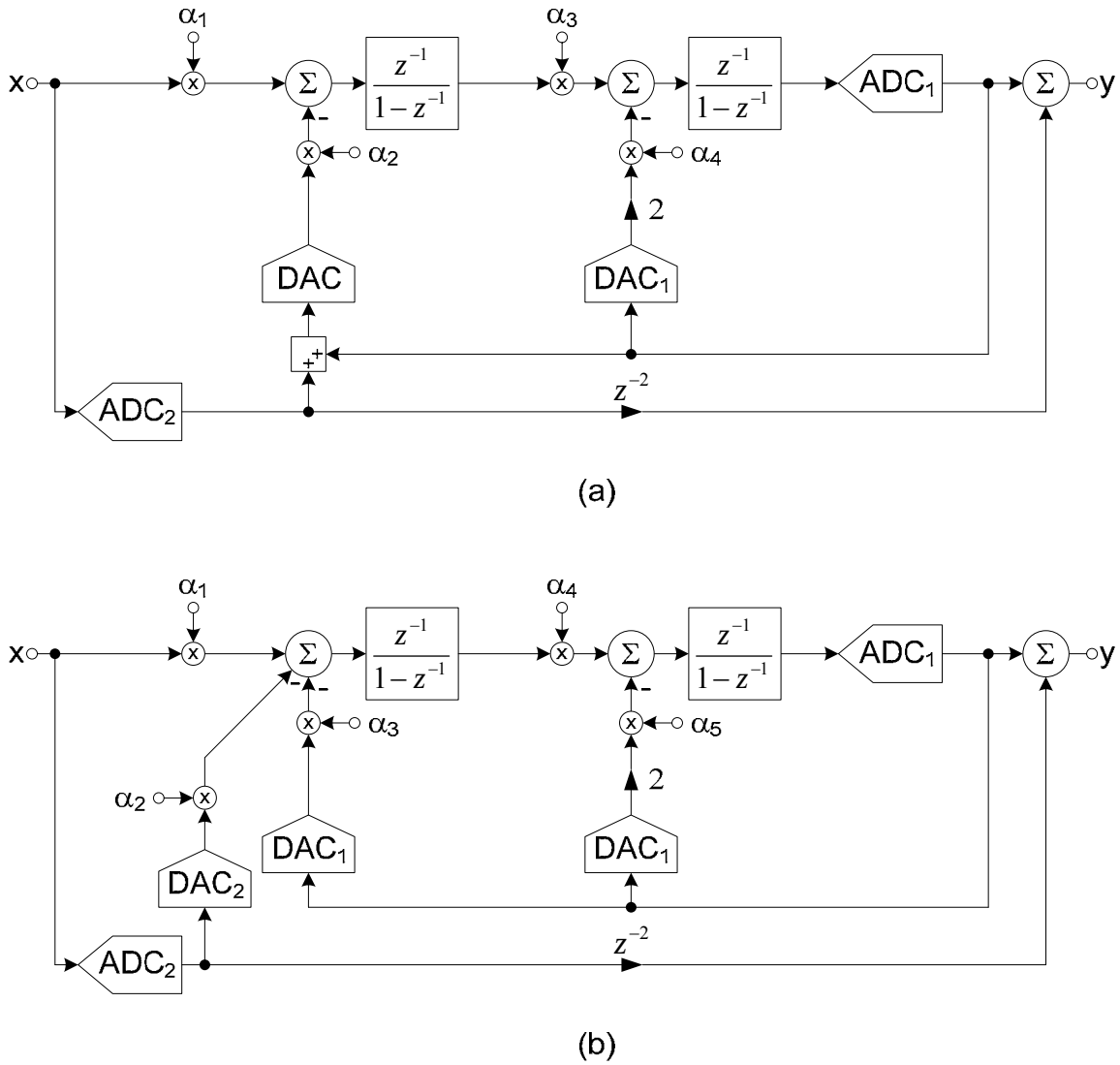

Fig. 4.25: System level of the ΔΣ modulator for Monte-Carlo simulations (a) digital implementation (b) analog implementation

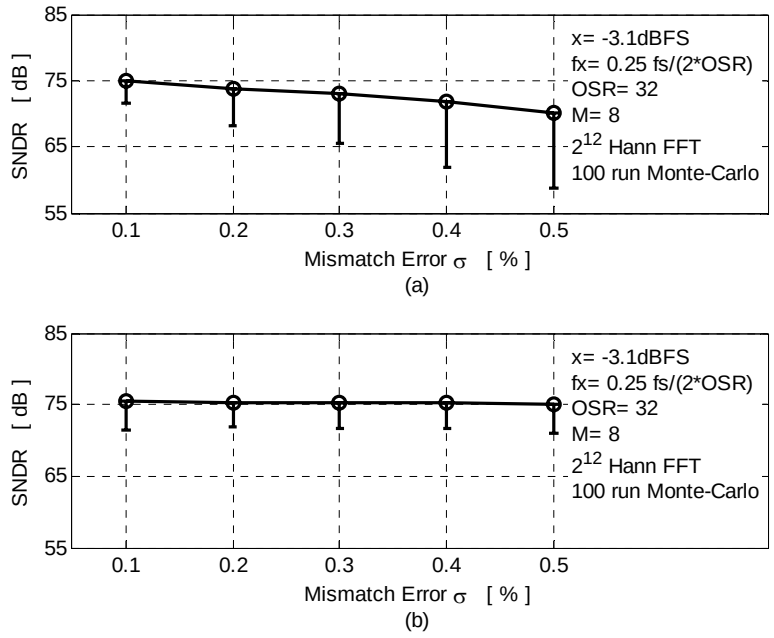

Fig. 4.26: SNDR mean "o" and lower 3σ variation "-" due to coefficient mismatch for a sinusoidal input (a) analog implementation (b) digital implementation

To understand the cause of the modulator behavior with a single DAC (digital implementation) and two separate DACs (analog implementation), consider the linearized first-order DIFF modulator shown in Fig. 4.27 with unity inter-stage gain. The separate errors in the coefficients of the external DAC (ε_2) and the internal DAC (ε_1) imply analog domain addition. Analysis of the modulator leads to the following results:

$$y = \frac{z^{-1}\left[\left(1-\varepsilon_2\right)+z^{-1}\varepsilon_1\right]}{1+z^{-1}\varepsilon_1}x + \frac{1-z^{-1}}{1+z^{-1}\varepsilon_1}q_1 + \frac{z^{-1}\left[-\varepsilon_2+z^{-1}\varepsilon_1\right]}{1+z^{-1}\varepsilon_1}q_2$$

On the other hand, if the addition is performed in the digital domain, the errors are equal ($\varepsilon_1 = \varepsilon_2 = \varepsilon$) and the equation describing the modulator becomes:

$$y = \frac{z^{-1}\left[1-\varepsilon\left(1-z^{-1}\right)\right]}{1+z^{-1}\varepsilon}x + \frac{1-z^{-1}}{1+z^{-1}\varepsilon}q_1 - \frac{z^{-1}\varepsilon\left(1-z^{-1}\right)}{1+z^{-1}\varepsilon}q_2$$

A plot of the magnitude response of the external quantizer (q_2) is shown in Fig. 4.28 for both implementations with DAC coefficient error. At low frequencies, the quantization noise leakage from the external quantizer to the output is smaller for the single DAC implementation. Since the low frequency region is the section of the spectrum of interest due to oversampling, the digital implementation has lower sensitivity to DAC coefficient errors.

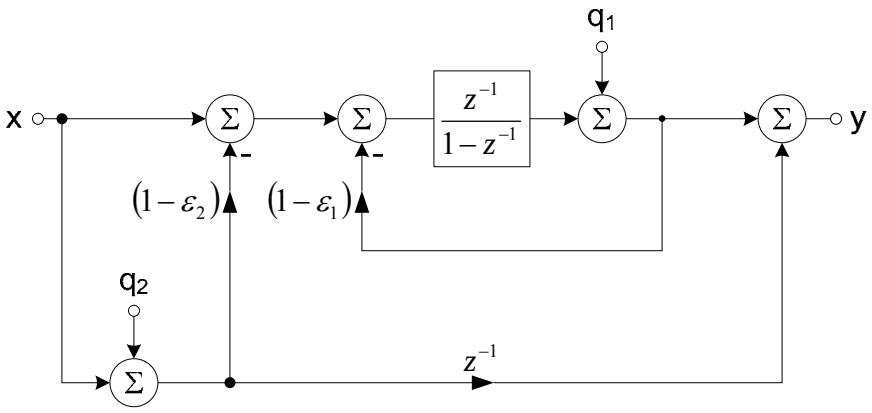

Fig. 4.27: Linearized first-order modulator with DAC errors

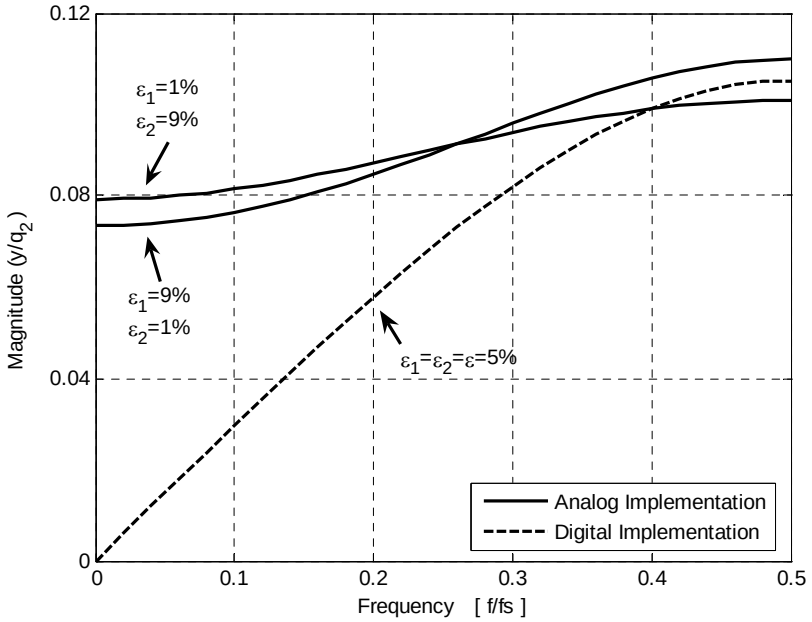

Fig. 4.28: Magnitude response for the external quantizer with DAC error using analog and digital implementations

4.3 Summary

Input-feedforward modulators are attractive for implementation in low OSR and low supply voltage environment. However, the input-feedforward path introduces two complications: a timing constraint and an adder at the quantizer input. A double sampled input is proposed to mitigate the timing constraint due to the critical path. The capacitive-input-feedforward is proposed to eliminate the problematic adder at the quantizer input while maintaining low distortion and low signal swing at the important nodes.

The DIFF ΔΣ modulator is proposed and evaluated. It eliminates the analog adder at the quantizer input and increases the achievable SNDR, in addition to the low swing and low distortion benefits of input-feedforward topologies. Since the DIFF modulator is a noise canceller, it requires analog and digital matching. Matching can be achieved by designing the analog circuits with stringent requirements or by calibrating the digital circuits. The timing constraint due to the critical path in the DIFF topology can be overcome with circuit techniques (the double sampled input) or at the architectural level (the delaying external quantizer).

Chapter 5:

Design of the Experimental Modulator

IN Chapter 4, the digital input-feedforward concept was proposed. The tradeoffs involved in the DIFF design were analyzed. This chapter discusses the implementation of the experimental modulator based on the DIFF concept. In this proof-of-concept implementation, the main characteristics of the DIFF ΔΣ modulator are illustrated.

The system, structural, and circuit level design of the experimental modulator are presented here. The system level provides the mathematical description of the modulator and is discussed in Section 5.1. Then, Section 5.2 presents the structural level which shows the mapping of the system model into the equivalent switched-capacitor circuits. Next, circuit level implementation of the building blocks in 0.18μm CMOS technology is discussed in Section 5.3. Finally, the measured performance of the test chip is presented in section 5.4.

5.1 System Level Design

The objective of the experimental chip is to build a configurable modulator that is capable of operating as a DIFF ΔΣ modulator or as a traditional feedback ΔΣ modulator. The configurability feature facilitates the evaluation of the proposed modulator and allows the comparison with traditional architectures. However, the two modulators impose different requirements on the building blocks. Therefore, some compromises had to be made in order to share the building blocks between the two architectures.

The system level of the DIFF ΔΣ modulator is shown in Fig. 5.1. The second stage is a third-order feedback ΔΣ modulator topology with a resonator to create non-dc zeros to optimize the NTF for the desired OSR of 8. It uses a 17-level internal quantizer (ADC_1) with reference voltage levels of $\pm 0.5\ V_{diff}$. The first stage (ADC_2) also uses a 17-level quantizer. The DIFF ΔΣ modulator is intended for use in the low swing and low distortion region of operation only (external ADC_2 is not saturated) with an input-signal of $\pm 1.0\ V_{pp,diff}$. Therefore, ADC_2 uses reference voltage levels of $\pm 1.0\ V_{diff}$. The digital filter and digital adder are implemented off-chip.

The inter-stage gain is chosen to be unity to simplify the configurability implementation. The modulator in Fig. 5.1 can operate as a feedback ΔΣ modulator by simply turning ADC_2 and DAC_2 off. Note that the analog implementation is chosen to realize the adders at the modulator input to keep the configurability feature simple. Fig. 5.2 illustrates the parts of the experimental ΔΣ modulator that are implemented on-chip and indicates the inputs and outputs.

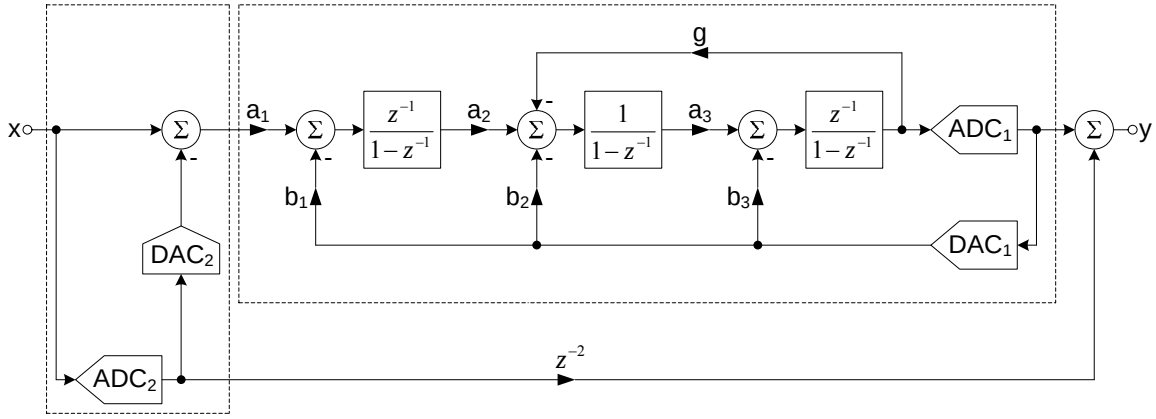

Fig. 5.1: System level of the experimental ΔΣ modulator

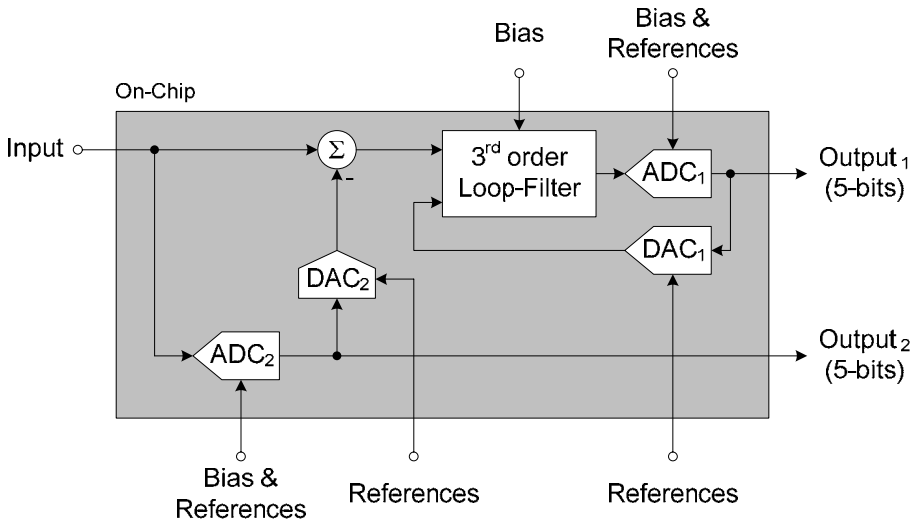

Fig. 5.2: Block diagram illustrating the parts of the experimental ΔΣ modulator that are implemented on-chip

The delta-sigma toolbox [32] is used to synthesize the optimized third-order NTF with maximum out-of-band gain and an OSR of 8. The synthesized coefficients and the values used in the modulator are summarized in Table 5.1.

Table 5.1: Coefficients for the ΔΣ modulator

Coefficient	Value from toolbox	Value for implementation
a_1	1	1/2
b_1	1	1/2
a_2	1	2
b_2	1.9082	32/17 (≈1.8824)
g	0.0918	2/17 (≈0.1176)
a_3	1	1
b_3	1	1

The coefficients for the first integrator (a_1 and b_1) were scaled down by a factor of two (which increases a_2 by a factor of two). The coefficient scaling reduces the signal swing at the output of the first integrator and makes it smaller than that of the second and third integrators. This is done to reduce distortion resulting from the first integrator when the modulator is operating as a feedback ΔΣ modulator since distortion from the second and third integrators is less significant. Of course, the signal swing is not an issue when the modulator is operating in the DIFF mode. A summary of the 3σ signal swings at the output of the integrators and the achievable SNDR for both modes of operation are summarized in Table 5.2 for a sinusoidal input signal with the maximum input-signal specified in the table.

Table 5.2: 3σ signal swings at the output of the integrators and SNDR at maximum input

		DIFF ΔΣ	Feedback ΔΣ
Maximum Input-Signal		2.0 V_{refl} (6 dBFS)	0.8 V_{refl} (-2 dBFS)
SNDR		80 dB @ 6 dBFS	71 dB @ -2 dBFS
Single ended 3σ signal swings	Integrator 1 output	0.25 V_{refl}	0.8 V_{refl}
	Integrator 2 output	0.5 V_{refl}	1.2 V_{refl}
	Integrator 3 output	0.5 V_{refl}	1.2 V_{refl}

The other changes in the coefficient values are b_2 and g which modifies the NTF. The NTF modification results in a reduction of the achievable SNDR since the zeros are not in their optimum location. However, practical considerations justify the small reduction in the SNDR. There are two factors that determine the new b_2 and g value. First, the new values should allow a practical unit size capacitor without significantly changing the NTF. Second, the sum of b_2 and g should remain the same, for our case the sum is 2. If the sum is not maintained, the STF of the ΔΣ

modulator will change. The transfer functions of the third-order ΔΣ modulator as a function of b_2 and g are given by:

$$STF = \frac{z^{-2}}{1+(b_2+g-2)z^{-1}-(b_2+g-2)z^{-2}}$$

$$NTF = \frac{1-(3-g)z^{-1}+(3-g)z^{-2}-z^{-3}}{1+(b_2+g-2)z^{-1}-(b_2+g-2)z^{-2}}$$

As pointed out earlier, the change in the NTF is not significant. On the other hand, the STF change will result in high frequency boost which is undesirable. In addition, since the digital filter must match the STF, it is more efficient for the digital filter to be simple delay elements instead of a more complicated filter.

The maximum achievable SNDR for the feedback ΔΣ modulator is 71 dB at its maximum input-signal of -2 dBFS. The maximum achievable SNDR for the DIFF ΔΣ modulator is 80 dB at an input-signal of 6 dBFS (ADC_2 is not saturated) and is 83 dB at the absolute maximum input-signal of 9 dBFS as shown in Fig. 5.3.

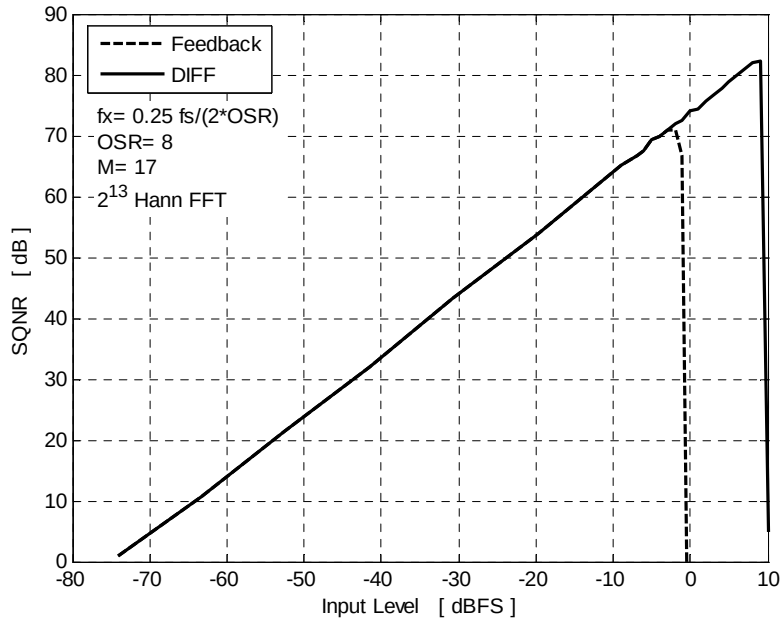

Fig. 5.3: SQNR versus input-signal amplitude

Matching between the STF of the feedback ΔΣ and the digital filter is required for the proper operation of the DIFF modulator. For the experimental modulator, the matching is achieved by making the analog path match the digital one. Therefore, to determine the design specifications, the modulators are simulated taking into account the effects of finite gain and

bandwidth in the opamps. The second stage opamp has 5% less gain and bandwidth than those in the first stage and the third stage has 5% less gain and bandwidth than those in the second stage. The results are summarized in Fig. 5.4 where f_{-3dB} is the closed-loop -3 dB bandwidth of the opamp and $f_{sampling}$ is the sampling frequency.

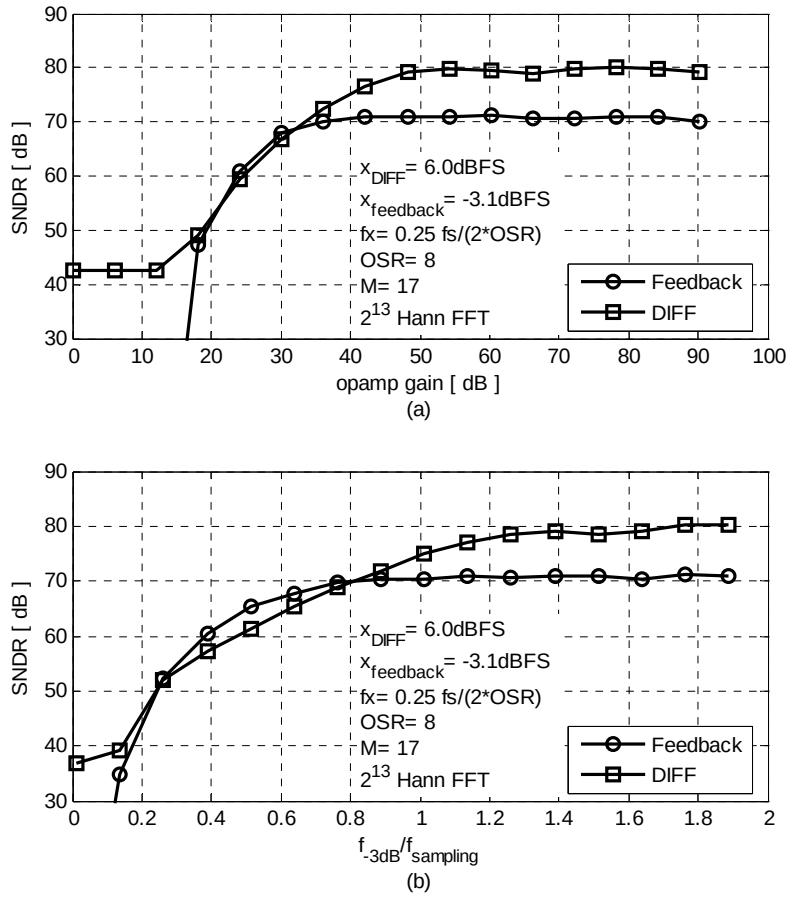

Fig. 5.4: SNDR versus (a) opamp gain (b) normalized bandwidth

The component matching requirements for the ΔΣ modulator are determined using a 100 point Monte-Carlo simulation in Matlab with the model shown in Fig. 5.5. The parameters α_n are one plus a normally distributed random number.

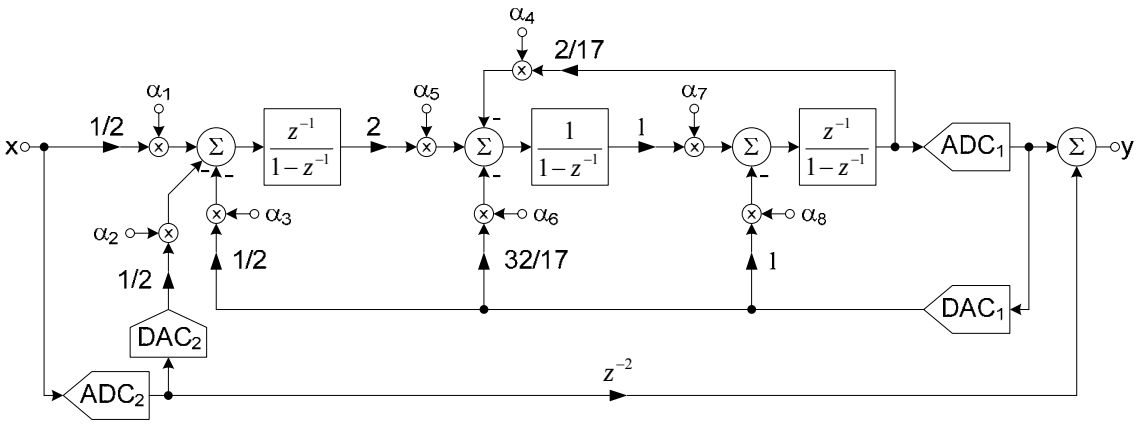

Fig. 5.5: System level of the experimental ΔΣ modulator for Monte-Carlo simulations

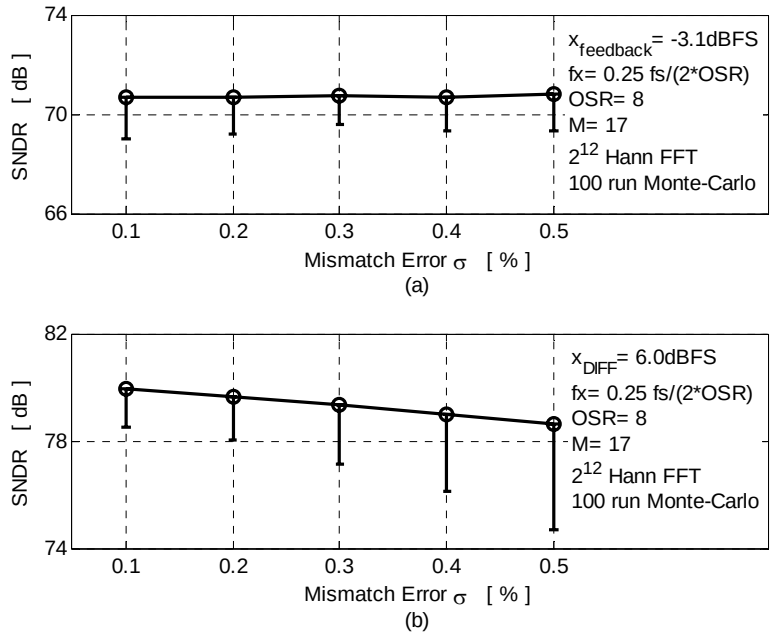

Fig. 5.6: SNDR mean "o" and lower 3σ variation "-" due to coefficient mismatch for a sinusoidal input (a) feedback ΔΣ (b) DIFF ΔΣ

The expected SNDR and lower 3σ variations due to mismatch are summarized in Fig. 5.6. Since 0.1% capacitor matching is possible with careful layout, the matching requirements are achievable with good reliability for both topologies in the experimental modulator in the 0.18μm CMOS technology.

5.2 Structural Level Design

The next step in the design is mapping the system model into the equivalent switched-capacitor implementation. The resulting structure is shown in Fig. 5.7 in the single-ended form for simplicity, the actual implementation is fully-differential. The feedback signals to the first and third integrators go through a DWA block but the second integrator does not. This is due to the delaying integrators in the first and third sections and the non-delaying integrator in the second section. Therefore the timing requirements for a DWA in the second integrator can not be met at the required speed. Of course, DWA for the first stage is critical for the operation of the modulator since the DAC is feeding the signal to the input of the modulator. However, it is not critical for the second and third integrators since those errors are noise shaped when referred back to the input.

The first integrator uses the double sampled input technique to mitigate the timing constraint of the DIFF ΔΣ modulator [23] and [21]. The signal from DAC_1 goes through a DWA block and is then added to the modulator in the analog domain. The addition in the analog domain has some drawbacks: more kT/C noise is injected into the modulator, the feedback factor is reduced, and the modulator is more sensitive to mismatch. However, it is the simplest method to facilitate the configurability of the modulator. Furthermore, it reduces the latency in the DWA block since digital addition requires larger barrel shifter to shuffle the sum of two signals.

The quantizers are latched at the falling edge of the delayed phase 2 while the sampling capacitors sample their signal at the falling edge of phase 2. The small sampling skew this clocking arrangement introduces at the input is not significant for the operation of the modulator as discussed in the previous chapter. It is done to ensure that any kickback from ADC_2 does not affect the sampled input-signal.

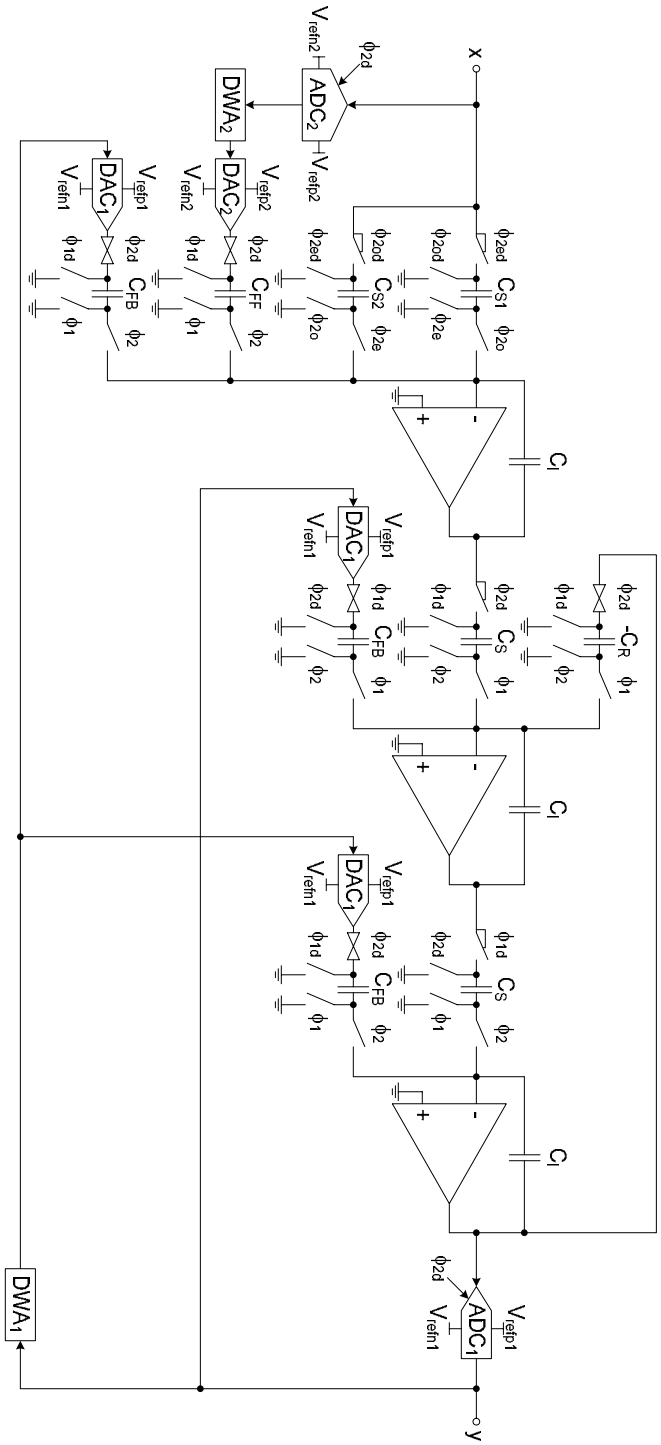

Fig. 5.7: ΔΣ modulator structural level

The next step is to verify the mapping, timing, and capacitor ratios. Both open-loop and closed-loop tests are carried out to perform the verification. For this purpose, ideal blocks are used to build the modulator in Fig. 5.7 and Spectre is used in the simulations. Note that in the

following, the open-loop tests and the closed-loop STF test are carried out excluding ADC_2 and DAC_2 (stage one).

The open-loop test involves breaking the feedback path, removing the quantizer, and finding the impulse response of the resulting system. The system now has two inputs and one output, therefore, two impulse responses. The first is from the input to the output, while the second is from the feedback to the output. The impulse response for the Simulink model and the switched-capacitor circuit match.

The closed-loop tests include the verification of the STF and the NTF. The STF is verified by comparing the impulse response of the Simulink model and the switched-capacitor circuit where the quantizer is replaced with a sample-and-hold circuit. The closed-loop impulse response shows a STF match. The NTF verification is performed by comparing the SNDR and the shape of the PSD from the output of the Simulink model and the switched-capacitor circuit. Both SNDR and PSD shape were similar.

The next step is to determine capacitor sizes for the desired 12-bit performance. The following noise analysis assumes ideal opamps and therefore noise is determined by the sampled thermal switch noise. This assumption can be justified for the following reasons. First, the error resulting from the ideal opamp assumption is small [33]. Second, since we need the capacitor sizes to design the opamp, we can not determine the noise from the opamp before determining its load. Therefore, the capacitor sizes can be designed for better performance than required, and once the opamps are complete, the designer can verify the noise performance and adjust capacitor sizes as desired. Note that although thermal noise dominates the total noise in the final modulator, it is not the only source of noise.

Noise analysis involves the determination of the stage noise and the total noise from all the stages when referred back to input. Total noise in $\Delta\Sigma$ modulators is dominated by the noise from the first stage because noise from later stages is shaped when referred back to the input. Unfortunately, the error resulting from ignoring later stages can be significant for low OSR such as the one chosen for this design. Therefore, noise from all stages is used to determine capacitor sizes for the desired SNR. First, for the stage noise, a generic integrator is shown in Fig. 5.8 with the input sampling capacitor, a possible feedback and feedforward capacitors.

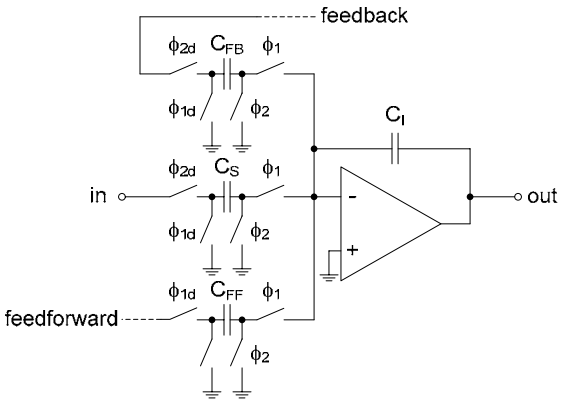

Fig. 5.8: Input referred noise from a general integrator

The total input referred noise for each stage is given by:

$$\overline{v_{no\_in}^2} = \frac{2kT}{C_S}\left(1 + \frac{C_{FB}}{C_S} + \frac{C_{FF}}{C_S}\right) \tag{5-1}$$

Next, total input referred noise from all integrators is given by:

$$\overline{v_{no\_in\_total}^2} \approx \sum_{i=1}^{n} \frac{\left(\overline{v_{no\_in}^2}\right)_n}{\pi(2i-1)\prod_{j=1}^{i-1} a_j^2}\left(\frac{\pi}{OSR}\right)^{2i-1} \tag{5-2}$$

where n in the stage number and a is the integrator coefficient (C_S/C_I). Therefore, these formulas were used to estimate the total input referred noise for the DIFF modulator. Then, noise, input-signal swing, and desired SNR were used to find capacitor sizes. Eqs. (5-1) and (5-2) provide good approximation of the thermal noise contribution in a switched-capacitor ΔΣ modulator. Recently, simulation programs provided transient noise simulation capability. However, because of the excessive required simulation time and the sufficient accuracy provided by the above equations, transient noise was not simulated.

Table 5.3 summarizes the capacitor sizes used in the experimental modulator. The capacitors in the second stage are limited by the minimum unit size capacitor possible in the 0.18μm. The capacitors in the third stage are chosen such that the specifications of the opamp in the third stage are similar to those in the second stage. Therefore, the opamp designed for the second stage can be used for the third.

Table 5.3: Capacitor sizes used in the experimental modulator

	Capacitor	Size [pF]	Size [unit cap]
Stage 1 unit cap=62.5fF	C_I	2	32
	$C_{S1,2} = C_{FB} = C_{FF}$	1	16
Stage 2 unit cap=20fF	C_I	0.34	17
	C_S	0.68	34
	C_{FB}	0.64	32
	C_R	0.04	2
Stage 3 unit cap=31.25fF	$C_I = C_S = C_{FB}$	0.5	16

Based on the these capacitor values, the SNR due to switch thermal noise only is 78 dB for the DIFF ΔΣ modulator and 70 dB for the feedback ΔΣ modulator.

5.3 Circuit Level Design

The next step in the design process is to implement each of the building blocks in the 0.18μm CMOS technology. This section describes the transistor level implementation of the building blocks. In the following, it is assumed that the source and bulk of the transistors are connected unless otherwise specified.

5.3.1 Operational amplifiers

As pointed out earlier, the opamp requirements were determined using system level simulations with opamp non-idealities. The telescopic opamp architecture is picked for implementation and is shown in Fig. 5.9.

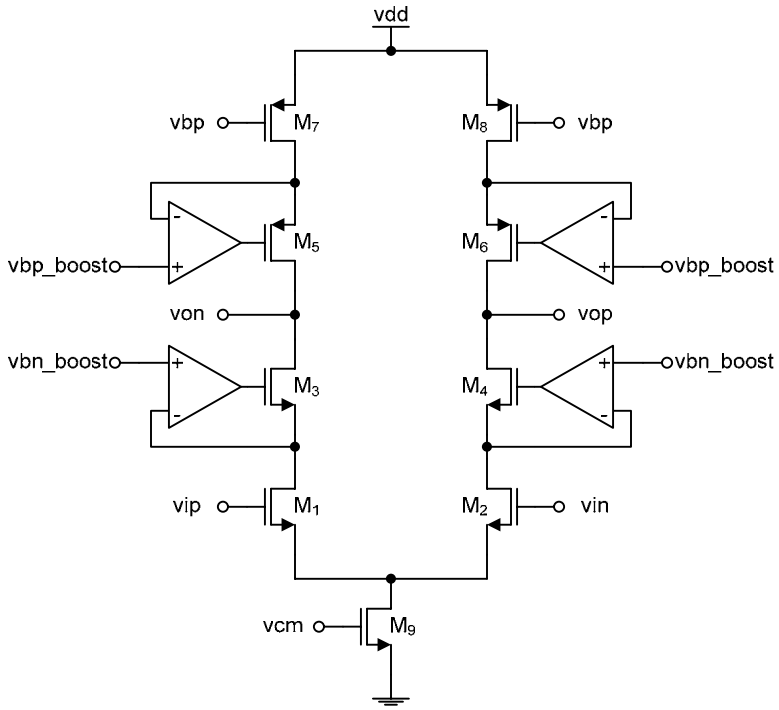

Fig. 5.9: Telescopic opamp

Telescopic opamps with NMOS inputs have the advantage of high-speed operation because of the all NMOS signal path and the small time constant at the second pole node. In addition, telescopic opamps have good noise performance due to the small number of noise contributing devices. The source of the input and the cascode NMOS transistors are tied to their bulk to maintain a lower threshold voltage and improve the common-mode rejection. The output common-mode voltage is set using a typical switched-capacitor common-mode feedback circuit where the control voltage (vcm) is feedback to the tail transistor. The DC gain from the telescopic opamp is not sufficient and gain boosters are needed to achieve the desired gain. The disadvantages of telescopic opamps are the small output swing and the small common mode input range. The former limitation is not important for input-feedforward ΔΣ topologies. However, the input common mode is a significant limitation because its value is roughly mid-rail (0.85 V for experimental modulator). This value complicates the design of the switches because of the larger on-resistance due to the small gate-source voltage. In addition, the small input common mode range translates to tight design margin which is undesirable.

The transistor sizes used for the opamp in the first stage are summarized in Table 5.4. The opamps in the second and third stages are half the size of the first.

Table 5.4: Component sizes for the opamp in the first stage

	L [μm]	W [μm]	No. fingers
M_1,M_2	0.24	2	150
M_3,M_4	0.24	2	60
M_5,M_6, M_7,M_8	0.24	8	60
M_9	0.24	2	120

For the DIFF ΔΣ modulator, the opamp in the first integrator has a DC gain of 97 dB at 0.5 V_{diff} swing and a loop bandwidth of 720 MHz with 76° phase margin. And for the feedback ΔΣ modulator, the opamp in the first integrator has DC gain of 84 dB at 1.6 V_{diff} swing and a loop bandwidth of 900 MHz with 75° phase margin. The following stages have a similar performance but with reduced capacitor sizes and hence less power.

The gain boosting amplifier for the NMOS (PMOS) cascode transistors is shown in Fig. 5.10 (Fig. 5.11). The transistor sizes used in the opamp in the first stage are summarized in Table 5.5 (Table 5.6). The gain boosters in the second and third stages are half the size of the first.

There are two constraints in the design of the gain boosting amplifier: stability and settling [34]. For stability, the unity gain frequency of the gain booster should be less than the second pole of the main amplifier, and for settling, the unity gain frequency of the gain booster should be larger than the closed-loop bandwidth of the main amplifier. This condition ensures that the doublet generated by the gain booster is high enough in frequency such that it does not effect the settling.

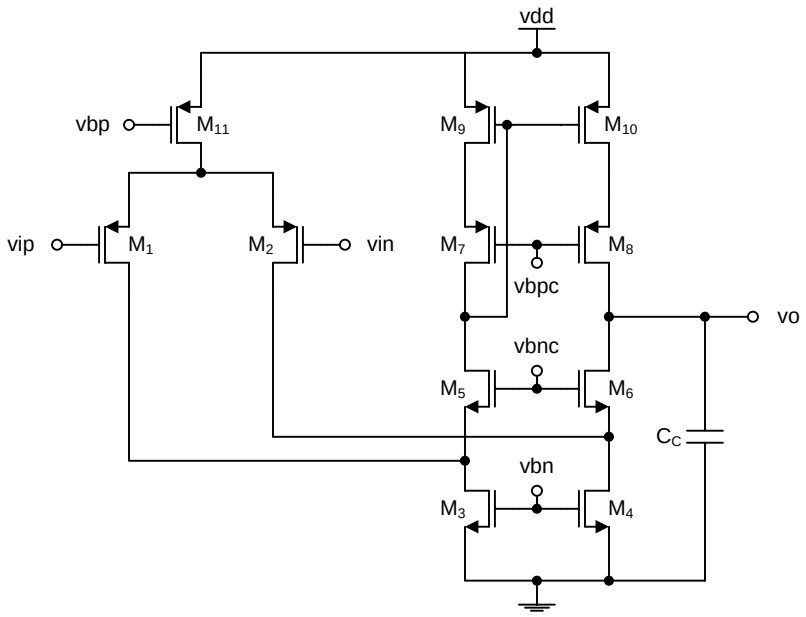

Fig. 5.10: NMOS cascodes gain booster

Table 5.5: Component sizes for the NMOS cascodes gain booster

	L [μm]	W [μm]	No. fingers
M_1,M_2,M_7,M_8, M_9,M_{10}	0.24	8	2
M_5,M_6	0.24	2	2
M_3,M_4	0.24	2	4
M_{11}	0.24	8	4
C_C	100 fF		

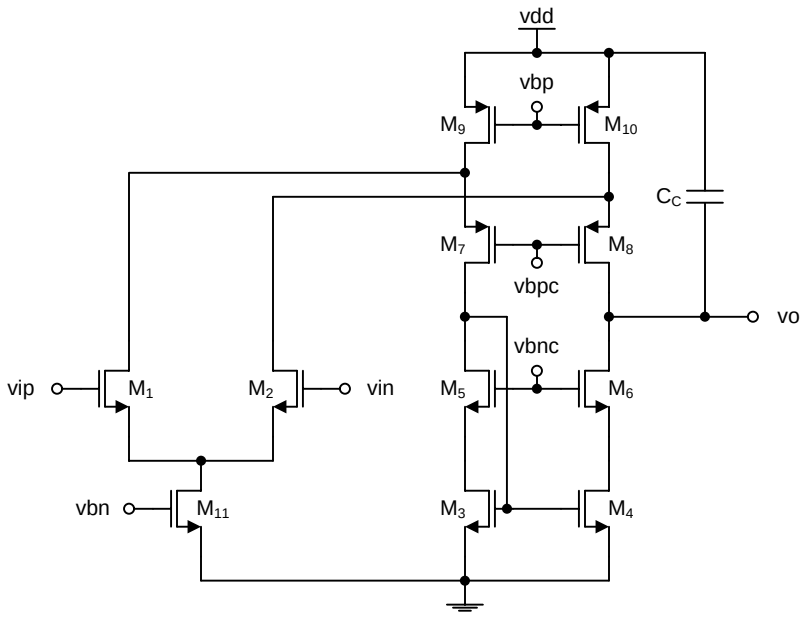

Fig. 5.11: PMOS cascodes gain booster

Table 5.6: Component sizes for the PMOS cascodes gain booster

	L [μm]	W [μm]	No. fingers
M_1,M_2,M_3,M_4, M_5,M_6	0.24	2	2
M_7,M_8	0.24	8	2
M_9,M_{10}	0.24	8	4
M_{11}	0.24	2	4
C_C	100 fF		

All the biasing voltages for the opamps and their gain boosters are generated using typical wide-swing cascode current mirrors except for vbn_boost. The reference voltage for the NMOS cascode gain booster (vbn_boost) is generated as shown conceptually in Fig. 5.12a [35] and the transistor level implementation is shown in Fig. 5.12b. This biasing scheme improves the common-mode rejection ratio. This is because variations in the input common-mode would result in drain-source voltage variations of the input differential pair if the reference voltage of the gain boosters is generated externally. However, since the current through the NMOS transistors of the biasing network is constant, its drain-source voltage and hence the drain-source voltage of the input differential pair is constant regardless of the input common-mode. The input common-mode range is limited by the NMOS cascodes or the tail transistor going out of saturation.

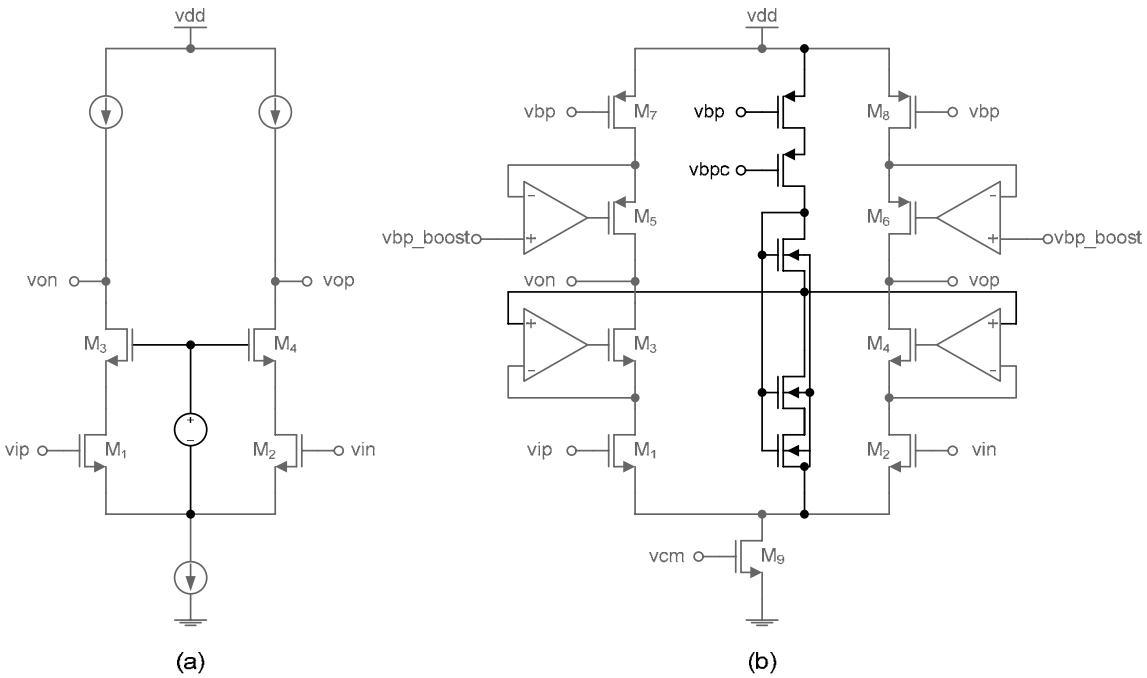

Fig. 5.12: The cascode gain booster reference voltage (a) principle of operation (b) implementation

5.3.2 Quantizers

The internal quantizer ADC_1 and the external quantizer ADC_2 are implemented as 17-level flash ADCs. Each ADC has 16 parallel comparators and each comparator is a cascade of a preamplifier, a latch, and RS latch. The reference levels are generated using a resistive ladder where R is 100 ohms. MOS capacitors were placed at all reference voltages to reduce noise and stabilize the voltages. The flash ADC is shown in Fig. 5.13. The total input capacitance of the flash is 0.24 fF which is about one-fourth the input sampling capacitor (1 pF). Therefore, the extra load at the input due to ADC_2 is not significant.

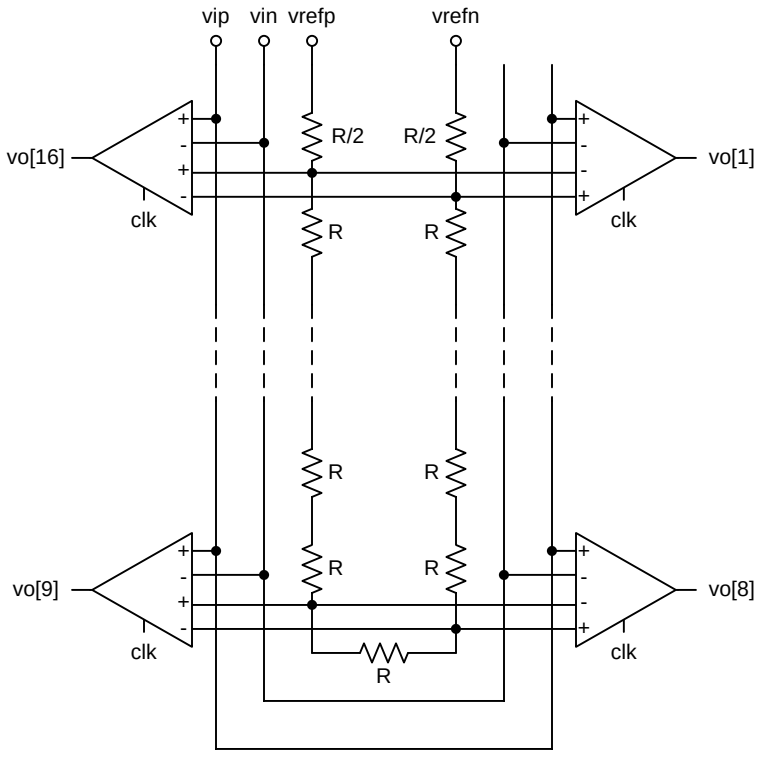

Fig. 5.13: 17-level flash ADC

The preamplifier is a *differential difference amplifier* (DDA) with resistive loads as shown in Fig. 5.14. It has a gain of 5 V/V and a unity-gain frequency of 1.8 GHz.

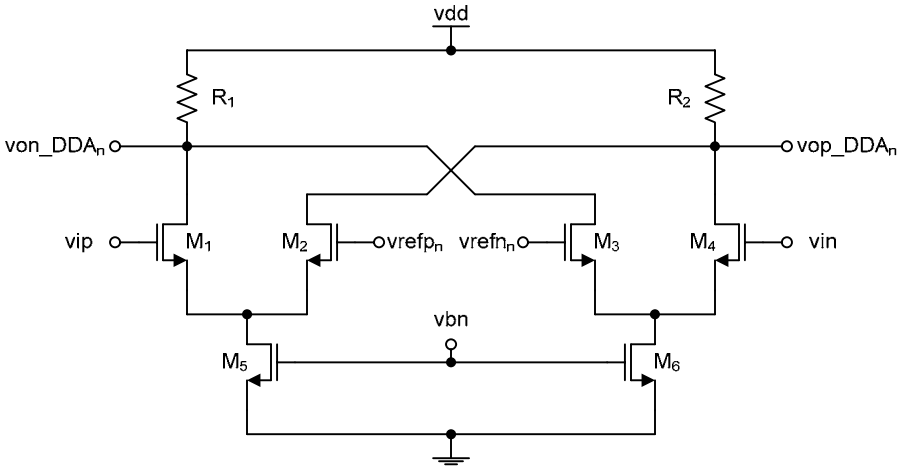

Fig. 5.14: Preamplifier

The preamplifier compares the differential input and differential reference and amplifies the difference. The difference is then processed by the regenerative latch. The gain in the preamplifier is important to reduce the offset of the regenerative latch when referred back to the

input. This is because offsets from the preamplifier are less than those from the latch. In addition, the preamplifier attenuates the kickback noise from the latch. The transistor and resistor sizes used in the preamp are summarized in Table 5.7.

Table 5.7: Component sizes for the preamplifier

	L [µm]	W [µm]	No. fingers
M_1,M_2,M_3,M_4	0.24	2	6
M_5,M_6	0.5	2	4
R_1,R_2	20 kΩ		

A dynamic regenerative latch is used because it is fast and power efficient and it is shown in Fig. 5.15 [36]. The latch is reset when the control signal (latch) is low. Therefore, a simple RS-latch is used to hold the output of the dynamic latch for the remainder of the period. The transistor sizes used in the latch are summarized in Table 5.8.

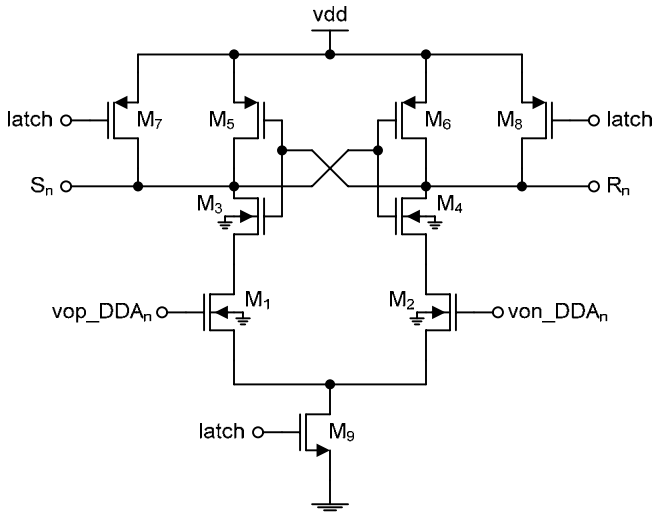

Fig. 5.15: Regenerative latch

Table 5.8: Component sizes for the regenerative latch

	L [µm]	W [µm]	No. fingers
M_1,M_2,M_3,M_4	0.18	2	3
M_5,M_6,M_7,M_8	0.18	2	1
M_9	0.18	2	3

5.3.3 Switches

The switched-capacitor implementation of the modulator indicates that three different types of switches were used as shown in Fig. 5.7. The three types are NMOS, CMOS, and bootstrapped switches as shown in Fig. 5.16.

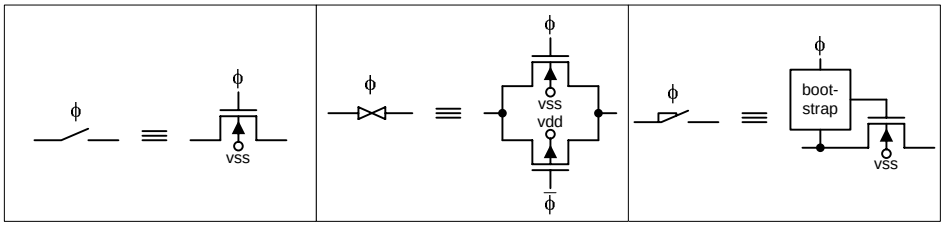

Fig. 5.16: Switches used in the modulator

NMOS switches were used wherever the gate-source voltage is fixed. The switches were sized such that the integrator time constant is five times larger than the switch and capacitor time constant.

CMOS switches were used mostly for cases where the source voltage is one of two fixed voltages such as the voltages from the DACs. They were also used for the local feedback that creates the resonator.

Bootstrapped switches were used for all floating switches that exist at the input of the integrators [37] and [38]. Bootstrapping maintains a constant gate-source voltage for the sampling switch at Vdd. Therefore, the signal range, bandwidth, and linearity are improved. The bootstrapping circuit is shown in Fig. 5.17 and transistor sizes are summarized in Table 5.9. Note that the bulks for all NMOS transistor are connected to Vss; this is not explicitly shown in Fig. 5.17 for simplicity.

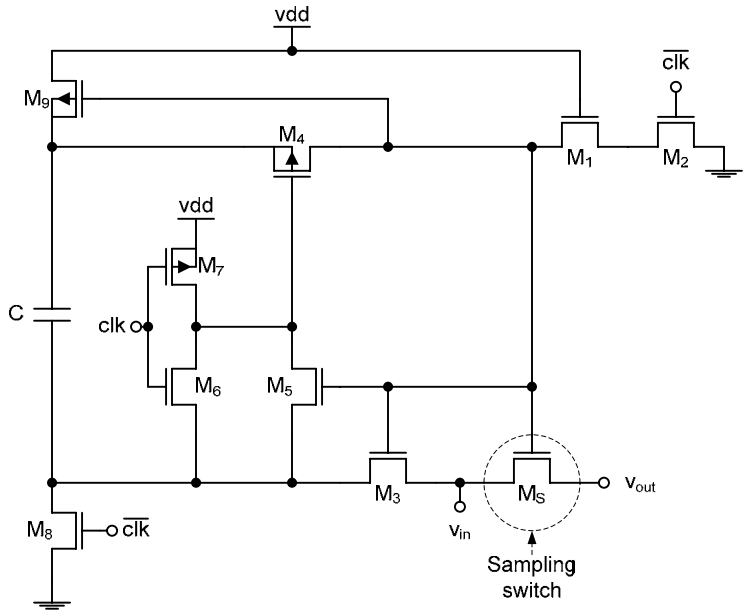

Fig. 5.17: Bootstrapped switch

Table 5.9: Component sizes for the bootstrapped switch

	L [µm]	W [µm]	No. fingers
M_1	0.18	2	20
M_2	0.18	2	30
M_3,M_4,M_5,M_6	0.18	2	10
M_7	0.18	8	10
M_8,M_9	0.18	2	5
C	2 pF		

5.3.4 Data weighted averaging

A block diagram of the data weighted averaging circuit is shown in Fig. 5.18. It has three main components: a barrel shifter, a thermometer-to-binary converter, and the pointer update logic. The barrel shifter takes the output from the flash, performs the shifting, and sends the processed thermometer output to the DAC. The shifting is controlled by a 4-bit pointer that is stored from the previous pointer update logic operation [22]. These 4-bits are sufficient to cover all possible shifting scenarios. The pointer update logic adds the current value from the thermometer-to-binary encoder to the previous pointer value to produce the 4-bit control signal. The pointer rotation is achieved by simply allowing the adder to overflow.

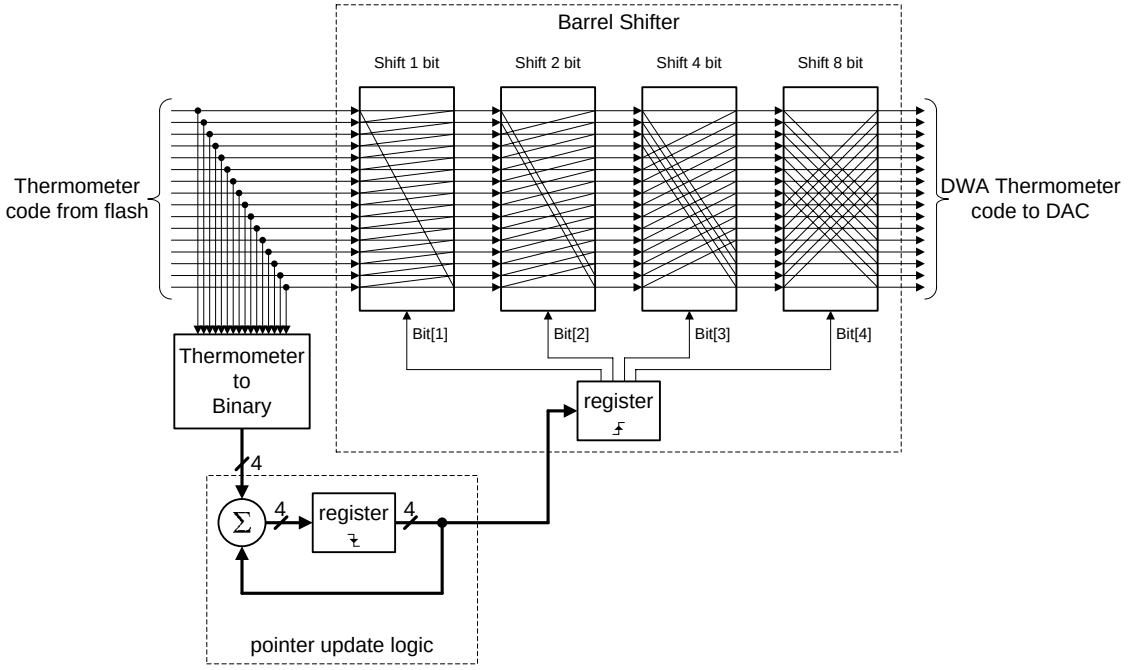

Fig. 5.18: Data weighted averaging

The DWA block is coded in Verilog and synthesized using Synopsys with the standard 0.18-µm CMOS digital library provided by the *Canadian Microelectronics Corporation* (CMC). Under worst case conditions, the barrel shifter requires 1-ns to perform the shifting.

5.3.5 Clock generator

The non-overlapping clock generator and its timing diagram are shown in Fig. 5.19. Phases 1 and 2 are generated using a typical two phase non-overlapping clock circuit shown at the top of Fig. 5.19. The rising edge of phase 1 and its delayed version are the same; only the falling edge is different (same for phase 2). This allows for maximum utilization of the available time to perform the different operations. A delayed phase 2 is divided by 2 using the D-flip-flop in feedback. The divided clock is used to generate the odd and even versions of phase 2.

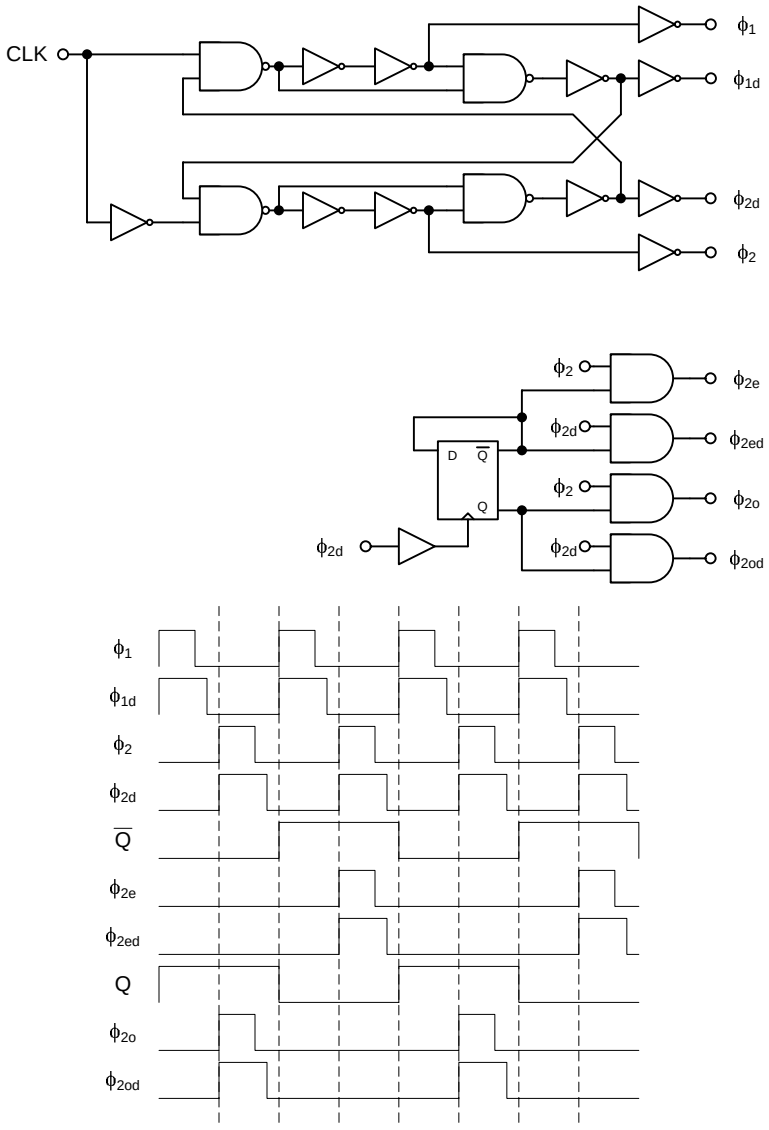

Fig. 5.19: Non-overlapping clock generator and its timing diagram

5.3.6 Simulation Results

Transistor level simulations for the ΔΣ modulator in Fig. 5.7 are presented for both modes of operation. The simulations show the PSD for the output of the modulator, the distribution of the signal at the output of the three integrators, and the PSD for the sampled signal on the front-end sampling capacitor (C_{S1}). For the feedback ΔΣ modulator mode, the results are shown in Fig. 5.20-Fig. 5.22.

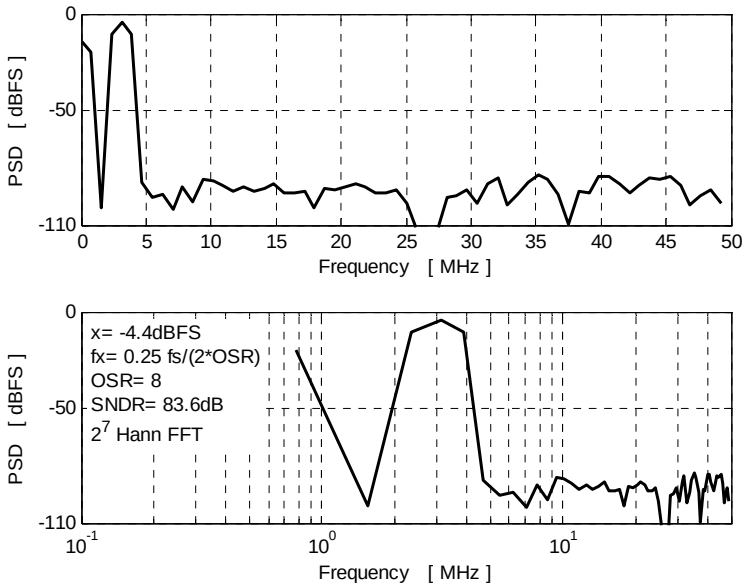

Fig. 5.20: Spectrum for the single-ended sampled signal on C_{S1}

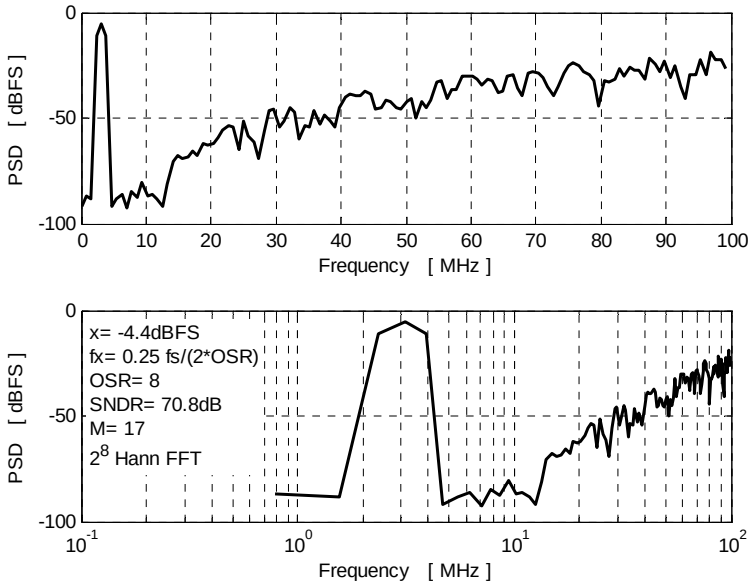

Fig. 5.21: Output spectrum for the ΔΣ modulator in feedback mode

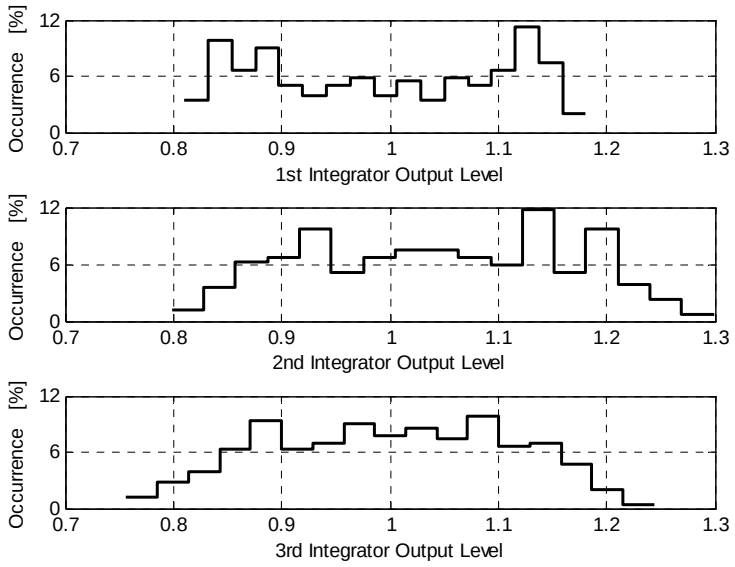

Fig. 5.22: Single-ended output level distribution for the integrators (same specifications as in Fig. 5.21)

Simulation results for the ΔΣ modulator in the DIFF mode are shown for two input levels. First, for the maximum input level before the external quantizer is saturated, the results are shown in Fig. 5.23-Fig. 5.25. Second, for 8.0 dBFS input level, the results are shown in Fig. 5.26-Fig. 5.29.

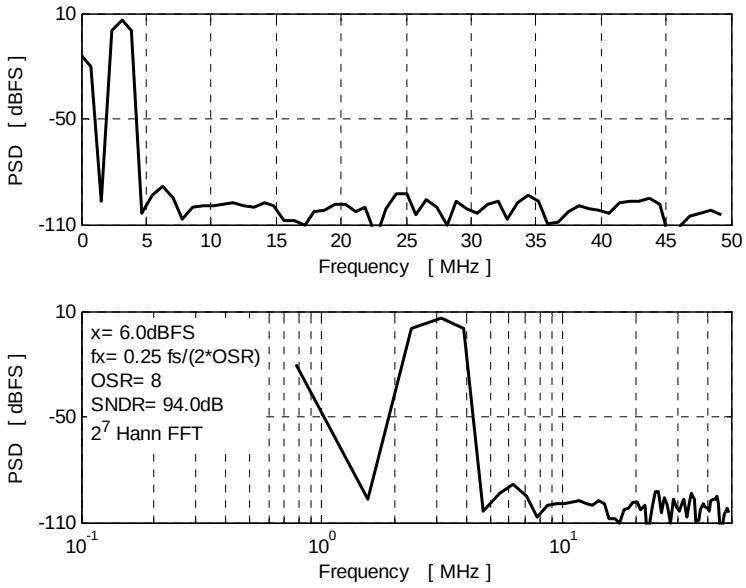

Fig. 5.23: Spectrum for the single-ended sampled signal on C_{S1}

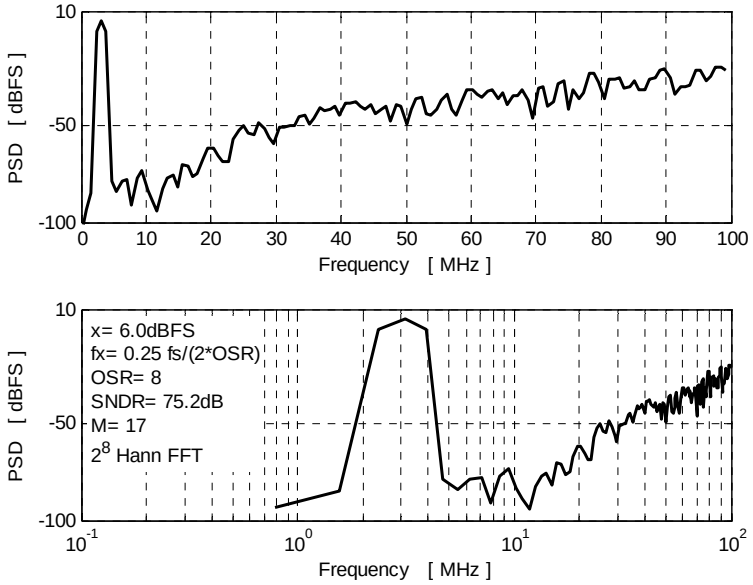

Fig. 5.24: Output spectrum for the ΔΣ modulator in DIFF mode

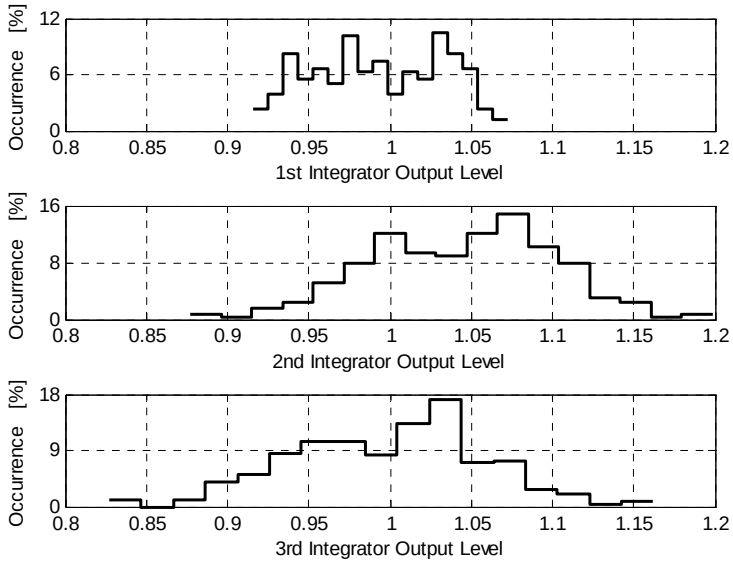

Fig. 5.25: Single-ended output level distribution for the integrators (same specifications as in Fig. 5.24)

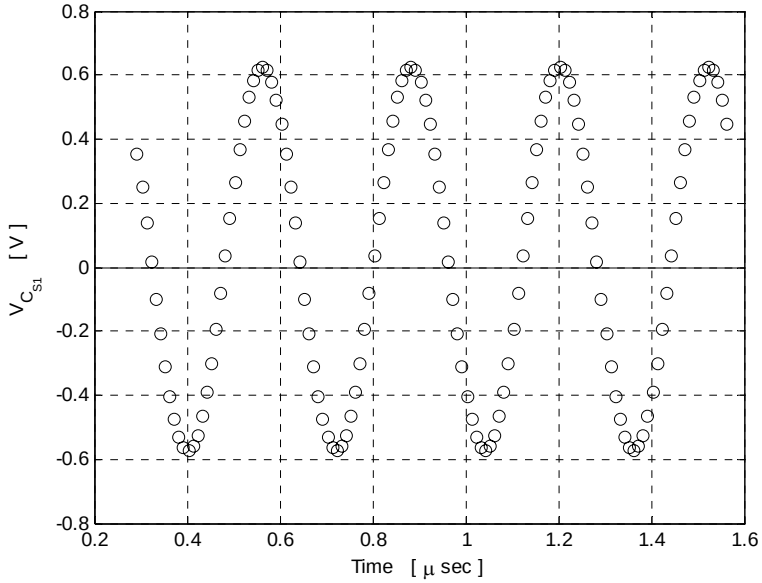

Fig. 5.26: Sampled signal on C_{S1} (single-ended)

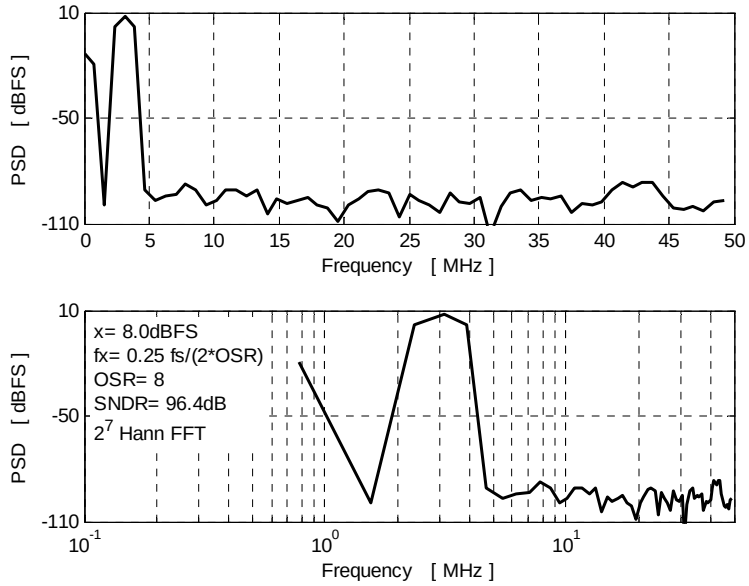

Fig. 5.27: Spectrum for the single-ended sampled signal on C_{S1}

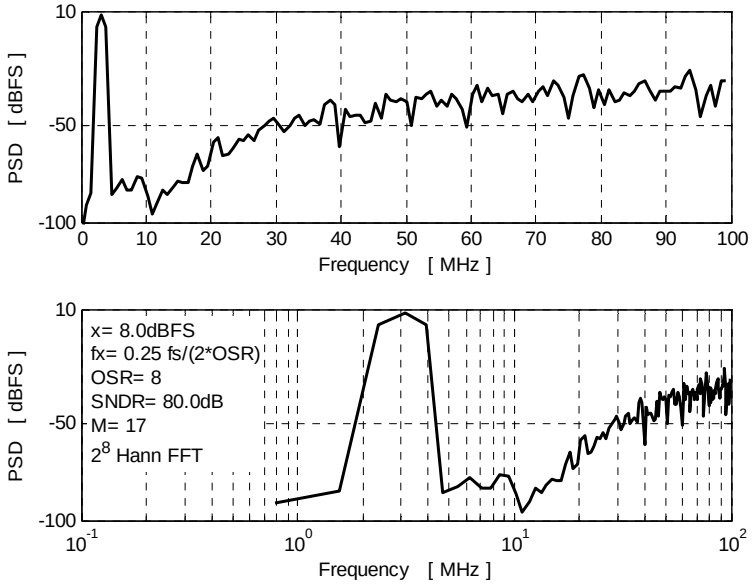

Fig. 5.28: Output spectrum for the ΔΣ modulator in DIFF mode

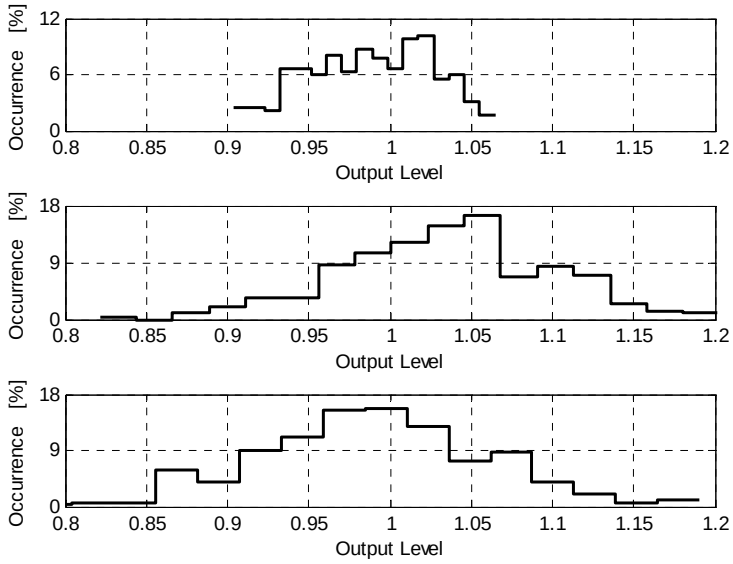

Fig. 5.29: Single-ended output level distribution for the integrators (same specifications as in Fig. 5.28)

5.4 Experimental Results

This section describes the evaluation methodologies and results for the test chip. First, the test chip is briefly described. Then, the test setup and equipment used are explained. Finally, experimental results are presented.

5.4.1 Test chip

The configurable ΔΣ modulator is implemented in 0.18μm single-poly, 6-metal CMOS process. In addition, the process includes the *metal-insulator-metal* (MIM) capacitor and deep n-well options, both of whom are used in the modulator. The chip active area is 1.8mm^2 and the total area is 3.96mm^2 as shown in Fig. 5.30. The die is packaged in a 44-pin *Ceramic Quad Flat pack* (CQFP) package.

All reference voltages required by the modulator are generated off-chip and decoupled off-chip and on-chip to stabilize them. Since constant current biasing is used for the modulator, off-chip resistors are used to generate the biasing voltages. Separate analog, digital, and I/O supplies and grounds are used to minimize noise coupling between the different domains. In addition, the non-overlapping clock generator circuit uses a dedicated supply and ground to give extra controllability over the chip for testing purposes. Multiple pins are allocated to supply and ground lines.

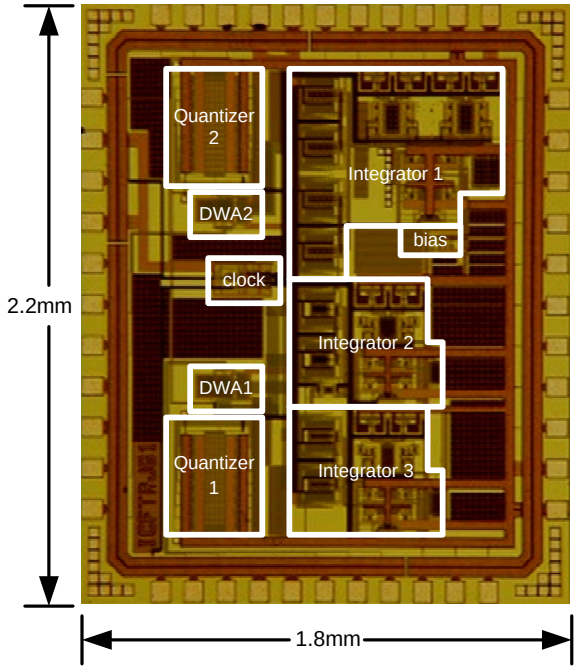

Fig. 5.30: Die photo

5.4.2 Test setup

The diagram of the test setup of the *device under test* (DUT) is shown in Fig. 5.31. The *printed circuit board* (PCB) is a 4-layer board with FR4 dielectrics between layers. The top side is used for signal, clock, reference routing and component mounting. The second and third layers are

used for ground and power planes respectively. The bottom side is used for routing and component mounting.

Separate power split planes are used to isolate the analog, digital, I/O, and clock supplies. In addition, the reference voltage generators use a separate split plane to separate their power consumption from the DUT. The voltage for each plane is generated by a linear voltage regulator (LM1117). All voltage regulators are powered by a single DC Power Supply (Agilent E3620A).

The reference voltages are generated using resistive dividers from a linear voltage regulator. They are then buffered using rail-to-rail input and output opamps (OPA2364) in the voltage follower configuration. Reference currents (I_{ref}) are generated with adjustable off-chip resistors. A crystal oscillator (SG51P) is used for the clock reference.

The differential input-signal to the ΔΣ modulator is generated using a differential function generator (DS 360). The generator outputs are filtered at the DUT inputs with a first-order RC low-pass filter. The digital outputs from the chip are captured using a logic analyzer (Tektronix TLA714). Then, data are transferred to a computer where they are processed using Matlab.

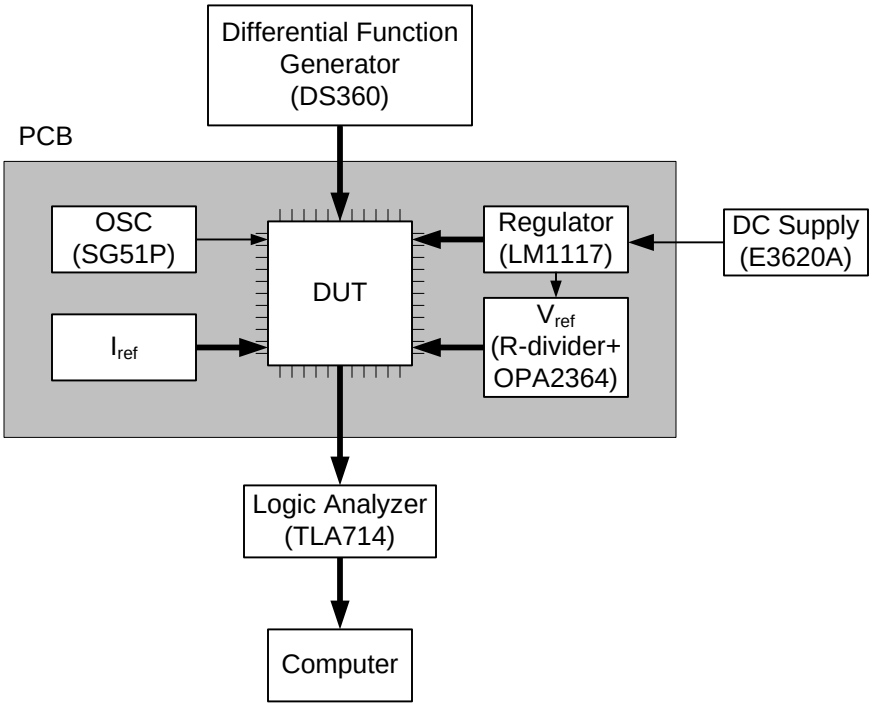

Fig. 5.31: Test setup

5.4.3 Measured performance

The test chip is designed to operate at 200 MHz sampling rate, unfortunately, the testing is carried out at 20 MHz clock. This is due to problems with the PCB and delays in the chip fabrication. However, some of the important concepts of the DIFF ΔΣ modulator can be verified from the current test chip.

The trouble with the PCB is the coupling of the clock signal into the DAC references. The coupling has a tremendous effect on the modulator performance since the DAC voltages feed into the input of the modulator. The problem was reduced by adding extra decoupling capacitors on the reference lines. To illustrate the effect of the extra decoupling capacitors, consider the output spectrum for the modulator in the feedback mode before adding the extra decoupling as shown in Fig. 5.32. At 5MHz clock, the in-band noise power is close to the expected value. However, as the clock frequency increases, the in-band noise power increases. On the other hand, the performance of the modulator improves with the extra decoupling capacitors as show in Fig. 5.33. The noise floor is maintained at the expected level with higher clock rates (note that the maximum crystal oscillator frequency available is 65MHz).

Although the noise floor with zero input follows the expected performance at high speed, the behavior of the modulator with a sinusoidal input shows increasing distortion with higher clock rates. The performance remains good at the 20MHz sampling. The distortion starts to increase at the next available crystal oscillator clock of 40MHz. Therefore, the characterization of the ADC is done at the 20MHz speed. Measurements were not performed at the maximum operating speed of 200MHz.

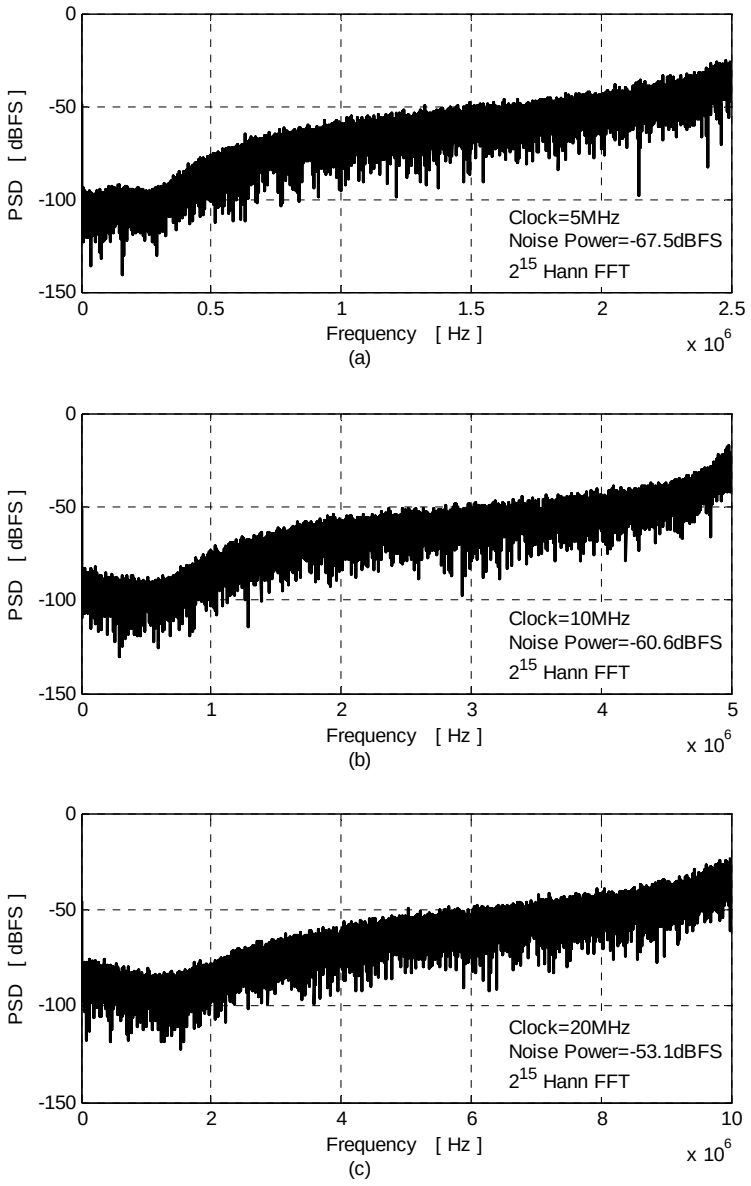

Fig. 5.32: Output spectrum before improving the decoupling on the DAC references for zero input-signal with a sampling clock at (a) 5MHz (b) 10MHz (c) 20MHz

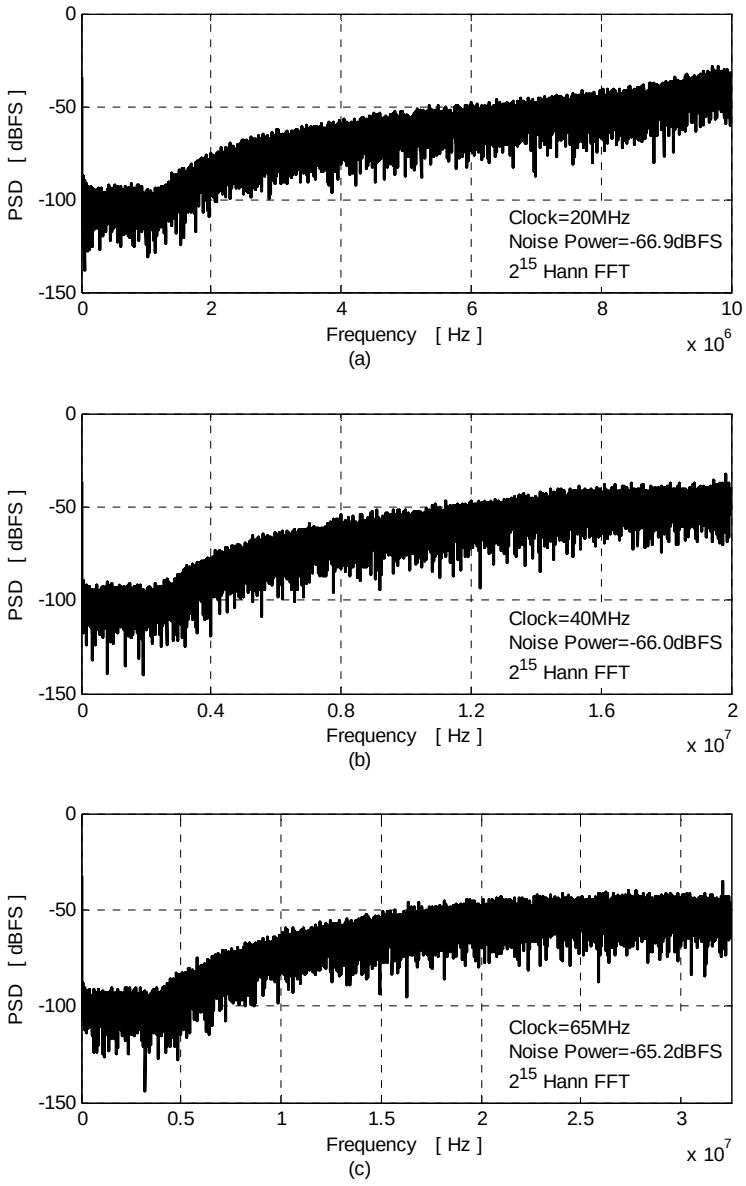

Fig. 5.33: Output spectrum after improving the decoupling on the DAC references for zero input-signal with a sampling clock at (a) 20MHz (b) 40MHz (c) 65MHz

To investigate the effect of the off-chip reference voltage generator, the ΔΣ modulator is simulated in the DIFF mode with a 5 nH inductance between the DAC reference and the switched capacitor circuit. The inductance simulates the effect of the improper decoupling network on the references. The achievable SNDR is degraded and harmonic distortion appears in the output spectrum as shown in Fig. 5.34.

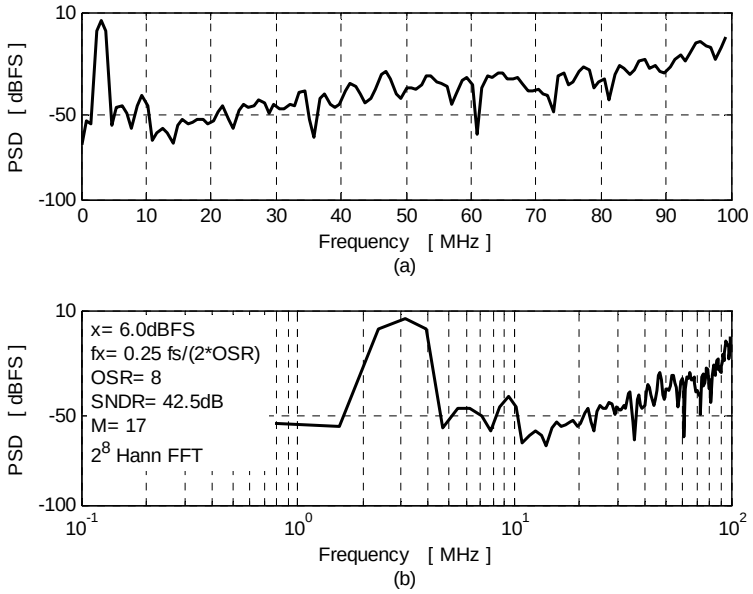

Fig. 5.34: Sample output spectrum for the ΔΣ modulator in DIFF mode (a) linear scale (b) log scale

The measured performance of the configurable ΔΣ modulator is summarized in Table 5.10. The DIFF modulator consumes more power than the feedback modulator, however, it can achieve better resolution. The improvement in the performance of the DIFF modulator is reflected in its *figure of merit* (FOM) which is less than half of that achieved by the feedback topology. Note that the reported power consumption is half the expected number for the 200MHz operation. The reduction is achieved by simply reducing the biasing current. The power is reduced because the large bandwidth achieved with the original power consumption is not required for the low sampling speed.

Table 5.10: Summary of the measured performance for the ΔΣ modulator

	DIFF ΔΣ	Feedback ΔΣ
Voltage supply	1.8 V	1.8 V
Sampling frequency	20 MHz	20 MHz
OSR	8	8
Signal bandwidth	1.25 MHz	1.25 MHz
Analog power consumption	19 mW	17 mW
Digital power consumption	3 mW	2 mW
Total power consumption	22 mW	19 mW
Differential input range (at maximum SNDR point)	2 V_{p-p} [1] 2.59 V_{p-p} (max)	0.62 V_{p-p}
Peak SNR	74.9 dB [1] 77.1 dB (max)	65.9 dB
FOM [power/$2^{(SNR-1.76)/6.02}$/(2*BW_{signal})]	1.9 pJ/step [1] 1.5 pJ/step (min)	4.7 pJ/step
Peak SNDR	72.5 dB [1] 73.7 dB (max)	64.3 dB
FOM [power/$2^{(SNDR-1.76)/6.02}$/(2*BW_{signal})]	2.6 pJ/step [1] 2.2 pJ/step (min)	5.7 pJ/step

[1] These numbers are for the DIFF ΔΣ modulator operating in the region where the input-level does not overload the external ADC (ADC_2).

As pointed out in chapter 4, one of the main advantages of the DIFF topology is increasing the achievable SNR by allowing a larger input-signal. This benefit is illustrated by the measured SNR versus input-signal level in Fig. 5.35 and by the measured SNDR versus input-signal level in Fig. 5.36. For example, the maximum SNR occurs at -3.3 dBFS input-signal for the feedback modulator and at 8 dBFS input-signal for the DIFF modulator which translates to 11 dB improvement in SNR.

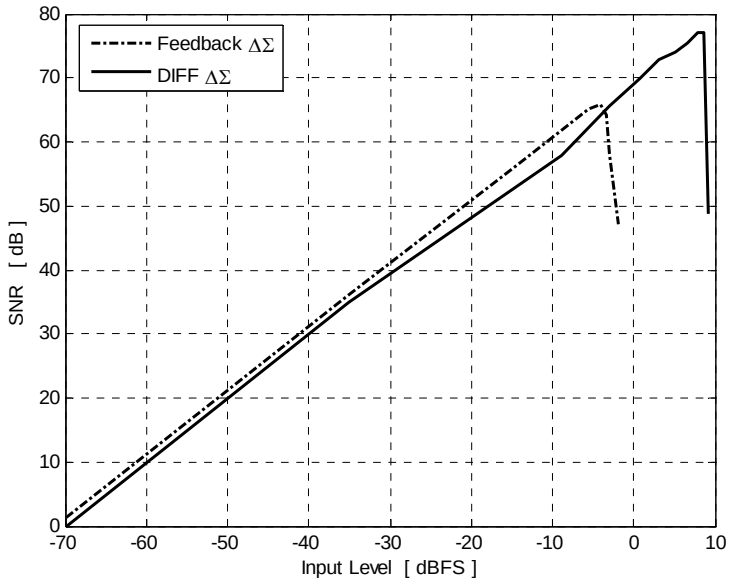

Fig. 5.35: Measured SNR versus input-signal level

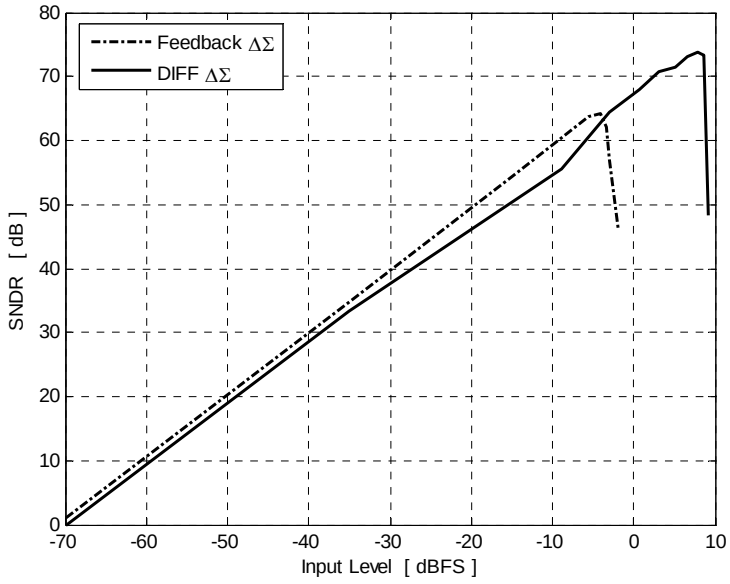

Fig. 5.36: Measured SNDR versus input-signal level

The internal nodes of the DIFF modulator contain quantization noise only. Although this feature is difficult to verify for all three opamps in the modulator, it can be confirmed for the third opamp. This is because the test structures that are needed for the first two opamps would increase the loading and hence the power consumption in addition to increasing the silicon area. However, the third opamp output is quantized and processed off-chip and therefore its distribution can be

analyzed. By confirming the output of the third opamp, we can deduce the validity of the quantization noise only feature for the other opamps.

The 17-level outputs of the third opamp are shown for a zero input-signal from both configurations in Fig. 5.37. As expected, the outputs are normally distributed since the input is thermal noise. When the input is increased to -4.1 dBFS (maximum SNR point for the feedback modulator), the output distribution for the DIFF modulator shows a similar characteristics to that with zero input as shown in Fig. 5.38. However, the feedback modulator distribution shows more occurrences at the reference limit which indicates that the modulator is getting closer to overloading. As the input in increased further to 6.0 dBFS (maximum point before the external quantizer overloads in the DIFF modulator), the DIFF modulator still shows a similar distribution to that with zero input as shown in Fig. 5.39. The feedback modulator is unstable at this input-signal level. Finally, for an input of 8.3 dBFS (maximum SNR point for the DIFF modulator), the output distribution shows more occurrences at the reference limit as shown in Fig. 5.40.

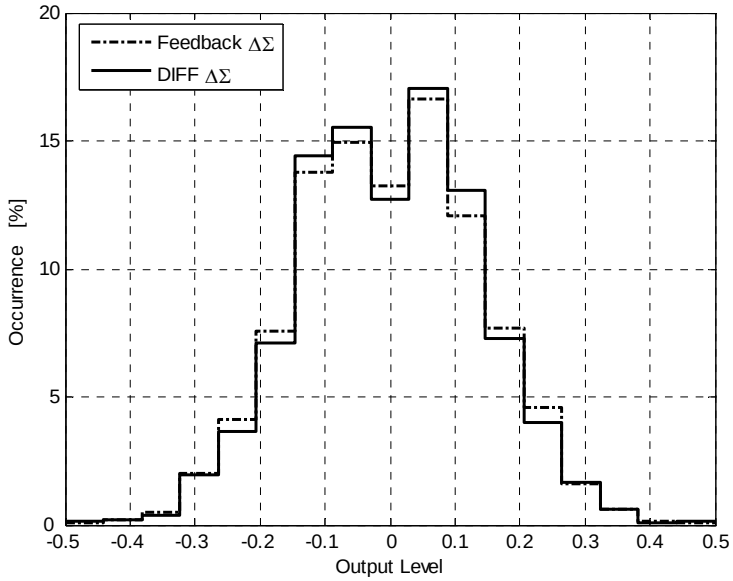

Fig. 5.37: Measured output level distribution for zero input-signal

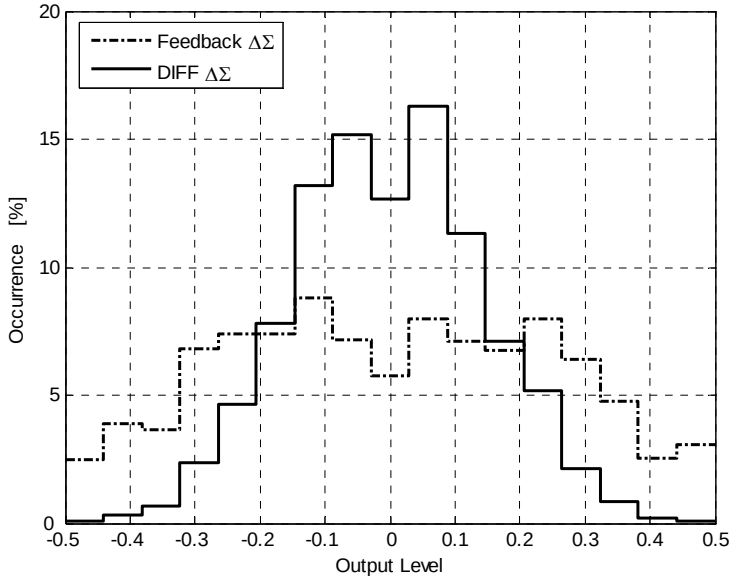

Fig. 5.38: Measured output level distribution for -4.1 dBFS input-signal (maximum SNR point for the feedback modulator)

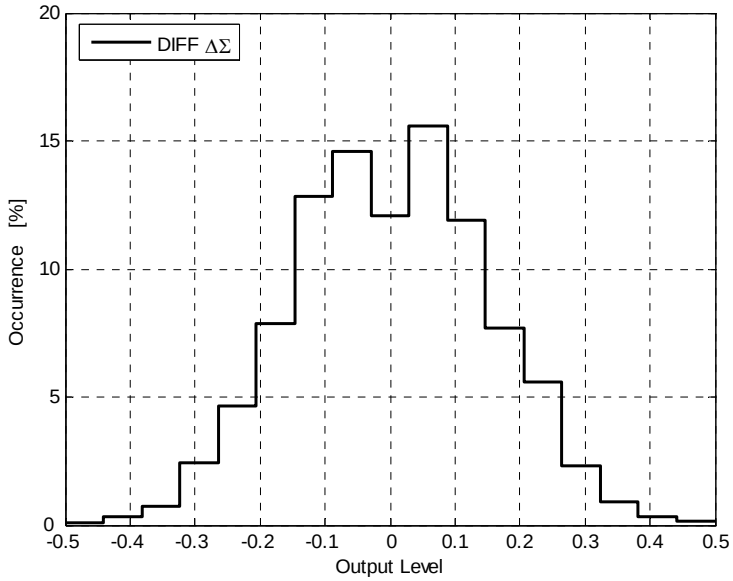

Fig. 5.39: Measured output level distribution for 6.0 dBFS input-signal (maximum level before the external quantizer is overloaded in the DIFF modulator)

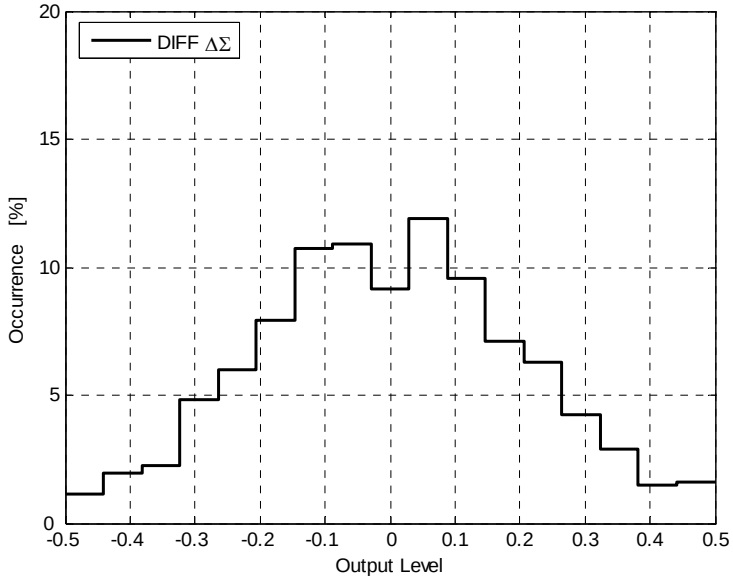

Fig. 5.40: Measured output level distribution for 8.3 dBFS input-signal (maximum SNR point for the DIFF modulator)

The output spectrum for the two configurations at their maximum SNDR (maximum SNR occurs at the same input-level) is shown in Fig. 5.41 and Fig. 5.42. The input frequency is at 100 kHz and with amplitude of -4.1 dBFS for the feedback modulator and 8.3 dBFS for the DIFF modulator. More samples of the output spectrum for both modulators are shown in Fig. 5.43 and Fig. 5.44 for a small input-level.

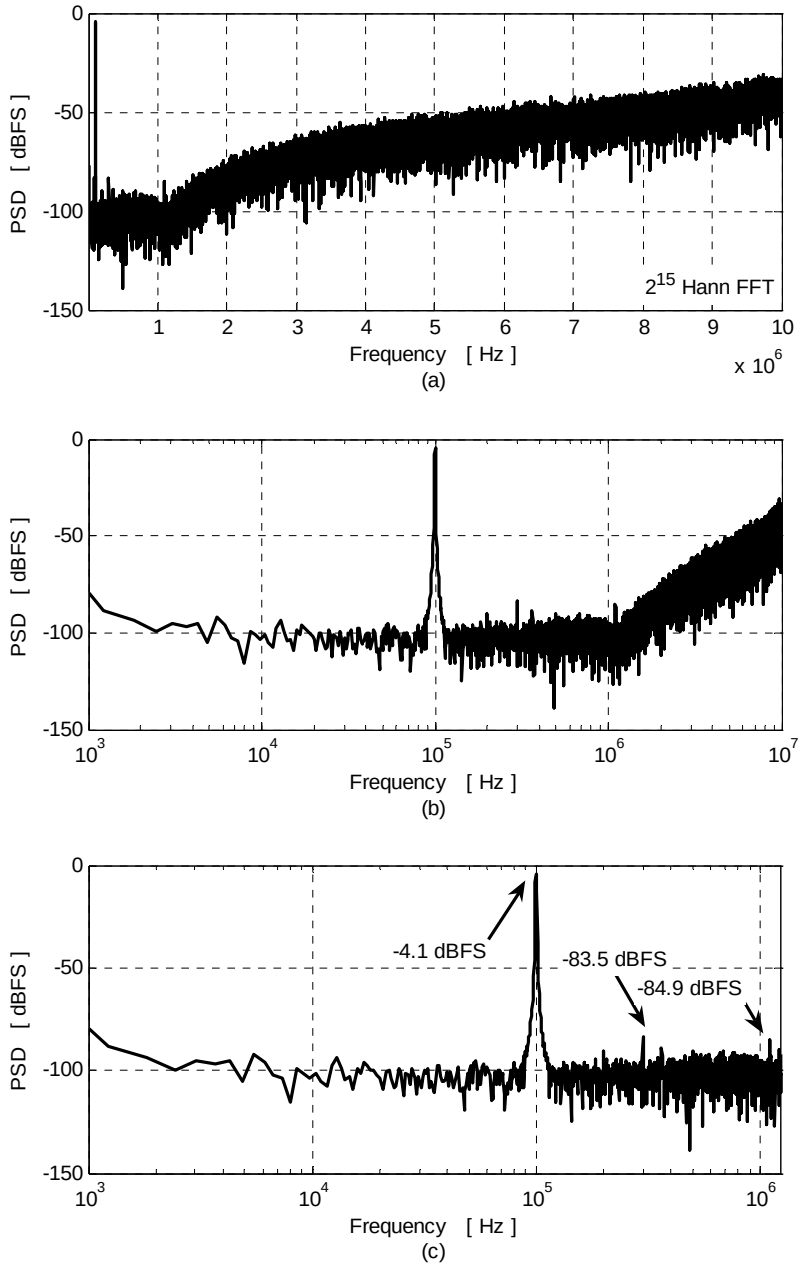

Fig. 5.41: Sample output spectrum at peak SNR and SNDR for the feedback ΔΣ modulator (a) linear scale (b) log scale (c) signal band in log scale

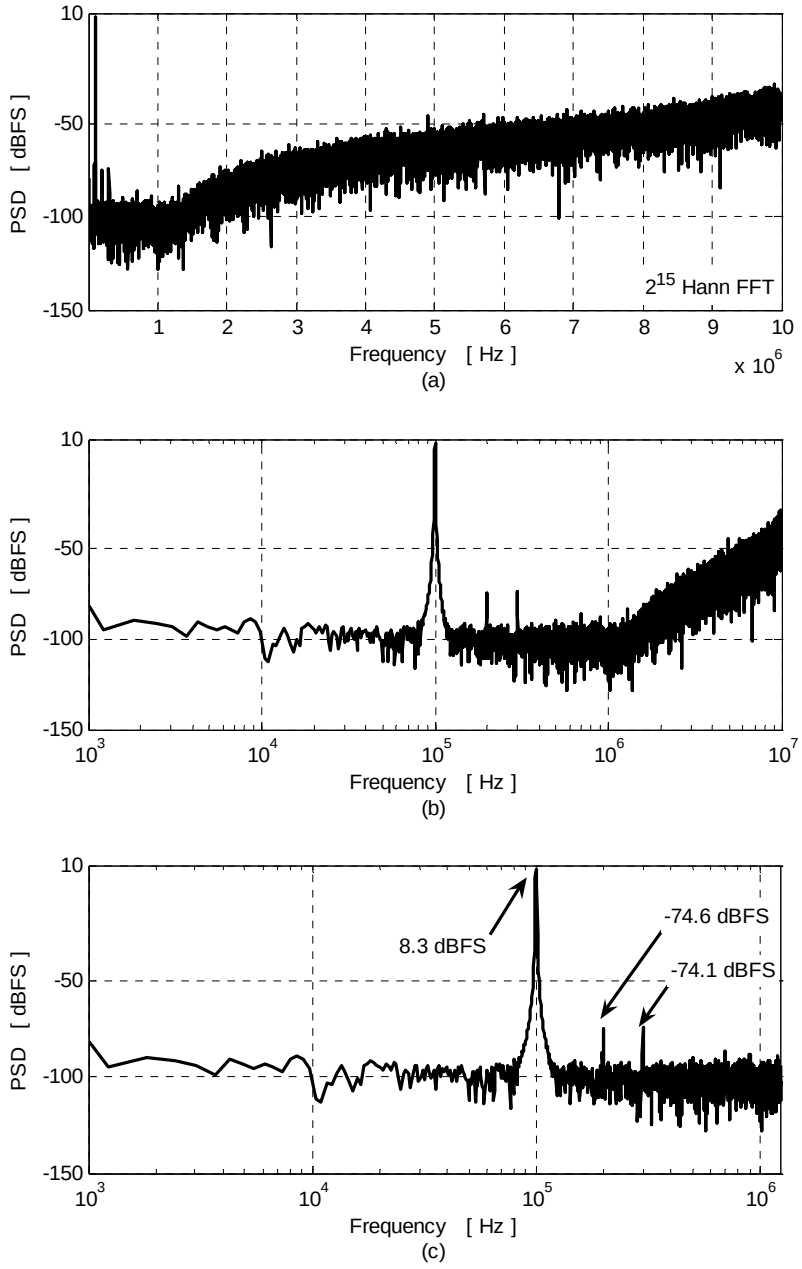

Fig. 5.42: Sample output spectrum at peak SNR and SNDR for the DIFF ΔΣ modulator (a) linear scale (b) log scale (c) signal band in log scale

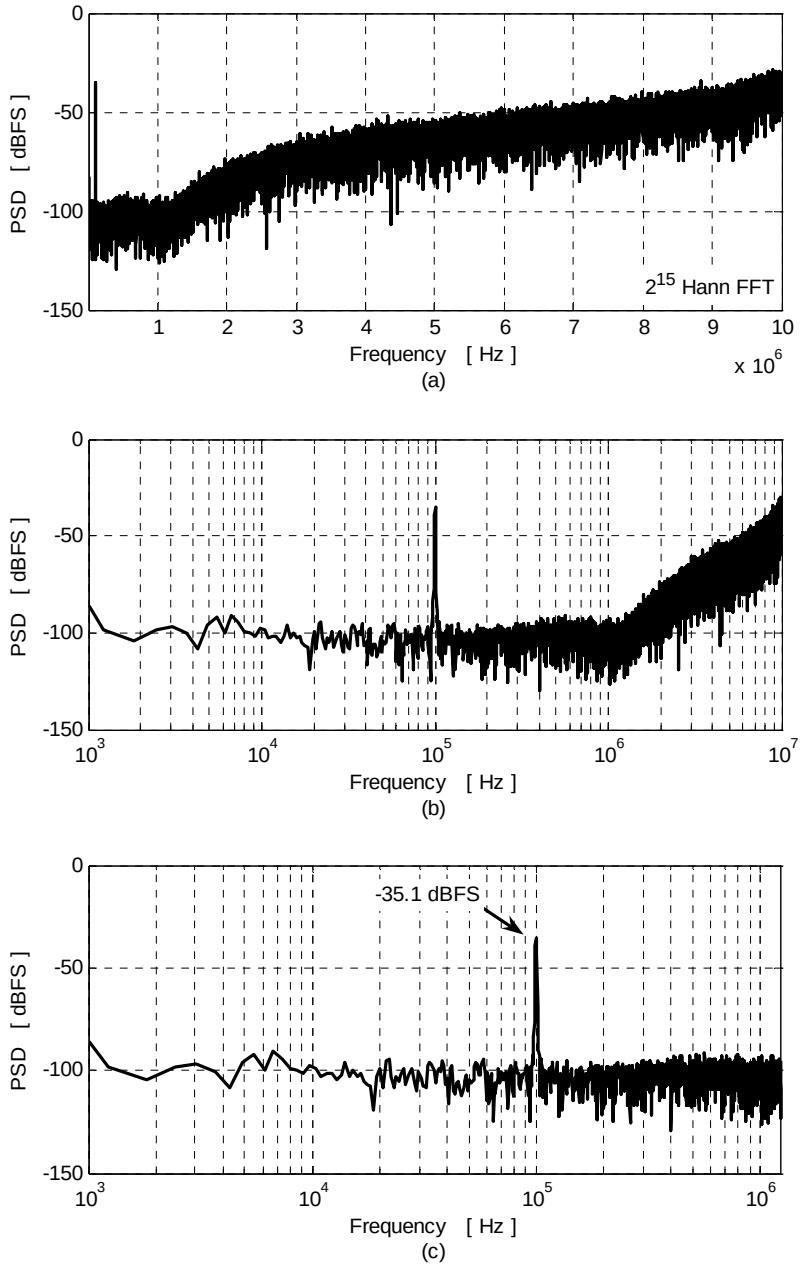

Fig. 5.43: Sample output spectrum for the feedback ΔΣ modulator (a) linear scale (b) log scale (c) signal band in log scale

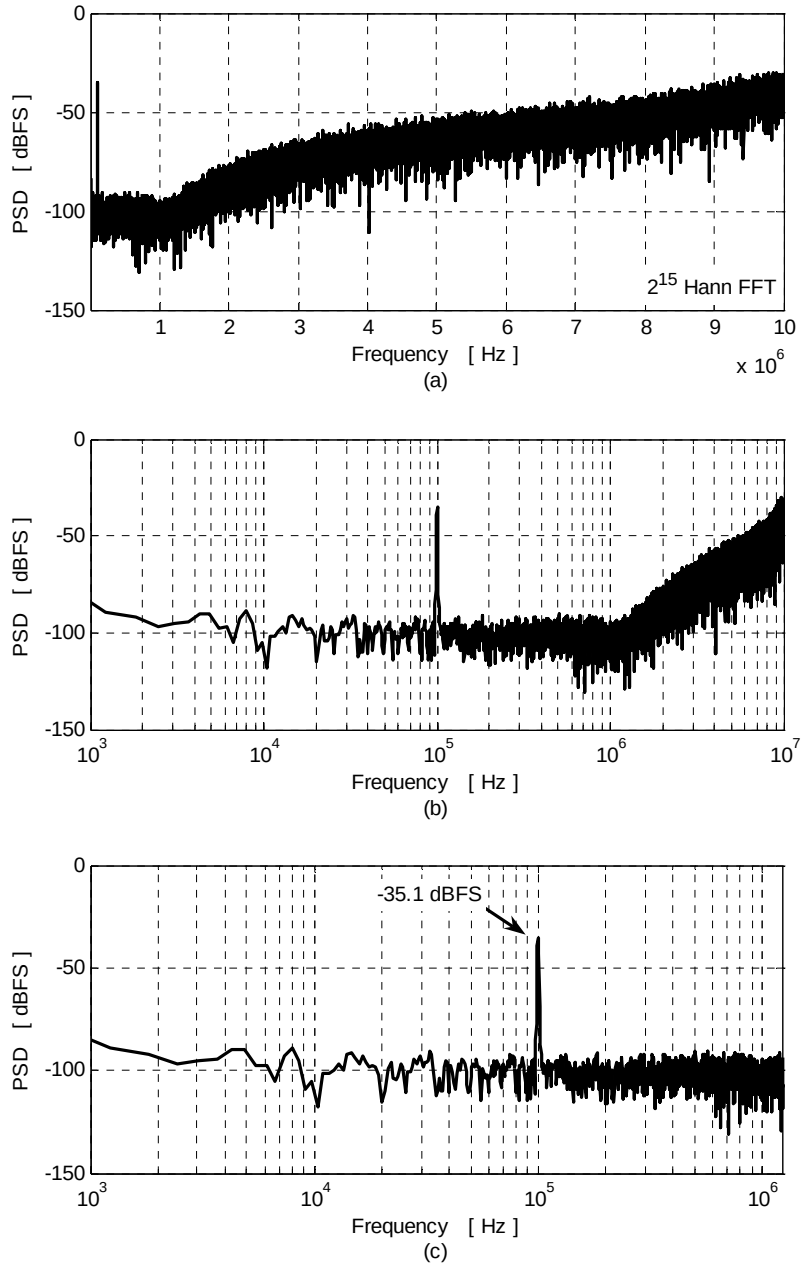

Fig. 5.44: Sample output spectrum for the DIFF ΔΣ modulator (a) linear scale (b) log scale (c) signal band in log scale

5.5 Summary

The system level design of the configurable experimental modulator is described. The configurability allows the modulator to operator in the traditional feedback mode or in the DIFF

mode. The system is then mapped into an equivalent switched-capacitor circuit. The mapping is verified using several open-loop and closed-loop tests. Finally, the circuit level implementation of the building blocks is discussed.

The configurable ΔΣ modulator is implemented in 0.18μm CMOS technology to evaluate the DIFF concept and compare it to the feedback modulator. Both topologies are tested at 20 MHz with an OSR of 8 and powered from 1.8 V supply. The DIFF modulator achieves 77.1 dB peak SNR (73.7 dB peak SNDR) which is 11.2 dB (9.4 dB) better than the feedback modulator at the expense of 15% increase in power consumption. Therefore, the energy required per conversion step for the DIFF architecture is less than half of that required by the feedback architecture.

Measured results prove some of the main characteristics of the DIFF topology. First, the input-signal amplitude is larger than the feedback modulator. Second, in region one of operation, the DIFF modulator processes quantization noise only.

Chapter 6:

Conclusion

THIS chapter summarizes the thesis and outlines its main contributions. In addition, areas of research for future exploration are recommended.

6.1 Summary

The trend of moving more of the signal processing to the digital domain will continue. This is mainly due to the robustness and small size of digital circuits which enables the design of dense and complex systems. Moreover, advanced CMOS technology is aiding digital circuits by making them smaller and faster. On the other hand, analog circuits suffer due to the scaling of voltage supplies in modern technologies. However, those sophisticated digital circuits still need to interface to the analog world. Therefore, the analog-digital interface must evolve to keep up with the increasing demands from new applications and technologies.

One of the critical parts of the analog-digital interface is the analog to digital converter. ΔΣ modulators have proven to be less sensitive to analog imperfections than other types of ADCs. Unfortunately, their relaxed requirements come at the cost of speed. Moreover, nano-scale CMOS has proven to be a hostile environment for analog circuits in general including ΔΣ modulators. This work has sought to devise new architectures to improve the speed of ΔΣ modulators and enable their implementation in low voltage environment.

6.2 Contributions

The key contributions of this thesis are:

1) Single-path time-interleaved ΔΣ modulators [39]: Two procedures are presented to derive the SPTI ΔΣ topology. The effects of removing the demux at the modulator input are discussed. Next, the main limitation of the SPTI topology is identified to be the mismatch between the NTFs of the internal quantizers due to finite opamp gain and bandwidth. The NTF matching requirements can be relaxed by using a hybrid time-interleaved modulator where the first stage is multi-path and the later stages are single-path. Alternatively, a digital-calibration

technique is proposed to mitigate the NTF mismatch problem. Finally, mismatch shaping for multi-bit DAC in the SPTI is investigated and a method to minimize the mismatch effect is proposed.

2) The identification of the drawbacks of input-feedforward ΔΣ architectures and the introduction of techniques to overcome them [21]: Low swing and low distortion in input-feedforward topologies are useful characteristics. However, this desirable behavior comes with some drawbacks, namely: the critical path and the analog adder at the quantizer input. The double sampled input technique is proposed to remove the critical path problem. And the capacitive input feedforward is proposed to eliminate the analog adder.
3) Digital input-feedforward ΔΣ modulators [31]: The proposed DIFF ΔΣ topology has several advantages. First, its internal nodes have low swing and low distortion characteristics. Second, it eliminates the analog adder at quantizer input. Third, it improves in the achievable SNDR via the utilization of the inter-stage gain and the appropriate choice of the levels and reference voltage of the external quantizer. In addition, although the extra circuits increase the power consumption, the energy required for each conversion step is smaller due to improved resolution. On the other hand, good matching is required between the analog path and the digital path of the external quantizer to eliminate the added quantization noise.
4) Switched-capacitor circuit implementation: A configurable ΔΣ modulator which can operate as a feedback modulator or in DIFF mode is implemented in 0.18μm CMOS technology. The test chip allows the verification of the DIFF architecture and facilitates the comparison between the traditional feedback ΔΣ topology and the DIFF ΔΣ topology.

6.3 Future research

There are several areas that can be further investigated:

1) Several new time-interleaved topologies were introduced. The design and implementation of theses topologies to enable their evaluation is of great interest. A configurable modulator can be built to facilitate the assessment of several time-interleaved modulators.
2) The calibration method presented to overcome the NTF mismatch problem in the SPTI modulator forces the error for the worst NTF to zero. This zero forcing calibration improves the resolution but does not fully recover the achievable performance if the opamps were ideal. It is interesting to investigate a better calibration criterion where the error from the aggressor NTF is not completely cancelled. Alternatively, the calibration should attempt to make the NTF mismatches equal for all quantizers. It is likely that the mismatch minimization criterion would result in better performance.

3) The double sampled input and the capacitive input feedforward techniques can simplify the design of input feedforward topologies. It is interesting to design an experimental modulator incorporating these techniques to demonstrate their advantages. Additionally, a modulator without these techniques but with the same performance can be implemented to enable a fair comparison.
4) The DIFF architecture requires matching between the analog and the digital domains. In the experimental modulator, the matching is achieved through making the analog path match the digital path by designing better analog circuits. Investigating calibration techniques that attempts to make the digital path mimic the non-ideal analog path is important. The digital calibration relaxes the requirements imposed on the analog building blocks and makes the DIFF topology more attractive especially in modern CMOS technologies.
5) The DIFF ΔΣ modulator with delay in the external ADC path presents an interesting modification. Half a unit delay in the external quantizer eliminates the critical path in the DIFF topology and allows more processing time for quantization, DEM and DAC. Unlike double sampled input, the delaying technique allows for easy sharing of sampling and feedback capacitors. Sharing the capacitors reduces power consumption and improves the efficiency of the modulator.
6) The possibility of including delay in the external ADC path can be exploited to map the DIFF topology into the continuous-time domain where delay is inevitable. The delaying external ADC topology can be utilized for the realization of a continuous-time DIFF ΔΣ modulator.
7) The experimental modulator is fabricated in 0.18μm CMOS technology. The low swing and low distortion advantages of the DIFF architecture makes it very attractive for implementation in the low voltage environment of modern CMOS technology. Future research can target implementing the DIFF modulator in a more modern technology and operating from a lower supply.

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