DESIGN OF HIGH ACCURACY POWER SCALABLE MEMS SENSOR INTERFACE

by

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Graduate Department of Electrical and Computer Engineering
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ABSTRACT

A TECHNIQUE to improve power scaling efficiency of automotive MEMS pressure sensor interfaces is presented. The overall power consumption of the interface is inversely proportional to the square of the amplitude and directly proportional to the input bandwidth. Power scaling with respect to amplitude is achieved by using a novel technique of cascading gain stages through an input gain-select mux, which scales better than previous approaches. Power scaling with respect to input bandwidth of the sensor is achieved through periodic power-down of the interface. A prototype of the interface was fabricated in a $1.8V$, $0.18\mu m$ CMOS process. Its power consumption scales between $4\mu W - 5.33mW$, while maintaining a Spurious Free Dynamic Range (SFDR) range of approximately $72 - 92dB$, a Total Harmonic Distortion (THD) range of $70 - 90dB$, and an input referred noise of $170.0nV/\sqrt{Hz}$.

Acknowledgment

All Praise is Due to God, The Most Gracious, The Most Merciful

THIS work would not have been possible without the guidance, help, and support of those who I have come to cherish as teachers, mentors, friends, and family. I would like to thank Professor David Johns, who had guided me throughout my Masters tenure, and has contributed significantly into shaping me to become a mixed signal designer, and a researcher. His faith in my abilities, and his expectations of excellence have driven me to heights I would not have reached otherwise. I would also like to thank professor Kenneth Martin, who, although is not my supervisor, would never let an opportunity pass without lending me his sincere feedback, and advice. I would also like to thank Johan Vanderhaegen and Christoph Lang from BOSCH Research and Technology Center (RTC), who funded and collaborated with us in this project. I am also immensely indebted to the 'PhD Group' who I consider my mentors: Imran Ahmed, Ahmed Gharbiya, Trevor Caldwell, and Bert Leesti. Their support and mentorship was a key factor in the success of this project. I would also like to thank the pillars that brought me into this world, my mother and father, who willingly sacrificed more than I could ever repay them, to make me into the man I am today. Finally, saving the best for last, I would like to thank my dear and beloved wife, Samar, who has brought focus into my life, and through her love and support, helped me through the tough times of this project. I sincerely hope I am able to be as good to the people who have been good to me, and who contributed to my growth as a person, and as an engineer.

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Chapter 1

Introduction

1.1 Motivation

THE use of electronic systems in cars have increased rapidly over the last decade [1]. Some of the most important developments in the field of automotive electronics have been in the field of automotive sensors. Currently, there are over 100 different kinds of sensors in automobiles, which serve a variety of different functions: safety, comfort, and drivetrain [2]. Figure 1.1 shows an example of the different kinds of sensors in a car [3]. To put the automotive sensor market in perspective, we will mention other market sectors here. The sensor market can be categorized as follows:

- machinery manufacturers
- processing industries
- aircraft and shipbuilding
- construction sector
- consumer electronics and applications
- automotive
- other

The automotive sensor market is worth $10.5 billion, which is 25% of the total sensor market, making it the largest of all the other segments. In terms of projected growth, the overall sensor market is expected to grow by 4-5% by 2010, and the expected growth for the automotive sensor market ranges from 5.1% to 7.5%. As such there is huge driving force for automotive electronics, which is strongly coupled to the market drive for sensors.

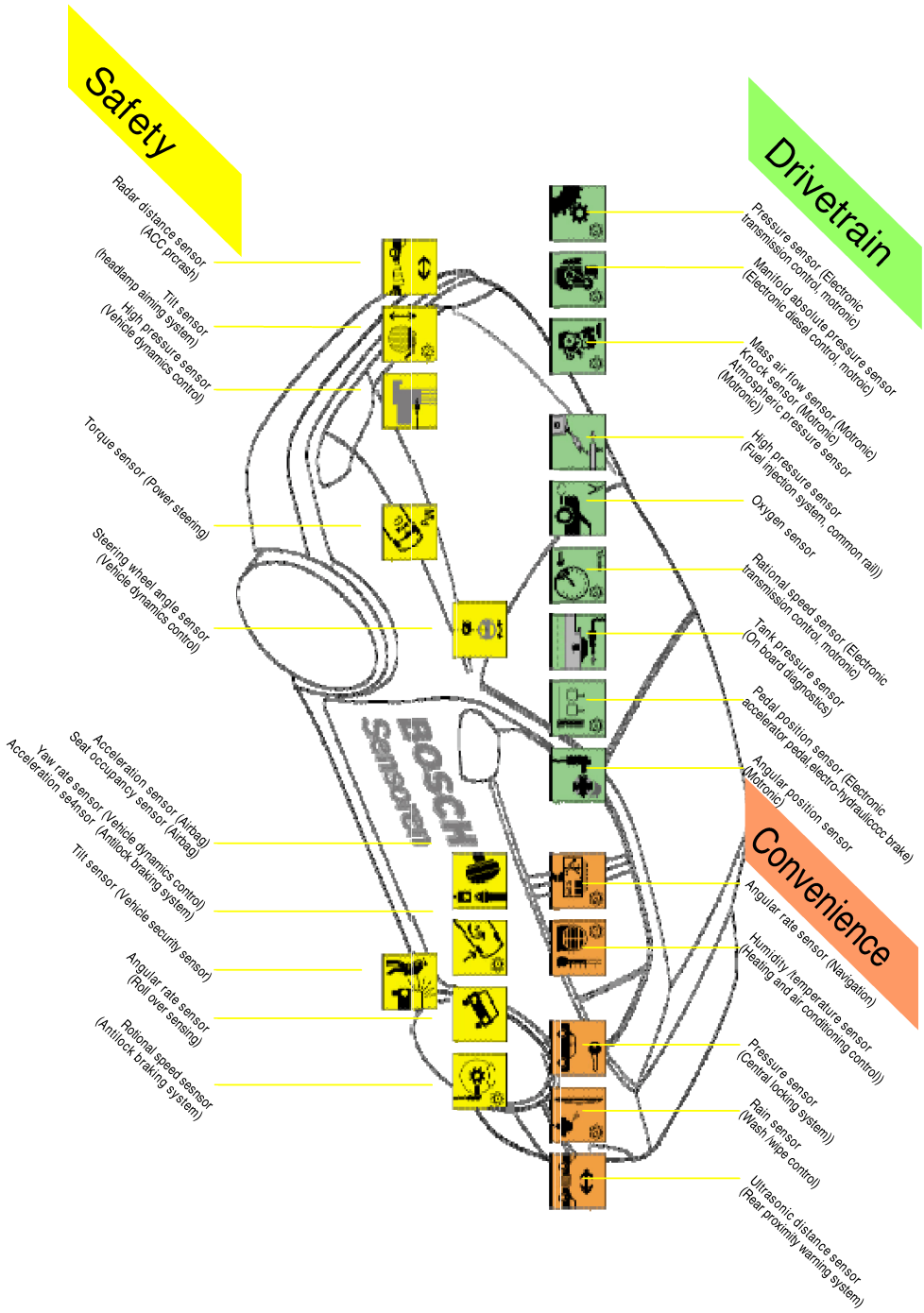


Figure 1.1: Sensors in a modern car (Acquired from BOSCH RTC [1])

Because cost pressure on all automotive components are high, low-cost, high-volume processes are a pre-requisite for automotive electronics, including sensors. Because each sensor needs to be specifically designed for a particular function in the vehicle, generally the electronics needed to interface with the sensor were custom designed as well, in terms of accuracy, and power. This has led to a new drive to build power-scalable electronics, which allows one design to be used in a multitude of applications, and be optimal for each.

This work focuses on building a novel power scalable sensor interface, whose power scales with both frequency and input signal amplitude. The interface is designed to be implemented for different types of sensors, and hence a wide range of sensor output amplitudes ($40mV_{pp}$ - $400mV_{pp}$) and frequencies (0.5Hz - 0.5kHz) [4]. In sensor applications, the front-end circuitry consumes most of the power, and hence is the bottleneck for low power applications. By making the interface power scalable, the entire system becomes power efficient. This work is part of a larger integrated system of advanced MEMS pressure sensor for automotive electronics, as well as low power consumer applications, such as altimeters [1]. This project was proposed by BOSCH Electronics as part of an effort to design an ultra-low power 14 bit Oversampling Analog to Digital Converter (ADC) for sensor applications. BOSCH is the largest MEMS producer in the world, especially in the automotive sector. Figure 1.2 shows the volume of automotive MEMS sensors produced by BOSCH by 2003 in Millions per annum (Mio/a). This work has potential to increase their

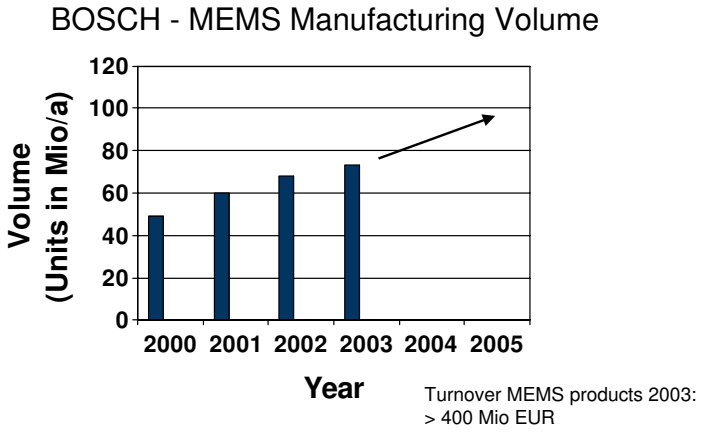


Figure 1.2: BOSCH's MEMS sensor production volume (Acquired from BOSCH RTC [1])

profit margins by reducing design time of making customized electronics for each sensor application. Moreover, because of economies of scale, the design can be produced in larger quantities, which reduces the cost per unit.

1.2 Thesis Outline

In this dissertation, the development of a 14 bit, power scalable PGA (Programmable Gain Amplifier) as a sensor interface is discussed. In chapter two, we discuss the design of pressure sensors in detail, design considerations in sensor applications, such as $1/f$ noise cancelation techniques, as well as high accuracy ADC architectures compatible with power-scalability. The third chapter discusses the system design methodology for the power scalable PGA, by examining and comparing alternative architectures. Power scalability techniques are also described from a system level perspective. The fourth chapter describes the circuit implementation of the power-scalable PGA, which includes the design of the chopper amplifier, and the Power Resettable OPAMP. Key simulation results, and design limitations are also described in this section. Chapter 5 in this dissertation describes the measured results, and in chapter 6 we provide key conclusions from this project, and briefly describe potential future research topics.

Chapter 2

Background

THE nature of sensors is that they convert one type of energy into another that can be measured and used in different applications. As such, both the input energy, and the output signal of the sensor are analog signals. In the case of the pressure senor, the sensing element converts mechanical energy, into an electric signal. Since most high accuracy signal processing in the modern age is done in the digital domain, the sensor output signal needs to be converted to a digital signal by an Analog to Digital Convertor (ADC). Depending on the application, the signal may need to be amplified or buffered before it gets to the ADC, in order to reduce the ADC area, power or complexity requirements. Figure 2.1 shows a top level representation of the sensor system.

In this chapter, we will discuss, in detail, the background material needed to design

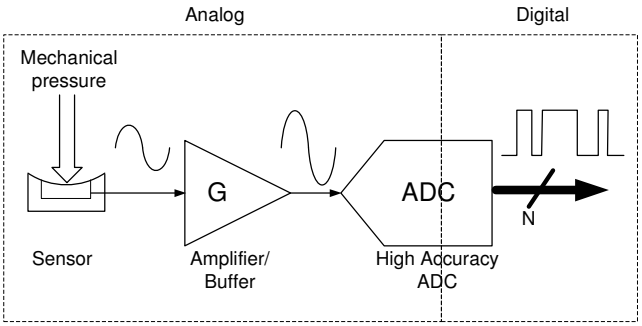


Figure 2.1: A typical sensor system

a high accuracy, power scalable PGA as a sensor interface. In section 2.1, we will first discuss the design and workings of the pressure sensor used in automotive and consumer electronics. In section 2.2, we will discuss some of the major design considerations in sensor applications, such as offset and $1/f$ noise cancelation techniques. Finally, in section 2.3, we will discuss the different types of ADC's that can potentially be used in sensor applications, and some tradeoffs between topologies when designing high accuracy power scalable systems.

2.1 Pressure Sensors

2.1.1 Pressure Sensor Applications and Requirements

As mentioned in the introduction, this work is part of a larger system of integrated pressure sensors for, primarily, automotive sensors, and for consumer electronics. In terms of the consumer electronics market, the primary application will be in altimeters. In automobiles, the pressure sensor is used in many places, some of which are:

- turbocharger pressure
- suspension
- oil pressure
- climate control
- fuel-tank pressure
- tire pressure
- brake-fluid pressure
- gasoline vapor pressure
- gasoline/diesel direct inject pressure
- Locomotive fuel inject pressure

Each of these applications have different requirements in terms of the required pressure range that needs to be measured, the accuracy of measurement, and the temperature range [2].

For altimeters, the requirements are to measure atmospheric levels at different heights relative to sea level, and over a narrow temperature range. Table 2.1 shows the atmospheric pressure, in Pascals, over the seven different atmospheric levels.

Table 2.1: Atmospheric Pressure ranges

Atmospheric Layer	***Height Above Sea Level (km)***	***Static Pressure (Pa)***	***Standard Temperature (^oC)***
0	0	101,325	15.0
1	11.0	22,632	-56.5
2	20.0	5,475	-56.5
3	32.0	868	-44.5
4	47.0	110.91	-3.5
5	51.0	66.94	-3.5
6	71.0	3.96	-58.5

Table 2.2: Automotive pressure sensor's pressure and temperature ranges

Application	***Full Scale Pressure (kPa)***	***Temperature Range (^oC)***
Gasoline vapor leakage	5.0	-30 to 120
Suspension	2,000	-30 to 120
Air-conditioning	3,500	-30 to 135
Gasoline/Diesel injection	20,000	-30 to 120
Locomotive fuel injection	200,000	-30 to 120

As for the automotive applications, applications mentioned above require a much larger temperature, and pressure range. Table 2.2 lists some of the automotive pressure sensor applications, with the their operating pressure and temperature requirements [5].

It is clear from the above two tables that automotive sensor requirements are more stringent than that of the altimeter. In terms of circuit requirements, the automotive electronics will require to be more robust over process corner and temperature than that for consumer electronics. However, consumer electronic circuitry will need to be low power, especially for hand-held altimeters that run off batteries. These requirements pose an interesting design challenge for this Power-Scalable Interface.

2.1.2 Pressure Sensor Types

There are three main types of pressure sensors: piezocapacitive, piezoelectric, and piezoresistive pressure sensors. The most common, and most used type of pressure sensor, especially in automotive application is the piezoresistive pressure sensor. The principle of the piezoresistive sensor, is that an applied pressure changes the electrical properties of

diffused resistors (called piezoresistors, or gages) [5]. The piezoresistive sensors will be explained in greater detail in the next section.

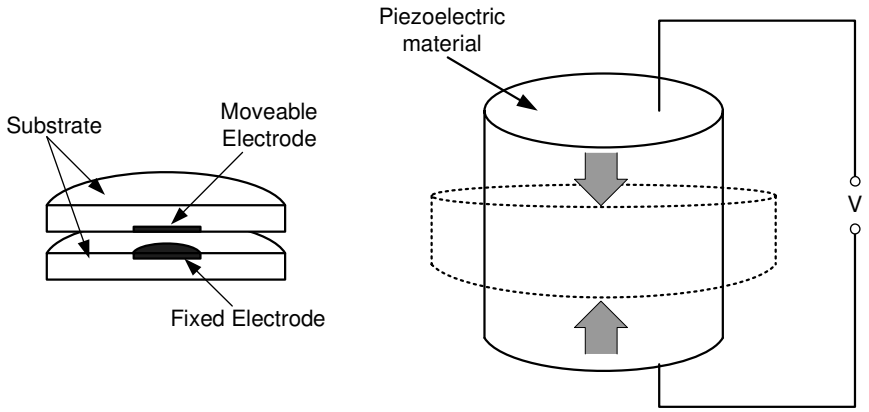


Figure 2.2: *(left)* A piezocapacitive sensor, and *(right)* a piezoelectric sensor

The piezocapactive sensor is shown in Figure 2.2. The two electrodes form a capacitance, which changes when a pressure is applied. When the diaphragm is distorted due to pressure, the width of the gap between the electrodes changes, which translates into a change of capacitance. That capacitance change can be measured by using an Opamp with a fixed feedback capacitor, as shown in Figure 2.3.

The principle of the piezoelectric sensor is also shown in figure 2.2. The applied pressure to an appropriate material distorts its shape, and generates a voltage which can be measured.

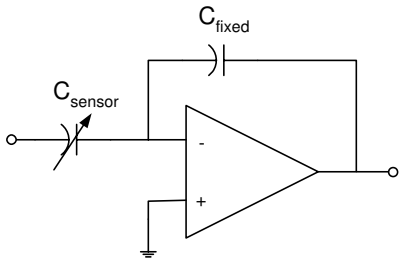


Figure 2.3: Measuring capacitance on piezocap sensor

2.1.3 Piezoresistive Pressure Sensor

As mentioned in the previous section, piezoresistive pressure sensors are the most commonly used types in automotive and consumer application, because of their high accuracy, and potentially low cost of manufacture. There are two types of piezoresistive pressure sensors: The silicon piezoresistive sensor, and the steel-substrate piezoresistive sensor. The silicon pressure sensor is used for low-medium pressure measurements, whereas the steel-substrate sensor is used in high-pressure applications. Figures 2.4 and 2.5 show the cross section of the steel-substrate, and silicon pressure sensors, respectively.

In terms of fabrication, the functional layers of any piezoresistive sensor are [5]:

- Substrate layer: The substrate is the transducer that detects strain, and is an important layer of the pressure sensor. Properties such as high resistance to corrosive material and low brittleness are important in enhancing the performance of the sensor.
- Isolation layer: This layer is to be used as insulation between the piezoresistors and the substrate. It also serves the function of transmitting the elastic deformations from the substrate to the piezoresistors. The material has to exhibit high thermal stability, and resist cracking.
- Sensing layer: This refers to the piezoresistors, or gage resistors. Their function is to transform mechanical stress into electrical energy. They should exhibit low temperature dependance on their electrical properties, high resistivity, and a strong correlation between the applied strain and resistance. More details of their properties as sensing layers are described in the next section.
- Passivation Layer: This layer protects the gage resistors from environmental exposure. the passivation layer should have high resistance to moisture and ion penetration, high insulation properties, and high thermal stability.

Steel-Substrate Piezoresistive Sensor

Figure 2.4 shows a cross section of the functional layers of a steel-substrate piezoresistive sensor. Stainless steel is used as a substrate material because of its high strength, its temperature stability, and its high corrosion stability. Because of these substrate properties, the steel pressure sensors are used for high pressure applications. The isolation layer is often made from SiO_2 or Al_2O_3, because of their good dielectric properties. SiO_2 is preferred

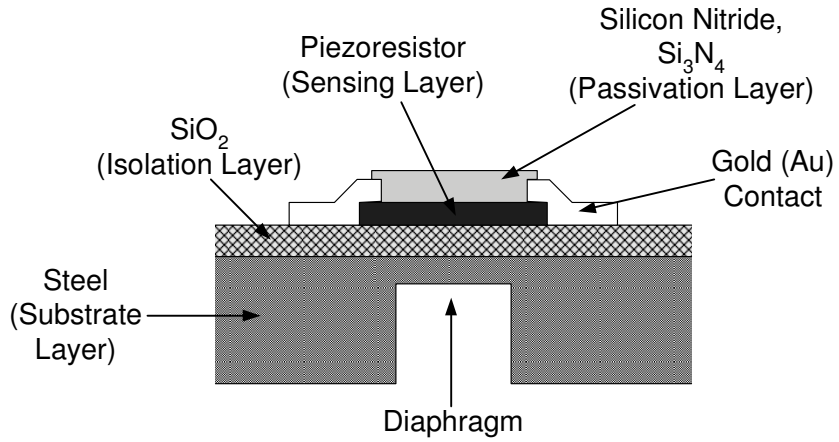


Figure 2.4: Cross section of a steel-substrate piezoresistive pressure sensor

because its insulating properties are superior to that of Al_2O_3. The sensing layer is often chosen to be p-doped polysilicon, because it has a high correlation (sensitivity) between stress and resistance. Moreover, because of its high resistivity, it can be fabricated into a small size. *NiCr* can also be used as a sensing layer for applications where lower temperature dependance, and high thermal stability is needed. The drawback of *NiCr* is that it has a much lower correlation between stress and resistance than polysilicon. Table 2.3 shows the trade-offs between *NiCr* and polysilicon, hence, the choice of sensing layer is dependant upon the target application.

The passivation layer is usually made out of Si_3N_4, because of its superior resistance to humidity, and high adhesion. Finally, the metal contacts on the resistors are usually made out of gold, because it is most stable against corrosion [6].

Table 2.3: Trade-offs between *NiCr* and Polysilicon as a sensing layer (*: very good, 0: sufficient)

Criteria	*NiCr*	***Polysilicon***
Gage Factor	0	*
Temperature dependance	*	0
Resistivity	0	*
Stability	*	0
Reproducibility	*	0

Silicon Piezoresistive Sensor

Silicon based sensors have become increasingly popular over the last decade, because of their low cost, potential for high production volume, and integration with silicon microelectronics. The silicon piezoresistive pressure sensor is no exception. Figure 2.5 shows a cross sectional view of a silicon piezoresistive sensor [7]. The diaphragm, which bends under stress and converts pressure into strain on the resistors, is etched out of the silicon substrate. The isolation layer is made out of Epipoly, a special type of polysilicon used for sensor applications. Details of epipoly fabrication is described in [6]. The advantage of epipoly as an isolation layer is that it is very stable over process parameters. The piezoresistors are made out of p-doped polysilicon, and the passivation layer is made out of SiO_2. When the sensor is packaged, difference in thermal expansion properties between the sensor and the package can affect the sensor characteristics. The glass base is used to lessen that effect.

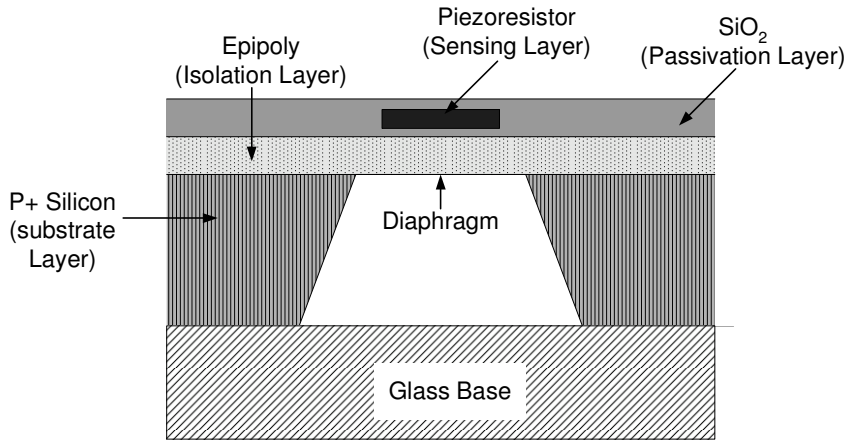


Figure 2.5: Cross section of a Silicon piezoresistive pressure sensor

2.1.4 Gage Factor and The Piezoresistive Coefficient

The Gage Factor is an important parameter which helps characterize the gage resistors. It describes the sensitivity of the resistors to the mechanical strain applied. The relationship between the fractional change of resistance ($\Delta R/R$) , and the mechanical strain (σ) is given

by:

$$\frac{\Delta R}{R} = K_{GF} \cdot \sigma \tag{2.1}$$

Where K_{GF} is the gage factor [6]. To illustrate the relationship between the gage factor and physical contributions, we start with the expression of defining the resistance R as:

$$R = \rho \frac{l}{A} \tag{2.2}$$

Where ρ is the resistivity, l is the length of the resistor, and A is the cross sectional area. When a mechanical strain is applied, the fractional change in resistance can be expressed to a first order approximation by:

$$\frac{\Delta R}{R} = \frac{\Delta \rho}{\rho} + \frac{\Delta l}{l} - \frac{\Delta A}{A} \tag{2.3}$$

Given that:

$$\frac{\Delta l}{l} = \sigma \tag{2.4}$$

and:

$$\frac{\Delta A}{A} = -2\nu \frac{\Delta l}{l} \tag{2.5}$$

Where ν is the Poisson ratio, the relative resistance variation is given by:

$$\frac{\Delta R}{R} = \left(1 + 2\nu + \frac{\Delta \rho}{\rho \cdot \sigma}\right) \cdot \sigma \tag{2.6}$$

Which shows how the relative resistance change due to physical contributions. By equating 2.1 and 2.6, we get:

$$K_{GF} = 1 + 2\nu + \frac{\Delta \rho}{\rho \cdot \sigma} \tag{2.7}$$

The first two terms of this equation represent the geometrical contributions to the gage factor, and the last term represents the change in resistivity [6]. The property by which a material changes its resistivity due to mechanical strain is called the piezoresistive effect [8]. The last term in this equation is called the piezoresistive coefficient, and is represented as:

$$\pi_{44} = \frac{\Delta \rho}{\rho \cdot \sigma} \tag{2.8}$$

For silicon based gage resistors, the geometrical contribution of the gage factor is negligible, and the piezoresistive coefficient term (π_{44}) dominates. The coefficient is also dependant on the doping qualities of the semiconductor material.

2.1.5 Wheatstone Bridge

In order to detect the changes in resistance of the gage resistors, four piezoresistors are arranged in a wheatstone bridge structure, as shown in Figure 2.6. Although currently used for pressure sensor applications, the wheatstone bridge configuration (originally called a "differential resistance measurer") was invented by Samuel Hunter Christie in 1833, although it was named after Charles Wheatstone, who elaborated more on the concept in 1843 [9]. The output resistance of wheatstone bridge automotive pressure sensors are typ-

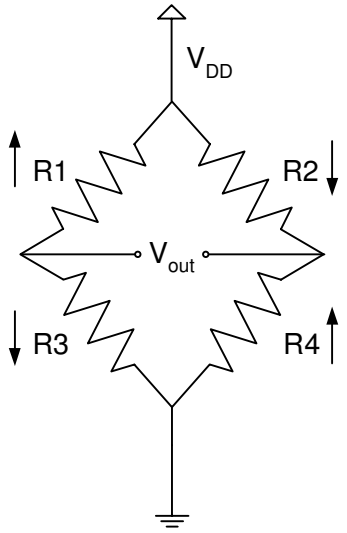


Figure 2.6: A Wheatstone Bridge

ically on the order of kilo ohms. To maximize the output voltage the resistors have to experience changes in resistance that differ in sign. Refer to Figure 2.7, which shows the top view of the gage resistor arrangement on the diaphragm, as well as the stress plot along the diaphragm. From this stress plot, we see that the resistors in the middle of the diaphragm experience negative stress, whereas those on the edges of the diaphragm experience positive stress [5]. Since the resistance of the gage resistors is directly proportional to the

mechanical strain, when pressure is applied on the gage resistors, the resistance of R_1 and R_4 increase, and the resistance of R_2 and R_3 decrease. The output voltage of Wheatstone bridge resistors is given by:

$$V_{out} = \frac{1}{4}\left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2} + \frac{\Delta R_3}{R_3} - \frac{\Delta R_4}{R_4}\right) \cdot V_{DD} \tag{2.9}$$

Where $\Delta R_i/R_i$ is given by equation 2.6.

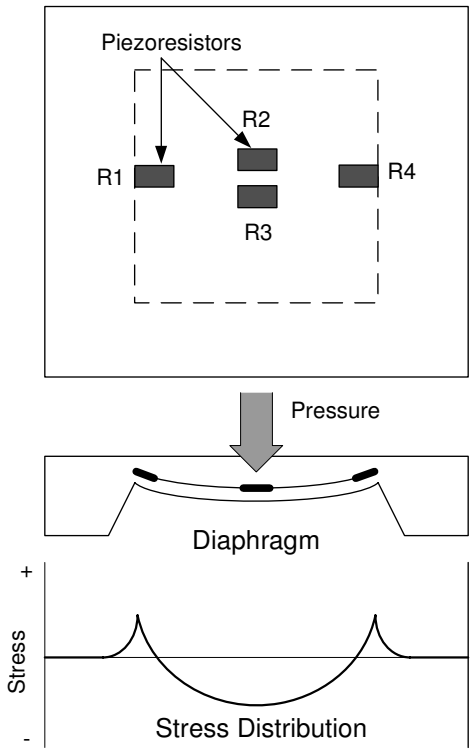


Figure 2.7: *(top)* Top view of piezoresistive sensor, *(middle)* cross sectional view, and *(bottom)* stress plot along the diaphragm length

2.2 Dynamic Offset and $1/F$ Noise Cancellation Techniques

In pressure sensor applications, the performance of the system is limited by offset and $1/F$ noise. That is because the sensor output are low frequency, low amplitude signals

($40mV_{pp} - 400mV_{pp}, 0.5Hz - 0.5kHz$), hence any low frequency noise or phenomenon above the thermal noise floor need to be eliminated or mitigated. In this section we discuss the sources of offset and $1/F$ noise, and the two most common methods of canceling them: auto-zeroing, and chopping.

2.2.1 Sources of Offset and $1/F$ Noise

In an ideal amplifier, when a zero input is applied, the expected output is also zero. However, that never happens in real life. Offset is defined as the amount of input voltage or current that needs to be applied at the input in order to get a zero output. It is also referred to as input-referred offset. No matter how well matched the design and layout of any amplifier is, due to non-idealities in the fabrication process, there will always be mismatches. V_t mismatches (transistor threshold voltage mismatch) dominates the mismatch of transistors that operate in the active region, whereas β mismatches (mismatches in the W/L) dominates in transistors that operate in the triode region, such as pass transistors, or switches. In the frequency domain, the offset appears as a component at DC.

$1/F$ noise occurs in semiconductors when carriers that would normally constitute a DC current in active devices are held for a while before being released [10]. PMOS carriers (holes) are much larger than NMOS carriers (electrons), thus are less likely to be trapped and released, giving PMOS transistors better $1/F$ noise performance than NMOS transistors. In the frequency domain, $1/F$ noise appears as a component at DC that rolls off at a $-10dB/dec$.

Figure 2.8 shows a frequency domain plot of the offset and $1/F$ noise relative to the thermal noise floor. The intersection between the $1/F$ and the thermal noise floor is called the $1/F$ corner frequency. in a MOS transistor, $1/F$ noise is modelled by a voltage source at the input with the value

$$V_n^2 = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \tag{2.10}$$

In a differential pair such as the one in figure 2.9, the input referred $1/F$ noise component is double that of a single transistor. The current sources, active loads, and cascode transistors in an Opamp also contribute to the noise, however, the input differential pair has the largest contribution [11].

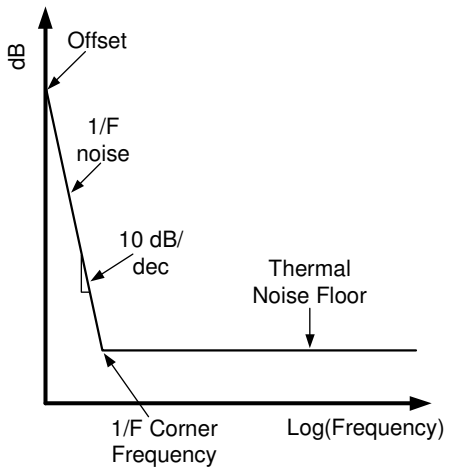


Figure 2.8: Typical Amplifier Noise spectrum

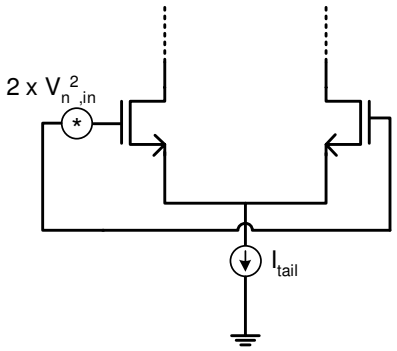


Figure 2.9: Input referred noise of a differential pair

2.2.2 Auto-zeroing

Operating Principle

Auto-zeroing is a switch capacitor method of cancelling offset. Its basic principle is that it applies a zero input to the amplifier, and measures its offset. Then, when the signal is amplified, subtracts the measured offset from the signal [12]. Figure 2.10 shows an example of a switch capacitor amplifier that utilizes auto-zeroing.

Clocks ϕ_1 and ϕ_2 are non-overlapping phases. Figure 2.11 shows the operating phases of the above amplifier.

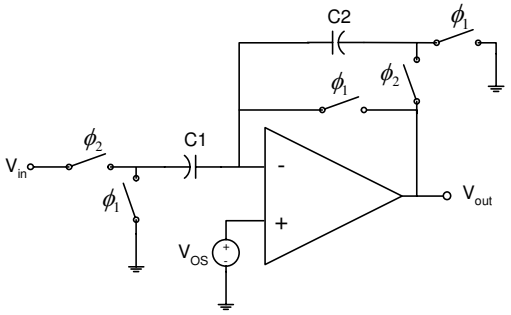


Figure 2.10: An auto-zeroing amplifier

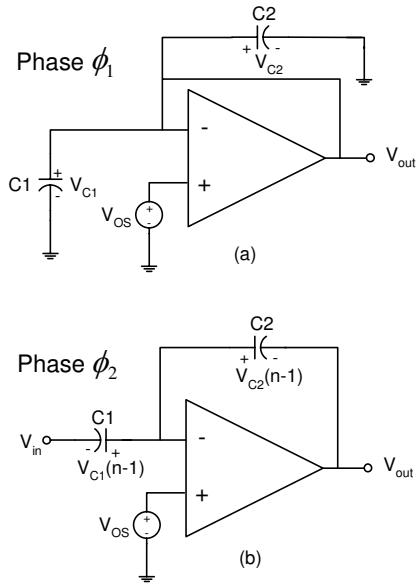


Figure 2.11: operation of auto-zeroing amplifier during *(a)* phase ϕ_1 and *(b)* phase ϕ_2

On phase ϕ_1, capacitors C_1 and C_2 sample and store the amplifier offset, V_{OS}. On phase ϕ_2, the offset voltage is subtracted from the input, and the offset-free signal is amplified, leaving the output of the amplifier at $V_{out} = V_{in} \cdot C_1/C_2$. From a signal processing perspective, auto-zeroing is equivalent to high-pass filtering the signal to get rid of offset and low frequency $1/F$ noise components.

Correlated Double Sampling (CDS)

Correlated Double Sampling (CDS) is another switched capacitor technique to eliminate offset and $1/F$ noise. Instead of sampling the offset and then cancelling it from the signal, CDS works by sampling the signal twice, and then performing a linear combination of the two samples to eliminate the offset. Figure 2.12 shows an example of a switched capacitor

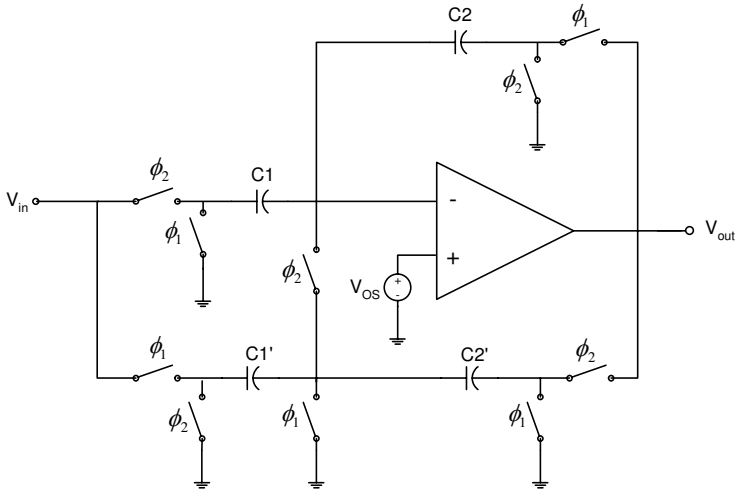


Figure 2.12: A switch-cap amplifier using CDS

gain amplifier that utilizes CDS. On phase ϕ_2, the input is sampled on capacitor $C1'$, and on phase ϕ_1, the input is sampled on $C1$, and the difference of the two input signals is amplified by $C2$ and $C2'$ and appears at the output. The output of the CDS amplifier on phase ϕ_2 is $V_{out} = (V_{in2} - V_{in1})C_1/C_2$, where V_{in1} and V_{in2} are the input voltage at the end of phase ϕ_1 and ϕ_2 respectively. Because the inputs are sampled with the offset in both phases, when the difference is taken, the effect of the offset is not seen at the output.

CDS amplifiers are useful in applications where only the time difference of two signals are needed, such as image sensors. We will not go into details of the CDS technique, since it is not as applicable for pressure sensors.

Design Considerations

There are some design considerations that have to be kept in mind when designing auto-zeroing switched capacitor amplifiers. One of them is charge injection, which is a common

problem for any switched capacitor circuit, and can be a source of distortion. Charge injection occurs during the falling edge of a clock, and is given by $Q_{ch} = WLC_{ox}(V_{GS} - V_t)$, and $V_{ch} = Q_{ch}/C_{in}$. Switches must be made small, and input capacitors made large in order to minimize their effect. However, that may cause settling issues due to a large switch on-resistance (r_{ON}), and a large C_{in}. For optimal noise and power performance, the capacitance C is sized according to KT/C noise calculations. The switch is then sized to optimize the time constant $r_{ON}C_{in}$, and the charge injection, based on simulation. There are other circuit techniques that can minimize their effects, which can be referred to in [10].

A consequence of auto-zeroing is that the in-band residual noise for auto-zeroed amplifiers is larger than the thermal noise floor. That is because all the out-of-band noise is aliased back in-band, as with all sampled systems. The in-band thermal noise due to auto-zeroing is given by

$$V_{n,az} = V_n\sqrt{2B/F_s} \tag{2.11}$$

Where V_n is the thermal noise power, B is the noise bandwidth, and F_s is the clock frequency. Intuitively, the equation can be understood as calculating the out-of-band noise that folds back in-band due to the switched capacitor sampling. An in-depth analysis of the in-band noise level is given in [12]. Figure 2.13 shows an illustration of the noise spectra before and after auto-zeroing. This applies to all switched capacitor circuits, hence, the auto-zeroing amplifier is ideal for sampled-data systems, where the inherent base-band behavior is not made worse by auto-zeroing.

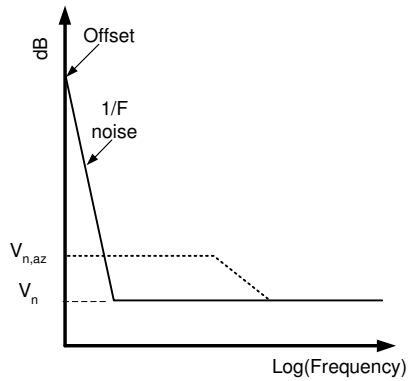


Figure 2.13: Noise spectrum of auto-zeroed switch capacitor amplifier

2.2.3 Chopping

Operating Principle

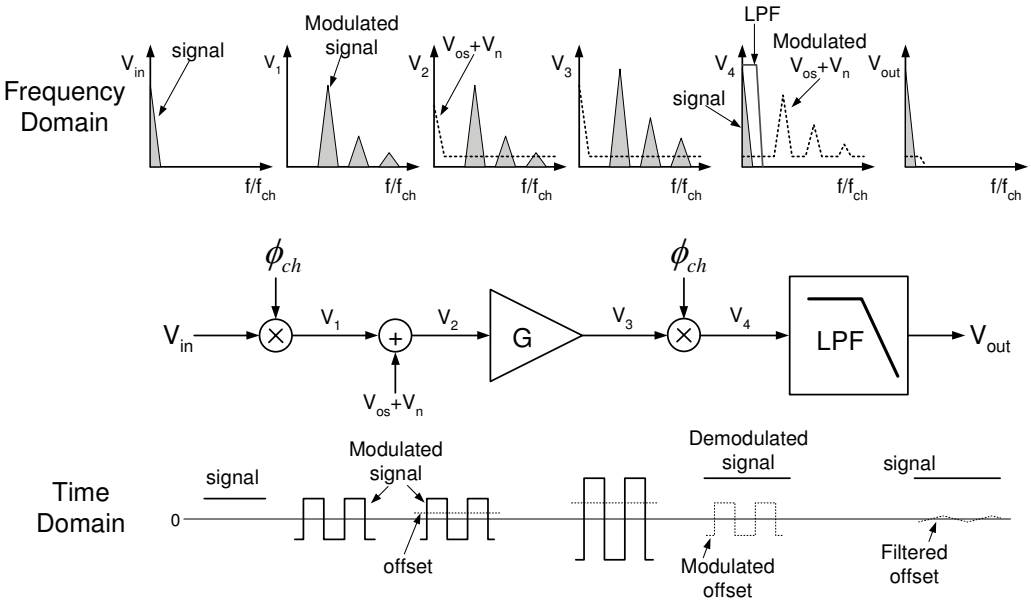


Figure 2.14: System diagram of the chopping principle with time and frequency domain plots

Chopping is a continuous-time technique that uses modulation to get rid of offset and $1/F$ noise, as shown in figure 2.14. Using this technique, the input signal is square-wave modulated to a higher frequency, f_{ch} before is reaches the amplifier-with-offset. Both the signal and offset are amplified, after which the signal is demodulated back to baseband, whereas the offset and $1/f$ noise are modulated to f_{ch}. A low pass filter following the output chopper filters out the modulated offset and $1/F$ noise [12].

The choppers can be easily implemented in CMOS technology using a four switches in a polarity reversing topology, as in figure 2.15. A condition for the chopping technique to completely eliminate the $1/F$ noise, is that the chopping frequency, f_{ch}, must be greater than the $1/F$ corner frequency (F_c).

The advantages of chopping over auto-zeroing is that the in-band noise is equal to the thermal noise level in chopping, whereas it is always higher in auto-zeroing. Both methods

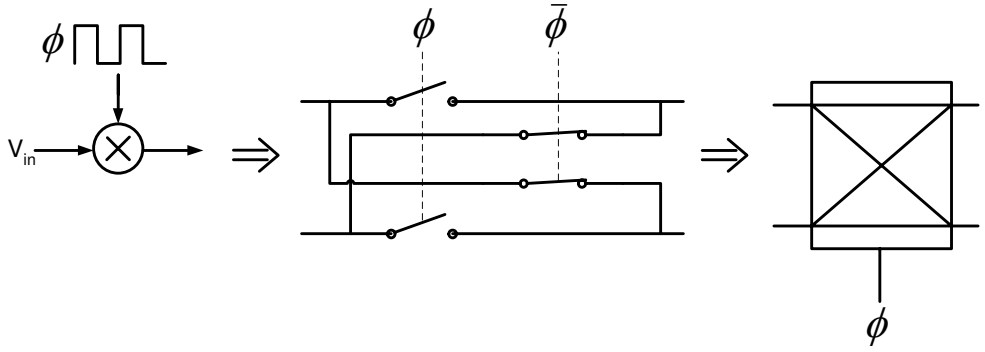


Figure 2.15: Implementation of the chopper

suffer from the problem of switch sizing that can handle the necessary signal swing, and at the same time minimize the charge injection. The disadvantage of the chopping technique is that chopping reduces the effective gain of the amplifier, and hence increases the gain errors [13]. The amplifier bandwidth (BW) must be designed much larger than the chopping frequency to reduce the gain errors. The effective gain of the chopper amplifier is given by:

$$A_{eff} = A\left(1 - \frac{4\tau}{T_{ch}}\right) \tag{2.12}$$

Where $\tau = 1/(2\pi \cdot BW)$, A is the open loop gain of the amplifier before chopping, and T_{ch} is the chopping period [13]. If the amplifier BW is designed 6 times the chopping frequency, then the effective gain, A_{eff}, is approximately 10% lower than the open loop gain, A, of the non-chopped amplifier. This happens because the glitches that occur due to chopping reduces the output signal's amplitude, and hence reduces the DC gain. How fast the opamp can recover from the glitches will affect how much the amplitude changes, and hence affect the effective gain.

One way to get around this problem is to perform the chopping operation within the feedback of the amplifier. Figure 2.16 shows an example of an amplifier in feedback, where the chopping is done within the feedback resistors. In this case, the overall amplifier gain is less sensitive to the open loop gain of the Opamp, and hence reducing gain errors [13]. Moreover, the input choppers only see the virtual ground of the amplifier, which has a signal amplitude of V_{out}/A. Since this signal is much smaller than the input signal, the input chopper switches can be made much smaller than in the previous case where the

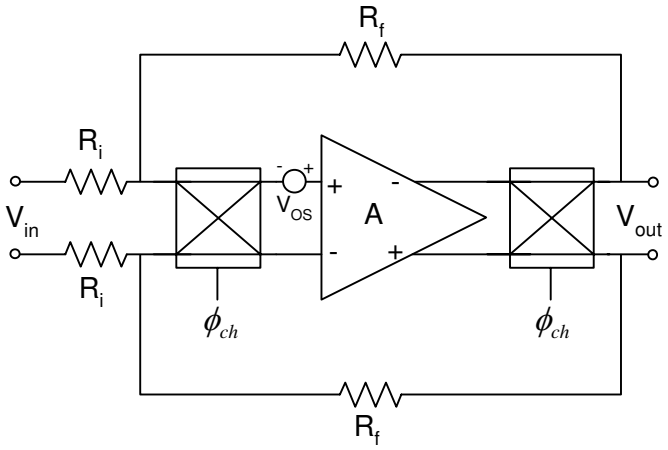


Figure 2.16: A chopper amplifier with feedback

input choppers had to tolerate the entire input signal swing. This significantly reduces the charge injection errors due to the input switches. The output switches still have to be made large in order to tolerate the full output signal swing, however, their effect is reduced when referred to the input, and hence do not significantly affect the performance. In the case where a two stage Opamp is used, a common technique is to include the demodulation chopper at the output of the first stage [14]. An example of that is shown in figure 2.17.

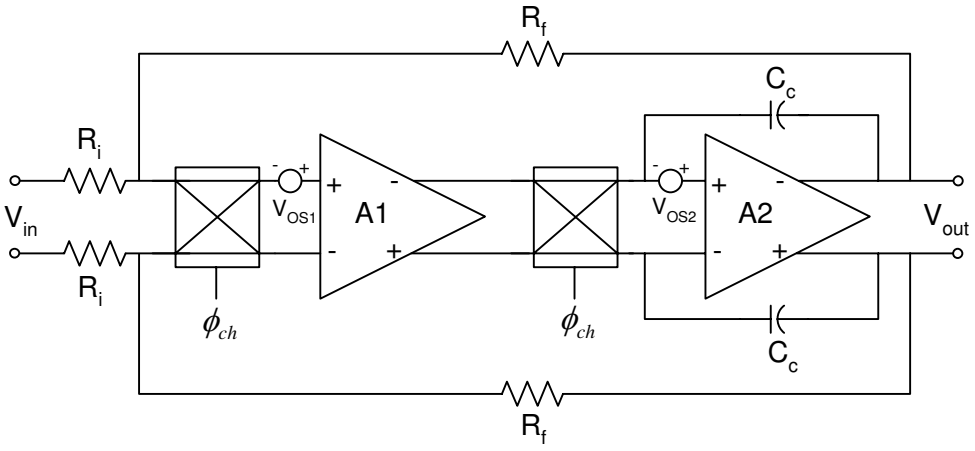


Figure 2.17: A two-stage chopper amplifier

Once again, the switch sizes of the second stage can be reduced, since the signal swing

at the input of the second stage is V_{out}/A_2. Moreover, this method is more power efficient than chopping across the entire two stages, since it is takes less power to make the bandwidth of the first amplifier much larger than f_{ch}, than it is to make the two-stage amplifier bandwidth as large. In other words, this method allows chopping at higher frequencies if necessary for the same power consumption [15]. Furthermore, due to the compensation capacitor, the second stage acts as a low-pass filter to get rid of the chopping artifacts, and hence greatly reduces the requirements of the external low-pass filter if required. The disadvantage of this method, is that the offset and $1/F$ noise of the second stage is not canceled, hence A_1 has to be made large in order to reduce its effects when referred to the input.

Chopping in the Digital Domain

In the beginning of this section, we showed a system diagram of the sensor-interface-ADC system, in figure 2.1. In this section, we show how we can incorporate chopping into the system in an efficient way. In the introduction to chopping, we showed that a LPF was needed in order to filter out the modulated $1/F$ noise and offset (figure 2.14). One of the challenges of that system, is that it is difficult to design an analog LPF with a low cut-off frequency, and sharp roll-off. However, this can be done easily with a digital filter. Figure 2.18 shows a the pressure sensor system with chopping, where the demodulation and filtering are done in the digital domain [16].

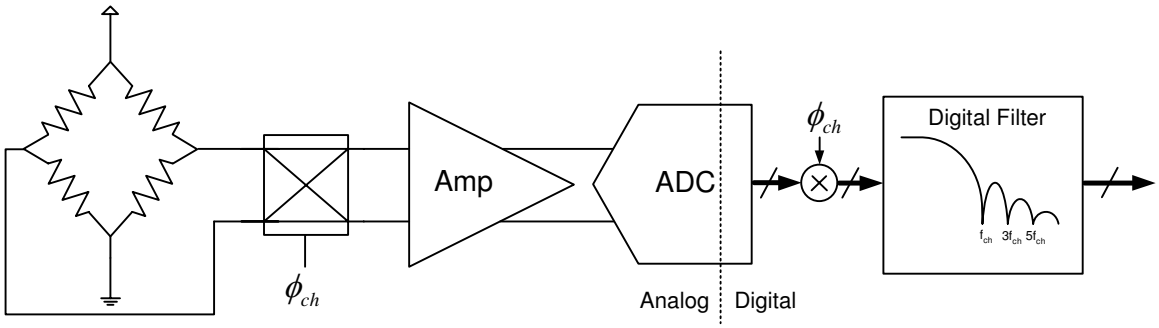


Figure 2.18: Sensor system with demodulation in the digital domain

Other advantages of doing the filtering in the digital domain, is that the digital filter

can be implemented with much less power consumption than an analog filter. Moreover, the filter can be designed with notches at odd harmonics of f_{ch}, which will completely eliminate the chopping artifacts. Moreover, if an oversampling converter is used as the ADC, then the digital filter and the decimation filter can be integrated, so there is no extra power consumption due to filtering. Demodulating in the digital domain eliminates the need for big switches in the signal path which degrades the signal quality due to distortion from charge injection.

Design Considerations

In addition to charge injection and chopper switch sizing, one of the major design considerations when designing a chopper amplifier is the chopper frequency. While it may be desirable to chop at higher frequencies to reduce the requirements of the LPF, there is an inverse relationship between the chopping frequency, and the residual offset due to chopping. The residual offset occurs due to the spikes that occur during switching, as shown in figure2.19.

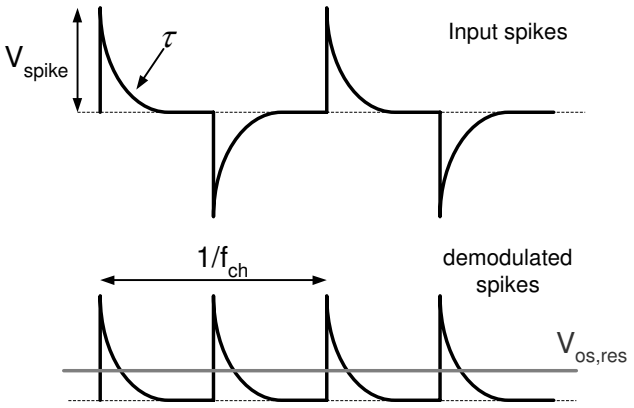


Figure 2.19: Chopping switching spikes

The relationship between the chopping frequency and the residual offset is:

$$V_{os,res} = 2 f_{ch} V_{spike} \tau \tag{2.13}$$

where τ is related to the bandwidth of the amplifier [12]. Other sources of residual offset

is non-symmetrical layout. The choppers must be laid-out as symmetrically as possible to ensure that the chopped signals see the same impedance, and clock coupling.

In conclusion, chopping is the dynamic offset cancellation technique of choice in continuous time, low bandwidth applications. There are several other amplifier topologies that utilize chopping that can be referred to in [17] [18] [19] [20] [21]. The above topologies are meant to introduce the concept of chopping as an offset cancellation technique, as well as explore some of the issues that need to be considered when designing a chopping amplifier.

2.3 High Accuracy ADC Architectures

In this section, we will provide an overview of high accuracy ADC architectures that can be used for power scalable pressure sensor applications. This section is not meant to provide an explanation of how the ADC's work. Instead, this section will explore different ADC architectures from the perspective of how applicable they are for high accuracy, power scalable applications. The main criteria for evaluation of the ADC's are:

- Accuracy
- Size
- Power Scalability, or ability to periodically power-down

2.3.1 Flash ADC

The flash ADC is one of the simplest ADC's that can be designed, since it behaves like a ruler. The accuracy of the ADC is defined by the number of comparators or "ruler divisions" is needed. For the case of the pressor sensor, in order to measure accurately to 14 bits, a total of $2^{14} - 1 = 16383$ comparators is required! This makes the flash ADC impractical to implement, since the number of comparators would make the total ADC size too large and too power hungry.

2.3.2 Pipeline ADC

The pipeline ADC is one of the most popular Nyquist ADC's used nowadays for high-speed, medium accuracy applications. Its design allows for a smaller number of comparators by doing the conversion over several "pipelined" stages. Achieving 14 bit accuracy

in a pipelined ADC is difficult, but not impossible. The pipeline design is also very compatible with power scalability requirements [35]. The reason why the pipeline ADC is not commonly used in high accuracy sensor applications, is because of the large input capacitor sizes needed for small signal swings to bring the thermal noise floor to the 14 bit level. Moreover, there achieving 14 bits resolution requires more MDAC stages, and hence more power consumption. Assuming that the input signal of the ADC is $400mV_{pp}$ differential, which corresponds to an average power $P_{ave} = 5mW^2$ (referenced to 1Ω), and that the required thermal noise floor is 14 bits ($SNR = 86dB$), then, the noise power required is

$$V_n = \sqrt{\frac{P_{ave}}{10^{SNR/10}}} \Rightarrow V_n = \sqrt{\frac{5 \times 10^{-3}}{10^{86/10}}} = 3.5\mu V_{rms} \tag{2.14}$$

Given that the thermal noise of the pipeline is dominated by the first stage sample-and-hold, which has a noise power of

$$V_n^2 = \frac{2KT}{C} \tag{2.15}$$

Assuming room temperature conditions ($T = 300K$), then the required input capacitance is

$$C_{in} = \frac{2KT}{V_n^2} = 0.67nF! \tag{2.16}$$

This is a very impractical capacitance to use on a modern integrated chip. Assuming that the a MIM capacitor is used, and that the average capacitance per unit area is $1fF/\mu m^2$, then the total area for just the input capacitance is $0.67mm^2$!.

2.3.3 Dual-Slope (Integrating) ADC

Dual Slope (or Integrating) ADCs are very popular high accuracy, low offset converters that can be used with very slow signals [10]. The principle behind this topology is that for a fixed number of clock period, the converter integrates the input signal, and then the reference voltage is subtracted from it until the output reaches zero. For an $N-bit$ ADC, 2^N clock cycles are required for one conversion. Hence for a $14-bit$ ADC, at least $16,384$ cycles are needed! This means that higher clock frequencies will be utilized to reduce the overall conversion time, or, a sample-and-hold will need to be used to hold the signal voltage for a longer time period, which increases the overall power consumption. Moreover,

this topology works well in power scalable applications, because the integrator is reset after each conversion cycle.

2.3.4 $\Delta - \Sigma$ ADC

The $\Delta\Sigma$ ADC is the most popular converter in high accuracy sensor applications. Their accuracy performance is attributed to the noise shaping quality of the oversampling converter [22]. Although they do not operate as fast as pipeline or flash ADC's, their operating speeds are more than enough for low frequency pressure sensor applications. The main advantage of the $\Delta\Sigma$ architecture, or any oversampling ADC in general, is that the input capacitor size is reduced by the oversampling ratio. Using the same example as the pipeline case above, and assuming that an oversampling ratio (*OSR*) of 1000 was used, then the input capacitor of the modulator is:

$$C_{in} = \frac{2KT}{V_n^2}/OSR = 0.67pF \tag{2.17}$$

This is a more favorable capacitor size to use on an integrated semiconductor chip. Although a pipelined ADC can also be oversampled to reduce the input capacitor size, there is still the problem of a large number of stages required to achieve 14 bits resolution. This increases the size of the overall ADC and its power consumption. Moreover, a larger number of stages means that more noise is generated when referred to the input, which means that the input capacitor has to be increased further. Because the $\Delta\Sigma$ ADC can achieve higher accuracy with a fewer number of stages, most people prefer oversampling ADC's. The disadvantage of the $\Delta\Sigma$ ADC is that the loop filter must always be integrating, and hence cannot be powered down periodically, unless certain modifications are made to the architecture. This brings us to the incremental ADC.

2.3.5 Incremental ADC

An incremental ADC has been proposed several years ago as a hybrid between the $\Delta\Sigma$ and Dual-Slope ADC architectures [23]. It is often modeled as a $\Delta\Sigma$ ADC with the integrators being reset after each conversion [24]. It is similar to the Dual-Slope ADC in that it has a fixed number of integration cycles per conversion. The OSR for the incremental ADC is defined as the number of cycles per conversion. The difference between the incremental

and the Dual-Slope ADCs is that the integration and reference subtraction are mixed in time [25]. Because of that, incremental ADCs are not limited to 1^{st} order architectures. In order to reduce the number of integration cycles, 2^{nd} order (and more) architectures can be used. Moreover, $\Delta\Sigma$ techniques, such as MASH architectures, using input feed-forward techniques, etc. can be used to improve distortion performance, and reduce conversion time even further. This means that high accuracy incremental ADCs can be used with low conversion time. Moreover, because the integrators can be reset, they can be powered down, making this topology compatible with power scalability options.

Because this topology combines the best of both $\Delta\Sigma$ and Dual-Slope ADCs, it is the best high accuracy ADC that can be used in low power, low speed sensor applications.

Chapter 3

The Sensor Interface System

IN this chapter, we will discuss in detail the power scalable sensor interface system that we will use for the automotive pressure sensor. As discussed in chapter 2, sensor output signals are usually amplified before analog to digital conversion is done. Due to the resource and time limitations, the entire sensor interface was not designed. Only the power scalable amplifier portion of it was designed and fabricated. We will discuss the different topologies that could be used for the amplifier, advantages and disadvantages of each, and reach an optimal solution for this application. We will show how these design choices helps us meet the specifications, in particular that of power scalability.

3.1 Programmable Gain Amplifier (PGA) and System Requirements

Figure 3.1 shows the system diagram of the sensor interface system that will be designed. As mentioned above, only the PGA will be designed for this thesis, as indicated in the dashed box. The PGA will make use of one of the dynamic offset cancelation techniques, chopping or auto-zeroing, depending on the PGA topology. In order to determine what the design specifications are for the PGA, it is worth reviewing the design specifications for the entire system, and from that determine the requirements for the PGA to meet the overall specifications.

As mentioned in chapter 1, it is desired to reduce their manufacturing costs by mass-producing a standard interface system that can be used for a number of their pressure sensor

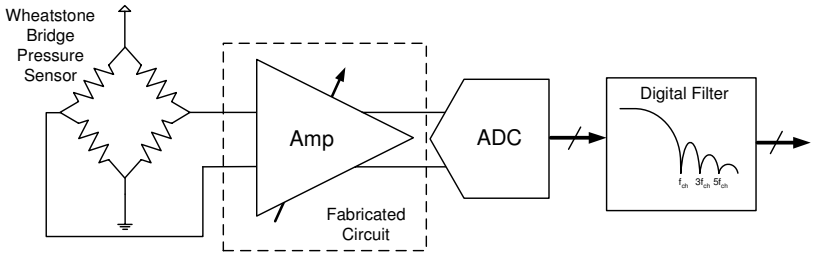


Figure 3.1: The Sensor Interface System of Choice

applications (mainly automotive). The interface must be optimal for any of the target applications, in terms of power and noise/distortion performance. An intuitive look at the application range shows us that, when the application changes so that the output amplitude goes from $40mV_{pp}$ to $400mV_{pp}$, the input capacitor size of a SC PGA will reduce by 100 $\times$, hence the power of the opamp driving it should also reduce by the same factor. Moreover, when the sensor output bandwidth decreases by $1000\times$, the PGA bandwidth must also decrease by the same factor, and thus, the power. Therefore, the interface must:

- Be optimally designed for signals whose amplitude ranges from $40mV_{pp}$ to $400mV_{pp}$ differential
- Be optimally designed for signals whose frequency ranges from $0.5Hz$ to $0.5kHz$
- Be quadratically power scalable across the signal amplitude range
- Be linearly power scalable across the signal frequency range
- Be 14-bit accurate (noise and distortion)
- Consume $5\mu A$ of average current for the $40mV_{pp}$, $0.5Hz$ test case

The methodology of the proposed system, shown in figure 3.1, is that the ADC will be designed as a low power stand-alone ADC, which is able to handle input signal amplitudes of $400mV_{pp}$ and above. The function of the PGA would then amplify the sensor output signal to at least $400mV_{pp}$. Using this method, we spare the ADC from having to deal with low voltages, which relaxes the requirements on the input capacitor sizes. Based on the previous chapter, the incremental ADC is the best choice for this application, because it makes use of the advantages of the $\Delta - \Sigma$ ADC's in its high-accuracy performance, and has a limited number of conversion cycles per output, making it compatible with power scalability. This will be discussed in more detail in the rest of the chapter. Before we describe in detail the different PGA topologies, it is worth describing the Incremental ADC

topology that would be used, as this will help determine the target specifications of the PGA.

3.1.1 Incremental ADC topology

Figure 3.2 below shows the block diagram of a second order incremental ADC with input feed-forward. As mentioned in the previous chapter, the incremental ADC is modeled as a $\Delta - \Sigma$ ADC with integrators that reset after each conversion cycle [25].

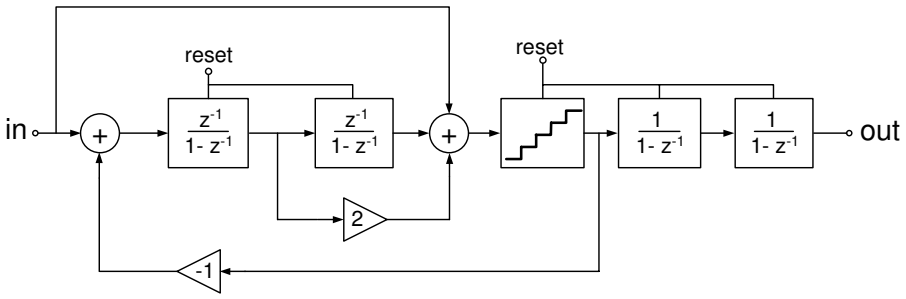


Figure 3.2: 2^{nd}-Order Incremental ADC Model with Input Feed-Forward

MATLAB simulations were used to figure out the minimum oversampling ratio that should be used. figure 3.3 below shows a plot of SQNR Vs OSR for the second order incremental ADC shown above. The input of the ADC was a $400mV_{pp}$ signal.

The figure shows that in order to attain 14 bits SQNR, an OSR of at least 250 is required. Given that the sensor output frequency is a maximum of $0.5kHz$, this means that a sampling frequency of at least $2 \times 0.5kHz \times 250 = 250kHz$ is needed for a $14-bit$ incremental ADC.

3.2 Variable Input and Feedback PGA

Several PGA topologies have been suggested in the literature. We will not discuss all the different architectures, but will go through an overview of some of the most significant ones. Using those architectures as a starting ground, and through discussing the advantages and disadvantages of each, we will eventually develop a solution that is optimal for our design application.

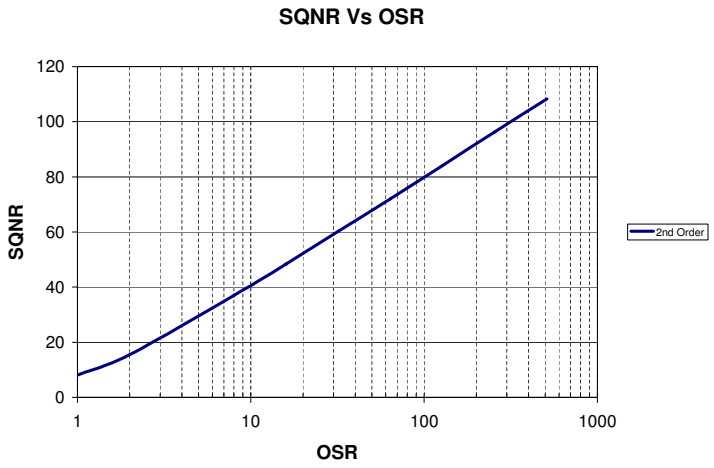


Figure 3.3: SQNR Vs OSR for the 2^{nd}-Order Incremental ADC Model with Input Feed-Forward

3.2.1 Variable Feedback PGA

Figure 3.4 shows a block diagram of a programmable gain inverting amplifier topology with variable feedback impedance [26] [27]. We are assuming that all the designs are fully differential, although we are representing the single-ended versions for illustration. Moreover, we are assuming that all amplifiers employ some method of dynamic offset cancelation technique, whether chopping for continuous time amplifiers, or auto-zeroing for switched capacitor amplifiers.

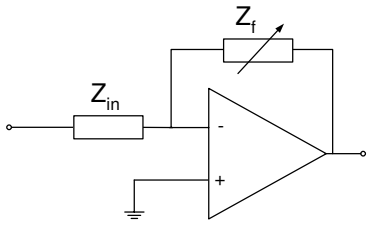


Figure 3.4: Programmable Gain Amplifier (Single ended representation) with Variable Feedback Impedance

The variable feedback is implemented by switching in a different series or parallel combination of resistors or capacitors. The advantage of the above topology is that since the input impedance is constant, there are no switches at the input of the system. Input

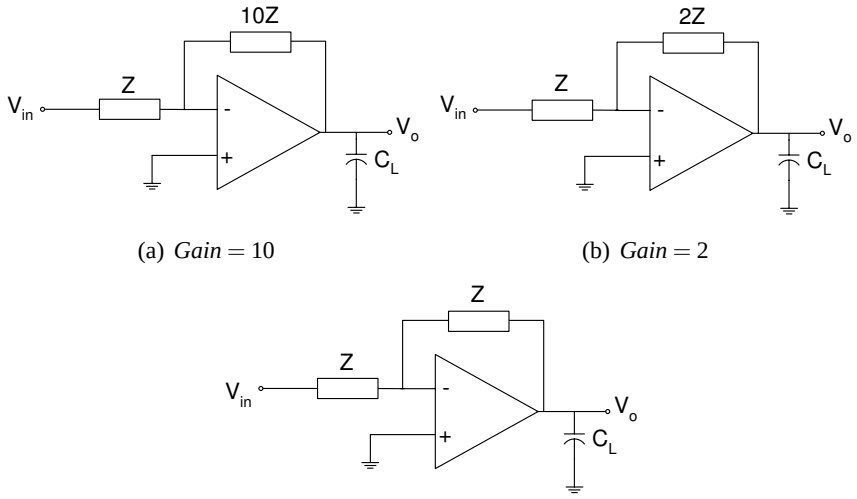
switches are usually a bottle-neck in any switched design because the switch resistance varies as a function of input. This results in either a gain error, or distortion. Because these switches are in the feedback network, the effect of variable switch resistance is reduced by the gain of the amplifier.

The major disadvantage of this topology is that because the input impedance is constant, it is not always optimized for noise. Assuming a switched capacitor amplifier was used, the input referred noise power would be related to KT/C. In a variable feedback PGA topology, that means that the input capacitor has to be sized for the worst case ($40mV_{pp}$) to achieve a 14 bit thermal noise level. That means that it would be $100\times$ oversized for the $400mV_{pp}$ case! The same argument applies in the continuous time amplifier case where the noise power is a function of $4KTR \times NoiseBandwidth$. In this case, the input resistor will be designed for the worst case, which would be $100\times$ undersized for the $400mV_{pp}$ case. This inherently makes variable feedback topologies very power inefficient.

Another disadvantage with this topology, is that the power cannot be scaled linearly with input amplitude to achieve the same opamp bandwidth. To illustrate this further, let us consider the closed loop $3dB$ bandwidth of the opamp:

$$f_{3dB} = \frac{g_m}{C} \cdot \beta$$
$$f_{3dB} = \frac{g_m}{C_L + C_f//C_{in}} \cdot \beta \tag{3.1}$$

where C_L is the input capacitance of the next stage, C_{in} and C_f are the input and feedback capacitances, and β is the beta factor of the gain stage, equal to $\beta = C_f/(C_f + C_{in})$. Let us refer to figure 3.5. Assume that the f_{3dB} is chosen to be $10\times$ the chopping frequency. Also, let us assume that either a single stage amplifier is chosen, or that a two-stage is chosen where the compensation capacitor (C_c) is a fixed fraction of the load capacitor (C_L). C_L is assumed to be the sampling capacitor of the incremental ADC.



(a) $Gain = 10$ (b) $Gain = 2$

(c) $Gain = 1$

Figure 3.5: Variable Feedback PGAs with different gain settings

The bandwidth of the three cases is

$$f_{3dB-Gain10} = \frac{g_{m1}}{C_L} \cdot \frac{1}{11}$$

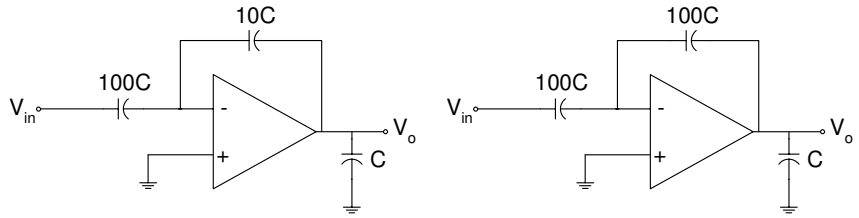
$$f_{3dB-Gain2} = \frac{g_{m2}}{C_L} \cdot \frac{1}{3} \tag{3.2}$$

$$f_{3dB-Gain1} = \frac{g_{m3}}{C_L} \cdot \frac{1}{2}$$

The above equations show that in order to maintain the same opamp bandwidth for all gain settings, $g_{m3} = g_{m1}/5.5$, and $g_{m3} = g_{m2}/1.5$. This shows that using this method, the power does not scale linearly with gain setting or amplitude. Ideally, as the input power increases by $100\times$ (from $40mV_{pp}$ to $400mV_{pp}$), so should the amplifier power consumption decrease by much.

The above equations assume that the load capacitor is dominated by C_L. This is true in a continuous time topology, but not true in a switch capacitor gain amplifier. Figure 3.6 a variable feedback switched capacitor (SC) PGA with gain setting of 10 and 1. in this

example, we are assuming that the capacitor "C" is adequately sized to achieve 14 bit noise floor at $400mV_{pp}$ input amplitude. Hence, for a $40mV_{pp}$ input amplitude, "$100C$" brings the noise floor to the same 14 bit level. Since the input to the ADC is $400mV_{pp}$, $C_{in,ADC} = C$



(a) $Input = 40mV$, $Gain = 10$ (b) $Input = 400mV$, $Gain = 1$

Figure 3.6: Variable Feedback SC PGA with different gain settings

The bandwidth of the these cases is

$$f_{3dB-Gain10} = \frac{g_{m1}}{10.1C} \cdot \frac{1}{11} = \frac{g_{m1}}{111.1C}$$
$$f_{3dB-Gain1} = \frac{g_{m2}}{51C} \cdot \frac{1}{2} = \frac{g_{m2}}{102C} \tag{3.3}$$

Equating the two bandwidths ($f_{3dB-Gain10} = f_{3dB-Gain1}$), means that $g_{m1} \approx g_{m2}$. This result is worse than the continuous time case shown in equation 3.2. This clearly shows that SC variable feedback PGAs are not suitable for power scalable applications.

3.2.2 Variable Input PGA

One way solve some of the challenges mentioned above is to make the feedback constant, and change the input impedance of the amplifier, as indicated in figure 3.7. in this case, the input is scaled by the gain requirement of the PGA [28] [29]. Because this method relies on switching different impedances at the input, we fall into the problem of gain errors and distortion due to signal dependant switch resistance. This can be overcome by making "impedance-select" switches large enough to reduce the switch resistance. Because these switches are not being continuously turned on and off, there is no problem of charge injection associated with large switches. Also, assuming a continuous-time amplifier is

used, the larger the input resistance, the less the effect the switch resistance will have on the gain accuracy.

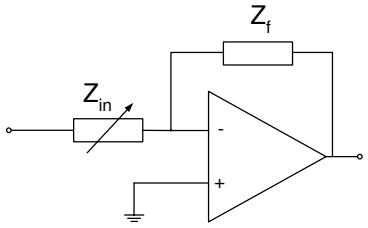
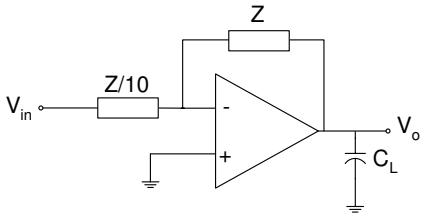
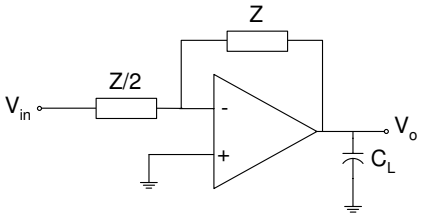


Figure 3.7: Programmable Gain Amplifier (Single ended representation) with Variable Input Impedance

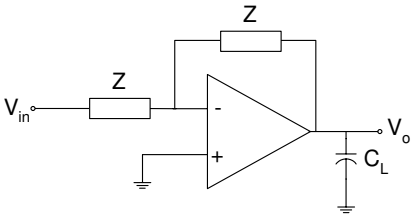
Although the above method scales the input impedances according to the gain, they are still not optimally sized for noise. Referring to figure 3.8, if we were to assume that the impedance was sized for optimal noise performance at $40mV_{pp}$, then in the $200mV_{pp}$ case, the impedance should increase by $(200/40)^2 = 25$ times, However, if only the input impedance changes, then it increases by only a factor of 5. Likewise for the $400mV_{pp}$ input case, the impedance increases by a factor of 10 as opposed to the factor of 100 needed.



(a) $Input = 40mV$, $Gain = 10$



(b) $Input = 200mV$, $Gain = 2$

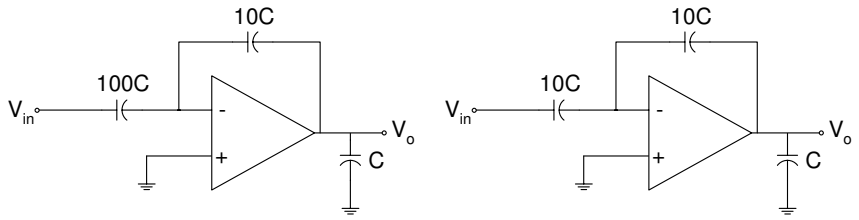


(c) $Input = 400mV$, $Gain = 1$

Figure 3.8: Variable Input PGAs with different gain settings

In terms of power scalability, the continuous time case will yield the same results as

equation 3.2. As for the SC case, figure 3.9 shows an example of two gain settings in the variable feedback case.



(a) $Input = 40mV$, $Gain = 10$ (b) $Input = 400mV$, $Gain = 1$

Figure 3.9: Variable Input SC PGA with different gain settings

In this case, the bandwidth is equal to

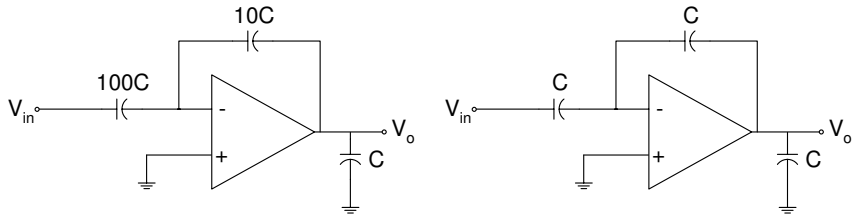
$$f_{3dB-Gain10} = \frac{g_{m1}}{10.1C} \cdot \frac{1}{11} = \frac{g_{m1}}{111.1C}$$
$$f_{3dB-Gain1} = \frac{g_{m2}}{6C} \cdot \frac{1}{2} = \frac{g_{m2}}{12C} \tag{3.4}$$

which means that in order to make $f_{3dB-Gain10} = f_{3dB-Gain1}$, $g_{m2} = g_{m1}/9.25$. Although this topology scales better than in the previous case, it still does not scale down by the same factor as the input power.

3.2.3 Variable Input and Feedback PGA

In order to overcome the problem of optimal impedance sizing in relation to the thermal noise, a proposed method would be to scale both the input and the feedback impedances [30] [31]. The input impedance is optimally sized according to the thermal noise requirements, and the feedback is sized according to the gain setting required to produce the $400mV_{pp}$ minimum output. Figure 3.10 shows the switched capacitor example of a Variable Input and Feedback PGA. In this case, the capacitor is optimally sized for thermal noise for both gain settings. This topology will result in both the input and feedback capacitors having “impedance select” switches. The effect of those switches is dominated by the input switches, which we have established in the previous section, is not a problem given proper

switch sizing, and thorough simulation.



(a) $Input = 40mV, Gain = 10$ (b) $Input = 400mV, Gain = 1$

Figure 3.10: Variable Input and Feedback SC PGA with different gain settings

Let us examine the power scalability of this method. The bandwidths of the two gain settings are:

$$f_{3dB-Gain10} = \frac{g_{m1}}{10.1C} \cdot \frac{1}{11} = \frac{g_{m1}}{111.1C}$$
$$f_{3dB-Gain1} = \frac{g_{m2}}{1.5C} \cdot \frac{1}{2} = \frac{g_{m2}}{3C} \tag{3.5}$$

which means that in order to make $f_{3dB-Gain10} = f_{3dB-Gain1}$, $g_{m2} = g_{m1}/37$. Again this is an improvement over the above two methods, although it still does not scale with the input power by the same proportion.

With the above analysis, it is worth looking at a different method of designing programmable gain amplifiers. Rather than switching in different opamps, and impedances, we will examine Cascaded Gain PGAs.

3.3 Cascade Gain PGA

In this section, we will discuss the Cascaded Gain PGA, and will compare it to the single stage, variable input and feedback topologies.

3.3.1 Cascaded Gain Amplifier with Output Gain Select

Figure 3.11 shows a block diagram of a cascaded gain amplifier with an output gain select mux [32] [33]. This means that the gain is set by selecting which amplifier ***output*** passes through to the ADC.

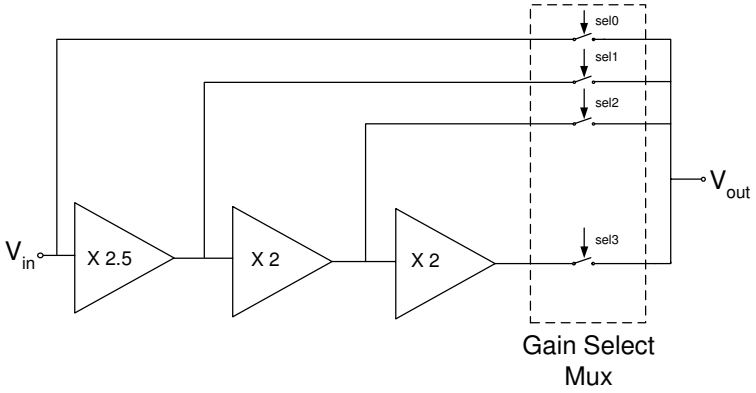


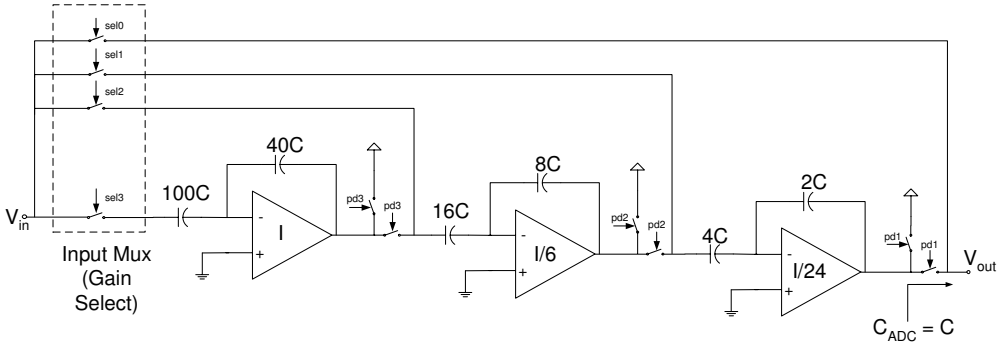
Figure 3.11: Cascaded Gain stage with output gain select mux

Although this is the most commonly used cascaded gain amplifier, it has many disadvantages which are similar to the variable feedback amplifier. Because all signals must pass through the first amplifier (with the exception of "Gain 1" setting which bypasses all gain stages), the input impedance is not optimally sized for thermal noise. Moreover, the first stage opamp must be sized for the worst case, and hence is larger than the others to drive the next stage's large capacitance, or resistance . This means that this topology does not power scale well, since all signals must be amplified by the first, power hungry, amplifier. This makes this topology very unsuitable for sensor applications.

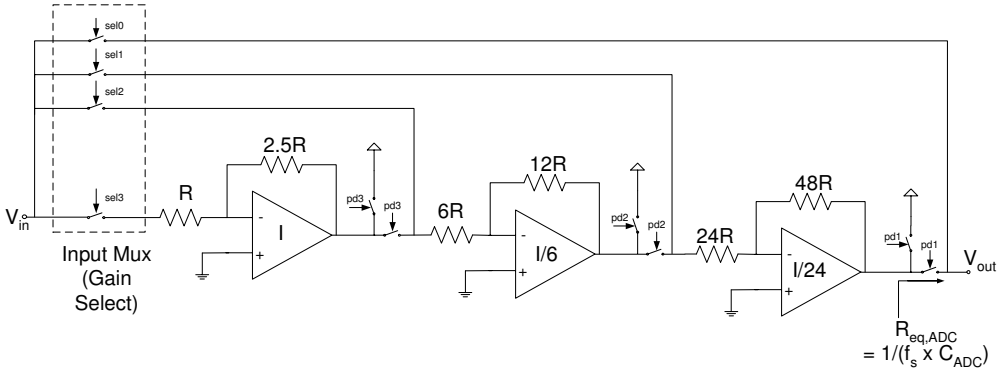
3.3.2 Cascaded Gain Amplifier with Input Gain Select

Instead of selecting which amplifier ***output*** should be selected, we propose selecting which amplifier ***input*** should be selected. Figure 3.12 shows the switched capacitor (3.12(a)) and continuous time (3.12(b)) versions of the cascaded gain amplifiers with input gain select. The first amplifier is designed for input signals ranging from $40mV_{pp}$ to $100mV_{pp}$, the second stage $100mV_{pp}$ to $200mV_{pp}$, and the last stage $200mV_{pp}$ to $400mV_{pp}$. Any signal greater than $400mV_{pp}$ would bypass all the stages and output directly into the ADC. Each stage's

input impedance is optimized for the signal power that it is meant to amplify. In these two diagrams, we are assuming that "C" is the capacitance needed to bring the thermal noise floor 14 bit below the $400mV_{pp}$ signal, and "R" is the resistance needed to bring the noise 14 bit below the $40mV_{pp}$ signal. $R_{eq,ADC}$ is the equivalent input resistance of the input capacitance of the ADC that follows the PGA, and is equal to $R_{eq,ADC} = 1/(f_s \times C_s)$. Similar to the variable input and feedback amplifier, the input impedances become optimally sized for thermal noise.



(a) Switched Capacitor



(b) Continuous Time

Figure 3.12: Cascaded Switched Capacitor Amplifier with Input Gain Select Mux

Now let us examine the power scalability of this topology. For the switched capacitor case in Fig. 3.12(a), the closed loop bandwidth of the amplifiers is given by:

$$f_{3dB-stage1} = \frac{g_{m1}}{44.57C} \cdot \frac{1}{3.5} = \frac{g_{m1}}{156C}$$

$$f_{3dB-stage2} = \frac{g_{m2}}{9.33C} \cdot \frac{1}{3} = \frac{g_{m2}}{28C} \tag{3.6}$$

$$f_{3dB-stage3} = \frac{g_{m3}}{2.33C} \cdot \frac{1}{3} = \frac{g_{m3}}{7C}$$

Equating the amplifier bandwidths gives $g_{m3} = g_{m2}/4$, which is exactly equal to the signal power scaling, $(200mV_{pp}/100mV_{pp})^2 = 4$. Similarly, $g_{m2} = g_{m1}/5.6$, which is almost equal to the signal power scaling, $(100mV_{pp}/40mV_{pp})^2 = 6.25$. The reason why the first stage does not scale as well, is because it has a higher gain amplification (hence a smaller β than the other two stages. With that, assuming that the first stage opamp is designed to consume current "I", then the second stage opamp can be designed to consume current "$I/6$", and the third stage to consumes "$I/24$", as indicated in the figure.

A similar analysis can be made for continuous time amplifiers in figure 3.12(b). The closed-loop gain accuracy of an opamp is given by $1/A\beta$, which is the inverse of the loop gain. Since sensor applications require quantities to be measured to absolute accuracy, the closed-loop gain accuracy is critical. Thus, it is important that when the PGA gain scales, the gain accuracy remains constant. The inverse of the gain accuracy is equal to $A \times \beta = g_m R_o \times \frac{R_{in}}{R_{in}+R_f}$.

Resistor values are calculated according to $4KTR$. In this case, the opamp is scaled with the resistors to maintain a constant gain (according to $g_m \times r_o$), and a constant bandwidth (according to $g_m/(\beta \cdot C_L)$). Examining the amplifier gain accuracy of this topology yields:

$$\begin{aligned} A\beta_{stage1} &= 0.6g_{m1} \times R \\ A\beta_{stage2} &= 3.5g_{m2} \times R \\ A\beta_{stage3} &= 14g_{m3} \times R \end{aligned} \tag{3.7}$$

which yields identical scalability to the switched capacitor case. Therefore, by scaling the resistors according to thermal noise tolerances, one can scale the opamp size to get the

same opamp gain and bandwidth.

From the above above topologies, it becomes apparent that the cascaded gain amplifier with input gain select is the best for automotive sensor applications. The question still remains as to whether switched capacitor, or continuous time topology should be used.

3.3.3 Switched Cap Vs Continuous Time PGA's

In order to figure out whether switched capacitor or continuous time PGA should be used, we should better understand the interaction between the sensor and the PGA. Because the sensor is a piezoresistive one, it has a finite output resistance. This means that if a switched capacitor topology is used, the *RC* time constant may be too large for the sensor output signal to settle. In a continuous time topology, the input resistance of the amplifier may be too small, which will in effect reduce the gain of the first amplifier in the cascade. In either case, the sizes of the input resistance and capacitors play a role in determining which will be used. for that we need to analyze both topologies from a thermal noise perspective.

Thermal Noise Considerations

Figure 3.13 shows the switched capacitor amplifier which was presented in the previous section as the auto-zeroing amplifier.

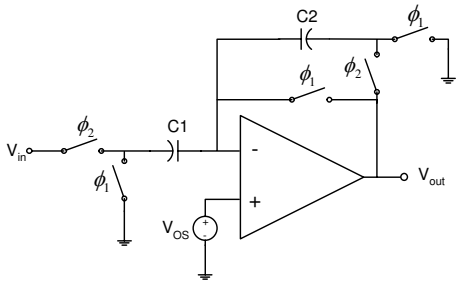


Figure 3.13: Switched capacitor amplifier

Where the gain *G* of the amplifier is C_2/C_1. The input referred noise due to the switch-

ing capacitor is

$$V_{in,n}^2 = \frac{2KT}{C} + \frac{2KT}{C} \cdot \frac{1}{G^2} = \frac{2.5KT}{C} \tag{3.8}$$

In the previous sections, we assumed that if a unit capacitor size of "C" is sufficient to bring the thermal noise power $14-bit$ below a $400mV_{pp}$ signal, then "$100C$" is sufficient to achieve a $14-bit$ SNR in the $40mV_{pp}$ case. Because all three cascaded stages are identical but scaled, it is sufficient to examine the noise of one of the stages, and then scale the capacitors by the same factor as the signal power. In our case, "C" would be the input capacitor of the incremental ADC, and the input capacitor of the amplifier stages would be as shown in figure 3.12(a).

In order to calculate the unit capacitor "C", we have to first calculate the thermal noise that can be tolerated for a $400mV_{pp}$ differential signal. A thermal noise floor of 14 bits yields $84dB$ SNR. To allow for extra margin, we designed for a noise floor of $90dB$ (15 bits):

$$V_n^2 = \frac{P_{ave}}{10^{SNR/10}} = \frac{(0.1)^2/2}{10^{90/10}} = 20pW \tag{3.9}$$

When referenced to 1Ω.

Assuming based on figure 3.3, that we select the OSR of the incremental to be 250, then the input capacitor of the incremental ADC is equal to [22]:

$$C = \frac{2.5KT}{V_n^2}/OSR = \frac{2.5KT}{20pW}/250 \approx 2pF! \tag{3.10}$$

Note that this is the differential capacitance, which means that the single-ended capacitance

is $2 \times 2pF = 4pF$, which means that the total capacitance is equal to $8pF$. That means that the input of the first stage of the cascaded amplifier will be $100C = 800pF$! which is impractical for fabrication. By increasing the OSR to 1000, the capacitor $C = 2pF$. By making the $OSR = 5000$, C can be made equal to $400fF$, which is a reasonable size for the input capacitor of a low power ADC. The input to the amplifier will still be equal to $100C = 40pF$, which is still pretty large, but not impractical for fabrication. going to higher oversampling ratios will not be practical, as that would mean increasing the bandwidth of the operational amplifiers by the OSR, and hence the power. Depending on the size of the output resistance of the piezoresistive sensor, it may not be practical to load it with a switch capacitor amplifier with such a large input capacitor. This makes switched capacitor amplifiers unattractive for resistive based sensors.

Let us examine the continuous time amplifier stages with from a thermal noise perspective. Figure 3.14 shows the noise model of the continuous time inverting amplifier.

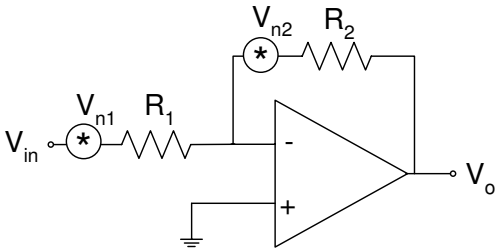


Figure 3.14: Noise model of Inverting R-amplifier

Based on the resistor noise model, we can derive the output noise power of the continuous time amplifier as being [34]:

$$V_{out,n}^2 = 4KTR_1 \times \left(\frac{R_1}{R_2}\right)^2 \times f_{NBW} + 4KTR_2 \times f_{NBW} \tag{3.11}$$

where $f_{NBW} = f_{3dB} \cdot \pi/2$. When referred to the input, the thermal noise becomes

$$V_{in,n}^2 = 4KTR_1 \times f_{NBW} + 4KTR_2 \times \left(\frac{R_2}{R_1}\right)^2 \times f_{NBW} \tag{3.12}$$

The above formulas show that there is a dependance on not only the input resistance,

but also on the $3dB$ bandwidth of the closed loop amplifier. To calculate the input resistance required to achieve $14-bits$ noise floor for a $40mV_{pp}$ signal, we get

$$\begin{aligned} V_n^2 &= \frac{P_{ave}}{10^{SNR/10}} = \frac{(0.02)^2/2}{10^{90/10}} \\ &= 200\,fW \end{aligned} \tag{3.13}$$

Therefore, the value for R_1 can be calculated in a similar way to C. Assuming that the $OSR = 5000$, then the ADC sampling frequency is equal to $2 \times 0.5kHz \times OSR = 5MHz$. Assume that the f_{3dB} of the amplifier is equal to $5\times$ the ADC sampling frequency, then R_1 can be calculated to be

$$\begin{aligned} R_1 \leq \frac{V_n^2}{4KT \times f_{NBW}} \times OSR &= \frac{200W}{4KT \times f_{3dB}\pi/2} \times 5000 \\ &\approx 1.5k\Omega \end{aligned} \tag{3.14}$$

This resistor value is too small to be the input resistance of the amplifier, considering that the output resistance of the sensor is in the order of kilo-Ohms. We cannot arbitrarily increase the resistance without reducing the effective noise bandwidth. We can see that by reducing the noise bandwidth, f_{NBW}, of the amplifier, we can increase that resistance, however, we would run into settling issues, as well as degraded residual offset due to chopping.

It is clear from the above two examples that the ideal topology for the gain stages is one where the input resistance can be increased arbitrarily without affecting the noise. The larger the input resistance, the less the effect of the variable resistance (due to the sensor and switches) will have on the amplifier. The problem with the topology above is that the because we are following a continuous-time system with a sampled system, the out-of-band noise will alias back in-band, which increases the in-band noise. This makes an anti-aliasing filter necessary for the above topology.

An active RC amplifier solves the above two problems of anti-aliasing, and R-dependance. Let us examine the noise model of the RC-Amplifier shown in figure 3.15. Analyzing the output noise power of the amplifier, we get

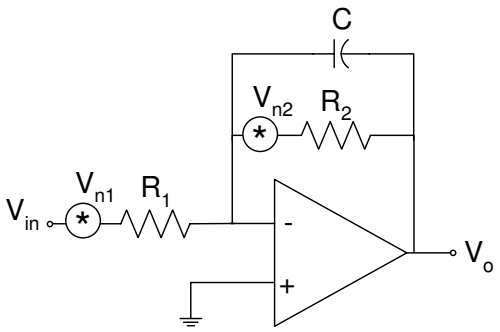


Figure 3.15: Noise Model of active RC stage

$$V_{out,n}^2 = 4KTR_1 \times (H_1(s))^2 + 4KTR_2 \times (H_2(s))^2 \tag{3.15}$$

where,

$$H_1(s) = \frac{R_2/R_1}{1+R_2Cs} \tag{3.16}$$

and,

$$H_2(s) = \frac{1}{1+R_2Cs} \tag{3.17}$$

combining 3.15, with 3.16 and 3.17, results in

$$\begin{aligned} V_{out,n}^2 &= 4KTR_1 \times \left(\frac{R_2}{R_1}\right)^2 \times \frac{1}{4R_2C} + 4KTR_2 \times \frac{1}{4R_2C} \\ &= \left(1+\frac{R_2}{R_1}\right) \times \frac{KT}{C} \end{aligned} \tag{3.18}$$

Which is independent of R_1. It is dependant only on the value of the gain (R_1/R_2), and the value of "C". Because this topology allows us to choose a high value for "R", the gain of the amplifier is not affected by the output impedance of the sensor. This means that this topology has a higher gain accuracy than the previous topologies.

3.3.4 RC Cascaded Amplifiers

Figure 3.16 shows the RC cascaded amplifier PGA with input gain select. Based on the noise calculations, the capacitors were selected to be:

$$\begin{aligned} C_1 &= 30pF \\ C_2 &= 5pF \\ C_3 &= 1.25pF \end{aligned} \tag{3.19}$$

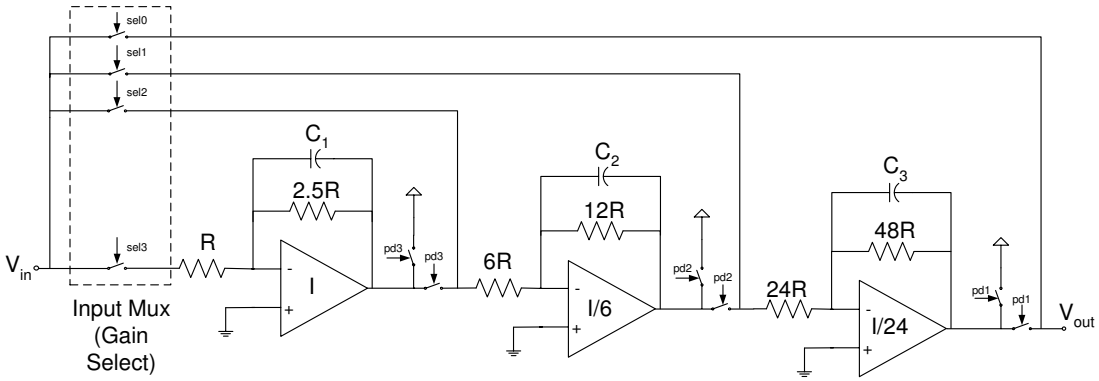


Figure 3.16: Cascaded active RC-Gain stage

$\boldsymbol{R}$ was chosen to be equal to $10k\Omega$. The value for $48R = 480k\Omega$ is a little large, however, using high resistivity poly resistors, the size on the die would not be large compared to the capacitors. Note that even though the capacitor sizes are slightly large, the total capacitor value on-chip is still less than those in the switched capacitor design.

In order to reduce the capacitor size even further, we realize that for noise purposes, a third order low pass filter (LPF) may be overkill. We can achieve the same noise performance with a first order LPF if the capacitor is sized correctly. Figure 3.17 shows the cascaded amplifier where only the last stage is an RC amplifier.

The noise calculation for this circuit is shown in the Appendix, but is summarized to be $V_{out,n}^2 = 10KT/C$ for the "Gain 10" setting, which represents the worst case. Based on that, the value of capacitor "C" is $\approx 4pF$. To allow for some margin, the capacitor was designed on-chip to be $5pF$. This design embodies all the requirements needed for amplitude power

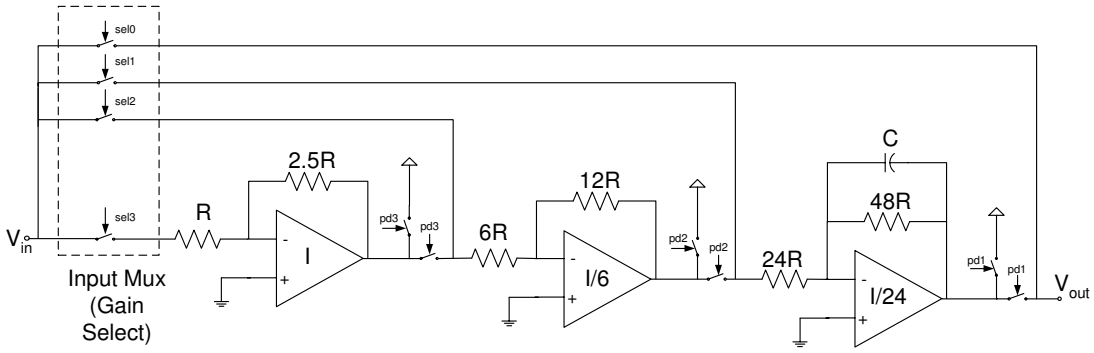


Figure 3.17: Cascaded Gain stage with final active RC stage

scalability in a sensor interface system. We have yet to examine frequency power scalability and its implementation.

3.4 Frequency Power Scaling: Periodic Power Down

There have been many implementations of frequency power scaling in ADC's, particularly, in pipelined ADC's. We will not attempt to go through a detailed analysis or comparison of the different frequency power scalable methods, and will refer the reader to the following reference [35]. We will instead explain the method that was chosen, and list some of its advantages. The objective of frequency power scaling, is to scale down the power of the

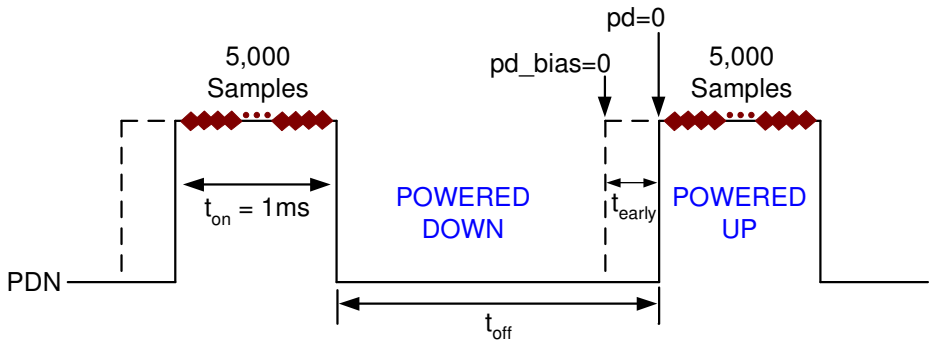


Figure 3.18: Power Down cycle of the interface

interface by a factor of 1000, when the frequency of the signal scales down by 1000 from

$0.5kHz$ to $0.5Hz$. The basic principle of the selected method of power scaling, is that, instead of scaling down the current and clock frequency of the interface and ADC, the entire interface is powered down for a period of time. That effectively reduces the average power consumption by the same amount as the Power Down (PD) factor. Figure 3.18 illustrates the power down cycle of our design. If the interface was on for t_{ON}, and off for t_{OFF}, then the power down factor would be

$$PD = \frac{t_{OFF} + t_{ON}}{t_{ON}} \tag{3.20}$$

and the average power would be:

$$P_{avg} = P_{ON} \cdot \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{P_{ON}}{PD} \tag{3.21}$$

We designed the interface so that in the $0.5kHz$ case, the system is never powered down, and in the $0.5Hz$ case, the interface and ADC have a PD factor of 1000. Since the system is oversampled by 5000, this leads to an ADC sampling clock frequency of $2 \times 0.5kHz \times 5000 = 5MHz$. This means that the interface is always turned on for $t_{ON} = 1ms$, and t_{OFF} varies depending on the frequency of the input signal. This makes the effective sampling rate of the ADC equal to:

$$F_{s,effective} = \frac{F_s}{PD} \tag{3.22}$$

Which means that the effective OSR is maintained regardless of the input frequency. For the $0.5Hz$ case ($PD = 1000$), the OSR is equal to $F_{s,effective} / (2 \times fin)$.

In figure 3.18, we have shown that there are two ”power up” signals, with a time difference of t_{EARLY}. This is to allow crucial parts of the circuits, such as opamp bias circuits to be powered up and ready before the rest of the interface and ADC are powered up. The power down control was implemented by programming a finite state machine (FSM) on an FPGA board.

Chapter 4

Circuit Level Implementation and Simulations

In this chapter, we will discuss the circuit level implementation of our sensor interface system that was presented in the previous chapter. We will discuss the opamp topologies used in the interface design, and circuit implementation of power-down techniques used. We will then discuss the buffer stage that was used after the interface. The chopper clock generation techniques will also be presented. Finally, we will discuss design for testability, and present its implementation in our design.

4.1 Operational Amplifiers

As discussed in chapter 2, because sensor applications deal with very slow signals, dynamic offset and $1/F$ noise cancelation techniques are necessary in order to achieve high accuracy. We have discussed different implementations, such as auto-zeroing and chopping. Since our interface implementation uses continuous-time amplifier stages, chopping is the technique of choice. In our design, we will use the two-stage chopper amplifier, with the demodulation chopper after the first stage. We have discussed this topology in chapter 2, and in figure 4.1, we re-show the two-stage amplifier of choice.

For this application, a two stage amplifier was better than a single stage one because it has a higher gain, and hence a better gain accuracy. The chopping frequency was selected to be $1/2$ of the ADC sampling frequency, $f_{chop} = 2.5MHz$. In chapter 2, we have discussed how the above architecture is suitable for high chopping frequencies.

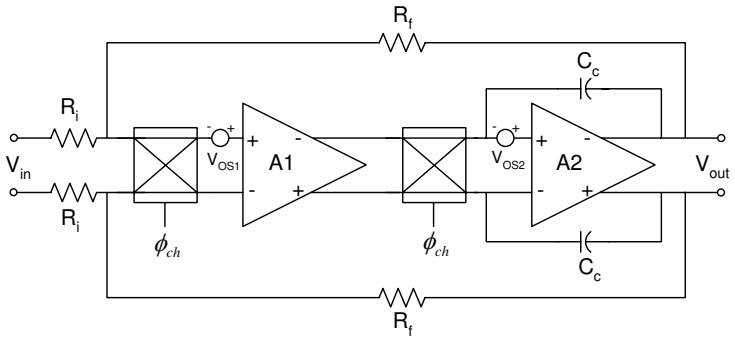


Figure 4.1: The two-stage chopper amplifier

4.1.1 Opamp Topology and Sizes

Figure 4.2 shows the circuit implementation of the fully differential opamp shown in figure 4.1. The architecture presented is based the Power Resettable Opamp (PROpamp) shown in [35], although in the reference, the opamp used was a gain boosted folded cascode opamp [36] as opposed to a two-stage one presented in here.

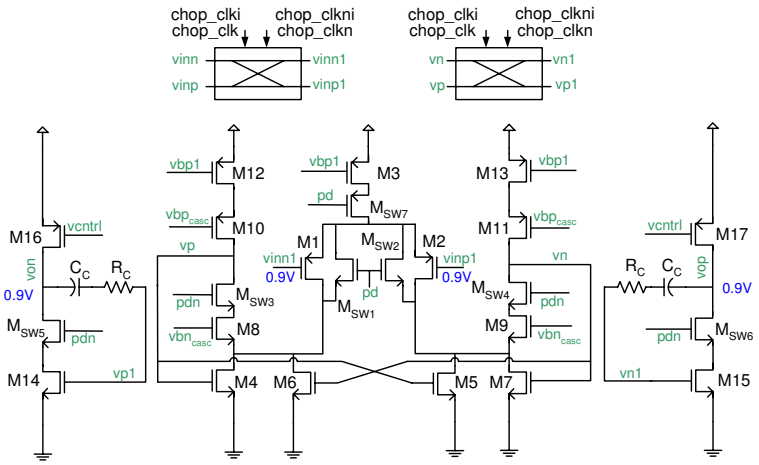


Figure 4.2: two-stage chopped Opamp circuit diagram

Table 4.1 shows the transistor and component sizing for the three stages in the opamp. The transistor lengths used were larger than the minimum size in order to reduce the $1/F$ noise effect by increasing the area. PMOS input transistors are often used in sensor applications because they exhibit better $1/F$ noise performance. As was stated in chapter

2, $1/F$ noise comes from the trapped carriers in the gate oxide. Since the PMOS carriers (holes) are larger then the NMOS carriers (electrons), they are less likely to get trapped and gradually released.

Table 4.1: Opamp Transistor Sizing for the three stage cascade amplifier

Component Name	***First Stage Sizing***	***Second Stage Sizing***	***Third Stage Sizing***
$M1, M2$	$96 \times 2/0.25$	$16 \times 2/0.25$	$4 \times 2/0.25$
$M3$	$48 \times 4/0.50$	$8 \times 4/0.50$	$2 \times 4/0.50$
$M4 - M7$	$24 \times 1/0.50$	$4 \times 1/0.50$	$1 \times 1/0.50$
$M8, M9$	$24 \times 1/0.50$	$4 \times 1/0.50$	$1 \times 1/0.50$
$M10 - M13$	$24 \times 4/0.50$	$4 \times 4/0.50$	$1 \times 4/0.50$
$M14, M15$	$56 \times 1/0.50$	$8 \times 1/0.50$	$4 \times 1/0.50$
$M16, M17$	$52 \times 4/0.50$	$8 \times 4/0.50$	$4 \times 4/0.50$
M_{SW1}, M_{SW2}	$8 \times 2/0.18$	$4 \times 2/0.18$	$1 \times 2/0.18$
M_{SW3}, M_{SW4}	$20 \times 2/0.18$	$10 \times 2/0.18$	$4 \times 2/0.18$
M_{SW5}, M_{SW6}	$60 \times 2/0.18$	$30 \times 2/0.18$	$8 \times 2/0.18$
M_{SW7}	$26 \times 4/0.18$	$12 \times 4/0.18$	$4 \times 4/0.18$
R_C	$1k\Omega$	$4k\Omega$	$5k\Omega$
C_C	$6pF$	$1.2pF$	$900fF$

Table 4.1 also shows how the opamp transistors scale with the input signal power. R_C is a lead compensation resistor and is sized to optimize the phase margin of the amplifiers.

The amplifiers were designed to achieve a gain of approximately $80dB$, and a bandwidth of approximately $25MHz$, which is $10\times$ the chopping frequency. The AC simulation parameters of the opamps are presented in table 4.2.

Table 4.2: AC Simulation Parameters for the Three Amplifiers

Parameter	***First Stage***	***Second Stage***	***Third Stage***
$A\beta$	$82.2dB$	$81.7dB$	$80.9dB$
$\beta \cdot F_t$	$25MHz$	$23MHz$	$23MHz$
$PhaseMargin$	88^o	68^o	77^o
$CurrentConsumption$	$2.14mA$	$319.72\mu A$	$121.72\mu A$

4.1.2 Common Mode Feedback (CMFB)

Transistors $M4 - M7$ in figure 4.2 form the common-mode feedback for the first stage of the opamp, known as the "inherent common mode feedback" [37]. Due to stability considerations, a two-stage fully differential opamp is usually designed with two common-mode feedback stages, one for each stage. This is increases power consumption, which is unwanted in low power sensor design. The "inherent common mode feedback" structure eliminates the need for a specialized CMFB circuit. Its basic operating principle is that the cascoded current source is split into two equally sized sources, and the gates are cross coupled at the differential output of the first stage to form a negative feedback. The output impedance seen by the differential signal is high, limited by the output impedance of the PMOS cascoded load. The common mode impedance, however, is dominated by $(gm_{M4} + gm_{M6})$ and $(gm_{M5} + gm_{M7})$. Because of this low common mode impedance, the cross coupled feedback structure is sufficient and there is not need for an additional CMFB circuit [37] [38].

The second stage of the opamp, which is a Class A common-source output stage, requires its own common mode feedback circuitry, shown in figure 4.3. Since the amplifiers are continuous time, the output is always expected to be available, and so is the common mode, hence a continuous time common mode structure was used. The circuit senses the output common mode voltage of the opamp through resistors R_{CM}, and compares it to an off-chip common mode level, vcm_{oc}. The relative current in the branches is then steered either way to produce a common mode control voltage, *vcntrl*, that feeds into the current source of the output stage.

Similar to the opamp, the CMFB circuit was scaled in size by the same factor as the opamp whose common mode it controls. Table 4.3 shows the sizing of the CMFB circuit in the three amplifier stages.

R_{CM} was selected at a relatively high value so that the output impedance would not be affected, hence reducing the gain of the amplifier.

4.1.3 Chopper Switches

The chopper switches were implemented using transmission gates, such as the ones shown in figure 4.4.

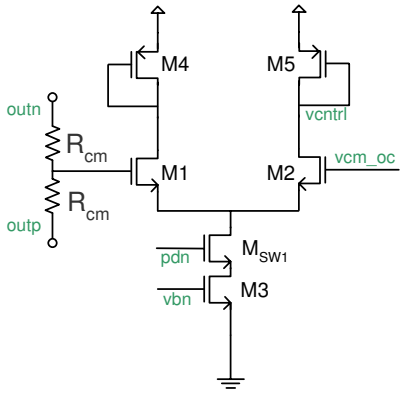


Figure 4.3: CMFB circuit

Table 4.3: CMFB Transistor Sizing for the three stage cascade amplifier

Transistor Name	***First Stage Sizing***	***Second Stage Sizing***	***Third Stage Sizing***
$M1, M2$	$96 \times 2/0.25$	$16 \times 2/0.25$	$4 \times 2/0.25$
$M3$	$48 \times 4/0.50$	$8 \times 4/0.50$	$2 \times 4/0.50$
$M4, M5$	$24 \times 1/0.50$	$4 \times 1/0.50$	$1 \times 1/0.50$
R_{CM}	$100k\Omega$	$200k\Omega$	$200k\Omega$

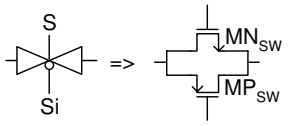


Figure 4.4: Chopper switch implementation: transmission gate

The sizings of the switches are shown in table 4.4. Since the input chopper are on the virtual ground node, there is no signal component, and hence the transistors are minimum sized. Since the output choppers contain some signal component (although still small, equal to V_{out}/A_2), the transistors are sized 5 times the minimum. This sized was optimized to produce the best distortion performance after simulation.

4.1.4 Bias Circuit Power Down

The first amplifier stage has its own bias circuit, whereas the second and third stage both share a bias circuit. Because the opamps are periodically powered down due to power

Table 4.4: Input and Output Chopper Switch Sizing

Transistor Name	*Input Chopper W/L*	*Output Chopper W/L*
MN_{SW}	$1 \times 0.6/0.18$	$5 \times 4/0.18$
MP_{SW}	$1 \times 2.0/0.18$	$5 \times 1/0.18$

scaling with respect to frequency, there is no use for the bias circuit during the "OFF" time, hence the bias circuit must also be powered off.

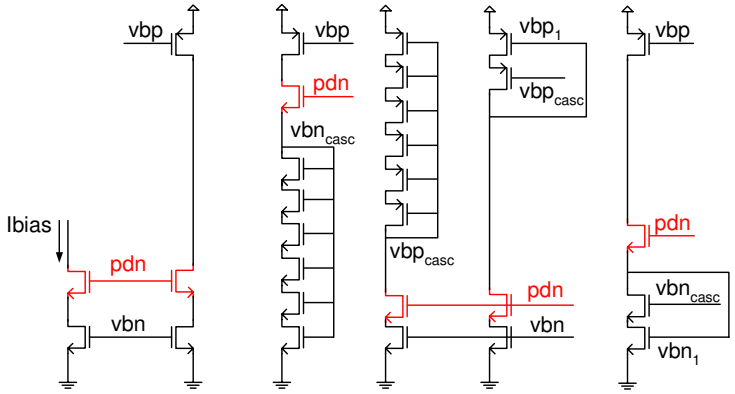


Figure 4.5: Opamp bias with power down switches

Figure 4.5 shows a schematic diagram of the opamp bias circuit with power down switches. The power down switches are shown in red. When the opamp and bias are in power down mode and are "OFF", the current is literally cut off from the branches, and the bias voltages get pulled to V_{th} for NMOS, and $V_{DD} - V_{th}$ for PMOS. During the "ON" time, the bias circuit is given a few clock cycles to recover prior to the opamp, as explained in the previous chapter. This ensures that the opamp recovers faster, and hence no samples are wasted.

4.2 Output Buffer Stage

The last stage of the cascade amplifier is designed to drive the next stage's ADC, which would have an input sampling capacitance of $500\,fF$. Because the interface design did not include the on-chip ADC, the last stage amplifier sees an output capacitance that includes

the sum of the bonding pad and bonding wire capacitance, the PCB trace capacitance, as well as the input capacitance of the off-chip ADC. This bonding pad and wire capacitance on their own add up to approximately $2pF$, which is $4\times$ the capacitance that the amplifier was meant to drive. This may lead the amplifier to go unstable unless an output buffer stage was designed to drive that large capacitance.

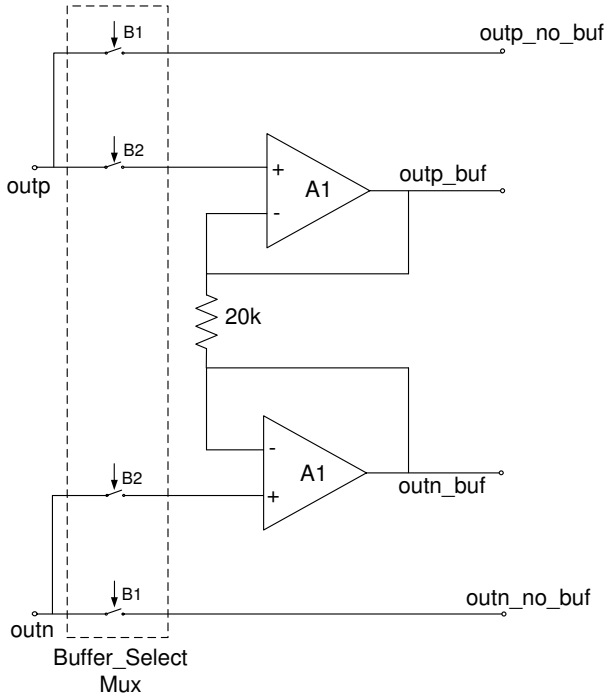


Figure 4.6: Output buffer topology

Figure 4.6 shows a system diagram of the output buffer. An instrumentation amplifier topology was used for the output stage. This topology has the advantage of infinite input impedance, and hence does not affect the gain of last stage amplifier. Moreover, this topology has high common mode rejection [39]. The disadvantage of this topology is that the input amplifier has to tolerate the entire output swing which may degrade the distortion performance compared to other architectures. However, since the signals we are dealing with are low amplitude signals ($400mV_{pp}$ differential), this design is sufficient to ensure low distortion performance. Figure 4.6 also shows that the buffer can be bypassed through the "Buffer-Select" mux. The buffer would be bypassed during the testing phase, in the

case where we would like to verify the output common mode of the PGA.

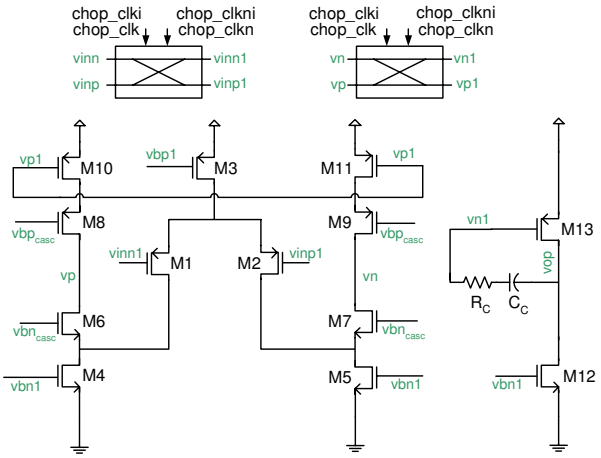


Figure 4.7: Buffer Opamp circuit

Figure 4.7 shows the circuit implementation of one of the buffer opamps. The design is a differential-to-single-ended two-stage opamp with a PMOS folded cascode as a first stage and a class-A common source output stage. This amplifier is also chopped to reduce its offset and $1/F$ noise contribution. Because the input differential pairs experience the full signal swing, the input choppers have to be sized appropriately. In this case, both the input and output choppers were designed to be $5\times$ the minimum size switches.

Table 4.5: Opamp Transistor Sizing for the three stage cascade amplifier

Component Name	***Component Sizing***
$M1, M2$	$88 \times 2/0.25$
$M3$	$48 \times 4/0.50$
$M4, M5$	$48 \times 1/0.50$
$M6, M7$	$24 \times 1/0.50$
$M8 - M11$	$24 \times 4/0.50$
$M12$	$216 \times 1/0.50$
$M13$	$216 \times 4/0.50$
R_C	100Ω
C_C	$15pF$

Table 4.5 shows the transistor sizes of the buffer opamp. The opamp was designed to

drive a $20pF$ output capacitance, which is sufficient for our purposes. The buffer stage was designed with a gain of $97dB$, and a bandwidth of $27MHz$. The current consumption of the buffer opamp is $2.414mA$, although the buffer power consumption is not included within the interface power budget since it was designed only so that the interface can be properly tested.

4.3 Chopping Clock Generation

The chopper clocks were implemented using non-overlapping clocks. Figure 4.8 shows the non-overlapping clock generator used.

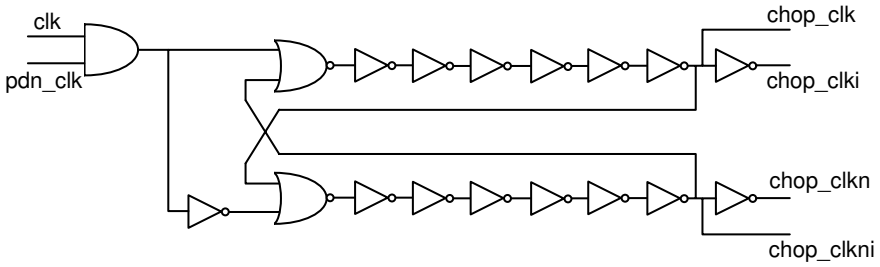


Figure 4.8: Non-overlapping chopper clock generator

The clock generator can also be powered down with the rest of the interface when in frequency scaling mode. Moreover, the clock power down signal is given a separate pin, which means that the clock generator can be powered down independently from the rest of the interface. This will become useful in the testing phase when we would like to examine the effects of chopping.

4.4 Gain and Buffer Select Mux

The input Gain-Select mux, and the Buffer-Select mux have similar implementations such as the one shown in figure 4.9. The switches are implemented using transmission gates, since the common mode of the input signals is mid-rail.

The control logic uses a “one-hot-encoding” logic which turns on only one of the switches at a time, preventing the signal from entering the amplifier through multiple paths. The switches have to be sized so that the variation in switch resistance does not severely

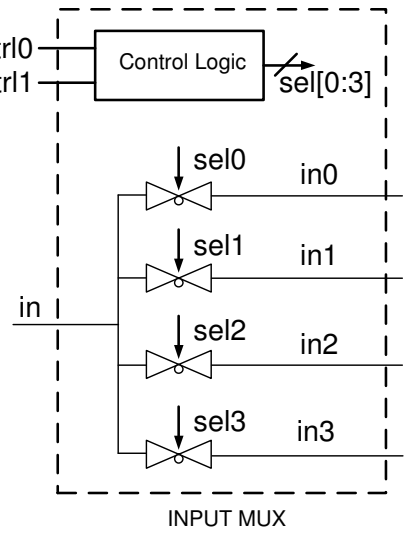


Figure 4.9: Circuit implementation of input select Mux

degrade the distortion performance of the entire system. Based on simulation, the switches were sized to $5\times$ the minimum size, similar to the buffer chopper switches.

4.5 Design for Testability: Analog Test Mux

One of the major challenges of any IC engineer is to be able to debug a design with limited access to the internal nodes. Because any IC will have a limited number of output pins, it is virtually impossible to debug a design in the lab as we do in simulation without planning for it during our design phase, hence the term "Design for Testability". The idea is that a designer has to identify critical signals that would help identify, with certainty, the functionality of the circuit blocks, and the sources of error in cases when we do run into problems in the lab.

In our case the key signals are the opamp bias signals, and the intermediate output signals of each amplifier stage. As such, we have implemented an "Analog Test Mux", in order to probe the important signals in our design.

Figure 4.10 shows a diagram of our implementation of the analog test mux (Amux). The switches are arranged in a "T" configuration, and were designed using minimum sized transistors in a transmission gate topology. The switch control signals were applied using

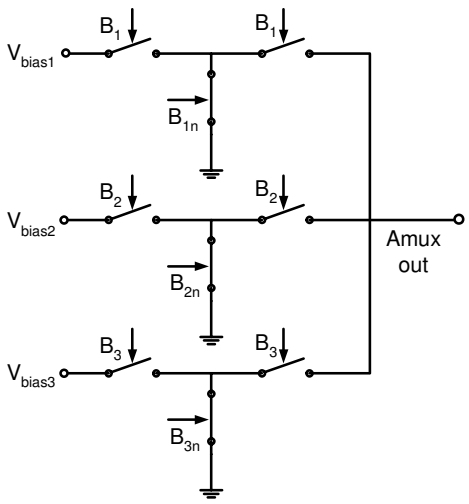


Figure 4.10: Implementation of the analog test mux

a custom-designed shift register. When the signal is being probed (say V_{bias1}), the top two switches (B_1) at the head of the T are closed, and the bottom switch (B_{1n}) at the tail is open. The other two paths have the opposite switching configuration. The paths between the two switches are pulled to ground for the signals that are not being probed. This ensures that there is no signal feed-through between the signal that is being probed and the ones that are not being probed. The bits that select which Amux signal to probe are encoded using the "one hot encoding" scheme. Using the Amux allows multiple signals to be probed using only a few output pins.

4.6 Key Simulation Results

In this section, we show key simulation results of the PGA interface at nominal process (TT), voltage ($1.8V$) and temperature (25^o). Because the system was designed with a very large oversampling ratio, simulating it at its operating bandwidth ($0.5Hz - 0.5kHz$) would be impractically long. Hence, the input signal applied was increased to $10kHz$ to decrease the simulation time. The output of the interface was sampled at $5MHz$ using a verilog sampler block. Figure 4.11 shows a Total Harmonic Distortion (THD) Vs input amplitude plot of the interface.

Excluding the "Gain = 1" setting, which bypasses the entire interface, the PGA has a

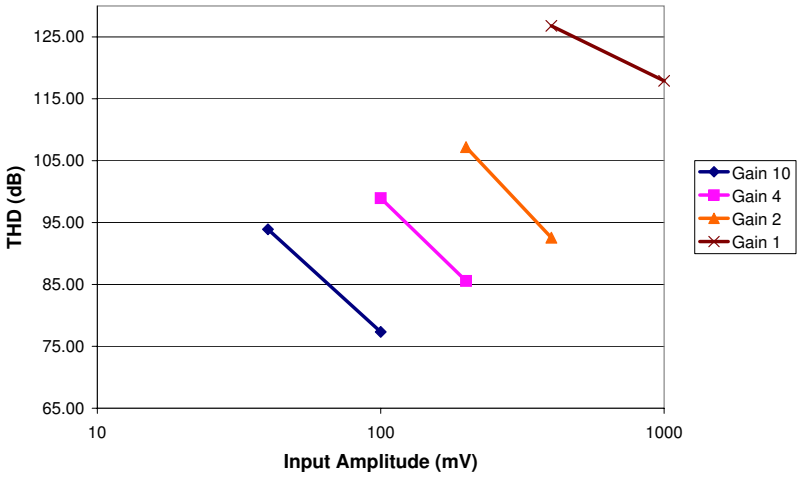


Figure 4.11: THD Vs Input Amplitude with different Gain settings

THD range of $77dB - 107dB$. From the plot, it is apparent that the worst case is the "Gain = 10" setting, with an input amplitude of $100mV_{pp}$. Simulations at lower input frequencies were run at that gain setting to verify the functionality and performance, however, not at the rest of the gain settings, due to lengthy simulation times mentioned earlier.

Figure 4.12 shows a plot of the PGA power consumption Vs input amplitude when simulated at a nominal process and a temperature of 25^o. Based on the simulations, the power of the PGA scales as predicted with respect to input amplitude.

Table 4.6 shows the power consumption values of the interface. One observation from the plot is that the ratio of power going from the Gain 4 setting to the Gain 2 setting is approximately 2.8 instead of 4. This is because the calculations did not account for the opamp bias circuitry power, which makes up for the difference in power consumption.

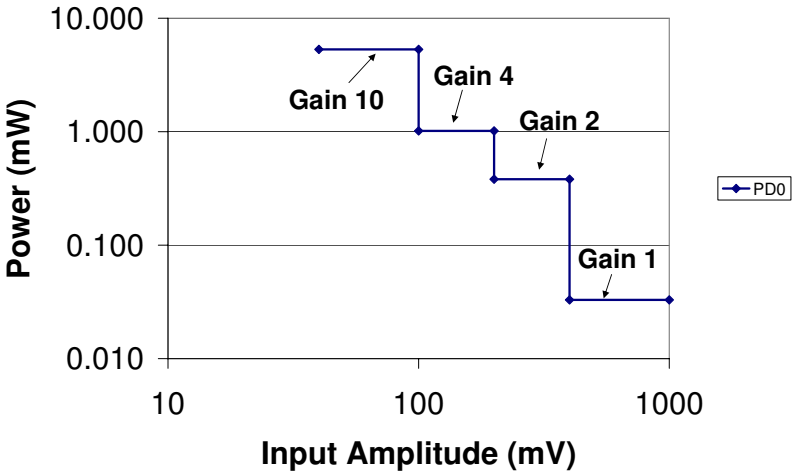


Figure 4.12: Power Vs Input Amplitude

Table 4.6: Simulated Power Consumption

Input Amplitude (mV_{pp})	***Gain Setting***	***Power Consumption*** (mW)
40	10	5.278
100	10	5.278
101	4	0.984
200	4	0.984
201	2	0.349
400	2	0.349
401	1	0.001
1000	1	0.001

Chapter 5

Experimental Results

IN this section, we discuss the experimental results of the power scalable PGA, which was fabricated in 0.18μm CMOS process. In section 5.2, we discuss the Test setup in detail as well as the test methodology used to characterize the PGA. In section 5.3 and 5.4, we characterize the signal generator, and the off-chip ADC used to capture data from the PGA. The purpose of these tests is to establish with certainty the maximum performance that can be captured from the entire system, since the performance can potentially be limited by setup, and not by the PGA itself. In section 5.5, we present and explain the test results of the fabricated PGA. The PGA was able to achieve a dynamic range of 80dB (13 bits), and a noise distribution of 170$nV/\sqrt{Hz}$ with chopping. Power scalability with respect to input amplitude was done by running the PGA with a wide range of input amplitudes (40mV_{pp} -1V_{pp}), and varying the gain accordingly to get a 400mV_{pp} -1V_{pp} output . Power scalability with respect to input frequency was tested by running 5 different power down modes. The operating power range for the PGA (over frequency and amplitude) is 4μW to 5.33mW.

5.1 IC Fabrication

The power scaleable PGA was implemented in a 0.18μm CMOS process (nominal $V_{DD} = 1.8V$), and fabricated through the Taiwan Semiconductor Manufacturing Corporation (TSMC) in a single poly, 6-metal process, including MIM capacitor and Deep N-Well layer options. The PGA core area was $1.0mm \times 0.6mm (0.6mm^2)$, the core area including the

buffer was $1.3mm \times 0.6mm (0.8mm^2)$, and the total area including the bonding pads was $1.7mm \times 1.0mm (1.70mm^2)$. The integrated circuit was packaged in a 44-pin CQFP package. To minimize power supply related noise, analog pins were separated from digital (clock) pins on the power supply ring surrounding the ADC core. Moreover, the buffer's power supply was seperated from the PGA's analog supply, to allow for higher supply voltages for the buffer. A die photograph of the fabricated IC is shown in figure 5.1, with key blocks highlighted.

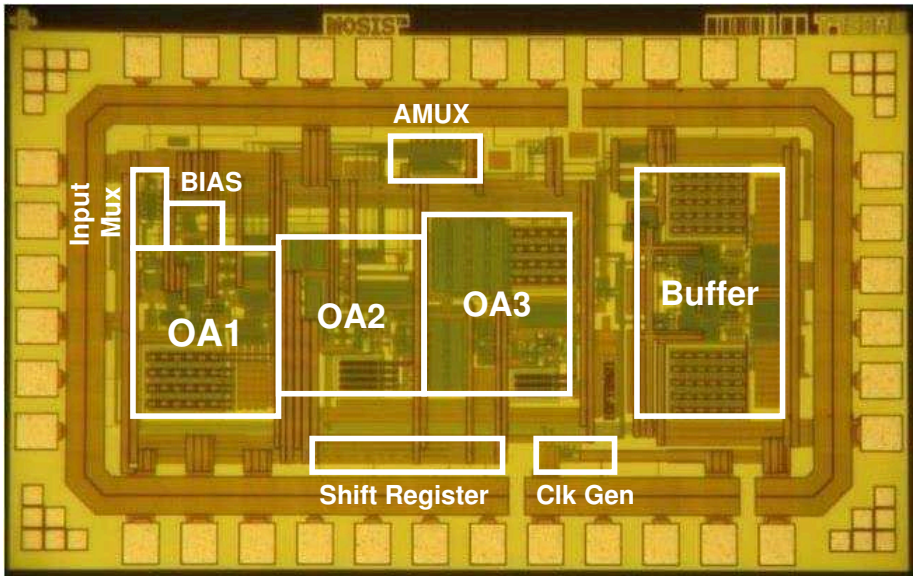


Figure 5.1: DUT Die Photo

5.2 Test Setup

5.2.1 System Level Representation

Figure 5.2 shows a system level diagram of the test setup used to evaluate the performance of the DUT (***Device Under Test***). The Stanford Research System (***SRS***) function generator was used because it has a high dynamic range at low frequencies. The Analog Devices ADC (***AD9240***) was used because it can measure up to 14 bits resolution (12.2 SNDR ENOB). It is also has a typical SFDR rating of $90dB$, and a typical THD of $85dB$ at maximum input

range. The ADC was sampled at 5*MHz* using a crystal oscillator. An Altera FPGA board was used for Power-Down signal generation. The FPGA was clocked using the same 5*MHz* crystal oscillator used to sample the ADC.

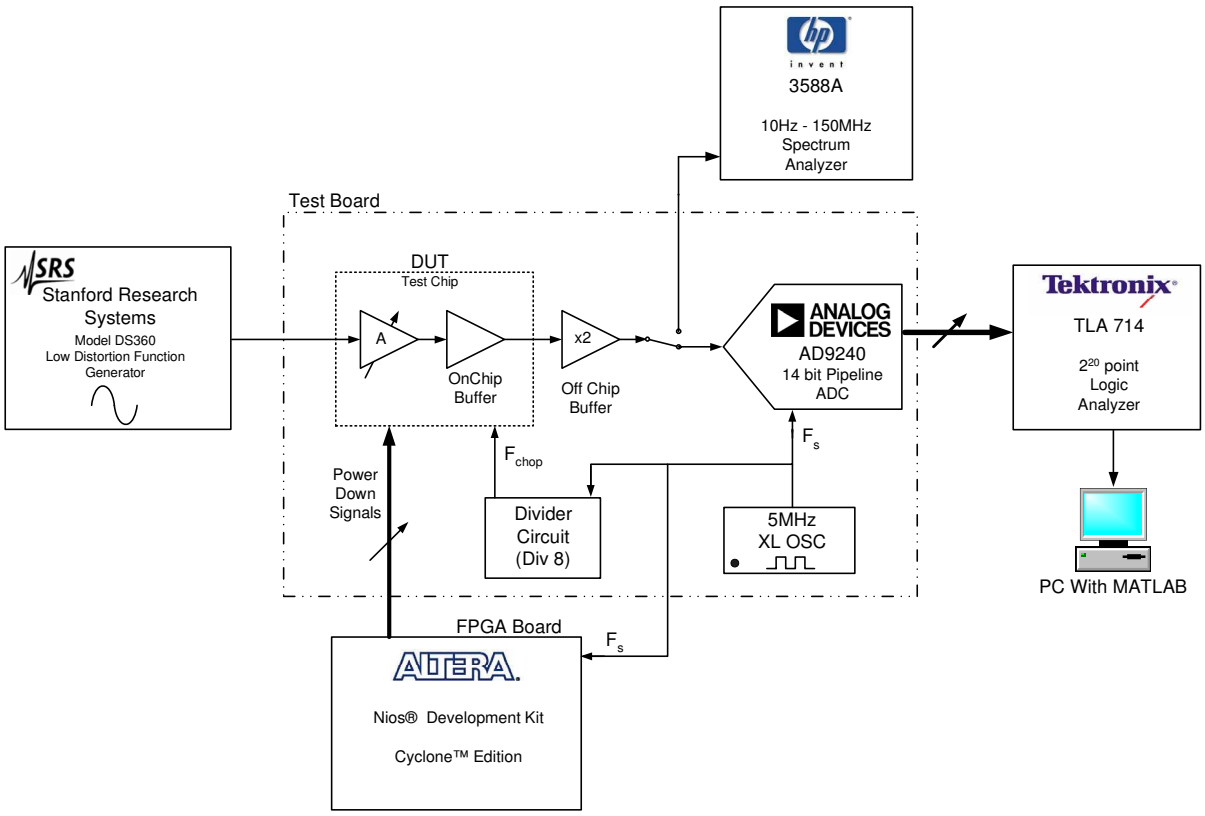


Figure 5.2: System Diagram of The Test Setup

The output of the PGA can be disconnected from the ADC and connected to an ***HP3855A*** spectrum analyzer. This serves as both a contingency in case the ADC does not work properly, as well as helps isolate any anomalies that might occur from the ADC.

5.2.2 Printed Circuit Board

A 4 layer FR4 dielectric PCB board with a minimum 6*mil* trace was designed and constructed for the DUT. Figure 5.3 shows the layout of the Printed Circuit Board (PCB). The Power planes on the board was split up into analog, digital, and board power planes. The

power supply voltages for the DUT, and other on-board IC's were generated by low noise ***LM1117*** regulators. The common mode was generated by using a potentiometer as a resistor divider. The desired voltage is then buffered through an ***LM7301*** opamp connected in unity gain configuration.

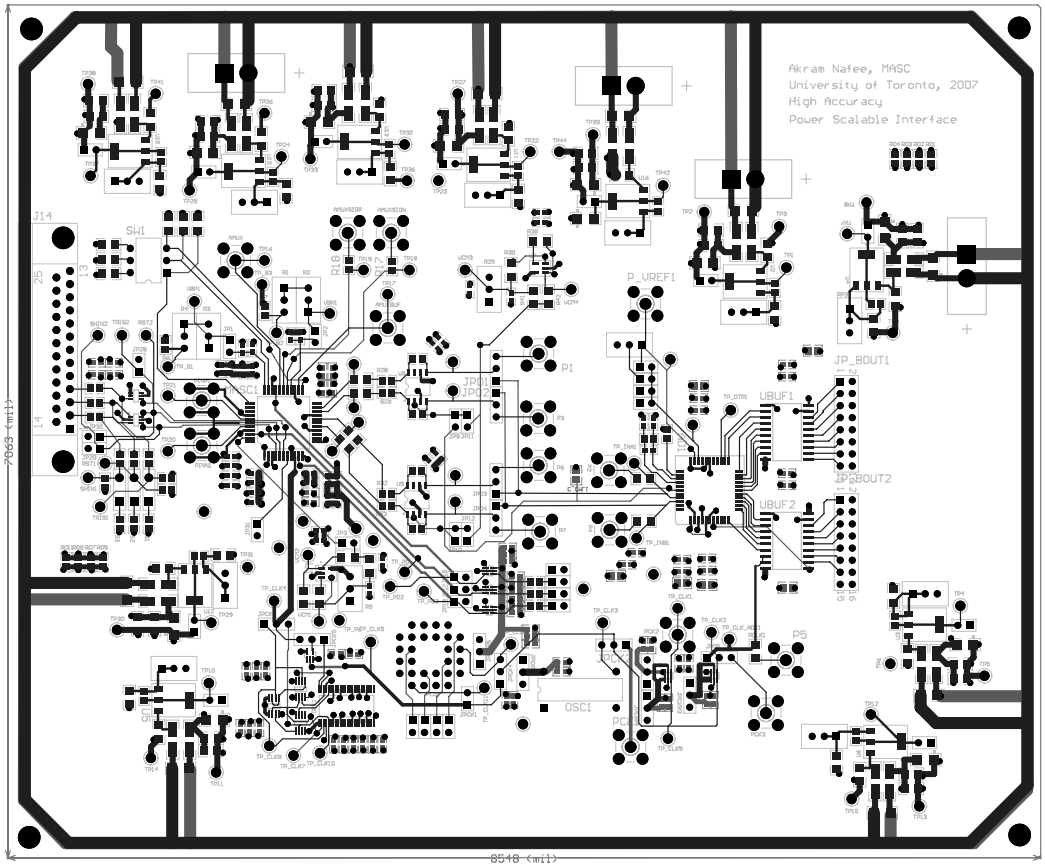


Figure 5.3: Printed Circuit Board Layout

5.2.3 IC Test Methodology

Due to limitations in the test setup, the DUT was tested under slightly different than the intended operation. Figure 5.4 illustrates a representation of the intended operation (a), which was also illustrated in chapter 3, and the testing method when the power-down modes are used (b).

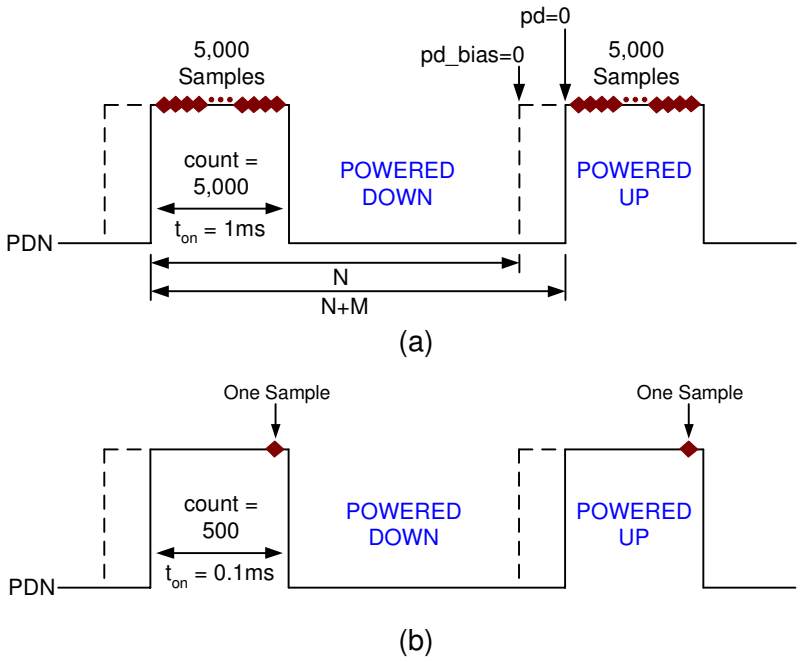


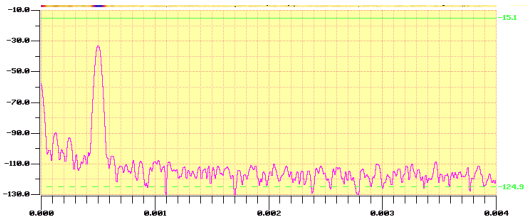
Figure 5.4: Power-Down Cycle (a)intended operation, and (b)measured

Because the logic analyzer could only store $2^{20} = 1048576$ points, if we were to average 5000 sample points for every ON time (as shown in figure 5.4(a)), we would end up with only 200 points to plot an FFT. As an alternative, only one point was sampled every ON time (as shown in figure 5.4(b)). Moreover, in the power down by 1000 case (where the input signal is $0.5Hz$), the interface would be ON for $1ms$, and OFF for $0.999s$. That means that we would take only one data point every second, which meant that we would have to wait a million seconds for a million point FFT! In order to reduce the testing time, we reduced the power down period by a factor of 10, while keeping the ON/OFF duty cycle the same. Moreover, as we go to lower input frequencies, the number of FFT points was reduced, in order to reduce the data capture time.

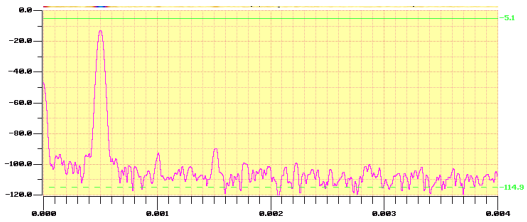
For the "No-Power-Down" case ($F_{in} = 0.5kHz$) the signal was sampled at the full rate of $5MHz$ (OSR = 5000), and the full million point FFT was taken without averaging every 5000 samples.

5.3 Signal Generator Characterization

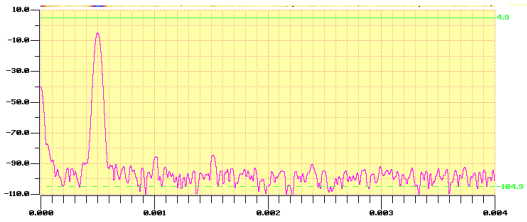
Because of the high accuracy requirement of the DUT, the test setup must be characterized to verify that it does not limit the overall performance of the system. The SRS Signal generator was characterized using the $HP3588A$ spectrum analyzer to determine its maximum linearity as a function of amplitude and frequency. Figures 5.5(a) to 5.5(c) show the spectra for the signal generator output at $481.605Hz$ and different amplitudes, and figures 5.6(a) to 5.6(c) show the spectrum for a $243.187Hz$ signal.



(a) Amplitude = $40mV_{pp}$



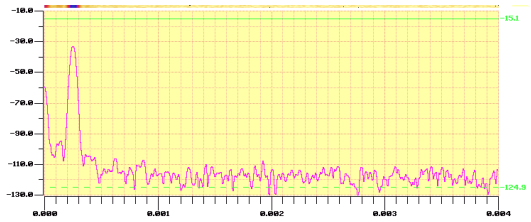
(b) Amplitude = $400mV_{pp}$



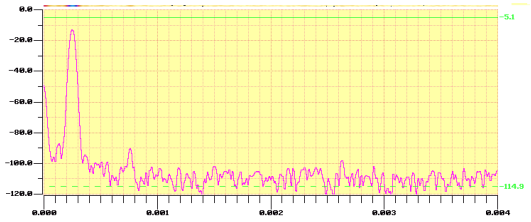
(c) Amplitude = $1V_{pp}$

Figure 5.5: Signal Generator Spectra with different output amplitudes, $F = 481.605Hz$

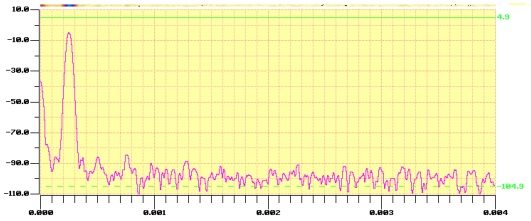
There are two important points to note from the output spectra. First, in all cases, the signal generator seems to be give a worst case SFDR of around $84dB$. This is sufficient to test a 13-bit system, and a little less than sufficient to test a 14-bit system. Ideally a $90dB$



(a) Amplitude = $40mV_{pp}$



(b) Amplitude = $400mV_{pp}$



(c) Amplitude = $1V_{pp}$

Figure 5.6: Signal Generator Spectra with different output amplitudes, $F = 243.187Hz$

dynamic range signal source would be sufficient to test a 14 bit system, to ensure that the system is not limited by the signal source. Second, it is apparent that there is a $60Hz$ (and its harmonics) component in the output signal. This will be ignored in any further analysis of test results for the DUT, since the target application is battery powered and would not suffer from AC supply noise.

5.4 ADC Characterization

As was mentioned in the ***Test Setup*** section, a 5MHz ADC was used on board to digitize the output sine wave for analysis. The AD9240 was characterized by applying the input from the SRS signal generator directly into the ADC input through SMA connectors at the input

of the ADC. The reference voltage of the ADC was measured to be $1.5V$ ($V_{top} = 4.0V$, $V_{top} = 1.0V$, and $VCM = 2.5V$). Figures 5.7 and 5.8 show the Spurious Free Dymanic Range (SFDR) and the Total Harmonic Distortion (THD), respectively of the ADC.

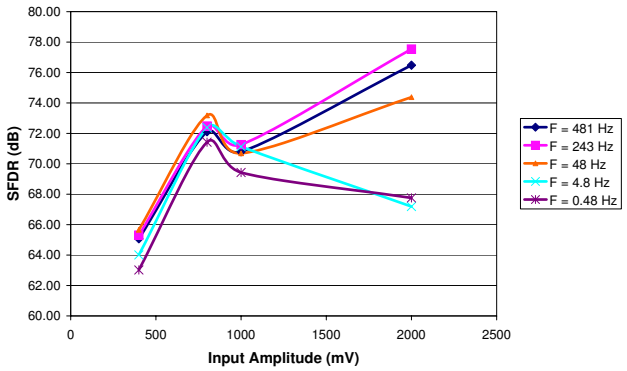


Figure 5.7: SFDR Vs Input amplitude of the External ADC

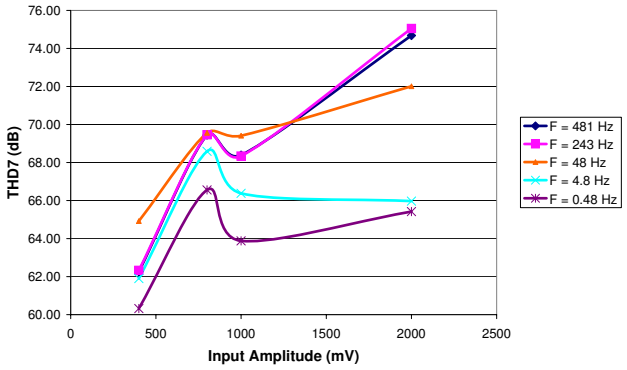
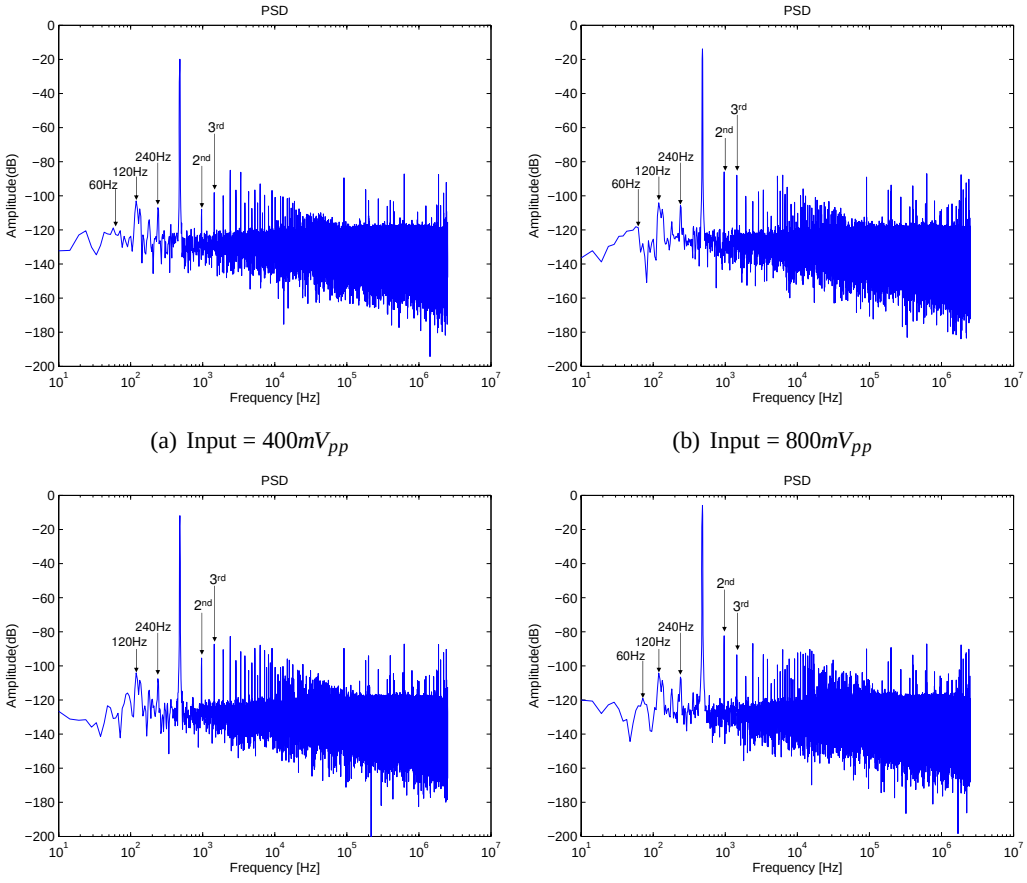


Figure 5.8: THD7 Vs Input amplitude of the External ADC

Figure 5.9 shows some sample power spectral density plots of the ADC output with different input amplitudes. From the PSD's we can see that there are higher order spurs that dominate over the third order harmonic. That may be attributed to the fact that the ADC input was not buffered, or that the voltage references are not clean. Due to the lack of testability in the external ADC, it was difficult to ascertain the cause of that dominant $5, 6$ and 7^{th} order harmonics.

Figures 5.10 and 5.11 show the SFDR and THD plots of the ADC that only include up



(a) Input = $400mV_{pp}$

(b) Input = $800mV_{pp}$

(c) Input = $1000mV_{pp}$

(d) Input = $2000mV_{pp}$

Figure 5.9: ADC Characterization Spectra, $F_{in} = 481.605Hz$

to the third order harmonic. The difference between the curves below and above clearly indicate that in nearly 50% of the cases, the dominant harmonic was higher in frequency than the third order harmonic.

5.5 IC Test Results

5.5.1 DC Bias Points

Because of the analog test mux (AMUX) that was designed, it was relatively easy to be able to probe the DC bias voltages of the OPAMPs and compare them to the simulations.

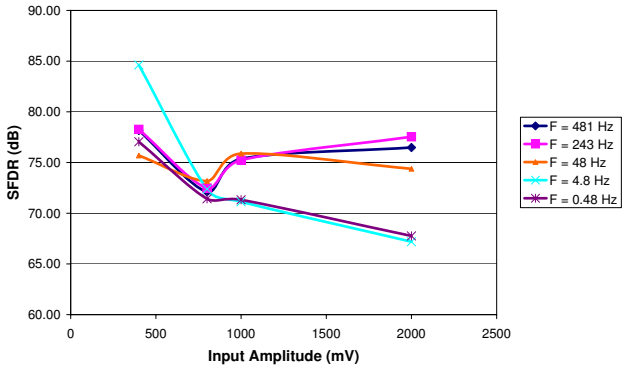


Figure 5.10: SFDR Vs Input amplitude of the External ADC

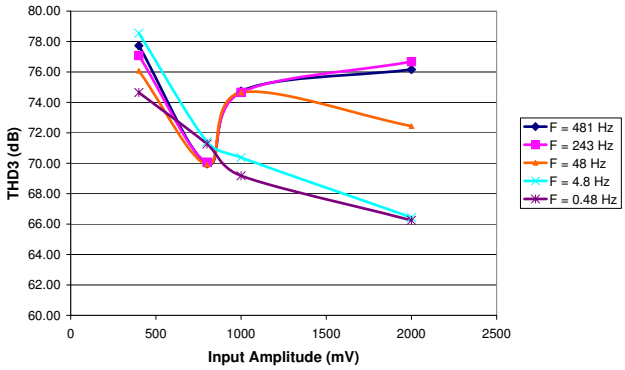


Figure 5.11: THD3 Vs Input amplitude of the External ADC

table 5.1 below shows the measured and simulated (over typical and slow corners) results of DC bias points in the Amplifier OPAMPs as well as the buffer. Refer to figure 4.5 for the bias voltage names.

Relative to the typical corner, all of the measured bias voltages were within $50mV$ from the simulated values. This table shows that all current sources and cascode transistors are well within the active region, with no transistors in triode.

Table 5.1: DC Bias Points: Simulated and Measured

	AMPLIFIER1			***AMPLIFIER 2,3***			***BUFFER***		
	Simulated		Measured	Simulated		Measured	Simulated		Measured
	[V] (TT)	[V] (SS)	[V]	[V] (TT)	[V] (SS)	[V]	[V] (TT)	[V] (SS)	[V]
VDD	1.80	1.80	1.80	1.80	1.80	1.80	1.91	1.91	1.91
VBP	1.22	1.17	1.17	1.22	1.17	1.17	1.36	1.31	1.31
VBN	0.60	0.66	0.62	0.60	0.66	0.63	0.58	0.64	0.61
$VBP1$	0.83	0.77	0.86	0.83	0.77	0.83	0.99	0.94	1.00
$VBN1$	0.99	1.04	0.94	0.99	1.04	0.97	0.92	0.99	0.87
VBP_{CASC}	1.21	1.17	1.16	1.21	1.17	1.16	1.34	1.30	1.29
VBN_{CASC}	0.62	0.67	0.65	0.62	0.67	0.66	0.59	0.64	0.61

5.5.2 Spurious Free Dynamic Range (SFDR)

In this section we show the SFDR performance of the DUT. Having tested the performance limits of the external ADC and the signal source, we are now able to see how well the DUT performs, knowing that the overall system can be limited by the ADC performance. Figure 5.12 below shows the SFDR plot of the DUT. The input is swept from $40mV_{pp}$ to $1.0V_{pp}$ at an input frequency of $481.6Hz$, while adjusting the gain setting so that the output is at least $400mV_{pp}$. The plot shows that the SFDR ranges from approximately $72dB$ to $97dB$.

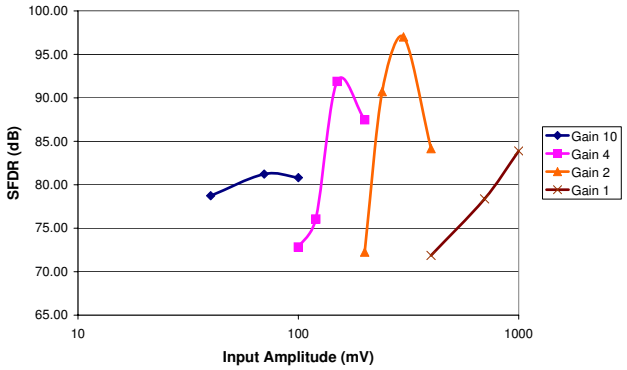
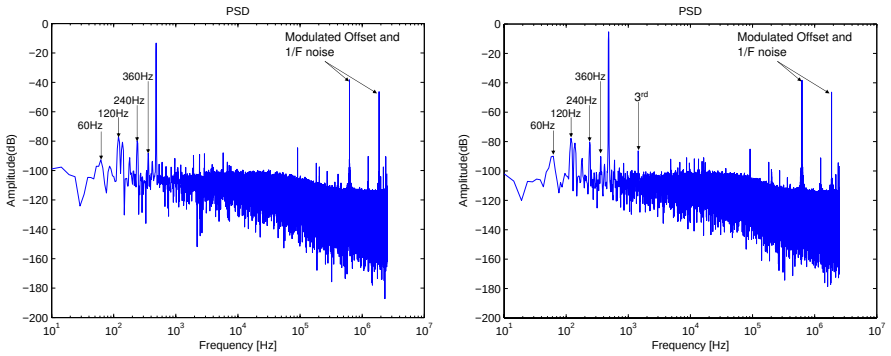


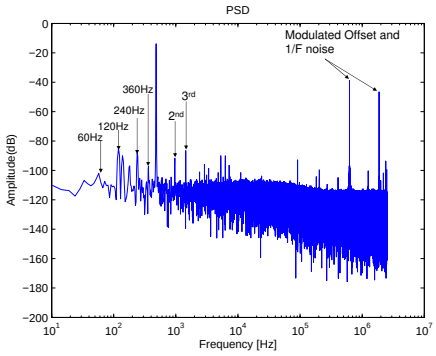
Figure 5.12: SFDR Vs Input Amplitude with different Gain settings

Figures 5.13(a)to 5.13(h) show the power spectral densities of the system output. The $60Hz$ components and its harmonics were ignored in the SFDR calculation. The spurs past the third harmonic were similar to the higher order spurs observed in the ADC output PSD.

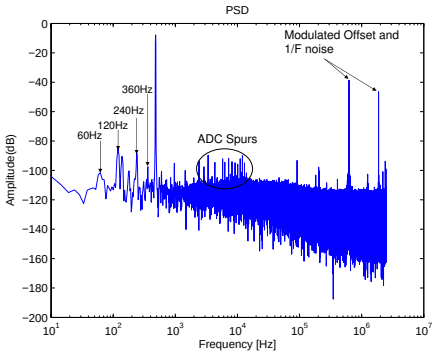


(a) $Input = 40mV_{pp}$, $Gain = 10$

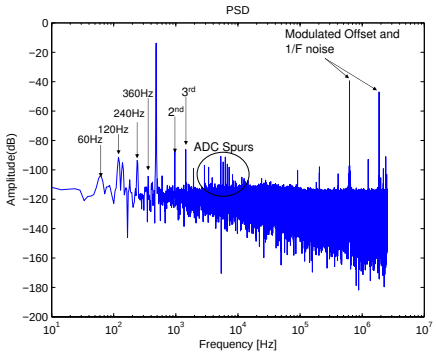
(b) $Input = 100mV_{pp}$, $Gain = 10$



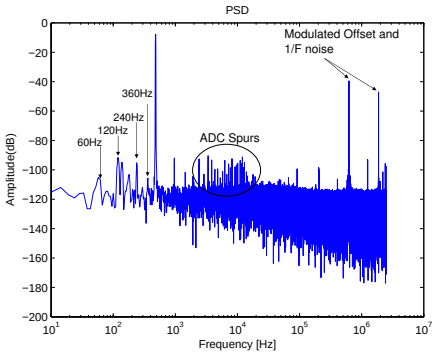
(c) $Input = 100mV_{pp}$, $Gain = 4$



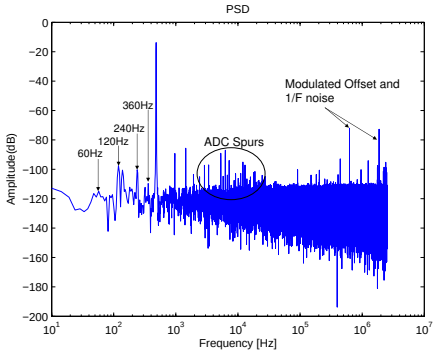
(d) $Input = 200mV_{pp}$, $Gain = 4$



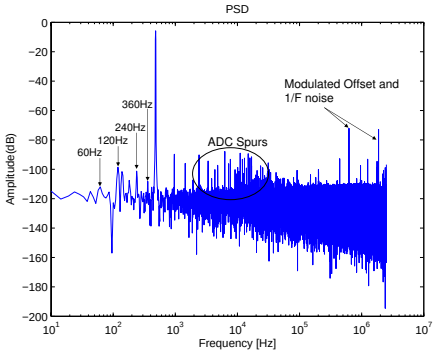
(e) $Input = 200mV_{pp}$, $Gain = 2$



(f) $Input = 400mV_{pp}$, $Gain = 2$



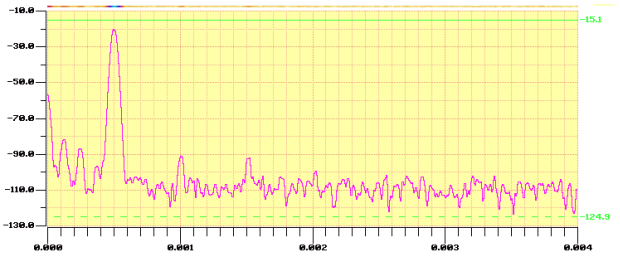
(g) $Input = 400mV_{pp}$, $Gain = 1$



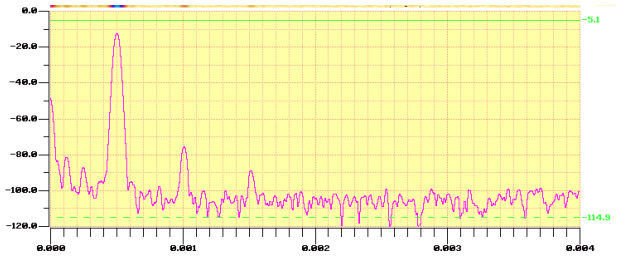
(h) $Input = 1V_{pp}$, $Gain = 1$

Figure 5.13: PSD plots of DUT output with different Input and Gain settings at $F_{in} = 481.6Hz$

In order to ascertain that they did not come from the DUT, the DUT was disconnected from the ADC, and the output was connected to the spectrum analyzer. Figure 5.14 below shows the output spectral densities.



(a) $Input = 40mV_{pp}$, $Gain = 10$



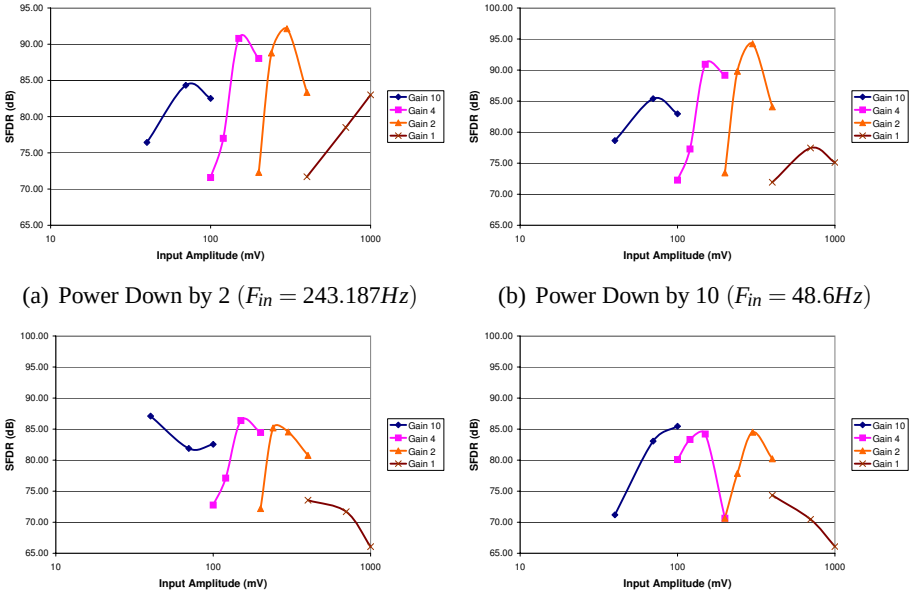
(b) $Input = 100mV_{pp}$, $Gain = 10$

Figure 5.14: Output of DUT through a Spectrum Analyzer

The gain setting of "10" represents the worst case, since the signal goes through the largest number of Opamps. Moreover, with $100mV_{pp}$ input signal swing, the entire circuit experiences its largest dynamic range for this application. In this case we can see that there are no visible harmonics past the third harmonic.

This leads to the conclusion that any harmonics in the previous PSD's are from the ADC and not from the DUT. Hence, any spurs past the third harmonic can be ignored. From the spectra we can see that there is a large second order harmonic component. That is because the spectrum analyzer can only accept single-ended inputs, hence the above spectra are single-ended spectra. The second harmonic is greatly reduced when measured differentially, as is apparent in figures 5.13.

Figures 5.15(a) to 5.15(d) shows the SFDR Vs input amplitude plots with different power down modes (i.e. different input frequencies). As can be seen in the figures, the



(a) Power Down by 2 ($F_{in} = 243.187Hz$)

(b) Power Down by 10 ($F_{in} = 48.6Hz$)

(c) Power Down by 100 ($F_{in} = 4.86Hz$)

(d) Power Down by 1000 ($F_{in} = 0.486Hz$)

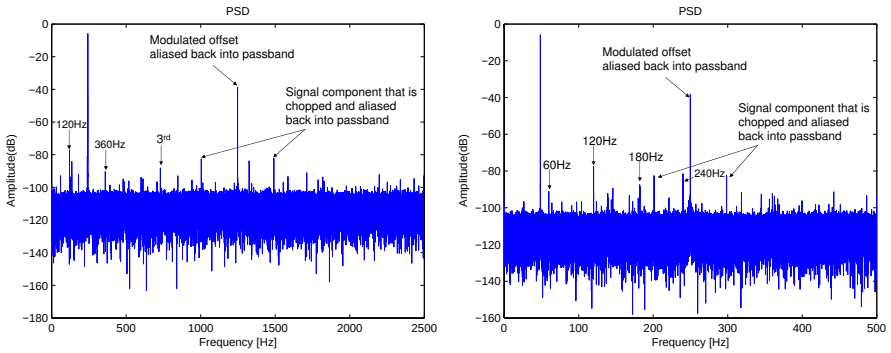
Figure 5.15: SFDR with different power down modes

results are consistent regardless of the power down mode. Moreover, for frequencies below $10Hz$, the linearity of the signal source seems to deteriorate. Figures 5.16(a) to 5.16(d) shows the PSD's with the power down modes. Because there is no filter to remove the modulated offset and $1/F$ noise, they get aliased back in the visible band. In the power down by 100 and 1000 cases, the $60Hz$ harmonics also bet aliased back.

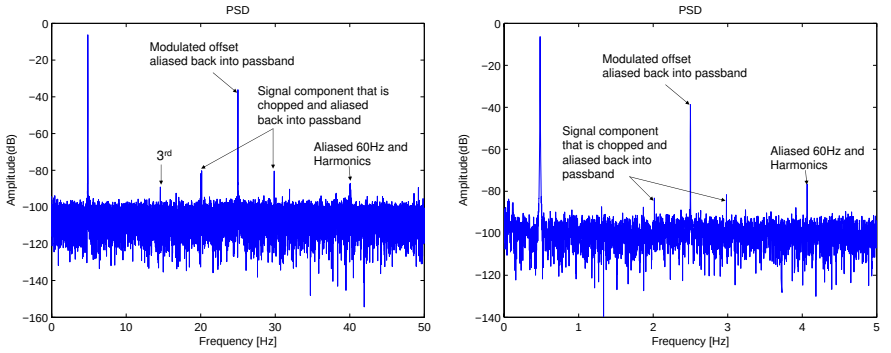
5.5.3 Total Harmonic Distortion (THD)

Figure 5.17 shows the THD Vs input amplitudes with different gain settings. Similar to the SFDR, the THD was calculated by counting only up to the forth order harmonics. In the previous section we have established that any higher order harmonics come from the ADC as opposed to the DUT.

As with the SFDR case, it is worthwhile to see the effect of powering down on the performance of the DUT. Figures 5.18(a) to 5.18(d) show the THD Vs input plots using different power down modes. Once again, powering down causes no significant change in performance.



(a) $Input = 100mV_{pp}$, $Gain = 10$, $PD = 2$, $(F_{in} = 243.187Hz)$ (b) $Input = 100mV_{pp}$, $Gain = 10$, $PD = 10$, $(F_{in} = 48.6Hz)$



(c) $Input = 100mV_{pp}$, $Gain = 10$, $PD = 100$, $(F_{in} = 4.86Hz)$ (d) $Input = 100mV_{pp}$, $Gain = 10$, $PD = 1000$, $(F_{in} = 0.486Hz)$

Figure 5.16: PSD plots of DUT output with different Power Down modes

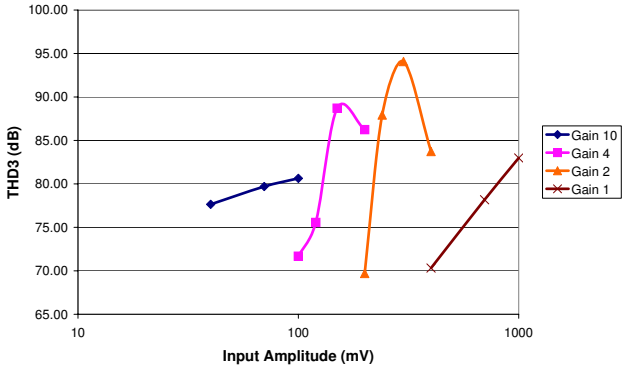
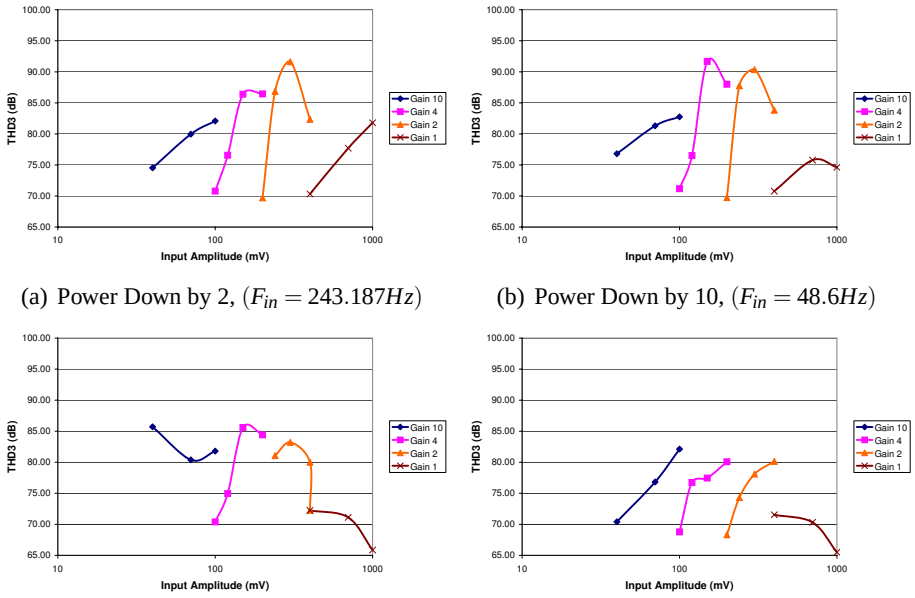


Figure 5.17: THD Vs Input Amplitude with different Gain settings



(a) Power Down by 2, ($F_{in} = 243.187Hz$)

(b) Power Down by 10, ($F_{in} = 48.6Hz$)

(c) Power Down by 100, ($F_{in} = 4.86Hz$)

(d) Power Down by 1000, ($F_{in} = 0.486Hz$)

Figure 5.18: THD with different power down modes

5.5.4 Power Scaling

Now that we have established that the DUT is 13-bits linear on average, even under different power-down modes, it is time to see how well does the amplifier power scale. In this section, we will measure how well the DUT power scales relative to amplitude and bandwidth.

Amplitude Power Scaling

Figure 5.19 shows the PGA power consumption under different gain settings. As can be seen from the plot, the "Gain 4" setting (designed for $100mV_{pp}$ input) consumes approximately 6 times less power than the "Gain 10" setting (designed for $40mV_{pp}$ input). However, we notice that the "Gain 2" setting only consumes around 2.5 times less power than the "Gain 4" setting. As explained in the previous section, this is because the total power does not account for the opamp bias power consumption.

Figure 5.20 shows the amplitude power scaling plots with different power down modes.

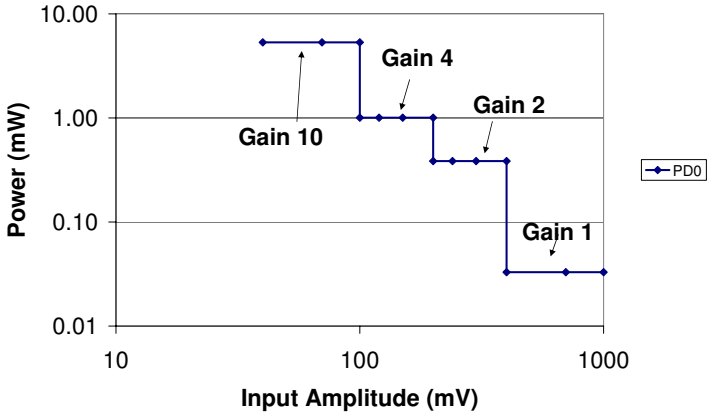


Figure 5.19: Power Vs Input Amplitude, ($F_{in} = 481.6Hz$)

The y-axis is plotted on a log scale to be able to clearly distinguish low power levels. It is apparent that under lower power down modes, the amplitude power scaling does not seem to work that well. That is because the input bias current of $18\mu A$ is not being powered down. That will become more apparent in the next subsection.

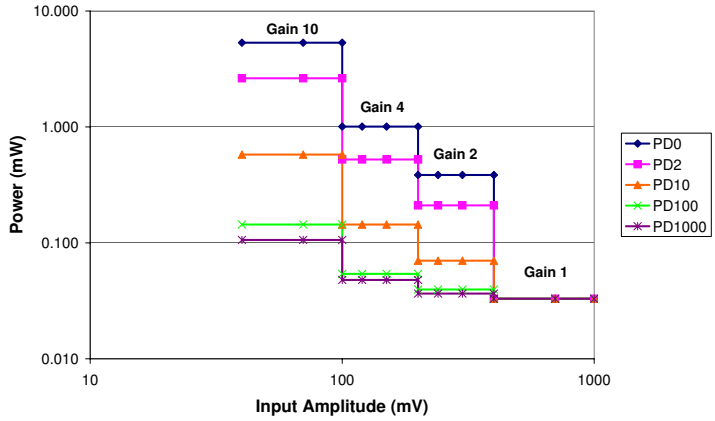


Figure 5.20: Power Vs Input Amplitude with different Power-Down Modes

Frequency Power Scaling

Figure 5.21 shows the power consumption plot vs signal frequency. The different plot lines refer to the different gain settings, and hence the plot shows how the different gain settings'

power scales with frequency. The plot shows a very linear relationship between power consumption and frequency, However, because the x-axis is plotted on a linear scale, it is difficult to ascertain what is going on in the lower frequency range.

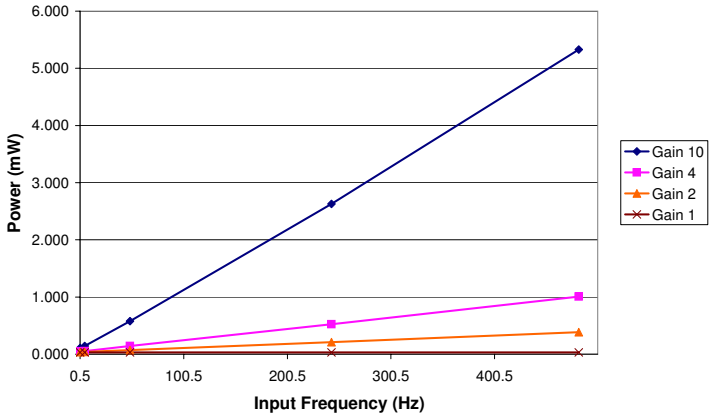


Figure 5.21: Frequency Power Scaling

Figure 5.22 shows the same plot, but with both x and y-axes on a log scale. From this plot, we can see that frequency power scaling works well until the frequency is scaled down to $50Hz$ after which it no longer scales linearly. Moreover, if we look at the $0.5Hz$ power points, we can see as we indicated in the previous subsection that they do not power-scale well with different gain settings. This can be seen easily, as the distance between the different line-plots are not uniform, indicating a difference in power ratios between the $0.5Hz$ case and the $0.5kHz$ case.

In the previous subsection, we mentioned that the degradation in power-scalability can be attributed to the fact that the input bias current is not powered down with the rest of the circuit. Figure 5.23 shows the same frequency power-scaling plot after the constant input bias current has been subtracted from the overall average current consumption.

In this case, the DUT's power seems to scale better with frequency, although it still does not scale perfectly linearly in the $0.5Hz$ case (equivalent to a power down mode of 1000). The "Gain 1" case, all amplifiers have been bypassed, and any power consumption comes from leakages and the logic gain-selection blocks.

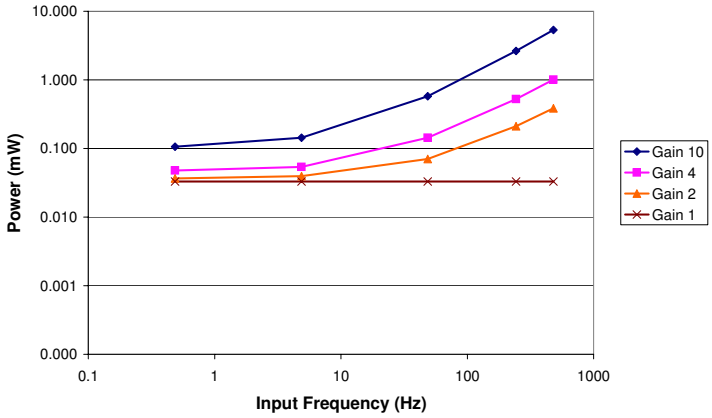


Figure 5.22: Frequency Power Scaling on a LOG scale

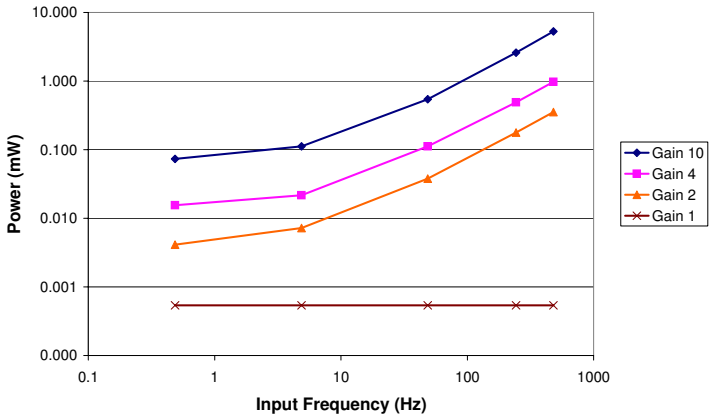
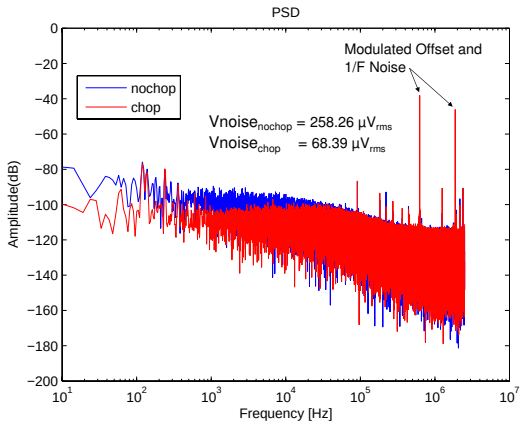


Figure 5.23: Frequency Power Scaling after removing the Ibias

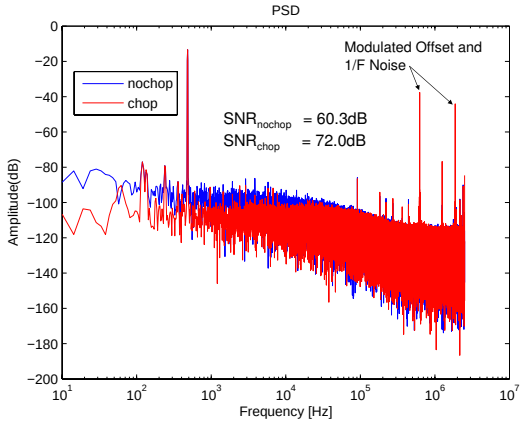
5.5.5 Effects of Chopping

It is important to find out how much impact on performance did chopping have on the DUT. Figure 5.24 shows the output PSD (with and without a signal), for the "Gain 10" setting. From the PSD's, it is apparent that the inband noise reduced 4 times as a result of chopping. That translates into a $12dB$ difference in SNR, or $2-bits$.

There was no accurate means to measure the residual offset of the amplifier, because the test setup was not designed to measure it. This is not significantly important for this test chip, as the goal in this case was to see the effect of chopping on $1/F$ noise, especially in smaller technologies, where $1/F$ noise gets worse. We have shown here that we are capable



(a) No signal



(b) With signal ($40mV$)

Figure 5.24: Effect of Chopping with and without signal, ($F_{in} = 481.6Hz$)

of achieving at least 12-bits noise level with relative to low signal amplitudes ($40mV_{pp}$) in $0.18\mu m$ CMOS technology. From the plots we can also see that the 1/F noise corner frequency is approximately $50kHz$.

5.6 Summary

Table 5.2 shows a comparison between simulated and measured interface power consumption. As was mentioned in chapter 4, due to long simulation times, the power down modes were not simulated, and so an accurate comparison can only be made in the no power down mode case ($500Hz$).

Table 5.2: Simulated Vs Measured Power Consumption

Input Amplitude (mV_{pp})	***Input Bandwidth*** Hz	***Gain Setting***	***Simulated Power Consumption*** (mW)	***Measured Power Consumption*** (mW)
40	500	10	5.278	5.296
101	500	4	0.984	0.974
201	500	2	0.349	0.353
401	500	1	0.001	0.001
40	50	10	N/A	0.545
101	50	4	N/A	0.112
201	50	2	N/A	0.038
401	50	1	N/A	0.001
40	5	10	N/A	0.112
101	5	4	N/A	0.022
201	5	2	N/A	0.007
401	5	1	N/A	0.001
40	0.5	10	N/A	0.074
101	0.5	4	N/A	0.015
201	0.5	2	N/A	0.004
401	0.5	1	N/A	0.001

Tables 5.3 - 5.5 show the results summary for the DUT for different input voltage ranges and gain settings. Overall, the test results show that a sensor interfacing PGA with 13-bit linearity can be designed to be power-scalable in both frequency and amplitude.

Table 5.3: Results Summary for Input = $40mV_{pp}$ - $100mV_{pp}$

Technology	0.18µ*m* CMOS
Power Supply	1.8*V*
ADC Sampling Freq.	5.0*MHz*
Signal Bandwidth Range	$0-0.5Hz$(min), $0-0.5kHz$(max)
Chopping Frequency	625.0*kHz*
Gain Settings	20*dB*
SFDR	72*dB*(min) 95*dB*(max)
THD	70*dB*(min) 90*dB*(max)
Input Referred Noise	$170.0nV/\sqrt{Hz}$
Power Consumption Range	$74.0\mu W-5.30mW$
PGA Area	$0.617mm^2$

Table 5.4: Results Summary for Input = $100mV_{pp}$ - $200mV_{pp}$

Technology	0.18µ*m* CMOS
Power Supply	1.8*V*
ADC Sampling Freq.	5.0*MHz*
Signal Bandwidth Range	$0-0.5Hz$(min), $0-0.5kHz$(max)
Chopping Frequency	625.0*kHz*
Gain Settings	12*dB*
SFDR (Mean)	72*dB*(min) 95*dB*(max)
THD (Mean)	70*dB*(min) 90*dB*(max)
Input Referred Noise	$160.0nV/\sqrt{Hz}$
Power Consumption Range	$15.0\mu W-0.974mW$
PGA Area	$0.617mm^2$

Table 5.5: Results Summary for Input = $200mV_{pp}$ - $400mV_{pp}$

Technology	0.18µ*m* CMOS
Power Supply	1.8*V*
ADC Sampling Freq.	5.0*MHz*
Signal Bandwidth Range	$0-0.5Hz$(min), $0-0.5kHz$(max)
Chopping Frequency	625.0*kHz*
Gain Settings	6*dB*
SFDR (Mean)	72*dB*(min) 95*dB*(max)
THD (Mean)	70*dB*(min) 90*dB*(max)
Input Referred Noise	$220.0nV/\sqrt{Hz}$
Power Consumption Range	$4.0\mu W-0.35mW$
PGA Area	$0.617mm^2$

Chapter 6

Conclusion

IN this dissertation, a technique to improve power scaling efficiency of automotive MEMS pressure sensor interfaces is presented. Power scaling with respect to amplitude is achieved by cascading gain stages through an input gain-select mux, which scales better than previous approaches which utilize either a cascaded gain stage with output gain select, or varying the input and/or feedback impedances in a negative feedback configuration. Power scaling with respect to input bandwidth of the sensor is achieved through periodic power-down of the interface. A prototype of the interface was fabricated in $1.8V$, $0.18\mu m$ CMOS process. Its power consumption scales between $4\mu W - 5.33mW$, while maintaining a Spurious Free Dynamic Range (SFDR) range of approximately $72 - 92dB$, a Total Harmonic Distortion (THD) range of $70 - 90dB$, and an input referred noise of $170.0nV/\sqrt{Hz}$.

6.1 Future Work

As mentioned in the introduction, this work is part of a larger integrated system of MEMS pressure sensors. This work presents a solution to a key challenge in meeting the system expectations. Future work in this field would include:

- One key challenge with this project is that, while the analog power consumption scales down with respect to both frequency, and amplitude, the digital power consumption remains virtually constant, and large compared to the scaled analog power. Therefore, the Power Down FPGA was implemented off-chip. Low power digital

techniques can be utilized to implement an On-chip FPGA, while maintaining the overall power efficiency of the system.

- Integrating a low-power incremental ADC to follow the PGA interface stage. This would provide a complete integrated solution for MEMS pressure sensors or any other resistive-based pressure sensor.
- While this project deals with pressure sensors, the next step would be to implement similar power-scalable topologies with different kinds of sensors that may be capacitive, inductive, mechanical, or otherwise.

This work provides lots of promise in the field of sensor electronics. By reducing cost pressures of producing customized electronics for each sensor application, the sensor industry can look forward to having power efficient, and economical solution to a growing market demand.

Appendix A

Output Noise of a Cascaded Amplifier with Input Gain Select

Figure A.1 shows the noise model of the cascaded gain amplifier with a last stage active RC amplifier. The resistor values are the same as the ones shown in figure 3.17 in chapter 3, which means

$$\begin{aligned} R_1 &= R \\ R_2 &= 2.5R \\ R_3 &= 6R \\ R_4 &= 12R \\ R_5 &= 24R \\ R_6 &= 48R \end{aligned} \tag{A.1}$$

In order to analyze the worst case output noise of this system (Gain setting = 10), we will use superposition to calculated the noise transfer function of each of the noise sources:

$$\frac{V_{out}}{V_{n6}} = \frac{1}{1+R_6Cs} \tag{A.2}$$

$$\frac{V_{out}}{V_{n5}} = -\frac{R_6}{R_5}\frac{1}{1+R_6Cs} \tag{A.3}$$

$$\frac{V_{out}}{V_{n4}} = -\frac{R_6}{R_5}\frac{1}{1+R_6Cs} \tag{A.4}$$

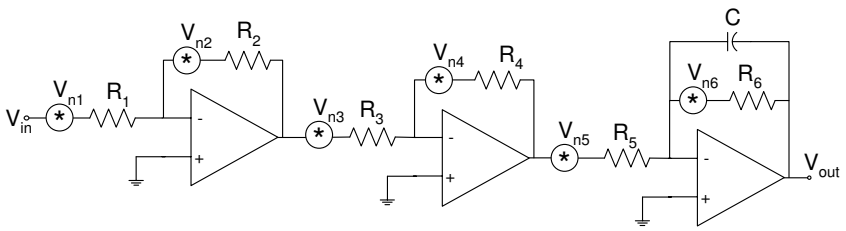


Figure A.1: Noise Model of Cascaded Gain Stage with Final Active RC Stage

$$\frac{V_{out}}{V_{n3}} = \frac{R_4}{R_3} \cdot \frac{R_6}{R_5} \frac{1}{1+R_6Cs} \tag{A.5}$$

$$\frac{V_{out}}{V_{n3}} = \frac{R_4}{R_3} \cdot \frac{R_6}{R_5} \frac{1}{1+R_6Cs} \tag{A.6}$$

$$\frac{V_{out}}{V_{n1}} = -\frac{R_2}{R_1} \cdot \frac{R_4}{R_3} \cdot \frac{R_6}{R_5} \frac{1}{1+R_6Cs} \tag{A.7}$$

$$\tag{A.8}$$

Using those transfer functions to calculate the noise yields:

$$V_{out,n}^2 = 4KTR_6 \frac{1}{4R_6C} + 4KTR_5 \left(\frac{R_6}{R_5}\right)^2 \frac{1}{4R_6C} + 4KTR_4 \left(\frac{R_6}{R_5}\right)^2 \frac{1}{4R_6C} + 4KTR_3 \left(\frac{R_4R_6}{R_3R_5}\right)^2 \frac{1}{4R_6C} + 4KTR_2 \left(\frac{R_4R_6}{R_3R_5}\right)^2 \frac{1}{4R_6C} + 4KTR_1 \left(\frac{R_2R_4R_6}{R_1R_3R_5}\right)^2 \frac{1}{4R_6C} \tag{A.9}$$

Which is dependant on the ration of the resistors. Substituting all the resistor values in equation A.1 into equation A.9 yields

$$V_{out,n}^2 \approx \frac{10KT}{C} \tag{A.10}$$

References

[1] M. Metz, "Trends in automotive sensors," BOSCH Research and Technology Center, Tech. Rep., 2005.

[2] K.-F. Reinhart and M. Illing, *Sensors for Automotive Technology*. Wiley-VCH, 2003, ch. 2, pp. 5–21.

[3] G. Lammel, S. Armbruster, C. Schelling, and H. Benzel, "Next generation pressure sensors in surface micromachining technology," BOSCH Research and Technology Center, Tech. Rep., 2005.

[4] C. Lang and J. Vanderhaegen, "Kickoff meeting: Scalable ADC," Bosch RTC, Tech. Rep., 2006.

[5] I. Yokomori and Y. Suzuki, *Sensors for Automotive Technology*. Wiley-VCH, 2003, ch. 7, pp. 314–342.

[6] R. Henn, T. Honma, and S. Finkbeiner, *Sensors for Automotive Technology*. Wiley-VCH, 2003, ch. 5, pp. 123–158.

[7] R. Johnson and R. Johnson, "High temperature silicon-on-insulator pressure sensor technology," in *Proc. Third European Conference on High Temperature Electronics HITEN 99*, 1999, pp. 45–48.

[8] R. Singh, L. L. Ngo, H. S. Seng, and F. Mok, "A silicon piezoresistive pressure sensor," in *Proc. First IEEE International Workshop on Electronic Design, Test and Applications*, 29–31 Jan. 2002, pp. 181–184.

[9] S. Ekelof and S. Ekelof, "The genesis of the wheatstone bridge," *Engineering Science and Education Journal*, vol. 10, no. 1, pp. 37–40, 2001.

[10] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, C. Robey, Ed. John Wiley & Sons, Inc., 1997.

[11] B. Rezavi, *Design of Analog CMOS integrated Circuits*. McGraw-Hill International Edition, 2001.

[12] C. Enz and G. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization,", *Proceedings of IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[13] J. H. Anton Bakker, "High-accuracy CMOS smart temperature sensors," Ph.D. dissertation, Delft University of Technology, 2000.

[14] A. Bakker and J. Huijsing, "A CMOS chopper opamp with integrated low-pass filter," in *Proc. 23rd European Solid-State Circuits Conference ESSCIRC '97*, 16–18 Sept. 1997, pp. 200–203.

[15] A. Bakker and J. Huijsing, "Offset reduction in current-mode microsystems," in *Proc. IEEE International Symposium on Circuits and Systems ISCAS '96., 'Connecting the World'*, vol. 4, 12–15 May 1996, pp. 344–347.

[16] D. McCartney, A. Sherry, J. O'Dowd, and P. Hickey, "A low-noise low-drift transducer ADC," *IEEE Journal of Solid State Circuits*, vol. 32, no. 7, pp. 959–967, 1997.

[17] A. Bakker, K. Thiele, and J. Huijsing, "A CMOS nested-chopper instrumentation amplifier with 100-nV offset," *IEEE Journal of Solid State Circuits*, vol. 35, no. 12, pp. 1877–1883, Dec. 2000.

[18] C. Menolfi and Q. Huang, "A low-noise CMOS instrumentation amplifier for thermoelectric infrared detectors," *IEEE Journal of Solid State Circuits*, vol. 32, no. 7, pp. 968–976, July 1997.

[19] J. F. Witte, J. F. Witte, K. A. Makinwa, and J. H. Huijsing, "A CMOS chopper offset-stabilized opamp," in *Proc. 32nd European Solid-State Circuits Conference ESSCIRC 2006*, K. A. Makinwa, Ed., 2006, pp. 360–363.

[20] M. Sanduleanu, A. Van Tuijl, R. Wassenaar, M. Lammers, and H. Wallinga, "A low noise, low residual offset, chopped amplifier for mixed level applications," in *Proc. IEEE International Conference on Electronics, Circuits and Systems*, vol. 2, 7–10 Sept. 1998, pp. 333–336.

[21] Y. Christoforou, "A chopper-based CMOS current sense instrumentation amplifier," in *Proc. 19th IEEE IMTC/2002 Instrumentation and Measurement Technology Conference*, vol. 1, 21–23 May 2002, pp. 271–273.

[22] R. Schreier and G. Temes, *Understanding Delta-Sigma Data Converters*, S. Kartalopoulos, M. Akay, J. Anderson, R. Baker, and J. E. Brewer, Eds. John Wiley & Sons, Inc., 2005.

[23] J. Robert and P. Deval, "A second-order high-resolution incremental A/D converter with offset and charge injection compensation," *IEEE Journal of Solid State Circuits*, vol. 23, no. 3, pp. 736–741, June 1988.

[24] J. Markus, J. Silva, and G. Temes, "Theory and applications of incremental $\Delta - \Sigma$ converters," *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, vol. 51, no. 4, pp. 678–690, April 2004.

[25] T. Caldwell and D. Johns, "An incremental data converter with an oversampling ratio of 3," in *Proc. Ph Research in Microelectronics and Electronics 2006 D*, 12–15 June 2006, pp. 125–128.

[26] B. Woo, "Digitally programmable gain amplifiers with arbitary range of integer values," *Proceedings of the IEEE*, vol. 68, no. 7, pp. 934–936, July 1980.

[27] S. C. D. Roy, "Digitally programmable gain amplifiers," *IEEE Transactions on Instrumentation and Measurement*, vol. 33, no. 4, pp. 329–332, Dec. 1984.

[28] G. Xu, G. Xu, and H. Bilhan, "A programmable gain amplifier buffer design for video applications," in *Proc. International Symposium on Circuits and Systems ISCAS '04*, H. Bilhan, Ed., vol. 1, 2004, pp. I–557–60 Vol.1.

[29] F. Gebara, S. Martin, E. Marsman, K. Kraver, and R. Brown, "900mV programmable gain amplifier for cochlear implants," in *Proc. IEEE International Workshop on Biomedical Circuits and Systems*, 1–3 Dec. 2004, pp. S1/3/INV–S1/3/1–4.

[30] G. O'Donoghue, M. Mallinson, and P. Holloway, "A novel programmable gain amplifier," in *Proc. Third Annual IEEE ASIC Seminar and Exhibit*, 17–21 Sept. 1990, pp. P8/6.1–P8/6.4.

[31] M. Sanz, M. Sanz, S. Celma, and B. Calvo, "Approach to high-linear programmable gain amplifiers," in *Proc. 47th Midwest Symposium on Circuits and Systems MWSCAS '04*, S. Celma, Ed., vol. 1, 2004, pp. I–157–60 vol.1.

[32] S. Spiridon and F. Op't Eynde, "Low power CMOS fully differential variable-gain amplifier," in *Proc. International Semiconductor Conference CAS 2005*, vol. 2, 3–5 Oct. 2005, pp. 383–386.

[33] P. Furth and H. Om'mani, "A 500-nW floating-gate amplifier with programmable gain," in *Proc. Midwest Symposium on Circuits and Systems*, 9–12 Aug. 1998, pp. 134–137.

[34] C. Motchenbacher and J. Connelly, *Low-Noise Electronic System Design*, A. Gasiewski, E. Kennedy, and E. Chenette, Eds. John Wiley & Sons, Inc., 1993.

[35] I. Ahmed, "A power scaleable and low power pipeline ADC using power resettable opamps," Master's thesis, University of Toronto, 2004.

[36] I. Ahmed and D. Johns, "A 50 MS/s (35 mW) to 1 kS/s (15 μ W) power scaleable 10b pipelined ADC with minimal bias current variation," in *Proc. Digest of Technical*

Papers Solid-State Circuits Conference ISSCC. 2005 IEEE International, 6–10 Feb. 2005, pp. 280–598.

[37] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio $\Delta - \Sigma$; modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE Journal of Solid State Circuits*, vol. 36, no. 3, pp. 349–355, March 2001.

[38] M. Dessouky and A. Kaiser, "Very low-voltage fully differential amplifier for switched-capacitor applications," in *Proc. ISCAS 2000 Geneva Circuits and Systems The 2000 IEEE International Symposium on*, vol. 5, 28–31 May 2000, pp. 441–444.

[39] A. Sedra and K. Smith, *Microelectronic Circuits, Fifth Edition*, A. Sedra, Ed. Oxford University Press, 2004.