A Frequency-Scalable 14-bit ADC for Low Power Sensor Applications

by

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Abstract

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In this thesis, a 14-bit low-power Analog-to-Digital Converter (ADC) is designed for sensor applications. Following on previous work, the ADC is designed to be frequency scalable by 1000 times from 1.67S/s to 1.67kS/s. To reduce power, class AB opamps are used. The design was fabricated in $0.18\mu m$ CMOS and occupies an area of $0.35mm^2$. Operating at full-rate as a Delta-Sigma modulator, the ADC achieves 91.8dB peak SNDR while consuming $83\mu W$. In incremental mode, the ADC powers off periodically to achieve frequency scalability, maintaining 84.7dB to 89dB peak SNDR while operating from 1.67S/s to 1.67kS/s.

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Contents

List of Tables

List of Figures

List of Abbreviations

α	"Relative Increase in Opamp Noise" (*See section A.1.2 of Appendix*)
βf_t	Closed-Loop Unity Gain Bandwidth
ω_t	Unity Gain Bandwidth (in Radians)
τ	Time Constant of First-Order System
ADC	Analog-to-Digital Converter
C	Capacitance
CIFB	Cascade of Integrators Feedback
CMFB	Common Mode Feedback
CRFB	Cascade of Resonator Feedback
DR	Dynamic Range
DUT	Device Under Test
ENOB	Effective Number of Bits
f	Frequency
ft	Unit Gain Bandwidth
Gm	Transconductance
K	Boltzmann's Constant

MEMS	Microelectromechanical System
NBW	Noise Bandwidth (*See section 3.3.1*)
NTF	Noise Transfer Function
OSR	Oversampling Ratio
PGA	Programmable Gain Amplifier
R	Resistance
RMS	Root Mean Square
SFDR	Spurious Free Dynamic Range
SNDR	Signal to Noise-plus-Distortion Ratio
SNR	Signal to Noise Ratio
SQNR	Signal to Quantization Noise Ratio
STF	Signal Transfer Function
T	Temperature (in Kelvin)
THD	Total Harmonic Distortion
V_{eff}	Mosfet Overdrive Voltage = (Gate-Source Voltage)-Vt
Vt	Threshold Voltage

Chapter 1

Introduction

In the past decade, Microelectromechanical Systems or MEMS have increasingly been applied to a wide range of sensor applications. Using tiny mechanical structures, MEMS technology can form the basis of pressure sensors, accelerometers and gyroscopes, among others. The benefit of MEMS devices is that they can be manufactured using existing Integrated Circuit technologies such as CMOS. As a result, they can be easily integrated with modern microelectronics, leading to compact, highly integrated solutions. This makes them particularly attractive where high volume and low cost are desired, including the automotive and consumer electronics industries.

MEMS sensor devices must typically interface with digital electronics. Applied in automobiles for example, tire pressure sensors might be monitored by on-board computers to warn drivers of deflating tires and prevent possible accidents. The interface between MEMS devices and the digital domain is therefore crucial. Configured in electronic circuits, MEMS sensors can provide outputs as highly sensitive electrical signals. These analog electrical signals must then be converted to digital for use by other systems such as micro-controllers or transmitters. This thesis continues on the work of Akram Nafee [1] in designing a sensor interface consisting of a gain stage and an Analog-to-Digital Converter or ADC.

The development of a 14-bit accurate sensor interface including ADC, that could be scaled in power based on varying signal amplitudes (40-400mV peak-to-peak differential) and bandwidths

(0.5Hz-0.5kHz) was proposed in [1]. As a result, a single interface could be used for a variety of sensor types, reducing development costs. Power-scaling also has other potential uses where a signal's dynamic range and bandwidth might vary. To accomplish amplitude-based power scaling, in [1], a programmable gain stage was designed, fabricated and tested. A method for frequency-scaling an oversampled ADC was also elaborated. In this work, the remaining task of designing a high-resolution, frequency-scalable Analog-to-Digital Converter is carried out. An Incremental converter topology is used. In order to be compatible with MEMS technology, the complete interface is implemented in $0.18\mu m$ CMOS technology.

1.1 Thesis Overview

In Chapter 2, the concept of the sensor interface is described. Next, some background on Delta-Sigma and Incremental data converters is presented. Chapter 3 describes the system-level design of the Incremental ADC produced in this work. Chapter 4 begins with the circuit implementation of the ADC at the block level. The remainder of the chapter discusses reducing the power of the operational amplifiers (opamps) which largely dictate the power consumption of the ADC. In Chapter 5, the complete circuit implementation of the ADC is described at the transistor level. Finally in Chapter 6, the experimental results of the fabricated circuit are presented.

Chapter 2

Introduction and Background

This chapter begins by introducing the MEMS sensor interface which performs Analog-to-Digital conversion on the sensor's output. In [1], the overall system concept was elaborated and an input gain stage was designed. Section 2.1 summarizes this previous work. To complete the interface, a 14-bit accurate Incremental Analog-to-Digital Converter (ADC) must be designed, which is the subject of this work. Design decisions made in [1] dictate some of the specifications of the Analog-to-Digital Converter. These specifications are summarized in section 2.2.4. Starting with section 2.3, the remainder of the chapter provides background on Delta-Sigma data converters, of which Incremental converters are a subset. Initial estimates of the required order of Incremental converter and oversampling ratio (OSR) are also made.

2.1 Sensor Interface

The sensor interface is designed to be driven by a class of Microelectromechanical System (MEMS) pressure sensors employing micro-machined structures to achieve a piezoelectric, or pressure-sensitive electrical effect. In particular, the class of sensors under consideration have a piezoresistive property meaning that their resistance varies with changes in pressure. Various circuits can be used to to translate these changes in resistance into electrical signals. In this case, a Wheatstone bridge is used to drive the sensor interface. From Figure 2.1, one can see that for example, if the resistance of R3 and R2 increase with pressure, it will lead to a positive

change in output voltage.

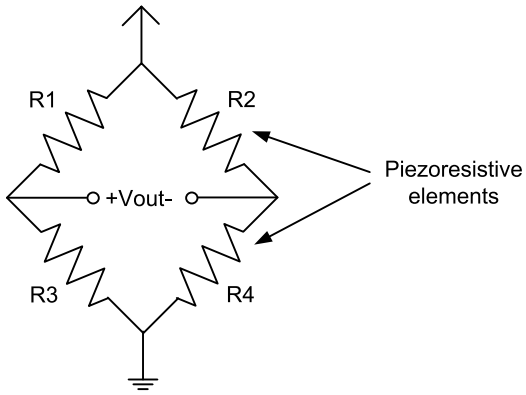


Figure 2.1: Wheatstone Bridge

The specified equivalent resistance of the sensor is 2.5kΩ per side [1], and the sensor interface must have sufficiently high input impedance to avoid loading the Wheatstone bridge.

2.1.1 Amplitude-Based Power-Scaling

The accuracy of the sensor interface is determined by its Signal-to-Noise Ratio (SNR). Therefore, as input signal amplitudes decrease, lower noise levels are needed to maintain the desired accuracy. In power-efficient designs, the noise limitation comes from thermal noise. Since achieving lower thermal noise requires more power, the interface is designed to use only as much power as is required for a given input level. The specifications call for input signal swings ranging from 40mV to 400mV peak-to-peak differential, corresponding to a 100 times change in signal power. The interface should therefore scale its power consumption by the same factor.

To achieve power scaling, in [1], a Programmable-Gain Amplifier (PGA) was designed to provide a gain of 1, 2, 4 or 10 and provide a minimum output level of 400mV peak-to-peak differential while maintaining more than 14-bits equivalent SNR at its output. The PGA uses the inverting amplifier configuration using resistors. The resistors were sized to maintain a relatively high amplifier input impedance of 10kΩ. The amplifier is shown in Figure 2.3. By adjusting its gain, the PGA can scale its power by 100 times based on the input amplitude while maintaining the same SNR. The ADC following the PGA can therefore be designed to

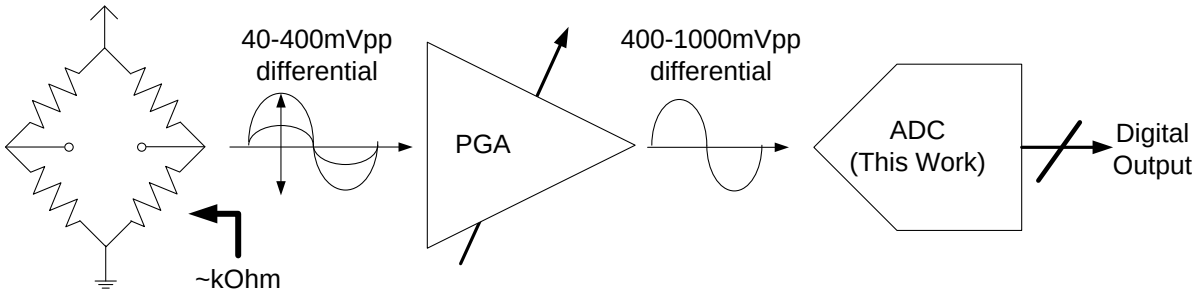


Figure 2.2: Overall Sensor Interface

deal with a fixed minimum input level of 400mV peak-to-peak differential, which requires much less power. Consequently, the PGA dominates power consumption, and its power scaling effect extends to the overall interface.

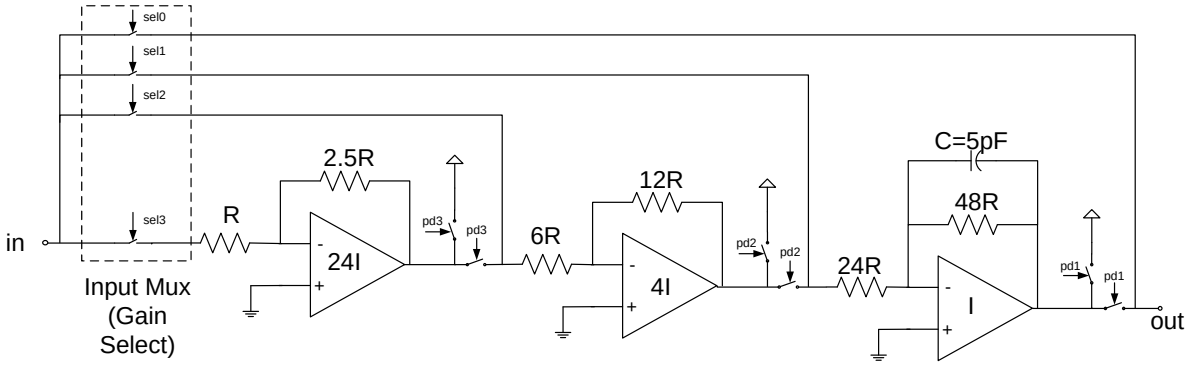


Figure 2.3: PGA Designed in [1]

(R=10kΩ)

Alternative Topology

The alternative to using a PGA for power-scaling is to design a power-scalable ADC. A straightforward implementation would consist of a number of parallel ADC circuits, each having the same noise level, which could be tied together. Since individual ADCs are assumed to have uncorrelated noise, combining 2 parallel ADCs increases SNR by 3dB or 2 times. With lower input amplitudes, more parallel ADCs would be used. Therefore for a 100 times change in

Table 2.1: PGA Specifications [2]

THD	70-90dB
SFDR	72-92dB
Power (Operating at Full-Rate)	
Gain=2	0.35mW
Gain=4	0.9mW
Gain=10	5.3mW

input signal power, 100 parallel ADCs would be required.

This would however, likely require significantly more area, and possibly more power than using an input gain stage. An intermediate solution might combine a lower-gain PGA with an ADC power scalable over a smaller range of 10 for example.

2.1.2 Frequency-Based Power-Scaling

The interface is also designed to deal with sensors and or signals having bandwidths varying from 0.5kHz to 0.5Hz, or 1000 times. For power efficiency, the interface should reduce its sampling rate when possible, therefore reducing its power consumption. Scaling the power and bandwidth of analog circuits by 1000 times can be quite difficult. For example, by varying the bias current of circuits, their power consumption can be scaled. However, it is not easy to maintain correct circuit operation over a wide range of bias conditions. [6] contains a frequency scalable pipeline ADC which uses a form of pulse-width modulation to vary the effective bias current of circuits. The alternative, also discussed in [6] and ultimately chosen in [1] is to always operate the circuits with the same bandwidth and sample rate, and power-down circuits between samples. In this way, analog circuits always operate at a consistent operating point.

For the remainder of this dissertation, the following terminology will be used to describe power scaling:

$$\text{Effective Sample Frequency} = \frac{\text{Nominal Sample Frequency}}{\text{Power Down Ratio}} \tag{2.1}$$

2.2 ADC Architecture Selection

The accuracy of an ADC can be quantified using its SNR, or in terms of bits. The "Effective Number of Bits" (ENOB) of an ADC is given by equation 2.2 below, assuming a sinusoidal input signal. Using this relation, the ADC to be designed requires an SNR of 86dB to achieve 14-bit accuracy. The design of Analog-to-Digital Converters is a vast area of research and industrial design. A large variety of topologies exist but fall into two general categories [7]: Nyquist-Rate and Oversampled ADCs.

$$\text{ENOB} = \frac{SNR_{dB} - 1.76dB}{6.02} \tag{2.2}$$

2.2.1 Nyquist-Rate Converters

Nyquist-Rate converters, as per their name, sample the input at the Nyquist rate. Some examples are Flash, Pipeline and Successive-Approximation (SAR) ADCs. Each topology has its pros and cons and attainable range of specifications, namely resolution and bandwidth. The 14-bit resolution required in this design is not easily attainable with Nyquist-Rate converters.

Flash ADCs simply use as many comparators as there are quantizer levels and are popular in high-speed applications. For 14-bit resolution, this requires 2^{14}-1=16383 comparators! This number can be reduced using folding and interpolating, but the number of comparators is still huge. In addition, individual comparator offsets tend to limit Flash ADCs to relatively low resolution. Pipeline ADCs use a cascade of ADC and amplifier stages to extract bits over several "pipelined" stages. They are capable of medium to high resolution but would likely require calibration to achieve 14-bit accuracy as in [8]. Successive-Approximation ADCs use capacitors and switches in a sequence of charge redistribution steps to extract each bit. They also have difficulty achieving higher resolutions without calibration, due to non-idealities caused by switching.

2.2.2 Oversampled ADCs

Oversampled ADCs sample signals at a multiple of the Nyquist frequency, and exploit this to achieve high resolution. The multiple is called the Oversampling Ratio or OSR (see below). The advantage of oversampling is that since the sample rate is higher than the Nyquist bandwidth, the output can be low-pass filtered, to extract the band of interest. In a basic sampled system (including any ADC using a Sample-and-Hold), all thermal noise aliases in band, leading to a uniform noise floor from DC to the sampling frequency. Therefore the low-pass filtering operation effectively divides the total RMS noise of the ADC by the OSR, assuming ideal brick-wall low-pass filtering is used. Therefore bandwidth can be traded off to achieve lower noise.

$$\text{OSR} = \frac{\text{Sampling Frequency}}{\text{Nyquist Frequency}} \tag{2.3}$$

For a simple RC circuit the RMS squared noise voltage due to thermal noise is given by KT/C [7], where K is the Boltzmann constant and T is the temperature in Kelvin. Since oversampling and filtering reduces this noise, in a sampled circuit employing capacitors, the sampling capacitance C required for a given thermal noise level can be reduced by the OSR [9]. The effect is crucial for this design.

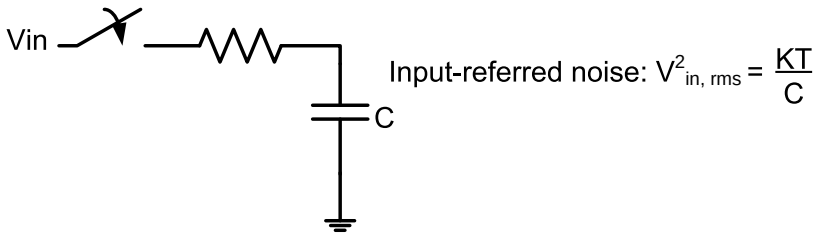


Figure 2.4: Basic Sampled RC Circuit

Using the above, for the given input level of 400mVpp and required SNR of 86dB without oversampling:

$$V_{N,rms}^2 = \frac{1}{2} \cdot \left(\frac{V_{pk-pk}}{2}\right)^2 \cdot 10^{\frac{-SNR}{10}} \tag{2.4}$$

$$\frac{KT}{C_{sample}} = \frac{1}{2} \cdot \left(\frac{400mV}{2}\right)^2 \cdot 10^{\frac{-90}{10}} \tag{2.5}$$

$$C_{sample} = \frac{(1.38x10^{-23})(300K)}{\frac{1}{2}\cdot\left(\frac{400mV}{2}\right)^2\cdot 10^{\frac{-90}{10}}} \quad (2.6)$$

$$C_{sample} = 207pF \quad (2.7)$$

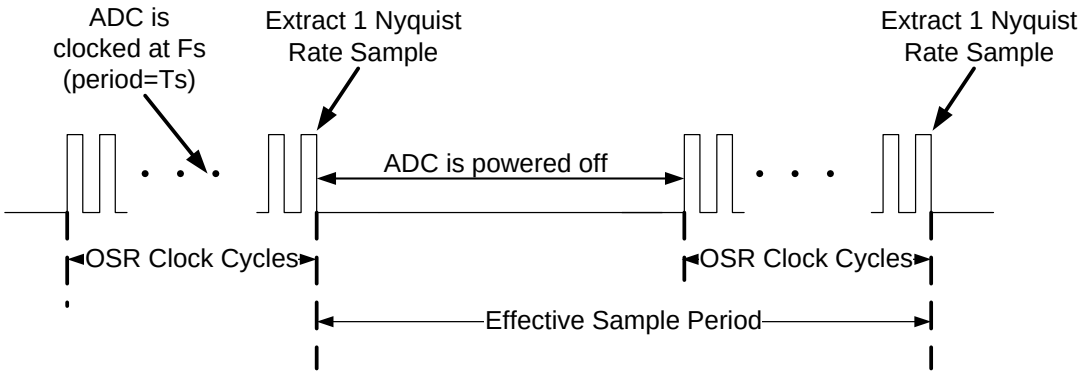
So a simple sample-and-hold circuit would require a capacitor size of 207pF which is quite large for integration in CMOS and would require significant area. Oversampling can reduce this significantly. (This also demonstrates the need for a gain stage in the sensor interface. Without a gain stage, at the minimum input level of 40mVpp, massive 20nF capacitors would be required without oversampling!)

2.2.3 Powering-Scaling Oversampled ADC: Incremental ADC

As discussed section 2.1.2 above, it was decided that the analog ADC circuits would be powered down between conversion steps in order to scale with frequency. This however, is problematic with the most common oversampled ADC architecture, the Delta-Sigma ADC (also called Delta-Sigma modulator). As will be seen later, Delta-Sigma modulators rely on integrator circuits which accumulate charge in capacitors. In order to power down circuits between samples, these integrator circuits would have to maintain their charge while circuits are shut down. Due to leakage, and startup problems with the required opamps, this is impractical. In [1], it was therefore decided to use a subset of Delta-Sigma modulators, the Incremental ADC. As will be discussed, Incremental ADCs use OSR back-to-back conversion steps to produce each output, but can then be reset. They are therefore suitable for power-scaled operation. The concept is shown in Figure 2.5.

2.2.4 ADC Specifications from [1]

Based on the above, and preliminary calculations, some specifications for the interface and ADC were decided in [1] and listed in Table 2.2. The maximum ADC input capacitance was determined by the PGA's last stage amplifier. It was designed assuming a 500fF output load. Due to its two-stage, Miller-compensated topology, excessive ADC input capacitance would reduce the PGA's phase margin and possibly cause instability.



$$\text{Effective Sample Rate } = \frac{\text{Clock Frequency}}{OSR \times \text{Power Down Ratio}} \tag{2.8}$$

Figure 2.5: Power-Scaled Operation of Oversampled Incremental Converter

Power Supply

In addition, it was decided that to achieve high linearity, a standard 1.8V supply would be used for the PGA implemented in 0.18μm CMOS technology. Although many low-power ADCs employ reduced supply voltages to reduce power consumption, low power supplies complicate circuit design, requiring for example, clock-boosting to increase the effective clock voltage. Due to these reasons, and the fact that dual supplies would be undesirable in a fully-integrated solution, it was decided that the same 1.8V supply would also be used for the ADC.

2.3 Introduction to Delta-Sigma Modulators

Although the chosen ADC architecture is that of an Incremental converter, one must first understand the basics of Delta-Sigma modulators of which Incremental converters are a subset.

Table 2.2: Interface and ADC Specifications

Clock Rate	5MHz
PGA Chopper Clock Rate	625kHz
Maxmimum ADC Input Capacitance	500fF

The most basic Delta-Sigma modulator is a First-Order Delta-Sigma Modulator shown in Figure 2.6.

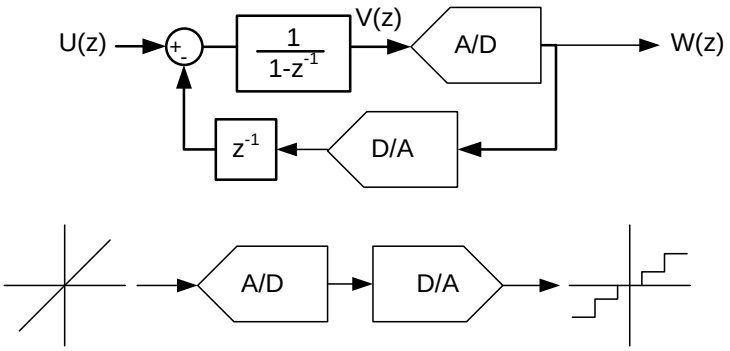


Figure 2.6: First-Order Delta-Sigma Modulator

The modulator can be more easily understood by modeling the A/D or Quantizer as simply adding "quantization error" E(z) to its input, as shown in Figure 2.7. Quantization noise has a broad-band spectrum, and may be approximated as white noise [7].

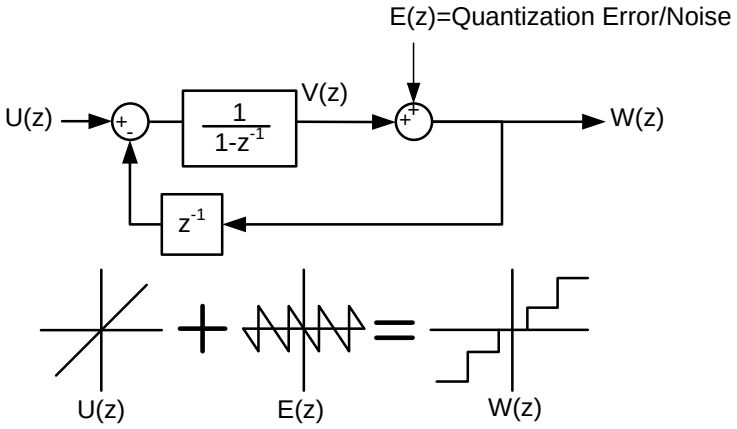


Figure 2.7: Alternate Representation First-Order Delta-Sigma Modulator

From Figure 2.7, one can calculate the transfer function of the modulator as:

$$W(z) = U(z) + (1 - z^{-1})E(z) \tag{2.9}$$

So the First-Order Delta-Sigma modulator outputs the desired input signal, but filters the quantization error E(z) by the transfer function $(1 - z^{-1})$ which has a zero at DC. The quan-

tization noise near DC is therefore heavily suppressed, which is useful assuming that the input frequency is small. By low-pass filtering the modulator output, the quantization noise is largely removed, while retaining input signal content near DC.

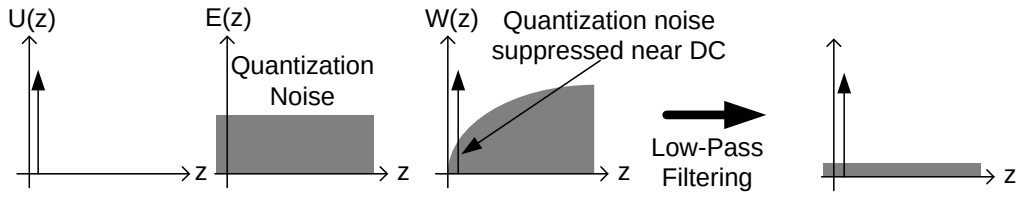


Figure 2.8: Quantization Noise-Shaping Effect of Delta-Sigma Modulator

2.3.1 General Delta-Sigma Modulator

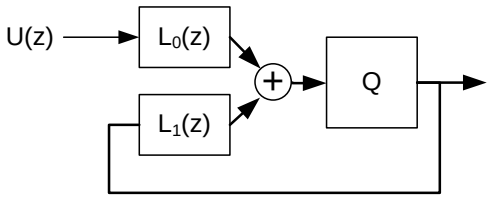
In general, Delta-Sigma modulators are defined by their Signal and Noise Transfer functions or STF and NTF. NTFs are designed to suppress quantization noise in the signal band. The STF on the other hand, is typically chosen to be flat, at least in the band of interest (although other transfer characteristics might be desired).

$$\text{General Delta-Sigma Output: } W(z) = STF(z) \cdot U(z) + NTF(z) \cdot E(z) \tag{2.10}$$

The first order Delta-Sigma modulator shown in Figure 2.6 has an STF equal to unity, and an NTF of $(1 - z^{-1})$. A second order modulator has the same STF but uses two stages of integrators to achieve an NTF equal to $(1 - z^{-1})^2$. A second order modulator therefore has improved noise suppression by imposing two zeros at DC. A general N-th order (low-pass) Delta-Sigma modulator has an NTF given by:

$$\text{For N-th Order Delta-Sigma: } NTF(z) = (1 - z^{-1})^N \tag{2.11}$$

Figure 2.9 shows a general implementation of a single-loop Delta-Sigma modulator. One can see that the NTF is defined by the feedback transfer function $L_1(z)$. Having chosen the appropriate $L_1(z)$ to achieve the desired noise-shaping, $L_0(z)$ can be selected to maintain the required STF.



$$NTF(z) = \frac{1}{1 - L_1(z)} \ , \ STF(z) = \frac{L_0(z)}{1 - L_1(z)} \tag{2.12}$$

Figure 2.9: General Delta-Sigma Modulator

2.4 Incremental A/D Converter

Although initially proposed as a unique architecture of A/D converter in [10], the concept has been further elaborated and generalized [11],[12] as a simple extension of traditional Delta-Sigma modulators.

Due to oversampling, the data rate emerging from Delta-Sigma converters is at Fs, which is 2×OSR times higher than the actual signal bandwidth. This far exceeds the Nyquist criterion for sampling, which requires a much smaller data/sample rate of $F_{Nyquist} = 2 \cdot F_{signal}$ where F_{signal} is the bandwidth of the signal of interest. Therefore, included in the post-filtering process, may be down-sampling to lower the data rate closer to the Nyquist frequency. [3] describes a two-step process, with two stages of filtering and down-sampling to the Nyquist frequency.

Incremental A/D converters operate the Delta-Sigma modulator in transient mode. This transient operation includes resetting the integrators in the converter's loop filter and incorporates filtering and down-sampling operations into the core operation of the ADC. The general concept is shown in Figure 2.10.

Rather than running the converter continuously, the converter is run at a clock rate Fs for N cycles before having its integrators reset. This N is equivalent to the OSR of a conventional

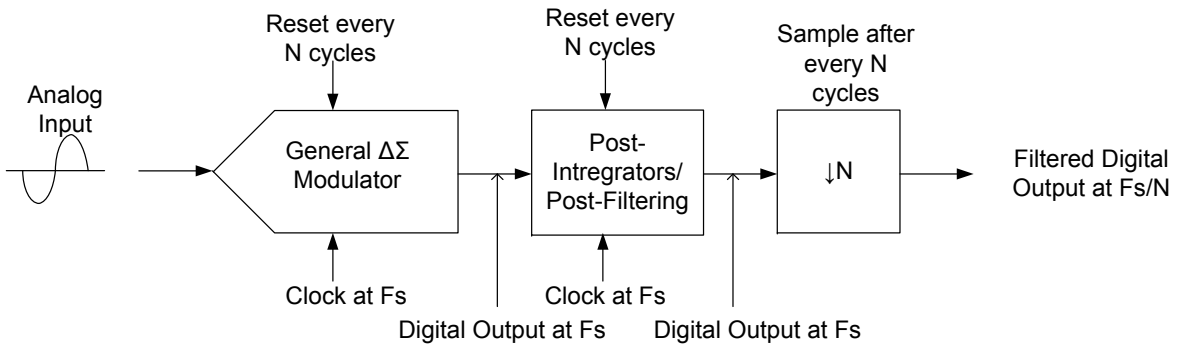


Figure 2.10: A General Incremental Modulator

Delta-Sigma modulator. During this time, the digital output is sent directly to a series of digital integrators/accumulators. After N cycles, the output of the post-integrators is sampled before being reset as with the modulator. These data samples form the digitized samples of the Incremental converter. The modulator's output data rate is therefore at Fs/N. The concept is illustrated with a first-order system shown in Figure 2.11. It should also be noted that in the system in Figure 2.11, the quantizer is assumed to be single-bit.

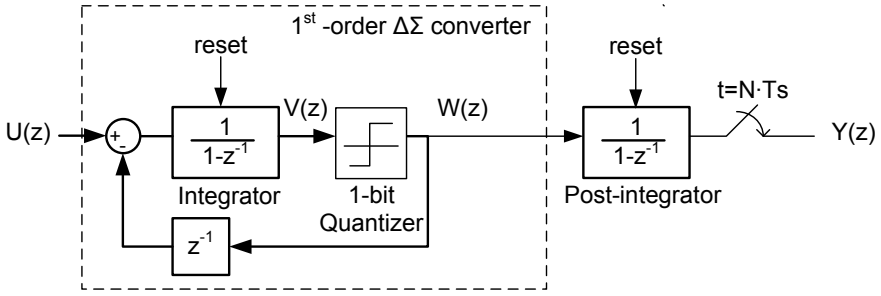


Figure 2.11: 1st-Order Incremental Modulator (Single-bit Quantizer)

From the system in Figure 2.11, the output of the Delta-Sigma modulator is given by:

$$W(z) = U(z) + (1 - z^{-1}) \cdot E(z), \text{ where } E(z) \text{ is the quantization error} \tag{2.13}$$

Following the post-filter operation:

$$Y(z) = W(z) \cdot \frac{1}{1 - z^{-1}} = \frac{U(z)}{1 - z^{-1}} + E(z) \tag{2.14}$$

So in actual fact, the modulator in Figure 2.11 outputs the original quantization error, whose magnitude is bounded by $[-Vref, Vref]$, (or the full-scale input swing) while integrating the input. The post-integrator has infinite gain at DC, amplifying the low frequency signal content, while leaving the original quantization noise alone. So rather than attenuating the quantization noise, the modulator amplifies the signal-content relative to the quantization noise.

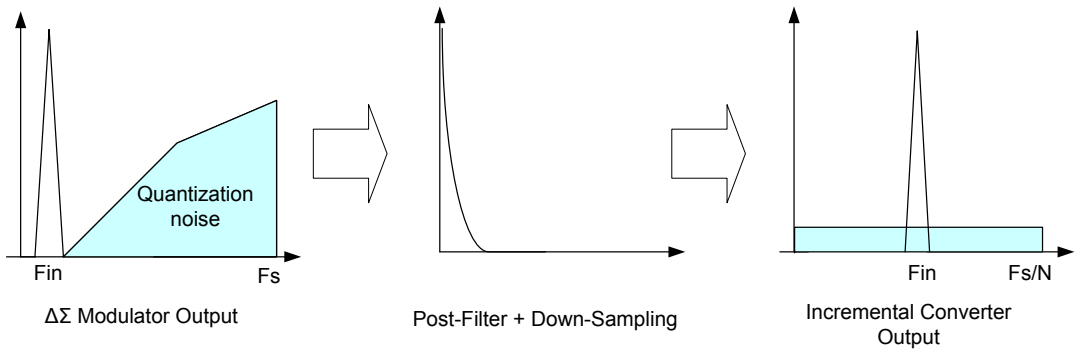


Figure 2.12: Functionality of Post-Integration

Some aspects of this basic topology should be noted:

- Filter Quality:

  The post-filter is basically a poor quality low-pass filter. Compared to the ideal brick-wall filtering assumed with traditional Delta-Sigma modulators, the suppression of quantization is therefore not as good. The filter quality can be improved using multiple stages and leading to higher order filtering

- Low-Pass Filtering of Signal

  As shown above, integration is applied to the input signal, leading to averaging of the input signal [13]. (Since N samples are taken of the input, this is equivalent to rectangular windowing, which leads to a Sinc-shaped low-pass filtering effect in the frequency domain.) However, the resultant low-pass filtering effect is unimportant assuming that the OSR of the converter is high, and the bandwidth of the input is small relative to the clock rate.

2.4.1 Analysis of 1st Order Incremental ADCs

Having decided on a traditional discrete-time implementation of an Incremental data converter, the next step is to decide what order of modulator is required to obtain 14-bit resolution with an appropriate OSR. The most basic topology is, as described in section 2.3, the first-order converter. [11] contains a mathematical framework for evaluating the resolution, and required OSR for this and higher order Incremental converters. The following discussion will assume a 1-bit quantizer. Obviously the use of more quantization levels should lead to improved resolution. The ultimate choice of quantizer levels is discussed in the next chapter.

The analysis of the first order design is straight forward, considering that it can be seen as equivalent to a dual-slope ADC where the positive and negative slopes are interleaved [13]. [11] obtains a similar result by bounding the quantization error. Either way, the result is that a first order Incremental converter requires 2^N clock cycles to achieve N-bit resolution. For 14-bit resolution, this leads to:

$$2^N = 2^{14} = 16384 \tag{2.15}$$

This is equivalent to the required OSR. Such a high OSR is a bit excessive and would lead to much higher power dissipation in digital circuitry due to the high clock rate required. A marked improvement can be obtained by simply adding a second digital post-integrator after the Delta-Sigma modulator, as well as dithering to spread out the power spectrum of the 1-bit quantizer [12]. However, much more significant improvements can be made by increasing the order of the entire ADC. Just as a 2nd order Delta-Sigma modulator has much higher resolution than a first order, so is the case of Incremental converters.

2.4.2 2nd Order Incremental ADCs

Analogous to the first order case, the second order Incremental ADC consists of a resettable 2nd order Delta-Sigma modulator followed by a 2nd order, or cascade of 2 post-integrators as shown in Figure 2.13. As with Delta-Sigma modulators, the order of the post-integrators must be at least as high as that of the modulator itself, to sufficiently suppress quantization noise [3].

From equation 2.13 discussed earlier, the cancellation effect between the modulator NTF and post-filtering is clear when they are of equal order. In fact it is suggested [3] that N+1 order filtering be used. This is also an option in Incremental converters and will be discussed below.

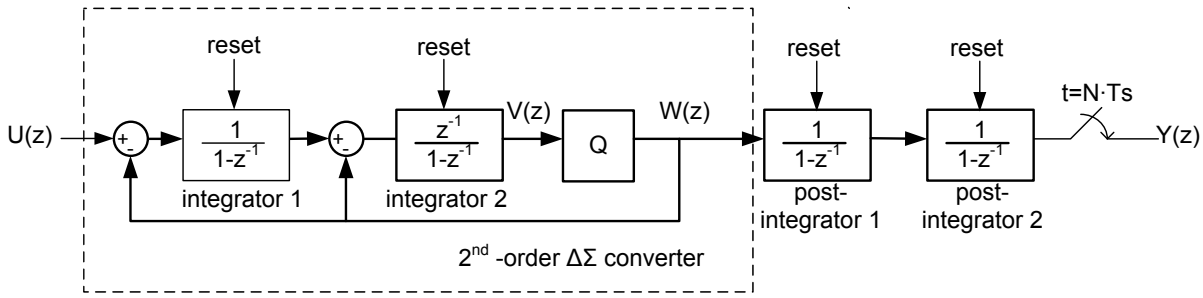


Figure 2.13: 2nd-Order Incremental Modulator With 2 Post-Integrators (Single-bit Quantizer)

To quantify the SNR of this design, [12] uses a time-domain description of the post-integration process as a double summation. The assumption is made that the converter's signal u is at DC (which is reasonable assuming high OSR). As in the case of the first order system, the post-filters essentially cancel out the 2nd order modulator's NTF, while applying integration to the input signal.

$$W(z) = U(z) + (1 - z^{-1})^2 \cdot E(Z) \text{ , where } E(z) \text{ is the quantizer error} \quad (2.16)$$

$$Y(z) = \frac{U(z) + (1 - z^{-1})^2 \cdot E(Z)}{(1 - z^{-1})^2} \quad (2.17)$$

$$Y(z) = \frac{U(z)}{(1 - z^{-1})^2} + E(z) \quad (2.18)$$

Since the input is considered a constant, after the 2 integrator stages and N integration steps, the output of the post-filter in the time domain is:

$$y[n] = \left(\sum_{m=1}^{N} \sum_{n=1}^{m} u[n] \right) + e[n] \quad (2.19)$$

$$y[n] = \frac{N \cdot (N-1)}{2} \cdot u + e[n] \quad (2.20)$$

$$Y_N[n] = u + \frac{2}{(N-1) \cdot N} \cdot e[n] \quad (2.21)$$

Now e[n], the quantization error is bounded by $(-Vref, +Vref)$, so $|e[n]| \leq Vref$. Normalizing the expression above, the relative error can be given by [11]:

$$Error \leq \frac{2 \cdot |Vref|}{u \cdot N \cdot (N-1)} \tag{2.22}$$

For the case of quantizers with more levels, $e[n]$ can simply be bounded using its expected value, which would decrease for more quantization levels. From equation 2.4.2, in order to achieve 86dB SNR (14-bits) with an input level at half of full-scale (-6dBFS) requires:

$$10^{\frac{-86}{20}} \geq \frac{2 \cdot |Vref|}{(0.5Vref) \cdot N \cdot (N-1)} \tag{2.23}$$

$$N \cdot (N-1) \geq 4 \cdot 10^{+4.3} \tag{2.24}$$

$$N \approx 283 \tag{2.25}$$

As mentioned earlier, increasing the filter order to three post-integrators should improve quantization noise suppression analogous to the case of Delta-Sigma modulators. [12] contains a detailed analysis treating quantization noise as a uniformly distributed random variable. Rather than repeat that here, simulation is used to assess the impact of adding a third digital post-integrator in section 3.1.

2.4.3 3rd Order Incremental ADCs

Analysis of a complete third order Incremental converter combining a third order Delta-Sigma modulator with three post-integrator stages follows the 2nd order analysis using time-domain analysis, and simply replacing the double summation formula with a triple summation:

$$Error \leq \frac{3! \cdot |Vref|}{u \cdot N \cdot (N-1) \cdot (N-2)} \tag{2.26}$$

To achieve 86dB SNR:

$$10^{\frac{-86}{20}} \geq \frac{3! \cdot |Vref|}{(0.5Vref) \cdot N \cdot (N-1) \cdot (N-2)} \tag{2.27}$$

$$N \cdot (N-1) \cdot (N-2) \geq 12 \cdot 10^{+4.3} \tag{2.28}$$

$$N \approx 63 \tag{2.29}$$

2.4.4 Thermal Noise and OSR

The above discussions have considered only the quantization noise of the design. A power efficient, high-resolution ADC will however, be limited by thermal noise, rather than quantization noise. In a typical oversampled modulator, the output brick-wall filter suppresses flat thermal noise by integrating only a fraction, namely 1/OSR of the total thermal noise. The post-integrators in the Incremental converter have an analogous effect. The basis for this is the fact that the integrator sums correlated input samples, as well as uncorrelated samples of thermal noise. As a result, the integrated signal has power on the order of N^2, while noise power simply gets multiplied by N. This effectively reduces noise by N.

However, due to the low quality of filtering, the effect is not quite as straight forward. [12] contains a detailed analysis of Gaussian random noise in an Incremental converter. For 2 post-integrators, the actual thermal noise suppression is 4/3N, which leads to 33% excess noise, or 1.25dB, which is not too significant.

Chapter 3

System-Level Design of Incremental Converter

This chapter describes the system-level design of the Incremental converter implemented in this work. In the previous chapter, a brief overview was given of the concept of Delta-Sigma modulators, and their role as the heart of an Incremental data converter. Using established theory, the OSR needed for 2nd and 3rd order Incremental converters to achieve 14-bit SNR was analyzed. In this chapter, the performance of these Incremental converters is first verified with simulation. The basic design choices of the Incremental converter are described. Beginning with section 3.2, the remainder of the chapter describes the design of the Delta-Sigma modulator at the core of the Incremental converter. The design of the Delta-Sigma modulator begins with the modulator's NTF and STF. The NTF and STF characteristics, i.e. the location of their poles and zeros, determine the attainable SNR and stability of the modulator's feedback loop. Next, the modulator transfer functions must be implemented using realizable circuits such as discrete-time integrators.

3.1 Incremental Converter Design

Matlab simulations were conducted using the second and third order topologies of Incremental converter described in the previous chapter. Table 3.1 shows the results. The case of the

Table 3.1: Simulated Performance of 2nd and 3rd Order Incremental Converters

Configuration	OSR	SQNR	Calculated OSR Requirement
2nd Order + 2 Post-Integrators	275	86.5	283 *(From Eq. 2.25)*
2nd Order + 3 Post-Integrators	177	86.2	-
3rd Order + 3 Post-Integrators	83	86.0	63 *(From Eq. 2.29)*

second order topology with two post-integrators matches quite well with predictions. However, the third order analysis (equation 2.29) of the previous section over-predicts the performance attained with the simulated third order converter. Due to the large out-of-band gain of the ideal third order NTF $(1 - z^{-1})^3$, a converter implementing this NTF tends to have poor stability. As a result, the simulated third order Incremental converter has different NTF poles which help improve stability, but reduce the maximum noise suppression of the NTF. As a result, the simulated third order converter shows reduced performance.

3.1.1 Choice of Single-Bit Quantizer

The above results all assume the use of a single-bit quantizer. As mentioned, more quantization levels reduces the expected value of the quantization error, increasing SNR. Single-bit quantizers do have some drawbacks [3] including idle tones, in which DC inputs can lead to strong tonal components. In higher order modulators, they may also lead to unstable feedback loops due to the relatively high effective gain of the quantizer. However, there are also compelling reasons to use single-bit quantizers in low-power applications, and particularly in the case of Incremental converters:

1. Linearity:

   Since single-bit quantizers only have two levels, they are inherently linear [3]. With more quantization levels, the DAC required to feedback to the input will suffer form non-linearities due to mismatch in the circuits. To achieve low distortion, techniques such as Data-Weighted-Averaging (DWA) are required to suppress DAC non-linearities. This requires additional digital circuitry. In this low-power design, with relatively few circuit components, any added digital circuits could cause a significant increase in power.

2. Simplified Filtering

   In Incremental ADCs where the post-filtering uses simple digital integrators, single-bit quantization means that the first post-integrator can simply be a binary counter. Multi-bit quantization requires additional circuitry to add the quantizer outputs. The advantage does however only apply to a first-stage post-integrator.

Ultimately, single-bit quantization was chosen for the above reasons. The low modulator order also means that stability was not much of an issue; i.e. more quantizer levels were not needed to maintain stability.

3.1.2 Selection of Modulator Order and OSR

OSR Tradeoff

The choice of OSR determines the attainable signal bandwidth for a given clock rate. This is particularly important at high speeds where clock rates become technology-limited and bandwidths can only be increased by reducing the OSR.

The benefit of a lower OSR is that the required clock rate is minimized. Therefore digital clock circuitry (whose power scales with clock rate) and analog circuits can operate with lower bandwidth. The benefit to analog circuits is canceled by the capacitor size which must increase to maintain the thermal noise level, but the savings in digital circuits should remain. From Table 3.1, moving from a second to third order modulator cuts the required clock rate to a third, potentially cutting digital circuit power by the same amount. Typically, adding a third stage to the Delta-Sigma modulator (aside from digital circuits) should not increase analog power consumption by three times, so if digital power is comparable, the digital power savings may be worthwhile. The trade-off becomes less obvious moving to higher order modulators, as increased circuit complexity and modulator stability come increasingly into play.

Cost of Filtering

However, the above discussion does not include the cost of the digital post-filter which is included in the Incremental converter being designed. Increasing the order of filtering following the Delta-Sigma modulator increases digital circuit complexity and power consumption. However, the same is true of higher OSRs. Higher OSRs mean that the post-integrators must have more register bits to prevent bit over-flows. So from the filtering perspective, both increasing filter order or OSR both increase digital complexity. The trade-off here therefore requires more detailed analysis in terms of the numbers of required gates.

Chosen OSR and Topology

In this design, the OSR was actually dictated by thermal noise requirements. As stated in section 2.3, the maximum ADC sampling capacitance was determined by the load that could be handled by the PGA. As will be discussed in the next chapter, this meant that **an OSR of at least 1500 was required** to achieve sufficiently low thermal noise. In order to be power efficient, the design was also intended to be thermal noise-limited, with quantization noise pushed below thermal noise. Using an OSR of 1500, a second order modulator with 1-bit quantizer offers sufficiently low quantization noise, and was chosen for this design.

3.2 (Delta-Sigma) Modulator System Implementation

3.2.1 Modulator Filter Structure

Having chosen a 2nd order modulator with single-bit quantization, the task remains to select the filter architecture of the Delta-Sigma modulator. The structure depicted in Figure 2.13 is only one way of implementing second order noise-shaping. Figure 2.13 consists of a feedback architecture which includes both delaying and non-delaying integrators and which may be referred to as a CRFB or "Cascade of Resonators Feedback" topology [14].

In addition to a variety of feedback architectures, there are also several feed-forward architectures (see [3]) where integrator outputs feed directly into the quantizer input. These architectures complicate circuit design due to the required summation at the quantizer input. In some cases, this requires an additional amplifier stage as in [15]. However, alternative approaches have been proposed [16] that avoid this additional stage.

For this design, a CIFB "Cascade of Integrators Feedback" architecture was selected as shown in Figure 3.1. As opposed to CRFB, this topology simplifies timing somewhat as both integrator stages sample the feedback and input signals at the same time. In this topology , the input also feeds into the input of the second integrator. This reduces the input signal content contained in the output of the first stage integrator, which should reduce distortion [17] due to non-linearities in the first stage.

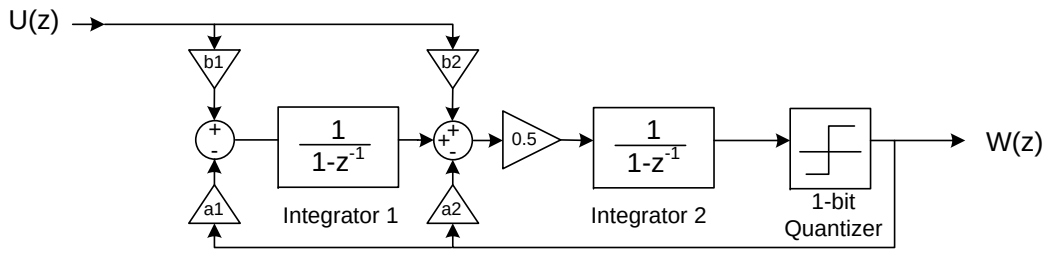


Figure 3.1: 2nd-Order CIFB Delta-Sigma Modulator

The modulator in Figure 3.1 has the following transfer functions:

$$\text{NTF}=\frac{(z-1)^2}{z^2+(a2-2)\cdot z+(a1-a2+1))}\ ,\ \text{STF}=\frac{b2\cdot z+(b1-b2)}{z^2+(a2-2)\cdot z+(a1-a2+1))} \tag{3.1}$$

3.2.2 Dynamic Range Scaling

In order to keep the integrator output signal range within the swing of the opamp, the input of the second stage integrator was scaled by 0.5. This had little impact since its output drives a single-bit quantizer. If done in the first stage, it would require a subsequent gain to preserve the filter transfer function. With multi-bit quantizers, it would also affect the reference voltage range of the quantizer.

Table 3.2: Modulator Filter Coefficients

Coefficient	Value	Rounded Value
a1=b1	0.4721	0.5
a2=b2	1.2361	1.5

3.2.3 Filter Coefficients

In higher order filter designs, the effectiveness of noise shaping must be traded off against the modulator's stability, with higher SNR sometimes coming at the cost of a reduced stable input range. (NTFs which have higher SNR tend to have higher out-of-band gain, reducing loop stability.) An extremely useful aspect of the second order topology is its demonstrated stability for inputs very close to full-scale [3]. This greatly simplified the filter design. Using the ubiquitous Delta-Sigma Toolbox [14], the required filter coefficients of the modulator were easily obtained. [1]

In the converter circuit, the filter coefficients are implemented as capacitor ratios, and must therefore be rounded or truncated. Fortunately, this second order design is very robust to variations in its coefficients. Figure 3.2 shows that even 30% coefficient variations lead only to ±5dB variations in SNR for an OSR of 256.

Due to the small capacitor sizes used and the limitation of minimum unit capacitor sizing, the coefficients used were rounded aggressively as shown in Table 3.2. The resultant NTF is given by:

$$\text{Unrounded NTF: } \frac{(z-1)^2}{(z-0.484e^{0.213\pi})\cdot(z-0.484e^{-0.213\pi})} \tag{3.2}$$

$$\text{Rounded NTF: } \frac{(z-1)^2}{z\cdot(z-0.5)} \tag{3.3}$$

[1] NTF was synthesized using the "synthesizeNTF" function specifying a second order loop, 2-level quantizer and maximum out-of-band NTF gain of 2.

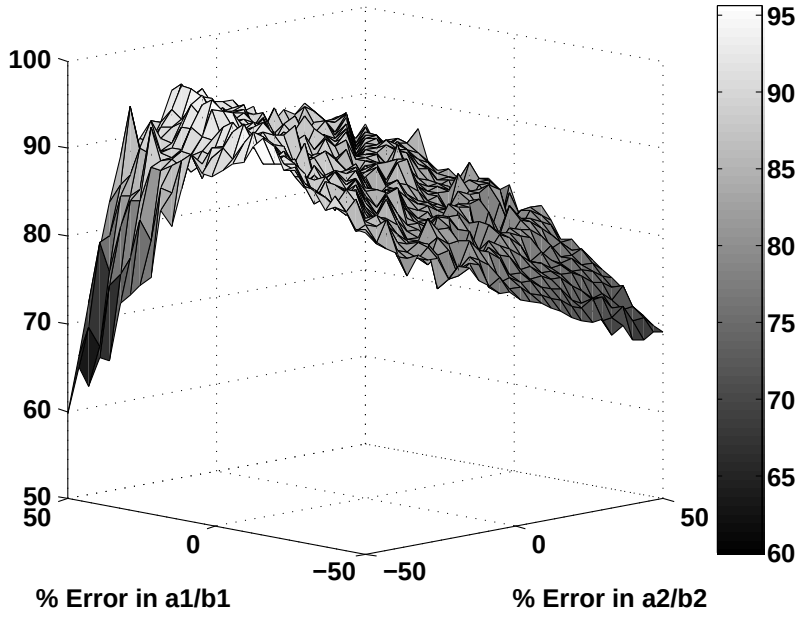


Figure 3.2: SNR (dB) Vs. Coefficient Errors

3.2.4 NTF Characteristics

All discussion thus far has assumed a modulator NTF of the form $(1 - z^{-1})^N$ for an Nth order (low-pass) Delta-Sigma modulator. NTFs of this form have their zeros at DC. This is not always the case. Depending on the bandwidth of interest, it may be beneficial to move these zeros to higher frequencies. This can steepen the slope of the NTF at the edge of the signal band, reducing quantization noise for lower OSRs. In this design, the OSR is so high that this is not required and the filter coefficients required to accomplish it would not be practical to implement, so the NTF zeros were placed at DC.

The topology chosen also has non-zero poles in the modulator NTF and STF. By keeping them away from the unit circle, their effect is reduced. In the NTF, the zeros which lie on the unit circle mostly dominate, especially near DC. The effect is more evident in the STF. In this case, these poles are not canceled and lead to peaking at the signal band edge and which is shown in Figure 3.3. (The STF poles and zeroes could be canceled by adding a b3 input feed-in to the input of the quantizer, but that was not done here.)

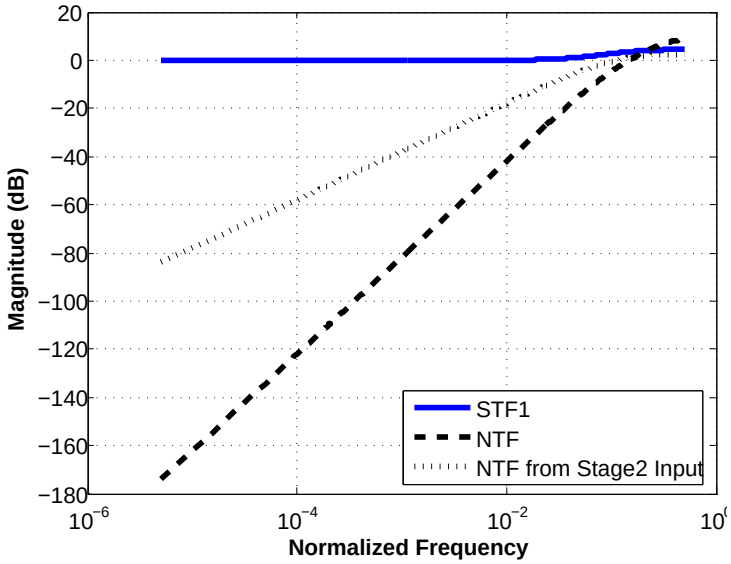


Figure 3.3: Modulator NTF and STF

3.2.5 Signal Suppression Effect of Input Feed-Ins

The output of each integrator in the modulator contains the input signal as well as noise-shaped quantization noise. Injecting signal into the input of the next stage following an integrator suppresses the signal content that must be carried by that integrator. In Figure 3.1, this should cause the first stage to carry mostly quantization noise. This is confirmed by comparing Figures 3.5 and 3.4 which show simulation results with and without the feed-in to the input of the second integrator. Adding the b2 feed-in path reduces stage 1's input U(z) signal content by roughly 40dB. As a result, non-linearities in the first integrator stage are less likely to result in input-dependent distortion.

Figure 3.6 shows results where there is also a feed-in directly to the quantizer. This not-only suppresses the signal content in the second integrator, but further suppresses stage 1's signal level by approximately 15dB. As will be discussed later, the second stage's performance is less constrained, meaning it is less important to reduce its signal content. In addition, simulations later on in the design confirmed that the impact on stage 1 had no significant benefit in terms of linearity, so this extra feed-in was omitted.

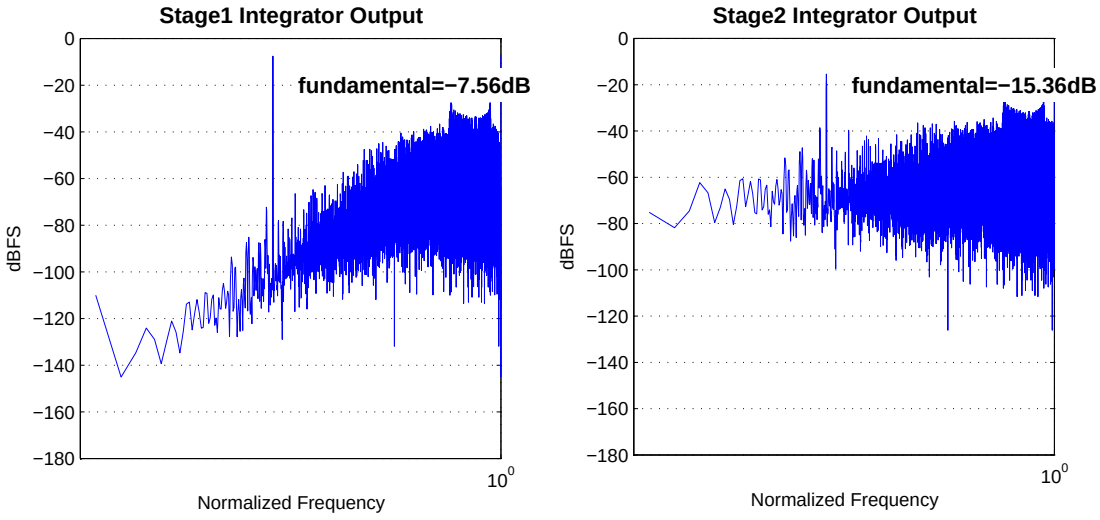


Figure 3.4: Simulated Integrator States Without b2 Feed-in

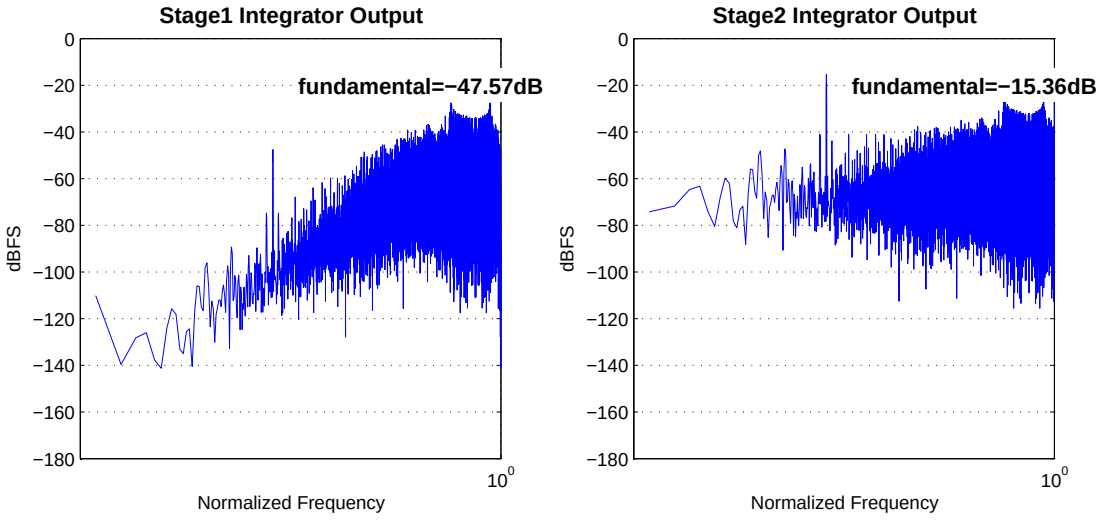


Figure 3.5: Simulated Integrator States of Design in Figure 3.1

3.2.6 Effect of Finite Opamp Gain

All discussion thus far has assumed ideal integrator stages. In fact, with traditional switched-capacitor integrators, the integrator pole can only be as close to DC as the opamp gain is high. Finite gain causes these integrators to become "lossy" [3], meaning that rather than having the response $I(z) = I(z)z^{-1} + U(z)$, they instead have a response similar to $I(z) = I(z)z^{-1} + U(z) - \frac{1}{A} \cdot I(z)z^{-1}$, where A is the opamp's open loop gain. Equivalently, this can be seen from the fact that the ideal integrator response has infinite gain at z=1. In the real

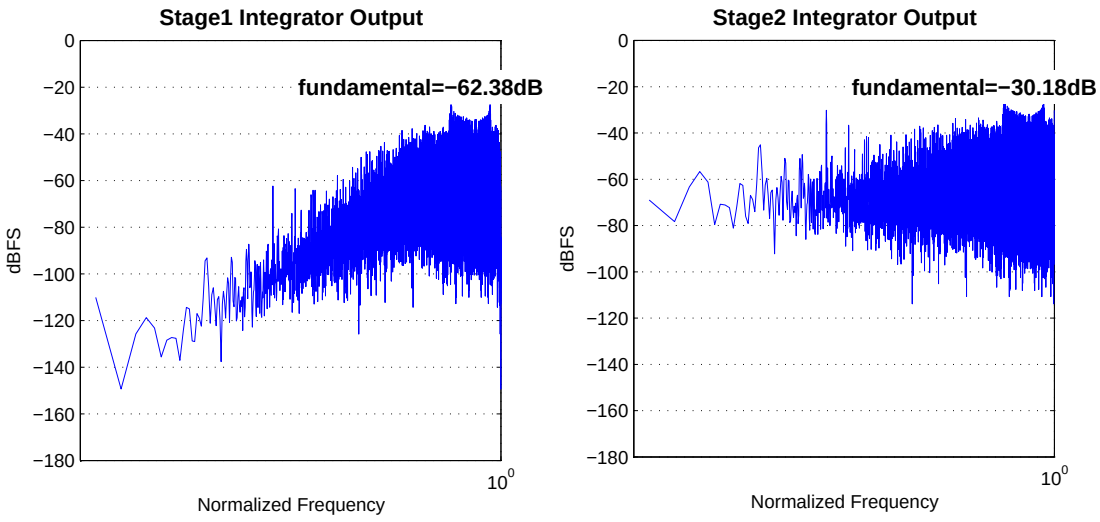


Figure 3.6: Simulated Integrator States With Input Feed-in to Quantizer

analog circuit, no amplifier can achieve infinite gain, so the DC gain of the integrator becomes the DC gain of the opamp.

With ideal integrators, at low-frequencies, the NTF should continue to push noise lower and lower towards DC. With finite opamp gain however, the amount of noise suppression is bounded below by the combined opamp gains of the modulator. The SNR-OSR trade-off will hit a maximum, where the NTF stops decreasing and becomes uniform. The transition can be seen from Figure 3.7 which shows the NTF of the same system as in Figure 3.3 for varying values of opamp DC gain (both opamp gains are equal). When operating in the flat region of the NTF, the SNR is determined only by the number integrator stages and each of their DC gain values. The required opamp gain for this design is discussed below.

3.2.7 Note on Simulation of Delta-Sigma Modulator vs. Incremental Converter

The above discussion has centered on the design of the Delta-Sigma modulator, which combined with the post-integrators constitute the Incremental modulator. Because incremental operation requires OSR samples to generate a single Nyquist-rate sample, generating an N-point spectrum requires N×OSR samples. In Delta-Sigma operation however, every point can be

used in the FFT. This, combined with the need for post-filtering means that simulation time, both in Matlab and at the circuit level, is much greater for the Incremental converter. Because the post-integrators are digital, their performance can be assumed to be ideal. Therefore the performance of the Delta-Sigma modulator corresponds directly to that of the incremental converter. Most notably, any distortion in the Delta-Sigma translates directly into the incremental converter. For simplicity, most simulations centered on the Delta-Sigma modulator, with much fewer simulations used to confirm the performance of the Incremental converter.

High OSRs also lead to increased simulation time due to the increased number of FFT-points needed to obtain sufficient in-band bins for SNR calculation. Therefore, simulations were conducted a the much lower OSR of 256. It was found through simulation that if the Delta-Sigma modulator could achieve roughly 90dB SNR with an OSR of 256 at the required input signal level, it would have sufficient performance for the overall Incremental converter which will operate with a much higher OSR.

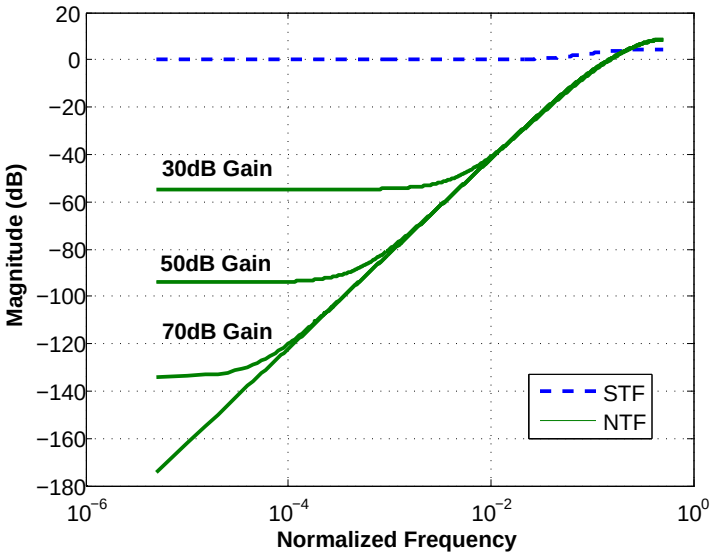


Figure 3.7: Effect of Opamp Gain on NTF

3.2.8 Required Opamp Gain and Modulator Order

For this design, it was found through simulations (see Figure 3.8) that 50-60dB gain was sufficient to push quantization noise to the desired levels (more than 10dB below the targeted thermal noise floor). This requirement brings up an additional aspect of modulator design. While achieving the required opamp gain was not problematic in this design, it does become difficult in newer CMOS technologies where low voltage supplies may prevent the use of cascoding. In such a case, a higher order modulator might be required, where the opamp gain could be distributed across more stages, requiring less gain from each stage and possibly permitting the use of low-voltage topologies.

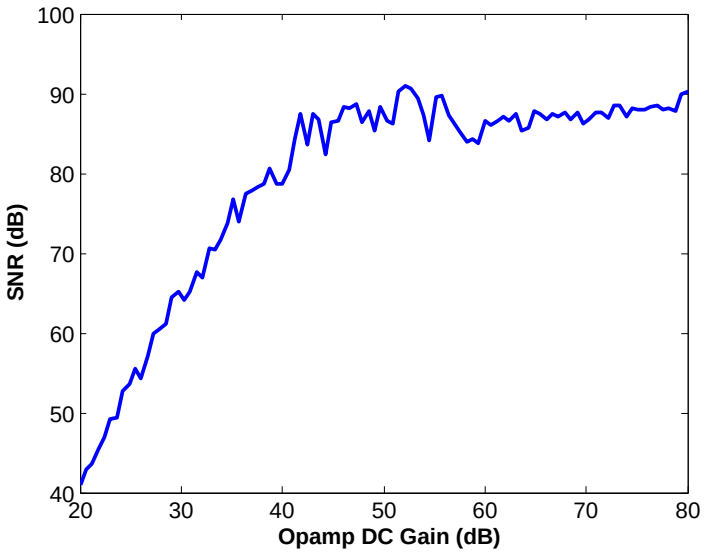


Figure 3.8: SNR vs. Opamp Gain (Delta-Sigma Modulator with OSR=256)

3.3 Matlab Simulation Results

Figure 3.9 shows the simulated output spectrum of the Delta-Sigma modulator with an OSR of 256. The SNR of the Delta-Sigma modulator is calculated by summing the quantization noise up to Fs/2/OSR. This is equivalent to having an ideal brick-wall filter. Figure 3.10 on the other hand, shows the converter operating in incremental mode with the same OSR. As suggested earlier, the Incremental converter's basic post-filtering does not achieve the same

noise suppression as is assumed with the Delta-Sigma modulator.

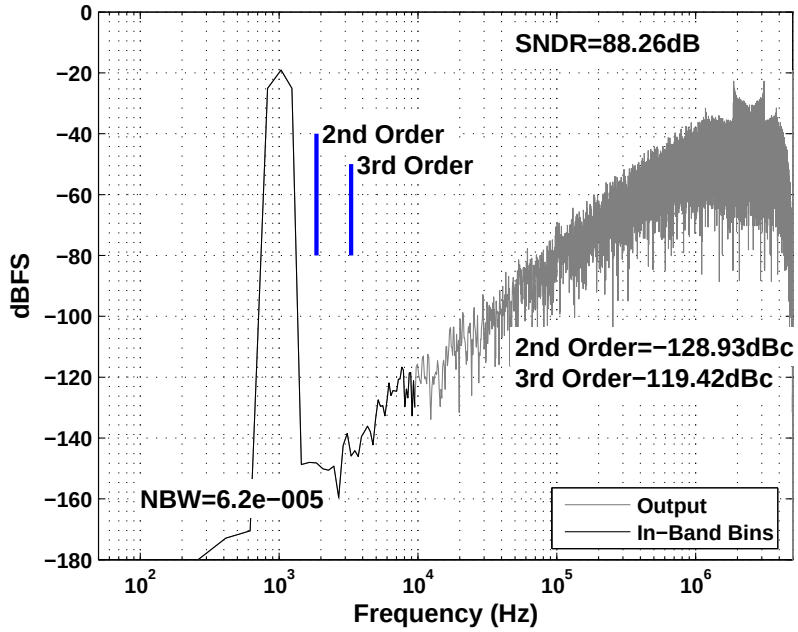


Figure 3.9: Simulated Delta-Sigma Modulator Spectrum for 400mVpp Input and OSR=256)

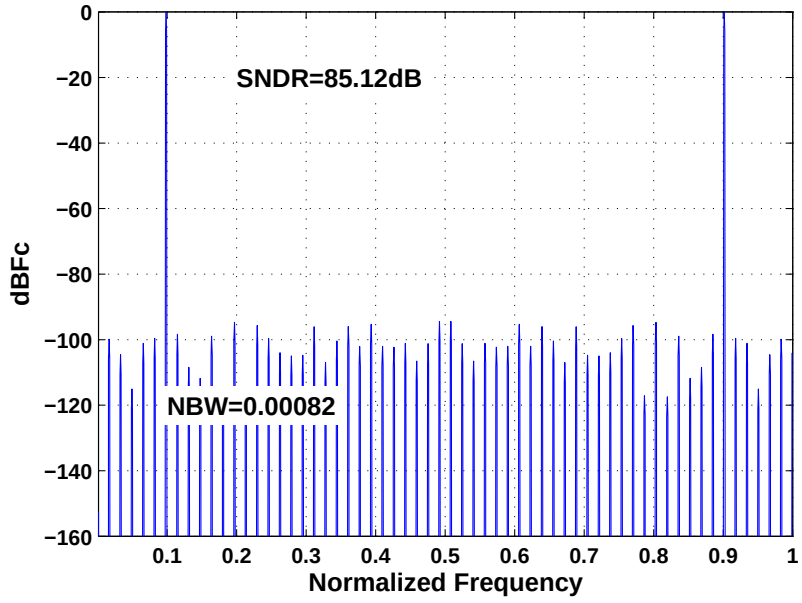


Figure 3.10: Incremental Converter Spectrum for 400mVpp Input and OSR=256)

However, given that a much higher OSR will be used in the actual circuit, the Incremental modulator does have sufficient noise performance. For an OSR of 1500, the quantization noise is more than 10dB lower than the targeted 14-bit accuracy, as shown in Figure 3.11.

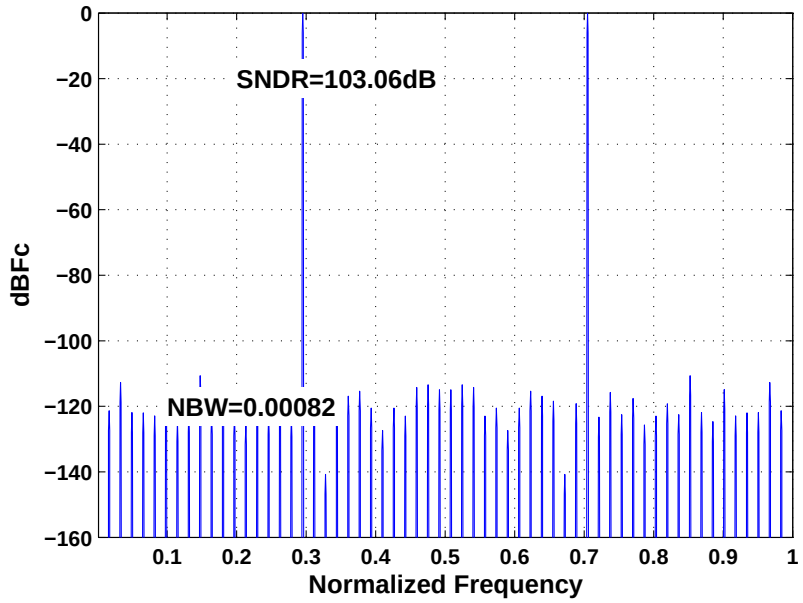


Figure 3.11: Incremental Converter Spectrum for 400mVpp Input and OSR=1500)

3.3.1 Note on FFT Spectra: NBW

NBW denotes the equivalent "Noise Bandwidth" of the FFT plot. Each FFT bin contains the total broadband/white noise within a bandwidth of NBW, so to find the power spectral density of white noise, one must divide the FFT value by the NBW. The NBW is given in units of normalized frequency, 1/Fs (where Fs is the sample rate in Hz). For the Hanning windowing used in FFT plots throughout this thesis, this has a value of 1.5/(The Number of Points in the FFT).

Chapter 4

Circuit Design

Having designed the Incremental data converter at the system level, attention is turned to the implementation of the modulator at the circuit level. Section 4.1 describes the switched-capacitor circuits used to implement the Delta-Sigma modulator. Capacitor sizes required to implement filter coefficients and achieve thermal noise requirements are summarized. The complete circuit also includes chopping to remove low frequency flicker noise. Crucial to the operation and performance of the modulator are the two operational amplifiers (opamps), which dominate the power consumption of the converter's analog circuitry. Beginning with section 4.2 , the remainder of the chapter is devoted to the selection and design of a low-power opamp topology. First, the performance requirements of the opamps are determined through simulation. Next, the power consumption of several popular opamp topologies are compared. Section 4.3 describes possible techniques to increase the power efficiency of opamps. It is concluded that a class-AB opamp should be used. Finally in section 4.5, the chosen opamp topology is described.

4.1 Circuit Level Implementation of Delta-Sigma Modulator

4.1.1 Capacitor Sizing

Input Sampling Capacitors

As discussed in section 2.2.4, the input sampling capacitor size of the ADC was limited by the maximum load that could be handled by the PGA stage, which was approximately 500fF per side of the differential circuit. This led to a certain thermal noise level. Since the circuit bandwidth tends to exceed the clock rate in switched-capacitor circuits, sampling causes all thermal noise to fold back in-band leading to a uniform noise floor from DC to Fs. As a result, for a given OSR, the in-band noise is found by dividing the total RMS noise by the OSR. A suitable OSR was therefore chosen to achieve 90dB SNR for a sinusoidal input with an amplitude of 400mV peak-to-peak differential. (To allow for some margin beyond the required 86dB, an SNR of 90dB was targeted in the design.) This was done using the basic assumption of total input-referred noise of 4kT/C [3], which is true when the opamp noise is negligible, but still fairly accurate when a low-noise opamp is used.

$$V_{N,rms}^2 = \frac{1}{2} \cdot \left(\frac{V_{pk-pk}}{2}\right)^2 \cdot 10^{\frac{-SNR}{10}} \tag{4.1}$$

$$\frac{4kT}{C_{sample}} \cdot \frac{1}{OSR} = \frac{1}{2} \cdot \left(\frac{400mV}{2}\right)^2 \cdot 10^{\frac{-90}{10}} \tag{4.2}$$

$$OSR = \frac{4(1.38x10^{-23})(300K)}{500fF \cdot \frac{1}{2} \cdot \left(\frac{400mV}{2}\right)^2 \cdot 10^{\frac{-90}{10}}} \tag{4.3}$$

$$OSR = 1656 \tag{4.4}$$

In order to reduce the OSR to a round number of 1500, the input sampling capacitors were increased to 550fF per side, which should have minimal impact on the stability of the input PGA.

Stage 2 Sizing

When referred to the input, the thermal noise of the second stage is divided by the high gain of the first stage integrator. The second stage capacitors could therefore be scaled down

significantly. In addition, the high phase-margin of the first stage opamp (to be discussed) allowed the opamp to remain stable when driving only the smaller stage 2 sampling capacitors during the sampling phase. (A less stable opamp might require larger stage 2 capacitors to maintain stability during both clock phases.) As a result, the stage 2 capacitors were limited only by the minimum size of the MIM-Capacitors of the technology and the required filter coefficients. Due to DRC rules, the minimum capacitor size is 20fF. The second stage input coefficient of 1.5, requires a capacitor ratio of 3:2, therefore the minimum capacitor size used was 2 times the minimum size at 40fF.

4.1.2 Chopping

The use of switched capacitor circuits greatly simplifies the addition of chopper stabilization to suppress flicker noise. Chopping was done using chopper switches at the input and output of the opamp, within the integrator circuit as in [18]. The chopper switches were clocked at half of the sampling rate which was higher than the flicker noise corner frequency (allowing good suppression of flicker noise). Once again, since the noise of the second stage is greatly attenuated by the stage 1 opamp gain, chopping was done only in the first stage.

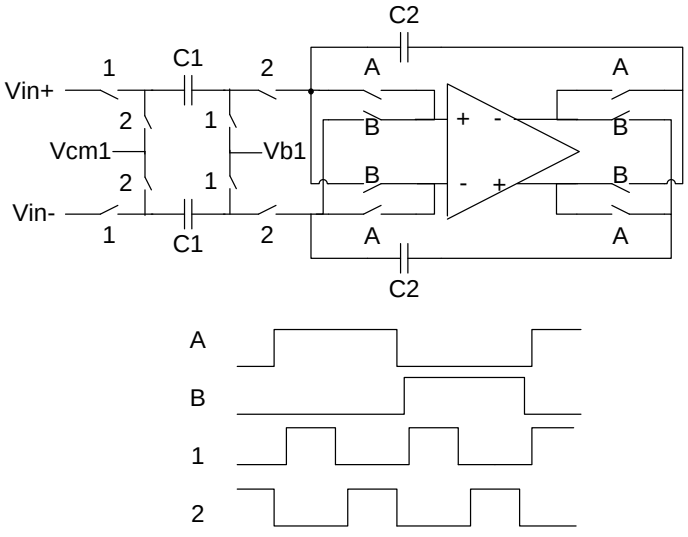


Figure 4.1: Switched-Capacitor Integrator with Chopping at Fs/2

Unlike continuous-time circuits, where chopping can have implications for bandwidth, chopping does not otherwise alter the SC integrator circuit's operation. There are however, implications for noise. The chopper switches essentially add resistor noise to the opamp input, adding to the opamp's input-referred noise.

$$V^2_{N,Opamp,Effective}(f) = 4kTR_{Switches} + V^2_{N,Opamp}(f) \tag{4.5}$$

However, if the switch resistance is much smaller than the inverse of the opamp gm, the opamp thermal noise dominates and these switches should not degrade the circuit noise. In this design, the switch noise was assumed to be small and ignored.

4.1.3 Complete Circuit Implementation

Figure 4.2 shows the complete circuit description of the Delta-Sigma modulator. Of note are a few aspects of the design:

- Shared DAC Feedback Capacitors:

  The same capacitors were used to sample the input signal and apply the feedback from the quantizer. If separate DAC capacitors were used instead, they would inject additional thermal noise. If extra capacitors are required due to common mode issues for example, the effect of the added noise can be canceled by re-sampling the input on both clock phases as in [18].

- Advanced/Delayed Clock Phases:

  Delayed clock phases were used to reduce input-dependent charge injection [7]. In addition, switches at the inputs of the opamps were kept small to reduce charge injection at these sensitive input nodes.

4.2 Power Efficient Opamp Design

Having decided on a switched capacitor architecture [3], and having sized the capacitors based on thermal noise and filter coefficients, the primary design choice now consisted of designing a

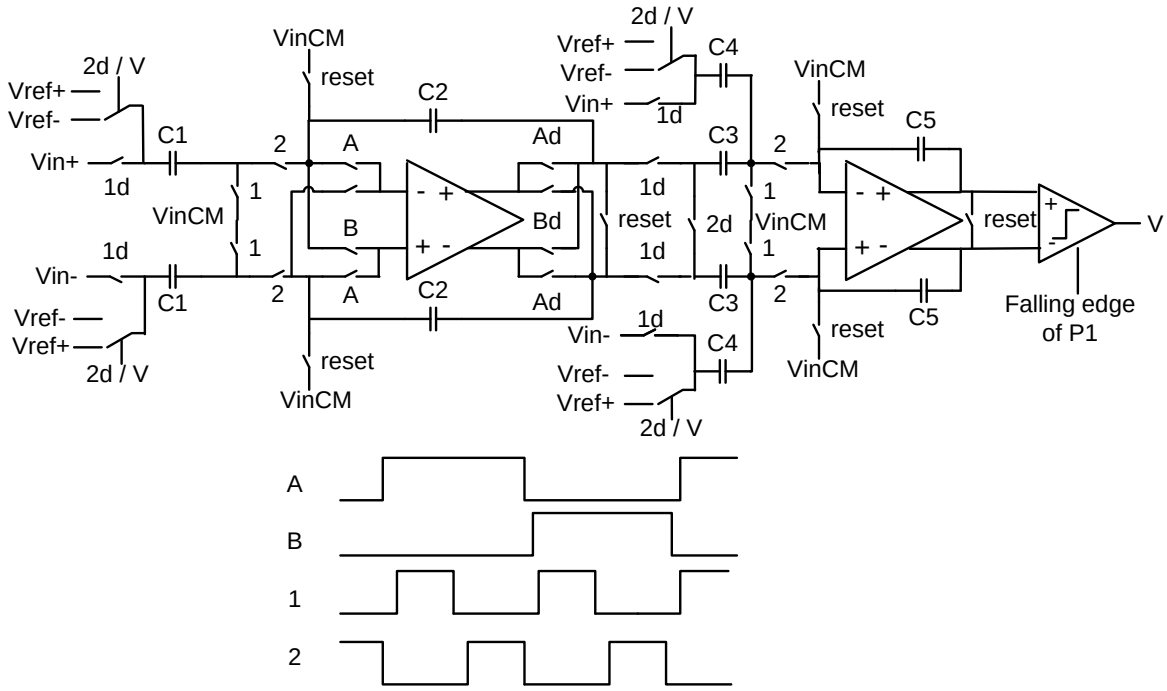


Figure 4.2: Complete Delta-Sigma Modulator

Table 4.1: Capacitor Sizes

C1	550fF
C2	C1/a1=1.1pF
C3	40fF
C4	C3/a2=60fF
C5	C3×2*=80fF

*for dynamic range scaling

suitable opamp and switches.

The resulting integrator must settle the output to an appropriate level of accuracy. It has been shown [3] that the switched capacitor integrator with opamp modeled as a transconductance, behaves as a first order system with a single time constant given by equation 4.6. Since switch resistance and opamp transconductance have equal impact on integrator bandwidth, in the interests of power efficiency, the integrator's bandwidth should be limited by its opamp transconductance, not switch resistance [9].

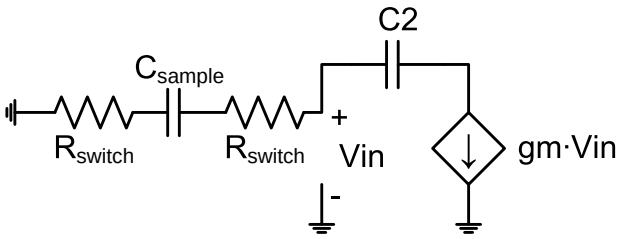


Figure 4.3: Model of Switched-Capacitor Integrator During Integration Phase [3]

$$\text{SC-Integrator Time Constant [3]: } \tau = (2R_{switch} + 1/gm)C_{sample} \tag{4.6}$$

Obviously this leads to larger switch transistors, and consequently, the clock buffer circuits will draw more power. In this design however the relatively slow clock rate and use of small capacitors led to relatively small switches. In fact, it was shown in simulation that the clock tree's wiring parasitics were similar to the actual switch capacitances.

4.2.1 Combined Bandwidth and Slewing Requirements

The above neglects the other aspect of opamp settling likely to occur: slew-rate limiting. In fact, if the integrator's settling was strictly linear, it would have very little impact on the modulator's resolution. Since each settling phase of a switched-capacitor occurs over a consistent time, all outputs would simply be multiplied by a coefficient $(1 - e^{\frac{-T_0}{\tau}})$ due to incomplete settling. Since this coefficient has no signal dependence, it would alter the modulator filter

coefficients but would not otherwise degrade performance.

However, the abrupt switching inherent in the switched-capacitor circuits leads to large instantaneous voltages across opamp inputs and slew-rate limiting during integrator settling. This introduces non-linearities as the duration of slewing depends directly on the magnitude of the input and DAC feedback signals. These can be incorporated into simulation models, some examples of which are found in [19] and [20]. The model in [20] not only includes finite opamp gain, bandwidth and slew-rate, but contains an analysis derived based on charge-conservation in switched capacitor circuits.

4.2.2 Matlab Simulation of Bandwidth and Slewing Requirements

Matlab simulations were carried out using the models of [20]. It was assumed that the current Io in each side of the opamp transconductor was equal to the maximum output (slew) current as in a differential pair. An overdrive voltage (V_{eff}) of 150mV was assumed. The opamp transconductance (Gm) and corresponding unity-gain bandwidth (f_t) were related using equation 4.7. Using these relations, the f_t for the first stage opamp was then swept. The second stage opamp, which has a reduced impact on linearity was assumed to be ideal.

Characteristics of simulated opamp with output load capacitor C_{out}:

$$f_t = \frac{gm}{2\pi \cdot C_{out}} \tag{4.7}$$

$$\text{(Using Square-Law Mosfet) } Io = \frac{gm \cdot V_{eff}}{2} = \frac{2\pi \cdot f_t \cdot C_{out} \cdot V_{eff}}{2} \tag{4.8}$$

$$\text{Slew-Rate} = \frac{Io}{C_{out}} \tag{4.9}$$

$$\text{DC Gain} = 70\text{dB (Achievable in simulation.)} \tag{4.10}$$

Figure 4.4 shows the changes in SNDR as the first stage opamp bandwidth was varied. Below a certain bandwidth, the modulator's SNDR declined steadily due to increasing third order distortion.

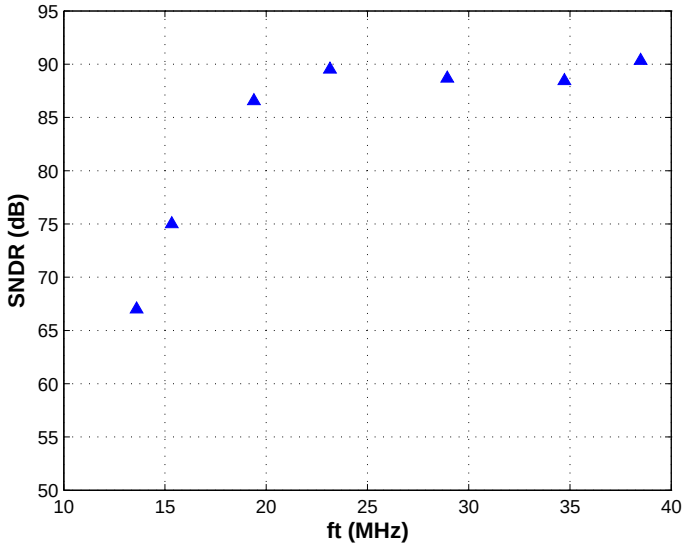


Figure 4.4: Matlab Simulation of SNDR vs. Stage 1 Opamp f_t

4.2.3 Circuit-Level Verification of Bandwidth and Slewing Requirements

The above requirements were then compared to circuit-level simulations in Cadence Spectre. The entire switched-capacitor circuit, including actual transistor switches (mosfets), was simulated. The stage 1 opamp under consideration was implemented ideally using VerilogA behavioural modeling. (The opamp was modeled with a transconductance and output impedance and included output clipping and slew-rate limiting.) From the results below, the Spectre simulations can match the Matlab results to within 1 or 2dB provided that opamp performance is sufficient.

Comparing Figures 4.4 and 4.5, the Spectre simulations more strictly constrained the required opamp bandwidth and slew-rate. Compared to the Matlab requirement of roughly 23MHz f_t, circuit simulations required 30MHz or more. One factor in this difference might be the effect of the switches used in the circuit simulation. Although these were sized such that their resistance should not greatly affect the integrator's settling bandwidth, they still have some impact, which is not included in the Matlab model. Although the peak resolution of both simulations was close, other circuit non-idealities such as charge injection, not contained

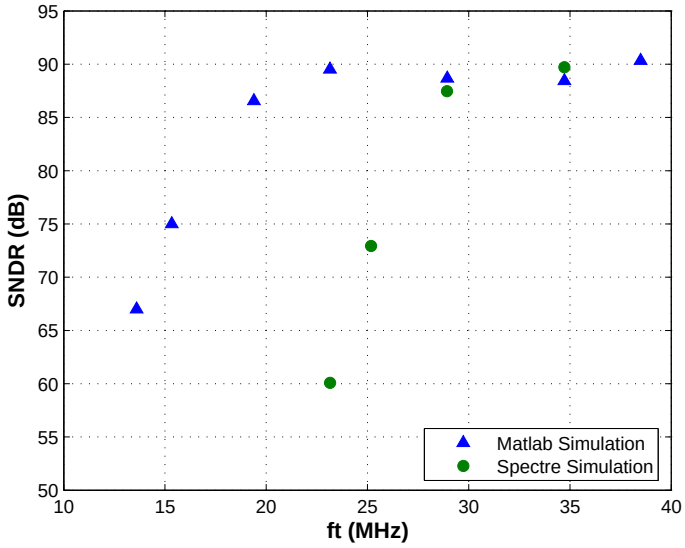


Figure 4.5: Spectre Simulation of SNDR vs. Stage 1 Opamp f_t

in the Matlab model might also account for the increased degradation seen in circuit simulation. These results do suggest though, that such non-idealities are exacerbated by poor opamp settling.

4.2.4 Opamp Topologies

Given the gain, slew-rate and bandwidth requirements discovered through Matlab and Spectre circuit simulations, the task remained to select the most suitable, power efficient opamp for the task. The common telescopic, folded-cascode, current-mirror and 2-stage opamp topologies were compared in terms of their bandwidth and noise characteristics. The details of this comparison are contained in the Appendix.

The opamp with the highest bandwidth for a given power consumption and the lowest noise is desired. Opamps with higher noise levels require larger sampling capacitors to suppress their thermal noise. More power is then required to maintain sufficient bandwidth with the increased capacitive loads.

Relative Noise Factor α

As detailed in section A.1.2 of the Appendix, a relative increase α in noise was defined and estimated for the various topologies. α describes a fractional increase in a switched-capacitor integrator stage's noise caused by excess opamp noise. Because of the impact of noise on power, the total power of an integrator/opamp stage is proportional to $(1+\alpha)$.

Conclusion on Topologies

Among the topologies compared, the telescopic opamp was found to be the most power efficient. By maximizing transconductance for a given current, its bandwidth is maximized, while its noise is minimized (α was the lowest at $\sim$0.2). Next however, the possibility of increasing power efficiency further is explored. The telescopic opamp is later used as a point of comparison.

4.3 Opamp Enhancement Techniques

There exist several options to improve power efficiency by addressing the bandwidth and or slew rate achievable from opamps.

4.3.1 Gm-Enhancement

The bandwidth-related aspect of power consumption has been addressed through some designs which seek to enhance the transconductance of the differential pair. Through the use of additional circuitry, the transconductance can be for example, doubled, by injecting signal at the input gate *and* source of the input devices. These topologies have been explored quite extensively by the authors of [21], and have demonstrated significant gains, particularly in terms of slew-rate.

However, the majority of these designs are based on a 2-stage topology with a single-ended output stage. On one side of the single-ended output stage, a diode-connected transistor eliminates the need for common-mode feedback in the output stage. In addition, the diode-connection leads to a mirroring effect that helps create a symmetrical slew-rate. It is not clear

how these output stages can be made fully differential while preserving their advantages. The bandwidth enhancement aspect of these designs does remain.

4.3.2 Class-AB Output Stages

As in the above case, class-AB output stages are often used in the interests of power efficiency. Referring to Table A.1, the constraints on required current due to slew-rate, are based on a class-A amplifiers where slew rate is limited by the use of an active load. Looking at the NMOS common source amplifier (see Figure 4.6), the NMOS input device can see large gate-to-source voltages, allowing it to pull large amounts of current. However, the PMOS active load is biased to supply Ibias, regardless of the input voltage Vin, thereby limiting the positive slew-current to Ibias. In the traditional differential pair, this is balanced on the negative slide by the tail current source which similarly limits the negative slew current.

If the restriction on positive slew current could be lifted, the common source stage offers potentially, a vastly improved slew-rate. That is the goal of class-AB output stages used in some low-power applications such as [22] and [17].

Implementation Issues

The most straight-forward approach to creating a class-AB output stage is to replace the active load of a common source amplifier, with a second, complementary common source amplifier. However, when used in a fully differential 2-stage opamp, the additional issues of *1) common-mode feedback* and the requirement of *2) level shifting* come into play. These both have to do with how the active load can be correctly biased to act as a second common source amplifier.

1. Common-Mode Feedback (CMFB):

   The current source actve load is typically biased as part of a common-mode feedback loop. It is still possible to provide common mode control by splitting the current source as in [22] and illustrated in Figure 4.7. In this way, the slew-rate is still enhanced significantly.

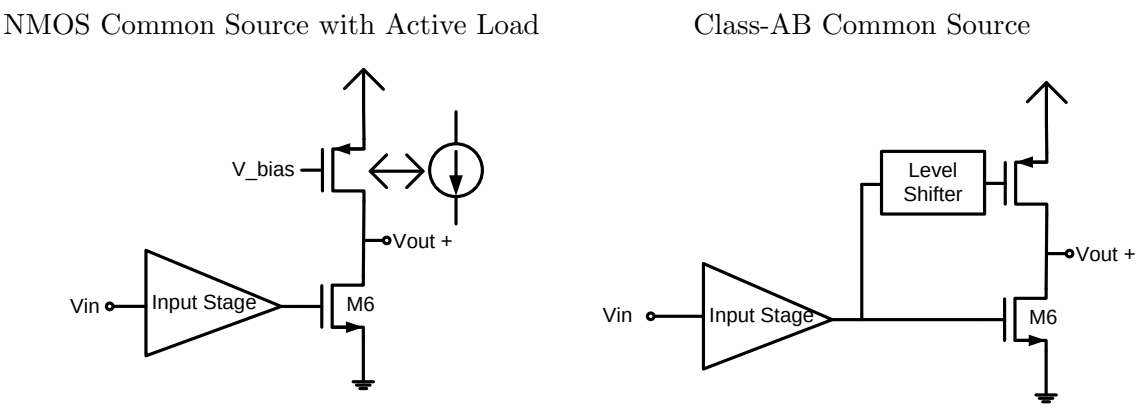


Figure 4.6: Concept of Class-AB Output Stage

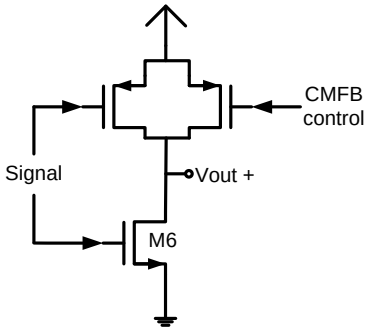


Figure 4.7: Class-AB Output Stage with CMFB Control

Alternatively, an active or switched-capacitor network can be used to apply CMFB as a common mode input to the current source. This allows a differential signal to still be driven into the current source, allowing it serve as a amplifier.

2. Level Shifting:

   The second issue is how to appropriately bias the complementary common source device. One way to accomplish this is to use a source-follower with common-mode feedback to provide a signal with the correct common-mode level. The common mode reference level of the source follower can also be set by a CMFB loop to maintain the common mode of the output stage. In theory, this source follower can consume very little power due to the low output impedance of the source follower, but the Miller-capacitance seen at the common source amplifier input can be large, still requiring a certain amount of current to push its time constant to higher frequencies.

To avoid this extra power consumption, [4] proposes using a capacitor as a battery as shown in Figure 4.8. A large resistor sets the DC level of the output stage, but is essentially floating, meaning that its output tracks the input.

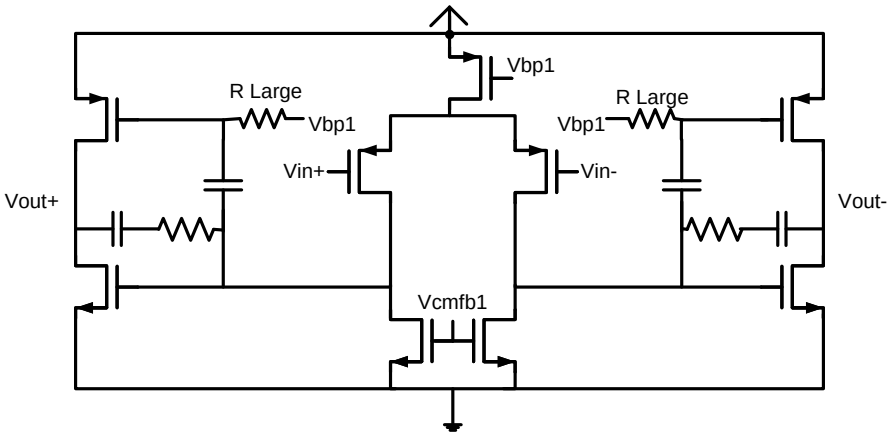


Figure 4.8: Class-AB Output Stage with "Free" Level Shifter [4]

The above discussion addresses increasing power efficiency using class-AB output stages. However, by affecting only the output stage, the gains are limited. In for example, a 2-stage opamp, the input stage, whose Gm determines the crucial opamp bandwidth is unaffected.

4.4 Concept of Class-AB Input Stage

Recently, some ([5],[23]) have sought to extend the class-AB concept to single-stage opamps. As seen from Table A.1, the advantage of the Telescopic opamp is that the entire current contributes to the input transconductance of the opamp. The use of complementary NMOS and PMOS devices in a class-AB configuration at the input of an OTA can potentially double the current utilization, achieving roughly *double* the Gm for the same current.

- Bandwidth:

  As shown in Figure 4.9, the PMOS device consumes no extra current compared to a standard common-source stage, but assuming M1 and M2 have the same Veff, would

double the available Gm and therefore halve the power required to achieve a given unity-gain bandwidth with the same load capacitance. Compared to the most efficient opamp from Table A.1, the Telescopic opamp, such a stage can achieve twice the bandwidth or consume half the power.

- Slew-Rate:

  If used in a single stage design, the class-AB input stage also operates as a class-AB output stage, potentially achieving very high slew-rates.

- Noise:

  In terms of noise, since both NMOS and PMOS sources now also contribute to the input Gm, the noise of this design is also as low as half of the telescopic design, if all transistors have the same Veff. Referring to Equation A.11, in terms of the entire integrator circuit, α=0 compared to 0.2 for a telescopic.

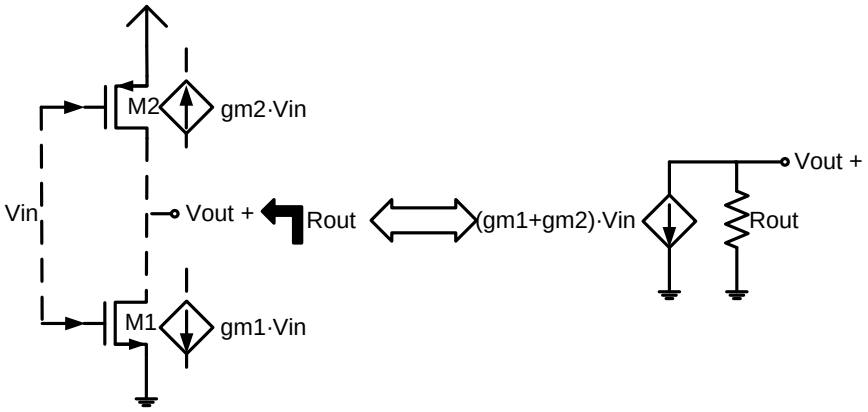


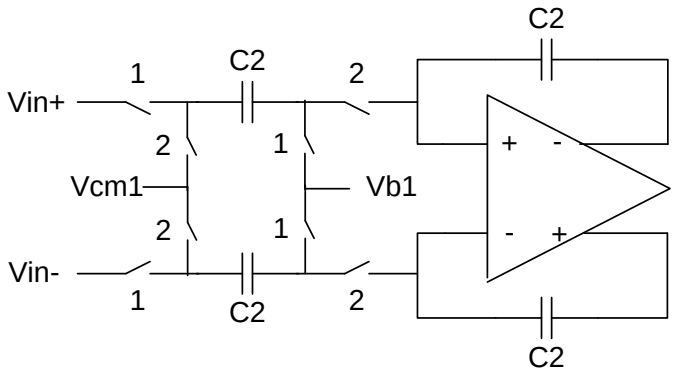
Figure 4.9: Concept of Class-AB Input Stage

The above concept is highly attractive in terms of power efficiency. Not only does the class-AB stage require only half of the current for a given capacitor size, but due to its lower noise, can also permit the use of slightly smaller capacitors when used in a switched-capacitor integrator. However, implementing this topology presents several challenges including the issues mentioned in Section 4.3.2 for class-AB output stages. [5] and [23] have also offered possible solutions to these problems.

4.4.1 Issues with Class-AB Input Stage

Lack of True Fully Differential Operation / Common-Mode Rejection

If used as a single stage as shown in Figure 4.9, the class-AB input is not a fully differential, but a so-called "pseudo-differential" circuit. Due to the lack of a tail current source, the amplifier also sacrifices Common-Mode rejection, since in common mode, the input devices do not have source degeneration. This is not problematic when used in Switch-Capacitor circuits since the input level seen at the opamp input is usually well-defined, as shown in Figure 4.10. If an input signal's common mode is not known before-hand, double-sampling [18] can be used to decouple any reference and input common modes. In this design, the input common mode was well-defined, determined directly by the resistor divider of a Wheatstone bridge, or the common-mode feedback of an input amplifier stage.



$$\begin{aligned} \text{Opamp Input Common Mode} &= Vb1 + \frac{(Vin++Vin-)}{2} - Vcm1 \\ &= Vb1 \text{ , if } Vcm1 = \text{ Input Common Mode} \end{aligned}$$

Figure 4.10: SC Integrator Common Mode

CMFB

The need for CMFB is the same as discussed in section 4.3.2. As described, two possibilities are to split the current source, or as was done in [5] and [23], use the common mode level of the complementary device for CMFB.

Complementary Input Biasing

The input bias level for the complementary PMOS (or NMOS) device must be set. As in section 4.3.2, a possible solution uses a level shifter with CMFB at its output to set the appropriate level. As discussed though, this does require additional power. In discrete time applications, a switched-capacitor network might also be used for level-shifting which does not require additional power.

Another way to simplify the input biasing is to add a tail current source. This would preserve the high Gm achieved by the design. However, this would lead to a fixed bias current, and would sacrifice the enhanced slew-rate offered by a class-AB output stage. This could however be used in a two-stage configuration, or in applications where slew-rate is not limiting. In Figure 4.11, the use of a tail current source allows independent control of biasing through the input common-mode, while maintaining CMFB through the tail source. (These roles could also be reversed.)

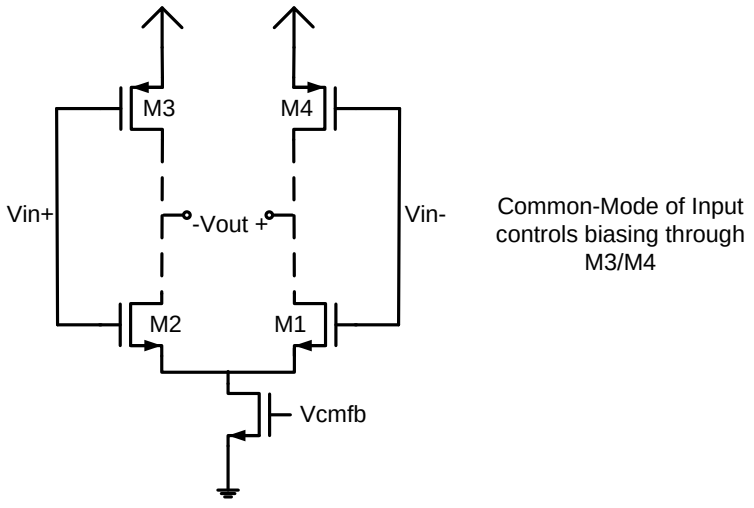


Figure 4.11: Class-AB Input Stage with Simplified Input Biasing Requirements

[23] has applied a unique dual-path structure where two-input sampling capacitor networks are used to independently bias the NMOS and PMOS devices of their class-AB OTA. The authors of [5] use a much more aggressive approach discussed below.

4.4.2 Case Study: State-of-the-Art Design using Inverters

Looking at Figure 4.9, the simplest way to achieve a class-AB input stage is to simply use an inverter, as in [5] and shown in Figure 4.12 below. In fact, since the design is biased in deep subthreshold, the authors call it a class-C amplifier, but the fundamental concept is the same. This design has also achieved the highest figure-of-merit for recent low-speed 14-bit Delta-Sigma Modulators. In the inverter, there is only a single input, other than the supply. The input level must therefore be responsible for CMFB as well as overall biasing. The authors of [5] accomplish this by controlling the voltage supply level. By setting the supply voltage close to the threshold voltages Vtn+Vtp, for a particular input level, the biasing of the inverter can be well controlled.

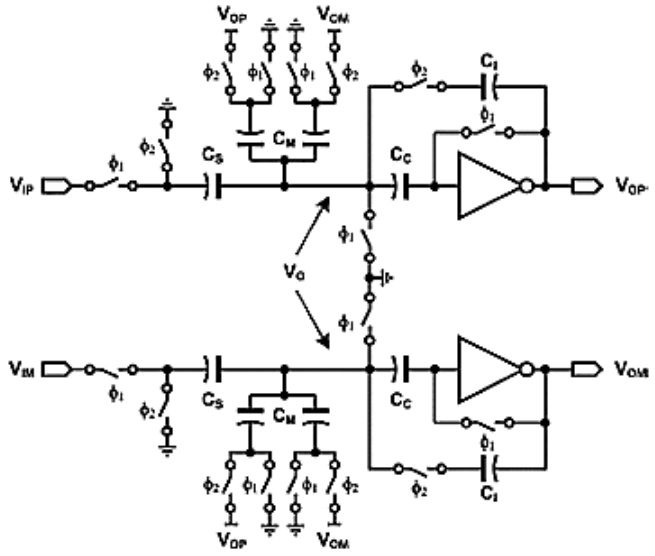


Figure 4.12: Use of Inverters as OTA *Taken From [5]*

In this design, this also leads to a low supply voltage, which helps reduce overall power consumption. Due to the low supply however, voltage headroom is restricted, likely preventing the use of cascode devices. This restricts the design to lower gains and limited input swings. More of an issue is the design's reliance on an exact power supply level to avoid huge variations in power consumption. In [24], the authors confirm that for only a 10% variation in supply voltage, the design's current consumption varies by 85%. Part of this variation can also be attributed to the biasing of transistors in subthreshold, which makes their current more sensitive to Vt

variations. This design was seen as too aggressive for this thesis. The use of a level shifter at the input might reduce the design's sensitivity to power supply changes.

4.5 Selected Opamp Design

Given the above issues, a compromise design was used which is basically a PMOS input folded-cascode in which the NMOS sources are also driven. As shown in Figure 4.13, the opamp follows the concept of Figure 4.11, essentially splitting the PMOS sources into two paths to allow for CMFB control. The use of a tail current on the PMOS inputs allows them to share the low-common mode level used to bias the input of the NMOS devices. This design functions similar to any traditional opamp and does not require any additional biasing networks.

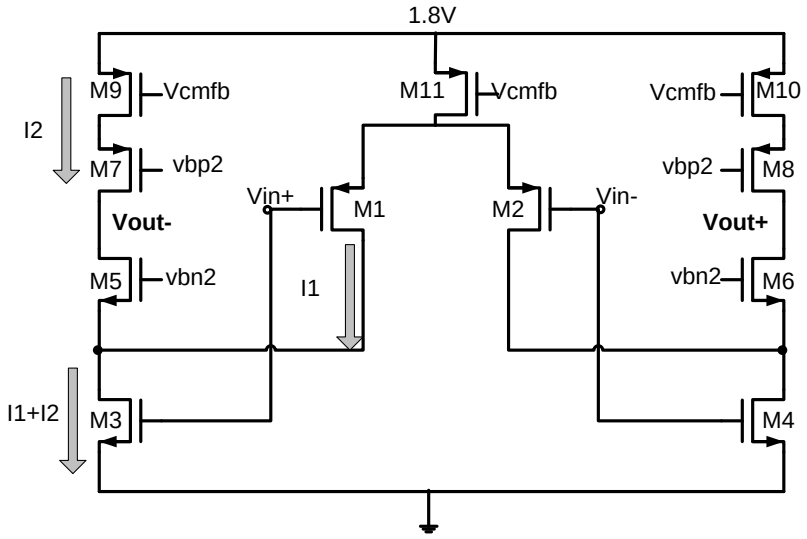


Figure 4.13: Opamp Core

Splitting the PMOS current reduces the attainable gm, but by making I1 approximately 2.5 times greater than I2, the opamp core can still achieve a large increase in gm. Reducing I2 also increases the output impedance leading to improved gain. However, having I1 larger than I2 severely limits the slew-rate of the opamp. An additional network was added to recover these losses.

4.5.1 Slew-Rate Enhancing Network

The network relies on the fact that the due to the low impedance looking into the source of M5, the gain from the input to this node is close to 1. In addition, the voltage at this node is close to a Veff, less than Vtn. Under large signal slewing conditions, a large voltage swing roughly tracking the input will appear at the sources of M5 and M6. Diode-connected transistors are connected to these nodes, similar to [7]. Although off at DC, under large signal conditions, these diode-connected transistors will begin to turn on, sinking current. Using current-mirrors, this current is mirrored to the locations where increased slew-current is required. The complete network is shown in Figure 4.14.

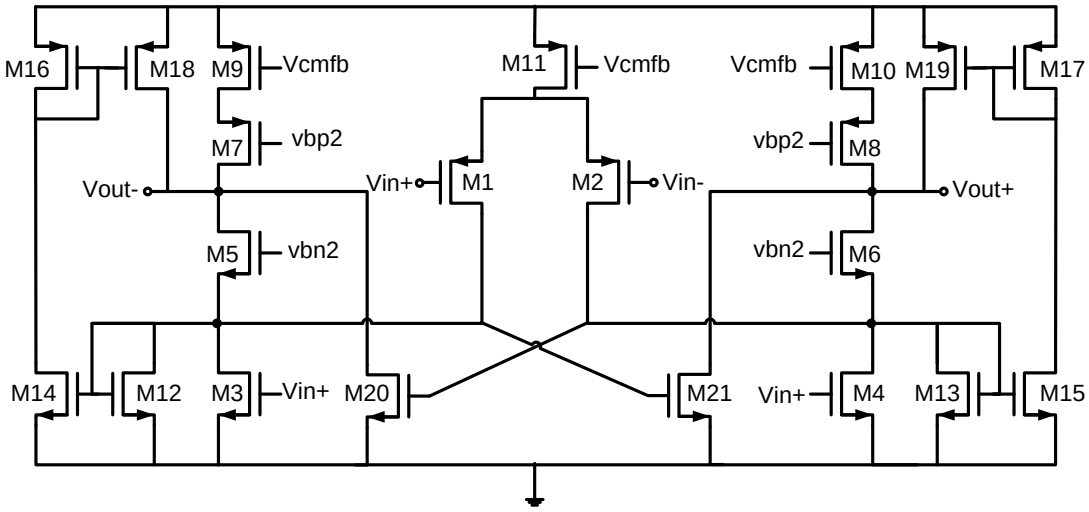


Figure 4.14: Complete Opamp

Since the diode-connected devices only turn on for large input signals, the current mirrors only turn on dynamically, consuming dynamic power. Even so, the current mirrors, which don't directly contribute to output current do increase power consumption by roughly 20%. It should also be noted that since the current mirrors are driven directly with signal, the opamp's slew rate is in fact somewhat proportional to the input step, and not fixed. An additional characteristic of this design is that the Gm-based bandwidth and slew-rate requirements of the opamp can be decoupled in the design, so that the level of slew-rate improvement can be varied for a fixed opamp bias current.

4.5.2 Comparison to Other Opamp Topologies

One can compare the expected performance of the above-described opamp to the topologies considered in section A.1. In terms of bandwidth, this design attains an approximately 70% increase in gm for the same total current, and should therefore consume 1/1.7=59% of the power of a telescopic opamp using identically biased input devices (i.e. the same Veff) and attaining the same bandwidth. However, to increase slew rate, the additional network increases power by a further 20%, causing the opamp to consume roughly 59%×1.2=71% of the power of a telescopic, leading to a power savings of roughly 30%. This, along with the noise performance is summarized in Table 4.2 below.

The relative increase in integrator noise α of this opamp is calculated using equation A.14, assuming that the PMOS current sources (M9 & M10) have half of the Veff of the input devices M1 & M2 and M3 & M4, and using the square-law expression for gm. Additionally, the slew-enhancing network is assumed not to contribute noise since it should be off during final settling.

$$\alpha = \frac{\gamma}{1+\gamma} \cdot \left(\frac{\sum(Gm_{CurrentSources})}{\sum(Gm_{Input})} \right) \tag{4.11}$$

$$\alpha = \frac{\frac{2}{3}}{1+\frac{2}{3}} \cdot \left(\frac{\frac{2I_{9,10}}{V_{eff9,10}}}{\frac{2I_{1,2}+2I_{3,4}}{V_{eff1,2/3,4}}} \right) \tag{4.12}$$

$$\alpha = \frac{2}{5} \cdot \left(\frac{\frac{0.3}{2}}{\frac{1+0.7}{1}} \right) \tag{4.13}$$

$$\alpha = 0.04 \tag{4.14}$$

From Table 4.2, one can see that the opamp designed achieves more than half of the power savings possible with a fully class-AB design. However, it does so without having to add additional biasing and or level-shifting circuits.

As an additional note, the high slew rate achievable with this opamp can relax the bandwidth requirements of the opamp when used in switched-capacitor circuits. By reducing the duration of slew rate limiting, more time is available for settling, therefore requiring less bandwidth to

Table 4.2: Opamp Current Estimates Including Noise Requirement

(Based on same assumptions* as Table A.5 in Appendix)

Topology	**Base Current**	α	**Total Current** (Base Current × (1+α))	**Relative Power**
Design from Figure 4.14	0.6· I_o	0.04	0.6×1.04· I_o=0.62·I_o (× 1.2 margin)=0.75·I_o	-37%
Ideal fully Class-AB Opamp	0.5· I_o	0	0.5·I_o	-58%
Telescopic	I_o	0.2	1×1.2· I_o = 1.2· I_o	-
Folded-Cascode	2·I_o	0.6	2×1.6· I_o = 3.2· I_o	+166%
Current-Mirror (k=1)	2·I_o	0.6	2×1.6· I_o = 3.2· I_o	+166%
2-stage	2·I_o	0.2	2×1.2· I_o = 2.4· I_o	+100%

*Assuming:

- I_{Gm}=I_{Slew} (Input Gm pair have same current as slew current)

- Current sources have 1/2 the V_{eff} of input devices

- For 2-stage opamp, $C_{Miller,Stage1} = C_{out}$ and stage 1 gain is large

settle to the desired accuracy. In applications where slew-rate limiting rarely occurs, this design is less advantageous.

Chapter 5

Transistor-Level Circuit Implementation

This chapter describes the implementation of the complete Incremental data converter, including the Delta-Sigma modulator at the transistor level. Sections 5.1 to 5.6 describe the circuits making up the Delta-Sigma modulator. The first portions of the chapter are devoted to the design of the two opamps, beginning with the bias regime of the opamp input devices. Next the remaining analog circuits are described. Section 5.7 summarizes simulation results of the Delta-Sigma modulator including simulated quantization and thermal noise levels. Sections 5.8 to 5.9 describe the remaining digital circuits used to transform the Delta-Sigma modulator into an Incremental ADC. Finally in section 5.10, an issue discovered with the gain stage designed in [1], which leads to higher than expected thermal noise is described.

5.1 Opamp Design

5.1.1 Choice of Opamp Biasing Regime

Much of the previous discussion, on power efficiency has concentrated on maximizing the transconductance (Gm) for a given bias current. At the transistor level, this involves operating the opamp input devices with low Veff's. It is clear from the Mosfet square-law model, where Gm can be written as Gm=2·Id/Veff, that Gm is maximized for low Veff's. For a constant bias

current, for low enough Vgs, the transistors enter the subthreshold region where current is modeled by an exponential relationship, and transconductance eventually saturates [25], ceasing to be a function of Vgs. Figure 5.1 shows Gm/Id vs Vgs for the $0.18\mu m$ CMOS used in this design. One can see that Gm/Id increases as Vgs decreases, but begins to saturate as Vgs approaches 0.

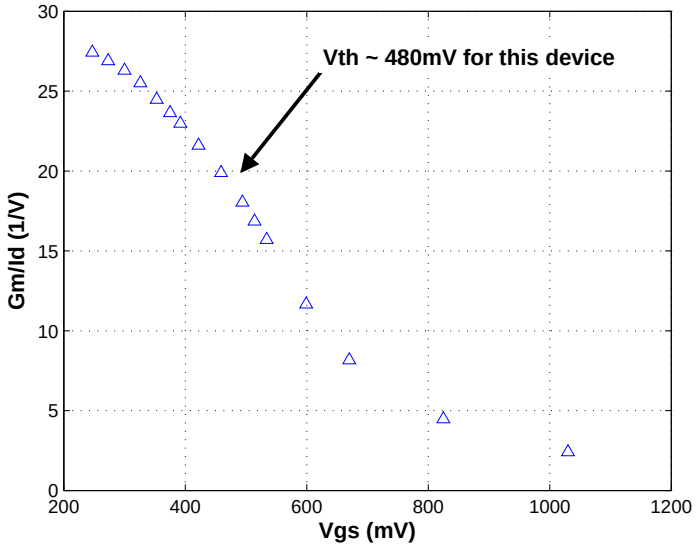


Figure 5.1: Simulated Gm/Id vs. Vgs

Subthreshold Operation

Although it seems an obvious choice to operate the opamp in deep subthreshold. There are drawbacks:

1. Increased Parasitic Capacitance:

   Firstly, for a constant Gm the required W/L ratio of the transistors becomes increasingly large in subthreshold. For a fixed length, this leads to larger device gate areas, which will reduce the opamp's achievable bandwidth, due to the increased capacitive loading. This makes subthreshold operation impractical at higher speeds. However, it is possible at the low clock rates of this design.

2. Bias Sensitivity:

   The second significant issue is the transistor's increased susceptibility to variations in its bias voltage. This is particularly important in the chosen pseudo-differential opamp (see figure 4.14) where the NMOS input devices also control the opamp's bias current. Due to mismatch, Vt variations, ohmic losses etc, the intended bias voltage may vary. Moving towards weak inversion as the Veff becomes smaller, or as the transistor enters subthreshold (where current varies exponentially with Vgs), such variations could lead to increased variability in the operating point. Figure 5.2 shows the percentage change in bias current for a $\pm 1\%$ in Vgs and shows that variation does increase as Vgs decreases.

   However, this may also be an overly pessimistic assessment. In practice, this sensitivity is counteracted somewhat by the fact that random Vt mismatch is reduced in weak-inversion due to the increased gate area.

3. Modeling Accuracy:

   The $0.18\mu m$ CMOS kit used in the design uses older BSIM3v3 modeling. This older model may not properly model device operation in deep subthreshold [26]. Specifically, it might over-estimate the peak achievable gm in subthreshold.

Selected Bias Point

The power savings available in weak, compared to strong inversion were too large to ignore. In addition, reducing the bias sensitivity significantly requires such large Veff's that voltage headroom would be restricted. Figure 5.3 shows the current required to achieve a fixed gm for varying bias conditions. From the plot, there is a point near a device width $100\mu m/\text{mA}$, beyond which power savings fall off as the device enters subthreshold operation. Beyond that point, the exponential subthreshold behaviour kicks in, which is seen from Figure 5.3 as the Vgs vs W relation becomes linear on the logarithmic x-axis.

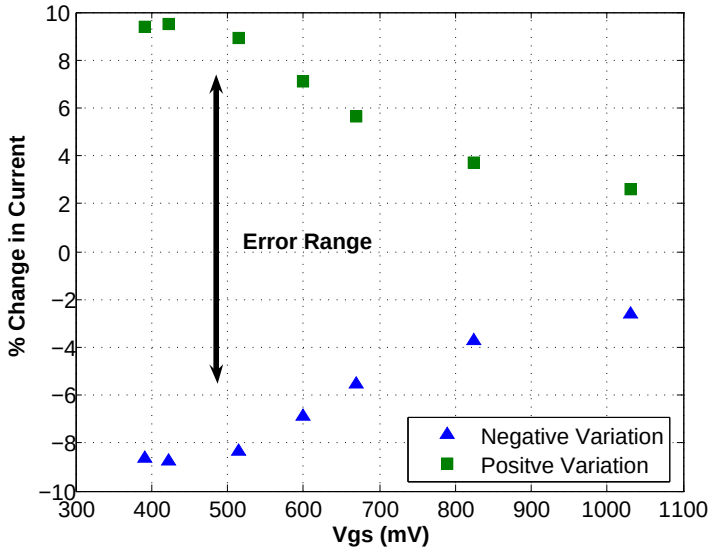


Figure 5.2: Simulated Bias Current Variation for ±1% Change in Vgs

A bias point of approximately 130μm/mA was chosen, beyond which, additional power savings require increasingly large devices widths. A further 30-40% power savings can be had, but at the cost of a 10 times wider device width.

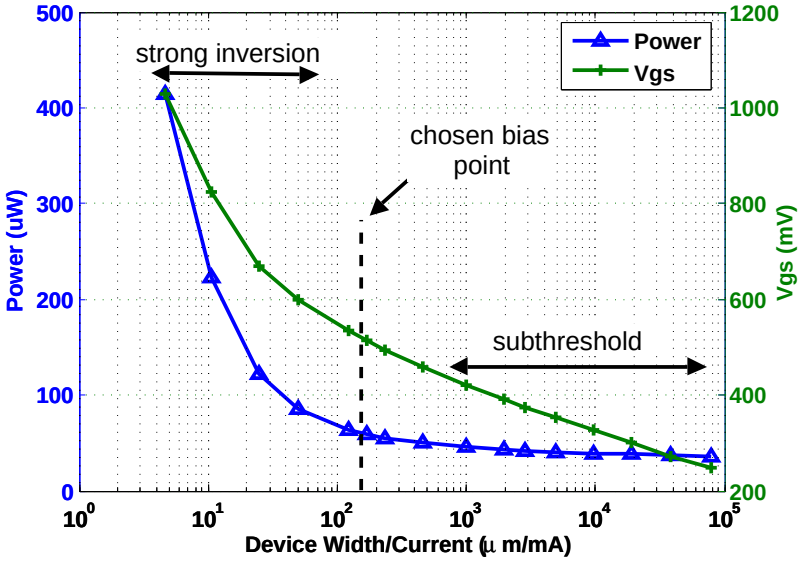


Figure 5.3: Power Required to Achieve Gm=1mA/V vs. Width/Current Ratio

5.1.2 Stage 1 Opamp

The opamp architecture used in the first integrator stage of the modulator has been discussed previously. It should be noted that using this high slew-rate design, the required bandwidth was lower than predicted in section 4.2.3 for a traditional opamp having a fixed slew rate.

The circuit was biased using constant current biasing to reduce variations in power consumption over process and temperature. However, in order to reduce the power consumed by bias circuits, they used much longer channel lengths than was possible in the opamps themselves. As a result, the opamp and bias circuits do not track well together over process variations. Table 5.1 shows the opamp specifications for typical and worst case conditions for supply and temperature. The opamp's current consumption varies approximately ±10% for ±10% change in supply voltage and over temperature extremes. Including the supply voltage variation, power consumption variation increases to ±25% over the same conditions.

Table 5.1: Stage 1 Opamp Specifications

Specification	TT/1.8V/80°C	SS/1.6V/125°C	FF/2.0V/0°C	Monte-Carlo Standard-Deviation (σ)
βf_t (MHz)	23.2	20.0	28.5	0.76
PM (°)	75.9	76.8	77.6	2.67
DC Gain (dB)	75.2	76.4	69.7	0.6
DC Current (μA)	9.0	8.3	9.9	0.44
DC Power (μW)	16.4	13.3	19.8	0.79

Noise Efficiency of Opamp

As in the previous chapter, the relative noise increase α, caused by this opamp can be calculated based on the gm of various transistors. Using simulated gm values, α was again calculated using equation A.14 (see section A.1.2):

$$\alpha = \frac{2}{5} \cdot \frac{gm_{PMOS,Source}}{gm_{PMOS,Input} + gm_{NMOS,Input}} \tag{5.1}$$

$$= \frac{2}{5} \cdot \frac{13.2\mu A/V}{61.3\mu A/V + 69.5\mu A/V} \tag{5.2}$$

$$= 0.04 \tag{5.3}$$

The above result matches closely with equation 4.14. As expected, this opamp has quite a low noise level. From the above, one can also see how the opamp's transconductance is increased compared to an opamp using only the NMOS devices, such as in a telescopic opamp. (The PMOS devices were biased more aggressively, closer to subthreshold than the NMOS devices since variations in their Vt would not affect the opamp's overall bias current and operating point.)

Power Down of Opamps

In order to power the opamp on and off, the NMOS cascode devices were used as series switches to turn the opamp current on and off. A separate PMOS series switch was used to power off the PMOS input pair. The low gain from these devices to the outputs means that the requirement of large decoupling capacitors (to reduce noise) is reduced at these nodes. Using the cascode devices, high decoupling capacitance could still be used on the current sources. Figure 5.4 shows the complete opamp circuit.

5.1.3 Stage 2 Opamp

Due to the smaller capacitor sizes used in the second stage, the power consumption is inherently smaller, making more aggressive power-efficient designs less worth-while. The stage 2 opamp was designed as a telescopic opamp without the tail current source. The removal of the tail current allows a lower input common mode, simplifying switch design. Since nonlinearities in the second stage opamp are attenuated by the first stage integrator gain, the second stage opamp requires less bandwidth. However, it was still designed with extra margin since any power savings would be quite small.

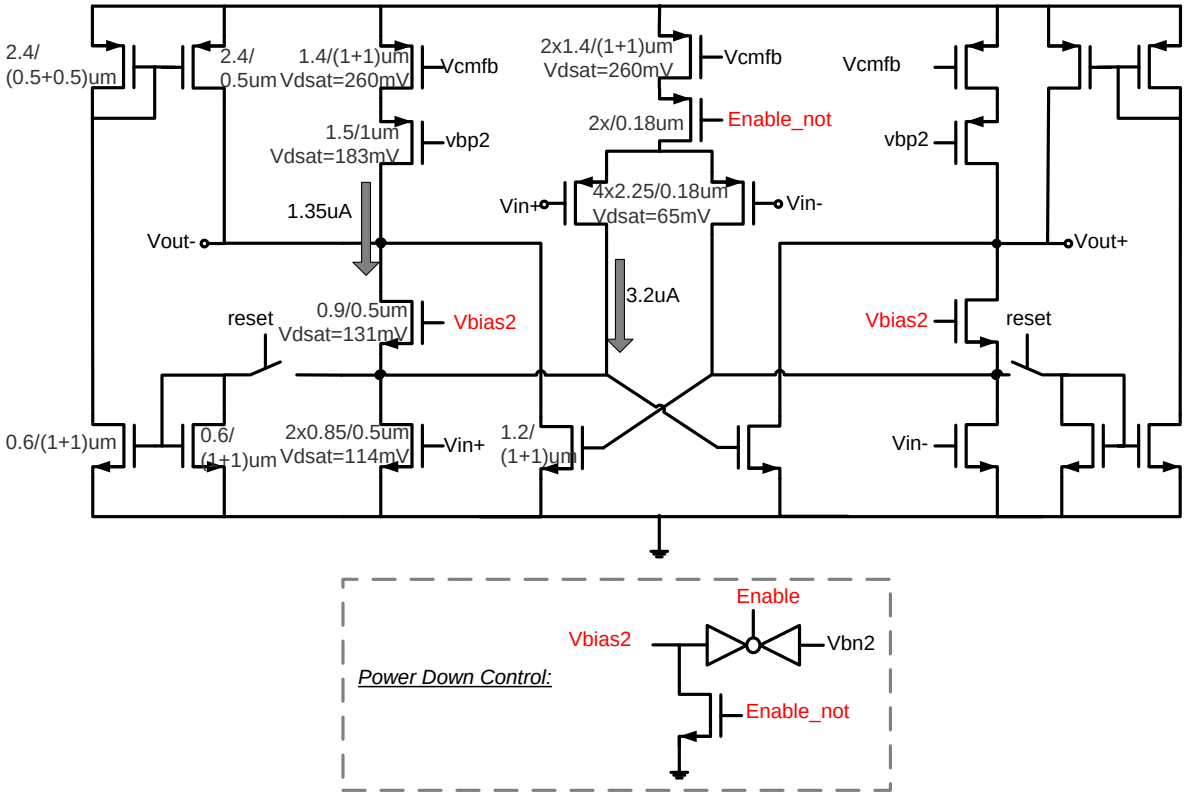


Figure 5.4: Stage 1 Opamp

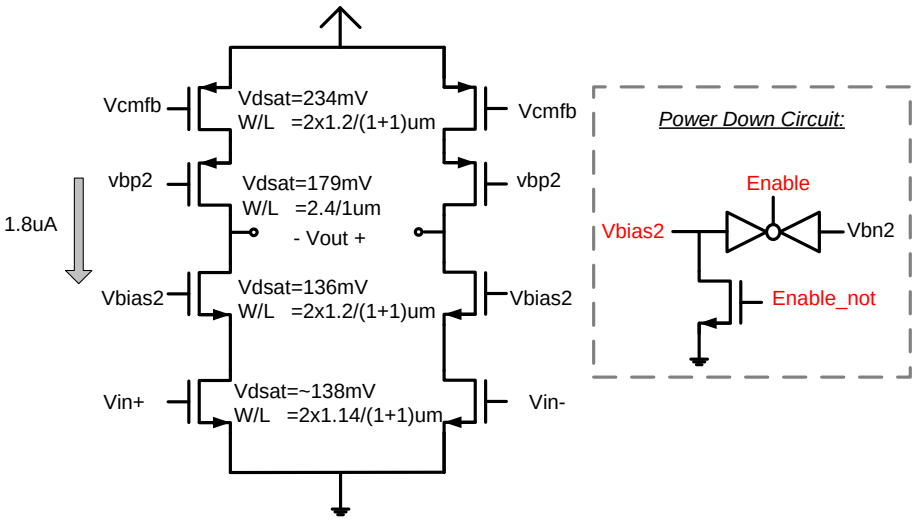


Figure 5.5: Stage 2 Opamp

Table 5.2: Stage 2 Opamp Specifications

Specification	TT/1.8V/80°C	SS/1.6V/125°C	FF/2.0V/0°C	Monte-Carlo Standard-Deviation (σ)
βf_t (MHz)	21.7	18.4	27.1	0.42
PM (°)	79.2	79.2	79.8	0.3
DC Gain (dB)	82.9	81.6	79.0	0.3
DC Current (μA)	3.6	3.4	3.7	0.11
DC Power (μW)	6.5	5.5	7.3	0.19

5.1.4 Conservative Design: High Phase Margin

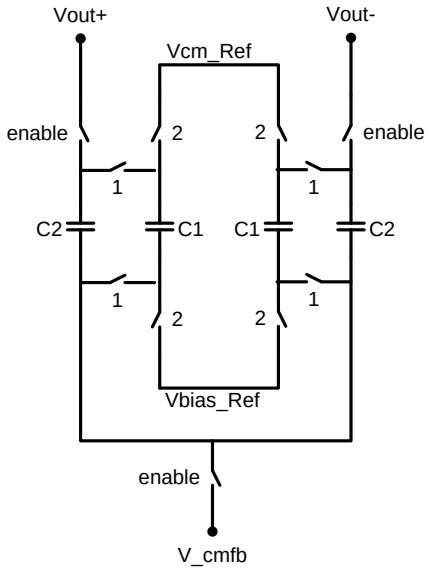
The above results show that both opamps were designed with quite high phase margin. Operating the input devices closer to subthreshold could reduce power by an additional 10-20% and maintain phase margins near 70°. As this was a first-cut design however, a conservative approach was taken.

5.1.5 Opamp Common-Mode Feedback (CMFB)

Switched-capacitor CMFB is the obvious choice when dealing with traditional SC circuits and was used for both opamp stages. Its main benefit is its lack of static power consumption. In simulation, the CMFB circuit was verified as being very stable and able to correctly startup circuits. Therefore there was no need to reduce the loop gain or add compensation. As shown in Figure 5.6, the CMFB circuits were disconnected when the circuits were powered down.

5.2 Dynamic Comparator

A single-bit quantizer requires only a single comparator. A single-stage dynamic comparator as used in [6] was chosen for power efficiency. Offset in a single bit quantizer only results in some DC offset in the ADC, and does not otherwise degrade its performance. This combined with the low sample rate leads to quite lax comparator design constraints. The comparator has a (random) offset of approximately 9mV and latches in 2nS or 3nS in the SS corner. The



	C1=C2
Stage 1	100fF
Stage 2	20fF

Figure 5.6: Switched-Capacitor CMFB Circuit

comparator, as well as the following SR latch [22] are shown in Figure 5.7.

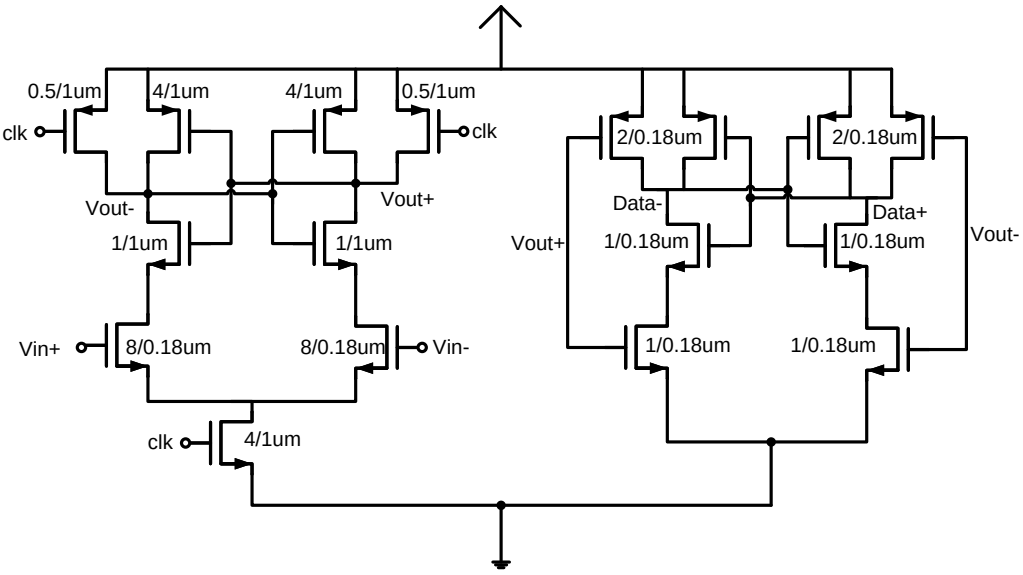


Figure 5.7: Comparator and SR Latch

As mentioned, due to the low clock rate, the comparator's speed was not crucial. However, due to the modulator structure, the comparator should latch within the non-overlap time to

Table 5.3: Comparator Specifications

Offset (Due to Mismatch)	9mV*
Latch Time	2nS Typical (3nS at SS/125/1.6V)
Average Power	$1.6\mu W$
Average SR Latch Power (5MHz)	60nW

*Offset is zero without mismatch. Value is Standard Deviation of offset in Monte-Carlo mismatch simulation.

avoid changing the feedback DAC signal during the integration phase. Simulations showed that the non-overlap time, combined with delays in clock buffers allowed sufficient time for the comparator and SR latch to latch.

5.3 Bias Circuits and Powering Up/Down

To avoid undesired transient behaviour in the opamps, and improve startup time [6], the bias circuits are powered on before the opamps preventing incorrect bias voltages from being applied to the opamps during startup. In addition, since the bias circuit consumes very little power, it can be powered on over a longer period of time without increasing power consumption significantly. Simulations showed that using this scheme, the opamps could power up in roughly 100 clock periods.

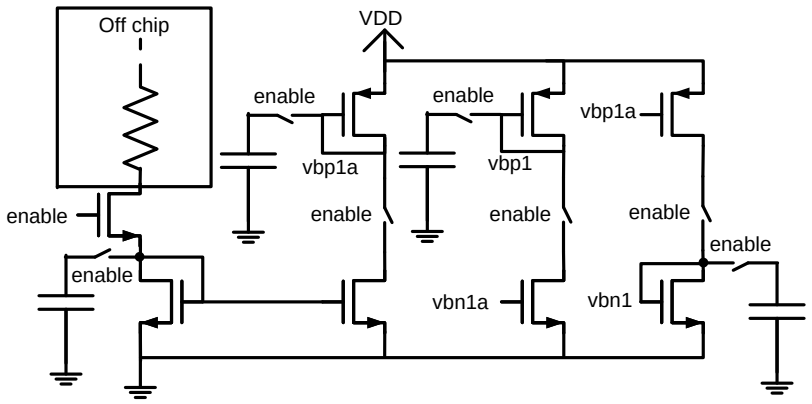


Figure 5.8: Bias Circuit Power Down Scheme

The only non-trivial aspect of designing the bias circuits was how to power them down, given that large decoupling capacitors are typically attached to bias voltage nodes to reduce noise. Similar to the opamps and in [1], series switches were used to turn off the bias circuits. This allows all current consumption to be cut off, without having to directly ground any bias nodes. In addition, the large decoupling caps were disconnected from the circuit when powered off. In simulation, this reduced the size of voltage transients during bias startup as the decoupling capacitors are not completely discharged when the circuit is off. In reality though, this might not have any benefit as over long periods of time, the capacitors might discharge due to leakage.

Large device lengths were used to reduce bias power consumption. This came at the cost of considerable area, but was necessary to prevent bias power from becoming a significant portion of overall power consumption.

5.3.1 Power Down of Off-Chip Bias Circuit

As shown in Figure 5.8, the master bias current from off-chip is also powered off. This is necessary to maintain power scaling, since any static power dissipation would lead to a fixed minimum power consumption. In this case, it would limit power scaling to approximately 100 times reduction, since the master bias current accounts for approximately 1% of the total analog power.

However, due to large pad and packaging capacitance and the low bias currents used, it may be problematic to power down the master bias circuit. The 200nA master bias current requires an off-chip resistance of approximately 5MOhm. Assuming a pad capacitance of 1pF, this leads to a time constant of 5uS, or 25 clock periods. This makes it possible to power of the bias circuit in a reasonable amount of time. However additional capacitance can be problematic, and no off-chip decoupling capacitors can be used.

5.4 Test Circuits: Analog Mux (Multiplexer)

Analog muxes were used to allow measurement of various DC levels during testing. A simple "T" configuration was used to isolate mux channels that are not in use (see figure 5.9). 4-bits of programmability were used to select between up to 16 sets of analog nodes.

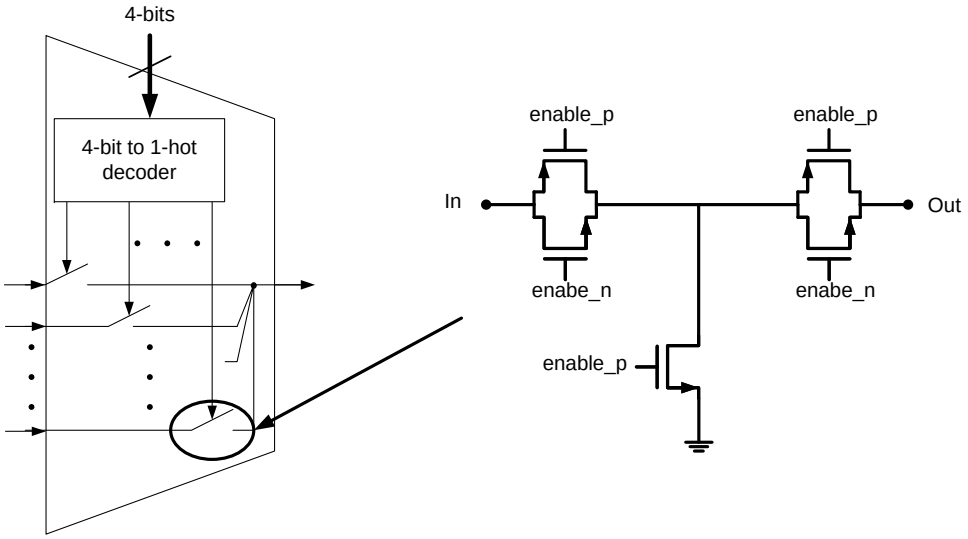


Figure 5.9: Analog Mux

5.5 Clock Phase Generation

All chopper clock and non-overlapping switched-capacitor (SC) clock phases are generated from a single 5MHz clock assumed to have a 50% duty cycle. While the SC clock phases are generated directly from the input clock, the chopper clock requires a clock divider to output a half-rate clock. Both the SC and chopper clocks consist of 2 non-overlapping phases with delayed phases to suppress input-dependent charge injection. The timing between the chopper and SC clock phases is not crucial. For example, the chopper clocks' rising edges need not coincide with the rising edges of the SC clocks. The two sets of clocks could therefore be generated by two identical, independent circuits, except that the chopper clock uses a divided clock.

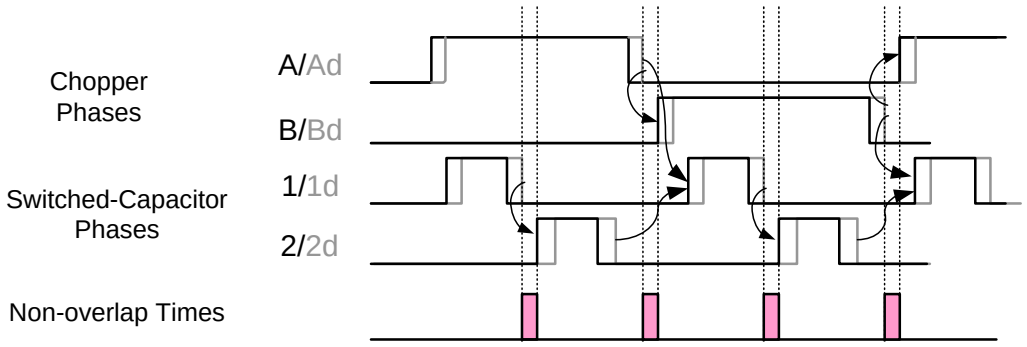


Figure 5.10: Clock Phases

There is however, a possible case which could cause the circuit to malfunction. In Figure 5.10, if clock 1 rises before A has fallen, this would lead to cross-sampling between the positive and negative outputs of the stage 1 integrator by the second stage. This case never occurred in simulation. and would only be possible with some extreme skewing of clock signals. However, to guarantee that this could not occur, a single latch was used to trigger the rising edge of clock 1 from the falling edge of the chopper clock. Figure 5.11 shows both clock generators.

5.5.1 Power Consumption

Estimated power consumption increased dramatically from $18\mu W$ before, to well over $30\mu W$ after parasitic extraction using Diva software. Compared to the small size of the switches, the overall dimensions of the ADC and length of clock wires were quite large, making wiring parasitics large compared to the switch capacitance. To combat capacitance between adjacent clock lines, the minimum distance between clock lines was increased, but could not be further increased due to need for more area. This combined with the use of a relatively high voltage supply contributed to high power consumption in the clock circuits.

5.5.2 Local Buffering (Not Used)

As an additional note, local clock buffers were not used. Local buffers might be used to improve signal rise times going into switches, or for example, invert clocks so that positive and negative clock lines are not required. Extracted simulations showed that buffering or inverting clocks

locally did not improve and actually worsened power consumption, meaning that the power of the additional buffers canceled out the benefit of fewer clock lines. It also did not seem to impact modulator performance. Avoiding local buffers also has benefits, including guaranteeing that non-overlap times are preserved since all buffers are within the clock generator loop. Furthermore local clock buffers may also lead to increased substrate noise by injecting large currents close to the switches which carry sensitive analog signals. For these reasons, local clock buffers were not used.

5.6 Total Power Consumption of Delta-Sigma Modulator

Table 5.4 shows the total simulated power consumption of the Delta-Sigma modulator designed. Of note is the high proportion of power dedicated to simple clock buffering. This high digital circuit power is a key motivating factor for using low supply voltages since dynamic digital power scales with Voltage-squared.

Table 5.4: Simulated Power Consumption

Component	Power (μW)
Stage 1 Opamp	19.8
Stage 2 Opamp	6.5
Comparator + SR Latch	1.6
Bias	2.0
Clock Gen. + Buffers	38 (post-extraction)

5.7 Delta-Sigma Modulator Simulations

The Delta-Sigma modulator was simulated extensively. As mentioned, simulations were conducted using an OSR of 256 to reduce simulation time. In addition, sweeps of input amplitude were not done due to excessive simulation time. Simulations were conducted at the targeted input level of 400mVpp differential.

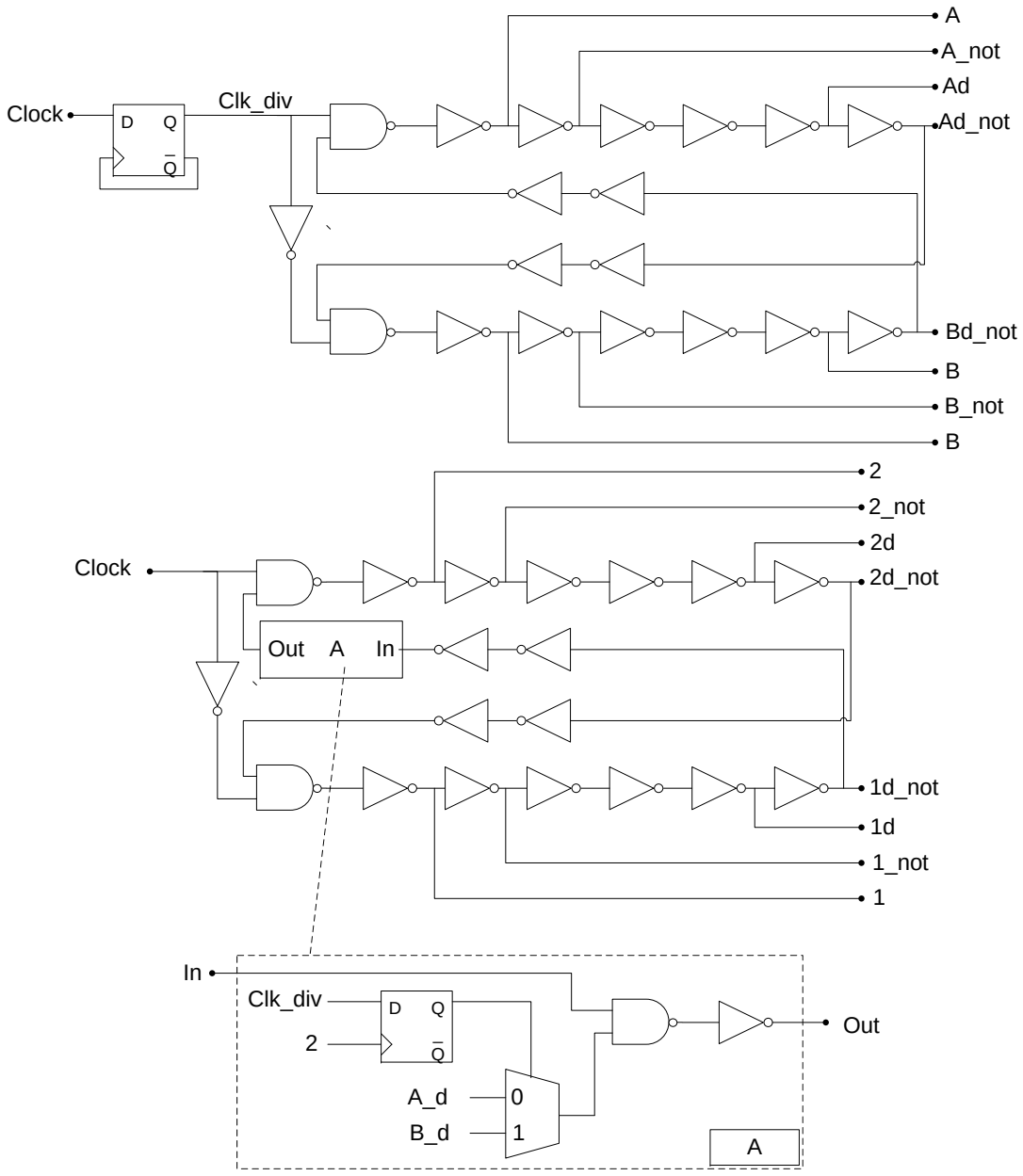


Figure 5.11: Clock Generator

The following simulations were conducted to verify correct circuit operation under the following conditions:

- Nominal conditions TT/80°C/1.8V
- Worst case corner SS/125°C/1.6V
- Worst case mismatch-manually adding 2-3σ Vt mismatch in all differential circuits. (Monte-carlo simulation time would be excessive.)
- Including post-layout extracted parasitics.

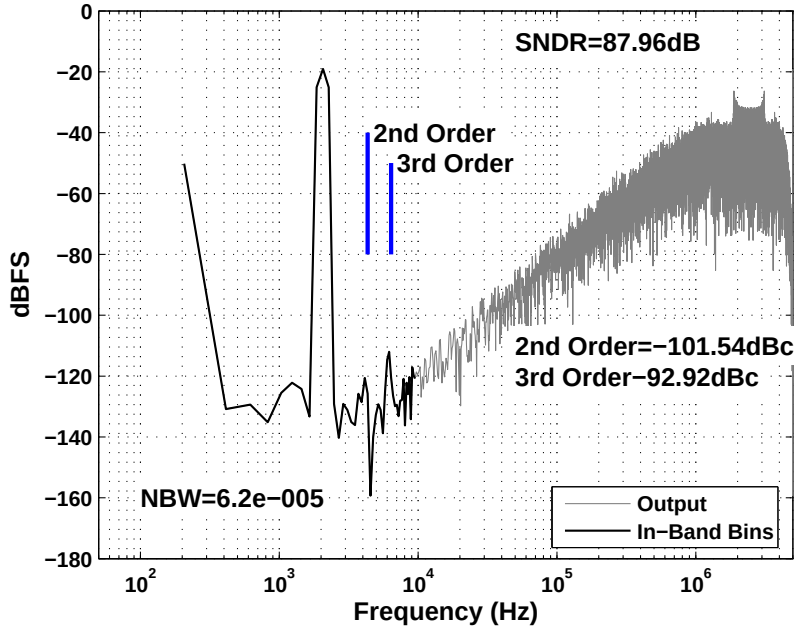


Figure 5.12: Post-Extraction Simulation at Worst Case SS/125°C/1.6V

5.7.1 Verification of Noise Level

Using Spectre PSS and Pnoise simulation, the input noise of the first stage integrator was simulated. Since second stage noise should be severely attenuated, only the first stage noise was simulated. Using PSS simulation, the effect of chopping can be simulated.

Simulations provide the in-band noise power spectral density shown in Figure 5.15. Mulitplying by the effective noise bandwidth and dividing as in Equation 5.5, gives the total RMS

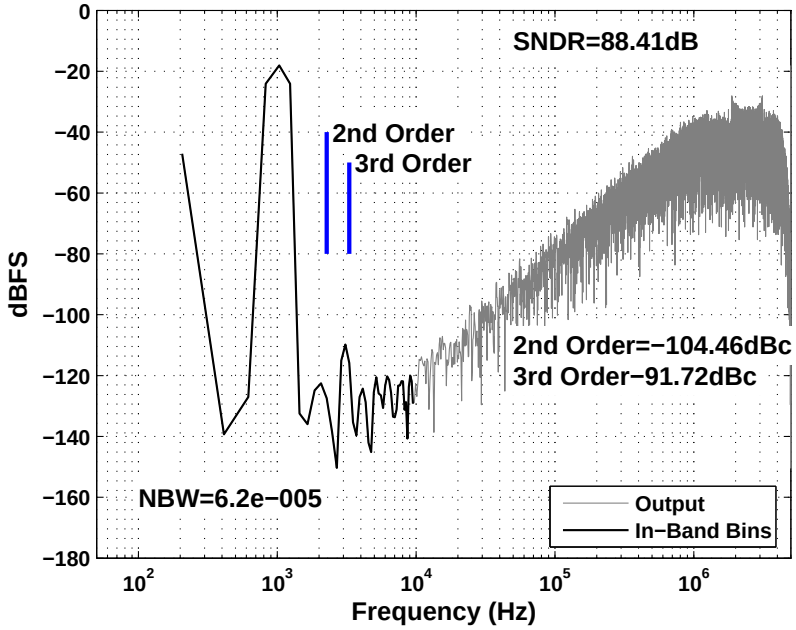


Figure 5.13: Simulation With Worst-Case 2-3σ Vt Mismatch

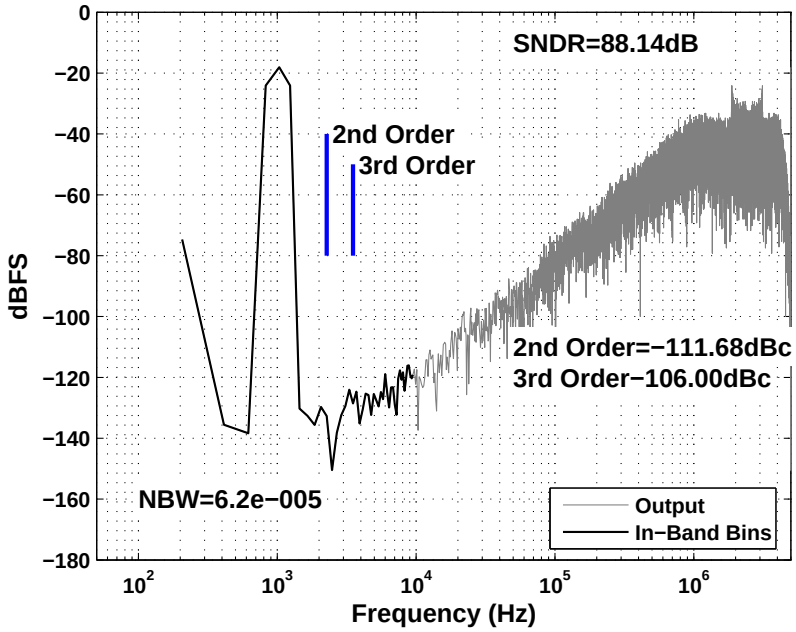


Figure 5.14: Partially-Extracted Simulation at Typical TT/80°C/1.8V

noise. Since the thermal noise floor is flat within the signal band, one can simply divide the noise by the OSR to get the in-band RMS noise. As discussed previously, the bandwidth to be used is the integrator loop bandwidth, which was simulated as 30MHz.

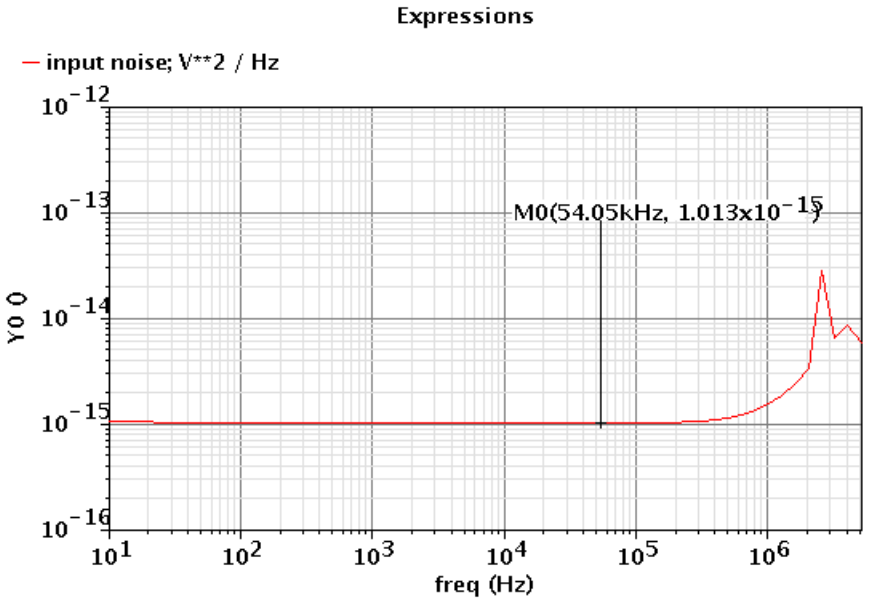


Figure 5.15: (Input-Referred) Chopped Noise Spectrum

Total Noise With Chopping:

$$V^2_{rms,in-band} = V^2_N(f) \cdot \frac{\pi}{2} \cdot f_{3dB} \cdot \frac{1}{OSR} \quad (5.4)$$

$$= 1 \times 10^{-15} \cdot \frac{\pi}{2} \cdot 30 \times 10^6 \cdot \frac{1}{1500} \quad (5.5)$$

$$= 3.1 \times 10^{-11} V^2 \text{ , 1.77dB worse than target of } 2 \times 10^{-11} \quad (5.6)$$

The above simulation predicts noise roughly 50% higher than targetted. Simulator noise summaries indicate that the analysis of the integration phase may be overly simplistic. Although the noise of the opamp itself does not appear to be higher than expected, the opamp contributes roughly 50% more noise than predicted based on the simplified analysis. In addition, switches that were assumed to contribute negligible noise due to their small resistance such as the input chopper switches, still appear to contribute, adding roughly 20% to the total predicted noise floor.

As an additional test, a Folded-Cascode opamp achieving similar distortion performance was simulated for noise. In line with the results of section A.1.3, the use of a Folded-Cascode opamp increases total noise by more than 70% or 2.3dB compared to the opamp used in this design.

5.7.2 Noise without Chopping

Without chopping, the presence of flicker noise is evident as shown in Figure 5.16. Unlike thermal noise, which must be integrated over the entire bandwidth, flicker noise does not fold back in-band with sampling. Therefore the noise contribution of flicker noise is found simply by integrating over the band of interest. In this case, the noise was simulated from 10Hz to Fs/2/OSR=1.67kHz.

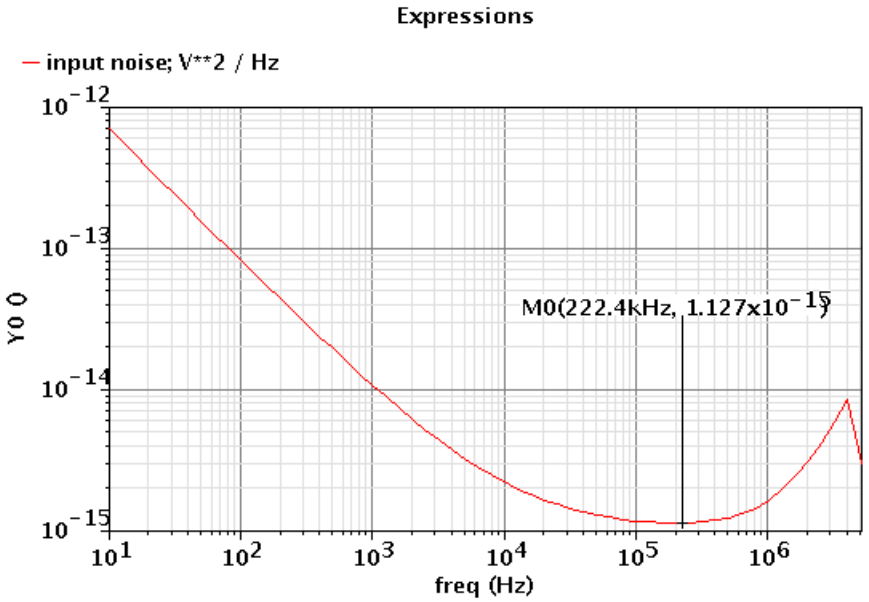


Figure 5.16: (Input-Referred) Noise Spectrum Without Chopping

Total Noise W/O Chopping:

$$V^2_{rms,in-band} = V^2_{N,Thermal}(f) \cdot \frac{\pi}{2} \cdot f_{3dB} \cdot \frac{1}{OSR} + \int_{10Hz}^{1.67kHz} V^2_{N,Flicker}(f)df \qquad (5.7)$$

$$= 1.13 \times 10^{-15} \cdot \frac{\pi}{2} \cdot 30 \times 10^{6} \cdot \frac{1}{1500} + 1.36 \times 10^{-10} \quad (5.8)$$

$$= 3.5 \times 10^{-11} + 1.36 \times 10^{-10} \quad (5.9)$$

$$= 1.7 \times 10^{-10} V^2 \text{ , roughly 7.4dB worse than Chopped} \quad (5.10)$$

5.7.3 Simulated Performance Summary: Delta-Sigma Modulator

Given the above simulation results, the expected performance of the Delta-Sigma modulator alone is summarized in Table 5.5.

Table 5.5: Simulated Specifications of Delta-Sigma Modulator (OSR=1500)

Supply Voltage	1.8V
Input Common Mode	900mV
Reference Voltages	1.3V / 500mV
Maxmimum Input Swing	1.6Vpp diff.
Clock Rate	5MHz
Signal Bandwidth	1.67kHz
Total Analog Power	$30\mu W$
Digital Clock Power	$38\mu W$
SNR @ 400mVpp diff. input (Thermal Noise)	88.2dB
SQNR @ 400mVpp diff. input (Quantization Noise)	∼100dB
3rd Order distortion (Typical)	<-100dBc

5.8 Digital Circuits and Post-Filter

5.8.1 Post-Filter

The 2 post-integrator stages were synthesized from Verilog using Synopsys Design Analyzer using TSMC "black-box" logic cells. This was done for simplicity rather than power efficiency. The synthesized design was clearly not optimal, using many full-adder circuits where they could be avoided. A careful manual design using the same black-box cells could likely reduce power

consumption by some margin. However, time did not allow for the design and verification of a hand design.

The post-filter's registers were designed to prevent possible bit-overflow at the chosen OSR. This was done assuming a comparator output stuck at 1 and calculating the resultant, maximum integrator values. Under normal operation, such a condition could never arise and the registers are therefore over-designed somewhat. To produce a more optimal filter design, simulations could be used to determine the maximum expected integrator values. The filter consumes $38\mu W$ in simulation.

Note: It was not discovered until well after tape out that the filter circuit is not properly powered down. Due to a late modification, the clock driving the filter circuit is never powered off, meaning that certain flip-flops continue to operate. ***As a result, the filter's power consumption does not scale with frequency.***

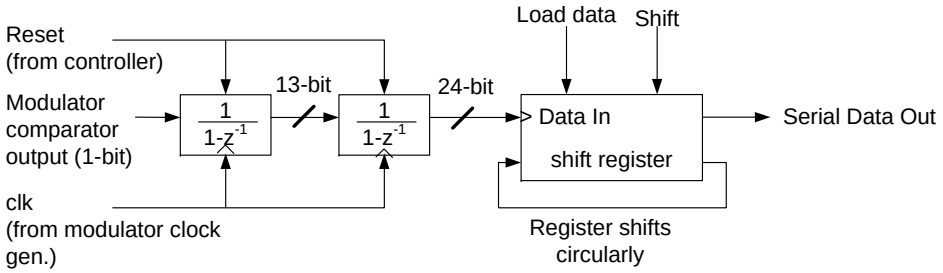


Figure 5.17: Filter

5.8.2 Serial Output

To more efficiently use the amount of available output pins, the filter output contains a shift register to enable serial output of the digital data using a single output pin. The loading and shifting of the shift register depends on outputs from the on-board digital controller and occurs during each reset-phase. In case of difficulty reading out the data, the shift register shifts circularly to allow redundant/repeated outputs.

5.8.3 Power Down Controller

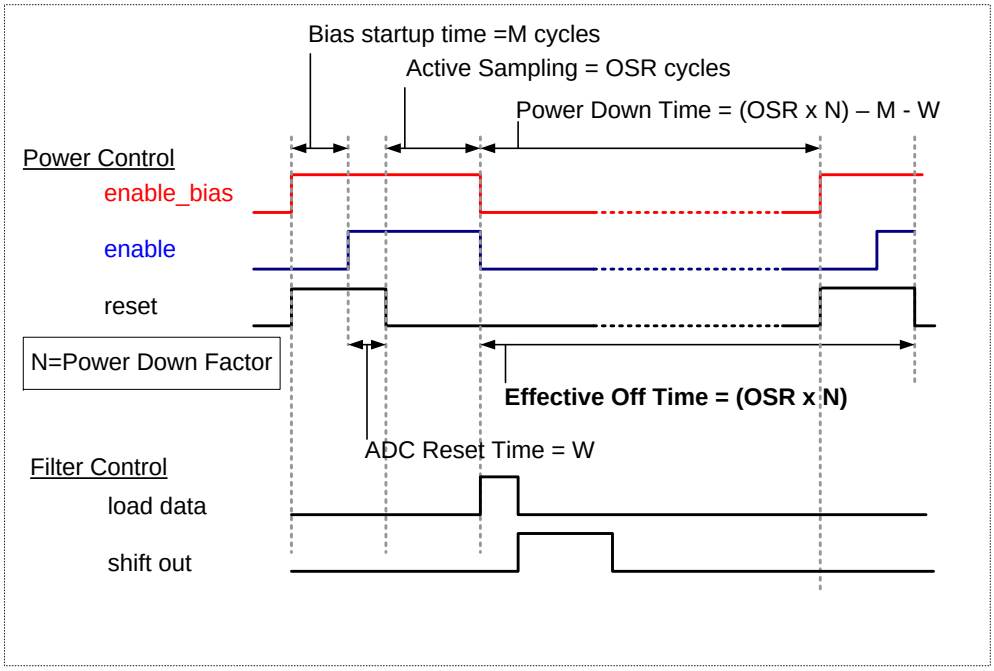


Figure 5.18: Controller Outputs

The on-board digital controller powers the Delta-Sigma modulator on and off and resets the integrators. In addition, it controls the serial output of the shift-register. For flexibility in testing and debugging, the controller was designed to operate at the full clock rate. As a result, the controller has to count up to a maximum value of OSR x PowerDown, which requires a 23-bit register. Operating at full-rate, the controller consumes excessive power. The controller may also operate from a divided clock to reduce its power consumption. In this case, the controller requires much fewer bits to operate. As a result, the controller consumes more power than would be necessary if designed solely for use with a divided clock.

Figure 5.18 shows the control signals generated by the controller. The length of each phase of operation, e.g. bias startup time, reset time etc are specified by variables stored in a shift register loaded from off chip. The controller was designed and simulated using ModelSim and again synthesized using TSMC black-box logic cells.

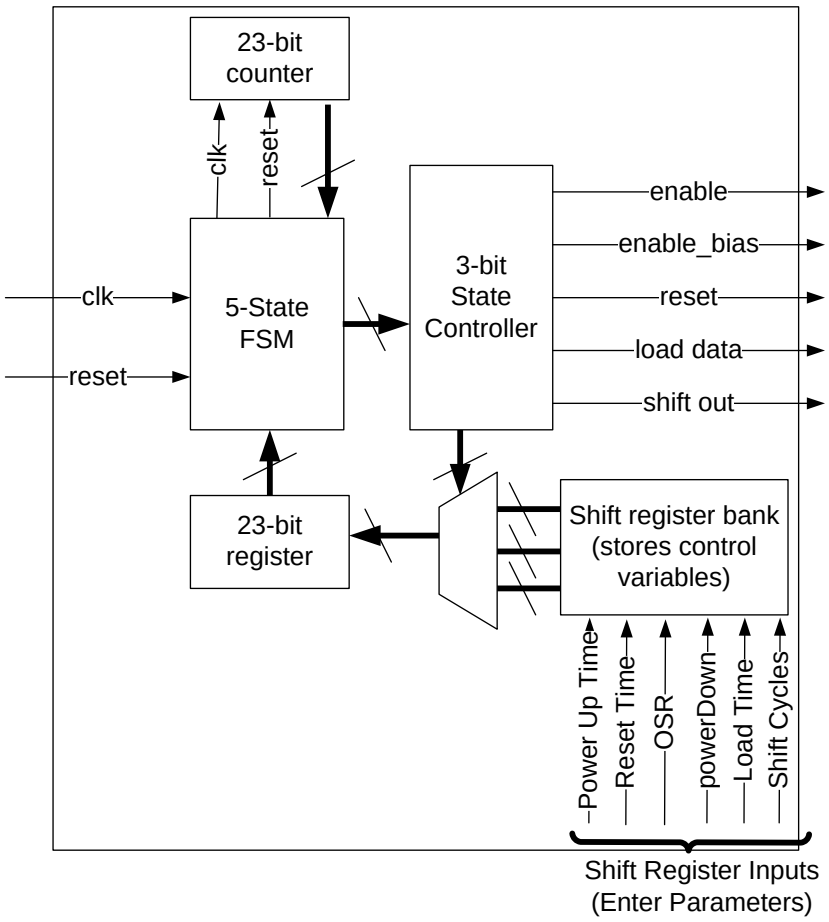


Figure 5.19: Controller Overview

5.8.4 Operation with Divided Clock

As mentioned, to save power the controller can be operated using a divided clock. A chain of flip-flops divides the clock by 128, therefore reducing the controller power by approximately 128. In this mode of operation, the controller power is dominated by the divider chain and clock buffering. Using a divided clock, the simulated power consumption was still quite high at $4.3\mu W$.

5.9 Complete Incremental ADC System

The complete Incremental converter including accompanying digital circuits was integrated together. Some additional signal MUX circuits were used to allow for increased testability.

Some circuit programming options include:

- Option to bypass PGA input stage and take input directly from off-chip
- Option to bypass on-chip controller with off-chip control signals
- Option to bypass post-integrators and carry out filtering off chip, e.g. in Matlab
- Option to operate controller from divided (by 128), or full-rate clock

In addition, the system supplies control signals as well as the chopper clock to the input PGA. A divider chain allows the PGA chopper clock to operate at Fs/2, Fs/4, Fs/8 or Fs/16. The complete system is shown in Figure 5.20.

5.10 Integration with PGA

As discussed, the Incremental data converter designed in this work is designed to operate with a programmable gain amplifier input stage (PGA) designed in [1]. The PGA was designed to provide 90dB SNR at its output, for an output signal with 400mVpp differential swing. Combining this with the designed ADC, also targeted at 90dB (although achieving slightly less in simulation), should provide roughly 86dB, or 14-bit combined SNR.

The PGA uses a cascade of three gain stages using 2-stage opamps in feedback. Depending on the gain, the input is applied through all three or none of the gain stages achieving gains of 2,4,10 and 1 if the entire system in bypassed. The system achieves power scalability based on input amplitude using the input gain select. In the highest gain setting, for example, the noise of the first stage is amplified by the subsequent stages. Therefore, the first stage is designed with the lowest noise, i.e. having the smallest resistors, and therefore the highest power opamp to drive them. As a result, the gain stage consumes less power for lower gains, and more when higher gain is required. The design is shown in Figure 5.21.

5.10.1 Verification of PGA and ADC Combined Operation

The PGA was originally fabricated and tested using an output buffer stage to drive off-chip capacitive loads. When integrated together with the ADC, the buffer is not required. The last

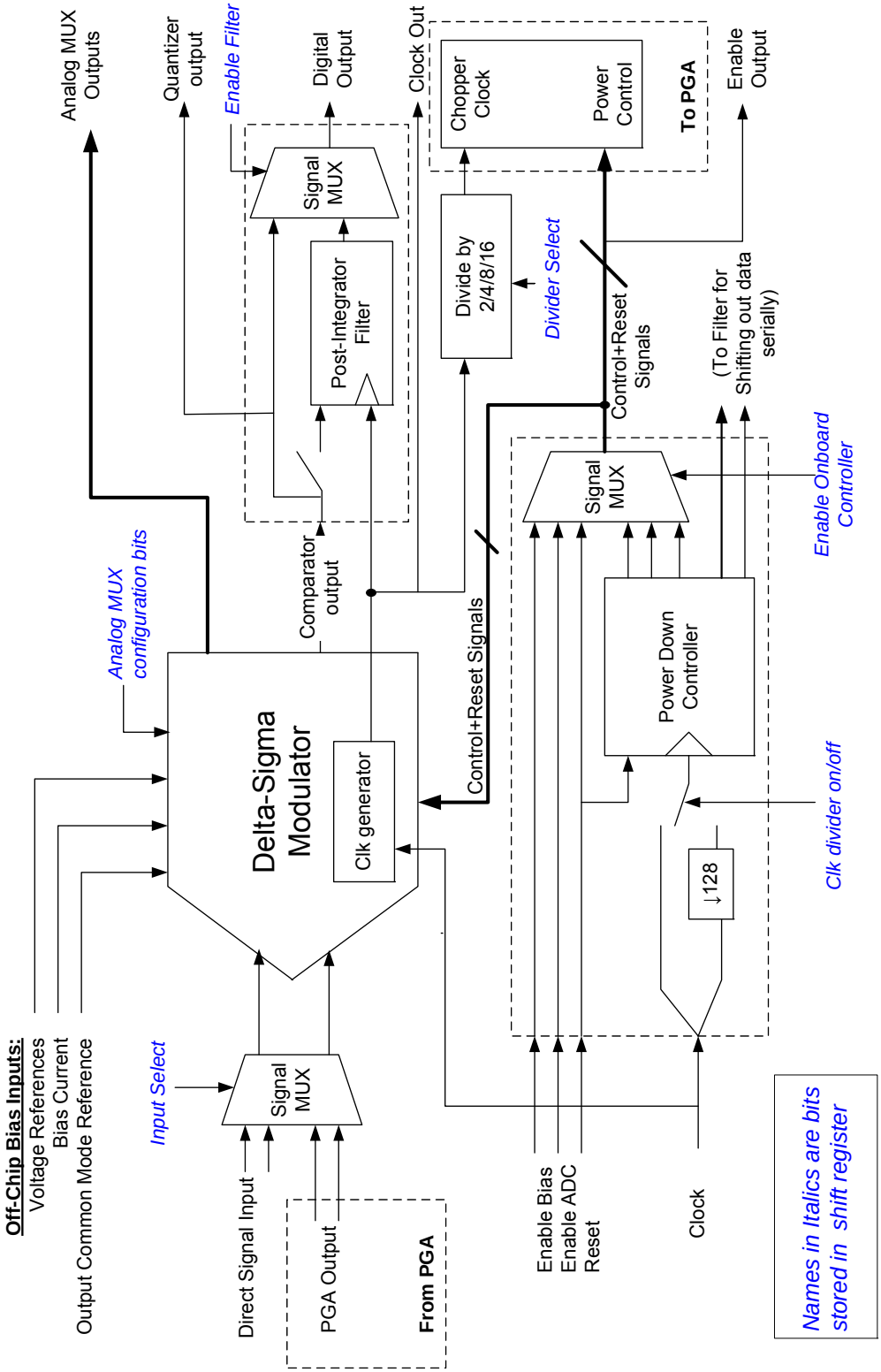


Figure 5.20: Complete System Design

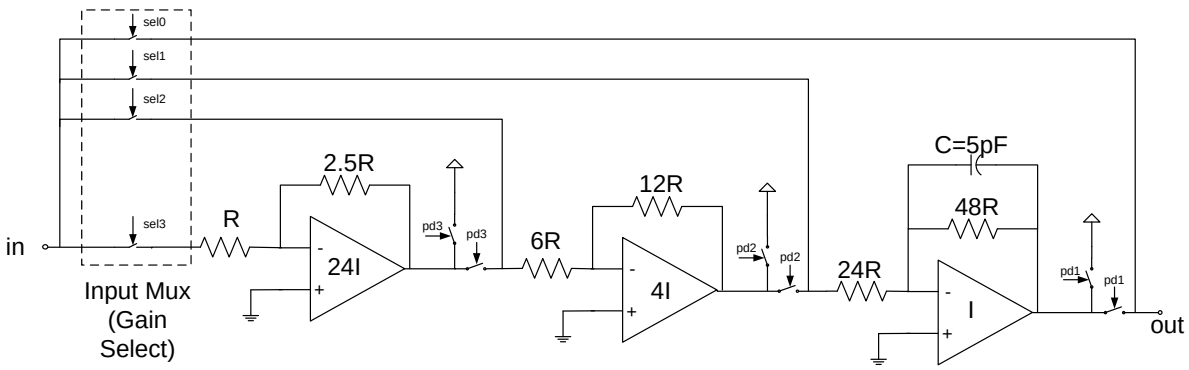


Figure 5.21: Input PGA Design from [1], R=10kΩ

opamp stage of the PGA was designed to drive the 500fF capacitive load presented by the ADC. Due to long simulation times, simulations with the complete ADC and gain stage were not practical. However, simulations were conducted to verify that the PGA could drive the ADC's input capacitance at the sample rate of 5MHz, without compromising linearity.

5.10.2 Excessive In-Band PGA Output Noise

Unfortunately, it was not noticed until the testing phase, that an oversight in the PGA design leads to excessive thermal noise at its output. Due to issues in testing, this excess noise was not obvious in the testing of the original PGA chip in [1].

From Figure 5.21, one sees that all circuit noise is filtered by an RC filter in the final gain stage. In [1], the total RMS output noise was therefore calculated using the equivalent noise bandwidth of a first order system:

$$\begin{aligned} V_{N,RMS}^2 &= \frac{1}{4\tau}\cdot\left[4KT(48R)+4KT(24R)\cdot\left(\frac{48R}{24R}\right)^2+4KT(12R)\cdot\left(\frac{48R}{24R}\right)^2\right. \\ &\quad +4KT(6R)\cdot\left(\frac{12R}{6R}\cdot\frac{48R}{24R}\right)^2+4KT(2.5R)\cdot\left(\frac{12R}{6R}\cdot\frac{48R}{24R}\right)^2 \\ &\quad \left.+4KT(R)\cdot\left(\frac{2.5R}{R}\cdot\frac{12R}{6R}\cdot\frac{48R}{24R}\right)^2\right] \end{aligned} \tag{5.11}$$

$$= \frac{KT(428R)}{\tau} \tag{5.12}$$

substituting $\tau = C \cdot 48R$,

$$= \frac{428 \cdot KT}{C \cdot 48} \tag{5.13}$$

$$\approx \frac{9 \cdot KT}{C} \tag{5.14}$$

Simple AC noise simulation confirms that this result is correct. Opamp noise, which was not considered is comparable, adding approximately 3dB to the RMS noise level in simulation. As the system was designed to be oversampled by 5000. The total noise was therefore calculated as:

$$\text{Total Calculated Noise After Oversampling } \approx \frac{9 \cdot KT}{C \cdot OSR} \tag{5.15}$$

Noise With and Without Aliasing

However, equation 5.15 above is an oversimplification. In real systems, thermal noise will have some finite bandwidth. When sampled, any out-of-band noise folds back in band, leading to a flat thermal noise floor. As a result, the result of oversampling is a straight division of the total RMS noise by the OSR. The effect is shown in Figure 5.22, for a first-order low-pass band-limited noise with flat PSD of S_N and equivalent noise bandwidth of $\frac{\pi}{2} \cdot f_{3dB}$.

From Figure 5.22, the in-band noise is calculated as:

$$\text{With Aliasing: } V^2_{N,RMS} = S_N \cdot \frac{f_{3dB} \cdot \pi/2}{f_S/2} \cdot \frac{f_S}{2 \cdot OSR} \tag{5.16}$$

$$= S_N \cdot \frac{f_{3dB} \cdot \pi/2}{OSR} \tag{5.17}$$

$$= \frac{\text{Total RMS Input Noise}}{OSR} \tag{5.18}$$

However, if the noise bandwidth does not exceed the sampling frequency f_S, the effect is not the same. As shown in Figure 5.23, if noise does not alias in band, the total in-band noise with oversampling is simply:

$$\text{Noise Without Aliasing: } V^2_{N,RMS} = S_N \cdot \frac{f_S}{2 \cdot OSR} \tag{5.19}$$

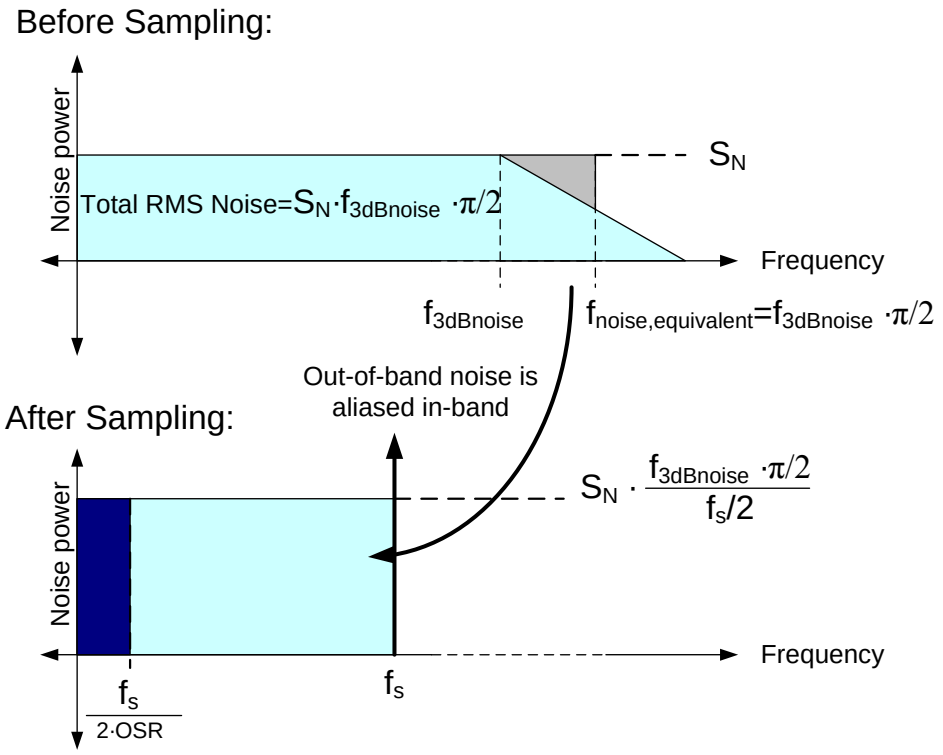


Figure 5.22: Effect of OSR on First-Order Band-Limited Noise With Aliasing

$$= S_N \cdot \frac{f_{3dB} \cdot \pi/2}{f_{3dB} \cdot \pi/2} \cdot \frac{f_S}{2 \cdot OSR} \quad (5.20)$$

$$= \frac{\text{Total RMS Input Noise}}{f_{3dB} \cdot \pi/2} \cdot \frac{f_S}{2 \cdot OSR} \quad (5.21)$$

$$= \frac{\text{Total RMS Input Noise}}{OSR} \cdot \frac{f_S}{f_{3dB} \cdot \pi} \quad (5.22)$$

Comparing the above to equation 5.18, one can see that if the sampling frequency f_S is greater than the 3dB noise bandwidth, equation 5.18 will underestimate the in-band noise by $f_S/f_{3dB}/\pi$.

Implications for PGA Noise

Unfortunately, in the PGA design of [1], the 3dB noise bandwidth of only 66kHz is much smaller than the targeted sample frequency of 5MHz. As a result, the in-band noise of the design was underestimated by $f_S/f_{3dB}/\pi$=24, or 14dB.

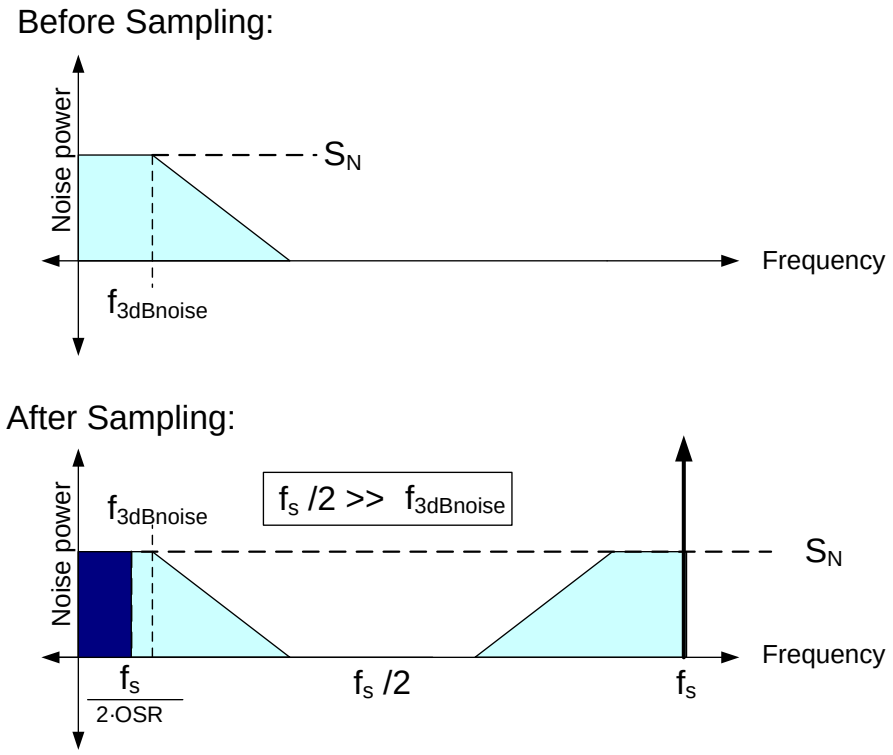


Figure 5.23: Effect of OSR on First-Order Band-Limited Noise Without Aliasing

This, combined with the added 3dB impact of opamp noise means that the expected output SNR of the PGA is only 73dB or just over 12 bits, not 90dB as was intended in the design.

Chapter 6

Experimental Results

The complete circuit designed in the previous chapter was laid out and fabricated in 0.18μm CMOS technology. This chapter describes the test results of the fabricated chip. First the Delta-Sigma modulator was tested to measure its basic performance including SNR, distortion and power consumption. Measured SNR was within 2dB of simulation results and while analog power consumption was within 1% of expectations, digital power consumption was roughly 31% higher than simulated. The Delta-Sigma converter is competitive with current state-of-the-art designs. Next, the Incremental converter including associated digital circuits was tested. The converter performance, including its effectiveness in power-scaled operation was measured. The SNR of the Incremental converter was slightly worse than expected compared to Delta-Sigma operation and degrades by several dB when powered down. While analog power was confirmed to scale as expected with frequency, digital power scaling could not be easily verified. Finally, the complete interface including the previously designed PGA was tested. As explained in the previous chapter, due to higher than desired noise, the PGA input noise appears to limit the resolution of the complete interface to roughly 12-bits.

6.1 Fabricated Chip

The complete Incremental data converter was integrated with the previously designed PGA and fabricated in 0.18μm TSMC CMOS technology with the MIM-Capacitor and deep N-

well options and standard top metal. The ADC occupies a core area of 0.7mm x 0.5mm = 0.35mm^2. Combined with the PGA, the complete interface occupies a core area of 1.4mm x 0.7mm=0.98mm^2. Including the pad-frame, the total area of the sensor interface is 1.8mm x 1.1mm=1.98mm^2. Testing was performed on a device in a CQFP44 package, using a custom PCB.

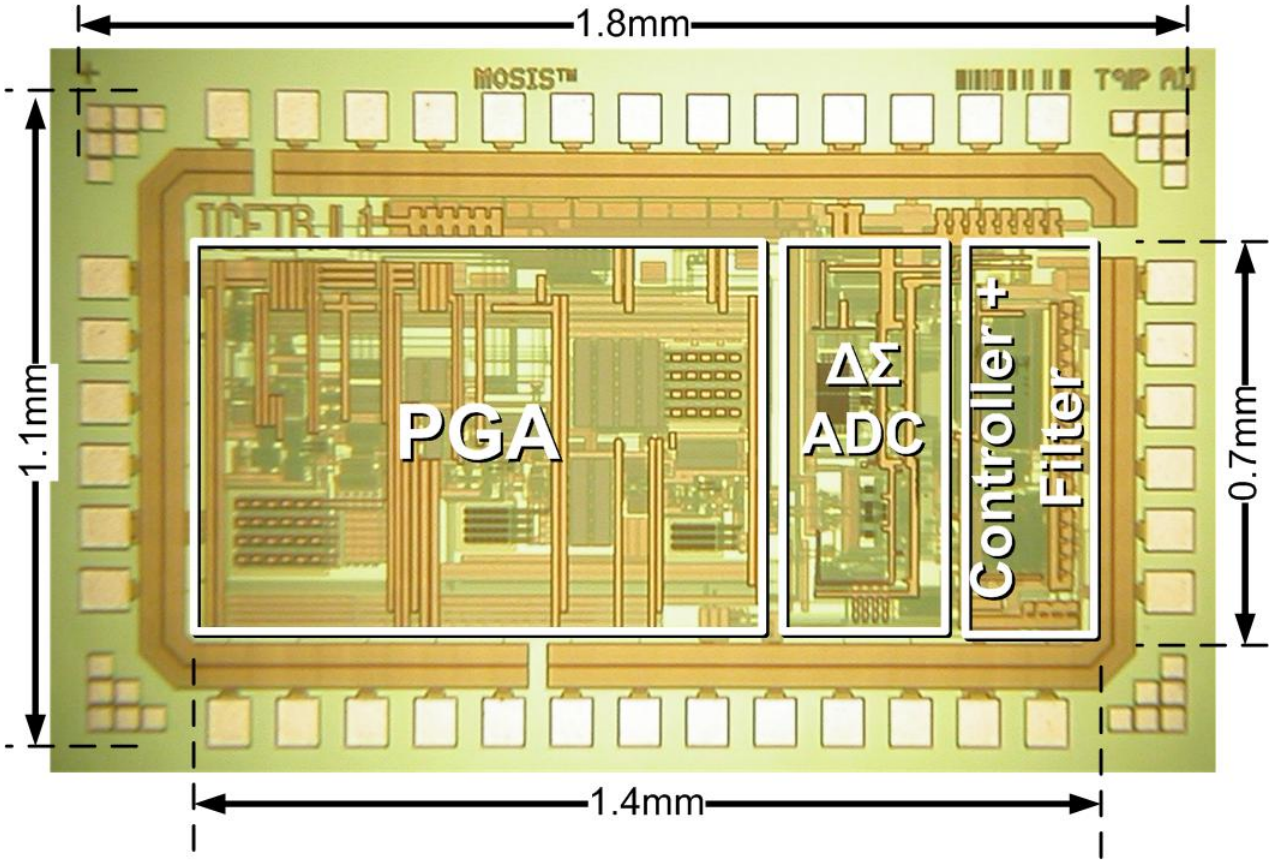


Figure 6.1: Complete Fabricated Chip

6.2 Test Setup

6.2.1 PCB

A 4-layer PCB was designed and fabricated. The PCB contained the following circuits:

- Voltage supplies using LM1117 linear regulators with adjustable output voltage. (PCB master power supply provided by Agilent E3620A Power Supply)

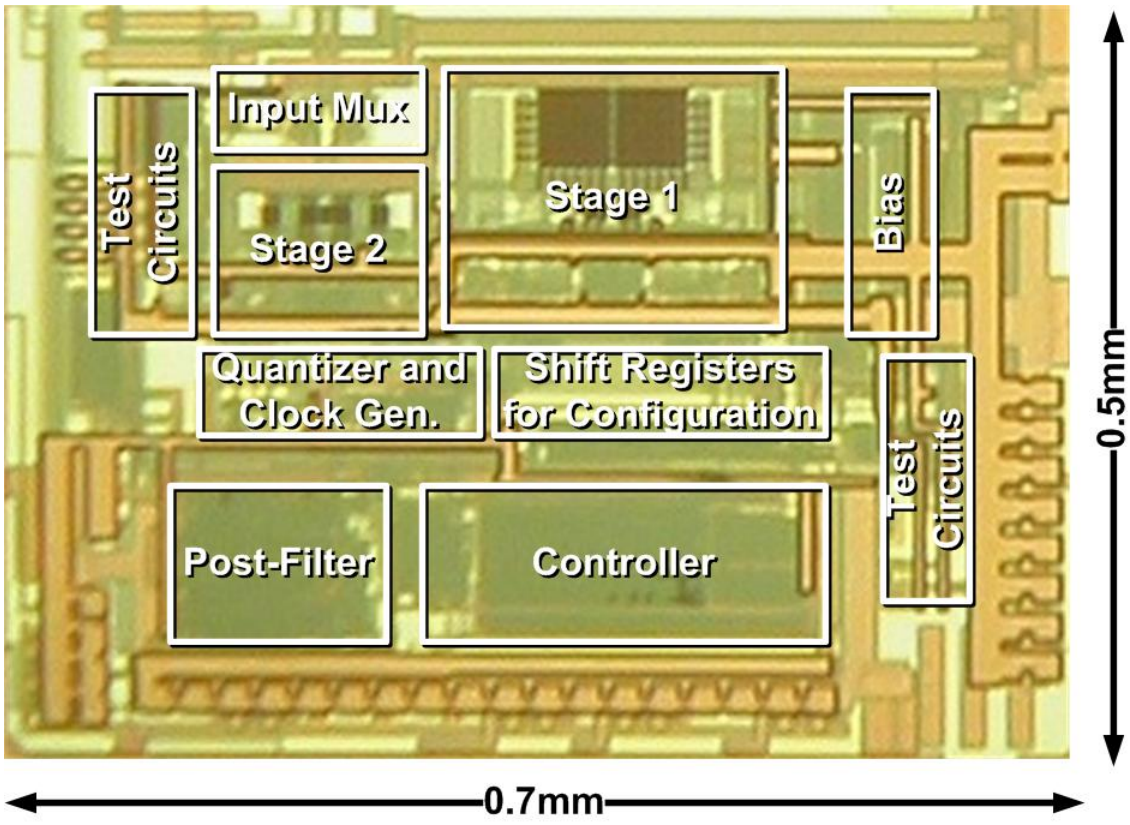


Figure 6.2: Cropped Image Showing Circuits Designed in This Work

- Bias current source using potentiometer and series resistor.
- DAC Voltage references using resistor dividers buffered by OPA364 opamps with large μF decoupling capacitors.
- Schmitt-Trigger buffers to supply and buffer digital input signals including clock and shift register inputs
- OPA364 Opamps with pA input bias current used in unity-gain feedback configuration to buffer analog mux outputs from chip

6.2.2 Test Equipment

Signal Source

Testing was performed using a Stanford Research DS360 low distortion function analyzer to mimic the sensor output that would drive the ADC in implementation. The function generator

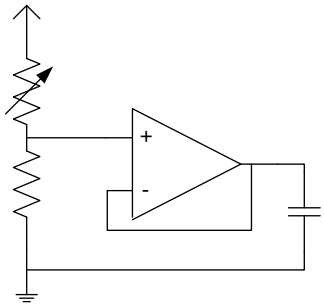


Figure 6.3: Off-Chip Voltage Reference

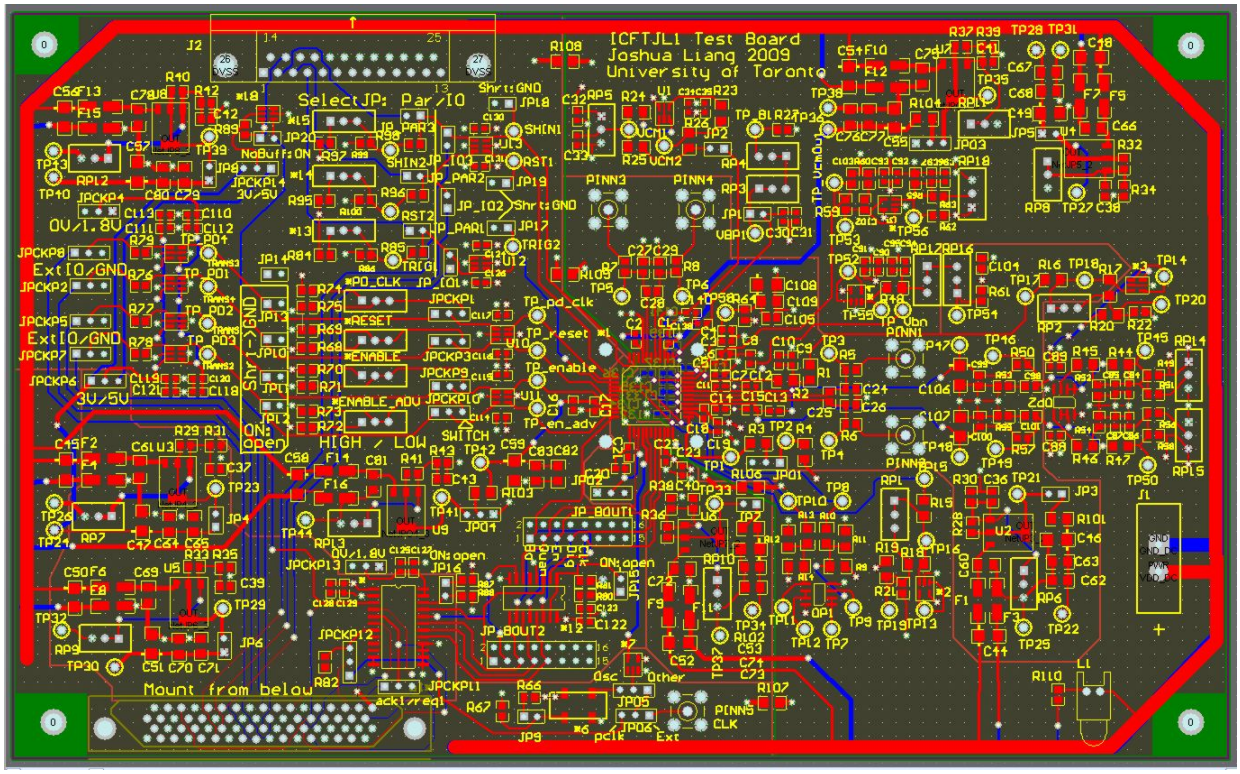


Figure 6.4: Custom-Designed PCB

has fully differential outputs and specified noise exceeds 14-bit performance [27]. In addition, a 100Ω resistor was placed across the signal input to provide a resistive load. 10nF capacitors were used to suppress the input resistor noise. The addition of the capacitors was found to improve SNR by 1-2dB.

Digital Input and Acquisition

A Sony/Tektronix TDS3052B Data Generator was used to supply a 0-1.8V square wave clock at 5MHz. Later, a 5MHz Crystal oscillator was used and was not found to have any impact on performance. The rise times going into the device under test (DUT) were determined however by a Schmitt-Trigger IC used to buffer the clock. A PC parallel port was used to program shift registers using the Data-Acquisition Toolbox in Matlab.

Digital output data was captured using a National Instruments NI-6534 Digital I/O PCI board installed in a PC, in conjunction with the NI-DAQmx C library and Matlab. The NI-6534 can capture data at up to 20MHz and has on-board memory. The NI-DAQmx software allows burst data transfer to the PC. At 5MHz, data could be captured continuously without interruption (for 20 minutes or more in testing).

Power Measurement

The fabricated chip uses separate supplies for Analog and Digital power, allowing each to be measured independently. Average current was measured by measuring voltage across a 100Ω resistor at the voltage supply output using an Agilent 34401A multimeter. To subtract the power consumed by the large IO buffers used to drive off-chip loads with digital signals, the IO buffers could be disabled.

6.3 DC Characterization

The potentiometer on the PCB was adjusted to deliver 200nA±10% input bias current as assumed in simulation. The voltage supply was set to 1.8V±1%. Using the analog mux, the DC bias nodes voltages were measured. As mentioned, off-chip buffers were used to prevent loading of the sensitive analog nodes by the multimeter. As a result, the measured voltages had 1-2mV of measurement error.

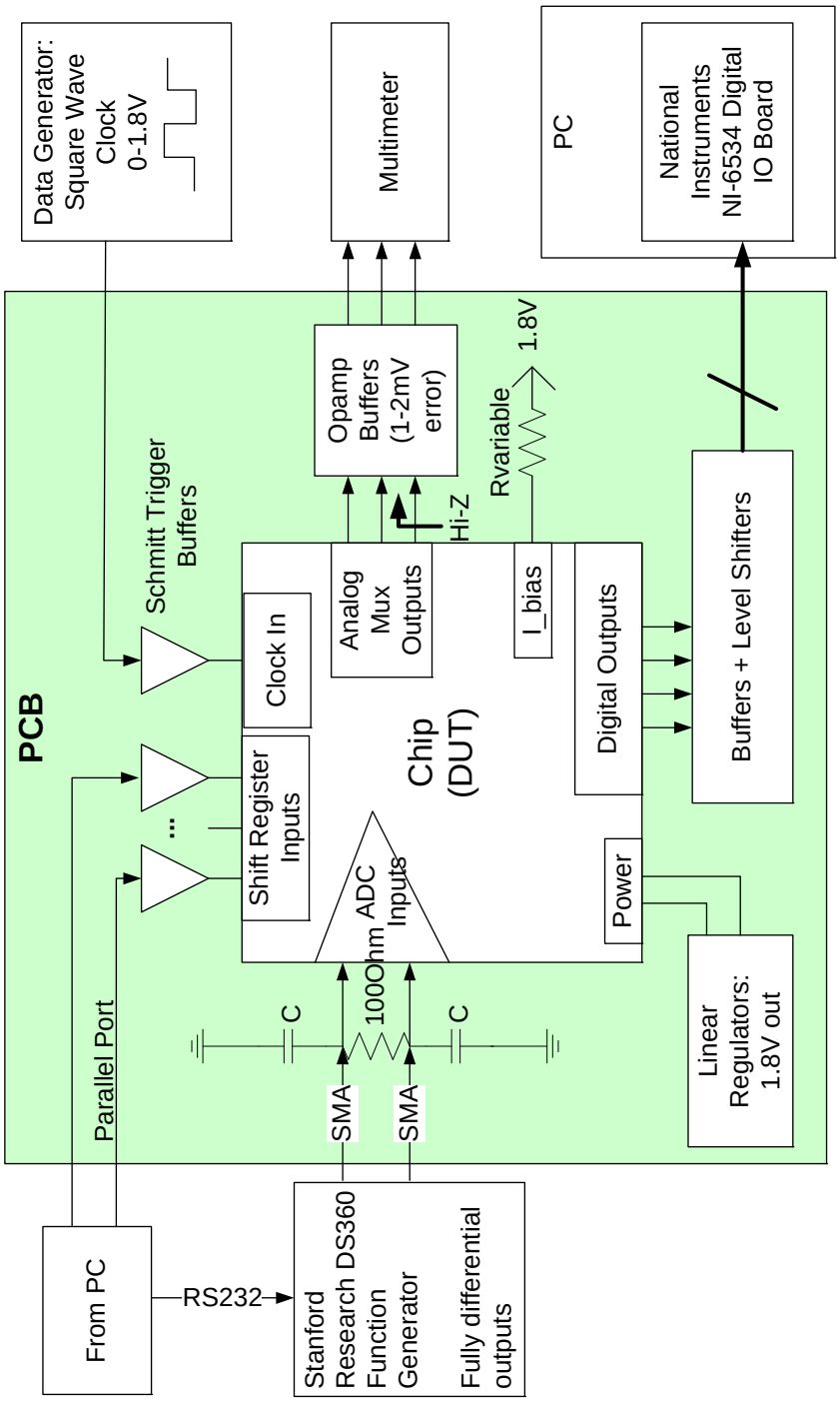


Figure 6.5: Simplified Test Setup

Table 6.1: Measured vs. Simulated DC Bias Voltages

Node Name	Simulated (1.8V/25C)			Measured (mV)	Description
	TT (mV)	SS (mV)	FF (mV)		
vbn1a	652	695	609	664	NMOS master bias
vbn1low	538	572	503	548	NMOS input
vbn2	729	776	684	741	NMOS cascode (stage 1)
vbn3	843	895	793	855	NMOS cascode (stage 2)
vbp2	745	698	792	787	PMOS cascode
vbp1	1137	1099	1175	1161	PMOS source

From Table 6.1, the fabricated chip appeared to be close to the SF process corner with NMOS being closer to Slow and PMOS being closer to Fast. At this corner, performance should be quite close to typical, with only a slight degradation in circuit bandwidth.

6.4 Performance Measurements in Delta-Sigma Mode

To assess the fundamental performance of the ADC, tests were conducted first in Delta-Sigma mode. This meant that the raw quantizer bits are captured and that the modulator is never reset. To improve distortion performance up to the 1Vpp diff. input level, the reference voltage swing was reduced somewhat. In addition, the reference common mode was shifted up by 10mV, increasing the input bias level of both opamps by 10mV.

6.4.1 SNR Measurement: AC Power Line Harmonics

In calculating SNR, several sinusoidal noise signals were removed and their FFT bins were replaced with an average noise level. These signals either coupled in through the air or PCB, or were present in the signal generator output spectrum. They were present in the ADC output spectrum with no input, and were at fixed frequencies independent of the ADC clock frequency. It was therefore concluded that they did not come from the ADC itself.

The frequencies removed were at 60Hz, 120Hz, 180Hz, 240Hz, 70Hz, and 140Hz. While the 60Hz tone and its harmonics are undoubtedly related to AC power lines, the 70Hz noise may be from some of the test equipment or a display. Figure 6.6 shows an example output spectrum. As can be seen from the figure, these low-frequency tones appear unrelated to the input signal.

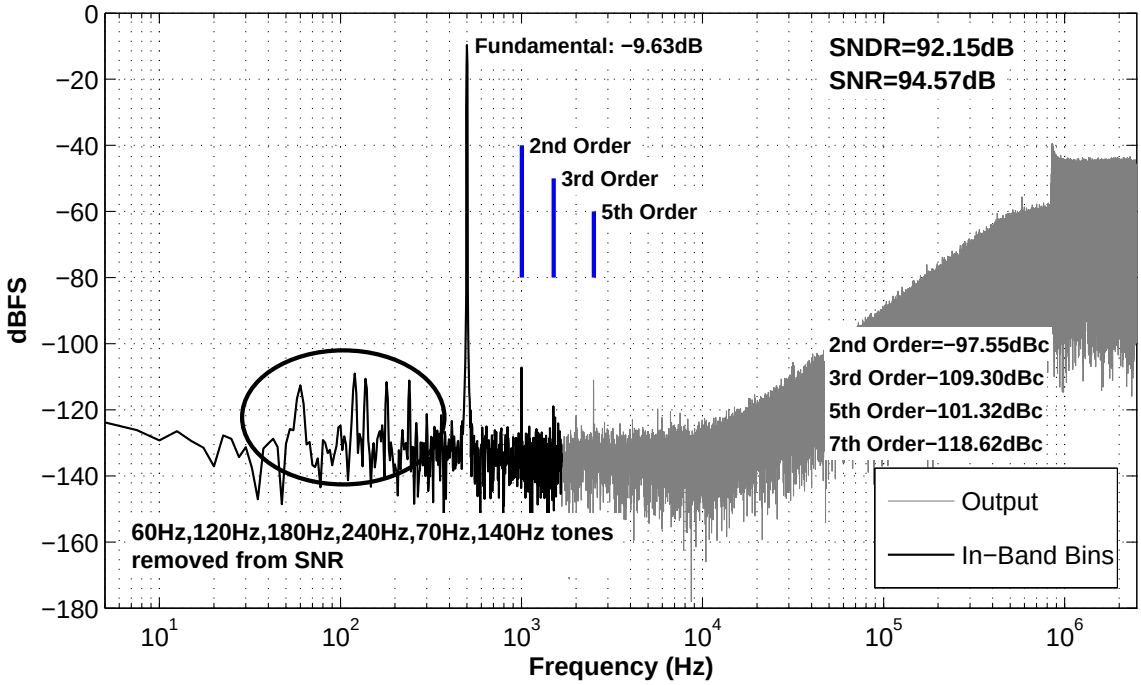


Figure 6.6: Example Output Spectrum Input at 500Hz, 990mVpp diff.

As an additional test, to verify that the above-mentioned tones were not from the DUT, the signal source (DS360 function generator) was connected directly to a Stanford Research Systems SR770m Spectrum Analyzer with differential inputs. The result shown in Figure 6.7 shows that 60Hz, and all of its harmonics are present, looking only at the signal source. Theses tones are therefore either present in the source's output, or are able to couple in through the cables. However, while the spectrum does show a harmonic near 140Hz at precisely 136Hz, the 70Hz signal seen in the ADC output is not visible. This tone might therefore originate from other sources such as the power supply used for the PCB. It was not possible to measure the signal spectrum directly at the ADC inputs due to a lack of available connections. Such a test

could be used to isolate the source of the remaining 70Hz harmonic.

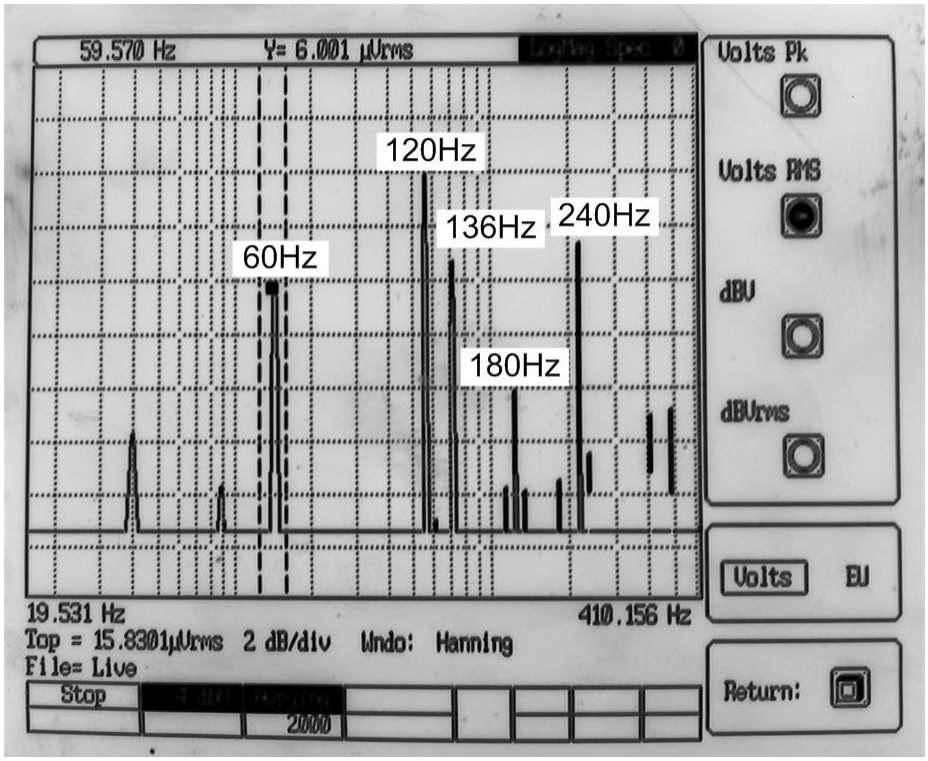


Figure 6.7: Spectrum Taken Directly From Output of DS360 Function Generator

Measured Using Stanford Research Systems SR770m Spectrum Analyzer

6.4.2 SNDR Measurement: Inclusion of Out-of-Band Harmonics

Depending on the input frequency used, several harmonics tend to fall out of band. However, due to an even noise floor up to approximately 10kHz, higher order harmonics were still visible and measurable in the spectrum. To calculate SNDR, all in-band harmonics were included. If falling out-of-band, **2nd, 3rd, 5th and 7th order distortion were still always included in distortion calculations**. 3rd and 5th order distortion terms tended to dominate the THD of the system.

6.4.3 Performance Results

Table 6.2 shows the simulated and measured results of the Delta-Sigma modulator. The key performance results include:

- **SNR:**

  SNR was worse by $\sim$ 2dB. Moving from the TT corner to SF alone, can increase simulated noise levels by approximately 13% or 0.53dB. In addition simulated noise levels still included assumptions about the equivalent noise bandwidth, which could have been underestimated. Aside from such errors, additional factors such as power supply and reference noise sources were completely ignored in calculations.

- **Analog Power:**

  Analog power consumption was increased by 10% over simulation, due to the 10mV change in the common mode of the voltage references. Without this change, analog power was roughly 30μW as expected.

- **Digital Power:**

  Digital power consumption was 31% higher than in simulation. This significant difference is likely related to a slow clock edge entering the ADC. The actual buffered clock entering the DUT had a significanly slower rise time than the 2nS assumed in simulation. This could lead to increased power consumption in the input clock buffers due to higher short-circuit current in the inverters. In addition, extracted parasitics may be have been underestimated, potentitally underestimating digital circuit power.

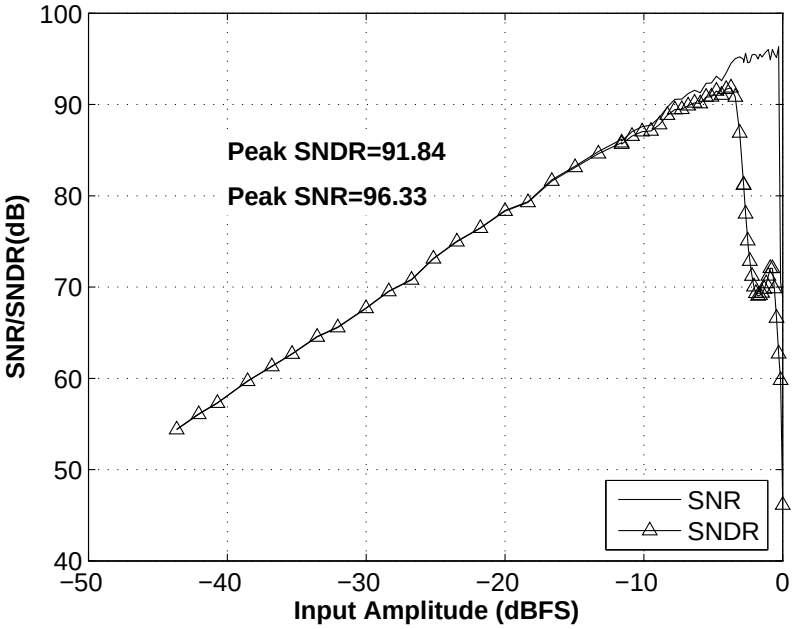
6.4.4 Effectiveness of Chopping

Figure 6.9 shows output spectra with and without chopping. With chopping disabled, noise clearly increased at low frequencies due to flicker noise as expected. SNR was roughly 10dB worse than the 86dB SNR achieved with chopping enabled at the same input level. Simulations predicted a degradation of 7.5dB without chopping.

6.4.5 Performance With Reduced OSR

The noise-shaping of the delta-sigma modulator means that a flat thermal noise floor is maintained up to roughly 10kHz of bandwidth. Increasing the ADC bandwidth only affects the off-chip decimation filter. The performance of the ADC designed here was measured, reducing

Figure 6.8: Measured Performance of Delta-Sigma (Input at 500Hz)



Input Level (pk-pk diff.)	SNR (dB)	SNDR (dB)
400mV	86.0	85.6
990mV	94.4	**91.8**
1.49V	**96.3**	62.7

Above results were averaged over 10 x 2 Million point FFTs.

Table 6.2: Measurement Results for Delta-Sigma Modulator (OSR=1500)

Parameter	**Simulated**	**Measured**
Supply Voltage	1.8V	1.8V
Input Common Mode	900mV	900mV
Reference Voltages	1.3V/500mV	1.29V / 530mV
Maximum Input Swing	1.6Vpp diff.	1.5Vpp diff.
Clock Rate	5MHz	5MHz
Signal Bandwidth	1.67kHz	1.67kHz
Total Analog Power	30μW	33μW
Digital Clock Power	38μW	50μW
SNR @ 400mVpp diff. input (Thermal Noise)	88.2dB	86dB
SQNR @ 400mVpp diff. input (Quantization Noise)	~100dB	not measurable
3rd Order distortion (Typical @ 400mVpp diff. input)	-100dBc	-102dBc

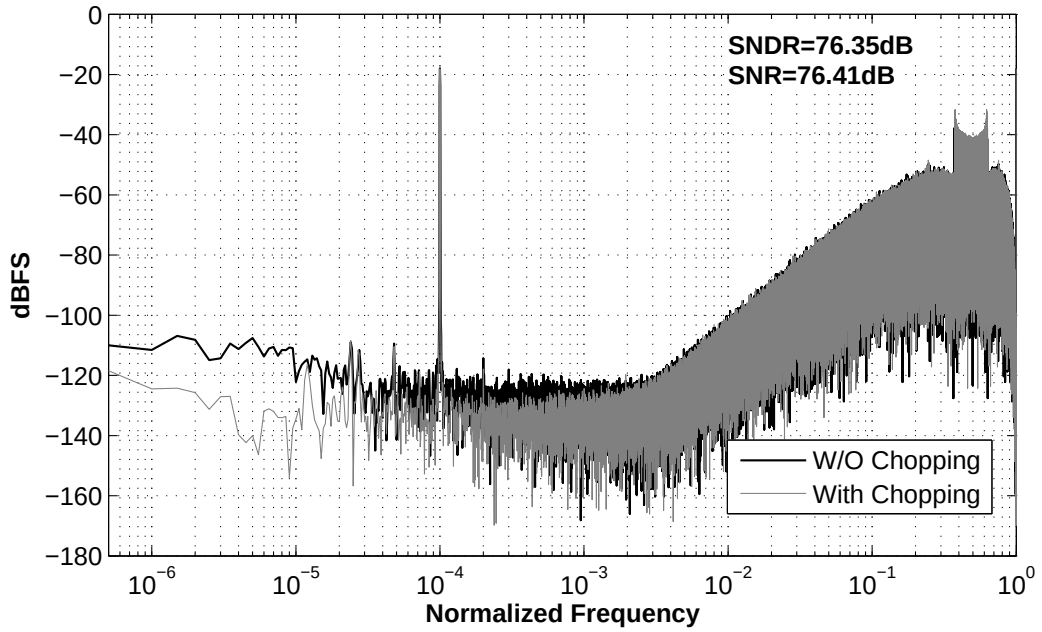
the OSR from 1500 to 250, and increasing the signal bandwidth to 10kHz. This decreased SNR, while distortion remained unchanged, the peak SNDR therefore moved closer to the peak SNR. See Figure 6.10.

6.5 Figure-of-Merit (FOM) For Delta-Sigma Modulator

To compare the relative performance of this Delta-Sigma modulator, a commonly used figure-of-merit can be used:

$$FOMdB = DR_{dB} + 10\log_{10}\left(\frac{Bandwidth}{Power}\right) \text{ , where DR=Dynamic Range} \qquad (6.1)$$

Table 6.3 shows the results of this work compared to recent high-resolution, low-power low-speed Delta-Sigma modulators. All of these designs use low-voltage supplies at 1V or less to save power, or meet the low-voltage requirements of newer deep-submicron CMOS technologies.



SNR Shown is With Chopping Disabled

Figure 6.9: Example Output Spectrum Input at 500Hz, 400mVpp diff.

Dynamic Range (DR), is defined as the range in input levels over which SNR is positive. This however, can be deceiving, as SNDR and SNR can drop off significantly approaching the maximum input level. Therefore in addition to the DR, the table shows adjusted FOMs replacing DR with peak SNR and SNDR, which shows the relative impact of distortion and may give a better sense of the true performance of the ADC. In all cases, a higher number is desired.

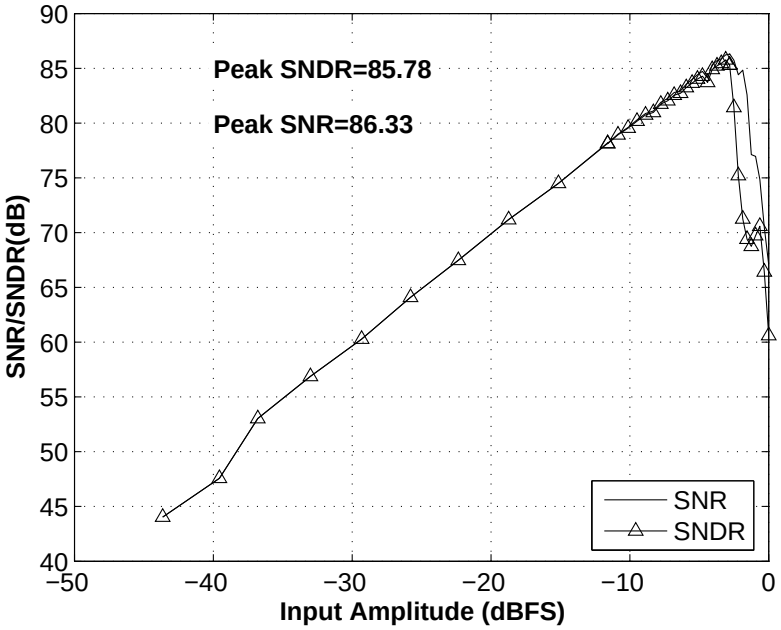
6.5.1 Alternative Popular FOM

An alternative FOM often used has units of pJ/Step, rather than dB. In this case, a lower number is desired.

$$\text{Alternate } FOM = \frac{Power}{2^{\left(\frac{SNR-1.76}{6.02}\right)} \times 2 \times Bandwidth} \text{, quoted in pJ/Step} \qquad (6.2)$$

However this FOM is flawed when applied to thermal noise-limited designs. It assumes that 1

Figure 6.10: Measured SNR with OSR Reduced to 250



Input Level (pk-pk diff.)	SNR (dB)	SNDR (dB)
400mV	78.2	78.1
990mV	85.7	85.2
1.06V	86.2	**85.8**
1.10V	**86.3**	85.3
1.44V	67.0	60.6

Above results were averaged over 5 x 2 Million point FFTs.

Table 6.3: FOM Comparison With Recent Low-Speed, Low-Power High Resolution Delta-Sigma Modulators

(A Higher FOMdB Number is Better)

Paper/ Conference	OSR	Clock Rate	Tech (um)	BW (kHz)	DR (dB)	SNR (dB)	SNDR (dB)	Power	Supply (V)	FOMdB (DR)	FOMdB (SNR)	FOMdB (SNDR)
JSSC2004 (Yao) [22]	100	4MHz	0.09	20	88	85.0	81.0	140μW	1.0	169.5	166.5	162.5
ISSCC2005 (Ahn) [28]	64	3MHz	0.35	20	82	81.0	81.0	1mW	0.6	155.0	154.0	154.0
ISSCC2006 (Goes) [29]	256	5MHz	0.18	10	83	82.0	80.0	200μW	0.9	160.0	159.0	157.0
JSSC2008 (Roh)[17]	50	2MHz	0.13	20	83	81.0	73.0	60μW	0.9	168.2	166.2	158.2
ISSCC2008 (Chae) [5]	100	4MHz	0.18	20	85	84.0	81.0	36μW	0.7	**172.4**	**171.4**	**168.4**
JSSC2008 (Kim) [30]	128	3MHz	0.13	24	92	91.0	89.0	1.5mW	0.9	164.0	163.0	161.0
ISCAS2009 (Gou)[31]	128	5.6MHz	0.18	22	?	91.0	?	300μW	0.9	?	169.7	?
This Work	**1500**	**5MHz**	**0.18**	**1.67**	**96.5**	**96.3**	**91.8**	**83μW**	**1.8**	**169.5**	**169.3**	**164.8**
This Work	**250**	**5MHz**	**0.18**	**10**	**89.1**	**86.3**	**85.8**	**83μW**	**1.8**	**169.9**	**167.1**	**166.6**

extra bit or 6dB in SNR requires only double the power, which is true in quantization noise-limited ADCs such as Flash architectures. However, 6dB corresponds to a 4 times reduction in thermal noise, leading to a 4-fold increase in power consumption for thermal noise-limited designs. The results of this FOM are shown in Table 6.4. While using the dB FOM above, changing the OSR of this design did not affect the FOM significantly, using this alternate FOM, it does have a major effect, and bandwidth is prioritized more than SNR, even though from a power perspective, there is a one-to-one trade-off between the two.

6.5.2 Conclusion on Relative FOM and Performance

From table 6.3, this work is competitive with recent designs in literature despite the use of the higher voltage supply. Only the designs in [5] and [31] show higher FOMs. The work in [5] uses the inverters discussed in Chapter 4. As was discussed, this design's power consumption relies on an exact power supply. It would therefore require a regulated power supply if used in a battery-powered application considered here, where the battery voltage might vary over time and temperature. Such regulation would add some additional power, and likely require an increased power supply to accommodate the regulator. [31] was presented recently but the authors did not have equipment able to measure the distortion levels of the ADC. [32], not included in the comparison contains a hearing-aid front-end including a delta-sigma modulator with an FOM similar to [31], but also does not include distortion results when configured for peak SNR.

In general, one can see that using a highly aggressive design, sacrificing robustness to power supply and process variations as in [5], higher power efficiency can be achieved. [31] uses a more traditional class-AB opamp, but the results presented thus far are incomplete in terms of distortion and SNDR. One can conclude however, that the increased power consumption caused by higher voltage supplies as used in this work cannot easily be overcome. Although the higher supply simplifies circuit design, removing the need for clock boosting, its cost in power is still high, particularly in digital circuits. Overall, the Delta-Sigma modulator designed here approaches, but cannot match the power efficiency of the best low-voltage designs.

Table 6.4: Alternative FOM Comparison With Recent Low-Speed, Low-Power High Resolution Delta-Sigma Modulators

(A Lower Number is Better)

Paper/ Conference	OSR	Clock Rate	Tech (um)	BW (kHz)	DR (dB)	SNR (dB)	SNDR (dB)	Power	Supply (V)	PJ/Step (DR)	PJ/Step (SNR)	PJ/Step (SNDR)
JSSC2004 (Yao) [22]	100	4MHz	0.09	20	88	85.0	81.0	140μW	1	0.170	0.241	0.382
ISSCC2005 (Ahn) [28]	64	3MHz	0.35	20	82	81.0	81.0	1mW	0.6	2.430	2.726	2.726
ISSCC2006 (Goes) [29]	256	5MHz	0.18	10	83	82.0	80.0	200μW	0.9	0.866	0.972	1.224
JSSC2008 (Roh)[17]	50	2MHz	0.13	20	83	81.0	73.0	60μW	0.9	0.130	0.164	0.411
ISSCC2008 (Chae) [5]	100	4MHz	0.18	20	85	84.0	81.0	36μW	0.7	0.062	0.069	0.098
JSSC2008 (Kim) [30]	128	3MHz	0.13	24	92	91.0	89.0	1.5mW	0.9	0.960	1.077	1.356
ISCAS2009 (Gou)[31]	128	5.6MHz	0.18	22	-	91.0	-	300μW	0.9	?	0.235	?
This Work	**1500**	**5MHz**	**0.18**	**1.67**	**96.5**	**96.3**	**91.8**	**83μW**	**1.8**	**0.456**	**0.466**	**0.783**
This Work	**250**	**5MHz**	**0.18**	**10**	**89.1**	**86.3**	**85.8**	**83μW**	**1.8**	**0.178**	**0.246**	**0.260**

6.6 Performance Measurement: Incremental Mode

6.6.1 Test/Measurement Setup

Operating in Incremental mode, the ADC operation included sampling and reset/power down modes. The fabricated DUT outputs included the enable output of the controller. This signal was used to trigger the starting and stopping of data capture. Since both the quantizer's output, as well as the post-filter output were available in testing, the raw quantizer output could be used to verify the correct operation of the digital post-filter. As discussed previously, programmable shift registers allowed extensive control of the timing, power-down ratios, etc. of the converter.

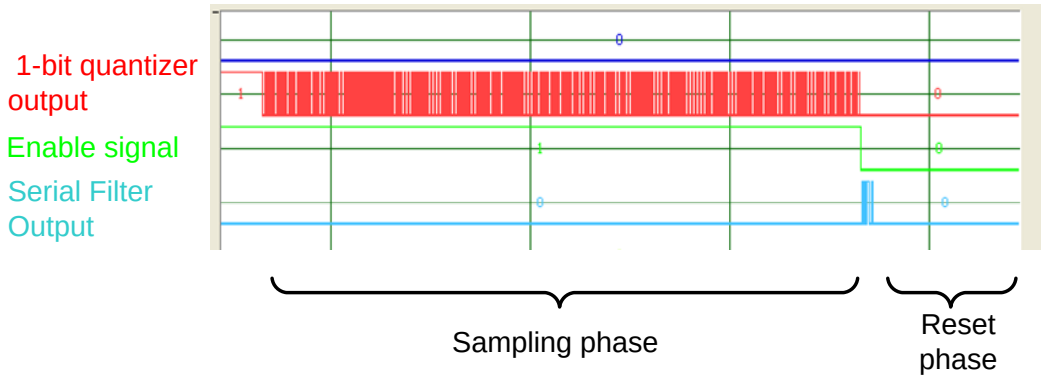


Figure 6.11: Snap-Shot of Captured Digital Outputs

6.6.2 Digital Circuit Operation

All digital circuitry including the digital post-filter and controller appeared to be fully operational in the fabricated chip. When the quantizer outputs were filtered ideally in Matlab, the results were bit-accurate matches for the results from the DUT's serial output. However, this was seen only empirically, as no test vectors were used to fully verify the digital circuit operation.

6.7 Incremental ADC Performance

To verify basic operation, the Incremental ADC was operated with a power-down ratio of 2, meaning that it is off for roughly half of the time, and has a corresponding sample rate of half of the 5MHz clock rate. 100 cycles each, were allowed for the bias circuits and ADC to power up before each sampling phase.

6.7.1 SNR

Figure 6.12 shows a spectrum for an input level of 400mV peak-to-peak differential. As shown, the measured SNR was roughly 84dB, 2dB less than achieved in standard Delta-Sigma mode. As discussed in section 2.4.4, 1.25dB of this gap is due to the nature of the post-filtering used in the Incremental converter. The filter simply does not achieve the same effect as ideal brick-wall filtering.

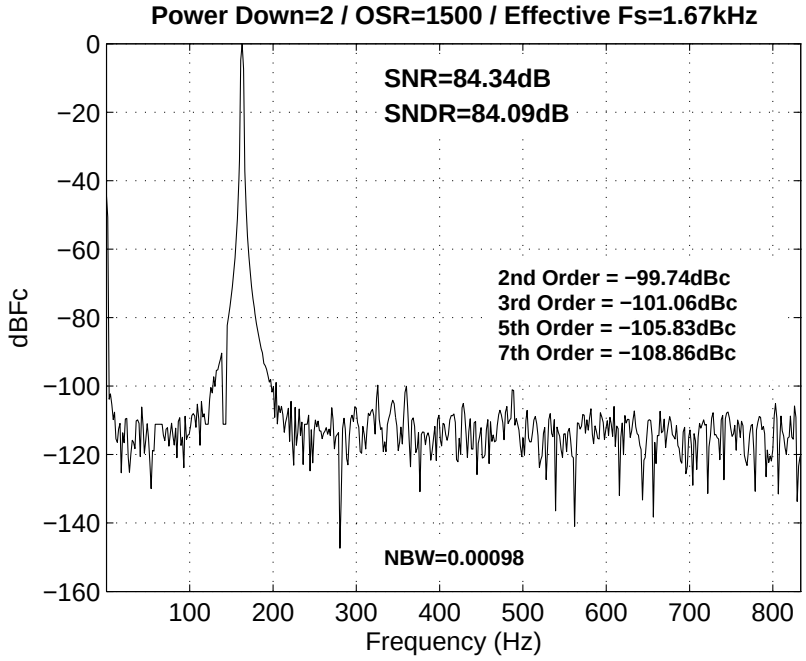


Figure 6.12: Incremental Converter Sample Spectrum (Input at 162.76Hz and 400mVpp diff.)

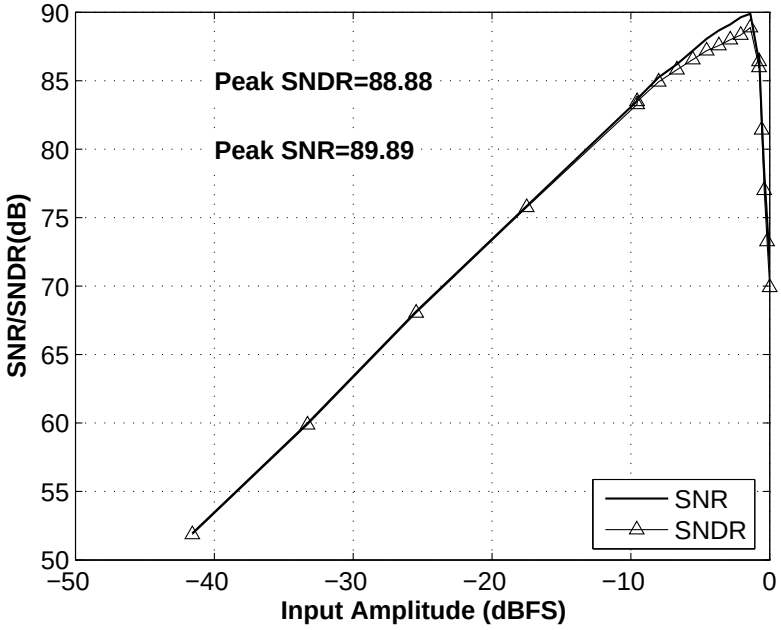


Figure 6.13: Incremental Converter Performance Powered Down by 2 (Averaged Over 5 Runs)

6.7.2 SNR for Higher Power Down Ratios

Scaling down the sample rate (and power) of the Incremental converter caused the SNR to fall off by several dB. Figure 6.15 shows the peak SNR and SNDR for the various power down modes.

The degradation does not seem related to problems with startup transients as changes in startup time did not impact performance. The degradation appears to be due simply to increased noise or offset at low frequencies. This is evident in figure 6.16, which shows an output spectrum from the ADC in Delta-Sigma mode. Any low frequency drift in biasing or reference voltages can lead to low-frequency noise. Such noise could also come from the test setup. In addition, since only the first integrator stage was chopped, flicker noise from the second stage might not be sufficiently suppressed. Furthermore, although chopping modulates flicker noise out of band, non-idealities in the chopper switches can lead to residual offset at DC. When operating at reduced sample rates, this low frequency content can dominate.

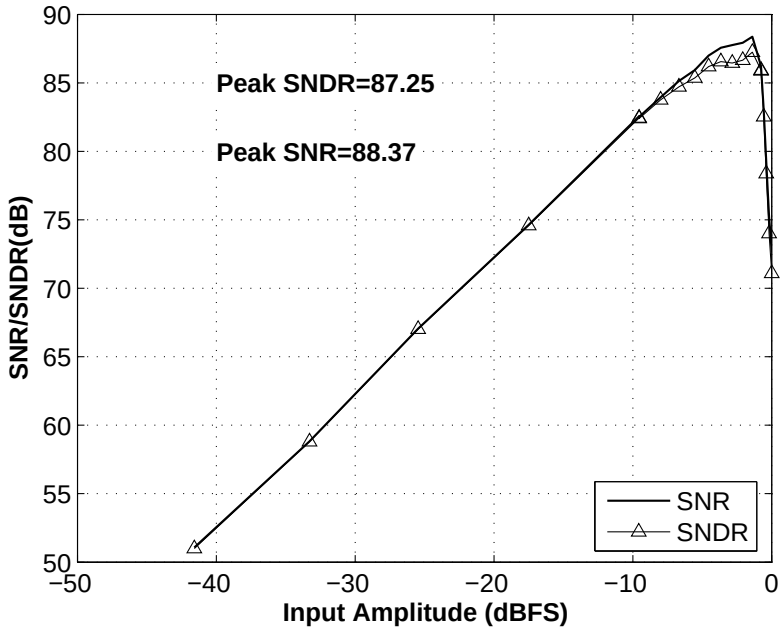


Figure 6.14: Incremental Converter Performance Powered Down by 10

(Averaged Over 5 Runs / Input at 32.552Hz)

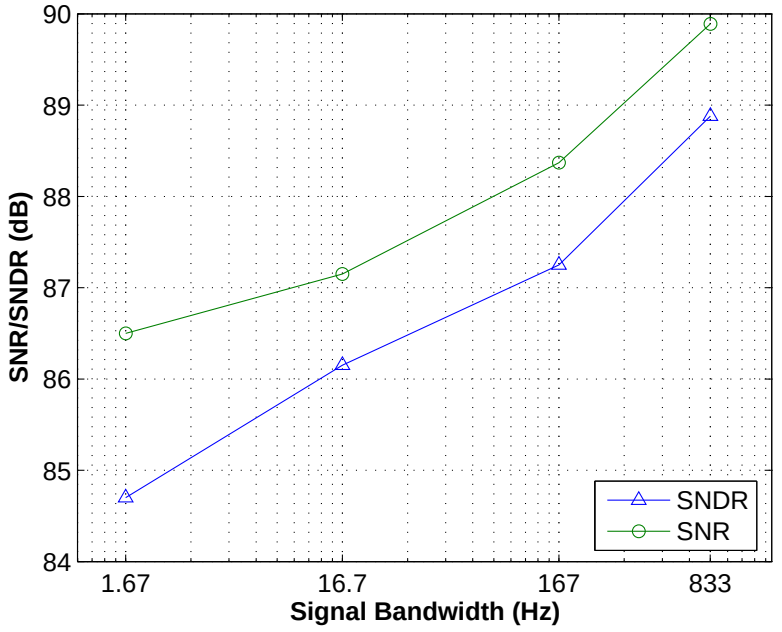


Figure 6.15: Peak SNR and SNDR vs. Power Down Ratios

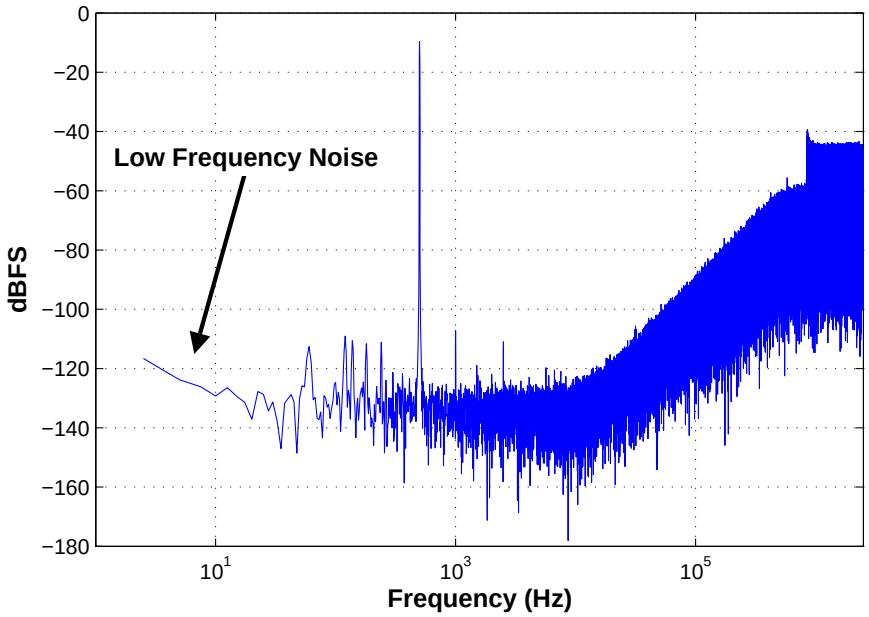


Figure 6.16: Delta-Sigma Spectrum Showing Low Frequency Offset/Noise

6.7.3 (Analog) Power Scaling

Power Down of Bias Current

As mentioned above, 100 cycles were allowed for powering up the ADC. This leads to a 6.7% increase in expected power consumption when in Incremental mode. As was discussed in the previous chapter, the RC time constant of the input-bias current source does allow for the input bias current to be powered up in less than 100 cycles.

However, in testing, an alternative technique was used using off-chip decoupling capacitors. A 0.1uF decoupling capacitor was placed at the bias current input to reduce possible noise entering the circuit. The capacitor prevented the bias node voltage from rising and falling when switched on and off, instead maintaining an average voltage determined by the effective input impedance of the bias input. This should also lead to smaller transient voltages in the circuit by avoiding large voltage swings. By adjusting the bias resistor for each power down mode, the correct voltage was maintained at the input of the circuit. Correct biasing was therefore maintained, without switching the bias node on and off.

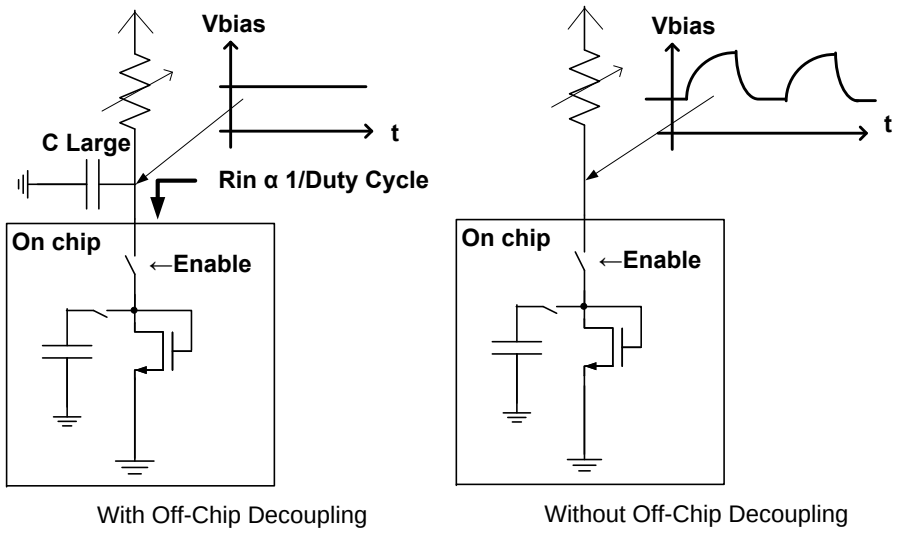


Figure 6.17: Powering Down of Master Bias Circuit

For higher power down ratios however, the required bias resistance became larger than the range of the resistor components on the PCB. Rather than desolder and resolder various resistor values, a parallel resistor was added to pull down the bias voltage. This led to increased power consumption, but would not be needed using the appropriate high value bias resistors.

Conclusion on Bias Configuration

At lower power down ratios, the reduction of startup voltage transients favours the use of the off-chip decoupling capacitor. At higher power down values, due to the large impedances, it becomes more practical to remove the decoupling capacitor on the PCB. Any resulting startup voltage transients could be addressed by increasing the bias startup time. The added power consumption becomes less significant compared to the high power down ratio.

6.7.4 Power Scaling Results

Figure 6.18 shows the measured results of the power-scalability of the Incremental converter. For the analog circuits, the measured results match quite well with expectations with analog power decreasing in proportion to the bandwidth reduction as the converter is power-scaled. For power

down ratios approaching 1000, the average power measurement approaches the measurement error of the test setup.

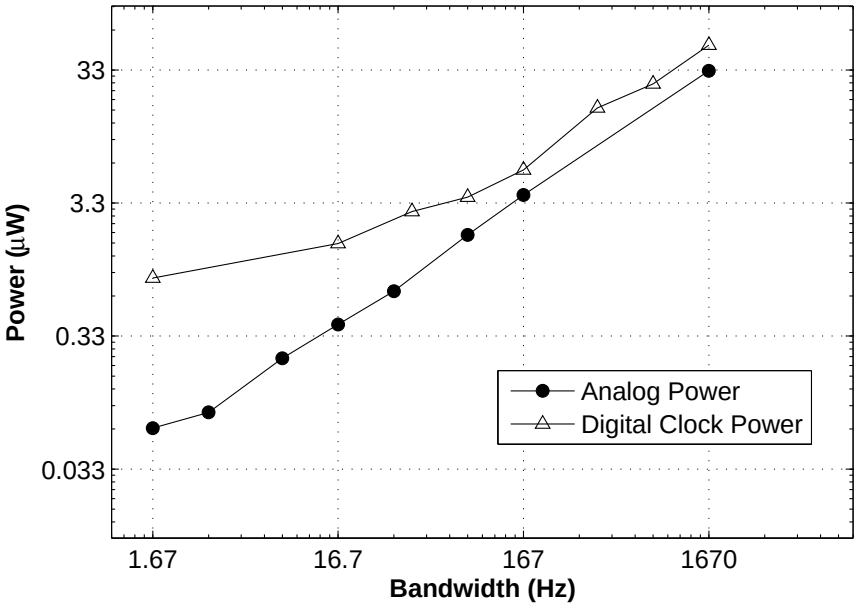


Figure 6.18: Measured Analog Power Scaling With Frequency

6.7.5 Power Consumption of Digital Circuits

However, power scaling of digital clock circuits drops off and levels off at a power reduction of approximately 50 times. This is due to an oversight in the design. Several clock buffer stages are not disabled, and always run as long as a clock is driving the chip. As a result, these buffers always consume about 0.9μW. This could be easily corrected by ensuring that all stages are disabled when desired.

Controller Power

Since all digital circuits including clock generators/buffers and the on-board controller were powered by the same supply, it was not possible to separately measure clock and controller power. However, at high power down ratios, clock power was known to decrease to roughly 0.9μW. As a result, in the lowest bandwidth configuration, controller power could be estimated

Table 6.5: Measured Controller and Filter Power

	Simulated (μW)	**Measured (μW)**
Controller Without (Full-Rate)	not simulated	41
Controller With Divider	4.3	4.3
Filter	38	42

by subtracting 1μW from the total digital power consumption. Using this method, the controller consumed approximately 41μW running at 5MHz.

Enabling the on-chip clock divider which divides the controller clock by 128, the controller power was measured as approximately 4.3μW (after subtracting 0.9μW for clock buffers), identical to the simulated value of 4.3μW.

Filter Power

As discussed in the previous chapter, due to an error in the design, the digital post-filter power does not scale with frequency. However, the filter could be fully disabled, which allowed its power consumption to be measured. The filter power was measured as approximately 42μW, a little higher than the simulated value of 38μW.

6.7.6 Performance Summary of Incremental Converter

Table 6.6 summarizes the performance of the incremental data converter.

6.7.7 Relative Performance of Incremental Converters

Incremental data converters are quite rare in literature and vary significantly in resolution and architectures. It is therefore not easy to assess the relative merit of this design in incremental mode.

Table 6.6: Simulated Specifications of Full-Rate Incremental Converter (OSR=1500)

Parameter	**Simulated**	**Measured**
Supply Voltage	1.8V	1.8V
Reference Voltages	1.3V/500mV	1.29V / 530mV
Maximum Input Swing	1.6Vpp diff.	1.5Vpp diff.
Clock Rate	5MHz	5MHz
Total Analog Power	30μW	33μW
Digital Clock Power	38μW	50μW
Post Filter Power	38μW	42μW
Controller Without (Full-Rate)	not simulated	41μW
Controller With Divider	4.3μW	4.3μW
SNR @ 400mVpp diff. input	87dB	83.5dB
3rd Order distortion (Typical @ 400mVpp diff. input)	-100dBc	-101dBc

6.8 Measurement With PGA Input Stage

As discussed in the previous chapter, an error in the design means that the PGA integrated with the ADC has much higher in-band noise than desired. Testing was done with the PGA driving the ADC input. Figure 6.19 shows the ADC output spectrum with the PGA set to a gain of 10. A 40mVpp diff. input was applied to the input of the ADC, leading to 400mVpp diff. at the input of the ADC. The measured SNR with an OSR of 5000 as in [1] is 72.5dB. From previous measurements, the SNR of the ADC exceeds this and should not be limiting. This result matches almost exactly with the 73dB calculated in section 5.10.2 accounting for the bandwidth of the PGA's thermal noise.

Do to the higher-than-desired PGA output noise, the gain of the PGA is unable to overcome the added noise, when connected to the ADC. Figure 6.20 shows that only the gain of 10 is able to increase SNR at lower frequencies above that of the ADC alone.

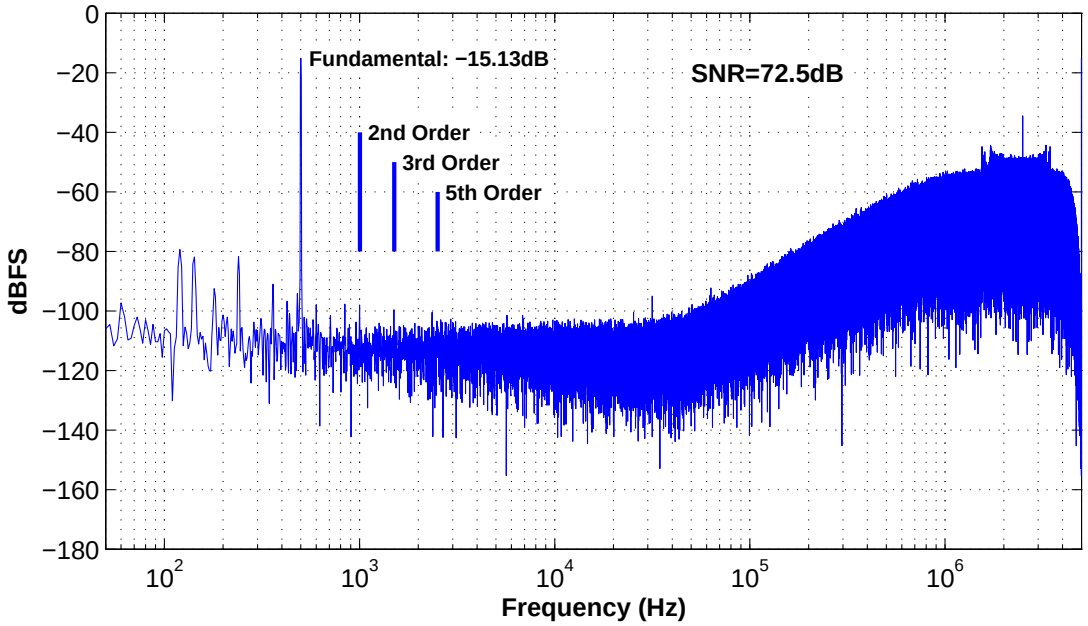


Figure 6.19: Output Spectrum With PGA Gain=10 (Input at 40mVpp Differential)

(Input to ADC is at 400mVpp differential / OSR=5000 as per PGA design [1])

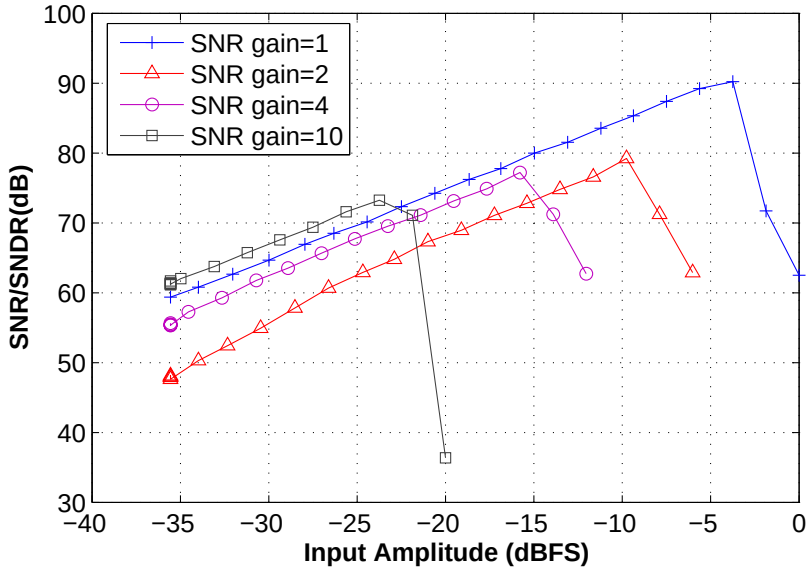


Figure 6.20: SNR Performance for Various PGA Settings (Gain=1 Bypasses PGA Amplifiers)

(Input at 500Hz, OSR=1500)

Chapter 7

Conclusion

In this dissertation, a frequency scalable Incremental ADC has been designed, and a fabricated chip tested. Operating as a Delta-Sigma converter, the fabricated design is competitive with current low-power, low-voltage designs despite using a higher supply voltage. SNR results are within 2dB of simulation results achieving a peak SNDR of 91.8dB, while power is roughly 20% higher at 83μW, due to increased clock power. Operating as a (resettable) Incremental converter, the converter is able to scale in (analog) power and frequency by 1000 times, although digital power scaling could not be measured. However, due to increased noise and or offset at low frequencies, its SNR does fall off by 3-4dB at lower frequencies. Unfortunately, due to increased noise in the PGA input stage, the amplitude-scalability of the combined sensor interface could not be demonstrated.

7.1 Future Work

When combined with the previously designed programmable gain stage of [1], the circuits designed in this work demonstrate the functionality of a sensor interface power scalable based on input amplitude and frequency. However, there remains additional work to optimize the overall system, and improve its power efficiency:

- **Revise Digital Circuit Design:**

  Although the required digital circuitry has been implemented, due to time constraints, it

was not optimally designed for low power. Insufficient attention was paid to the design of clock trees to reduce power and prevent slow clock edges. In addition, due to an error in the design, the digital output filter does not power-scale as required. Furthermore, the digital circuits, particularly the controller were over-designed, to allow flexibility in testing. Both the controller and filter register sizes can be reduced, reducing power while maintaining required functionality.

This design has also demonstrated the high cost of running digital circuits from a relatively high supply voltage. A future design might exploit a dual supply for digital circuits, using level-shifters and regulators to reduce portions of digital power consumption. Even with the added regulators, the power savings might be worthwhile.

- **Explore Different Tradeoffs Between ADC and Gain Stage:**

  Having completed the complete design of the sensor interface, it appears that a different trade-off between the input gain stage and ADC might be favourable. Without the use of a gain stage, the input capacitance of the ADC would be excessive. However, it was shown in [1], that achieving a relatively high gain of 10V/V can also be quite difficult in terms of maintaining low noise and high linearity. A compromise design might combine a gain stage having for example a gain of 2-4, and an ADC, power scalable by the remaining factor.

- **Revise PGA Design:**

  As discovered during testing, the PGA stage suffers from higher than desired in-band noise. To obtain full 14-bit SNR, the PGA design must be revisited, and the in-band noise power spectral density reduced. Using the same architecture, this would require the use of reduced resistor sizes, potentially lowering the input impedance. The alternative design discussed in [1], which uses capacitive gain stages might be considered.

Appendices

Appendix A

Power Efficient Opamp Design

A.1 Opamp Topologies

The common telescopic, folded-cascode, current-mirror and 2-stage opamp topologies were compared, assuming a unity gain bandwidth of ω_t and slew rate of SR, where Cout is the effective load capacitance seen at the opamp output during its worst case, either the sampling or integration phase.

For a traditional opamp using an input differential pair, the bandwidth requirement translates (using the square-law mosfet current equation) into a current requirement of:

$$\text{Current Required for Unity-Gain Bandwidth } \omega_t : \mathrm{I}_{Gm} \geq \frac{\omega_t \cdot Cout \cdot V_{eff}}{2} \tag{A.1}$$

The slew-rate requirement translates simply into a slew-current requirement of:

$$\text{Current Required for Slew-Rate= } SR\text{: } \mathrm{I}_{Slew} \geq SR \cdot Cout \tag{A.2}$$

Table A.1 compares the current requirements of the common opamp topologies shown in Figure A.1.

The results are easier to compare by assuming that I_{Gm} and I_{Slew} are equal as in Table A.2. (This is true in several common cases.) One can see that the Folded-Cascode and Current Mirror opamps require double and (1+1/k) times the current of a telescopic opamp. Assuming

Table A.1: Opamp Current Utilization

Topology	**Current Distribution**	$\mathbf{I}_{Gm}$	$\mathbf{I}_{Slew}$	**Total Current**
Telescopic	I1 in input pair	I1	I1	I1≥max(I_{Gm},I_{Slew})
Folded-Cascode	I1 in input pair, I2 in output	I1	min(I1,I2)	I1+I2≥max(I_{Gm},I_{Slew})+I_{Slew}
Current-Mirror	I1 in input pair, k·I1 in output	k·I1	k·I1	(1+k)·I1≥ $\frac{(1+k)}{k}$·max(I_{Gm},I_{Slew})
2-stage	I1 in input, I2 in output stage	I1·$\frac{C_{Miller}}{C_{out}}$	min(I1·$\frac{C_{Miller}}{C_{out}}$, $I2$)	Rough estimate: I1+I2≥ I_{Gm} · $\frac{C_{Miller}}{C_{out}}$+$I_{Slew}$

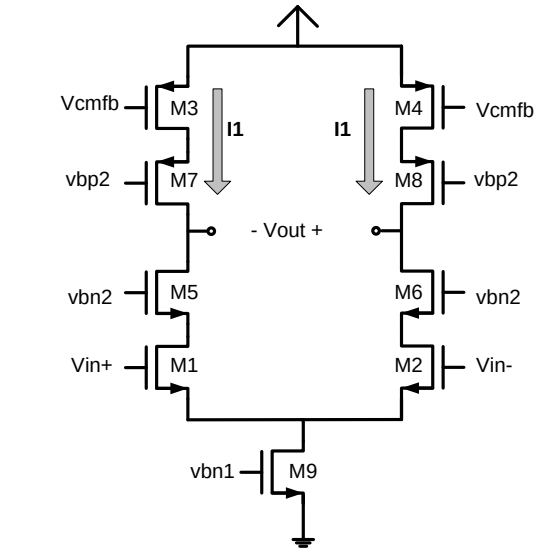
that the Miller capacitance seen by the first stage of the 2-stage opamp is comparable to Cout, it would also use double the current.

Table A.2: Opamp Current Requirement Assuming I_o=I_{Gm}=I_{Slew}

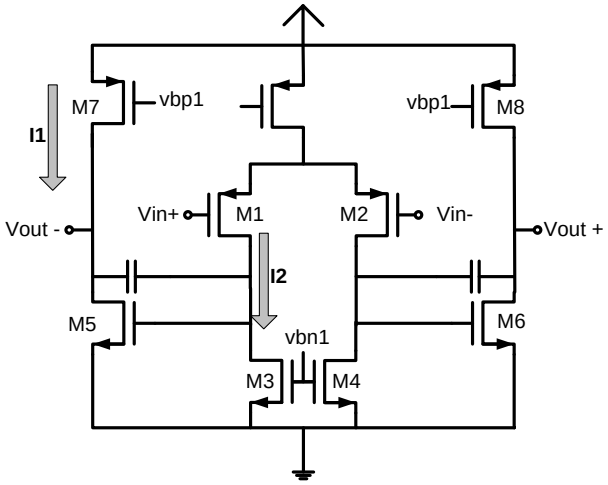
Topology	**Total Current**
Telescopic	I_o
Folded-Cascode	2·I_o
Current-Mirror	$\frac{(1+k)}{k}$·I_o
2-stage	2·I_o*

*Assuming $C_{Miller} = C_{out}$

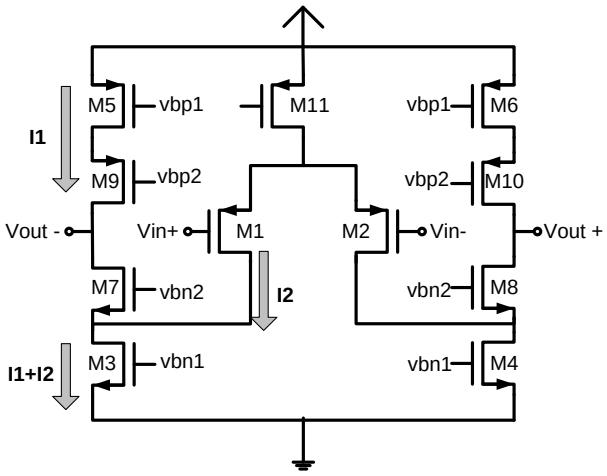
Therefore for the same voltage supply, the telescopic opamp should consume the least current and therefore power. However, the telescopic is not without its drawbacks [33]. Unlike the other topologies, the input and output common modes are stacked and cannot be set independently. With either PMOS or NMOS inputs, the input level cannot go within $2V_{eff}$+V_{th} of the rails, which precludes the use of either very low, or high input common modes levels, favoured in switch design. (Higher or lower input common modes more easily accommodate simple NMOS and PMOS switches[33].)



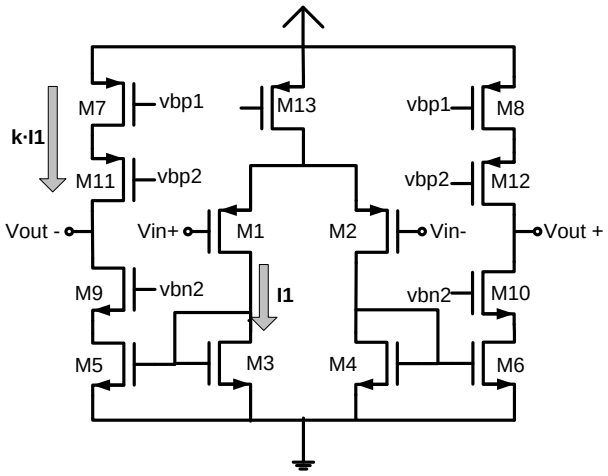
Telecopic Opamp



2-Stage Opamp



Folded Cascode Opamp



Current Mirror Opamp

Figure A.1: Opamp Configurations

A.1.1 Noise Contribution of Opamps (Integration Phase)

The other main aspect of opamp selection pertains to the noise levels of each opamp type. A power efficient opamp is of little benefit if this efficiency comes at the cost of increased noise.

A switched-capacitor integrator operates in two phases, the sampling and integration phases. During the sampling phase, the circuit consists simply of an RC circuit whose RMS noise is

given by the well-known expression [7] $\frac{KT}{C}$, or $\frac{2KT}{C}$ for a fully differential circuit assuming the noise on the positive and negative sides is uncorrelated. During the integration phase, the opamp and integration-phase switches contribute additional noise. The $4kTR$ [7] switch noise as well as the opamp's input-referred noise power are added to the sampled input.

As discussed previously, during the integration phase the circuit behaves as a first order system with time constant given by Equation 4.6. Assuming a first order (single-pole) response, it is a well known result that a flat noise spectral density $V_n^2(f)$ integrated over all frequencies is given by [7]:

$$V_{rms}^2 = \frac{V_n^2(f)}{4\tau} \tag{A.3}$$

The total noise in the switched-capacitor integrator with input sampling capacitor C_{sample} is therefore given by:

$$V_{N,total}^2(f) = V_{N,SamplingPhase}^2(f) + V_{N,IntegrationPhase}^2(f) \tag{A.4}$$

$$V_{N,total}^2(f) = \frac{2KT}{C_{sample}} + \frac{2 \cdot (4KTR_{Switches} + V_{N,Opamp}^2(f))}{4 \cdot \tau} \tag{A.5}$$

Assuming that the opamp dominates the bandwidth, $\tau \approx C_{sample}/gm$

$$V_{N,total}^2(f) = \frac{2KT}{C_{sample}} + \frac{2 \cdot (4kTR_{Switches} + V_{N,Opamp}^2(f))}{4 \cdot C_{sample}} \cdot gm \tag{A.6}$$

Opamp Noise

Assuming that some technique such as chopping, auto-zeroing or correlated double sampling is used to remove low frequency flicker noise, only the Mosfet channel thermal noise remains. Each Mosfet has a noise current given by [7]:

$$I_n^2(f) = 4KT\,(\gamma)\,gm, \text{ where } \gamma \approx \frac{2}{3} \tag{A.7}$$

$$\text{Equivalently } V_n^2(f) = \frac{4KT\,(\gamma)}{gm} \tag{A.8}$$

It was assumed that cascode devices do not contribute to output noise. (The low-impedance seen at the source of the cascode devices means that the thermal noise of the cascode devices

should not flow to the opamp output [7].) The results are shown in Table A.3.

Table A.3: Single-Ended Opamp Noise Characteristics (Refer to Figure A.1)

Topology	$V^2_{n,in}(f)$	ω_t	$V^2_{n,rms}$=$V^2_{n,in}(f)\cdot\frac{\omega_t}{4}$
Telescopic	$\frac{4KT\gamma}{gm_{1/2}}\left(1+\frac{gm_{3/4}}{gm_{1/2}}\right)$	$\frac{gm_{1/2}}{Cout}$	$\frac{KT\gamma}{Cout}\left(1+\frac{gm_{3/4}}{gm_{1/2}}\right)$
Folded-Cascode	$\frac{4KT\gamma}{gm_{1/2}}\left(1+\frac{gm_{3/4}}{gm_{1/2}}+\frac{gm_{5/6}}{gm_{1/2}}\right)$	$\frac{gm_{1/2}}{Cout}$	$\frac{KT\gamma}{Cout}\left(1+\frac{gm_{3/4}}{gm_{1/2}}+\frac{gm_{5/6}}{gm_{1/2}}\right)$
Current-Mirror	$\frac{4KT\gamma}{gm_{1/2}}\left(1+\frac{gm_{3/4}}{gm_{1/2}}+\frac{gm_{5/6}+gm_{7/8}}{k^2\cdot gm_{1/2}}\right)$	$\frac{k\cdot gm_{1/2}}{Cout}$	$k\cdot\frac{KT\gamma}{Cout}\left(1+\frac{gm_{3/4}}{gm_{1/2}}+\frac{gm_{5/6}+gm_{7/8}}{k^2\cdot gm_{1/2}}\right)$
2-Stage	$\frac{4KT\gamma}{gm_{1/2}}\left(1+\frac{gm_{3/4}}{gm_{1/2}}+\frac{gm_{5/6}+gm_{7/8}}{Gain_{Stage1}\cdot gm_{1/2}}\right)$	$\frac{gm_{1/2}}{C_{Miller}}$	$\frac{KT\gamma}{C_{Miller}}\left(1+\frac{gm_{3/4}}{gm_{1/2}}+\frac{gm_{5/6}+gm_{7/8}}{Gain_{Stage1}\cdot gm_{1/2}}\right)$

From Table A.3, one can see that each opamp's noise is increased by any current sources present in addition to the input differential pair. These contributions are proportional to the gm of these devices, which can be minimized by biasing these devices with high Veff's. There is though, a limit on how large these voltages can be as higher Veff's also reduce the voltage headroom available at the opamp outputs[9].

A.1.2 Noise of Overall Integrator (α Factor)

Examining equations A.6 and A.8, since an opamp's noise voltage is proportional to $1/gm$, the assumption that $1/gm >> R_{Switches}$ (or, that the opamp dominates the integrator bandwidth) also implies that the opamp noise dominates over switch noise in the integration phase of the integrator. This gives:

$$V^2_{N,total}(f) \approx \frac{2KT}{C_{sample}} + 2\cdot V^2_{N,rms,opamp} \tag{A.9}$$

C_{out} referred to in Table A.3 is proportional to C_{sample} in an integrator. Therefore the results from Table A.3 can be applied directly to Equation A.9 to compare the total noise of integrators using each opamp. One can also define the relative increase α in noise caused by various opamp topologies.

$$V^2_{N,total}(f) \approx \frac{2(1+\gamma)KT}{C_{sample}}\cdot(1+\alpha) \tag{A.10}$$

$$= \frac{10KT}{3 \cdot C_{sample}} \cdot (1+\alpha) \tag{A.11}$$

$$\text{where } \alpha = \frac{\gamma}{1+\gamma} \cdot \left(\frac{V_{N,rms,opamp}^2 \cdot C_{sample}}{\gamma \cdot KT} - 1 \right) \tag{A.12}$$

$$= \frac{2}{5} \cdot \left(\frac{V_{N,rms,opamp}^2 \cdot C_{sample}}{\gamma \cdot KT} - 1 \right) \tag{A.13}$$

The α factors for the opamps being compared are shown in Table A.4, substituting $\gamma = 2/3$.

Table A.4: (Approximate)Relative Opamp Noise (Refer to Figure A.1)

Topology	α = Relative Increase In Noise
Telescopic	$\frac{2}{5} \cdot \frac{gm_{3/4}}{gm_{1/2}}$
Folded-Cascode	$\frac{2}{5} \cdot \left(\frac{gm_{3/4}}{gm_{1/2}} + \frac{gm_{5/6}}{gm_{1/2}} \right)$, note that M3 carries I1+I2 vs M1 which carries I2
Current-Mirror	$\frac{2}{5} \cdot \left[(k-1) + k \cdot \left(\frac{gm_{3/4}}{gm_{1/2}} + \frac{gm_{5/6}+gm_{7/8}}{k^2 \cdot gm_{1/2}} \right) \right]$
2-Stage	$\frac{2}{5} \cdot \left[\left(\frac{C_{out}}{C_{Miller}} - 1 \right) + \frac{C_{out}}{C_{Miller}} \cdot \left(\frac{gm_{3/4}}{gm_{1/2}} + \frac{gm_{5/6}+gm_{7/8}}{Gain_{Stage1} \cdot gm_{1/2}} \right) \right]$

From table A.4, one can also see that the α factor can also be seen and calculated as:

$$\alpha = \frac{\gamma}{1+\gamma} \cdot \left(\frac{\sum(Gm_{CurrentSources})}{\sum(Gm_{Input})} \right) \tag{A.14}$$

From Tables A.3 and A.4, the advantages of the Telescopic opamp are re-affirmed. It has the lowest relative increase in noise α, due to its lack of additional current sources.

A.1.3 Effect of Noise on Power

Tables A.4 and A.1 compare the noise levels and current requirements for some required integrator bandwidth assuming that each opamp has the *same size capacitor load* designed to achieve the required thermal noise level. However, from Table A.4, each opamp topology contributes different thermal noise levels. To maintain the same thermal noise for each integrator, the capacitor sizes must be increased according to any increase in thermal noise. *Therefore, in terms of power, the power requirements get further multiplied by any increase in noise.*

Making a series of simplifying assumptions, one can compare the total power required by each design. This leads to Table A.5.

Table A.5: Opamp Current Estimates Including Noise Requirement*

Topology	**Base Current**	α	Total Current
Telescopic	I_o	0.2	$1.2 \cdot I_o$
Folded-Cascode	$2 \cdot I_o$	0.6	$2 \times 1.6 \cdot I_o = 3.2 \cdot I_o$
Current-Mirror (k=1)	$2 \cdot I_o$	0.6	$2 \times 1.6 \cdot I_o = 3.2 \cdot I_o$
2-stage	$2 \cdot I_o$	0.2	$2 \times 1.2 \cdot I_o = 2.4 \cdot I_o$

*Assuming:

- $I_{Gm}=I_{Slew}$ (Input Gm pair have same current as slew current)
- Current sources have 1/2 the V_{eff} of input devices
- For 2-stage opamp, $C_{Miller} = C_{out}$ and stage 1 gain is large

A.1.4 Conclusions on Opamp Topology

In terms of power efficiency and noise, the telescopic opamp appears to be the obvious choice. The one disadvantage of this topology is as mentioned, the lack of flexibility in input and output common modes, but this is less of a factor in the relatively high (compared to deeper-submicron) supply in use in this design. There are also many examples (e.g. [34],[15],etc) of successful implementations of the telescopic opamp in literature, particularly in high-speed applications.

In broader terms, it is useful to examine the nature of this topology's advantages. Firstly, from Figure A.1 it can be seen that 100 percent of the current in the opamp contributes both to the opamp transconductance *and* slew-rate. By their very nature, the other opamps consume more current through the presence of an input and output stage. Not only does this increase power consumption, but also degrades their noise level. **Therefore the target of both a power and noise efficient OTA should be to reduce any current consumption that does not contribute directly to the OTA input transconductance.**

References

[1] A. Nafee, "Design of high accuracy power scalable MEMS sensor interface," Master's thesis, University of Toronto, 2007.

[2] A. Nafee and D. Johns, "A 14 - bit micro-watt power scalable automotive MEMS pressure sensor interface," in *Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European*, Sept. 2008, pp. 450–453.

[3] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Converters*. Hoboken, NJ: John Wiley Sons. Inc, 2005.

[4] J. Ramirez-Angulo, R. G. Carvajal, J. A. Galan, and A. Lopez-Martin, "A free but efficient low-voltage class-AB two-stage operational amplifier," *IEEE Transactions on Circuits and Systems—Part II: Analog and Digital Signal Processing*, vol. 53, no. 7, pp. 568–571, Jul. 2004.

[5] Y. Chae, I. Lee, and G. Han, "A 0.7V 36μW 85db-DR audio $\Delta\Sigma$ modulator using class-c inverter," *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pp. 490–630, Feb. 2008.

[6] S. I. Ahmed, "Power scaleable and low power pipeline adc using power resettable opamps," Master's thesis, University of Toronto, 2004.

[7] D. Johns and K. Martin, *Analog Integrated Circuit Design*. John Wiley Sons. Inc., 1997.

[8] K. Iizuka, H. Matsui, M. Ueda, and M. Daito, "A 14-bit digitally self-calibrated pipelined ADC with adaptive bias optimization for arbitrary speeds up to 40MS/s," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 4, pp. 883–890, 2006.

[9] R. Schreier and T. Caldwell, "ECE1371 course slides, University of Toronto," 2008.

[10] J. Robert, G. C. Temes, V. Valencic, R. Dessoulavy, and P. Deval, "A 16-bit low voltage cmos a/d converter," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 2, pp. 157–162, Apr. 1987.

[11] J. Markus, J. Silva, and G. C. Temes, "Theory and applications of incremental $\Delta\Sigma$ converters," *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, vol. 51, no. 4, pp. 678–688, Apr. 2004.

[12] J. Markus, "Higher-order incremental delta-sigma analog-to-digital converters," Ph.D. dissertation, Budapest University of Technology and Economics, 2005.

[13] T. Caldwell and D. Johns, "An incremental data converter with an oversampling ratio of 3," in *Research in Microelectronics and Electronics 2006, Ph. D.*, 2006, pp. 125–128.

[14] R. Schreier, "The delta-sigma toolbox version 7.2," Feb. 2008.

[15] P. Balmelli and Q. Huang, "A 25-MS/s 14-b 200mW $\Delta\Sigma$ modulator in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2161–2169, Dec. 2004.

[16] A. Gharbiya and D. Johns, "On the implementation of input-feedforward delta-sigma modulators," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 53, no. 6, pp. 453–457, June 2006.

[17] J. Roh, S. Byun, Y. Choi, H. Roh, Y. Kim, and J. Kwon, "A 0.9-V 60-μW 1-bit fourth order delta-sigma modulator with 83-dB dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 361–370, Feb. 2008.

[18] J. M. de la Rosa, S. Escalera, B. Perez-Verdu, F. Medeiro, O. Guerra, R. del Rio, and A. Rodriguez-Vazquez, "A cmos 110-dB@40-kS/s programmable-gain chopper stabilized

third-order 2-1 cascade sigma-delta modulator for lower-power high-linearity automotive sensor ASICs," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 11, pp. 2246–2264, Nov. 2005.

[19] P. Malcovato, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioural modeling of switched-capacitor sigma-delta modulators," *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, vol. 50, no. 3, pp. 352–364, Mar. 2003.

[20] G. Suarez, M. Jimenez, and F. O. Fernandez, "Behavioral modeling methods for switched-capacitor $\Sigma\Delta$ modulators," *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, vol. 54, no. 6, pp. 1236–1244, Jun. 2007.

[21] A. J. Lopez-Martin, S. Baswa, J. Ramirez-Angulo, and R. G. Carvajal, "Low-voltage super class AB cmos ota cells with very high slew rate and power efficiency," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1068–1077, May 2005.

[22] L. Yao, M. Steyaert, and W. Sansen, "A 1-V 140-μW 88-dB audio sigma-delta modulator in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 11, pp. 1809–1818, Nov. 2004.

[23] Z. Cao, T. Song, and S. Yan, "A 14 mW 2.5 MS/s 14 bit $\Delta\Sigma$ modulator using split-path pseudo-differential amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 10, pp. 2169–2179, Oct. 2007.

[24] Y. Chae and G. Han, "Low voltage, low power, inverter-based switched-capacitor delta-sigma modulator," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 458–472, Feb. 2009.

[25] B. Razavi, *Design of CMOS Analog Integrated Circuits.* New York, NY: McGraw-Hill, 2001.

[26] W. Liu, *MOSFET models for SPICE simulation, including BSIM3v3 and BSIM4.* New York: Wiley, 2001.

[27] *Operating Manual and Programming Reference: Model DS360 Ultra Low Distortion Function Generator*, Stanford Research Systems.

[28] G.-C. Ahn, D.-Y. Chang, M. Brown, N. Ozaki, H. Youra, K. Yamamura, K. Hamashita, K. Takasuka, G. C. Temes, and U.-K. Moon, "A 0.6V 82dB $\Delta\Sigma$ audio ADC using switched-RC integrators," in *Solid-State Circuits Conference, 2006. ISSCC 2005. Digest of Technical Papers. IEEE International*, Feb. 2006, pp. 166–167.

[29] J. Goes, B. Vaz, R. Monteiro, and N. Paulino, "A 0.9V $\Delta\Sigma$ modulator with 80dB SNDR and 83dB DR using a single-phase technique," in *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, Feb. 2006, pp. 191–200.

[30] M. G. Kim, G.-C. Ahn, P. Hanumolu, S.-H. Lee, S.-H. Kim, S.-B. You, J.-W. Kim, G. Temes, and U.-K. Moon, "A 0.9V 92 dB double-sampled switched-RC delta-sigma audio ADC," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1195–1206, May 2008.

[31] X. Gou, Y.-R. Li, C. Jian-Qiu, X. Jun, and R. Jun-Yan, "A low power low voltage 16 bit audio $\Delta\Sigma$ modulator," in *Circuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on*, 24 2009-Yearly 27 2009, pp. 3142–3145.

[32] S. Kim, J.-Y. Lee, S.-J. Song, N. Cho, and H.-J. Yoo, "An energy-efficient analog front-end circuit for a sub-1-V digital hearing aid chip," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 4, pp. 876–882, Apr. 2006.

[33] A. Gharbiya, "Architecture alternatives for time-interleaved and input-feedforward delta-sigma modulators," Ph.D. dissertation, University of Toronto, 2008.

[34] Z. Li and T. S. Fiez, "A 14 bit continuous-time delta-sigma A/D modulator with 2.5MHz signal bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 9, pp. 1873–1883, Sep. 2007.