LOW-POWER CHARGE-PUMP BASED SWITCHED-CAPACITOR CIRCUITS

by

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A thesis submitted in conformity with the requirements for the degree of Doctor of Philosophy Graduate Department of Electrical and Computer Engineering University of Toronto

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Abstract

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In this thesis, low-power charge-pump (CP) based switched-capacitor (SC) circuits are proposed. The approach is validated in SC integrators and gain stages, and is shown to achieve power savings compared to conventional SC circuits. For the same thermal noise and settling performance, a CP based integrator with *N* sampling capacitors ideally consumes N^2 times lower OTA power compared to a conventional integrator. Practical effects such as the OTA partial slew-rate limitation and the CP parasitics reduce the power savings. In the case of a SC gain stage, reduction in power savings also occurs due to the load capacitance from the next stage. A prototype delta-sigma modulator employing a CP integrator at the front-end is fabricated. Experimental results demonstrate that the CP based ADC achieves the same performance as a conventional ADC while consuming three times lower OTA power in the front-end integrator. The CP ADC achieves 87.8 dB SNDR 89.2 dB SNR and 90 dB DR over a 10 kHz bandwidth while consuming 148 μ W from a 1.2 V power supply. The conventional ADC has similar performance but dissipates 241 μ W. The CP ADC figure-of-merit (FOM) is 0.369 pJ/conv-step, which is almost 40% lower than that of the conventional ADC.

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List of Acronyms

ADC analog-to-digital converter
CBSC Comparator-based switched-capacitor
CDS Correlated double sampling
CIFB cascaded integrators with distributed feedback
CM common-mode
CMFB common-mode feedback
CMOS complementary metal-oxide-semiconductor
CP charge-pump
CQFP Ceramic Quad Flat Pack
CT continuous-time
DAC digital-to-analog converter
DEM dynamic element matching
DIP dual in-line package
DWA data-weighted averaging
DR dynamic range
FFT fast Fourier transform

FOM figure-of-merit

- IC integrated circuit
- **ILA** individual level averaging
- MASH multi-stage noise shaping
- MDAC multiplying digital-to-analog converter
- MEMS microelectromechanical systems
- MIM metal-insulator-metal
- MS mean-square
- NTF noise transfer function
- **OSR** oversampling ratio
- OTA operational transconductance amplifier
- PCB printed circuit board
- **PSD** power spectral density
- **PSRR** power supply rejection ratio
- SC switched-capacitor
- **SNDR** signal-to-noise-and-distortion ratio
- **SNR** signal-to-noise ratio
- SQNR signal-to-quantization-noise ratio
- **STF** signal transfer function
- SR slew-rate
- **ZCBC** Zero-crossing based circuit

Chapter 1

Introduction

1.1 Motivation

Sensory and wireless systems typically have stringent power requirements. Such systems are often small and consume little power, but their lifetime is limited by their energy consumption. The required power in sensory systems is typically obtained from a battery or from external sources through energy harvesting. To satisfy the energy specifications in these systems it is not uncommon to design the system bottom-up, by determining the overall performance based on the available power budget [1,2].

The interface circuitry in sensory systems generally require high accuracy in a low input signal bandwidth. Examples of such systems include microelectromechanical systems (MEMS) based accelerometers, gyroscopes, and microphones [3–7]. In addition, the output signal of such sensors is typically small. For instance, capacitive accelerometers convert a small mechanical displacement to a corresponding capacitance change, which results in a small output voltage [4]. Similarly, capacitive microphone sensors typically produce outputs with an amplitude range of tens of millivolts and 10-20 kHz of signal bandwidth [6,7]. In highresolution switched-capacitor (SC) systems, to achieve low noise, small signals require large sampling capacitors or high oversampling ratios, both of which lead to an increased operational transconductance amplifier (OTA) power consumption. Even though technology scaling has considerably reduced digital power in sensory systems, analog circuits have not benefited from scaling in terms of power dissipation [8,9].

In this dissertation, charge-pump (CP) based SC circuits are proposed that achieve significant power savings compared to the conventional SC circuits. The approach is demonstrated in SC integrators and amplifiers, and is experimentally validated in a second order $\Delta\Sigma$ modulator analog-to-digital converter (ADC). The ADC in this work is designed for a 14-bit resolution in a 10 kHz input bandwidth, with an input signal amplitude of 400 mVpp differential. Considering the low bandwidth and high resolution specifications of the ADC, a $\Delta\Sigma$ modulator with a high oversampling ratio (OSR) is selected. Two $\Delta\Sigma$ ADCs are fabricated. The first ADC employs a CP based integrator, while the second ADC uses a conventional integrator in their first stages, respectively. Experimental results of the two ADCs show that the CP based modulator achieves the same performance as the conventional modulator, while consuming 3 times lower OTA power in the dominant front-end integrator.

1.2 Existing Low-Power SC Circuit Techniques

In this section, some of the existing analog techniques to reduce the power consumption of SC circuits are discussed, and the state-of-the-art performance achieved using these techniques are presented.

1.2.1 Comparator-based SC Circuits

Comparator-based switched-capacitor (CBSC) circuits were developed to address the challenges of OTA design in scaled CMOS technologies, and as an alternative approach to reduce the SC circuits power consumption [10]. In CBSC circuits the combination of a comparator and a current source replaces the OTA. The fundamental difference between the operation of a CBSC circuit and an OTA-based SC circuit is that in a comparator-based circuit the comparator



Figure 1.1: A CBSC MDAC stage.

detects the virtual ground condition and triggers sampling, while in an OTA-based circuit the OTA forces the virtual ground during the charge transfer phase.

Figure 1.1 shows the circuit diagram of a CBSC gain stage. As shown, the sampling phase Φ_1 in a CBSC circuit is the same as the sampling phase in an OTA-based circuit. However, in the comparator-based charge-transfer phase the output voltage is initially shorted to ground by the switch *P* during a short preset phase. Next, the current source *I* turns on and charges up the capacitor network consisting of C_s , C_f and C_l , until the virtual ground condition is detected, that is the comparator differential input voltage becomes zero. At this time, all the sampled charge on C_s has been transferred to C_f and the current source is turned off by the comparator.

The main limitation of CBSC circuits is the nonlinearity due to the finite comparator delay and the finite output resistance of the current source, which creates a voltage-dependent overshoot in the output. To reduce the overshoot dual-phase schemes have been proposed, which make use of a fine current source together with a coarse current source. However, this creates a trade-off between linearity and speed. With respect to power consumption it has been shown that for the same power and speed, CBSC circuits achieve a lower noise power spectral density (PSD) and noise bandwidth. Equivalently for the same speed and noise performance, CBSC circuits require lower power consumption [10]. CBSC circuits have been demonstrated in the realization of pipelined ADCs [10–13] as well as $\Delta\Sigma$ modulators [14–16]. In [11] the comparator is replaced by a simple zero-crossing detector, and in [15] the current source is replaced by a resistor. The design in [16] makes use of dynamic comparators and current pulse drivers and has the advantage of power consumption scalability with the sampling-rate. The state-of-the-art performance for $\Delta\Sigma$ modulators using CBSC circuits is a signal-to-noise-and-distortion ratio (SNDR) of 70.4 dB in a 2.5 MHz signal bandwidth with a power consumption of 3.73 mW [16]. The ADC figure-of-merit (FOM) defined as (equation (54) in [17]):

$$FOM - dB = SNDR(dB) + 10log_{10}(\frac{BW}{Power})$$
(1.1)

is equal to 158.5 dB.

1.2.2 Double Sampling

Double sampling technique has widely been used in SC $\Delta\Sigma$ modulators [18–22]. The purpose of double sampling is to utilize the OTA during both clock phases of SC operation. Figure 1.2 shows a double sampled SC integrator, where two sampling capacitors are used with interleaved clock signals. This effectively doubles the modulator sampling-rate and the OSR of the modulator, hence improves its performance. Alternatively, the clock frequency can be halved, which relaxes the OTA settling speed and reduces power.

The main drawback with the implementation shown in Figure 1.2 is the mismatch between the two sampling capacitors, which causes the modulation of the input signal as well as the feedback DAC signal D_iV_{ref} . Modulation of the wideband DAC signal increases the in-band noise power and reduces the signal-to-noise ratio (SNR) considerably. To address this issue, a number of solutions have been described in literature, which are based on additive error switching [23], individual level averaging (ILA) [24], and fully-floating differential SC integrators [25].



Figure 1.2: Double sampled SC integrator.

The low-voltage $\Delta\Sigma$ modulator reported in [22] makes use of double sampling and amplifiers with inverter output stages to achieve an SNDR of 81.7 dB for a 20 kHz signal bandwidth and consumes 35.2 μ W. The ADC *FOM* – *dB* is 169.2 dB.

1.2.3 Digitally-Assisted Amplifiers

Power consumption of analog circuits increases with their complexity. Digitally-assisted amplifiers are based on simplified analog circuits, and leverage digital signal processing to correct for their nonlinearity and mismatch.

Figure 1.3 illustrates a resistively loaded differential pair used as a residue amplifier in the first stage of a pipelined ADC [26, 27]. Since there is no feedback, a high gain amplifier is not required. Distortion in this open-loop structure is mainly caused by the nonlinear input capacitance, gain compression and mismatch of the differential pair. Also, the gain of this stage is very sensitive to process and temperature variations. In [26], the background calibration scheme required for correcting nonlinearities is implemented using 8400 gates, 64 bytes of



Figure 1.3: An open-loop SC amplifier.

RAM and 64 kb of ROM, while the achieved linearity is 12 bits.

1.2.4 OTA-less SC Gain Using a CP

In [28] a voltage gain of two resulting from a CP circuit is used to implement the 1.5-bit multiplying digital-to-analog converters (MDACs) in a 10-bit pipelined ADC. Figure 1.4 shows the circuit diagram of the MDAC. Since the output of the CP cannot drive the load capacitance of the next stage directly (due to charge sharing), a source follower is used to buffer the output. This way a voltage gain is achieved by summing the voltages on the CP capacitors, without using an OTA. However, one limitation with this approach is that the gain of the circuit is determined by the number of capacitors in the CP. For example, to implement a voltage gain of 8, a CP circuit with 8 capacitors must be used. Since the gain of the circuit is also sensitive to the CP parasitics, increasing the number of capacitors causes the gain error to increase. Therefore, its application is limited to gain circuits with a small gain. The pipelined ADC implemented using this technique achieves a peak SNDR of 58.2 dB at 50 MS/s and dissipates 9.9 mW. The ADC FOM - dB in this case is 152.2 dB.



Figure 1.4: A 1.5-bit MDAC stage using a capacitive CP and a voltage buffer.

1.2.5 Amplifier Sharing/Power Down

One approach to reduce the power consumption in SC circuits is based on amplifier sharing between SC networks operating on opposite clock phases. This is possible since SC networks require the OTA only during the charge transfer phase, and not during the sampling phase. Although this technique has been very popular in pipeline ADCs [29–32], it has also found applications in $\Delta\Sigma$ modulators. One example is in complex bandpass $\Delta\Sigma$ ADCs, where one amplifier can be time-multiplexed between two integrators of the in-phase and quadrature branches [33]. Amplifier sharing has also allowed the implementation of low-pass $\Delta\Sigma$ ADCs with only one OTA [18, 34]. [34] achieves an SNDR of 80 dB for a 10 kHz bandwidth and dissipates 200 μ W (*FOM* – *dB*=157.1 dB), while [18] has a peak SNDR of 61.1 dB in 16 kHz bandwidth and consumes 17 μ W (*FOM* – *dB*=150.8 dB). Similar to amplifier sharing, turning off the OTA for half a clock cycle has also saved analog power in $\Delta\Sigma$ ADCs [35, 36].

1.2.6 Other Schemes

Within the scope of $\Delta\Sigma$ ADCs, employing the input feedforward technique [37] eliminates the signal component in the integrator outputs. This together with multi-bit quantization reduces the output voltage swing of integrators. Reduction of the voltage swing lowers the linearity

and gain requirements of the integrator amplifier. Hence, simple amplifier structures with relaxed gain and output swing requirements such as single-stage OTAs can be used, thus saving power [38]. The design in [39] makes use of multi-bit quantization and linear incomplete settling to save the power consumption of a first stage folded-cascode OTA. Inverter-based designs replace the OTAs with power efficient inverters [40, 41]. However, performance of such designs is more sensitive to process, voltage and temperature compared to regular OTA based designs. Table 1.1 summarizes the experimental results of the recently-published SC ADCs utilizing the low-power techniques described in Section 1.2.

Table 1.1: Performance summary of the recently-published SC ADCs using the low-power techniques presented in Section 1.2.

	ADC Type	Technology	Signal BW	SNDR	Power	FOM-dB
 [10]	Pipeline	0.18 µm	3.95 MHz	52 dB	2.5 mW	144 dB
[13]	Pipeline	90 nm	25 MHz	62 dB	4.5 mW	159.4 dB
[15]	$\Delta\Sigma$	45 nm	0.833 MHz	47.7 dB	630 µW	139 dB
[16]	$\Delta\Sigma$	65 nm	2.5 MHz	70.4 dB	3.73 mW	158.5 dB
[18]	$\Delta\Sigma$	0.18 µm	16 kHz	61.1 dB	17 μW	150.8 dB
[21]	$\Delta\Sigma$	0.13 μm	24 kHz	89 dB	1.5 mW	161 dB
[22]	$\Delta\Sigma$	0.13 µm	20 kHz	81.7 dB	35.2 μW	169.2 dB
[28]	Pipeline	0.18 µm	25 MHz	58.2 dB	9.9 mW	152.2 dB
[34]	$\Delta\Sigma$	0.18 µm	10 kHz	80.1 dB	$200 \ \mu W$	157.1 dB
[39]	$\Delta\Sigma$	0.18 µm	25 kHz	95 dB	870 μW	169.5 dB
[41]	$\Delta\Sigma$	0.18 µm	20 kHz	81 dB	36 µW	168.4 dB

1.3 Thesis Outline

The organization of the thesis is as follows:

 Chapter 2 provides background information on SC circuits, ΔΣ modulators and capacitive CPs.

- Chapter 3 presents the proposed CP based SC integrator and discusses its practical considerations.
- Chapter 4 describes the CP based SC gain circuit.
- Chapter 5 discusses the design of a prototype chip fabricated in a 0.13 μ m CMOS technology. The chip consists of two $\Delta\Sigma$ ADCs. One ADC makes use of conventional SC integrators, while the second ADC employs a CP integrator in the first stage.
- Chapter 6 presents the experimental results of the proposed CP and the conventional ADCs.
- Chapter 7 concludes the thesis and provides a brief discussion of future work.

Chapter 2

Background Information

This chapter provides an overview of SC circuits, $\Delta\Sigma$ modulators and CPs. In Section 2.1, the SC integrator and gain stage are described, and the effect of channel charge injection of switches in SC circuits are explained. Section 2.2 describes the need for oversampling in SC circuits processing small input signals. Section 2.3 discusses the suitability of a $\Delta\Sigma$ modulator to meet the power, bandwidth and resolution requirements of the ADC in this work. In Sections 2.4 and 2.5 background information on $\Delta\Sigma$ modulators and capacitive CPs are presented.

2.1 SC Circuits

SC circuits are typically used in high-resolution, low-speed applications. This is because they achieve higher linearity and dynamic range but lower bandwidth compared to continuous-time (CT) circuits. In this section, the most commonly used SC circuits, *i.e.*, the SC integrator and the gain stage are described.

2.1.1 SC Integrator

Figure 2.1(a) shows the circuit diagram of a conventional parasitic-insensitive SC integrator. Two-phase nonoverlapping clocks Φ_1 and Φ_2 control the switches and determine when the



Figure 2.1: (a) Conventional SC integrator (b) Nonoverlapping clocks Φ_1 and Φ_2 and their advanced versions Φ_{1a} and Φ_{2a} .

charge transfers occur in the sampling capacitor C_s and the integrating capacitor C_i . In Φ_2 the sampling capacitor C_s samples the input signal V_{in} . In Φ_1 the sampled charge on C_s is transferred to C_i through the virtual ground of the OTA. The output voltage of the SC integrator can be sampled during Φ_1 or Φ_2 . The two clock phases must be nonoverlapping so that no charge is lost during the charge transfer between C_s and C_i . As shown in the timing diagram of Figure 2.1(b), Φ_{1a} and Φ_{2a} in Figure 2.1(a) are advanced clocks, that is their falling edge occurs slightly before Φ_1 and Φ_2 . As will be discussed next, this arrangement of clock signals makes the charge-injection errors of the circuit signal independent.

Assuming that the initial integrator output voltage, sampled during Φ_2 , is $V_{out}(nT - T)$ the time-domain equation describing the charge transfer between the sampling and integrating capacitors is given by

$$C_{i}V_{out}(nT) = C_{s}V_{in}(nT - T) + C_{i}V_{out}(nT - T).$$
(2.1)



Figure 2.2: Using a dummy switch to minimize the channel charge injection error.

In this case, taking the Z-transform of (2.1) gives the transfer function of the SC integrator as follows:

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_s}{C_i} \frac{z^{-1}}{1 - z^{-1}}.$$
(2.2)

The C_s/C_i in (2.2) is defined as the integrator coefficient k

$$k = \frac{C_s}{C_i}.$$
(2.3)

Charge-Injection

In high-resolution SC circuits, channel charge injection of switches may limit the circuit's accuracy. When a MOSFET switch turns off, its channel charge exits through the source and drain terminals. Depending on the impedance of each terminal to ground and the transition time of the clock, different fractions of charge exit through either terminals [42]. If the charge injection of switches is signal independent it creates a dc offset. Otherwise, it can lead to a gain error or nonlinearity.

One method for minimizing the charge injection errors is by adding a dummy switch as shown in Figure 2.2. In this circuit, if the width of the dummy switch Q_{dmy} is one-half of the main switch Q_1 , and the clock transition time is fast, the charge injection of the main switch can considerably be reduced [43].

Another common technique shown for the SC integrator of Figure 2.1(a), is based on us-



Figure 2.3: Conventional SC gain stage.

ing advanced clocks for the switches that are connected to ground or the OTA virtual ground. As shown in Figure 2.1(b), the falling edge of Φ_{1a} and Φ_{2a} clock phases are slightly advanced compared to Φ_1 and Φ_2 , respectively. This way by turning off S_2 (S_4) before S_1 (S_3), the chargeinjection errors of the circuit will only be due to the early switches. Also since these switches are connected to ground or virtual ground, their charge-injection is signal-independent. Therefore, it introduces only an offset error rather than gain error or nonlinearity.

2.1.2 SC Gain Stage

Figure 2.3 shows a conventional SC gain stage. In this circuit, during Φ_2 the input signal V_{in} is sampled onto the sampling capacitor C_s , while the feedback capacitor C_f is reset. In Φ_1 , the sampled charge $C_s V_{in}$ is transferred to the feedback capacitor $C_f = C_s/G$ through the virtual ground of the OTA. The stage gain is given by

$$G = \frac{C_s}{C_f}.$$
(2.4)

In Figure 2.3, C_l represents the load capacitance of the next stage, sampling the first stage output during the amplification phase Φ_1 .

2.2 Oversampling

In high-resolution SC circuits with small inputs, to reduce the circuit area the input signal is typically oversampled. Oversampling occurs when the system sampling-rate f_s is higher than its Nyquist-rate $2f_0$, where f_0 is the input signal bandwidth. In this case, the OSR is defined as the ratio of the sampling frequency over the Nyquist-rate: $OSR = f_s/(2f_0)$.

Oversampling effectively reduces the required sampling capacitor size in SC circuits. The input-referred thermal noise power of a fully-differential SC integrator with an oversampling ratio of *OSR* is approximately given by [44]

$$N = \frac{4kT}{OSR.C_s},\tag{2.5}$$

where *k* is the Boltzmann constant, and *T* is the absolute temperature in degrees Kelvin. In this case, for a given input signal power *S* and thermal noise $SNR_{TH}(dB)$, the required capacitor size can be calculated as

$$C_s = \frac{4kT}{OSR} \frac{10^{SNR_{TH}(dB)/10}}{S}.$$
 (2.6)

For example, with a 400 mVpp differential input and $SNR_{TH}(dB) = 89$ dB, the required capacitor size with no oversampling (*OSR*=1) is $C_s = 657$ pF, which is too large to be implemented on-chip. Increasing the *OSR* to 128 reduces the capacitor size to 5.1 pF, which can easily be integrated on the chip.

2.3 ADC Architecture Selection

Given the low power, low bandwidth and high resolution requirements of the ADC, a $\Delta\Sigma$ modulator or a successive-approximation (SAR) ADC can be used to meet the specifications. SAR ADCs are power-efficient, as they do not require an OTA in the signal path. Recent implementations of SAR ADCs in literature have mainly targeted applications with medium-to-high bandwidth and lower than 10-bit accuracy [45–48]. In order to achieve higher accuracy, SAR ADCs typically require background digital calibration to cancel out the errors associated with capacitor mismatches [49–51]. The peak SNDR of the ADCs in [49–51] is 66.5 dB, 56.9 dB and 71.1 dB, respectively.

 $\Delta\Sigma$ modulators can achieve high resolution (>14 bits) without the need for digital calibration [21, 38, 39]. In $\Delta\Sigma$ modulators, oversampling and noise shaping are combined to improve the dynamic range (DR) of an internal ADC. As discussed in Section 2.2, the ADC in this work needs to be highly oversampled. Assuming that the quantization noise of the internal ADC has a white PSD, with no noise-shaping doubling the ADC OSR reduces the quantization noise power by half. This is equivalent to a SQNR improvement of 3 dB/octave obtained from straight oversampling. In a first-order $\Delta\Sigma$ loop however, doubling the OSR increases the SQNR by 9 dB, and in a second-order $\Delta\Sigma$ by 15 dB. The other advantage associated with noise shaping (especially with a high OSR) is that it relaxes the requirements on the circuit building blocks within the $\Delta\Sigma$ loop, hence they can be designed with a low power consumption.

2.4 Overview of $\Delta \Sigma$ Modulators

The block diagram of a general $\Delta\Sigma$ modulator ADC is shown in Figure 2.4. In this figure, H(z) is the loop filter transfer function. A signal transfer function (STF) and a noise transfer function (NTF) are defined for the input signal and the quantization noise, respectively:

$$STF(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)},$$
(2.7)

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)}.$$
(2.8)



Figure 2.4: A general $\Delta\Sigma$ modulator block diagram.

The modulator output can be expressed as a linear combination of the input signal and the quantization noise:

$$Y(z) = STF(z)U(z) + NTF(z)E(z).$$
(2.9)

Quantization noise shaping is achieved by choosing H(z) such that it has a large gain over the signal band f_0 and a small gain at out-of-band frequencies. In this case, the modulator input signal appears almost unchanged at the output $(STF(z) \approx 1)$, while in-band quantization noise is largely attenuated $(NTF(z) \ll 1)$. As an example, a linear model of a first-order $\Delta\Sigma$ modulator is shown in Figure 2.5(a). For this modulator the loop filter consists of a delaying integrator with

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}.$$
(2.10)

The modulator output signal in this case contains a delayed version of the input signal and a differentiated version of the quantization noise.

$$STF(z) = z^{-1},$$
 (2.11)

$$NTF(z) = 1 - z^{-1}.$$
(2.12)



Figure 2.5: (a) Linear z-domain model of a first-order $\Delta\Sigma$ modulator (b) and its STF/NTF.

The STF and the NTF magnitude plots of this modulator are shown in Figure 2.5(b). The STF shows a constant gain of one over all frequencies up to $f_s/2$, while the NTF shows a strong attenuation of quantization noise at frequencies which are small compared to the sampling-rate $f \ll f_s$.

2.5 Charge-Pumps

Charge-pumps (CPs) are circuit building blocks that are typically used to generate voltages higher than the power supply voltage. They have traditionally been used in nonvolatile mem-



Figure 2.6: Dickson CP.

ories and smart power integrated circuits (ICs) as DC/DC converters. The first on-chip implementation of a capacitive CP was the Dickson CP or the Dickson multiplier, shown in Figure 2.6 [52]. In this circuit, the input signal is a DC voltage equal to the power supply V_{dd} , and Φ_1/Φ_2 are two-phase nonoverlapping clocks switching between the power rails. When Φ_1 is low D_1 is on, and C_1 is charged up to V_{dd} if the voltage drop across the diode is assumed to be zero. When Φ_1 goes high, the voltage at the top plate of C_1 is pushed up to $2V_{dd}$. This turns off D_1 and turns on D_2 , hence C_2 begins to charge to $2V_{dd}$. Next when Φ_2 goes high, the top plate of C_2 is pushed up to $3V_{dd}$. This turns off D_2 and turns on D_3 , and C_3 charges to $3V_{dd}$ and so on with the charge passing over to the next stages of the CP. In practice using *n* stages in the CP does not produce an output voltage of nV_{dd} . The output voltage is reduced by the voltage drop across the diodes and the parasitic capacitances to ground at each node.

CPs have also been utilized in the implementation of boosted clock drivers [53,54]. Clockboosting reduces the on-resistance of the switches in low-voltage environments. Figure 2.7(a) shows the circuit diagram of a boosted clock driver. In this circuit, when the clock signal *Clk* is low, the capacitor C_2 is charged up to V_{dd} by transistor M_2 . When *Clk* becomes high, C_2 provides a boosted clock through transistor M_3 to the load transistor M_{sw} . Capacitor C_2 is typically much larger than C_1 , as it needs to drive the gate of many NMOS transistors, while C_1 only drives a single NMOS transistor M_2 . To prevent latch-up for the PMOS transistor M_3 , its well is tied to a bias voltage generated by a voltage doubler shown in Figure 2.7(b).

In this thesis, capacitive CPs are used to reduce the OTA power consumption in SC circuits.



Figure 2.7: (a) Boosted clock driver and (b) voltage doubler to bias the well of M_3 in (a).

As will be discussed in Chapters 3 and 4, CP based SC circuits have a lower load capacitance and a higher feedback factor compared to the conventional SC circuits. They also have reduced requirements on the OTA input-referred noise as a result of the input voltage multiplication.

2.6 Summary

In this chapter, the conventional parasitic-insensitive SC integrator and gain stage were described. The problem of charge injection associated with switches in SC circuits was explained, and techniques to minimize the effects of charge injection errors such as adding a dummy switch or using advanced clocks were reviewed. It was shown that oversampling can effectively reduce the circuit area in SC circuits processing small input signals. $\Delta\Sigma$ modulators and their noise shaping property, which enables them to achieve high resolution while having relaxed requirements on the accuracy of analog blocks were reviewed. The concept of voltage multiplication with capacitive CPs (used in this thesis to reduce the OTA power consumption in SC circuits) was discussed, and its existing applications in generating voltages higher than the power supply and in clock-boosting circuits were reviewed.
Chapter 3

Charge-Pump Based Switched-Capacitor Integrator

In this chapter, SC integrators employing capacitive charge-pumps are described. It is shown by analysis and simulation that for a given thermal noise performance, the proposed CP integrator consumes significantly lower power compared to a conventional SC integrator. Section 3.1 presents the proposed CP integrator circuit. Section 3.2 discusses the power savings achievable using this technique. In Section 3.3 the input-referred thermal noise of the CP integrator is compared with that of the conventional integrator. Transient simulation results are provided in Section 3.4. Practical effects in the CP integrator are discussed in Section 3.5. Section 3.6 extends the proposed technique to N > 2 sampling capacitors.

3.1 Charge-Pump Integrator

Figure 3.1(a) shows the circuit diagram of a conventional SC integrator with an integrator coefficient of k. The proposed CP integrator circuit is shown in Figure 3.1(b) [55]. In this circuit, during Φ_2 sampling capacitors $C_{s1}, C_{s2} = C_s/2$ sample the input signal. During Φ_1 , C_{s1} and C_{s2} are connected in series and discharged into the integrating capacitor $C_i=C_s/(2k)$





Figure 3.1: (a) Conventional SC integrator and (b) proposed CP integrator.

through the virtual ground of the OTA. Ignoring the parasitic capacitances, series connection of the sampling capacitors implements a voltage gain of two for the input signal $(2V_{in})$, stored across an equivalent input capacitance of $C_s/4$. In order to integrate the voltage $(V_{in} - V_{ref})$ in the CP integrator, $2V_{ref}$ is applied during Φ_1 , and the difference of the sampled charge in the two phases $C_s(V_{in} - V_{ref})/2$ is transferred to the output. The integrator coefficient in this case is given by

$$k = \frac{C_s}{2C_i}.$$
(3.1)

Alternatively, the required digital-to-analog converter (DAC) reference voltage in the CP

integrator can be halved by sampling it during Φ_2 [56].

3.2 CP Integrator Power Consumption

In SC $\Delta\Sigma$ modulators with a large OSR, the first integrator of the loop filter dominates the ADC performance and power consumption. The first stage OTA power consumption depends on the sampling-rate, thermal noise performance and the required settling accuracy. More specifically, sampling capacitors are sized to achieve sufficiently low thermal noise [57], and for a given sampling-rate and settling accuracy this translates to certain bandwidth and power dissipation for the first stage OTA. In Section 3.2.1 the achievable power saving of the CP integrator is derived using a linear feedback model for the integrator. Section 3.2.2 takes the effects of signal feedforward and partial slew-rate limitation into account.

3.2.1 Linear Feedback Model

For a single-stage class-A amplifier with linear settling, the input differential pair transconductance (g_m) is proportional to the power consumption of the amplifier. To achieve maximum power efficiency, the input differential pair are typically biased in weak inversion. Therefore, their transconductance is linearly proportional to their bias current I_D . In weak inversion

$$g_m = \frac{I_D}{nV_T} = \frac{I_{SS}}{2nV_T},\tag{3.2}$$

where $I_D = I_{SS}/2$ is the current flowing through one transistor of the input differential pair, *n* is the weak inversion slope factor and V_T is the thermal voltage [58]. The bias current I_D is a fixed percentage of the OTA total bias current, therefore

$$P_{OTA} \propto g_m, \tag{3.3}$$

where P_{OTA} is the OTA total power consumption. For instance, in a simple differential pair or a telescopic-cascode OTA, the current I_D is 50% of the total OTA bias current. In a foldedcascode OTA when the input devices are biased at the same current level as the output devices, or in a current-mirror OTA with a current gain of one, I_D is 25% of the total OTA bias current.

The required OTA transconductance for a given sampling-rate, thermal noise performance and settling accuracy is given by [43]

$$g_m = \frac{\omega_{-3dB}C_L}{\beta},\tag{3.4}$$

where ω_{-3dB} is the closed-loop -3 dB frequency, C_L is the load capacitance seen by the OTA, and β is the feedback factor. The required -3 dB bandwidth is determined by the modulator sampling-rate and the integrator settling accuracy specification. The effective load capacitance C_L and feedback factor β however depend on the integrator circuit topology. To reduce power one should minimize C_L and maximize β .

Ignoring the parasitics, C_L consists of the feedback network of the current stage, plus the load capacitance from the next stage C_l . Figure 3.2 shows the equivalent circuits of the conventional and CP integrators during the integration phase. For the conventional integrator C_L and β are given by

$$C_{L,Conv} = \frac{C_s}{k+1} + C_l, \qquad (3.5)$$

$$\beta_{Conv} = \frac{1}{k+1}.\tag{3.6}$$

For the CP integrator, they are found to be

$$C_{L,CP} = \frac{C_s/2}{k+2} + C_l,$$
(3.7)



Figure 3.2: Equivalent circuits of (a) the conventional and (b) CP integrators during the integration phase.

$$\beta_{CP} = \frac{2}{k+2}.\tag{3.8}$$

Hence the effective closed-loop load capacitance C_L/β of the conventional and CP integrators are as follows:

$$\left(\frac{C_L}{\beta}\right)_{Conv} = C_s + C_l(k+1),\tag{3.9}$$

$$(\frac{C_L}{\beta})_{CP} = \frac{C_s}{4} + C_l(\frac{k}{2} + 1).$$
(3.10)

If C_l can be neglected, (3.9) and (3.10) indicate that C_L/β of the CP integrator is 1/4 of the conventional integrator. It is noted that this overall reduction is due to both a smaller C_L and a larger β for the CP integrator.

As will be discussed in Section 3.3, the CP integrator achieves the same input-referred

thermal noise as the conventional integrator. Intuitively, during the sampling phase Φ_2 , the sampled thermal noise power of the CP and the conventional integrators are equal. During the integration phase Φ_1 , the sampled noise power of the CP integrator is four times larger than the conventional circuit, due to the series connection of C_{s1} and C_{s2} . However, this is offset by the gain of two for the input signal. Hence, both circuits require the same sampling capacitor size C_s to meet a given thermal noise performance. In this case for the same speed, thermal noise performance and settling accuracy, the required OTA transconductance in the CP integrator is four times smaller than the conventional integrator:

$$g_{m,CP} = \frac{g_{m,Conv}}{4}.$$
(3.11)

This corresponds to four times reduction in the CP OTA power consumption:

$$P_{OTA,CP} = \frac{P_{OTA,Conv}}{4}.$$
(3.12)

Power savings in (3.12) can ideally be achieved when the integrator output is sampled during Φ_2 in which case $C_l = 0$. However, if the integrator output is sampled during Φ_1 , the CP integrator OTA requires a transconductance higher than 1/4 of the conventional integrator OTA to drive its total capacitive load. Figure 3.3 plots the ratio of the required OTA transconductance in the CP and conventional integrators $g_{m,CP}/g_{m,Conv}$ for k = 0.5 as a function of C_l/C_s . The required transconductance in the CP integrator is less than 40% of the conventional circuit when $C_l/C_s = 0.2$. In $\Delta\Sigma$ modulators with a high OSR, the ratio of C_l/C_s is small. This is because any error including sampled thermal noise voltage from the circuits following the first stage, when referred back to the input is attenuated by the gain of the first integrator, which is quite high in the signal band. As a result, sampling capacitors of such following stages are typically much smaller than the first stage.

It is noted that the CP integrator circuit shown in Figure 3.1(b) uses double the reference voltage as compared to the conventional integrator. In applications where the modulator in-



Figure 3.3: Ratio of the required transconductance in the CP and conventional integrators for k = 0.5 as a function of C_l/C_s .

put signal is large, using $2V_{ref}$ may limit the ADC input range. Sampling the DAC reference voltage during Φ_2 makes the required reference same as the conventional circuit. In this case, cancelation techniques may also be required to minimize the nonlinearity of the parasitic capacitances [56]. On the other hand, in applications with small input signals sampling the reference voltage during Φ_1 reduces the capacitive load of the reference voltage buffers by a factor of four. Therefore, it achieves considerable savings in the power consumption of the reference buffers as well.

Table 3.1 summarizes different parameters of the conventional and CP integrator circuits for $C_l = 0$.

3.2.2 Integrator Signal Feedforward and Partial SR-Limitation

The power consumption analysis presented in Section 3.2.1 assumed a linear feedback system for the integrator. However, in the integration phase of a SC integrator the feedback capacitor C_i provides not only signal feedback, but also signal feedforward. Also, depending on the magnitude of the output step, the OTA response typically includes a slewing period followed

	Conventional	СР
Sampling Capacitor	C_s	C_s
Integrator Coefficient	k	k
Integrating Capacitor	C_s/k	$C_s/(2k)$
Feedback Factor β	1/(k+1)	2/(k+2)
Load Capacitance C_L	$C_s/(k+1)$	$C_s/(2(k+2))$
Required OTA g_m	$\omega_{-3dB}C_s$	$\omega_{-3dB}C_s/4$
Total Capacitance (Area)	$C_s(1+1/k)$	$C_s(1+1/(2k))$

Table 3.1: Circuit parameters of the CP and conventional integrators for $C_l = 0$.

by a linear period. In this case, settling speed depends not only on the OTA transconductance, but also on its slew-rate (SR). In order to find the effect of SR-limited settling on the CP integrator power savings, a more accurate analysis of the SC integrator during the integration phase is required.

Assuming an infinite DC gain for the OTA and $C_l = 0$, the closed-loop transfer function of the SC integrators in Figure 3.1 during the integration phase is given by

$$\frac{V_{out}}{V_{in}}(s) = k \frac{1 - s/\omega_z}{1 + s/\omega_{-3dB}},$$
(3.13)

where for the conventional integrator

$$\omega_{-3dB,Conv} = \frac{g_{m,Conv}}{C_s} \quad , \quad \omega_{z,Conv} = \frac{g_{m,Conv}}{C_s/k} \tag{3.14}$$

and for the CP integrator

$$\omega_{-3dB,CP} = \frac{g_{m,CP}}{C_s/4} , \quad \omega_{z,CP} = \frac{g_{m,CP}}{C_s/(2k)}.$$
 (3.15)

The typical settling behavior of a SC integrator is illustrated in Figure 3.4. Here $K_z > 1$ causes an initial step in the output response and increases the overall voltage change from $V_{o,step}$ to



Figure 3.4: OTA settling behavior during the integration phase.

 $K_z V_{o,step}$. The value of K_z is given by

$$K_z = 1 + \frac{\omega_{-3dB}}{\omega_z}.$$
(3.16)

The CP integrator has a larger K_z compared to the conventional integrator as follows:

$$\frac{K_{z,CP}}{K_{z,Conv}} = \frac{k+2}{k+1}.$$
(3.17)

Also the OTA's slewing period T_{SR} in a SC integrator is given by [59]

$$T_{SR} = \frac{K_z |V_{o,step}|}{SR} - \tau.$$
(3.18)

For a single-stage OTA where bandwidth and SR are determined by the same amount of current I_{SS} , the ratio of the slewing periods in the CP and conventional integrators can be expressed as (For derivation of (3.19), see Appendix A)

$$\frac{T_{SR,CP}}{T_{SR,Conv}} = \frac{1}{2} \frac{I_{SS,Conv}}{I_{SS,CP}} \frac{|V_{o,step}/k| - V_{ov}/2}{|V_{o,step}/k| - V_{ov}},$$
(3.19)

where $V_{o,step}/k$ is the input-referred voltage step of the integrator, and $V_{ov} = 2nV_T$ is the overdrive voltage of the input differential pair biased in weak inversion. The assumption of the



Figure 3.5: A folded-cascode OTA with equal input and output branch currents.

OTA closed-loop bandwidth and SR being determined by the same current I_{SS} is the case for a folded-cascode OTA, where the input and output branch bias currents are equal, as shown in Figure 3.5. In this case, the OTA bandwidth and differential SR are given by

$$\omega_{-3dB} = \frac{\beta I_{SS}}{C_L V_{ov}},\tag{3.20}$$

$$SR = \frac{I_{SS}}{C_L}.$$
(3.21)

Similarly, this is the case for a differential pair, a telescopic-cascode OTA or a current-mirror OTA with a current gain of one between the input and output branches [43].

Equation (3.19) indicates that if $I_{SS,CP} = I_{SS,Conv}/4$ and $|V_{o,step}/k| >> V_{ov}$, the slewing period in the CP integrator is almost two times larger than the conventional integrator. This reduces the available time for linear settling in the CP integrator, and requires a CP OTA

transconductance higher than that given by (3.11). On the other hand, if $I_{SS,CP} = I_{SS,Conv}/2$, the slewing periods become almost equal. In this case, linear settling times are almost the same, while the final settling error of the CP integrator is smaller than the conventional integrator, as a result of a doubled -3 dB bandwidth.

In a general case, to find an estimate of the achievable power savings in the CP integrator, a theoretical minimum current for the OTAs [60] in the CP and the conventional integrators can be derived. In this approach, the integration phase is partitioned into a slewing period (T_{SR}) and a linear settling period (T_{LIN}) as shown in Figure 3.4. The required current for linear settling with N' time constants during the integration phase is given by

$$I_{SS,LIN} = \frac{N' V_{ov}}{\beta T_{LIN}} C_L.$$
(3.22)

Using (3.18) the required slewing current during T_{SR} is found to be

$$I_{SS,SR} = \frac{K_z |V_{o,step}|}{\tau + T_{SR}} C_L.$$
(3.23)

For the conventional and CP integrators, the required linear and slewing currents can be plotted versus the partition ratio T_{SR}/T_{INT} , as shown in Figure 3.6. The optimum partition ratio and the minimum bias current occur at the intersection of the two curves. As can be seen from the graphs, the optimum slewing period increases for the CP integrator compared to the conventional integrator. The plots in Figure 3.6 are based on N' = 12, $C_s = 10pF$, $V_{ov} = 2nV_T = 80mV$, k = 0.5 and $T_{INT} = 0.2\mu s$. The maximum differential input-referred step size is assumed to be $V_{o,step}/k = 150mV$, which corresponds to the $\Delta\Sigma$ modulator implemented in this thesis. The ratio of the minimum OTA currents in the CP and conventional integrators determines the achievable power saving. In this case, the CP integrator's minimum OTA current is 28.6% of that of the conventional integrator. Table 3.2 compares the results for three different



Figure 3.6: Theoretical linear and SR OTA currents I_{SS} required in (a) the conventional and (b) CP integrators for a differential input-referred voltage step of 150 mV.

input-referred steps of 350 mV, 250 mV and 150 mV. It can be seen that the power saving of the CP integrator increases for smaller step voltages. In $\Delta\Sigma$ modulators with a large OSR and a unity-gain STF in the signal band, multi-bit quantization reduces the step size of the SC integrator and makes the OTA response more linear [39]. Therefore, it helps to maximize the achievable power saving using the CP based technique.

Table 3.2: Optimum slewing fraction of the integration phase and the CP integrator current consumption relative to the conventional integrator for three input-referred step voltages.

$V_{o,step}/k$	350 mV	250 mV	150 mV
$T_{SR,Conv}/T_{INT}$	22%	15%	7%
$T_{SR,CP}/T_{INT}$	39.2%	30.5%	18.7%
$I_{SS,CP}/I_{SS,Conv}$	32.1%	30.5%	28.6%

3.3 CP Integrator Thermal Noise

3.3.1 Input-referred Thermal Noise Analysis

In this section input-referred thermal noise of the CP integrator caused by the switches and the OTA is derived [61]. Figure 3.7 illustrates the CP integrator circuit, where the input and reference voltages are set to zero for noise analysis. Also, conducting switches in each clock phase are replaced by their noise voltages and on-resistances, R_{on} . This is shown in Figure 3.8 for phase Φ_2 , where noise voltages and on-resistances of the series switches are combined. During Φ_2 , the mean-square (MS) value of the noise charge sampled from switches $S_1 - S_4$ onto C_{s1} and C_{s2} is: $kTC_{s1} = kTC_{s2} = kTC_s/2$. As shown in the figure, during Φ_1 the capacitors are reconfigured and the noise charge is redistributed. The noise charge entering C_i during Φ_1 is the same as the change in charge of the series capacitors C_{s1} and C_{s2} . The MS value of this noise charge is found to be:



Figure 3.7: CP integrator circuit used for noise analysis.



Figure 3.8: CP integrator sampling network during Φ_2 , and the noise charge redistribution during Φ_1 .

$$\overline{\Delta q_{C_i,\Phi_2}^2} = kTC_{eq} = \frac{kTC_s}{4}.$$
(3.24)

The equivalent noisy circuit during the integration phase Φ_1 is shown in Figure 3.9, where V_{n5-7} and $3R_{on}$ represent the combined voltage noise of the switches $S_5 - S_7$ and their onresistances, respectively. The OTA has an input-referred noise voltage of V_{no} and is modeled by a transconductance g_m in parallel with an output resistance R_{out} . Analysis of this circuit for large R_{out} gives the MS noise charge added to C_i by the switch noise sources during each Φ_1 phase as:



Figure 3.9: CP integrator during Φ_1 with the switches and the OTA noise sources.

$$\overline{\Delta q_{C_i,\Phi_1,SW}^2} = \frac{kTC_s}{4} (\frac{1}{1 + 1/3R_{on}g_m}).$$
(3.25)

If the OTA noise is dominated by the input differential pair, its input-referred thermal noise PSD, assuming long-channel devices, is given by

$$S_{OTA}(f) = \frac{16kT}{3g_m} \tag{3.26}$$

In this case, its contribution to the added noise charge on C_i during Φ_1 can be calculated as

$$\overline{\Delta q_{C_i,\Phi_1,OTA}^2} = \frac{kTC_s}{4} (\frac{4/3}{1+3R_{on}g_m}).$$
(3.27)

Since the three noise components above are uncorrelated, the MS value of the total noise is the sum of the individual MS values. Expressing the total noise in terms of the voltage change across C_i during Φ_1 results in

$$\overline{\Delta V_{C_i}^2} = \frac{kTC_s}{4C_i^2} \left(1 + \frac{1}{1 + 1/3R_{on}g_m} + \frac{4/3}{1 + 3R_{on}g_m}\right).$$
(3.28)



Figure 3.10: In-band input-referred thermal noise power of the CP and conventional integrators for $C_s = 8pF$ and OSR = 128.

Dividing (3.28) by the square of the CP integrator coefficient in (3.1), and the OSR yields the MS value of the in-band input-referred noise voltage as:

$$\overline{V_{N,in,CP}^2} = \frac{kT}{C_s.OSR} \left(1 + \frac{1}{1 + 1/3R_{on}g_m} + \frac{4/3}{1 + 3R_{on}g_m}\right).$$
(3.29)

It is shown that the baseband input-referred noise power of the conventional SC integrator is given by [57]:

$$\overline{V_{N,in,Conv}^2} = \frac{kT}{C_s.OSR} \left(1 + \frac{1}{1 + 1/2R_{on}g_m} + \frac{4/3}{1 + 2R_{on}g_m}\right).$$
(3.30)

Figure 3.10 plots the in-band input-referred noise power of the conventional and CP integrators versus $x = g_m R_{on}$ for a sampling capacitor of $C_s = 8pF$ and OSR = 128. It is noted that in power efficient implementations where OTA dominates noise and bandwidth $x \ll 1$. On the other hand, $x \gg 1$ yields the minimum possible noise for a given capacitor size.

The assumption of the OTA thermal noise being dominated by the input differential pair is a good approximation for a simple differential pair or a telescopic-cascode OTA. However, in



Figure 3.11: In-band input-referred thermal noise power of the CP and conventional integrators for $C_s = 8pF$, OSR = 128, and an OTA with $N_f = 2.5$.

other OTA structures such as the folded-cascode OTA the input-referred thermal noise PSD is higher. In this case, the OTA input-referred thermal noise PSD is represented by

$$S_{OTA}(f) = \frac{16kTN_f}{3g_m} \tag{3.31}$$

where N_f is the OTA noise excess factor [62]. Using (3.31) the expressions for the inputreferred thermal noise power of the CP and conventional integrators will be given by

$$\overline{V_{N,in,CP}^2} = \frac{kT}{C_s.OSR} \left(1 + \frac{1}{1 + 1/3R_{on}g_m} + \frac{4N_f/3}{1 + 3R_{on}g_m}\right),\tag{3.32}$$

$$\overline{V_{N,in,Conv}^2} = \frac{kT}{C_s.OSR} \left(1 + \frac{1}{1 + 1/2R_{on}g_m} + \frac{4N_f/3}{1 + 2R_{on}g_m}\right).$$
(3.33)

Figure 3.11 compares the input-referred noise power of the CP and conventional circuits using a folded-cascode OTA with $N_f = 2.5$. The sampling capacitor and the OSR in this figure are the same as Figure 3.10.

3.3.2 Simulation Results

SC circuits noise simulation feature in SpectreRF (Pnoise) was used to verify the CP integrator noise analysis presented above [63]. For the simulations, the CP integrator of Figure 3.7 was implemented in behavioral form. Specifically each switch was modeled as an ideal switch in series with an on-resistance R_{on} , which included thermal noise. The OTA was modeled as shown in Figure 3.9 with a dc gain of A = 1000 and an input-referred noise PSD of $S_{OTA}(f) =$ $16kT/(3g_m)$. Also, $C_s = 8pF$, $R_{on} = 200\Omega$, $T = 300^{\circ}K$ and OSR = 128 were assumed. The OTA transconductance in the conventional integrator $g_m = 8mA/V$ and in the CP integrator $g_m = 2mA/V$ was used.

Table 3.3 shows the input-referred thermal noise power of the conventional and CP integrators obtained from analysis and simulation. Simulation results confirm the analysis presented above, and indicate that the CP integrator achieves almost the same input-referred thermal noise while having 1/4 of the OTA transconductance compared to the conventional integrator.

Table 3.3: Simulated vs. calculated input-referred thermal noise power in the CP and conventional SC integrators for $C_s = 8pF$ and OSR = 128.

	CP/Calc.	CP/Sim.	Conv/Calc.	Conv/Sim.
$V_{N,in}^2(dBV)$	-110.5	-110.6	-110.6	-110.7

3.4 CP Integrator Transient Simulations

3.4.1 Integrator Settling Behavior Simulations

Spectre simulations were used to verify the settling behavior of the CP and conventional integrators. The first stage CP and conventional integrators of the $\Delta\Sigma$ modulators implemented in this work (as will be described in Chapter 5) were simulated with differential input voltage steps of 50 mV and 150 mV. A 50 mV voltage step corresponds to the standard deviation of the input signal to the first stage CP and conventional integrators of the $\Delta\Sigma$ modulators; while a 150 mV voltage step corresponds to the maximum input signal to the first stage integrators. The CP integrator OTA (1X) in this work is designed to be three times smaller than the conventional integrator OTA (3X), therefore it consumes three times lower power. For comparison, the conventional integrator was also simulated with the 1X OTA.

Figure 3.12(a) shows the simulated output response of the CP/1X, Conv/3X and Conv/1X integrators for a 150 mV voltage step. Simulations also show that the CP/1X integrator has a larger step in its output response at the beginning of the integration phase. In order to compare the settling speed of the integrators, the percentage of settling error versus time for the transient responses of Figure 3.12(a) is shown in Figure 3.12(b). The horizontal line in this figure indicates the settling error required for 15-bit accuracy. To reach this accuracy, the CP/1X integrator is much slower than the CP/1X and Conv/3X integrators. As a result, its settling error near the end of the integration phase is larger than that of the CP/1X and Conv/3X integrators by more than three orders of magnitude.

Figure 3.13(a) shows the simulated output response of the integrators for a 50 mV voltage step. In this case, OTA settling in both integrators is more linear. To reach 15-bit accuracy the CP integrator settling time is 163 ns, while the conventional integrator settling time is 182 ns. The larger settling time difference between the CP and conventional integrators shows that the CP integrator power saving in the case of 50 mV voltage step is larger than the 150 mV step.

3.4.2 Second Order Modulator Simulations

The CP integrator was simulated in a $\Delta\Sigma$ modulator loop and its thermal noise and settling performance was compared with that of a conventional integrator. The integrators were employed as the first stage of a second-order low-distortion $\Delta\Sigma$ modulator [37] utilizing a 5-level quantizer.

Figure 3.14 shows the block diagram of the $\Delta\Sigma$ modulator. First and second stage integrators sample and integrate during the same clock phases. Therefore, the second stage does



Figure 3.12: (a) Simulated output response of the CP/1X, Conv/3X and Conv/1X integrators implemented in this work for a differential input voltage step of 150 mV (b) Percentage of settling error versus time in the waveforms shown in (a).



Figure 3.13: (a) Simulated output response of the CP/1X, Conv/3X and Conv/1X integrators implemented in this work for a differential input voltage step of 50 mV (b) Percentage of settling error versus time in the waveforms shown in (a).



Figure 3.14: Second-order input feed-forward $\Delta\Sigma$ modulator.

not load the first stage during its integration phase. In the first stage CP and conventional integrators, the OTAs and the capacitors were realized using transistors and metal-insulatormetal (MIM) capacitors, respectively, from a typical 0.13 μ m CMOS process. To reduce transient noise simulation time, switches of the first stage were modeled behaviorally as ideal switches in series with their on-resistance, which included thermal noise. Transistor thermal noise for the OTAs was also included in the simulations. Circuits beyond the first stage were implemented in behavioral form, and their thermal noise contribution was assumed to be negligible as a result of noise shaping. The modulator input sine-wave was 320 mV peak-to-peak differential (80% of a 400 mV differential reference voltage). The single-stage OTAs in the first stage used a folded-cascode architecture with one being four times larger (4X OTA) than the other (1X OTA), hence dissipating four times the power.

To demonstrate the advantage of the CP integrator versus the conventional SC integrator, modulator performance was evaluated when the following three circuits were used as the first stage integrator:

- (i) conventional integrator with the 4X OTA (Conv/4X),
- (ii) CP integrator with the 1X OTA (CP/1X), and
- (iii) conventional integrator with the 1X OTA (Conv/1X).

Figure 3.15 shows the SNDR performance of the three modulators versus the samplingrate for a fixed input signal bandwidth. To obtain the SNDR of each data point, $256 \times OSR$ samples were taken to calculate the fast Fourier transform (FFT). At sampling frequencies up to $F_s = 10$ MHz, where quantization noise is dominant over thermal noise and distortion due



Figure 3.15: Simulated SNDR of the second-order $\Delta\Sigma$ modulator of Figure 3.14, with first stage CP/1X, Conv/4X, and Conv/1X integrators.

to the OTA insufficient settling, all three modulators achieve almost the same SNDR. Also, at $F_s = 20$ MHz SNDR remains the same for the three modulators, as it is limited by thermal noise. As the sampling-rate increases to $F_s = 40$ MHz and 50 MHz, the SNDR of the Conv/4X and CP/1X modulators remains thermal noise limited and increases at a rate of approximately 3 dB/Octave. However at these frequencies, the Conv/1X integrator becomes severely limited by the OTA settling distortion, hence its modulator SNDR drops significantly.

3.5 Practical Effects in the CP Integrator

3.5.1 CP Parasitic Capacitances

Figure 3.16 shows the CP integrator circuit with the CP parasitics $C_{p1} - C_{p4}$ explicitly shown. Parasitic capacitors affect the input-referred thermal noise and the integrator coefficient as discussed below.



Figure 3.16: CP integrator circuit with the CP parasitics shown.

Effect on Thermal Noise

CP parasitics C_{p2} to C_{p4} reduce the low-frequency gain of the integrator, hence increase the input-referred thermal noise in the signal band.

In this section, the effect of parasitics on the input-referred thermal noise of the CP integrator tor is simulated using the SC circuits noise simulation feature in SpectreRF. The CP integrator shown in Figure 3.16 is implemented in behavioral form. The single-stage OTA is modeled by a transconductance (g_m) in parallel with an output resistance R_{out} , with a DC gain of A = 60 dB. Each switch is modeled as an ideal switch in series with an on-resistance R_{on} , which includes thermal noise. The OTA thermal noise is assumed to be dominated by the input differential pair. In this case its input-referred noise PSD is given by $S_{OTA}(f) = 16kT/(3g_m)$. The sampling capacitor and the sampling-rate are $C_s = 10pF$ and $F_s = 2.5MHz$, respectively. Other simulation parameters are as follows: $R_{on} = 200\Omega$, $g_m = 0.2mA/V$, $T = 300^{\circ}K$, and OSR = 128.

To include the effect of parasitics, bottom-plate parasitic capacitance $C_{p1,3} = C_{bp}$ was varied from 0 to 10% of the sampling capacitors, while keeping the top-plate parasitics equal to 1/4 of the bottom-plate parasitics. Also, parasitic capacitance of the switches was assumed to be 20 *fF* on each side. Figure 3.17 shows how the input-referred noise power changes with C_{bp} .

From Table 3.2, the CP integrator power consumption is about 30% of the conventional integrator. The maximum thermal noise increase, which occurs at $C_{bp} = 0.1C_{s1,2}$ is about



Figure 3.17: Effect of bottom-plate parasitics C_{bp} on the input-referred thermal noise of the CP integrator with $C_s = 10pF$ and OSR = 128.

0.7 dB. To compensate for this increase in the input-referred thermal noise, capacitor sizes in the CP integrator must be increased by 17.5%. This increases the power consumption of the CP integrator to 35% of the conventional circuit, which still involves a substantial saving in power consumption. In nanometer CMOS technologies with MIM capacitors, top and bottom-plate parasitic capacitances are typically small, hence their effect on the CP integrator thermal noise performance is also small.

Effect on the Integrator Coefficient

Assuming an infinite gain for the OTA, C_{p2} and C_{p3} in Figure 3.16 affect the gain coefficient of the integrator in the input and reference voltage paths. Ignoring the variations in the parasitics, their effect can be modeled as coefficient errors ε_1 and ε_2 shown in Figure 3.18(a), where ε_1 and ε_2 are given by

$$\varepsilon_1 = \frac{C_{p3}}{C_s + C_{p2} + C_{p3}},\tag{3.34}$$



Figure 3.18: (a) Modeling the CP integrator parasitics as coefficient errors ε_1 and ε_2 (b) coefficient errors as a function of C_{bp} .

$$\varepsilon_2 = \frac{C_{p2} + C_{p3}}{C_s + C_{p2} + C_{p3}}.$$
(3.35)

Figure 3.18(b) plots the errors as a function of bottom-plate parasitics C_{bp} . In this plot, C_{p2} and C_{p3} are assumed to be dominated by the top and bottom-plate parasitics of the sampling capacitors respectively, where $C_{tp} = C_{bp}/4$. The maximum percentage of coefficient error in the case of 10% parasitics is about 6%.

Variation in the modulator coefficients alters the NTF, and therefore the amount of quantization noise suppression in the signal band. However, performance change in the case of single-loop modulators is negligible [64]. For instance, variation in the baseband quantization noise power of the $\Delta\Sigma$ modulator of this work, when ε_1 and ε_2 vary within the range shown in Figure 3.18(b), is less than 0.7 dB.

It is noted that parasitic capacitors can also cause distortion if they are nonlinear. However in applications with small input signals, such as sensory and wireless systems, performance is fundamentally limited by thermal noise as opposed to linearity.

3.5.2 Capacitor Mismatch

In practice sampling capacitors C_{s1} and C_{s2} deviate from their nominal value $C_s/2$. Such variations affect their equivalent series capacitance during the integration phase, and modify the CP integrator coefficient. However, as noted in Section 3.5.1, single-loop $\Delta\Sigma$ modulators are generally tolerant of large coefficient errors. Therefore variation in their performance caused by capacitor matching errors is insignificant.

3.5.3 OTA Finite Gain and Offset

The time-domain output of a delaying SC integrator with finite OTA gain (A) and offset (V_{OS}) can be expressed as

$$V_{out}(nT) = k\alpha_A V_{in}(nT - T) + \beta_A V_{out}(nT - T) + \gamma_{OS} V_{OS}$$
(3.36)

Here α_A modifies the integrator gain, β_A is the shifted pole location, and γ_{OS} is the gain seen by the OTA offset voltage. Table 3.4 shows the values of the above coefficients for the conventional and CP integrators. In this Table μ represents the inverse of the OTA gain ($\mu = 1/A$), and for the CP integrator parasitics in the CP are ignored. It is seen that α_A and β_A for the CP integrator are closer to the ideal value of one compared to the conventional integrator. For instance, the pole location in the CP integrator can be approximated as $\beta_{A,CP} \approx 1 - k\mu/2$, while for the conventional integrator $\beta_{A,Conv} \approx 1 - k\mu$.



Table 3.4: α_A , β_A and γ_{OS} in the CP and conventional integrators.

Figure 3.19: SQNR of the CP and conventional $\Delta\Sigma$ modulators of this work versus the first stage OTA DC gain.

The effect of finite OTA gain on the CP and conventional integrators was simulated in Spectre. For the simulations, the second order $\Delta\Sigma$ modulator of this work was modeled as behavioral schematics. The first integrator was implemented as both CP and conventional circuits. The second integrator was assumed to be a conventional integrator with a DC gain of A = 60 dB. Figure 3.19 shows the SQNR of the modulators versus the first stage OTA DC gain. It is seen that the performance of the modulator with a CP based front-end integrator is less sensitive to finite OTA gain.

In terms of the OTA offset voltage, γ_{OS} in the CP integrator is almost two times smaller than the conventional circuit. Therefore to achieve the same input-referred offset, the OTA offset voltage in the CP integrator can be two times larger than the conventional integrator. Since the OTA offset standard deviation is proportional to $1/\sqrt{WL}$, where W and L are transistor



Figure 3.20: CP integrator with N > 2 sampling capacitors.

dimensions, OTA scaling by four according to (3.12) results in the same input-referred offset voltage for the CP integrator as the conventional integrator.

3.6 CP Integrator with N Sampling Capacitors

The idea of using capacitive CPs at the input of a SC integrator can be generalized by splitting the sampling capacitor into N > 2 capacitors during Φ_2 as shown in Figure 3.20. The Nsampling capacitors are subsequently connected in series during Φ_1 and driven by NV_{ref} to integrate the voltage $V_{in} - V_{ref}$ onto the integrating capacitor $C_i = C_s/(Nk)$ with a gain of k. In this case, the power consumption can ideally be reduced by a factor of N^2 compared to the conventional integrator. However, with the effect of nonlinear settling taken into account the power savings decrease. The analysis presented in Section 3.2.2 is performed for the CP integrator with N = 3 sampling capacitors (CP3). The results in this case are shown in Table 3.5. For a 150 mV input-referred voltage step, the ratio of the minimum OTA currents in the CP and conventional integrators is $I_{CP3}/I_{Conv} = 14.3\%$.

Also in this case, parasitic capacitances at the various nodes of the CP increase the input-

 I_{CP3}/I_{Conv}

	υ		1	
$V_{o,step}/k$	350 mV	250 mV	150 mV	•
$T_{SR,Conv}/T_{INT}$	22%	15%	7%	
$T_{SR,CP3}/T_{INT}$	50.2%	41%	27.7%	

16%

14.3%

Table 3.5: Optimum slewing fraction of the integration phase and the CP3 integrator current consumption relative to the conventional integrator for three input-referred step voltages.

17.4%

referred thermal noise. For instance, assuming $C_{bp} = 0.05C_{s1-3}$, $C_{tp} = C_{bp}/4$ and 20 *fF* parasitics on each side of the switches, the input-referred thermal noise increase is about 0.9 dB. Including this thermal noise increase into account, the power consumption of the CP integrator becomes 17.6% of the conventional integrator. This corresponds to an OTA scaling by a factor greater than 5. In general, by using larger number of capacitors in the CP the effect of non-idealities such as the OTA SR limitation, the integrator thermal noise increase and coefficient variations caused by the parasitics in the CP will also increase. In practice, the choice of the number of capacitors in the CP is determined by the modulator input signal swing, the modulator architecture including the number of levels in the quantizer and its sensitivity to coefficient variations, as well as the percentage of parasitics at the intermediate nodes of the CP.

3.7 Summary

Using a CP with *N* capacitors at the input sampling network of a SC integrator can ideally reduce the OTA power consumption by N^2 . The above power savings can be achieved for the CP integrator, while maintaining the same input-referred thermal noise and settling performance as the conventional integrator. In practice, depending on the input step size to the integrator, the power savings may be limited by the OTA partial SR-limitation. Parasitics in the CP increase the integrator input-referred thermal noise as well as modify the integrator coefficient. The increase in the thermal noise also reduces the CP integrator power savings. The integrator coefficient errors caused by the CP parasitics have a negligible effect on the SQNR performance of single-loop $\Delta\Sigma$ modulators. In multi-stage noise shaping (MASH) $\Delta\Sigma$ ADCs, such errors may need to be digitally calibrated to cancel out the effects of quantization noise leakage at the output of the modulator. Nonlinear parasitics can also cause distortion and degrade the modulator SNDR if the input signal is large. However in applications with small inputs, such as wireless and sensory systems, performance and power consumption are fundamentally limited

by thermal noise. In such applications, the CP integrator technique can considerably reduce

the power consumption of dominant front-end circuits.

Chapter 4

Charge-Pump Based Switched-Capacitor Gain Stage

In Chapter 3, a technique using capacitive CPs was proposed to considerably reduce the power consumption in thermal noise limited SC integrators. In this chapter, the technique is extended to SC gain stages [65]. It is shown that the proposed approach can achieve similar power savings in SC gain stages at the front-end of SC systems. Since the power consumption of the front-end circuits with small inputs is generally higher than the circuits at the back-end of the signal processing chain, reducing their power can significantly improve the system FOM.

4.1 CP Gain Stage

Figure 4.1(a) shows the circuit diagram of the conventional SC gain amplifier. The proposed CP gain stage is shown in Figure 4.1(b). In this circuit, during Φ_1 sampling capacitors $C_{s1}, C_{s2} = C_s/2$ sample the input signal, while the feedback capacitor C_f is reset. During Φ_2 , C_{s1} and C_{s2} are connected in series to provide a voltage gain of two. The sampled charge $C_sV_{in}/2$ is transferred to the feedback capacitor, $C_f = C_s/(2G)$, and results in a closed-loop voltage gain





Figure 4.1: (a) Conventional SC gain stage (b) Proposed CP gain stage.

of G given by

$$G = \frac{C_s}{2C_f}.$$
(4.1)

The CP gain circuit can also be implemented with N > 2 sampling capacitors. In this thesis however, we focus on the case of two sampling capacitors C_{s1} and C_{s2} .

4.2 CP Gain Stage Power Consumption

Similar to a SC integrator, the transconductance of the OTA in a SC gain stage represents its power consumption. The required OTA transconductance for a given thermal noise level and settling accuracy is proportional to

$$g_m \propto \frac{C_L}{\beta},$$
 (4.2)

where C_L is the load capacitance seen by the OTA and β is the feedback factor. Figure 4.2 shows the equivalent circuit diagrams of the conventional and CP gain stages during the amplification phase Φ_2 . Ignoring the parasitics, C_L consists of the feedback network of the current stage, plus the load capacitance from the next stage C_l .

The effective closed-loop load capacitance C_L/β of the conventional and CP gain circuits are as follows:

$$\left(\frac{C_L}{\beta}\right)_{Conv} = C_s + C_l(G+1),\tag{4.3}$$

$$(\frac{C_L}{\beta})_{CP} = \frac{C_s}{4} + C_l(\frac{G}{2} + 1).$$
(4.4)

If loading from the next stage C_l is negligible, (4.3) and (4.4) indicate that C_L/β of the CP gain stage is 1/4 of the conventional circuit. As will be shown in Section 4.3, the CP gain stage achieves almost the same input-referred thermal noise, and therefore requires the same size sampling capacitor C_s as the conventional circuit. In this case, the required OTA transconductance (g_m) in the CP gain circuit can be four times smaller than the conventional circuit. For a single-stage class-A OTA with linear settling, this corresponds to four times reduction in power consumption.



Figure 4.2: (a) Equivalent circuits of (a) the conventional and (b) CP gain stages during the amplification phase.

The load capacitance C_l in thermal noise limited applications is determined by the inputreferred thermal noise of the second stage. The sampled noise power of the second stage, when referred to the input, is reduced by the square of the first stage gain *G*:

$$N_{2,in} \propto \frac{kT/C_l}{G^2},\tag{4.5}$$

With a higher first stage gain G, a smaller C_l can be used to meet a given thermal noise performance. Table 4.1 shows the ratio of the required transconductance in the CP and conventional circuits for different combinations of G and C_l . In this Table, the ratio of C_l/C_s is selected to be G^{-x} , where $1.2 \le x \le 1.4$ [66]. It can be seen that the achievable saving in the CP OTA transconductance (power) increases for larger closed-loop gains G.

On the other hand, in order to achieve a certain voltage gain from one or more SC gain

G(V/V)	C_l/C_s	gm,CP/gm,Conv
2	42%	48%
4	16%	40%
8	5%	34%

Table 4.1: CP gain stage transconductance for different stage gains (G) and load capacitances C_l .

stages, maximizing the first stage gain minimizes the overall power consumption. For example it has been shown that in pipeline ADCs, increasing the number of bits resolved in the first stage results in a lower overall power consumption for the MDACs [66], [67]. Based on the above, the CP gain stage can significantly reduce the power consumption of the high-gain front-end amplifiers in SC systems.

Similar to the analysis presented in Section 3.2.2, the effects of signal feed-forward and the OTA SR limited settling can also be taken into account. Table 4.2 compares the optimum slewing fraction of the amplification phase and the ratio of the required OTA currents in the two circuits for different input-referred voltage steps. The results in the Table are based on N' = 12, $C_s = 8pF$, $C_l = 0.4pF$, $V_{ov} = 80mV$ and G = 8V/V.

Table 4.2: Optimum slewing fraction of the amplification phase and the CP gain stage current consumption relative to the conventional gain stage, as a function of the input-referred voltage step.

$V_{o,step}/G$	400 mV	300 mV	200 mV	100 mV
$T_{SR,Conv}/T_{AMP}$	25%	18.7%	11.2%	2.2%
$T_{SR,CP}/T_{AMP}$	42.7%	35.2%	25%	11.2%
$I_{SS,CP}/I_{SS,Conv}$	45.3%	43.3%	40.8%	38.0%

4.3 CP Gain Stage Thermal Noise

In this section the input-referred thermal noise of the CP and conventional gain stages are simulated and compared using the SC circuits noise simulation feature in SpectreRF. The gain cir-
cuits shown in Figures 4.1(a) and 4.1(b) are implemented in behavioral form with a closed-loop gain of G = 8V/V. Each switch is modeled as an ideal switch in series with an on-resistance R_{on} , including thermal noise. The OTA is modeled by a transconductance (g_m) in parallel with an output resistance R_{out} , with a DC gain of A = 60 dB. The OTA thermal noise is assumed to be dominated by the input differential pair and $\gamma = 2/3$ for long-channel devices. The sampling capacitors and the sampling-rate are $C_s = 8pF$ and $F_s = 25MHz$ respectively. Other circuit parameters are as follows: $C_l = 0.4pF$, $R_{on} = 200\Omega$, $g_{m,Conv} = 6mA/V$, $g_{m,CP} = 2mA/V$ and $T = 300^{\circ}K$. The CP OTA transconductance is 1/3 of the conventional OTA transcoductance, which corresponds to the transconductance saving shown in Table 4.1 for G = 8V/V. The input-referred thermal noise of each gain circuit due to Φ_1 and Φ_2 switches and the OTA are simulated separately. The results are shown in Table 4.3.

Table 4.3: Input-referred thermal noise simulation results for the conventional and CP gain stages with $C_s = 8pF$ and G = 8V/V.

	$N_{in,Conv}(dBV)$	$N_{in,CP}(dBV)$
Φ_1 Switches	-92.4	-92.0
Φ_2 Switches	-94.6	-96.7
OTA	-94.0	-93.8
All Noise Sources	-88.8	-89.0

Analytical expressions for the input-referred thermal noise of the conventional and CP gain stages due to Φ_1 switches are given by

$$N_{in,Conv,\Phi_1,sw} = \frac{kT(1+1/G)}{C_s},$$
(4.6)

$$N_{in,CP,\Phi_1,sw} = \frac{kT(1+2/G)}{C_s}.$$
(4.7)

The calculated noise power of the conventional and CP based circuits due to Φ_1 switches are -92.3 dBV and -91.9 dBV respectively. The calculated noise powers agree very well with the



Figure 4.3: CP gain stage with the CP parasitic capacitances shown.

simulated results.

The noise power due to the Φ_2 switches and the OTA do not have simple expressions, hence are not analyzed in this thesis. It is noted however that the series connection of the sampling capacitors C_{s1} and C_{s2} in the CP gain circuit during Φ_2 does not affect the input-referred thermal noise power. This is because the four times increase in the sampled noise power is offset by the voltage gain of two across the CP capacitors. Simulation results presented above confirm that for the same sampling capacitance C_s , the CP gain stage achieves the same input-referred thermal noise as the conventional gain stage, while having 1/3 of the OTA transconductance.

4.4 CP Parasitic Capacitances

Figure 4.3 shows the CP gain circuit with the CP parasitic capacitors $C_{p1} - C_{p4}$. Parasitic capacitors affect the stage gain and the input-referred thermal noise as discussed below.

4.4.1 Effect on the Stage Gain

Assuming an infinite gain for the OTA, C_{p2} and C_{p3} in Figure 4.3 modify the stage gain *G*. Neglecting the variations in the parasitics, the gain error introduced is found to be

$$\alpha = \frac{C_s + C_{p2}}{C_s + C_{p2} + C_{p3}},\tag{4.8}$$



Figure 4.4: (a) Gain error α caused by the parasitics in the CP (b) α as a function of bottomplate capacitance C_{bp} .

where $C_s = 2C_{s1,2}$ in Figure 4.3. The gain stage model in this case is shown in Figure 4.4(a). Figure 4.4(b) depicts the gain error α as a function of the bottom-plate parasitics. In this plot the bottom-plate parasitic capacitance $C_{p1,3} = C_{bp}$ is varied from 1% to 10% of the sampling capacitors $C_{s1,2}$, while keeping the top-plate parasitic capacitance $C_{p2,4} = C_{tp}$ equal to 1/4 of the bottom-plate parasitics. In this case, the maximum gain error introduced by the parasitics is about -0.4 dB when $C_{bp} = 0.1C_{s1,2}$.

4.4.2 Effect on Thermal Noise

Effect of parasitics on the input-referred thermal noise of the CP gain stage was investigated using SpectreRF simulations. The OTA model and other simulation parameters were the same as those in Section 4.3. To see the effect of parasitics associated with the sampling capacitors $C_{s1,2}$, bottom-plate parasitic capacitance $C_{p1,3} = C_{bp}$ was varied from 1% to 10% while keeping



Figure 4.5: Thermal noise increase of a CP gain stage with $C_s = 8pF$ and G = 8V/V due to the parasitic capacitors in the CP.

the top-plate parasitics equal to 1/4 of it. In the simulations, parasitics capacitance of the switches was assumed to be 20 fF on each side. Figure 4.5 shows how the input-referred noise power changes with C_{bp} .

From Table 4.1, a CP gain stage with G = 8V/V consumes 34% of the power of a conventional gain stage. Figure 4.5 shows that the maximum thermal noise increase which occurs at $C_{bp} = 0.1C_{s1,2}$ is about 0.6 dB. To compensate for this increase in the input-referred thermal noise capacitor sizes in the CP gain circuit must be increased by almost 15%. This increases the power consumption of the CP gain stage from 34% to 39% of the conventional circuit, which still provides a substantial saving of 61% in power consumption.

4.5 OTA Finite Gain

Finite OTA gain in a SC gain stage introduces a gain error α_A in the closed-loop gain of the amplifier G. In this case, the gain of the SC gain stage becomes $\alpha_A G$. It can be shown that α_A in the conventional and CP gain circuits are given by the expressions shown in Table 4.4. In this Table μ is the inverse of the OTA DC gain ($\mu = 1/A$). Figure 4.6 shows the closed-



Table 4.4: Stage gain error α_A caused by the finite OTA DC gain in the CP and conventional SC gain circuits.

Figure 4.6: Stage gain error α_A as a function of the finite OTA DC gain, in the CP and conventional gain amplifiers with G = 8V/V = 18.06 dB.

loop gain error α_A (dB) as a function of the OTA DC gain (dB) for a closed-loop gain of G = 8V/V = 18.06dB. It can be seen that the gain error (in dB) in the CP gain amplifier is smaller than the conventional gain circuit. Therefore, the CP gain stage is less sensitive to finite OTA gain.

4.6 CP Gain Stage Transient Simulations

The CP and conventional gain circuits were simulated in Spectre using the behavioral models described in Section 4.3. For these simulations the on-resistance of the switches was reduced to $R_{on} = 50\Omega$ so that the OTAs in both circuits mainly dominate the bandwidth. The OTA with $g_m = 2mA/V$ is the 1X OTA, while the one with $g_m = 6mA/V$ is the 3X OTA. For the CP circuit bottom-plate parasitics were assumed to be 5%, and the parasitic capacitance of the switches



Figure 4.7: DC gain performance of the Conv/3X, CP/1X, and Conv/1X gain stages versus sampling-rate.

was assumed to be 20 fF on each side.

To demonstrate the advantage of the CP gain stage compared to the conventional circuit, the following three circuits were simulated:

- (i) conventional gain stage with the 3X OTA (Conv/3X),
- (ii) CP gain stage with the 1X OTA (CP/1X), and
- (iii) conventional gain circuit with the 1X OTA (Conv/1X).

Figure 4.7 shows the DC gain of the three circuits versus sampling-rate (F_s). At $F_s = 25MHz$ all three circuits achieve almost the same low-frequency gain which is close to ~18 dB (G = 8 V/V). In this case the DC gain of the (CP/1X) circuit is about 0.2 dB lower than the (Conv/3X) circuit, as a result of the parasitics in the CP.

At high sampling-rates however, the low-frequency gain of the (Conv/1X) circuit drops significantly. For instance at $F_s = 100MHz$, the DC gain of the (Conv/1X) circuit is about 13.4 dB which is almost 4.3 dB lower than its DC gain at $F_s = 25MHz$. At $F_s = 100MHz$, the DC gains of the (Conv/3X) and (CP/1X) circuits are both around 17.1 dB. The large gain error in the (Conv/1X) circuit at high sampling frequencies is due to insufficient settling of the 1X OTA. It can be shown that linear incomplete OTA settling results in a gain error in

SC circuits [39]. This is especially the case in the front-end gain circuits used to amplify the small input signals in sensory and wireless systems. The baseband gain drop in a SC amplifier degrades the overall system performance by increasing the input-referred noise. For instance, a drop of 3 dB in the baseband gain of a first stage SC amplifier results in 3 dB higher inband input-referred noise from the circuits following the first stage. In addition, incomplete OTA settling in the (Conv/1X) gain amplifier makes the system performance sensitive to clock jitter, which is generally not desirable. Also, in the case of nonlinear OTA settling, incomplete settling leads to increased distortion at the output.

4.7 Summary

The CP based gain circuit is shown to achieve the same input-referred thermal noise and settling performance, while consuming less than half of the OTA power, compared to the conventional SC gain stage. It is shown that the power saving of the CP based circuit increases for larger closed-loop gains. The effects of SR limitation and CP parasitics on the power savings and performance are discussed. The CP gain stage is shown to be less sensitive to finite OTA gain compared to the conventional gain amplifier. Also, simulation results indicate that the CP based gain circuit has an improved DC gain versus sampling-rate trade-off compared to the conventional circuit.

Chapter 5

Charge-Pump Based Delta-Sigma ADC Prototype

This chapter discusses the design of a prototype IC implemented in this thesis [68]. The chip consists of two $\Delta\Sigma$ modulators. The first ADC employs a CP integrator, while the second ADC uses a conventional integrator in their first stages, respectively. Circuits beyond the first stage are identical between the two ADCs. This allows for a direct comparison of the proposed CP based technique with the conventional approach. Section 5.1 presents the design specifications of the $\Delta\Sigma$ modulators. Section 5.2 discusses the system level design of the ADCs. Circuit implementation is described in Section 5.3.

5.1 ADC Specifications

The ADC specifications in this thesis are 14-bit resolution over a 10 kHz signal bandwidth, with a power consumption less than 200 μ W. The challenge in low power design is due to a small input signal of 400 mVpp differential.

5.2 System-Level Design

5.2.1 Modulator Architecture

A number of architectural choices in the design of $\Delta\Sigma$ modulators are the single-loop versus MASH topology, the modulator order (*L*), the OSR and the number of quantization levels (*M*). For the CP based modulator, a single-loop topology is preferred over a MASH $\Delta\Sigma$, due to its robustness to coefficient variations in the CP integrator. Also, given the high resolution and small input signal of the ADCs, the OSR must be relatively high to reduce the ADC area. In this design an OSR of 128 is selected. Higher OSR increases the power consumption of digital circuits including the quantizer and the decimation filter. However, power dissipation of analog circuits especially the first stage integrator is approximately constant with OSR.

Modulator order *L* and the number of quantization levels *M* are interrelated. They must be chosen based on the maximum stable input range and the achievable SQNR. To achieve a thermal noise limited SNR of 86 dB (14 bits), a SQNR of approximately 100 dB is required so that in-band quantization noise is sufficiently lower than thermal noise. Table 5.1 shows the maximum SQNR values obtained from simulating $\Delta\Sigma$ modulators with various orders *L* and quantization levels *M*.

Low-order modulators with more quantization levels are stable for larger inputs compared to high-order modulators [44]. Also, as discussed in Section 3.2.2, multi-bit quantization increases the power saving of the CP integrator compared to the conventional approach. Therefore, in this thesis a second-order modulator with a 5-level quantizer is selected to achieve the desired SQNR.

Table 5.1: Achievable SQNR for different modulator topologies.

Parameter	<i>M</i> =2	<i>M</i> =3	<i>M</i> =4	<i>M</i> =5	<i>M</i> =8
L=2	-	-	99.5 dB	102.1 dB	108.1 dB
L=3	103.2 dB	114 dB	-	-	-



Figure 5.1: $\Delta\Sigma$ modulator block diagram.

5.2.2 Loop Filter

The delta-sigma toolbox [69] is used to synthesize the modulator NTF with a maximum outof-band gain of 8 dB. The input coupling coefficients of a cascaded integrators with distributed feedback (CIFB) topology to the second integrator and the quantizer are set to zero. This avoids the timing issues associated with the input feedforward coefficient to the quantizer input [70]. In this case as will be shown, the STF of the modulator has a low-pass response with a constant gain in the signal band.

Figure 5.1 shows the block diagram of the modulator. The STF and NTF of the CIFB structure are as follows:

$$STF = \frac{b_1 c_1 c_2}{z^2 + (a_2 c_2 - 2)z + (a_1 c_1 c_2 - a_2 c_2 + 1)},$$
(5.1)

$$NTF = \frac{(z-1)^2}{z^2 + (a_2c_2 - 2)z + (a_1c_1c_2 - a_2c_2 + 1)}.$$
(5.2)

Modulator coefficients are obtained from the toolbox. Next, dynamic range scaling is performed to optimize the output signal range of the integrators. Modulator coefficients are then approximated to allow implementation with a practical unit capacitor size. The modulator coefficients before and after dynamic range scaling, and the rounded coefficients used for the implementation are shown in Table 5.2.



Figure 5.2: Magnitude plots of the modulator STF before and after coefficient scaling and approximation.



Figure 5.3: Magnitude plots of the modulator NTF before and after coefficient scaling and approximation.

Coefficient	b_1	a_1	<i>c</i> ₁	a_2	<i>c</i> ₂
From Toolbox	0.66	0.66	1	1.53	1
Scaled	0.5	0.5	1.33	1.53	1
Implemented	0.5	0.5	1.4	1.6	1

Table 5.2: $\Delta\Sigma$ modulator coefficients.

The modulator transfer functions are modified as a result of coefficient approximation, however in this case, the change in the NTF and the STF is not significant. Figures 5.2 and 5.3 show the magnitude plots of the transfer functions before and after the coefficients are modified. It is noted that no high-frequency peaking is observed in the STF of the modulator with rounded coefficients. Insensitivity of the modulator to coefficient approximation also confirms its robustness to coefficient variations caused by the parasitics in the CP.

5.2.3 MATLAB Simulations

The $\Delta\Sigma$ modulator of Figure 5.1 with the rounded coefficients shown in Table 5.2 was simulated in MATLAB. Figures 5.4 and 5.5 show the time domain waveform, the PSD, and the histogram of the two integrator outputs. Figure 5.6 shows the same plots for the first integrator input, I_1 in Figure 5.1. Due to the elimination of the input feed-ins to the second stage and the quantizer inputs, the first integrator input contains a signal component. However, as a result of a high OSR the input signal component is 56 dB below the full-scale input. The highly attenuated signal component in the first integrator input minimizes the distortion caused by the loop filter. Figure 5.7 shows the 2¹⁵-point FFT output PSD of the modulator using a Hann window. For a -3-dBFS input and an OSR of 128 the achievable SQNR is 99.7 dB.



Figure 5.4: First integrator output: time-domain waveform (top), PSD (middle) and histogram (bottom).



Figure 5.5: Second integrator output: time-domain waveform (top), PSD (middle) and histogram (bottom).



Figure 5.6: First integrator input: time-domain waveform (top), PSD (middle) and histogram (bottom).



Figure 5.7: 2¹⁵-point FFT output PSD of the modulator (Window=Hann).

5.3 Circuit-Level Design

5.3.1 First Stage Integrator

Figure 5.8 shows the CP and conventional first stage integrators of the $\Delta\Sigma$ modulators. Although the figure shows single-ended circuits for simplicity, the actual implementation is fully differential. With a full-scale input range of 400 mVpp differential and a 5-level DAC, the conventional integrator OTA (Conv/3X) uses three slices of the CP integrator OTA (CP/1X) and therefore consumes three times the power. The 5-level DACs are implemented using four SC unit elements.

To reduce the OTA power consumption, DAC capacitors are shared with input sampling capacitors. Using a separate DAC capacitor with the same size as the input sampling capacitor quadruples the OTA power consumption. A 2X increase in power is caused by a two times increase in the input-referred thermal noise, and another 2X increase is due to a similar increase in the integrator closed-loop load capacitance C_L/β , which requires a doubled OTA transconductance (g_m) for a given settling accuracy.

Capacitor Sizing

In high-resolution $\Delta\Sigma$ modulators with a high OSR, the first integrator input-referred thermal noise determines its sampling capacitor size. Analytical expressions for the input-referred thermal noise power of single-ended CP and conventional SC integrators were presented in Chapter 3, which are repeated here for convenience:

$$\overline{V_{N,CP,SE}^2} = \frac{kT}{C_s.OSR} \left(1 + \frac{1}{1 + 1/3R_{on}g_m} + \frac{4N_f/3}{1 + 3R_{on}g_m}\right),\tag{5.3}$$

$$\overline{V_{N,Conv,SE}^2} = \frac{kT}{C_s.OSR} \left(1 + \frac{1}{1 + 1/2R_{on}g_m} + \frac{4N_f/3}{1 + 2R_{on}g_m}\right).$$
(5.4)



Figure 5.8: (a) CP and (b) conventional first stage integrators. (Single-ended circuits are shown for simplicity.)



Figure 5.9: Folded-cascode OTA.

In a fully-differential integrator the noise contribution of the switches is doubled [62]. Therefore,

$$\overline{V_{N,CP,FD}^2} = \frac{kT}{C_s.OSR} \left(2 + \frac{2}{1 + 1/3R_{on}g_m} + \frac{4N_f/3}{1 + 3R_{on}g_m}\right),$$
(5.5)

$$\overline{V_{N,Conv,FD}^2} = \frac{kT}{C_s.OSR} \left(2 + \frac{2}{1 + 1/2R_{on}g_m} + \frac{4N_f/3}{1 + 2R_{on}g_m}\right).$$
(5.6)

In a folded-cascode OTA, as shown in Figure 5.9, the OTA input-referred thermal noise PSD is given by

$$S_{OTA,FC}(f) = \frac{16kT}{3g_{m1,2}} \left(1 + \frac{g_{m3,4}}{g_{m1,2}} + \frac{g_{m9,10}}{g_{m1,2}}\right),\tag{5.7}$$

where the noise contribution of the cascode devices $M_5 - M_8$ is assumed to be negligible [42]. From (5.7) the noise excess factor N_f caused by current sources $M_3 - M_4$ and $M_9 - M_{10}$ is given by

$$N_f = 1 + \frac{g_{m3,4}}{g_{m1,2}} + \frac{g_{m9,10}}{g_{m1,2}}.$$
(5.8)

If the drain currents of $M_9 - M_{10}$ are assumed to be the same as the input differential pair $M_1 - M_2$, the noise factor can be expressed as

$$N_f = 1 + 2\frac{V_{ov1,2}}{V_{ov3,4}} + \frac{V_{ov1,2}}{V_{ov9,10}},$$
(5.9)

where V_{ov} represents the overdrive voltage of transistors. In this case, for $V_{ov3,4} = V_{ov9,10} = 2V_{ov1,2}$, we have $N_f = 2.5$ [62].

Although the telescopic-cascode OTA achieves a lower power consumption and inputreferred noise, the folded-cascode OTA is generally preferred over the telescopic-casecode OTA. One drawback of the telescopic-cascode OTA is the limited input common-mode range around the mid-supply voltage. The limited common-mode range makes the OTA design more sensitive to process, voltage and temperature (PVT) variations. Also, transmission gate resistance increases near the mid-supply range and that leads to distortion caused by signaldependent variations in the settling time constant. Such issues become more important as the supply voltage shrinks with technology scaling. A PMOS input folded-cascode OTA on the other hand, allows for a low input common-mode voltage and relaxes the design of switches by affording NMOS transistors a large overdrive voltage. Therefore, it is used in this implementation.

Based on Equation (5.5), sampling capacitor size for a CP integrator utilizing a foldedcascode OTA with $N_f = 2.5$ is calculated, assuming an integrator thermal noise SNR of 88 dB at -3 dBFS input. Also, $g_m R_{on} = 0.1$ is considered so that integrator noise and bandwidth are dominated by the OTA rather than switches. The required capacitor size in this case is 10.24 pF. Similarly for the conventional integrator, using Equation (5.6) with the above parameters gives the input capacitor size to be 10.4 pF. In the implemented prototype, a first stage sampling



Figure 5.10: 1X OTA slice.

capacitor of $C_{s1} = 10 pF$ is used for both modulators.

First stage OTA

The 1X OTA slice used in the first stage CP integrator is shown in Figure 5.10. The OTA used in the first stage conventional integrator (3X) uses three slices of the 1X OTA shown in parallel, hence it consumes three times the power. The three OTA slices in the conventional integrator are connected at the input, the output and the folding nodes. Linear OTA settling resulted from multi-bit quantization allows saving the OTA power consumption by reducing the current in the output devices by about 20% compared to the input differential pair. Transistor sizes of the 1X OTA are summarized in Table 5.3.

Tables 5.4 and 5.5 show the AC simulation results of the CP/1X and Conv/3X OTAs respectively, over typical, slow and fast corners. Simulations also include temperature and 10% supply variation. The OTAs are simulated with the capacitive load of their respective feedback loops during the integration phase. As can be seen, in the typical corner the DC gain of the 1X

Transistor	Туре	No. Fingers	W (µm)	L (µm)
M_0	PMOS	24	1	1
M_1, M_2	PMOS	40	1	0.15
M_{3}, M_{5}	NMOS	6	0.5	2
M_4, M_6	NMOS	5	0.5	2
M_{7}, M_{8}	NMOS	4	1	0.5
M_{9}, M_{10}	PMOS	20	1	0.5
M_{11}, M_{12}	PMOS	10	1	1

Table 5.3: First stage 1X OTA transistor sizes.

Table 5.4: Simulation results of the CP integrator 1X OTA over typical, slow and fast corners.

Process Corner	TT/1.2V/60°C	SS/1.08V/125°C	FF/1.32V/0°C
Input Transconductance ($\mu A/V$)	239.4	204.2	278.8
Open Loop DC Gain (dB)	50.8	49.7	50.4
DC Loop Gain (dB)	48.7	47.7	48.3
Open-Loop Unity-Gain BW (MHz)	16.1	13.7	18.7
Loop Unity-Gain BW (MHz)	12.7	10.8	14.7
Phase Margin (°)	88.9	88.7	89.5
Power Consumption (μW)	51.8	44.7	60.5

Table 5.5: Simulation results of the conventional integrator 3X OTA over typical, slow and fast corners.

Process Corner	TT/1.2V/60°C	SS/1.08V/125°C	FF/1.32V/0°C
Input Transconductance ($\mu A/V$)	718.2	612.6	836.4
Open Loop DC Gain (dB)	50.8	49.7	50.4
DC Loop Gain (dB)	47.1	46.1	46.8
Open-Loop Unity-Gain BW (MHz)	14.9	12.6	17.1
Loop Unity-Gain BW (MHz)	9.8	8.3	11.2
Phase Margin (°)	89.8	89.3	89.7
Power Consumption (μW)	155.3	134.0	181.5

and 3X OTAs is 50.8 dB. The loop unity-gain bandwidth of the 1X OTA in the CP integrator is 12.7 MHz, while that of the 3X OTA in the conventional integrator is 9.8 MHz. The power consumption of the 1X OTA is 51.8 μW .

Switches

Switches in the conventional and CP integrators shown in Figure 5.8 are NMOS transistors with the exception of the switches sampling $V_{refp,CP}$ in the CP integrator, which are implemented as CMOS transmission gates. The size of the switches in SC circuits is determined by the required on-resistance R_{on} to achieve a certain settling time-constant. On the other hand, the switch on-resistance depends on the voltage level that it needs to pass. In the conventional integrator assuming the common-mode (CM) voltage sampled by the switch S'_2 is the same as the OTA input CM voltage V_{cmi} (as shown in Figure 5.8(b)), the DAC CM voltage $V_{cm,DAC,Conv}$ will be the same as the input CM voltage $V_{cm,in}$:

$$V_{cm,DAC,Conv} = V_{cm,in}.$$
(5.10)

In the CP integrator, assuming the CM voltage sampled by the switches S_3 and S_4 is the same as the OTA CM V_{cmi} , the CP DAC CM voltage $V_{cm,DAC,CP}$ will be given by

$$V_{cm,DAC,CP} = 2V_{cm,in} - V_{cmi}.$$
 (5.11)

Given that in the implemented prototype $V_{cm,in} = 0.4V$ and $V_{cmi} = 0.2V$, the DAC CM voltages in the CP and conventional integrators are as follows:

$$V_{cm,DAC,Conv} = 0.4V$$
 , $V_{cm,DAC,CP} = 0.6V.$ (5.12)

Switch	Туре	$W_N/W_P (\mu m)$	L (µm)
S_1	NMOS	2 / -	0.12
S_2	NMOS	2 / -	0.12
S_3	NMOS	2 / -	0.12
S_4	NMOS	8 / -	0.12
S_5	NMOS	4 / -	0.12
S_6	NMOS	6/-	0.12
S_7	T-Gate	4 / 16	0.12
S_8	NMOS	6/-	0.12

Table 5.6: Switch sizes in the first stage CP integrator.

Table 5.7: Switch sizes in the first stage conventional integrator.

Switch	Туре	$W_N (\mu m)$	L (µm)
S'_1	NMOS	4	0.12
S'_2	NMOS	8	0.12
S'_3	NMOS	8	0.12
S'_4	NMOS	6	0.12
S'_5	NMOS	2	0.12

Hence, the reference voltages shown in Figure 5.8 are given by

$$V_{refp,CP} = 0.8V$$
 , $V_{refn,CP} = 0.4V$, (5.13)

$$V_{refp,Conv} = 0.5V$$
 , $V_{refn,Conv} = 0.3V.$ (5.14)

From (5.13) a PMOS switch can be used to sample the reference voltage $V_{refp,CP}$. However, a transmission gate was used to allow flexibility in setting the CP DAC CM voltage during testing. Tables 5.6 and 5.7 summarize the switch sizes in the CP and conventional integrators, respectively. It is also noted that bottom-plate sampling with advanced clocks Φ_{1a} and Φ_{2a} is used in both integrators to minimize the signal-dependent charge-injection.



Figure 5.11: Implementation of chopper-stabilization for the first stage OTAs.

Table 5.8: Chopper switch sizes.

Switch	Туре	W_N/W_P (µm)	L (µm)
S _{CHin}	NMOS	2 / -	0.12
S _{CHout}	T-Gate	8/32	0.12

Chopper-Stabilization

Chopper-stabilization is used in the conventional and CP first stages to suppress the OTA offset and 1/f noise, as shown in Figure 5.11. Chopping is performed at half the sampling-rate, with the input chopping clocks being advanced compared to the output chopping clocks [71]. Input chopping switches are implemented as NMOS switches due to a low OTA input common-mode voltage of $V_{cmi} = 0.2V$. However, CMOS transmission gates are used for the output chopping switches to accommodate the OTA output voltage swings. Table 5.8 shows the switch sizes of the chopping circuit. It is important to maintain the symmetry of the layout of the chopping circuit as much as possible. This is simply because any asymmetry in the layout leads to residual input-referred offset. Also, the chopping network is properly shielded (especially at the OTA inputs) to avoid coupling of unwanted signals to the sensitive nodes.



Figure 5.12: Second stage integrators of the CP and conventional ADCs.

5.3.2 Second Stage Integrator

A single-ended version of the second stage integrator is shown in Figure 5.12. The required sampling capacitor size in the second stage is determined by its input-referred thermal noise. In the $\Delta\Sigma$ modulator shown in Figure 5.1 with a high OSR, the ratio of the required sampling capacitor in the second stage over the first stage sampling capacitor size is approximately given by

$$\frac{C_{s2}}{C_{s1}} \approx \frac{V_{N1,in}^2}{V_{N2,in}^2} (\frac{1}{k_1})^2 \frac{\pi^2}{3OSR^2},\tag{5.15}$$

where k_1 is the first integrator coefficient ($k_1 = a_1 = b_1$ in Figure 5.1), and $\overline{V_{N1,in}^2}$ and $\overline{V_{N2,in}^2}$ are the input-referred noise powers of the first and second stages, respectively. Assuming $\overline{V_{N1,in}^2}/\overline{V_{N2,in}^2} = 10$ so that thermal noise from the second stage is negligible compared to the first stage, the required sampling capacitor in the second stage is $C_{s2} = 80 fF$. However, due to a minimum unit capacitor size of $C_u = 60 fF$ available in the 0.13 μ m CMOS process, and to implement the feedback DAC coefficient $a_2 = 8/5$, the second stage DAC capacitor is

		e		
Transistor	Туре	No. Fingers	W (µm)	L (µm)
M_0	PMOS	7	1	1
M_1, M_2	PMOS	12	1	0.15
M_3, M_5	NMOS	2	0.5	2
M_4, M_6	NMOS	1	0.5	2
M_7, M_8	NMOS	1	1	0.5
M_{9}, M_{10}	PMOS	6	1	0.5
M_{11}, M_{12}	PMOS	3	1	1

Table 5.9: Second stage OTA transistor sizes.

Table 5.10: Simulation results of the second stage OTA over typical, slow and fast corners.

Process Corner	TT/1.2V/60°C	SS/1.08V/125°C	FF/1.32V/0°C
Input Transconductance $(\mu A/V)$	71.1	61.1	81.9
Open Loop DC Gain (dB)	50.0	49.2	49.5
DC Loop Gain (dB)	41.4	40.6	40.8
Open-Loop Unity-Gain BW (MHz)	12.7	10.9	14.5
Loop Unity-Gain BW (MHz)	4.7	4.0	5.4
Phase Margin (°)	90.1	90.0	90.4
Power Consumption (μW)	15.5	13.5	17.9

realized with 8 unit capacitors. Also, to save the OTA power consumption the DAC capacitor is shared with the input capacitor, therefore the second stage sampling capacitor size becomes $C_{s2} = 8C_u = 480 fF$. Since the input coefficient $c_1 = 7a_2/8$, one of 8 unit capacitors of the DAC samples the CM voltage instead of the first stage output, as illustrated in Figure 5.12. With 8 unit DAC capacitors each thermometer-code bit of the 5-level ADC is used to control two unit capacitors.

The OTA in the second stage of the $\Delta\Sigma$ ADCs is based on a PMOS input folded-cascode architecture similar to the one shown in Figure 5.10. Table 5.9 shows the transistor sizes of the second stage OTA. Simulation results of the OTA are summarized in Table 5.10.



Figure 5.13: Dynamic comparator used in the 5-level quantizer.

5.3.3 Quantizer

The 5-level quantizer is implemented as a flash ADC consisting of four dynamic comparators. Figure 5.13 shows the circuit diagram of the comparator [72]. It consists of a dynamic regenerative latch preceded by switched capacitors that are precharged to the input and quantizer reference voltages during the reset phase Φ_1 . A SR-latch follows the comparator to hold its outputs during Φ_1 . To reduce the OTA power consumption in the second stage, the unit capacitor size to implement C_{in} and C_{ref} is reduced by connecting two minimum size MIM capacitors (60fF each) in series. This helps to reduce the OTA load capacitance from the quantizer during the integration phase. The comparator threshold voltage is set by the capacitor ratio C_{ref}/C_{in} . In the implemented prototype, $C_{in} = 120fF$ and $C_{ref} = 30fF$, 90*fF* depending on the required threshold of comparison. The comparators worst-case offset standard deviation is approximately 6.2 mV, obtained from 200 Monte-Carlo simulations.

Transistor	Туре	No. Fingers	W (µm)	L (µm)
M_0	NMOS	2	1	0.15
M_1, M_2	NMOS	16	1	0.3
M_3, M_4	NMOS	1	1	1
M_5, M_6	PMOS	2	1	0.15
M_7, M_8	PMOS	4	1	1

Table 5.11: Latch transistor sizes.



Figure 5.14: Switched-capacitor CMFB circuit.

5.3.4 Other Circuits

Common-mode Feedback

In SC circuits, SC CMFB is typically preferred over CT CMFB. This is because it does not limit the output voltage swing, and does not dissipate static power. In this work, a SC CMFB circuit is used for the first and second integrator OTAs. The SC CMFB circuit implements a SC low-pass filter on the desired common-mode and bias voltages $V_{cmo,ref}$ and $V_{b,ref}$ as shown in Figure 5.14. During Φ_2 , $V_{cmo,ref}$ and $V_{b,ref}$ are sampled onto the capacitor C_1 . In Φ_1 , C_1 and C_2 are connected in parallel. The CMFB control voltage V_{cmfb} is generated by the average of the OTA output voltages V_{op} and V_{on} .

Clock Generator

A simplified circuit diagram of the non-overlapping clock generator is shown in Figure 5.15. In the actual implementation, the inverters adjusting the delays and the non-overlap time are repeated an odd number of times. The regular non-overlapping clocks Φ_1 , Φ_2 and the chopping



Figure 5.15: Two-phase non-overlapping clock generator.



Figure 5.16: Inverter chain used to buffer the clock signals (1X inverter size is $W_N = 1 \mu m$, $W_P = 4 \mu m$ and $L = 0.12 \mu m$.

clocks Φ_{CHA} , Φ_{CHB} are generated using two clock generators. The frequency of the input clock to the chopping clock generator is divided by two using a D-flip-flop in feedback. The advanced clocks Φ_{1a} , Φ_{2a} are generated to enable bottom-plate sampling. Similarly the input chopping clocks Φ_{CHAa} , Φ_{CHBa} are advanced compared to the output chopping clocks Φ_{CHA} , Φ_{CHB} . In the clock generator circuit shown in Figure 5.15, the rising edge of the advanced clocks is aligned with the rising edge of the regular clocks, and only the falling edge is early. In high speed applications where clock delays are not negligible compared to the length of the integration phase, this helps to maximize the OTA settling time and therefore save on power consumption. The clock signals are buffered using a chain of inverters, as shown in Figure 5.16. This ensures fast rise and fall times for the clocks and saves digital power consumption.

The clock waveforms resulted from extracted-RC simulations of the CP modulator at the SS corner are shown in Figure 5.17. The non-overlap time measured at the 10% of the supply voltage is 2.49 ns. Also, the delay between the falling edge of the advanced clock Φ_{1a} and Φ_1 is 1.4 ns.



Figure 5.17: Buffered clock waveforms resulted from extracted-RC simulations at the SS corner.

Data-weighted Averaging

In multi-bit $\Delta\Sigma$ modulators, mismatch error of the DAC elements results in nonlinearity in the modulator output. One approach to reduce the effect of DAC mismatch is to suppress the error in the signal band and move its spectral content to out-of-band frequencies (error shaping). The technique used in this thesis is based on element rotation and is commonly referred to as data-weighted averaging (DWA) [73]. DWA is used to linearize the DACs feeding both the first and the second stage integrators.

Figure 5.18 shows a block diagram of the DWA circuit. The thermometer code from the flash ADC is sent to a shifting block and a pointer update logic. The pointer update logic converts the input thermometer code to binary format and adds it with the current value of the pointer register. The shifting block consists of two cells to shift the thermometer code by one and two positions. The shifting cells are based on simple transmission gates, and are controlled by the individual bits of the pointer register.



Figure 5.18: Block diagram of the DWA circuit.

Analog Multiplexer

In order to have design observability while testing the two ADCs, an analog multiplexer is used as shown in Figure 5.19. A total of 24 nodes (12 nodes per ADC) are probed using the analog multiplexer. A four-bit decoder is used to select the test nodes to be probed and connect them to the differential outputs of the multiplexer. As shown in Figure 5.19, the multiplexer passes the selected node voltage to the output through two transmission gates (S_1 and S_2). When unselected, the corresponding path is pulled low by an NMOS switch (S_3) to avoid any coupling to the long route between the transmission gates. For the two $\Delta\Sigma$ modulators, the first and second integrator outputs, the OTA bias voltages, power supply and ground can be probed. Test nodes are directly connected to the pads with no additional buffering. Therefore, the integrator output voltages cannot be probed when the ADC is operating at nominal speed.

5.3.5 $\Delta\Sigma$ Modulators Extracted Simulations

Figures 5.20 and 5.21 show the output PSDs of the CP and conventional ADCs resulted from extracted simulations. For the simulations 2¹⁴ samples were taken to calculate the FFT, which corresponds to 64 in-band bins. The amplitude of the input signal was set to 320 mV peak-to-peak differential (80% of a 400 mV differential reference). Chopping and DWA circuits were enabled in the simulations. The SNDR of the CP and conventional modulators are 92.9 dB and 92.1 dB, respectively.



Figure 5.19: Analog Multiplexer.



Figure 5.20: Simulated 2¹⁴-point PSD of the CP modulator for a 320 mVpp differential signal and a 2.5 MHz clock (Window=hann).



Figure 5.21: Simulated 2¹⁴-point PSD of the conventional modulator for a 320 mVpp differential signal and a 2.5 MHz clock (Window=hann).

5.4 Summary

In this chapter, the design of a prototype chip consisting of two $\Delta\Sigma$ ADCs was presented. The first ADC makes use of a CP integrator in the first stage, while the second ADC employs a conventional integrator at the front-end. System-level simulations show that a second order modulator with a 5-level quantizer can achieve the required SQNR. Circuit-level design of the two ADCs was discussed. The first stage OTA in the CP ADC is three times smaller than the first stage OTA in the conventional ADC. In the two ADCs chopping is used in the first stage to reduce the OTA offset and 1/f noise, and DWA is used to linearize the feedback DACs. Simulation results of the first stage integrators show that the CP integrator achieves a higher loop unity-gain bandwidth, and therefore faster settling speed compared to the conventional integrator. Also, extracted simulations at 2.5 MHz sampling-rate indicate that the CP based modulator achieves similar SNDR performance compared to the conventional ADC, while consuming three times lower OTA power in the first stage.

Chapter 6

Experimental Results

In this chapter measurement results of the fabricated test chip are presented. Section 6.1 discusses the test chip. Test setup and measured results are described in Sections 6.2 and 6.3, respectively.

6.1 Test Chip

The chip is fabricated in a 1.2 V 0.13 μ m CMOS process. The fabrication process includes 8 metal layers and high density MIM and dual MIM capacitors. Dual MIM capacitors are used for on-chip decoupling of bias voltages, references and supply voltages. For each ADC multiple supply voltages are used to allow measurement of power consumption for different ADC sub-blocks. Analog power and ground lines are separated from digital to minimize noise coupling from digital circuits to analog blocks. The die micrograph of the test chip is shown in Figure 6.1, where the core area is 3.46 mm². The chip is packaged in an 80-pin Ceramic Quad Flat Pack (CQFP) package.



Figure 6.1: Die micrograph of the fabricated prototype in 0.13 μ m CMOS.



Figure 6.2: Custom 4-layer PCB photo.



Figure 6.3: $\Delta\Sigma$ modulators test setup.

6.2 PCB and Test Setup

A custom 4-layer printed circuit board (PCB) was designed to test the ADC prototypes. A photo of the PCB is shown in Figure 6.2. The PCB top layer is used for routing and placement of various components. The inner layers of the PCB are used for power and ground planes, and the bottom layer is used for routing and placement of surface mount decoupling capacitors. It is noted that a single ground plane is used for the entire PCB. However, to reduce crosstalk and interference between analog and digital circuits, separate analog and digital sections are used for component placement and routing [74]. In this case, analog/digital traces are routed in their respective sections only, without entering the other section.

Figure 6.3 shows the $\Delta\Sigma$ modulators' test setup. The input signal to the ADCs was generated from a low noise and distortion DS360 signal generator. The Texas Instruments THS4520 evaluation module (EVM) was used to convert a single-ended output of the signal source to a fully-differential signal. The outputs of the evaluation module were passed through Mini-Circuits low-pass filters before entering the chip.

Precision references were generated using the low noise ADR440/430 voltage references. To produce the appropriate voltage levels, the reference outputs were reduced using resistive dividers and buffered using the OPA350 opamps in unity feedback. This arrangement was

	Meas./CP (mV)	Meas./Conv (mV)	Sim./TT,27°C (mV)	Sim./SS,27°C (mV)
V_{bp}	795	790	814	787
V_{cp}	644	649	671	629
V_{cn}	574	565	552	615
V_{bn}	397	403	366	410
V_{bss}	793	796	814	783
V_{cmfb1}	336	338	311	353
V_{cmfb2}	363	382	350	394

Table 6.1: Measured vs. simulated biasing of the OTAs in the CP and conventional ADCs.

used to generate the CP DAC, the conventional DAC, and the quantizer references in addition to the modulators' CM voltages. During testing it was observed that reducing the differential reference of the quantizer improved the distortion performance.

Various power supplies on the PCB were generated using the low-noise TPS717 linear voltage regulators. The generated supply voltages on the board were 1.2 V and 3.3 V. The ADCs adjustable bias currents were generated using voltage references and potentiometers in series with resistors. An on-board crystal oscillator was used to generate the PCB reference clock. Alternatively, the clock signal could be produced using a SMT03 Rohde & Schwarz signal source. Since the signal source clock has the advantage of programmability compared to the on-board oscillator, it was used for measurements requiring a clock frequency sweep. Digital control inputs such as chopping and DWA enable were generated on the PCB using dual in-line package (DIP) switches. Digital outputs of the ADCs were captured by the National Instruments NI-6534 PCI card and post-processed in MATLAB.

6.3 Measurement Results

6.3.1 OTA Bias Voltages

In order to ensure proper biasing of the OTAs within the $\Delta\Sigma$ modulators, their bias voltages were measured. Table 6.1 shows the measured biases of the OTAs in the CP and conventional ADCs, and compares them with the simulated values over the typical and slow corners. From
the Table it can be seen that the measured bias voltages are between the typical and slow values.

6.3.2 SNDR/SNR

The measured 2²⁰-point FFT output spectra of the CP and conventional ADCs are shown in Figure 6.4. The input signal is a -1 dBFS 390 Hz sinusoid and the clock frequency is 2.56 MHz. The ADC outputs are windowed using a Blackman-Harris window before applying the FFT, and the resulting NBW of the spectra is 4.89 Hz.

The SNDR variation of the ADCs with sampling-rate for a fixed input bandwidth of 10 kHz is shown in Figure 6.5. At sampling-rates up to about 1 MHz the SNDR of both modulators is quantization noise limited. From about 2.5 MHz to 3 MHz thermal noise dominates the performance. Beyond 3.5 MHz, the SNDR of both ADCs drops almost at the same rate due to insufficient settling of the OTAs. For comparison, the SNDR of the conventional ADC when its OTAs' bias current is reduced by 66% is also shown on the same plot (Conv/1X). The conventional ADC performance drops significantly at 2.5 MHz, when its first stage consumes the same power as the CP ADC first stage. It is noted that in this case the second stage OTA current is also scaled down with the ADC bias current scaling, however the SNDR drop can mostly be attributed to settling errors in the first stage, which are not noise shaped. Figure 6.6 shows the SNDR variation versus sampling-rate for a fixed OSR of 128. In this case, the SNDR is limited by thermal noise at lower frequencies. At higher clock rates the SNDR drop follows a nearly similar trend as the fixed input bandwidth case.

Figure 6.7 shows the measured SNDR/SNR of the two modulators versus input signal level for a 2.56 MHz clock. The CP ADC achieves 87.8 dB SNDR, 89.2 dB SNR and 90 dB DR over a 10 kHz signal bandwidth while dissipating 148 μ W. The conventional ADC has similar SNDR, SNR and DR performance but dissipates 241 μ W. The key measurement results of the two ADCs are summarized in Table 6.2.



Figure 6.4: Measured 2²⁰-point PSDs of (a) the CP and (b) conventional ADC outputs for a -1 dBFS, 390 Hz input sinusoid and 2.56 MHz clock (Window=Blackman-Harris).



Figure 6.5: Measured SNDR variation of the CP and conventional modulators versus samplingrate (F_s) for a fixed input bandwidth of 10 kHz.



Figure 6.6: Measured SNDR variation of the CP and conventional modulators versus samplingrate (F_s) for a fixed OSR of 128.



Figure 6.7: Measured SNR and SNDR versus input signal level for the CP and conventional $\Delta\Sigma$ modulators.

Based on a FOM of

$$FOM = \frac{Power}{2 \cdot BW \cdot 2^{(SNDR(dB) - 1.76)/6.02}}$$
(6.1)

the CP ADC achieves 369 fJ/conversion-step, which is almost 40% lower than the conventional ADC FOM. This overall improvement in the FOM is accomplished through the use of the front-end CP integrator that consumes 66% lower OTA power compared to the conventional integrator.

6.3.3 Effect of Chopper-Stabilization

Figures 6.8 and 6.9 show the output spectra of the CP and conventional ADCs with and without chopping. As can be seen, when chopping is disabled the low-frequency noise floor increases in both modulators. In this case, the SNDR drops to approximately 81 dB, which is about 6.5 dB lower than the SNDR achieved when chopping is enabled.

	-	
ADC	Conventional	СР
Technology	0.13 μm	0.13 µm
Supply Voltage	1.2 V	1.2 V
Input Range (diff.)	0.4 Vpp	0.4 Vpp
Sampling Rate	2.56 MHz	2.56 MHz
Signal Bandwidth	10 kHz	10 kHz
Oversampling Ratio	128	128
Peak SNDR	87.7 dB	87.8 dB
Peak SNR	89.3 dB	89.2 dB
Dynamic Range	90 dB	90 dB
Total Power	241 µW	$148 \ \mu W$
FOM	607 fJ/conv-step	369 fJ/conv-step

Table 6.2: Performance summary of the CP versus conventional ADCs.



Figure 6.8: Measured 2²⁰-point PSD of the CP modulator with and without first stage OTA chopping for a -1 dBFS input and 2.56 MHz clock (Window=Blackman-Harris).



Figure 6.9: Measured 2²⁰-point PSD of the conventional modulator with and without first stage OTA chopping for a -1 dBFS input and 2.56 MHz clock (Window=Blackman-Harris).

Table 6.3: Measured power consumption breakdown of the CP and conventional ADC	Cs.
--	-----

ADC Power	Conventional (μW)	$CP(\mu W)$
Integrator 1	156.6	52.1
Integrator 2	22	21.7
5-level ADC	4	4
Biasing	10.6	10.6
Digital	47.8	59.6

6.3.4 Effect of DWA

The effectiveness of DWA in the CP and conventional ADCs is demonstrated in Figures 6.10 and 6.11, respectively. When DWA is disabled, the second order harmonic level rises in the ADC outputs. As a result, the SNDR drops to approximately 83 dB.

6.3.5 Power Consumption Breakdown

Table 6.3 shows the power consumption breakdown of the two modulators. The CP ADC consumes extra digital power in the clock buffers used to drive the PMOS switches in the CP integrator. However, this is not fundamental to the approach and could be avoided by selecting a lower common-mode for the CP DAC reference voltages.



Figure 6.10: Measured 2²⁰-point PSD of the CP modulator with and without DWA for a -1 dBFS input at $F_s = 2.56$ MHz (Window=Blackman-Harris).



Figure 6.11: Measured 2^{20} -point PSD of the conventional modulator with and without DWA for a -1 dBFS input at $F_s = 2.56$ MHz (Window=Blackman-Harris).

	Tech./Supply	Input Range	OSR	BW	SNDR	Power	FOM-dB
	[µm]/[V]	$[\mathbf{V}_{pp-diff}]$		[kHz]	[dB]	[µW]	[dB]
[21]	0.13/ 0.9	1.1	128	24	89	1500	161.0
[34]	0.18/ 0.9	1.0	256	10	80.1	200	157.1
[41]	0.18/ 0.7	1.0	100	20	81	36	168.4
[75]	0.18/ 1.0	0.5	100	20	84	660	158.8
[CP ADC]	0.13/ 1.2	0.4	128	10	87.8	148	166.1

Table 6.4: Comparison with other SC $\Delta\Sigma$ modulators with an input range ≤ 1.1 Vpp differential and OSR>100.

6.3.6 Comparison With the State-of-the-art

Table 6.4 compares the performance of the CP ADC with the state-of-the-art SC $\Delta\Sigma$ ADCs having an input signal range ≤ 1.1 Vpp differential and OSR ≥ 100 . Here, FOM-dB is defined as

$$FOM - dB = SNDR(dB) + 10log_{10}(\frac{BW}{Power}).$$
(6.2)

From the Table, [41] achieves a low power consumption of 36 μW for an input signal range of 1 Vpp differential. However, it makes use of pseudo-differential inverters instead of fullydifferential OTAs, and has a lower SNDR. Even though the CP ADC of this work digitizes a relatively small input signal, it achieves higher power efficiency compared to other OTA-based ADCs.

6.4 System Level Power Analysis

In this section, a first order power analysis for two implementations of a SC system with a high OSR is presented. In the first implementation as shown in Figure 6.12(a), a SC gain stage is placed in front of a conventional $\Delta\Sigma$ modulator ADC. The closed-loop gain of the SC amplifier is assumed to be G V/V. In the second approach, shown in Figure 6.12(b), a CP based $\Delta\Sigma$ modulator is used to digitize the input signal without amplification.



Figure 6.12: Two implementations of a SC system (a) conventional approach (b) CP based approach.

In the analysis only the analog power consumption of thermal noise limited front-end circuits is taken into account. As indicated by dashed outlines these circuits include the SC gain stage and the first integrator of the conventional ADC in Figure 6.12(a), and the first integrator of the CP based ADC in Figure 6.12(b). It is assumed that OTA settling is linear, and the analog power consumption is proportional to the sampling capacitance of SC circuits. The latter is the case when the load capacitance seen by the OTA is dominated by the feedback network of the current stage rather than the load capacitance from the next stage.

In the conventional approach C_s is the front-end gain stage sampling capacitor size, and G^{-x} is the scaling factor of the first stage sampling capacitor in the $\Delta\Sigma$ ADC, where $1 \le x \le 1.5$ [66]. In this case, the power consumption of the front-end circuits is given by

$$P_{Conv} = K_p C_s (1 + G^{-x}), \tag{6.3}$$

while the total input-referred thermal noise is

$$N_{Conv} = \frac{K_n}{C_s} (1 + G^{x-2}).$$
(6.4)

 K_p and K_n in (6.3) and (6.4) are constants of proportionality for power and noise, respectively.

For the CP based implementation

$$P_{CP} = \frac{K_p C_s}{3},\tag{6.5}$$

where C_s is the sampling capacitor of the first integrator of the CP ADC, and the factor of three saving in power is based on the experimental results of this work. The total input-referred thermal noise is given by

$$N_{CP} = \frac{K_n}{C_s}.$$
(6.6)

The product of power and noise *PN* quantifies the system analog power efficiency, where a lower figure indicates higher power efficiency. In this case, for the two implementations above

$$P_{Conv}N_{Conv} = K_p K_n (1 + G^{-x})(1 + G^{x-2}),$$
(6.7)

and

$$P_{CP}N_{CP} = \frac{K_p K_n}{3}.$$
(6.8)

Table 6.5 compares the two systems analog power efficiencies for different combinations of *G* and *x*. From the Table, the CP based approach achieves \geq 6.1 dB higher analog power efficiency compared to the conventional approach.

Table 6.5: Comparison of thermal noise limited analog power efficiency for the systems shown in Figure 6.12.

G(V/V)	x	$P_{Conv}N_{Conv}/P_{CP}N_{CP}(dB)$
2	1.2	8.3
4	1.3	6.8
8	1.4	6.1

6.5 Summary

Experimental results of the fabricated chip show that the CP ADC achieves similar performance as the conventional ADC, while saving 66% of the OTA power in the front-end integrator. The CP ADC FOM is 369 fJ/conversion-step, which is almost 40% lower than that of the conventional ADC. Measurement results indicate the effectiveness of chopping and DWA circuits in both the CP and conventional modulators. A system-level analysis comparing the analog power efficiency of a CP based SC system with a conventional SC system shows greater than 6 dB higher power efficiency for the CP based approach.

Chapter 7

Conclusions

7.1 Thesis Contributions

In this thesis, charge-pump (CP) based SC circuits were proposed. It was shown that employing capacitive charge-pumps at the front-end of SC circuits can considerably reduce the stage power consumption, while maintaining the same thermal noise performance. The approach was demonstrated in SC integrators as well as gain stages. The CP based SC integrator was shown to achieve a significantly improved linearity-speed trade-off compared to the conventional SC integrator [55]. The CP based amplifier was also shown to enhance the gain-speed trade-off of the conventional SC amplifier [65]. Practical considerations in design of CP based circuits, such as the effect of CP parasitics [61], capacitor mismatch, OTA finite gain and offset were discussed.

A prototype chip was implemented in a 0.13 μ m CMOS technology [68]. The chip consists of two $\Delta\Sigma$ modulators. The first ADC employs a CP integrator at the front-end, while the second ADC is based on a conventional first stage integrator. Circuits beyond the first stage are identical between the two ADCs. This facilitates a direct comparison between the CP based approach and the conventional approach. Experimental results demonstrate that the CP ADC achieves 87.8 dB SNDR, 89.2 dB SNR and 90 dB DR over a 10 kHz BW, while consuming 148 μ W. Compared to the conventional ADC, the CP based modulator achieves the same performance while saving 66% of the dominant front-end OTA power.

7.2 Future Research

The following topics related to the work presented in this thesis are worth further investigation.

7.2.1 CP SC Circuits with N > 2 Sampling Capacitors

As discussed in Chapter 3, CP based SC circuits can be implemented using N > 2 sampling capacitors. This is specially useful when processing small input signals in the order of tens of millivolts, where OTA settling is linear. In this case, the power savings of this approach can ideally increase to a factor of N^2 . It would be interesting to verify whether in practice power savings of 10X or more can be achieved using the CP based technique.

7.2.2 CP Gain Stage

A silicon implementation of the CP gain stage proposed in Chapter 4 is also of great interest. The CP gain circuit can be designed as a stand alone amplifier to verify its applicability at the front-end of SC systems with small inputs. Alternatively, the CP based gain amplifier can be used as a multi-bit MDAC in a pipelined ADC. However, in pipelined ADCs an accurate gain for the MDAC circuit is needed. Therefore, the gain error introduced by the CP parasitics may require a form of background or foreground calibration.

7.2.3 Comparator-based CP SC Circuits

The CP SC circuits can also be implemented using comparator-based circuits. The idea is shown in Figure 7.1 for a CBSC integrator. In this case the comparator-based CP integrator also achieves significant power savings compared to the conventional CBSC integrator in both



Figure 7.1: Comparator-based CP integrator.

the charge/ discharge current and the comparator.

In a comparator-based CP integrator, reduction in the effective load capacitance C_L seen by the current source compared to the conventional circuit directly affects the required charge/ discharge current. This is because for a fixed output voltage change (ΔV) caused by a constant current *I* charging a capacitive load C_L in a fixed amount of time ($\Delta t \simeq 1/2f_s$), the required charge/ discharge current is proportional to the load capacitance C_L . Therefore, the ratio of the required current in a comparator-based CP integrator over a comparator-based conventional integrator, both with coefficients of *k*, is as follows:

$$\frac{I_{CP}}{I_{Conv}} = \frac{k+1}{2(k+2)},$$
(7.1)

which varies between 1/4 and 1/2 depending on k. Moreover in this case, similar to the OTA-based CP integrator, implementing a gain of two for the input signal appears to relax the thermal noise requirements of the comparator, therefore it can be designed with a lower power (g_m) and higher input-referred thermal noise. This further reduces the power consumption of the comparator-based CP integrator compared to the conventional CBSC integrator.

7.2.4 CP Integrator in a MASH $\Delta\Sigma$

In this thesis, the CP integrator was employed in a single-stage $\Delta\Sigma$ modulator. It would be interesting to verify its application in cascaded $\Delta\Sigma$ ADCs. To achieve a high SQNR, MASH $\Delta\Sigma$ ADCs typically rely on precise matching between the analog and digital transfer functions. Therefore, their performance is sensitive to analog imperfections such as the parasitics in the CP. In a MASH $\Delta\Sigma$, coefficient variations due to the CP parasitics can cause the quantization noise to leak into the output and lower the SQNR. In this case, a method for digital calibration of the errors caused by quantization noise leakage may be required.

7.2.5 Combination with Other Low-Power Techniques

The CP based approach can also be combined with other low-power techniques such as doublesampling and/or inverter-based designs. Double sampling halves the SC clock frequency, and can further relax the CP OTA bandwidth requirement. An inverter-based CP integrator can save additional power by using low-power and low-noise inverters as amplifiers.

Appendix A

SR-Limited Settling in the CP vs Conventional SC Circuits

In the charge transfer phase of a SC circuit, the OTA response typically involves a slewing period followed by a linear settling period. As shown in Figure A.1, the OTA initial output voltage before applying the step at t = 0 is assumed to be 0 V. In this case, the partial SR-limited response of the OTA can be expressed as:

$$v_{o,SR}(t) = [(1 - K_Z)V_{o,step} + SR.t] \quad , \quad 0 \le t \le T_{SR}$$
(A.1)

$$v_{o,linear}(t) = [(1 - K_Z)V_{o,step} + SR.T_{SR}] , \quad T_{SR} \le t \le T_{CT}$$

+ $[V_{o,step} - (1 - K_Z)V_{o,step} - SR.T_{SR}][1 - e^{(-(t - T_{SR})/\tau)}].$ (A.2)

Based on the condition of continuity of derivatives of the output voltage in (A.1) and (A.2) the OTA slewing period T_{SR} is found to be:

$$T_{SR} = \frac{K_z |V_{o,step}|}{SR} - \tau. \tag{A.3}$$



Figure A.1: OTA settling behavior during the charge transfer phase.

The OTA SR in the conventional and CP circuits is determined by a current I_{SR} :

$$SR_{Conv} = \frac{I_{SR,Conv}}{C_{L,Conv}},\tag{A.4}$$

$$SR_{CP} = \frac{I_{SR,CP}}{C_{L,CP}}.$$
(A.5)

The OTA transconductance and bandwidth are determined by a current I_{gm} :

$$g_{m,Conv} = \frac{I_{gm,Conv}}{V_{ov}},\tag{A.6}$$

$$g_{m,CP} = \frac{I_{gm,CP}}{V_{ov}}.$$
(A.7)

In addition, the OTA settling time-constant in the conventional and CP circuits is given by

$$\tau_{Conv} = \frac{C_{L,Conv}}{\beta_{Conv}g_{m,Conv}},\tag{A.8}$$

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$$\tau_{CP} = \frac{C_{L,CP}}{\beta_{CP}g_{m,CP}},\tag{A.9}$$

From (A.3), the ratio of slewing periods in the CP and conventional circuits is

$$\frac{T_{SR,CP}}{T_{SR,Conv}} = \frac{K_{z,CP}|V_{o,step}|/SR_{CP} - \tau_{CP}}{K_{z,Conv}|V_{o,step}|/SR_{Conv} - \tau_{Conv}}$$
(A.10)

Assuming that in both OTAs the SR current I_{SR} is proportional to the linear current I_{gm} :

$$I_{SR} = mI_{gm}, \tag{A.11}$$

and substituting for SR, τ and g_m from equations (A.4)-(A.9) gives

$$\frac{T_{SR,CP}}{T_{SR,Conv}} = \frac{I_{SR,Conv}/C_{L,Conv}}{I_{SR,CP}/C_{L,CP}} \frac{K_{z,CP}|V_{o,step}| - mI_{gm,CP}/(\beta_{CP}g_{m,CP})}{K_{z,Conv}|V_{o,step}| - mI_{gm,Conv}/(\beta_{Conv}g_{m,Conv})}$$
(A.12)

where I_{gm}/g_m is the overdrive voltage of the transistor V_{ov} . Also, from equations (3.14)-(3.16), K_z can be expressed as

$$K_{z,Conv} = 1 + \frac{1}{k},\tag{A.13}$$

$$K_{z,CP} = 1 + \frac{2}{k}.$$
 (A.14)

In this case, (A.12) is simplified as follows

$$\frac{T_{SR,CP}}{T_{SR,Conv}} = \frac{1}{2} \frac{I_{SR,Conv}}{I_{SR,CP}} \frac{|V_{o,step}/k| - mV_{ov}/2}{|V_{o,step}/k| - mV_{ov}}.$$
(A.15)

If the OTA SR and linear currents are the same ($I_{SR} = I_{gm} = I_{SS}$), equation (A.15) can be written as:

$$\frac{T_{SR,CP}}{T_{SR,Conv}} = \frac{1}{2} \frac{I_{SS,Conv}}{I_{SS,CP}} \frac{|V_{o,step}/k| - V_{ov}/2}{|V_{o,step}/k| - V_{ov}}.$$
(A.16)

Bibliography

- L. Doherty, B. A. Warneke, B. E. Boser, and K. S. J. Pister, "Energy and performance considerations for smart dust," *Int. J. of Parallel and Distributed Systems and Networks*, vol. 4, no. 3, pp. 121–133, Mar. 2001.
- [2] A. P. Chandrakasan, N. Verma, and D. C. Daly, "Ultra low-power electronics for biomedical applications," *Annu Rev. Biomed. Eng.*, vol. 10, pp. 247–274, 2008.
- [3] ADXL001: High performance wide bandwidth iMEMS accelerometer, Datasheet [Online]: http://www.analog.com/en/mems-sensors/mems-inertialsensors/adx1001/products/product.html.
- [4] B. E. Boser, "Electronics for micromachined inertial sensors," in *Proc. IEEE Transducers*'97, pp. 1169–1172.
- [5] C. Zhang, Q. song Wu, T. Yin, and H. gang Yang, "A MEMS gyroscope readout circuit with temperature compensation," in *IEEE Intl. Conf. on Nano/Micro Engineered and Molecular Systems*, Jan. 2010, pp. 458–462.
- [6] O. Bajdechi and J. Huijsing, "A 1.8-V ΔΣ modulator interface for an electret microphone with on-chip reference," *Solid-State Circuits, IEEE Journal of*, vol. 37, no. 3, pp. 279– 285, Mar. 2002.
- [7] H.-B. Le, S.-G. Lee, and S.-T. Ryu, "A regulator-free 84dB DR audio-band ADC for compact digital microphones," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2010.
- [8] A.-J. Annema, B. Nauta, R. van Langevelde, and H. Tuinhout, "Analog circuits in ultradeep-submicron CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 132–143, Jan. 2005.
- [9] Y. Chiu, B. Nikolic, and P. Gray, "Scaling of analog-to-digital converters into ultra-deepsubmicron CMOS," in *Proc. IEEE CICC*, Sept. 2005, pp. 375–382.
- [10] J. Fiorenza, T. Sepke, P. Holloway, C. Sodini, and H.-S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2658–2668, Dec. 2006.
- [11] L. Brook and H.-S. Lee, "A zero-crossing-based 8-bit 200 Ms/s pipelined ADC," IEEE J. Solid-State Circuits, vol. 42, no. 12, pp. 2677–2687, Dec. 2007.

- [12] S.-K. Shin, Y.-S. You, S.-H. Lee, K.-H. Moon, J.-W. Kim, L. Brooks, and H.-S. Lee, "A fully-differential zero-crossing-based 1.2V 10b 26MS/s pipelined ADC in 65nm CMOS," in *IEEE Symp. VLSI Circ.*, Jun 2008, pp. 218–219.
- [13] L. Brooks and H.-S. Lee, "A 12b, 50 Ms/s, fully differential zero-crossing based pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3329–3343, Dec. 2009.
- [14] M.-C. Huang and S. luan Liu, "A fully differential comparator-based switched-capacitor $\Delta\Sigma$ modulator," *IEEE Trans. Circuits Syst. II Expr. Briefs*, vol. 56, no. 5, pp. 369–373, May 2009.
- [15] T. Musah, S. Kwon, H. Lakdawala, K. Soumyanath, and U.-K. Moon, "A $630\mu w$ zerocrossing-based $\Delta\Sigma$ ADC using switched-resistor current sources in 45nm CMOS," in *Proc. IEEE CICC*, Sept. 2009.
- [16] K. Yamamoto and A. Carusone, "A 1-1-1-1 MASH delta-sigma modulator with dynamic comparator-based OTAs," *IEEE J. Solid-State Circuits*, vol. 47, no. 8, pp. 1866 –1883, Aug. 2012.
- [17] K. Bult, "The effect of technology scaling on power dissipation in analog circuits," in *Analog Circuit Design*, M. Steyaert, A. H. M. Roermund, and J. H. v. Huijsing, (eds.), Springer, 2006.
- [18] K.-T. Tiew and M. Je, "A 0.06-mm² double-sampling single-OTA 2nd-order $\Delta\Sigma$ modulator in 0.18- μ m CMOS technology," in *Proc. IEEE Asian Solid-State Circ. Conf.*, Nov. 2011, pp. 253–256.
- [19] P. Hurst and W. McIntyre, "Double sampling in switched-capacitor delta-sigma A/D converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1990, pp. 902–905.
- [20] P. Rombouts, J. De Maeyer, and L. Weyten, "A 250-kHz 94-dB double-sampling ΣΔ modulation A/D converter with a modified noise transfer function," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1657–1662, Oct. 2003.
- [21] M. G. Kim, G.-C. Ahn, P. Hanumolu, S.-H. Lee, S.-H. Kim, S.-B. You, J.-W. Kim, G. C. Temes, and U.-K. Moon, "A 0.9 V 92 dB double-sampled switched-RC delta-sigma audio ADC," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1195–1206, May 2008.
- [22] Z. Yang, L. Yao, and Y. Lian, "A 0.5-V 35µW 85-dB DR double-sampled ΔΣ modulator for audio applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 722–735, Mar. 2012.
- [23] T. Burmas, K. Dyer, P. Hurst, and S. Lewis, "A second-order double-sampled delta-sigma modulator using additive-error switching," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 284–293, Mar. 1996.
- [24] C. Thanh, S. Lewis, and P. Hurst, "A second-order double-sampled delta-sigma modulator using individual-level averaging," *IEEE J. Solid-State Circuits*, vol. 32, no. 8, pp. 1269– 1273, Aug. 1997.

- [25] D. Senderowicz, G. Nicollini, S. Pernici, A. Nagari, P. Confalonieri, and C. Dallavalle, "Low-voltage double-sampled ΣΔ converters," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1907–1919, Dec. 1997.
- [26] B. Murmann and B. Boser, "A 12-bit 75-Ms/s pipelined ADC using open-loop residue amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.
- [27] E. Iroaga and B. Murmann, "A 12-Bit 75-MS/s pipelined ADC using incomplete settling," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 748–756, Apr. 2007.
- [28] I. Ahmed, J. Mulder, and D. Johns, "A low-power capacitive charge pump based pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1016–1027, May 2010.
- [29] K. Nagaraj, H. Fetterman, J. Anidjar, S. Lewis, and R. Renninger, "A 250-mW, 8-b, 52-Msamples/s parallel-pipelined A/D converter with reduced number of amplifiers," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 312–320, Mar. 1997.
- [30] B.-M. Min, P. Kim, I. Bowman, F.W., D. Boisvert, and A. Aude, "A 69-mW 10-bit 80-MSample/s Pipelined CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2031–2039, Dec. 2003.
- [31] S. Ryu, B. Song, and K. Bacrania, "A 10-bit 50-MS/s Pipelined ADC with opamp current reuse," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 475–485, Mar. 2007.
- [32] C.-H. Kuo, T.-H. Kuo, and K.-L. Wen, "Bias-and-input interchanging technique for cyclic/pipelined ADCs with opamp sharing," *IEEE Trans. Circuits Syst. II: Expr. Briefs*, vol. 57, no. 3, pp. 168–172, Mar. 2010.
- [33] B.-S. Song, "A 4th-order bandpass $\Delta\Sigma$ modulator with reduced number of op amps," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1995, pp. 204–205.
- [34] J. Goes, B. Vaz, R. Monteiro, and N. Paulino, "A 0.9V ΔΣ modulator with 80dB SNDR and 83dB DR using a single-phase technique," in *IEEE Int. Solid-State Circuits Conf.* (*ISSCC*) Dig. Tech. Papers, Feb. 2006, pp. 191–200.
- [35] J. Sauerbrey, T. Tille, D. Schmitt-Landsiedel, and R. Thewes, "A 0.7V MOSFET-only switched-opamp ΣΔ modulator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2002, pp. 310–311.
- [36] A. Gerosa and A. Neviani, "A 1.8-μw sigma-delta modulator for 8-bit digitization of cardiac signals in implantable pacemakers operating down to 1.8 v," *IEEE Trans. Circuits Syst. II Expr. Briefs*, vol. 52, no. 2, pp. 71–76, Feb. 2005.
- [37] J. Silva, U. Moon, J. Steensgaard, and G. Temes, "Wideband low-distortion delta-sigma ADC topology," *Electron. Lett.*, vol. 37, no. 12, pp. 737–738, Jun 2001.
- [38] L. Liu, D. Li, L. Chen, Y. Ye, and Z. Wang, "A 1-V 15-bit audio $\Delta\Sigma$ -ADC in 0.18 μ m CMOS," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 59, no. 5, pp. 915–925, May 2012.

- [39] H. Park, K. Nam, D. Su, K. Vleugels, and B. Wooley, "A 0.7-V 870µw digital-audio CMOS sigma-delta modulator," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1078– 1088, Apr. 2009.
- [40] J. Wang, T. Matsuoka, and K. Taniguchi, "A 0.5 V feedforward delta-sigma modulator with inverter-based integrator," in *Proc. of European Solid-State Circ. Conf. (ESSCIRC)*, Sept. 2009, pp. 328–331.
- [41] Y. Chae and G. Han, "Low voltage, low power, inverter-based switched-capacitor deltasigma modulator," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 458–472, Feb. 2009.
- [42] B. Razavi, Design of Analog CMOS Integrated Circuits. New York: McGraw-Hill, 2000.
- [43] T. C. Carusone, D. A. Johns, and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley, 2011.
- [44] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Wiley IEEE Press, 2004.
- [45] E. Alpman, H. Lakdawala, L. Carley, and K. Soumyanath, "A 1.1V 50mW 2.5GS/s 7b time-interleaved C-2C SAR ADC in 45nm LP digital CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 76–77.
- [46] Z. Cao, S. Yan, and Y. Li, "A 32mW 1.25GS/s 6b 2b/step SAR ADC in 0.13μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 542– 634.
- [47] I. Akita, M. Furuta, J. Matsuno, and T. Itakura, "A 7-bit 1.5-GS/s time-interleaved SAR ADC with dynamic track-and-hold amplifier," in *IEEE Asian Solid State Circuits Conf.* (A-SSCC), Nov. 2011, pp. 293–296.
- [48] Y.-Z. Lin, C.-C. Liu, G.-Y. Huang, Y.-T. Shyu, and S.-J. Chang, "A 9-bit 150-MS/s 1.53mW subranged SAR ADC in 90-nm CMOS," in *IEEE Symp. on VLSI Circuits*, Jun. 2010, pp. 243–244.
- [49] W. Liu, P. Huang, and Y. Chiu, "A 12-bit 50-MS/s 3.3-mW SAR ADC with background digital calibration," in *IEEE Custom Integrated Circuits Conference (CICC)*, Sept. 2012, pp. 1–4.
- [50] M. Yoshioka, K. Ishikawa, T. Takayama, and S. Tsukamoto, "A 10b 50MS/s 820µW SAR ADC with on-chip digital calibration," in *IEEE Intl. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 384–385.
- [51] W. Liu, P. Huang, and Y. Chiu, "A 12b 22.5/45MS/s 3.0mW 0.059mm² CMOS SAR ADC achieving over 90dB SFDR," in *IEEE Intl. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2010, pp. 380–381.
- [52] J. Dickson, "On-chip high-voltage generation in MOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, Jun. 1976.

- [53] T. Cho and P. Gray, "A 10-b, 20-Msample/s, 35-mW pipeline A/D converter," IEEE J. Solid-State Circuits, vol. 30, no. 3, pp. 166–172, Mar. 1995.
- [54] S. Rabii and B. Wooley, "A 1.8-V digital-audio sigma-delta modulator in 0.8-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 783 –796, Jun. 1997.
- [55] A. Nilchi and D. A. Johns, "Charge-pump based switched-capacitor integrator for $\Delta\Sigma$ modulators," *Electron. Lett.*, vol. 46, no. 6, pp. 400–401, Mar. 2010.
- [56] T. Wang and G. C. Temes, "Low-power parasitic-insensitive switched-capacitor integrator for delta-sigma ADCs," *Electron. Lett.*, vol. 46, no. 16, pp. 1114–1116, May 2010.
- [57] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 52, no. 11, pp. 2358–2368, Nov. 2005.
- [58] P. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits. New York: Wiley, 2001.
- [59] A. Hamoui, T. Alhajj, and M. Taherzadeh-Sani, "Behavioral modeling of opamp gain and dynamic effects for power optimization of delta-sigma modulators and pipelined ADCs," in *Int. Symp. on Low Power Electron. and Design (ISLPED)*, Oct. 2006, pp. 330–333.
- [60] F. Wang and R. Harjani, "Power analysis and optimal design of op amps for oversampled converters," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 46, no. 4, pp. 359–369, Apr. 1999.
- [61] A. Nilchi and D. A. Johns, "Analysis of thermal noise and the effect of parasitics in the charge-pump integrator," in *Ph.D. Research in Microelectronics and Electronics Conference (PRIME)*, Jul. 2010.
- [62] T. C. Caldwell and R. Schreier, "Noise in SC circuits," in University of Toronto ECE1371 Course Notes, 2009.
- [63] K. Kundert, "Simulating switched-capacitor filters with SpectreRF," [Online]. Available: http://www.designers-guide.com/Analysis//sc-filters.pdf.
- [64] B. E. Boser and B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1298–1308, Dec. 1988.
- [65] A. Nilchi and D. A. Johns, "Charge-pump based switched-capacitor gain stage," in *Proc. IEEE Int. Midwest Symp. Circuits Syst.*, Aug. 2012.
- [66] D. Cline and P. Gray, "A power optimized 13-b 5 Msamples/s pipelined analog-to-digital converter in 1.2 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 294–303, Mar 1996.
- [67] S. Devarajan, L. Singer, D. Kelly, S. Decker, A. Kamath, and P. Wilkins, "A 16-bit, 125 MS/s, 385 mW, 78.7 dB SNR CMOS pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3305–3313, Dec. 2009.

- [68] A. Nilchi and D. A. Johns, "A low-power delta-sigma modulator using a charge-pump integrator," *Accepted for publication in IEEE Trans. Circuits Syst. I: Regular Papers.*
- [69] R. Schreier, "The delta-sigma toolbox for Matlab," [Online]. Available: http://www.mathworks.com/matlabcentral/fileexchange/19.
- [70] A. Gharbiya and D. Johns, "On the implementation of input-feedforward delta-sigma modulators," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 53, no. 6, pp. 453–457, June 2006.
- [71] Y. Yang, A. Chokhawala, M. Alexander, J. Melanson, and D. Hester, "A 114-dB 68-mW chopper-stabilized stereo multibit audio ADC in 5.62 mm²," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2061–2068, Dec. 2003.
- [72] L. Sumanen, M. Waltari, V. Hakkarainen, and K. Halonen, "CMOS dynamic comparators for pipeline A/D converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2002, pp. 157–160.
- [73] M. Miller and C. Petrie, "A multibit sigma-delta ADC for multimode receivers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 475–482, Mar. 2003.
- [74] H. W. Ott, "Partitioning and layout of a mixed-signal PCB," in *Printed Circuit Design Magazine*, Jun. 2001.
- [75] C.-H. Kuo, D.-Y. Shi, and K.-S. Chang, "A low-voltage fourth-order cascade delta-sigma modulator in 0.18-μm CMOS," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 57, no. 9, pp. 2450–2461, Sept. 2010.