Design of a Power Scalable Capacitive MEMS Accelerometer Front End

by

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Graduate Department of Electrical and Computer Engineering
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Abstract

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This thesis presents the design, implementation and fabrication for a 0.13μm interface to a capacitive MEMS accelerometer.

By varying the number of amplifier slices used in concurrence based on different full scale input ranges, the analog circuitry power scales as the input range scales. Due to the oversampling nature of typical accelerometer front ends, for a full-scale input increase of N times, the analog circuitry power reduces by N^2 times. The front end has two signal amplification stages, with the first stage power scaled. The chip is 1.15mmx1.15mm and implemented in a 0.13μm CMOS process. The design was packaged with the MEMS accelerometer chip inside a 44 pin CQFP. Measured results show an output rms noise of 63μV_{rms} in a 100Hz bandwidth. The total analog circuitry power scales very linearly with different full scale ranges.

A novel simple offset removal network is also shown and confirmed via measurement results.

Acknowledgments

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List of Acronyms

g: 1 ‘unit’ of earth’s gravity, approximately 9.81m/s^2 of acceleration

CAGR: Compound Annual Growth Rate

MEMS: Micro-Electro-Mechanical Systems

SAW: Surface Acoustic Wave

CT: Continuous Time

DT: Discrete Time

SC: Switched Capacitor

CM: Common Mode

CMFB: Common Mode Feedback

ICMFB: Input Common Mode Feedback

C2V: Capacitance to Voltage

CVC: Capacitance to Voltage Converter

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

NMOS: N-Type Metal Oxide Semiconductor

PMOS: P-Type Metal Oxide Semiconductor

SNR: Signal to Noise Ratio

SDR: Signal to Distortion Ratio

SNDR: Signal to Noise and Distortion Ratio

ADC: Analog to Digital Converter

CQFP: Ceramic Quad Flat Pack

PCB: Printed Circuit Board

PSD: Power Spectral Density

Chapter 1

Introduction to MEMS sensors

This thesis presents a MEMS accelerometer front end circuit in 0.13 μm CMOS with power scalability and a miniature offset removal network. Section 1.1 will give an introduction to the MEMS market, as well as the accelerometer market. Section 1.2 shows some of the various applications of accelerometers. Section 1.3 details the motivation for this work.

1.1 Introduction

Microelectromechanical systems (MEMS) is a technology involving small systems with both mechanical devices and electrical components. MEMS devices include accelerometers and gyroscopes in navigation and safety systems, digital micromirror devices (DMD) in projectors, DNA microarrays for rapid DNA analysis, and inkjet print heads in many printers. Recent demand for MEMS devices has made it one of the fastest growing technologies.

A global market revenue forecast in 2011 (Fig. 1.1 [1]) predicted a very significant growth of 10.2% compounded annual growth rate (CAGR) with double the market value by 2016. A more recent forecast expects an even larger CAGR of 12.4% during the years 2011 – 2015 [2]. MEMS sensors make up a significant portion of this market value. Their forecasted growth is quite large due to recent use in a wide variety of consumer electronics and automotive applications. In particular, accelerometers play a key role in healthcare, vehicle safety, industrial applications, and more recently in

consumer electronics and appliances. They are currently one of the fastest growing MEMS sensors, and have been forecasted to grow at a CAGR of 17.5% in the same 2011 – 2015 time span [3].

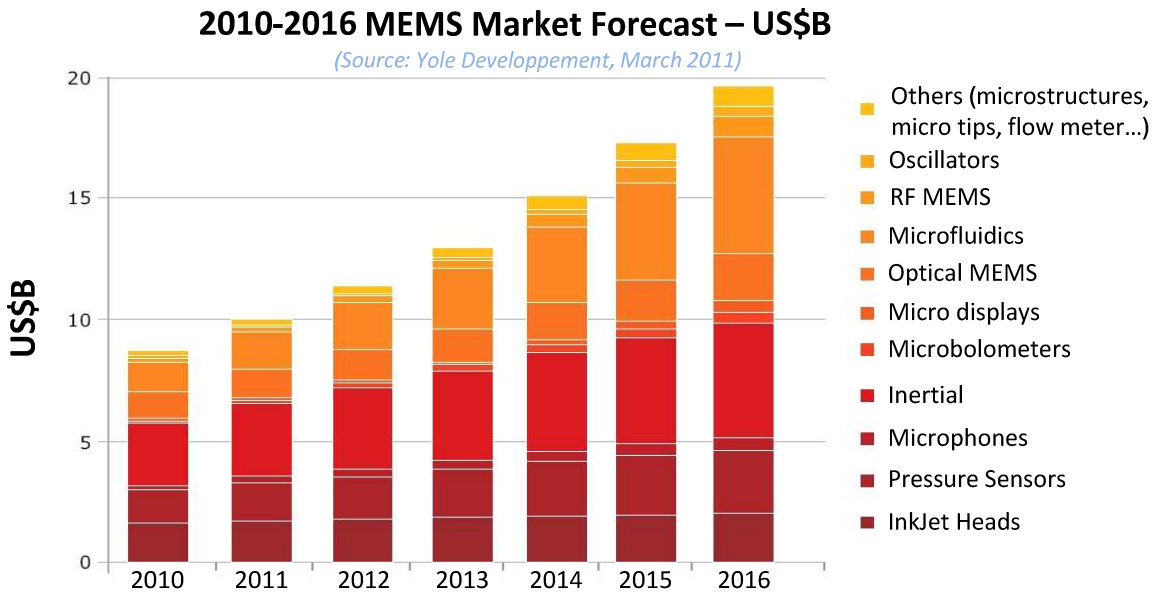

Fig. 1.1: 2011 MEMS Market Forecast [1]

The task of any sensor is to convert a measured physical quantity into a form which can be easily read or manipulated. In the case of an accelerometer, the physical quantity is force. This force is converted to acceleration through Newton's law F=ma. The output is an electrical quantity (typically capacitance) that represents this acceleration. This electrical quantity enables us to interface the accelerometer with a circuit.

1.2 Accelerometer Applications

Accelerometers play a large role in the world around us. There are a multitude of applications in which they are used. A list of some applications is shown below:

- **Automotive Applications**
  - Airbag deployment

- Anti-Lock Braking Systems/Traction Control Systems
- Vehicle Dynamics Control/Electronic Stability Control systems
- Anti-Theft Systems
- Active Suspensions

- **Industrial Applications**
  - Vehicle Tilt Monitoring
  - Railway Applications (Train Inclination and suspension)
  - Oil drilling, tilt measurement in harsh environments
  - Seismic Imaging and oil exploration
  - Structural stability tests

- **Consumer Electronics**
  - Inertial Navigation/GPS aid
  - Smartphones/Tablets/Laptops
  - Video Game Consoles
  - Sports aids (running devices, pedometers, etc)
  - Picture/Video image stabilization/anti-blur
  - Other: Hard Disk Protection

- **Medical/Sciences**
  - Sport Sciences
  - Geophysical Applications (ex earthquake monitoring)
  - Medical Treatment: Evaluating disorders, Radiation oncology

- **Military/Aerospace**
  - Explosions/Weapons Tests
  - Military Surveillance
  - Smart Weapons
  - Structural Analysis
  - Flight Testing

Many of these applications can require different full scale ranges. For instance, in automotive applications, whereas anti-lock braking systems and traction control systems have a typical range of ±1g, while vertical body motion of the car uses sensors in the ±2g range [4].

1.3 Motivation

Accelerometers in the market typically have multiple full scale range options. Common full scale ranges used are anywhere in a 1g to 8g range. The power of the full front end circuitry of commercial accelerometers is a constant independent of the full scale. A change in full scale causes a change in the dynamic range. However, constant dynamic range is desired in certain applications. For instance, if we use variable dynamic range and a specific error is targeted, if the full scale increases by a factor of 2, the error will decrease by a factor of 2. Since this new error is well below the target error, this means that power is being wasted.

In the case of an input full scale variation of 2 times and constant dynamic range, it is possible to save up to 2^2 or 4 times the power in the front end analog circuitry. For instance, for a full scale range of 1g and 10 bit accuracy, the minimum resolution is 1mg. If the full scale is now 2g, then the minimum resolution is now 2mg. Resolving 1mg requires 4 times the power than resolving 2 mg. The reason for this is that the sensor capacitance remains unchanged, meaning the kT/C noise remains the same. Since uncorrelated noise adds in a square root of sums fashion, in order to resolve a signal 2 times smaller, we must take 4 times the number of averaged samples which implies both 4 times the speed and 4 times the power. In general, if the input full scale is increased by n times, the theoretical power savings in the analog circuitry can be up to n^2.

The goal of this project is to create an open loop front end circuit for a capacitive accelerometer that will implement this power scalability based on full scale range. A chip was built in 0.13 um CMOS technology, and interfaced to an accelerometer supplied by Bosch. To demonstrate this scalability, a common accuracy of 9 bit SNDR is chosen with a selectable full scale range from 1g to 4g.

The second goal concerns offset, which is a major consideration in accelerometer front ends. The measured changes in capacitance are extremely small, typically on the order of attoFarads, or 10^{-18} Farads. This means that gains must be quite high, and so small capacitive offsets can potentially saturate the amplifiers. A novel, simplified offset removal network is presented as well.

Finally, advantages of inverting the clock phases of the typical inverting switched capacitor front ends are shown.

1.4 Thesis Outline

The remainder of this thesis is organized as follows:

- Chapter 2 describes background information on MEMS accelerometers. It then details implementation and circuit level challenges involved in building the front end circuitry.
- Chapter 3 details the system level design of the full front end circuit, as well as post layout simulation results.
- Chapter 4 summarizes the PCB designed, the test setup and the measurement results of the front end circuit.
- Chapter 5 concludes this thesis with a summary of the key aspects of the design. Potential future work is also detailed.

Chapter 2

Background

This chapter begins with an introduction to accelerometers. Second, capacitive accelerometers and some of the design challenges are described in more detail. Finally, a few recently published papers on accelerometer interfaces are described.

2.1 Types of Accelerometers

Today, there exist a multitude of different types of accelerometers. These include optical, resonant, tunnelling, surface-acoustic wave (SAW), thermal, piezoresistive, piezoelectric, and capacitive accelerometers. These will be described briefly, with piezoresistive piezoelectric, and capacitive described in more detail due to their more popular usage.

As shown in Fig 2.1, optical accelerometers use two optical fibers; one in which light enters, and one in which it exits and is measured. The amount of light in the return path will vary depending on a mass that moves due to external forces acting on the device, as shown in Fig 2.1. Optical accelerometers have high sensitivity.

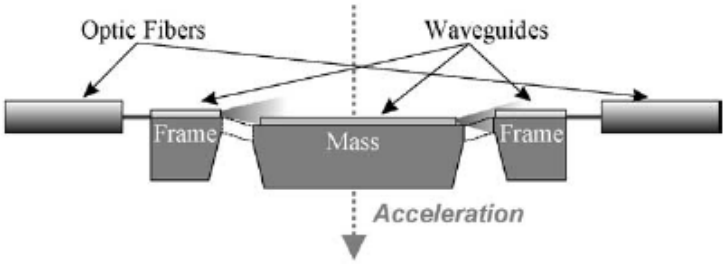

Fig. 2.1: Optical Accelerometer [5]

A tunnelling accelerometer works by measuring the changes in tunnelling current between a tunnelling tip and a 'counter' electrode. The distance between the tip and the electrode vary with external acceleration. Tunnelling accelerometers have extremely high sensitivity, on the order of a few V/g to as high as 50V/g. They can also have very high dynamic ranges. However, they vary strongly with temperature, as the tunneling gap distance changes considerably over temperature. Tunnelling accelerometers also tend to have large amounts of flicker noise, which can be very troublesome considering the low frequencies involved [6]. Fig 2.2 shows an example of a tunneling accelerometer.

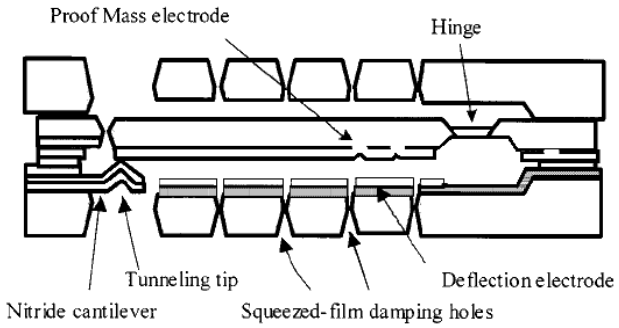

Fig. 2.2: Tunneling Accelerometer [7]

A resonant accelerometer works by inducing a frequency shift on a resonator due to stresses/loading caused by external forces acting on a mass (Fig 2.3). This is similar to a SAW accelerometer, which transmits a surface acoustic wave across a piezoelectric substrate. This wave is changed from stresses induced on the piezoelectric material due to acceleration. After crossing the substrate, the wave is converted back into an electrical signal and measured.

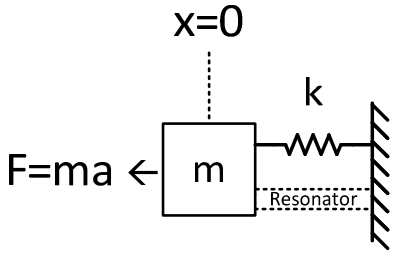

Fig. 2.3: Resonant Accelerometer

A thermal accelerometer consists of a heater in the middle of an open area on a rigid substrate. Thermal sensors are spaced equidistant from this heater, and the variations in temperature are measured, which indicate the applied acceleration. These tend to be very sensitive to the ambient temperature.

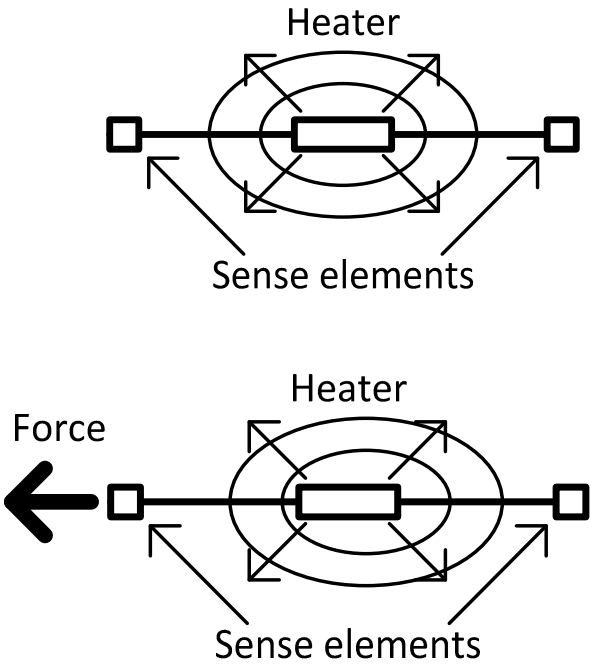

Fig. 2.4: Thermal Accelerometer

Commercially, the most common of accelerometers are the capacitive, piezoelectric, and piezoresistive sensors so these will be described in a bit more detail.

2.2 Piezoresistive Accelerometers

A piezoresistive accelerometer attaches a piezoresistive material to a mass. When the mass deflects, this induces stress/strain on the piezoresistor, and the resistive properties of the material change. In Fig. 2.5 below, a thin piezoresistor is placed on top of a cantilever. Since the top of a bending beam will have tension/compression and the bottom will have compression/tension, this ensures that the piezoresistor is only under tensile or compressive stress. This means that the effect of stress/strain on resistance is not cancelled out by opposite stress components.

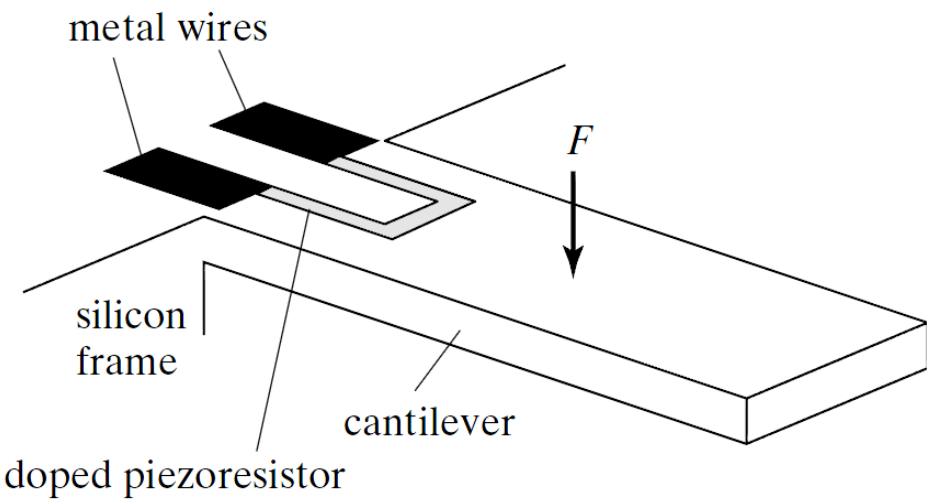

Fig. 2.5: Piezoresistive Accelerometer [8]

Piezoresistive accelerometers have several advantages:

- Tend to have a simple interface
- Can survive high shock conditions
- Medium frequency range (about 10kHz)
- Can measure very low frequency accelerations

Unfortunately, there are some major disadvantages as well:

- Low sensitivity (10's of mV/g-~150mV/g)[9]
- Tend to suffer from the effects of acceleration in perpendicular directions
- Tend to have higher power consumption; typically a Wheatstone bridge is used at the front end.
- The resistance exhibits temperature dependence and limits high-temperature use [10]

In particular, the low sensitivity and the temperature dependence exhibited are major weaknesses of the piezoelectric structures

2.3 Piezoelectric Accelerometers

Piezoelectric accelerometers are typically made from quartz or a piezoelectric ceramic. A mass subjected to some acceleration places stress on the piezoelectric material, causing

an output charge to appear between opposite ends of the piezoelectric material (Fig. 2.6). Since piezoelectric materials respond to changes in stress, these accelerometers cannot directly measure DC and very low frequency accelerations, which is a major disadvantage. A plot of a typical frequency response is shown in Fig 2.7, showing magnitude dropoff as DC is approached.

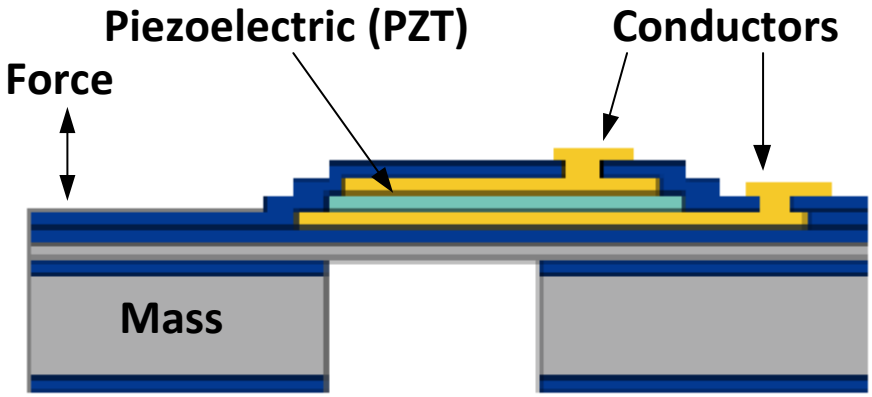

Fig. 2.6: Piezoelectric Accelerometer [11]

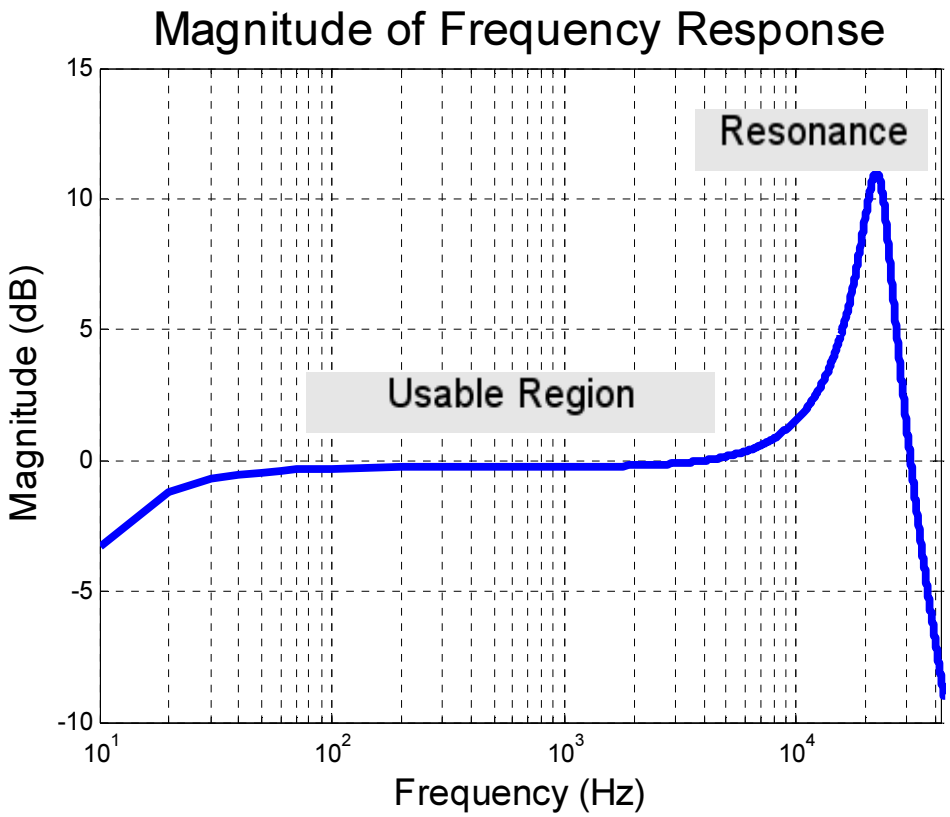

Fig. 2.7: Frequency response of piezoelectric accelerometer

Some of its advantages are [12]:

- Very high shock survival (up to 100,000g's)
- Very high dynamic range (due to large full scale range)
- Very high frequency range (10's of kHz)
- Very high temperature range (well below -40°C to above 100°C)
- Low power circuit interface (can be below 10's of μW)

Some disadvantages are:

- No DC response
- Low sensitivity (10-100mV/g)
- Sensitivity degradation with time
- High output impedance
- Temperature dependence of piezoelectric material
- More complex interface circuit

These accelerometers can operate in shear, flexural, or compressive modes, depending on the direction of the force acting on the piezoelectric material. Shear mode is the most common, as shear mode accelerometers tend to be smaller, have a better frequency response, and have lower temperature sensitivity. Due to the high frequency response and wide dynamic range, piezoelectric accelerometers are used often in shock tests. In applications where low power is critical but a DC response and high resolution is not needed, piezoelectric accelerometers can be a very good choice.

2.4 Capacitive Accelerometers

Capacitive accelerometers are the most common types of MEMS accelerometers due to a high performance vs cost ratio. They also have minimal temperature dependence and a wide temperature range as the dielectric material is typically air. These work by making use of a miniature mass spring damper (2^{nd} order) system. Capacitive accelerometers are a differential structure, providing one capacitor that increases and one that decreases for

acceleration in the same direction. Two fixed structures act as a plate for two separate capacitors. The mass of the accelerometer acts as the second plate for both of these capacitors. Fig. 2.8 shows one finger of a typical capacitive accelerometer and its electrical equivalent model. The fourth terminal is the substrate of the MEMS die. For a surface micromachined device, the typical nominal value for C_{s+} and C_{s-} is around 200fF.

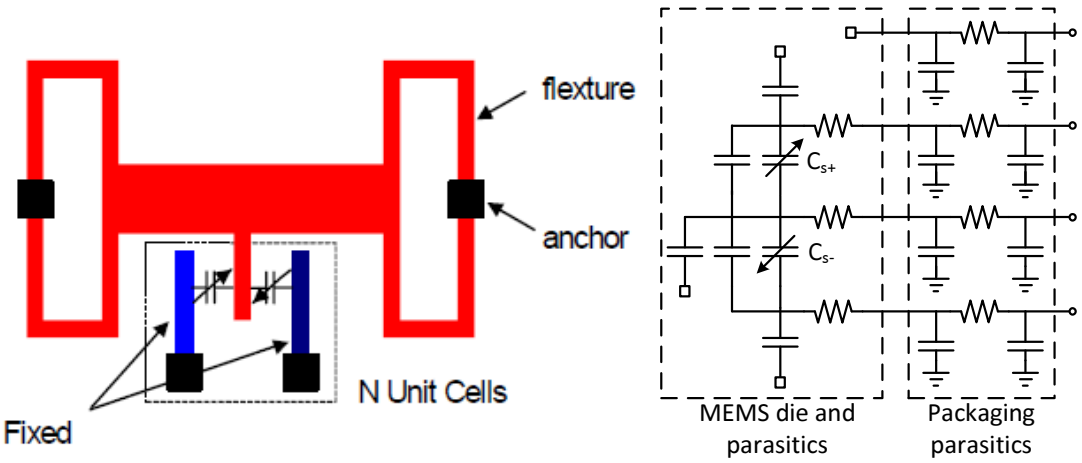

Fig. 2.8: Single Finger of Capacitive Accelerometer and Parasitics

When an acceleration is present, the mass moves and so the capacitances will change. Fig. 2.8 [13] only shows one finger of the accelerometer. In practice, there can be hundreds of these, with the appropriate fixed plates shorted to one another to provide the two differential capacitors. In the electrical domain, the accelerometer is simply seen as two capacitors: one that increases with a 'positive' acceleration, and one that decreases with a 'positive' acceleration. These capacitors have a common node (the mass), resulting in 3 electrical nodes. This is also shown in Fig. 2.8, along with the MEMS and packaging parasitics.

Some of the more important advantages of capacitive accelerometers are:

- High sensitivity (50mV/g – 900mV/g)
- Low temperature dependence due to gaseous dielectric
- Capable of measuring very low frequency accelerations
- Low power circuit interface(10's to 100's of μW)

- High temperature range

A few of its disadvantages are:

- Low frequency range (natural frequency: a few kHz)
- More complex interface circuit

Capacitive accelerometers are among the highest in sensitivity, and tend to have much less temperature dependence than other types of accelerometers. These advantages along with their cheap cost are the reason they are the most common among commercial devices. Since the front end for this project attaches to a capacitive accelerometer, these will be described in more detail.

2.5 Capacitive Accelerometer Model

The gap distance between the plates of the capacitors versus the input acceleration can be modelled with a mass spring damper system.

A spring mass damper system can be represented through a second order linear equation. The damping force is proportional to the velocity and the spring force to the displacement. The equation can be obtained by a simple force balance equation as shown below.

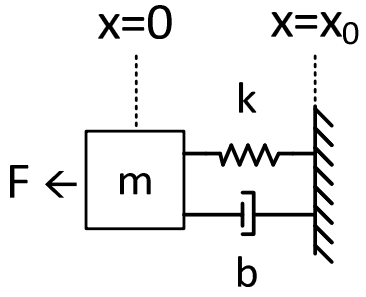

Fig. 2.9: Spring Mass Damper System

$$F_{ext}(t) = kx(t) + b\frac{dx(t)}{dt} + m\frac{d^2x(t)}{dt} \quad (2.1)$$

$$F_{ext}(s) = kx(s) + bsx(s) + ms^2x(s) \quad (2.2)$$

$$x(s) = \frac{a}{s^2 + \frac{b}{m}s + \frac{k}{m}} \quad (2.3)$$

$$\omega_n = \sqrt{\frac{k}{m}} \quad (2.4)$$

Here, ω_n is the resonant frequency of the system. Fig. 2.10 shows the frequency response for a typical underdamped accelerometer.

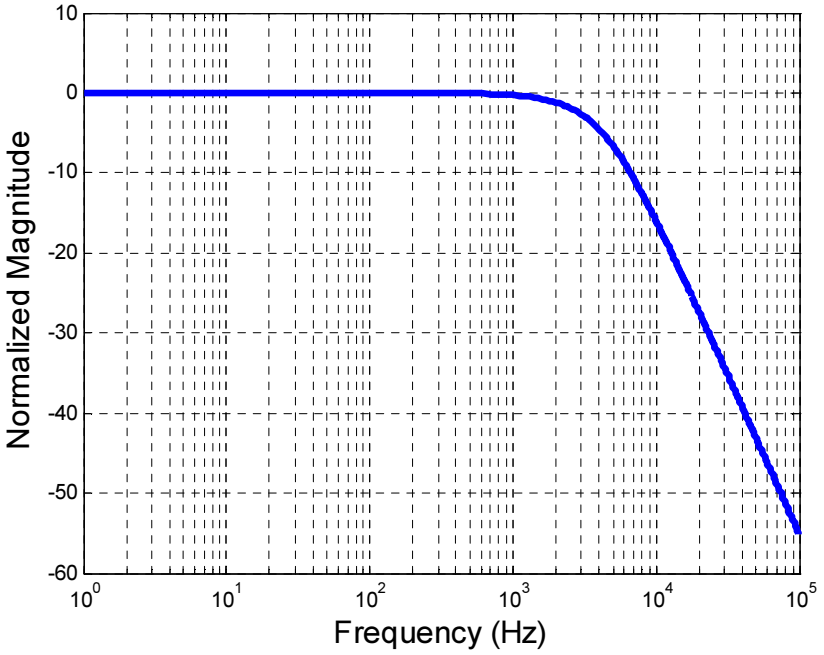

Fig. 2.10: Frequency Response of Typical Capacitive Accelerometer

Typical capacitive accelerometers have a resonant frequency of a few kHz, have a weight a few μg, and have a spring constant of a few N/m.

It is important to note that since the mass must move, the accelerometer capacitors are actually air gap capacitors; this means that any means of measurement that requires a voltage to be applied across the capacitors will actually cause an attractive electrostatic

force on the plates. This electrostatic force can potentially overcome the spring force. This is important to be aware of because in the event that this does happen, the accelerometer can be damaged. It is also possible that the mass will snap to one of the fixed plates and remain permanently stuck due to stiction (static friction). Fig. 2.11 shows typical mechanical ('over range') stops that are placed to prevent the mass from moving too close to the fixed plates. This protects the device from both physical damage and an electrical short.

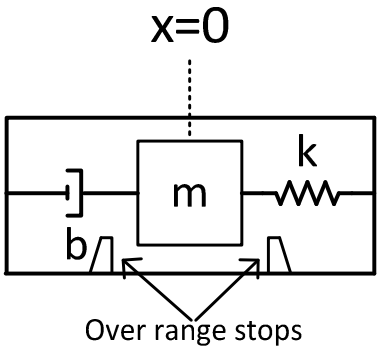

Fig. 2.11: Over Range Stops in a Capacitive Accelerometer

2.6 Undesired Electrostatic Forces and Pull In Voltage

The electrostatic force between two capacitive plates can be derived easily as follows. The work done in moving charges on a capacitor C to obtain a voltage V is

$$Wcap = \int QdV = \int CVdV = \frac{1}{2}CV^2 . \qquad (2.5)$$

For a parallel plate capacitor, the capacitance is

$$C = \frac{\varepsilon A}{(x_o - x)} . \qquad (2.6)$$

The variable x in this equation is defined in Fig. 2.9 above. Substituting (2.6) into (2.5) results in

$$Wcap = \frac{1}{2}QV = \frac{1}{2}CV^2 = \frac{1}{2}V^2\frac{\varepsilon A}{(x_o - x)}. \quad (2.7)$$

The force is (by definition) the derivative of the work done. Since the voltage is not a function of the displacement, we have

$$F_{electrostatic} = \frac{dW_{cap}}{dx} = \frac{d}{dx}\left(\frac{1}{2}V^2\frac{\varepsilon A}{(x_o - x)}\right) = -\frac{1}{2}V^2\frac{\varepsilon A}{(x_o - x)^2}. \quad (2.8)$$

An electrical spring constant can then be defined as

$$-k_{elec} = \frac{dF_{electrostatic}}{dx} = V^2\frac{\varepsilon A}{(x_o - x)^3}. \quad (2.9)$$

From (2.8), the electrostatic force is always negative regardless of x. This means that the electrostatic force is always attractive regardless of the direction of x, which is as expected since the charges on the capacitor plates are always opposite in sign. (2.8) also shows that if the applied voltage V is increased for a given position, $F_{electrostatic}$ will increase without bound. This means that for a large enough V, $F_{electrostatic}$ will eventually overcome the restoring spring force kx, causing two of the three accelerometer terminals to snap together and short circuit.

The equilibrium voltage for a given position can be calculated by equating F_{spring} and $F_{electrostatic}$.

$$F_{spring} = F_{electrostatic} \Leftrightarrow -kx = -\frac{1}{2}V^2\frac{\varepsilon A}{(x_o - x)^2} \quad (2.10)$$

$$\therefore V_{equil} = \sqrt{\frac{2kx(x_0 - x)^2}{\varepsilon A}} \quad (2.11)$$

Note that (2.11) above is only valid for $x<x_0$, otherwise this would mean the movable capacitor plate moves beyond the fixed plate. Fig. 2.12 below shows that there is a local maximum in V_{equil}.

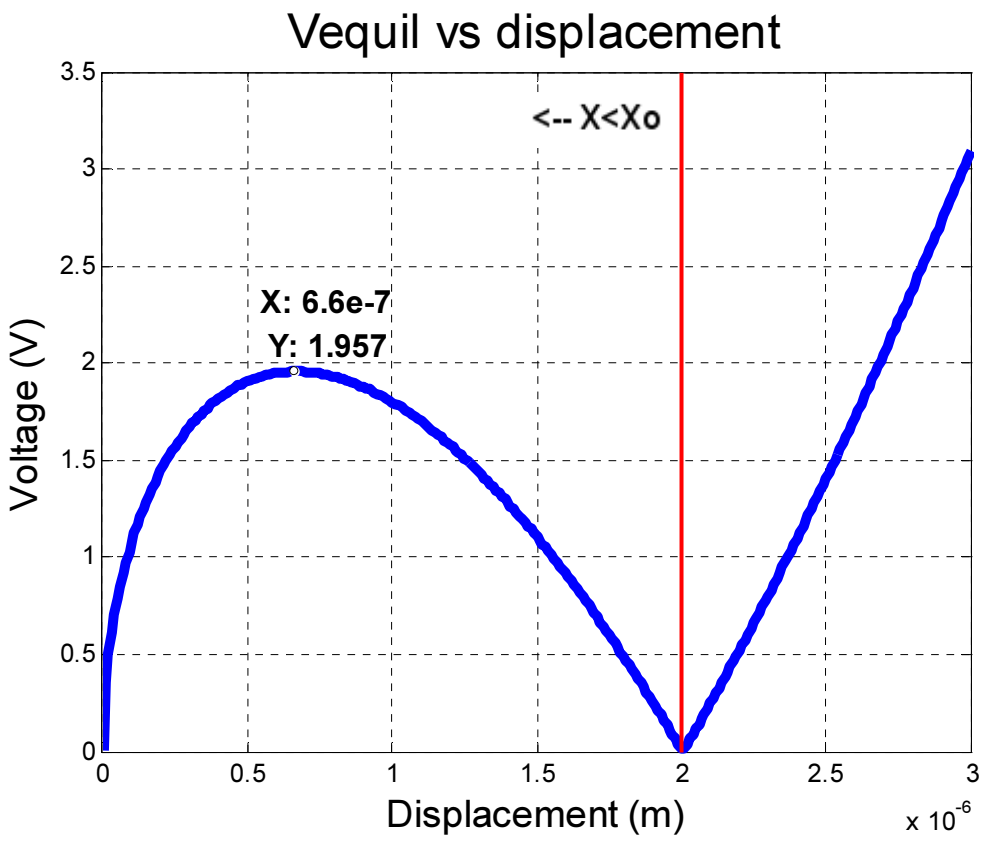

Fig. 2.12: Equilibrium Voltage for a Single Plate Accelerometer

We can find where the maximum occurs by equating the first derivative to 0.

$$\frac{dV_{equil}}{dx} = \frac{1}{2}\left(\frac{2kx(x_0 - x)^2}{\varepsilon A}\right)^{-1/2} \times \left\{2k(x_0 - x)^2 - 4kx(x_0 - x)\right\} = 0 \qquad (2.12)$$

The above equation is true for

$$\left\{2k(x_0 - x)^2 - 4kx(x_0 - x)\right\} = 0\,. \qquad (2.13)$$

$$x_{pull-in} = x_0, \frac{x_0}{3} \qquad (2.14)$$

$$\therefore x_{pull-in} = \frac{x_0}{3} \qquad (2.15)$$

Since the equation is only valid for $x<x_0$, we know this maximum occurs at $x_0/3$. Finally, substituting (2.15) into (2.11), we have

$$V_{pull-in} = \sqrt{\frac{8kx_0^3}{27\varepsilon A}}. \qquad (2.16)$$

This local maximum in voltage is called the pull in voltage, and represents the highest DC voltage that can be applied without the electrostatic force overcoming the spring force (when the mass is at $x=x_0/3$). Note that this is also the point where magnitudes of the electrical and mechanical spring constants are equal. Any DC voltages applied between these two plates must be well below the pull in voltage.

The above calculations were for a single capacitor accelerometer. Since most accelerometers use 2 differential plates, these equations change slightly. In the case of 2 differential (identical) capacitors, so long as the mass remains in the middle, the electrostatic forces balance out.

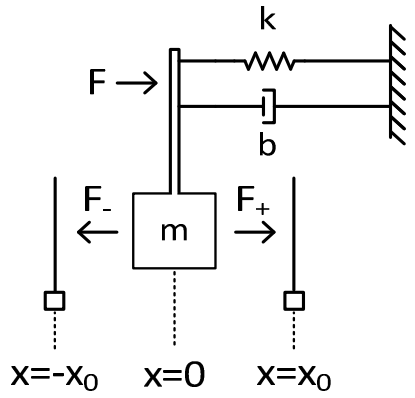

Fig. 2.13: Cancelling of Electrostatic Forces in a Differential Accelerometer

The electrostatic force now becomes the difference between the forces from each capacitive plate.

$$F_{electrostatic} = F_+ + F_- = \frac{1}{2}V^2\left(\frac{\varepsilon A}{(x_o - x)^2} - \frac{\varepsilon A}{(x_o + x)^2}\right) = \frac{\varepsilon A}{2}V^2\left(\frac{4x_0 x}{(x_0 - x)^2}\right) \qquad (2.17)$$

$$k_{elec} = \frac{dF_{electrostatic}}{dx} = \frac{\varepsilon A}{2} V^2 \frac{4x_0^{\,3} + 12x_0 x^2}{(x_o - x)^3} \qquad (2.18)$$

Note that this new force can occur in either the positive or negative direction, depending on which of the two forces is larger. The pull in voltage can be calculated by equating the mechanical and electrical spring constants above [14], resulting in

$$V_{pull-in} = \left[\sqrt{\frac{k(x_0^{\,2} - x^2)^3}{2\varepsilon A(x_0^{\,3} + x_0 x^2)}} \right]_{\max} = \sqrt{\frac{kx_0^{\,3}}{2\varepsilon A}}\,. \qquad (2.19)$$

Note that this equation is very similar to the single capacitor case, apart from the difference in the constant term being larger. For the Bosch accelerometer, this voltage is approximately 2.5V (between the plates).

2.7 Distortion from undesired electrostatic force feedback

Equation 2.17 shows that the electrostatic force is actually a function of the position of the mass, x. A Taylor expansion of the force in the neighbourhood of x=c shows that there are higher order terms, implying that this force feedback actually becomes a source of distortion.

$$F_{electrostatic} = -\frac{1}{2} V^2 \frac{\varepsilon A}{(x_o - x)^2} = -\frac{1}{2} V^2 \varepsilon A \left\{ \frac{1}{(x_0 - c)^2} - \frac{2}{(x_0 - c)^3}(x - c) + \frac{3}{(x_0 - c)^4}(x - c)^2 - \ldots \right\} \qquad (2.20)$$

$$F_{electrostatic} = -\frac{1}{2} V^2 \frac{\varepsilon A}{(x_o - x)^2} = -\frac{1}{2} V^2 \varepsilon A \left\{ \frac{1}{x_0^{\,2}} - \frac{2}{x_0^{\,3}} x + \frac{3}{x_0^{\,4}} x - \ldots \right\} \qquad (2.21)$$

The equation in (2.21) is for the case c=0. This means that when the mass is not precisely centered between the two fixed plates, the applied voltage during measurement of the acceleration will cause distortion. In particular, it is clear that this distortion will be a strong function of the voltage applied on the accelerometer.

2.8 Noise

This section provides a brief background on noise sources in the electrical and mechanical domains, as well as the effects of oversampling.

2.8.1 Electronic Noise

In any electrical system, noise is of primary importance. The level of noise determines sizing of capacitors as well as sampling frequencies in an oversampled system, which in turn dictate how much power needs to be spent driving these capacitors.

The classic example of noise is a simple RC circuit shown in Fig. 2.14. In the lowpass RC filter below, a noise root spectral density of $V_{nr} = \sqrt{4k_B TR}$ is associated with the resistor. This passes through a lowpass filter, and integrating this effect over all frequencies yields an output rms noise voltage of $V_{norms} = \sqrt{k_B T/C}$.

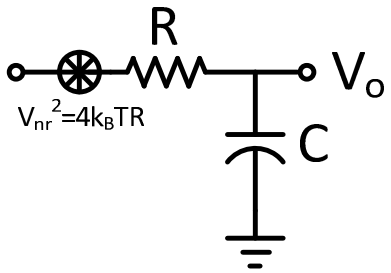

Fig. 2.14: RC Noise Model

For a sampled signal, the RC time constant is much smaller than the sampling period $T=1/f_s$ so that the signal is not attenuated. This means that the pole due to the low pass RC is always at least a few times higher than f_s. In a sampled system, the noise beyond the sampling frequency is in effect folded back so we obtain $V_{nrms} = \sqrt{k_B T/C}$ as expected. If we oversample, then we get an effective reduction by the OSR factor, so that $V_{nrms} = \sqrt{k_B T/(C \bullet OSR)}$.

2.8.2 Mechanical Noise

Since an RLC circuit has a similar governing equation as a mechanical spring mass damper system, we can define equivalencies between the two:

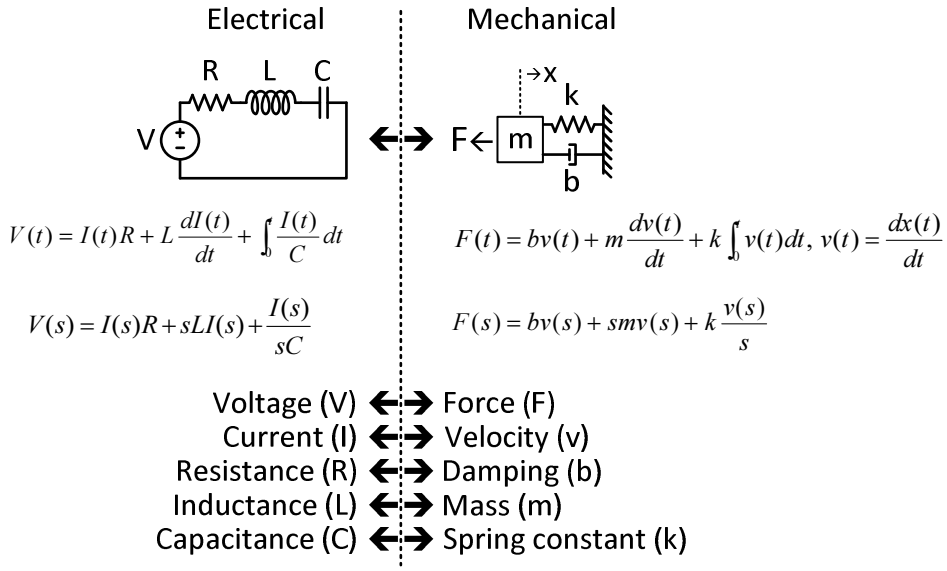

Fig. 2.15: Mechanical/Electrical equivalence

Using the equipartition theorem, assuming we have a linear mass-spring system, the energy in a spring is equal to

$$\int_0^x F dx = \frac{kx^2}{2}. \qquad (2.22)$$

$$\therefore \frac{k_B T}{2} = k x_{nrms}{}^2/2 \Rightarrow x_{nrms} = \sqrt{\frac{k_B T}{k}} \qquad (2.23)$$

In the above equations, T is temperature, k_B is Boltzmann's constant, F is force, and k is the spring constant. Notice the similarity to $V_{nrms} = \sqrt{kT/C}$, except that the capacitance is replaced with the spring constant.

Similar to the resistor voltage noise of $\sqrt{4k_B TR}$ in the electrical domain, a white spectral noise density force in a spring-mass-damper system is associated with the damping constant, $F_{nb} = \sqrt{4k_B Tb}$. This force represents the brownian noise in the mechanical

system. Since $F = ma$ and $F = kx$ for a spring, we can model the accelerometer noise as shown in Fig 2.16.

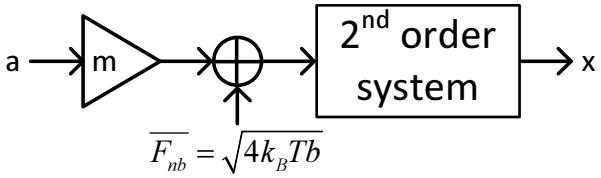

Fig. 2.16: Mechanical Noise Modelled by a Noise Force

So the input referred root noise spectral density can be calculated to be [15]

$$a_n = \frac{F_n}{m} = \sqrt{\frac{4k_B T \omega_0}{mQ}}\,. \qquad (2.24)$$

In (2.24), $Q = \omega_0 m / b$ is the quality factor and $\omega_0 = \sqrt{k/m}$ is the resonant frequency in radians/second. For the Bosch accelerometer this is close to $0.1 mg/\sqrt{Hz}$. Typically the electrical noise dominates, as if the Brownian noise dominates this means the electrical interface is overdesigned and power can be reduced in order to worsen the electrical noise.

2.9 Oversampling Limitations

In a mass spring damper system, the mechanical noise force passes through a second order system to an output displacement x, leading to a second order noise spectral density of the rms displacement noise.

Typical capacitive MEMS accelerometers are underdamped and have resonant frequencies around a few kHz. However, since accelerometer signal levels are extremely small, the interface is typically oversampled at a high OSR. As a result, the sampling frequencies are often much higher than the resonant frequency of the rms displacement noise. This case is unlike the typical sampling of a signal in the RC circuit above. In this case, the low pass filter is the MEMS accelerometer, and the resonant frequency can actually be lower than the sampling frequency. This means that the noise that is folded in

band is not quite thermal noise, but filtered by the MEMS device at $1/f^2$. This means that the improvement by a factor of $\sqrt{OSR}$ is in fact slightly less, and as the sampling frequency further increases, this improvement gradually decreases, and the in band noise gradually becomes less thermal.

This means that although oversampling does help improve the overall SNR, this improvement eventually diminishes, as when the sampling frequency moves too high, the higher frequency noise that is aliased back in band is a much smaller amplitude than the noise already in band.

2.10 Typical Front End Circuits

This section describes recent techniques that have been used in accelerometer front end circuits. The front end circuits typically use at least 2 gain stages due to the small signal levels. Generally, we can classify the front ends as open or closed loop systems, and continuous time or discrete time systems.

2.10.1 Closed Loop Front Ends

Closed loop front end circuits embed the mechanical MEMS sensor itself within a delta sigma feedback loop. However, instead of a voltage, the feedback is in the form of an electrostatic force applied to the accelerometer plates. This closes the loop and places the mechanical sensor within the feedback loop. Also, linearity due to the force feedback is minimized. This is because the mass will be near the center due to the feedback action of the delta sigma loop, causing the electrostatic forces to cancel out on average.

Since the accelerometer acts as a second order filter at a low resonance frequency, frequencies above the sensor resonance have a 180 degree phase shift. This causes issues with stability when the loop is closed, so that compensation is typically required [16]. The compensator must provide enough phase lead to ensure system stability at the unity gain frequency of the system loop gain [16][17].

2.10.2 Open Loop Front Ends

Open loop front ends do not make use of the ability to apply electrostatic forces on the accelerometer. This simplifies the circuitry considerably and removes issues of stability that are associated with closed loop designs. This simplification can lead to less design time and so help lower costs, which is why many products use open loop structures. However, the open loop circuits tend to be less linear than closed loop circuits. The open loop front ends are typically strictly oversampled in order to lower the noise floor.

2.10.3 Continuous Time vs Discrete Time Front Ends

Continuous Time (CT) front ends typically upmodulate the signal, convert it into a voltage, then demodulate. A standard way to do this is shown in Fig. 2.17.

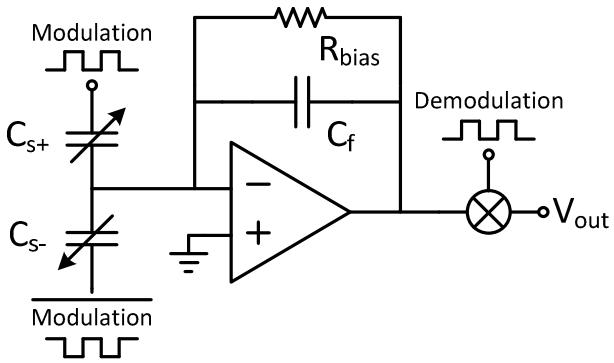

Fig. 2.17: Typical Continuous Time Accelerometer Front End

However, since capacitive accelerometers have very low resonance frequencies, biasing is a major challenge in CT front ends. For a typical CT circuit, a biasing resistor in the MΩ range can cause significant signal loss [18], and so an even higher resistance on the order of GΩ is often used [18][19]. Several different biasing schemes have been reported, including using subthreshold/'off' state transistors between the input and output of the amplifier, using subthreshold diode connected transistors to an internal opamp node [20], as well as making use of diode leakage currents [18].

Using a discrete time interface avoids these biasing issues. Since we are attempting to measure a capacitance in the case of capacitive accelerometers, a discrete time (DT) front end lends itself well to switched capacitor techniques. DT front ends use switched capacitor gain/integration stages in order to convert the delta capacitance into a voltage and multiply gain to the signal (Fig. 2.18). The accelerometer sense capacitors are typically used as the sampling capacitors in a typical switched capacitor amplifier; thus much of the thermal (electrical) noise is in fact a strong function of the size of the MEMS accelerometer and not the capacitors chosen in the circuit front end.

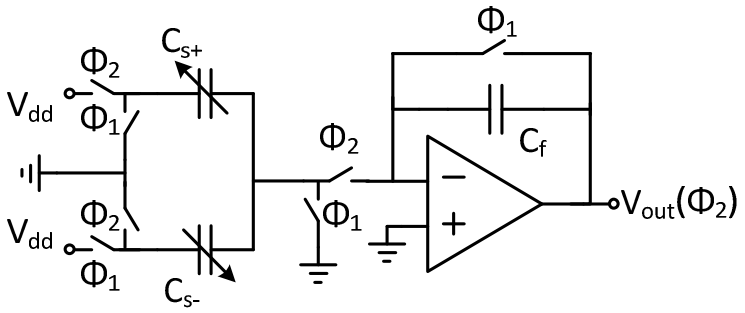

Fig. 2.18: Switched Capacitor Accelerometer Front End

2.10.4 Single Ended Front Ends vs Differential Front Ends

The circuits above are examples of single ended front ends, when only a single node is used as the input to the amplifier. However, differential circuits are typically preferred as both linearity and noise are improved for the same static power. One way to make the circuit differential is to drive the middle node (accelerometer mass) instead, as shown in Fig. 2.19 [21]. These so called 'differential' front ends are in fact pseudo-differential circuits due to the accelerometer capacitors being driven by a common node. This in fact leads to some complications which will be discussed in more detail in Chapter 3.

One technique to make the front end fully differential is to use two separate MEMS accelerometers. This however adds complexity in both the mechanical and electrical domains, and may not necessarily be feasible given a specific sensor. An example of a CT version of this is seen in Fig. 2.20 below.

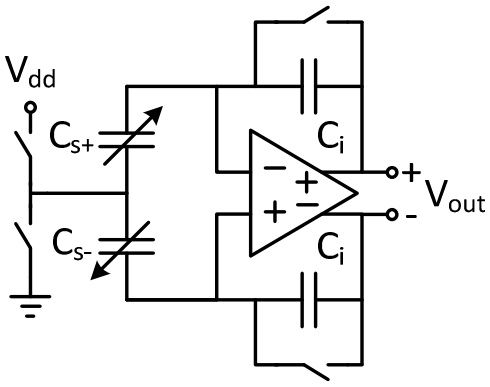

Fig. 2.19: Differential Accelerometer Front End

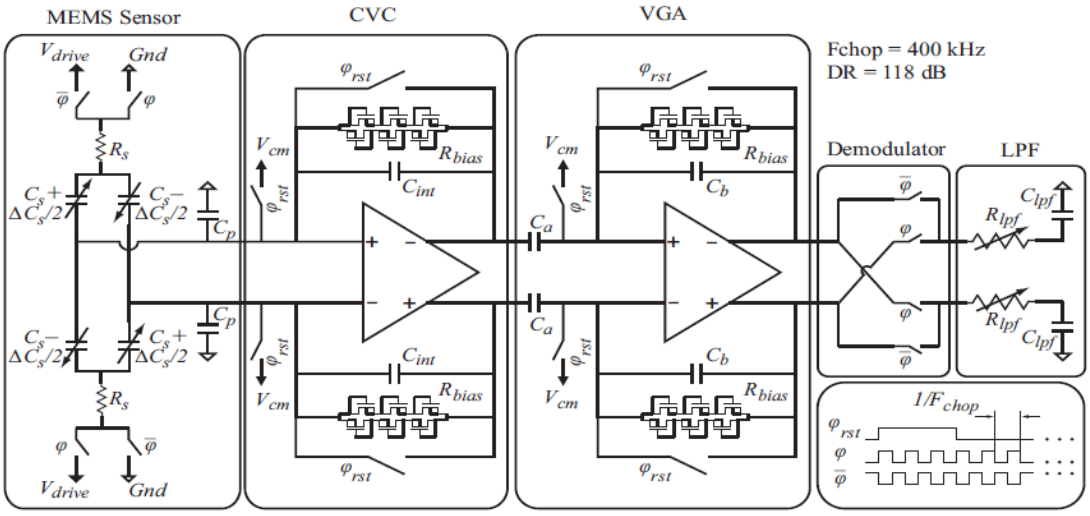

Fig. 2.20: Fully Differential Continuous Time Front End [22]

2.10.5 Distortion in Open Loop Structures

Distortion due to the undesired force feedback can be considerable in open loop front ends. This distortion is a function of the amount of force applied. From (2.17) above, we can see that this force is a very strong function of voltage (αV^2). The other variables in the equation are inherent to the sensor, and cannot be changed given a specific sensor to work with. However, although lowering the voltage seems like a good way to decrease the distortion, this directly reduces the signal amplitude at the output. This will be discussed further in the implementation section.

2.10.6 Offsets and Offset Removal Techniques

One major consideration in accelerometer interfaces is capacitive offset. A capacitive accelerometer measures the difference in between two capacitors. However, since this capacitance is on the order of a few attoFarads, a large system gain is required. This means that a small offset can easily saturate the output. For example, 1g acceleration will cause approximately a 2.5fF change in the Bosch sensor. For a sensitivity of 600mV/g, this means that merely 5fF of offset between the accelerometer capacitors is enough for a full 1.2 V offset in the output, easily saturating the output.

In order to alleviate this problem, offset removal networks are used. One possible solution is a differential pair to apply offset as shown in Fig 2.21 below.

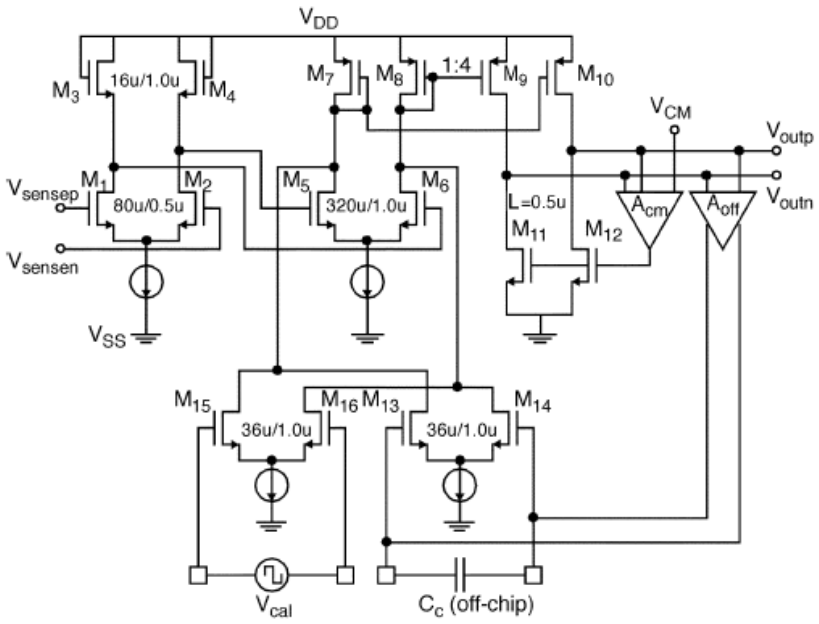

Fig. 2.21: Offset Removal via a Tuned Differential Pair [18]

[18] uses a CT front end. Here, two differential pairs are used for offset cancellation. One pair (M13, M14) removes offsets introduced by the circuit (with an additional filter), while the other differential pair M15 and M16 remove sensor offset. The problem with this is that an analog calibration voltage V_{cal} is required. Generating this on chip would require additional circuitry. The voltage would also vary across different chips. As well, this would add to the overall power consumption of the interface circuit.

Another common solution is a digitally controllable capacitor network which applies an effective offset in capacitance [19][21]. The circuit is shown in Fig. 2.22. The effective capacitance seen between nodes A and B in Fig. 2.22 is small. This network is applied in parallel to each of the two accelerometer capacitors. Bits b0 to b3 control the magnitude of the offset.

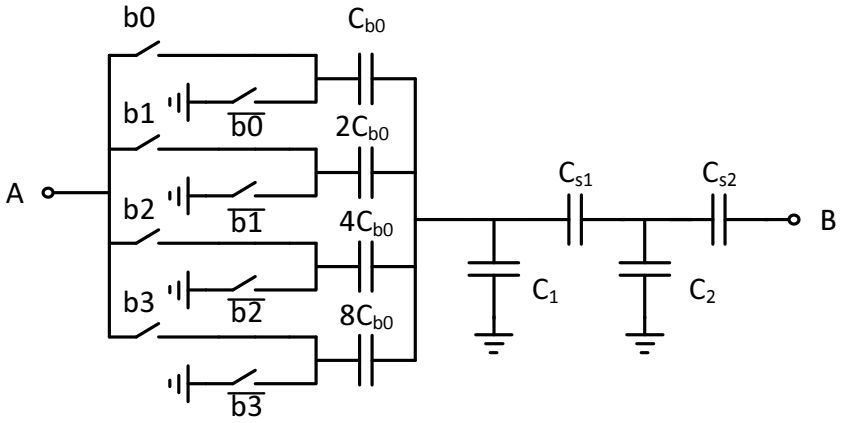

Fig. 2.22: Capacitance offset removal network

The effective capacitance between nodes A and B is [19].

$$C_{eq} = \frac{(b_0 C_{b0} + b_1 2C_{b0} + b_2 4C_{b0} + b_3 8C_{b0})}{(C_{b0} + 2C_{b0} + 4C_{b0} + 8C_{b0}) + C_1} \frac{C_{s1}}{C_{s1} + C_2} C_{s2}. \qquad (2.25)$$

Notice that of C_1, C_2, C_{s1}, and C_{s2}, the series capacitors are in the numerator of the equation, and the parallel capacitors C_1 and C_2 are in the denominator. It is this feature in particular that makes this network easy to implement. Since we would like C_{eq} to be small, this means that C_1 and C_2 should be large. So any parasitic capacitors do not appreciably change the effective capacitance of the network since they add to an already large C_1 and C_2. Additionally, any parasitic capacitors next to the control switches add to parasitics from the MEMS chip, which are also large.

This is more commonly used as it does not add significant power consumption, and is not too difficult to implement. A similar technique is used to remove the offset in this system, which has the same benefits of minimal power consumption and ease of use. This will be discussed along with the open loop structure implemented in Chapter 3.

Chapter 3

System Design and Simulations

This chapter will outline the design of the proposed MEMS interface circuit. First, the general structure of the front end will be discussed. Next, issues regarding distortion and noise will be presented. Next, the specifications will be described based on the target resolution. Finally, implementation details and simulations will be presented.

3.1 General Structure

The front end is a discrete time (DT) switched capacitor (SC) front end since the measurement of capacitors lends itself well to SC circuits. The circuit will be differential in order to take advantage of the natural benefits that come with differential circuits such as suppression of harmonics and common mode noise.

The power scalability will come from the amplifier in the 1st stage capacitance to voltage (C2V) conversion, as the front end of an analog circuit tends to consume the most power. When the full scale decreases by a factor of 2, to maintain the same SNR and input bandwidth, we can decrease the noise by a factor of 2 by increasing the sample-rate by a factor of 4 and averaging the 4 outputs together. Increasing the speed by 4x costs roughly 4x the power for the lower full-scale input range. Scalability for the change in power can be made very uniform by switching in a different number of amplifier slices in

parallel such that more slices are used when the closed loop amplifier is clocked at higher speeds.

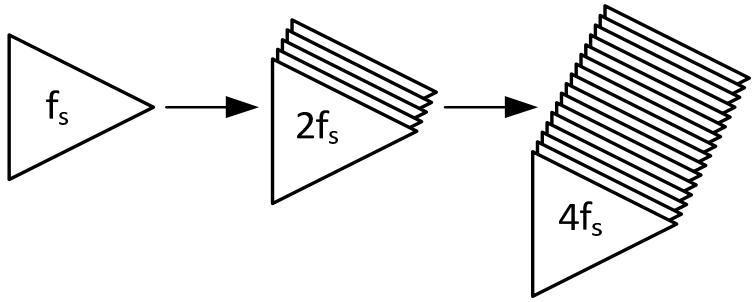

Fig. 3.1: Power Scaling of the main amplifier

To increase the overall system gain, a second static, non-scaled gain stage is added after with a gain of 4. The power consumption of the second stage is a single slice, which is small in comparison with the multiple slices in the first stage.

An offset network is placed in between these two stages. This offset network will be used to remove any signal that will potentially saturate the circuit without consuming any additional power.

Table 3.1 below shows the effective output clock speeds for a given full scale range. It also shows the number of integrations and the final effective output clock rates. The speeds and integrations are chosen based on noise considerations and will be shown in the next few sections.

Table 3.1: Main Stage Integrations, Slices, and Clock Rates

Full Scale (g)	1^{st} stage clock rate (f_s in kHz)	Number Slices N_s	Number Integrations N	Output Clock (f_s/N in kHz)
1	2000	16	16	125
2	500	4	8	61.25
4	125	1	4	31.25

Finally, output buffers are placed in order to ensure that the large capacitive pads, pcb lines, and the following integrated circuit can be driven stably and fast enough. The top level figure is shown below.

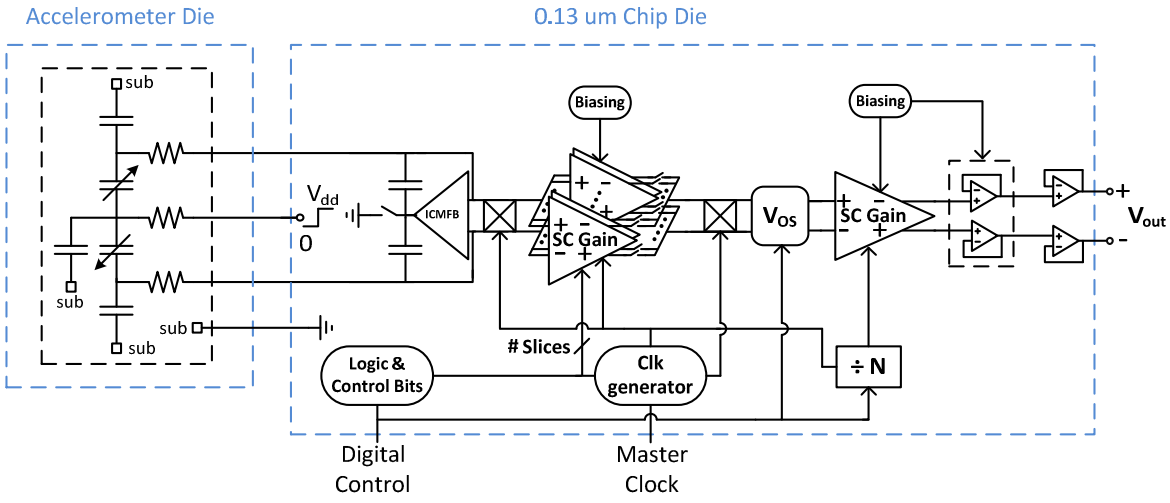

Fig. 3.2: Top Level Figure

3.2 1st Stage: C2V conversion

Generally, many DT SC accelerometer front ends use inverting type circuits [17][21][25][26]. Since the accelerometer capacitor is always the sense capacitor in SC DT front end circuits, this means that it is charged during the same phase as the integration (settling) phase of the opamp. For the opamp we generally want more time to settle, as this means the amplifier can be slower, requiring a lower transconductance and less power. For the accelerometer capacitors, however, we would like the opposite. This is because if the electrostatic force is applied for less time, there will be less physical movement resulting in less distortion.

3.2.1 1st Stage: Conversion Phase

If an inverting configuration is used, this places the opamp settling and the electrostatic force in the same phase. If we reverse this and use a non-inverting configuration,

however, then we see that both the distortion can be decreased and the opamp settling time can be increased by changing the duty cycle of the clock in the same direction. Fig. 3.3 shows the inverting version of the interface and Fig. 3.4 shows the non-inverting version.

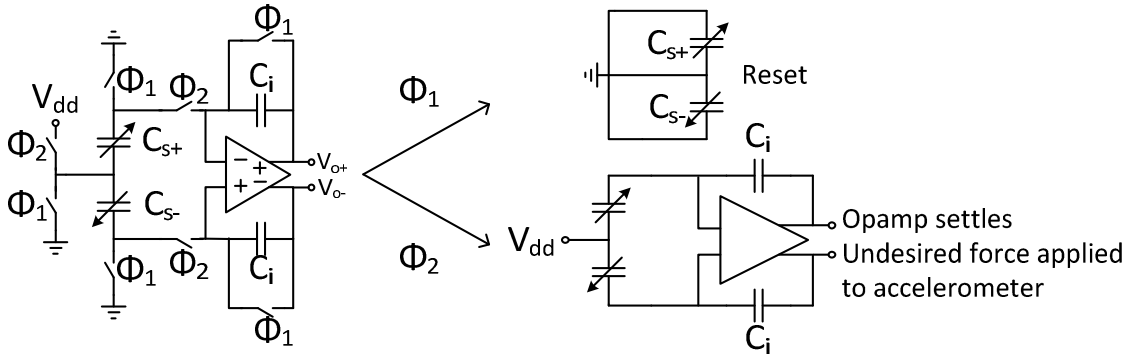

Fig. 3.3: Inverting Clock Phases in a Front End

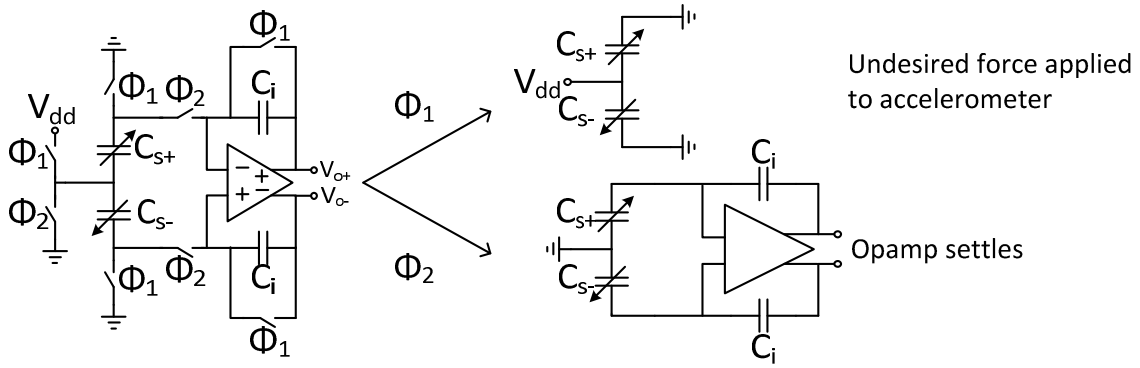

Fig. 3.4: Non-inverting Clock Phases in a Front End

3.2.2 1st Stage: Pseudo Differential Nature of Front End

Since this circuit is to be differential in nature, it is important to take a look at the very front end. If a configuration such as Fig. 2.19 is used, it is important to understand that this structure is in fact not truly differential. Applying a signal at the common middle node introduces a common mode input.

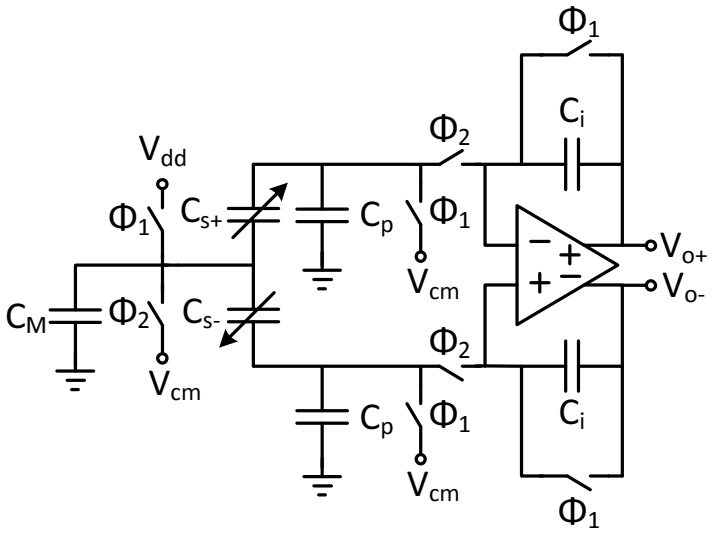

Fig. 3.5: Pseudo-Differential Front End Circuit

Similar to [21], the output for Fig. 3.5 after 1 period can be calculated to be

$$V_{out} = \left(V_{dd} - V_{cm}\right)\left[\frac{\Delta C_s}{C_i}\left(1 - \frac{C_s}{C_s + C_i + C_p}\right)\right]. \qquad (3.1)$$

Here, C_M is a parasitic capacitance due to the MEMS chip, and C_p is the parasitic capacitance due to the MEMS parasitic, the electrical parasitic, and the packaging parasitic. C_p tends to be rather large and dominated by the MEMS device. In this case it is much larger than 1pF.

The gain error is a function of the nominal sense capacitance, integration feedback capacitance, as well as the parasitic capacitance and can be significant. In addition to this, the use of a non inverting front end means that the common mode to the input of the amplifier will drop. Since the 1st stage amplifier has a finite common mode range over which it functions, the common mode here must be corrected in order for the stage to function at all.

In order to deal with this, an input common mode feedback (ICMFB) circuit is used to compensate for the CM drop. The feedback is applied through coupling capacitors to the input nodes of the opamp [21], which will ultimately add more noise to the circuit. However, the noise of the ICMFB itself is assumed negligible, since any

noise that is added through the coupling capacitors is common mode noise and the majority of this will be cancelled through the differential structure of the interface. Fig. 3.6 shows the addition of the ICMFB network:

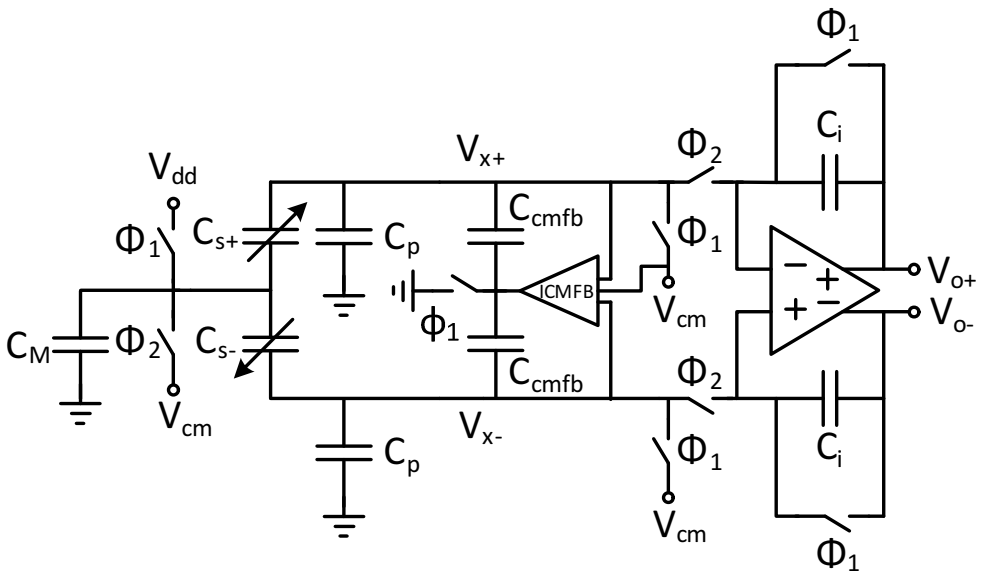

Fig. 3.6: Pseudo-Differential Front End with ICMFB Compensation

The addition of this network minimizes the gain error due to the common mode input, resulting in the equation

$$V_{out} = \left(V_{dd} - V_{cm}\right)\left[\frac{\Delta C_s}{C_i}\right]. \qquad (3.2)$$

3.2.3 1st Stage: Common-Mode Capacitor Sizes

The common mode voltage V_{cm} for the amplifier is chosen to be slightly below mid rail (500mV). This makes using PMOS inputs for the amplifier easier, which helps to reduce the flicker noise of the amplifier. The front end is chosen to switch from 0.5V to 2.5V. The reason for this will be made clear in the next section.

The sense capacitor value is dictated by the MEMS accelerometer properties and is close to 350fF. The parasitic capacitor C_p is close to 1.5pF. This includes the MEMS

parasitic capacitance, the pad capacitance between the two chip dies, and other electrical parasitics. In order to find the appropriate size of C_{cmfb} we need to find how much swing is required in order to bring the common mode voltage back to the desired voltage. The approximate common mode shift at V_{x+} and V_{x-} in Fig. 3.6 is given by

$$V_{xcm} = -(2.5-0.5)\frac{1}{2}\left[\left(\frac{C_{s+}}{C_{s+}+C_{cmfb}+C_p+C_i+C_{opin}}\right)+\left(\frac{C_{s-}}{C_{s-}+C_{cmfb}+C_p+C_i+C_{opin}}\right)\right].$$

$$\approx \frac{-2C_s}{C_s+C_{cmfb}+C_i+C_{opin}} \qquad (3.3)$$

C_{opin} is the input capacitance of the opamp and is assumed to be about 200fF. Note that this equation is negative because of the non-inverting phase of the front end. The ICMFB is able to swing the nodes V_{x+} and V_{x-} by

$$V_{shift\max} = (V_{\max}-V_{\min})\frac{C_{cmfb}}{C_{s-}+C_{cmfb}+C_p+C_i+C_{opin}}. \qquad (3.4)$$

V_{max} and V_{min} are the maximum and minimum voltages that the ICMFB network can apply. Equation (3.3) gives us the common mode at the nodes V_{x+} and V_{x-}. Equation (3.4) gives us the maximal swing of the ICMFB network. Using these, we find that for C_{cmfb}=400fF, we have sufficient common mode swing of about 375mV where less than 300mV is required, for V_{max}=3.15V and V_{min}=0.15V. So C_{cmfb}=400fF was chosen in order to satisfy the swing requirements.

3.2.4 1st Stage: 1st Stage Open and Closed Loop Gain

In a system with a closed loop amplifier, the error due to finite gain is a function of the open loop DC gain of the amplifier. The relative error is easily derived.

$$\frac{\frac{1}{\beta}-\frac{A}{1+A\beta}}{\frac{1}{\beta}} = \frac{\frac{1}{1+A\beta}}{\frac{1}{\beta}} = \frac{\beta}{\beta(1+A\beta)} = \frac{1}{1+A\beta} \approx \frac{1}{A\beta} < \frac{1}{2^n} \qquad (3.5)$$

$$\beta = \frac{C_i}{C_i + C_{cmfb} + C_p + C_s + C_{opin}} \quad (3.6)$$

The variable n in (3.5) is the number of bits of accuracy that we would like the amplifier to settle to. If we would like to design for 10 bits, to be conservative, n should be set to 11-12. Rearranging, we obtain

$$A > \frac{2^n}{\beta}. \quad (3.7)$$

For a small value of C_i, the required gain turns out to be extremely large. With C_i=200fF, β is well under 0.1 due to the large parasitic. This results in a required gain of 95dB for n=12, which is high. C_i is chosen as 800fF, resulting in a required gain of 84dB. More importantly, choosing a two stage amplifier also ensures that the output of the first stage is not saturated if a large offset exists near the accelerometer.

In addition to the gain stage, some of the oversampling rate is given up for a larger signal. This is done by simply resetting the closed loop amplifier after multiple integration cycles, effectively making the amplifier an integrator for N cycles. The effect of this on the overall signal to noise ratio (SNR) is minimal. Strictly oversampling gives approximately 3dB of SNR for every doubling of the system frequency [23]. Due to the system integrating values, this 3dB for every doubling in speed is lost. However, the integrating adds the signals together linearly while adding the squares of the uncorrelated noise voltages linearly. This means an increase in SNR of 3dB for every addition of 2 samples. This 3dB to SNR cancels with the -3dB from the reduction in speed, and so the overall SNR is not changed. So a full scale range of 4g requires half the integrations compared to a full scale range of 2g in order to reach the same output full scale, but the speed requirement is only one quarter. The number of integrations N can be set externally, and ranges from 2 to 16 in multiples of 2.

These choices make the overall closed loop gain of the first stage

$$A_{1CL} = N*(2.5-0.5)\frac{\Delta C_s}{C_i}$$
$$= 2N*\frac{\frac{\varepsilon_0 A}{x_0-\Delta x}-\frac{\varepsilon_0 A}{x_0+\Delta x}}{C_i}$$
$$= 2N*\frac{2\varepsilon_0 A\Delta x}{(x_0-\Delta x)(x_0+\Delta x)C_i}$$

$$\therefore A_{1CL} \approx \frac{4N\varepsilon_0 A\Delta x}{x_0^{\,2}C_i}, \qquad (3.8)$$

where Δx is the displacement of the mass, x_0 is the nominal accelerometer gap spacing, A is the effective area of the accelerometer capacitor, and C_i is the integration capacitor. Substituting these values we find a gain of approximately 180mV for a 1g input and 16 integrations. A plot of the front end with a real amplifier shows that this value is correct for an input of 1g. Note that when the full scale increases by 2 times, N is varied such that the final output full scale is always the same. Figure 3.6 below shows that the output voltage is close to the expected value predicted by the closed loop gain.

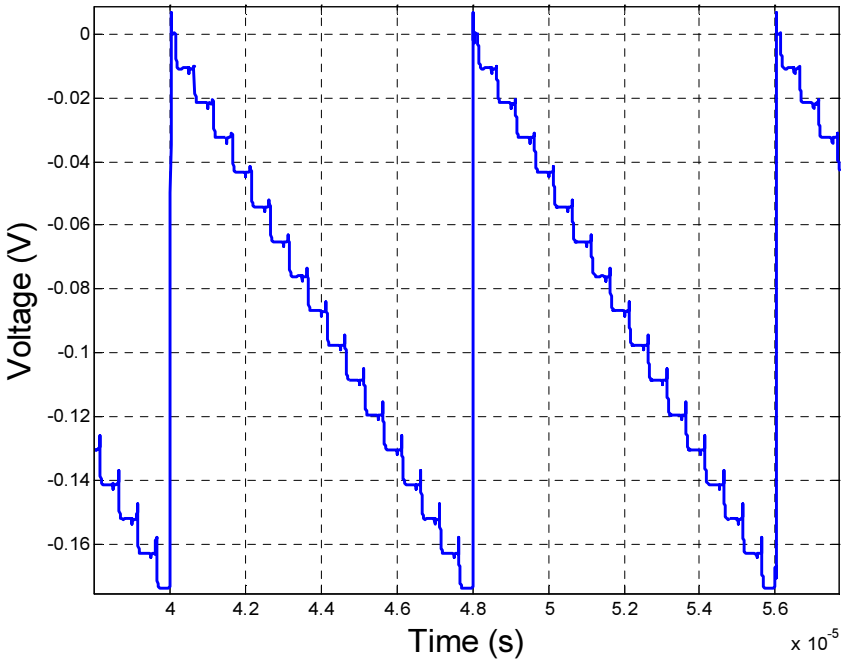

Fig. 3.7: Transient Waveform Of First Stage With Full Scale DC Input

As is typical in many front end circuits, more than one stage will be used for more gain. The second stage was selected as a standard closed loop SC gain stage with the duty cycle at 50%. Note that phases of the switches have to be changed slightly in order for the duty cycle to be varied between the two gain stages. As well, since there are N integrations in the first stage, this means that the clock rate of the second stage is reduced by N. The number N is varied with the full scale such that the full scale magnitude of the final output is always constant. So if N is a multiple of two, this makes the divided clocks easier to generate. For the largest case N=16, A_{1CL} is about 180mV. This means that the full scale of the output is

$$\therefore A_{CL} = A_{1CL}A_{2CL} \approx \frac{4N\varepsilon_0 A\Delta x}{x_0{}^2 C_i} * 4 = \frac{16N\varepsilon_0 A\Delta x}{x_{0^2} C_i}. \quad (3.9)$$

3.2.5 1st Stage: Front End Speed

The speed that the front end will run at is an important property needed before the amplifier can be designed. This is determined by estimating the thermal noise in the first stage capacitance to voltage (C2V) converter. The flicker noise is not as significant as a chopper amplifier will be used, upmodulating the signal before the majority of the flicker noise is introduced.

There are two major contributors to the thermal noise of the 1st stage. The first is the thermal noise due to the switches in the switched capacitor circuit. Including the ICMFB capacitors, the sampling capacitors, and the parasitic capacitors, the switch thermal noise is approximately [27]

$$V_{no} \approx 4x\sqrt{2\left(\frac{k_B T}{C_s} + \frac{k_B T C_i}{C_s{}^2} + \frac{k_B T C_P}{C_s{}^2} + \frac{k_B T C_{ICMFB}}{C_s{}^2}\right)} x \frac{C_s}{C_i}. \quad (3.10)$$

$$V_{noeff} = V_{no} / sqrt(OSR) \quad (3.11)$$

The second major contributor to the thermal noise is the opamp thermal noise. The input referred noise in an opamp is $16k_BTn_f/3g_m$ [23]. The transconductance of a single slice of the first stage is approximately 60uA/V. This means a total of 960uA/V for the full 16 slice amplifier. Assuming an n_f of 5, from [23] we have

$$V_{ni} \approx \sqrt{\frac{16k_BTn_f}{3g_m}\frac{1}{4\tau}}\sqrt{\frac{1}{OSR}}. \quad (3.12)$$

Here, τ is the time constant of the closed loop amplifier. We would like the total noise at the output to be less than 87.9 μV at the output. With a bandwidth of 100 Hz and an OSR of 10,000, we find a total of 58.6 μV output noise from the first stage, which is below the target 87.9 μV.

Specifications were chosen lower to be conservative and ensure that the noise level is low enough in simulation; Note that when testing the chip, this frequency can be scaled and lowered easily to raise the effective noise floor, but the frequency cannot be raised if the amplifiers cannot handle a high enough speed.

As the large majority of the 1/f noise is introduced by the amplifier, the first set of chopping switches is placed before the amplifier. In order to ensure that the 1/f noise is reduced enough, an autozeroing type of amplifier is also used in the first stage. Note that using this type of amplifier does not affect the closed loop gain of the first stage.

3.2.6 1st Stage: Full Front End Schematic

Based on the above information, a (pseudo) differential DT SC interface was chosen with input common mode feedback, autozeroing, chopping, and an altered 25% duty cycle during the integration phase. The circuit switches from the common mode voltage (0.5V) to 2.5V. The schematic is shown below.

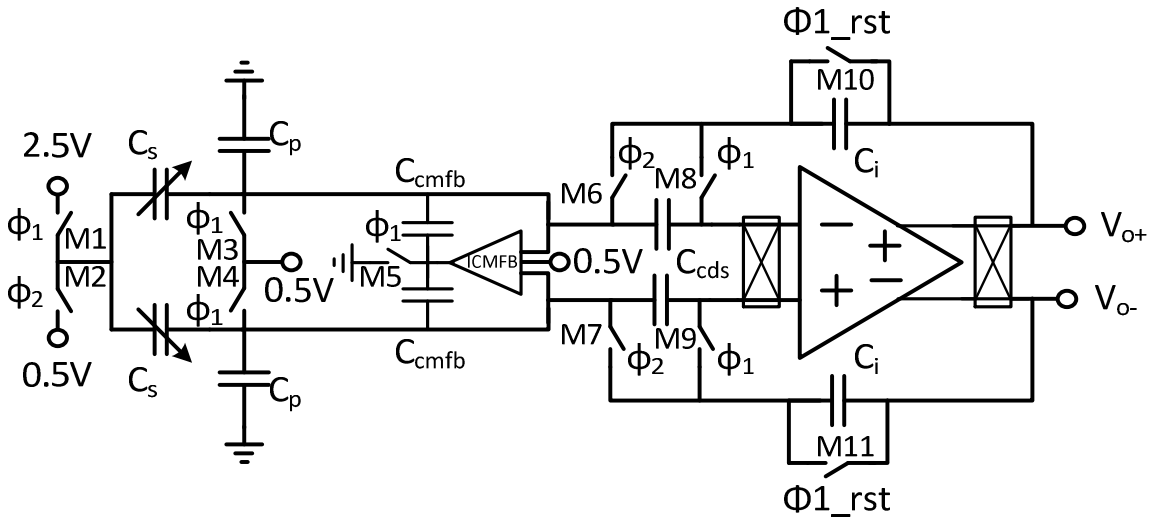

Fig. 3. 8: Full First Stage Gain Stage

Table 3.2: First Gain Stage Device Sizes

Device	Size (μm/μm)
M1 (Thick Oxide)	PMOS: 5x2/0.4
M2 (Thick Oxide)	NMOS: 1x4/0.4
M3, M4	NMOS: 2x2.5/0.12
M5	NMOS:4/0.4
M6,M7	NMOS: 2x2.5/0.12
M8,M9	NMOS: 2x2.5/0.12
M10,M11	NMOS: 2x2/0.4
Input chopper:	NMOS: 4u/0.12
Output Chopper (Thick Oxide)	NMOS: 4u/0.4u
C_{cds}	400fF
C_i	800fF
C_{cmfb}	400fF

The chopper circuit above is simply a set of 4 switches alternating the direction of the amplifier as shown in Fig. 3.9 below.

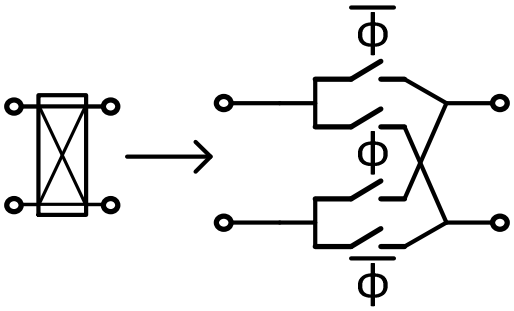

Fig. 3.9: Chopper Circuit

3.3 Mechanical Distortion: Undesired Force Feedback

This section concerns the model used to ensure that mechanical distortion was not too high. Simulations results that ensure that the target SNDR is not limited by mechanical distortion are also presented.

3.3.1 Model

As mentioned earlier, mechanical distortion due to the capacitor electrostatic forces can be a considerable issue in an open loop capacitive interface. This can be modelled as shown in Fig. 3.10.

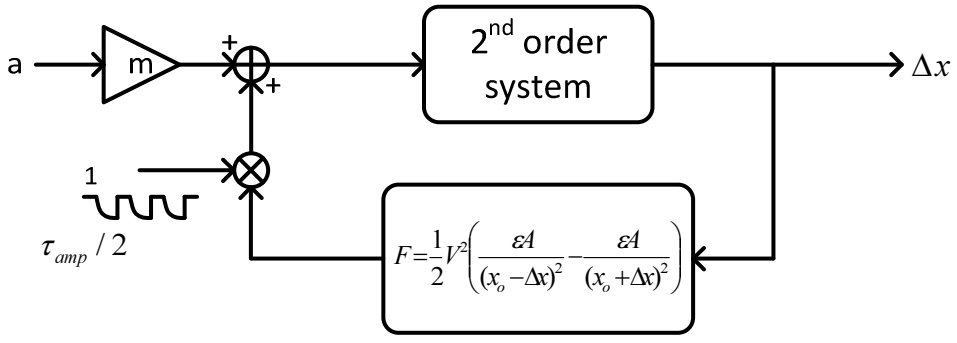

Fig. 3.10: Model for the Effect of The Undesired Electrostatic Force Feedback

In order to ensure that this distortion does not limit the target SNDR, a MATLAB model was built in order to determine what range of voltages are tolerable. The MATLAB model of Fig 3.10 above is shown in Fig. 3.11.

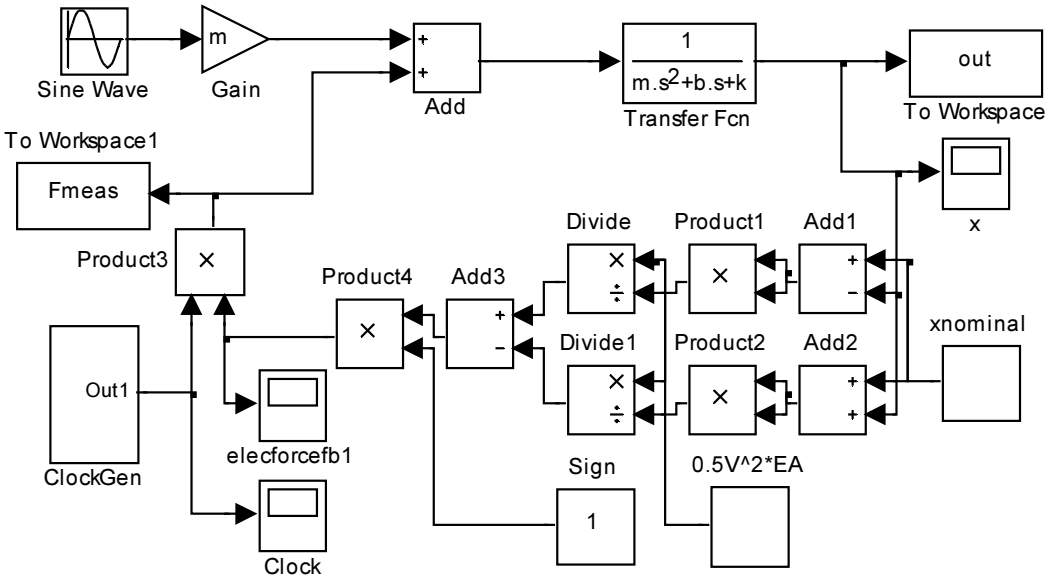

Fig. 3.11: Simulink Model for Electrostatic Force Feedback

Since the accelerometer capacitor will be attached to a front end with a closed loop opamp system, we will assume that there is a dominant pole in the settling behaviour of the amplifier. This means that we should expect exponential settling of the voltage across the accelerometer capacitors. As well, from (2.17), we know that the force applied on the MEMS accelerometer will be proportional to V^2.

$$V(t) = V_{init} e^{-\frac{t}{\tau_{CL}}}, \qquad (3.13)$$

where V_{init} is the initial voltage across the accelerometer capacitors and τ_{CL} is the effective closed loop time constant of the amplifier. Substituting (3.13) into (2.8),

$$F_{elec} = -\frac{1}{2} V^2 \frac{\varepsilon A}{(x_0 - x)^2} = -\frac{1}{2} \frac{{V_{init}}^2 \varepsilon A}{(x_0 - x)^2} e^{-\frac{t}{\tau_{CL}/2}}. \qquad (3.14)$$

$$\therefore \tau_{eff} = \tau_{CL} / 2 \qquad (3.15)$$

This means that the effective settling time constant of the electrostatic force will be *half* of the effective closed loop time constant of the amplifier network. This settling behaviour is assumed for the voltage across the capacitor in the model in Fig. 3.11.

The 'ClockGen' block outputs a square wave pulse with an exponentially decaying behaviour at half the time constant with a duty cycle D. The decay only occurs on the falling edge, however, as this is what the accelerometer will see. This signal is multiplied with the voltage applied on the accelerometer during the switched capacitor phase where charge is placed on the accelerometer capacitors. The sign in the feedback path is selected such that the direction of the electrostatic force is always towards the closest accelerometer plate, as the coulomb force between the charges on the accelerometer plates is always attractive.

3.3.2 Simulations

There is no noise added in the system (apart from the quantization noise in simulink) so we expect to see the signal, some harmonic content, and a very low noise floor. Since the accelerometer system is a 2^{nd} order lowpass, we also expect to see a drop of 40dB/decade in the frequency plot. Fig. 3.12 below shows an example with an input sinusoidal acceleration of 4g, a DC acceleration of 1g, duty cycle of 75, and SDR of 74dB.

A plot of multiple simulations shows how the signal to distortion (SDR) varies across different duty cycles in Fig 3.13. When the signal to distortion drops rapidly, this means the accelerometer is likely to be damaged from the electrostatic forces near this region. Notice how quickly this changes with voltage, since the force is proportional to the square of the voltage across the accelerometer V_{accel}^2. Recall that the pull in voltage is approximately 2.5V (DC). A higher voltage is possible since this is being switched temporarily for some duty cycle D.

Fig. 3.15 shows the SDR for varying DC input accelerations. Note here that the peak sinusoidal input acceleration plus the DC acceleration is always 4g. For instance the 1g case has a 3g sinusoidal input, and the 0.5g case has a 3.5g input. Since it was desired to keep this above 78dB, a duty cycle of 25% was selected, with a V_{accel} of 2V.

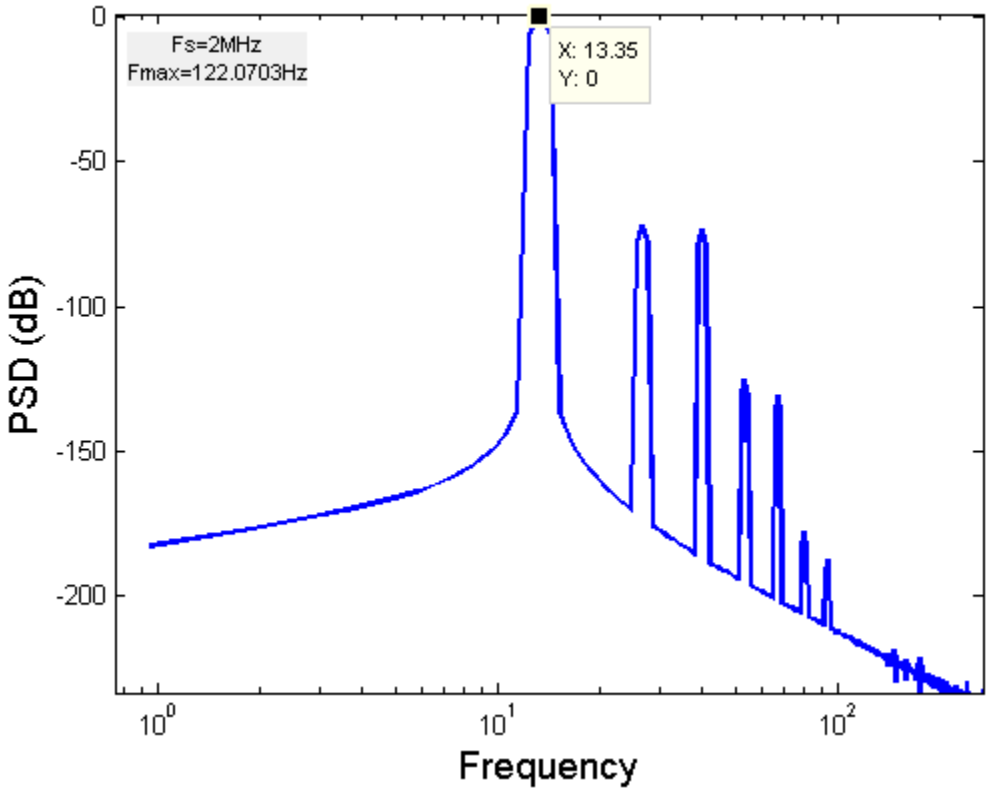

Fig. 3.12: Simulation for Signal to Distortion due to Undesired Force Feedback

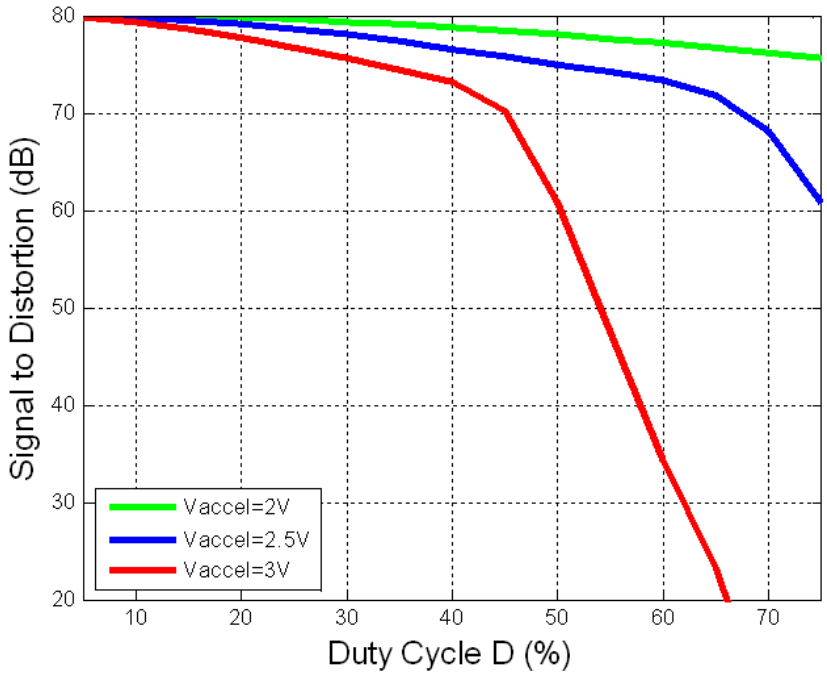

Fig. 3.13: Signal to Distortion across Vaccel with DC input=0g and sine input=4g

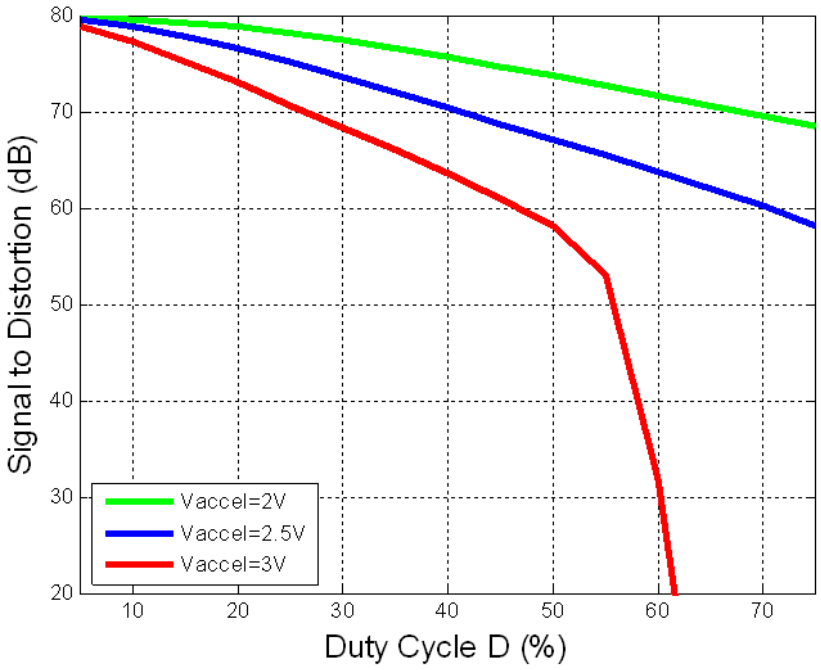

Fig. 3.14: Signal to Distortion across Vaccel with DCin=1g and sine input=3g

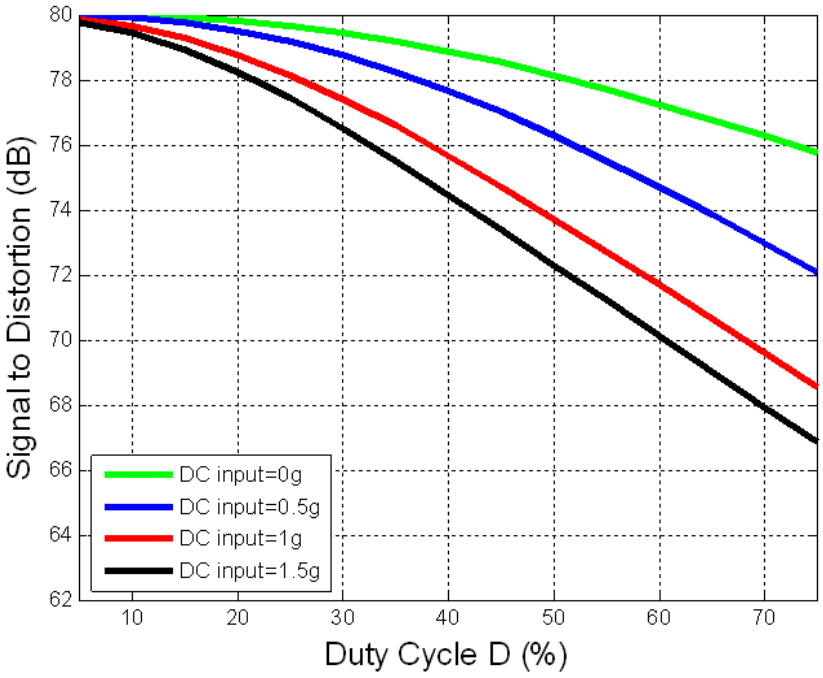

Fig. 3.15: Signal to Distortion across different DC input accelerations

3.4 Stage 1 Two Stage Amplifier Specifications

Section 3.1 showed that a minimum open loop DC gain of 84dB was required. The clock frequency was also derived based on the amount of thermal noise in the system. Also, section 3.2 determined that a duty cycle of 25% was required, meaning 75% of the clock period to allow the amplifier to settle. Due to the lack of offset removal in the first stage, a two stage amplifier was used as a precaution in order to ensure that the offset does not saturate the output. Assuming an extra 200mV of headroom after the first stage, this allows for nearly an extra 200/180=111% of offset removal relative to full scale.

These pieces of information and the capacitor values in the closed loop system enable us to calculate the required bandwidth. We can determine the effective closed loop time constant as follows: For a 2 stage amplifier, we have

$$A(s) \approx \frac{g_{m1}}{sC_C}. \qquad (3.16)$$

This equation assumes that a dominant pole exists. The closed loop transfer function is $\frac{A(s)}{1+A(s)\beta}$, and so the poles of the closed loop system are where

$$1+A(s)\beta=0. \quad (3.17)$$

$$\therefore \tau=\frac{C_C}{\beta g_m}=\frac{1}{\beta\omega_{unity}}, \quad (3.18)$$

where w_{unity} is the unity gain frequency of the amplifier. A first order system settles exponentially, and so to have n bits of settling accuracy, we must have

$$e^{-\frac{t}{\tau}}=\frac{1}{2^n}. \quad (3.19)$$

$$\therefore t=n\tau\ln 2=n\left(\frac{1}{\beta\omega_{unity}}\right)\ln 2. \quad (3.20)$$

With a duty cycle of D and clock period of fs, this means that we have

$$t=\frac{D}{f_s}. \quad (3.21)$$

Equating the settling times above, we have

$$\omega_{unity}=\frac{nf_s\ln 2}{\beta D}. \quad (3.22)$$

$$f_{unity}=\frac{nf_s\ln 2}{2\pi\beta D} \quad (3.23)$$

This is the unity gain frequency required in order to settle within n bits of accuracy given a duty cycle D and amplifier feedback factor β. Using β=0.25, n=12, fs=2MHz, and D=0.75, we see that a minimum unity gain frequency of 15 MHz is

required for the 16 slice amplifier. To be conservative, 30 MHz was used for the 16 slice amplifier.

The biasing for the single slice amplifier is shown in Fig 3.16 below. In order to actually switch on/off amplifier slices, the biasing nodes were taken advantage of and bias transistors were used to shut off current flow through the amplifier. In particular, nodes V_{bp} and $V_{cmfbbias}$ in Fig. 3.16 are disconnected from the amplifiers. Instead, the amplifiers have these nodes tied high to stop bias currents from flowing. All 16 amplifier slices use the same biasing network.

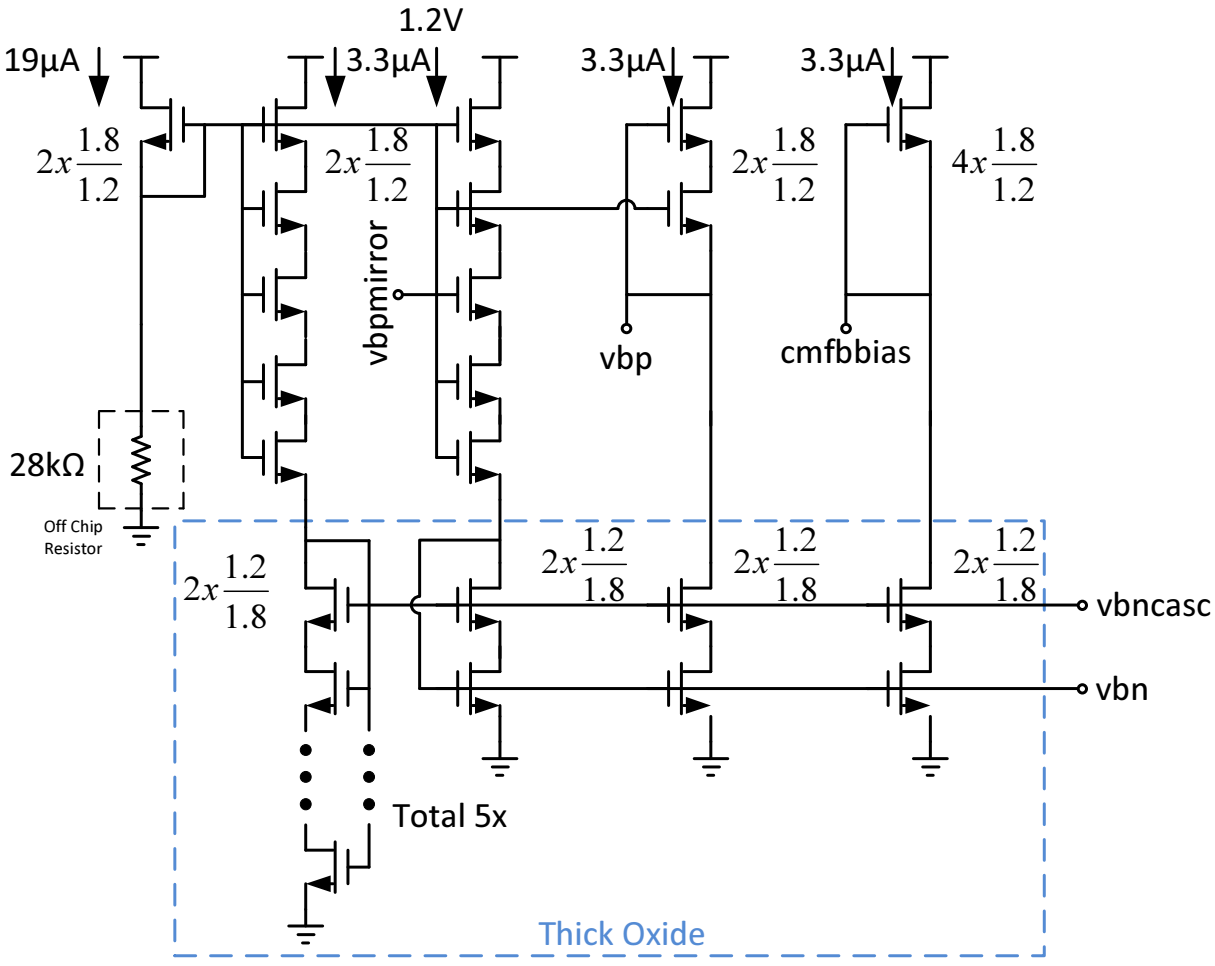

Fig. 3.16: Biasing for Amplifier

3.5 Input Common Mode Feedback (ICMFB) Network

The size of the coupling capacitor for the ICMFB network was derived above. The actual ICMFB is a fairly simple circuit. Due to the need for high swing, thick oxide transistors and a second output stage was used, as the reference voltage at the gate of the input limits the swing of the first stage output node. Fig. 3.17 below shows the circuit

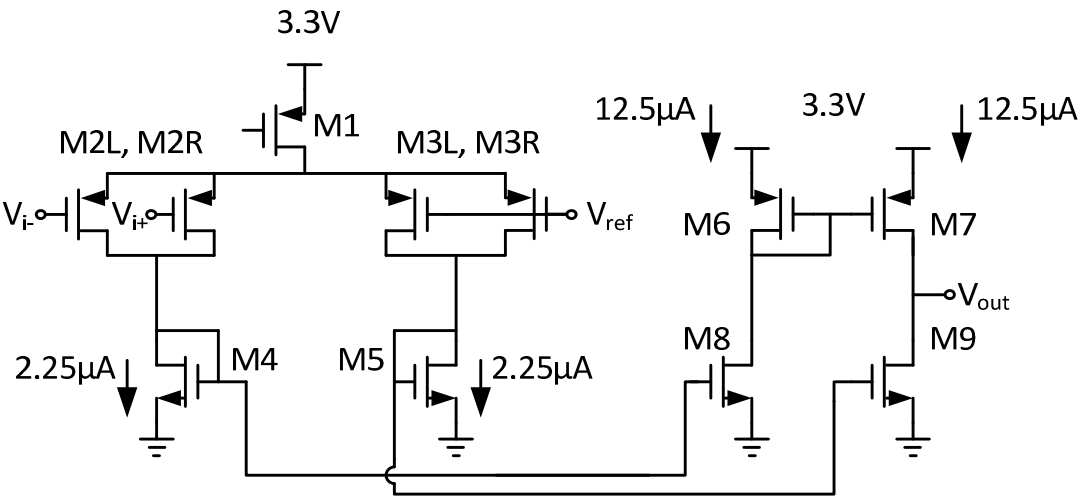

Fig. 3.17: ICMFB Circuit

Table 3.3: ICMFB Device Sizes

Transistor	Size (µm/µm)
M1	2/0.4
M2L,M2R,M3L,M3R	2x1.8/0.6
M4,M5	2x0.6/0.4
M6,M7	1/0.4
M8,M9	6x0.6/0.4

Stability is not a concern here, as the dominant node will obviously be the output due to the large capacitive loading on the node. The second stage is required as a large swing is needed. The reference voltage V_{ref} limits the swing to 500mV + V_t. The gain error expressed in (3.1) itself is not too large in magnitude, so suppressing this is not as critical. More importantly, the common mode at the input to the first stage amplifier

tends to become rather low, heavily reducing the amplifier gain as the bias points for the input pair are incorrect.

We would also like the ICMFB network to be fast enough to support the highest rates. A unity gain frequency above 15 MHz was chosen due to the bandwidth calculations shown above. The resulting circuit has 35dB of open loop gain and 28 MHz unity gain frequency. The bode plot is shown below.

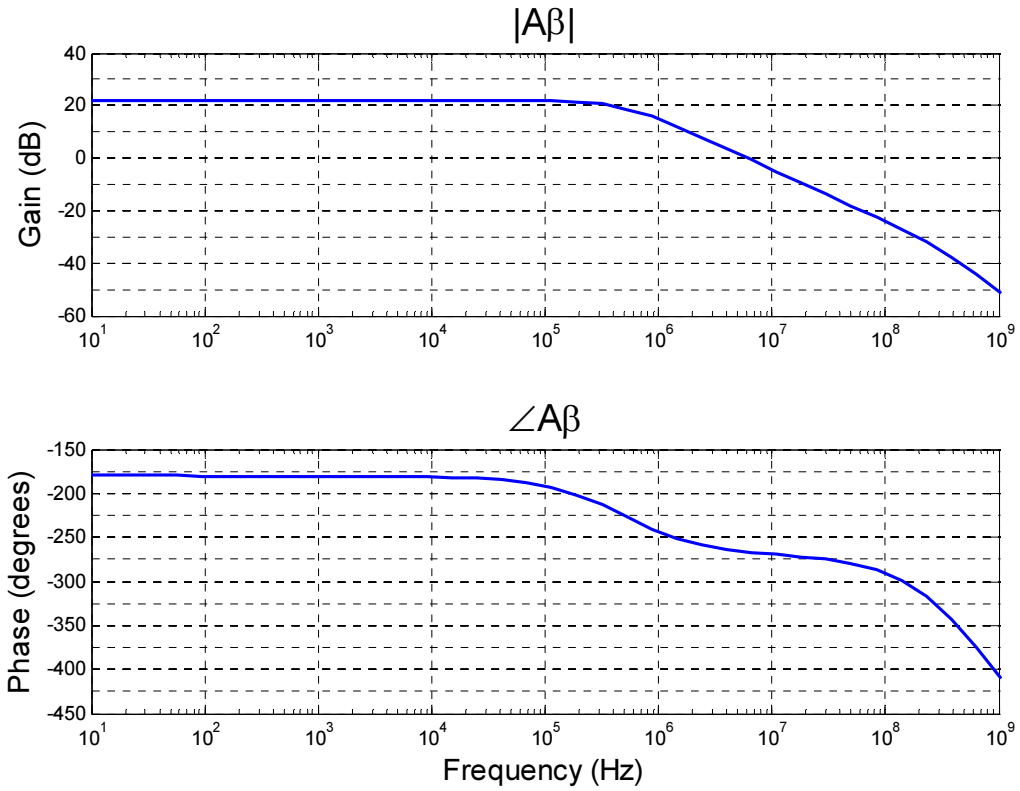

Fig. 3.18: ICMFB Bode Plot of Loop Gain

Fig. 3.19 is a transient simulation showing that the common mode does in fact settle close to the desired value. Fig. 3.20 below shows the same transient simulation with the ICMFB network removed; the common mode suffers quite a bit, and is brought well below the desired common mode, near the limits of the common mode capability of the amplifier.

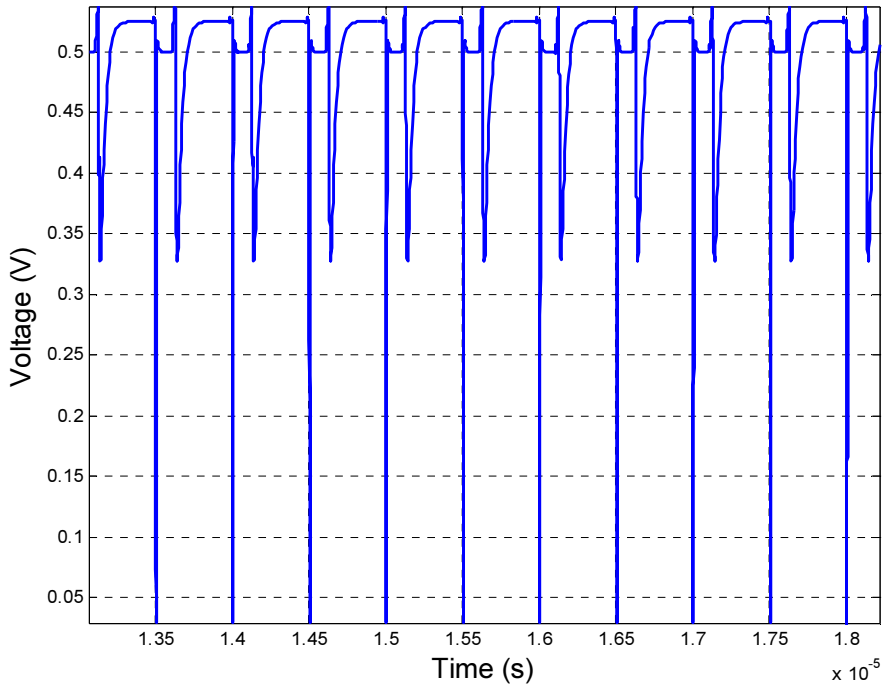

Fig. 3.19: Transient Simulation of Common Mode with ICMFB Circuit

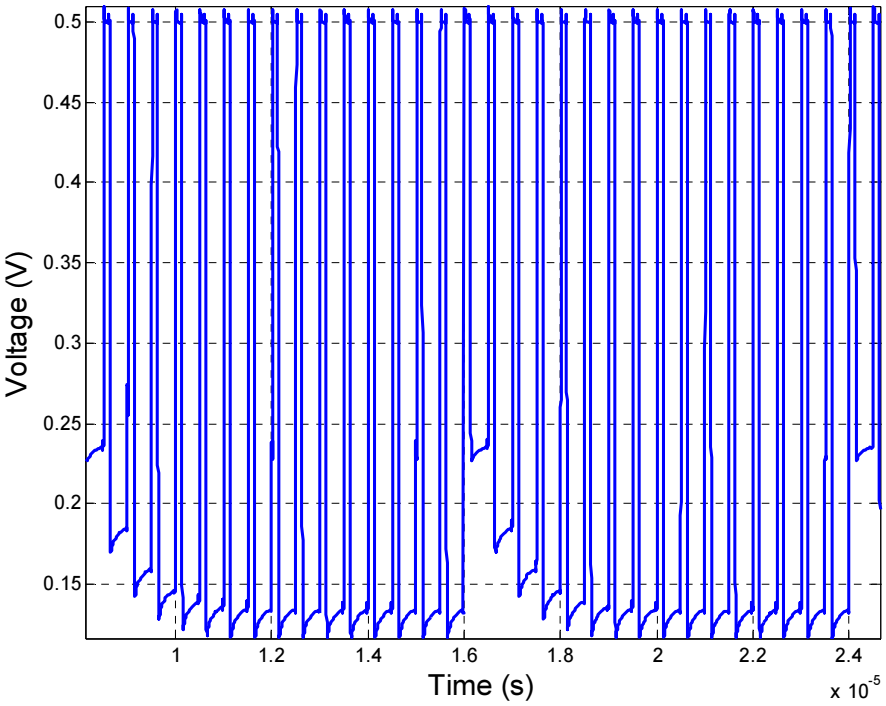

Fig. 3.20: Transient Simulation of Common Mode without ICMFB Circuit

3.6 Two Stage Self Common Mode Biased Amplifier

This section details the first stage amplifier used and its simulated characteristics. Next, the integration of all the amplifier slices is described, as well as the variation in the compensation that is required.

3.6.1 Common Mode Feedback

One challenge in the design of a fully differential 2 stage amplifier is the output common mode feedback. Often only one CMFB network is used; this can make it difficult to control the common mode of both the intermediary output as well as the second stage output, since we are attempting to control 2 nodes with only one voltage. One solution to this was proposed in [28]. [28] takes advantage of a negative impedance cross coupled MOSFET pair to decrease the common mode gain but maintain differential gain. This low common mode gain means that the CMFB loop can be used only around the outer stage; the low common mode impedance of the first stage means that a CMFB loop is not required to control the CM of the intermediary output. Placing the loop around the outer stage makes both stability and common mode control very easy.

A schematic of one amplifier slice, a variation to [28], is shown in Fig. 3.21. In this figure, Rc=40kΩ and Cc=2.8pF. This single amplifier slice draws a total of 22.7uA, has an open loop gain of 88.3 dB, and a unity gain frequency of 3.7MHz. More detail on the amplifier slices is provided in Table 3.5.

The differential output impedance of the first stage [28] is

$$R_{out} = R_u \,//\, R_d \tag{3.24}$$

$$R_u \approx g_{m4L} R_{o4L} R_{o3L} \tag{3.25}$$

$$\frac{1}{R_d} = g_{m6} - g_{m7} + \frac{g_{ds5L}\left(g_{ds1} + 2g_{ds6}\right)}{g_{ds5L} + g_{ds1} + 2g_{ds6} + g_{m5L}} \tag{3.26}$$

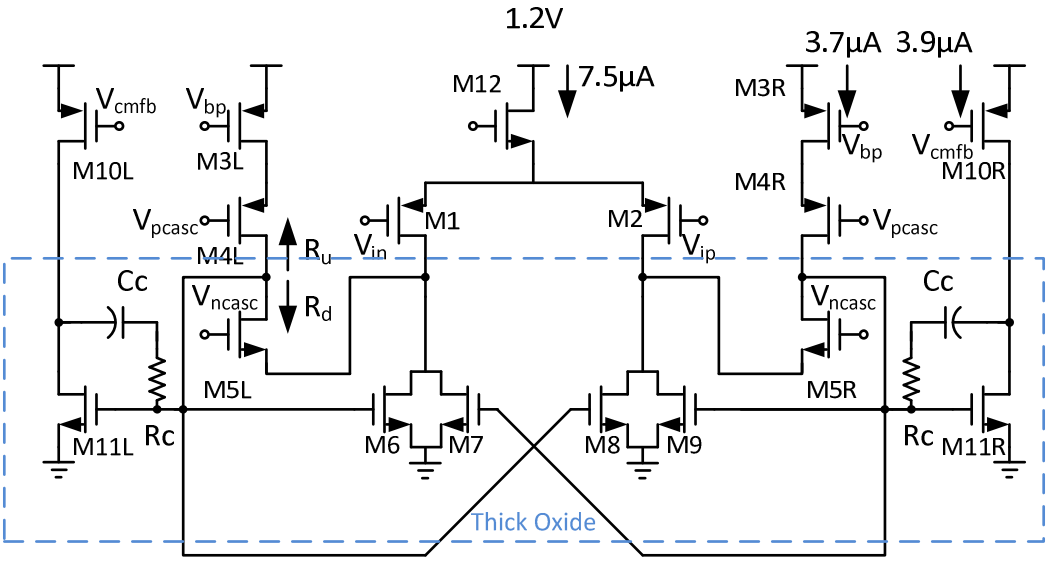

Fig. 3.21: Single Slice of Self Common Mode Biased Amplifier

Table 3.4: Device Sizes for Self Common Mode Biased Amplifier

Transistor	Size(µm/ µm)
M1-M2	4x1/0.5
M3L, M3R, M4L, M4R	2x1.8/1.2
M5L, M5R, M6-M9	2x1.2/1.8
M10L, M10R	4x1.8/0.6
M11L, M11R	2x1.2/1.8
M12	4x1.8/1.2

In (3.24) to (3.26), R_{oMx} is the output impedance of transistor M_x, g_{mx} is the transconductance of transistor M_x, and g_{dsx} is the conductance or inverse of the output impedance of transistor M_x. Note the sign of g_{m7}; as this is negative, and the sizes of M_6 and M_7 are identical, it helps to cancel out the effect of the diode connected g_{m6} transistor. As a result, the differential output impedance is similar to the case of a folded cascade amplifier.

Note that thick oxide devices have been used for the NMOS transistors. As M6-M9 sink the most current in the first stage, this helps to increase the output impedance, resulting in a higher gain.

The advantage of using M_6 and M_7 can be seen by looking at the common mode output impedance. This can be shown to be [28]:

$$R_{outcm} = R_{ucm} // R_{dcm} \tag{3.27}$$

$$R_{ucm} \approx g_{m4L} R_{o4L} R_{o3L} \tag{3.28}$$

$$\frac{1}{R_{dcm}} = g_{m6} + g_{m7} + \frac{g_{ds5L}\left(g_{ds1} + 2g_{ds6}\right)}{g_{ds5L} + g_{ds1} + 2g_{ds6} + g_{m5L}} \tag{3.29}$$

Notice that this time the sign on g_{m7} has inverted; this is because the cross coupled pair is seen similar to the diode connected pair in terms of common mode. In the case of the common mode, the conductance ($1/R_{dcm}$) dominates, making the impedance smaller. This is true in particular since transistors M6 and M7 sink the most current, making $g_{m6}+g_{m7}$ large. This in effect means that the common mode of the output of the first stage is low impedance and will not vary much, removing the need for common mode control for these output nodes. This is the reason that the CMFB loop only needs to be used on the outer loop. A bode plot of the loop gain of 16 slices of the amplifier is shown below:

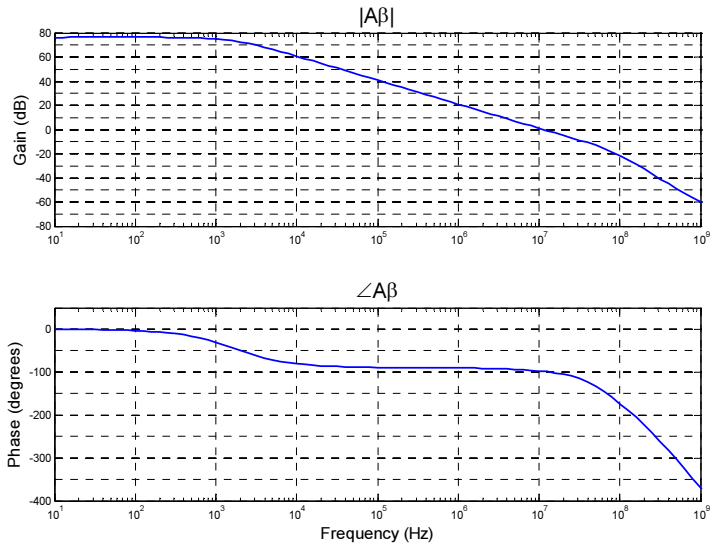

Fig. 3.22: Bode Plot for Full 16 Slices of the Amplifier

3.6.2 Output Common Mode Feedback

As mentioned in 3.4.1, the output common mode feedback only needs to work around the outer loop of the 2 stage amplifier. This makes stability a very simple issue since the output node is the dominant pole. A classic DT CMFB network is used [23] in order to push the common mode to its proper value. The biasing reference comes from the signal V_{cmbias} as shown in Fig. 3.16 above. Fig. 3.23 shows the CMFB network below.

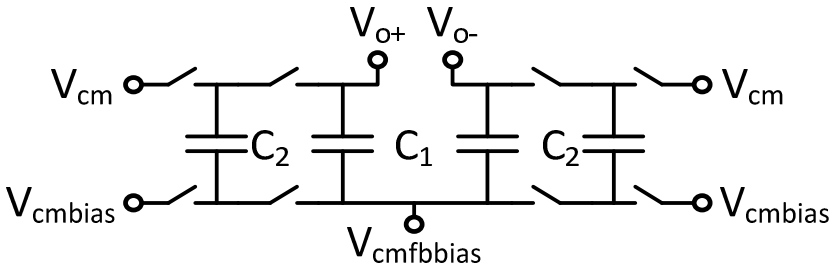

Fig. 3.23: Switched Capacitor DT Output CMFB Circuit

Here, V_{cm} is the desired common mode voltage, V_{cmbias} is the biasing reference, V_{o+} and V_{o-} are the amplifier outputs, and $V_{cmfbbias}$ is the common mode feedback voltage that returns to the amplifier bias transistors.

3.6.3 Replicated Amplifiers and Compensation

The single slice amplifier is re-used, and based on the full scale setting, a different number of amplifiers will be used. Replicated amplifiers are placed in parallel depending on the full scale setting. Switches are placed between amplifier slice outputs.

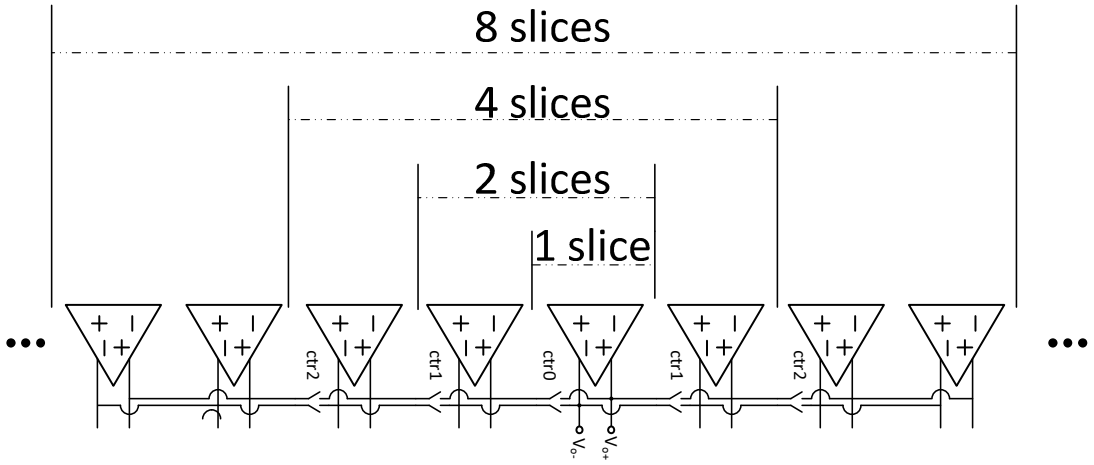

Fig. 3.24: Switches between Replicated Amplifier Slices

Stepping in to the actual two stage amplifier, we see the following:

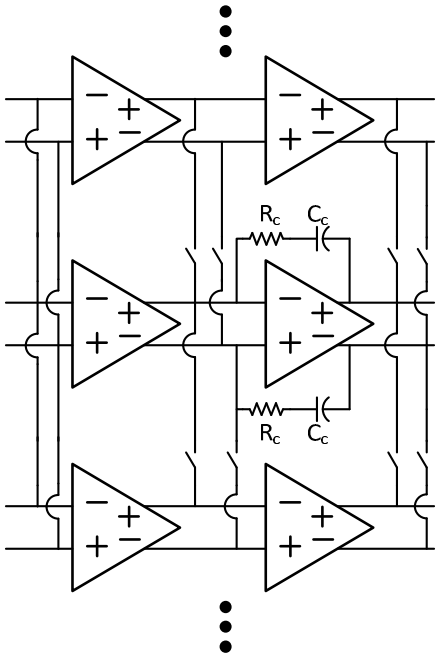

Fig. 3.25: Compensation in the Two Stage Amplifier Slices

Placing N amplifiers in parallel will directly multiply the effective transconductance of the amplifier by N. In order to ensure that the amplifiers maintain stability, scaling of the compensation resistor R_c is used. The 2 most dominant poles and the compensation zero can be found to be [23]

$$\omega_{p1} \approx \frac{1}{g_{m11} R_{out1} R_{out2} C_C}, \quad (3.30)$$

$$\omega_{p2} \approx \frac{g_{m11}}{C_{load}}, \quad (3.31)$$

$$\omega_z = \frac{1}{\left(1/g_{m11} - R_c \right) C_c}, \quad (3.32)$$

where M_{11} is the second stage common source transistor, R_{out1} is the output impedance of the first stage, and R_{out2} is the output impedance of the second stage.

Notice that in (3.30), if N slices are placed in parallel, the effective transconductance will increase by N times, but both the output impedances will decrease by N times since each stage is placed in parallel. This means that the location of the dominant pole w_{p1} will increase by N times. Similarly, in (3.31), since the effective transconductance will increase by N times, the second pole will also increase by N times. Finally, the zero in (3.32) shows that if we decrease the compensation resistor R_c by N times, we will arrive at the same result since $1/g_{m11}$ will increase by N times The end result is that all the major poles and zeroes will shift up by N times, resulting in similar frequency response but at higher frequencies. Table 3.5 summarizes the number of slices versus clock frequency, input full scale, and compensation values.

Table 3.5: Compensation and Integration Values at Different Full Scale Inputs

# Slices	Clock Freq. (kHz)	Full Scale (g)	Rc (kΩ)	Cc (pF)	Integrations
1	125	1	2.5	3.2	16
2	250	$\sqrt{2}$	5	3.2	N/A
4	500	2	10	3.2	8
8	1000	$2\sqrt{2}$	20	3.2	N/A
16	2000	4	40	3.2	4

The AC response parameters are shown over a different number of slices in Table 3.6 below.

Table 3.6: AC Amplifier Characteristics Versus Number of Amplifier Slices

# Slices	Open Loop Gain (dB)	Unity Gain Frequency (MHz)	1^{st} stage Power μA(μW)	Phase Margin (degrees)
1	88.87	3.768	23.01 (27.2)	96.14
2	88.9	7.64	45.5 (54.6)	95.65
4	88.91	14.79	90.67 (108.8)	93.93
8	88.91	27.18	181.4 (217.8)	90.81
16	88.91	45.23	362.3 (434.76)	84.17

Notice how cleanly the power scales, since we are simply switching in opamp slices. The variation in the phase margin is due to the increased capacitive loading at the input transistors of the amplifier, causing the second pole to move lower in frequency.

3.6.4 Distortion

After running some simulations on the distortion in the first stage, it was found that the distortion increases as the number of amplifier slices increases. The worst case distortion is with the 16 slice amplifier, at a speed of 2 MHz with 55.1dB signal to distortion. This distortion is actually due to the presence of the ICMFB network; when the input common mode is corrected, since the accelerometer capacitors are slightly different in size, this causes a slightly different distribution of the charges due to the ICMFB. This distortion tends to worsen with the number of slices of the amplifier due to the variation in the input capacitance as more slices are switched on. Despite this distortion, all signal to distortion values are within 9 bits.

3.7 Offset Network

Since it is common to use more than one gain stages in accelerometer front ends, offset is removed after the first gain stage is applied. In doing so, the offset has been converted to voltage domain, while no significant power consumption is added.

For offset removal, placing the network further after some signal amplification allows us to use a simple offset network as shown in Fig. 3.26 below. With this simplified network, we are able to attain an input referred offset of 0.4fF, which is about 10% of the full scale. This is sufficient in order to ensure that minimal headroom is wasted, and that the offset does not saturate the output. The network also has inherent sign control by using vdd and ground as input signals. Power consumption is very small since the power is simply CV^2f for the effective capacitance C of the offset network, but the frequency of operation f is low and in the kHz range.

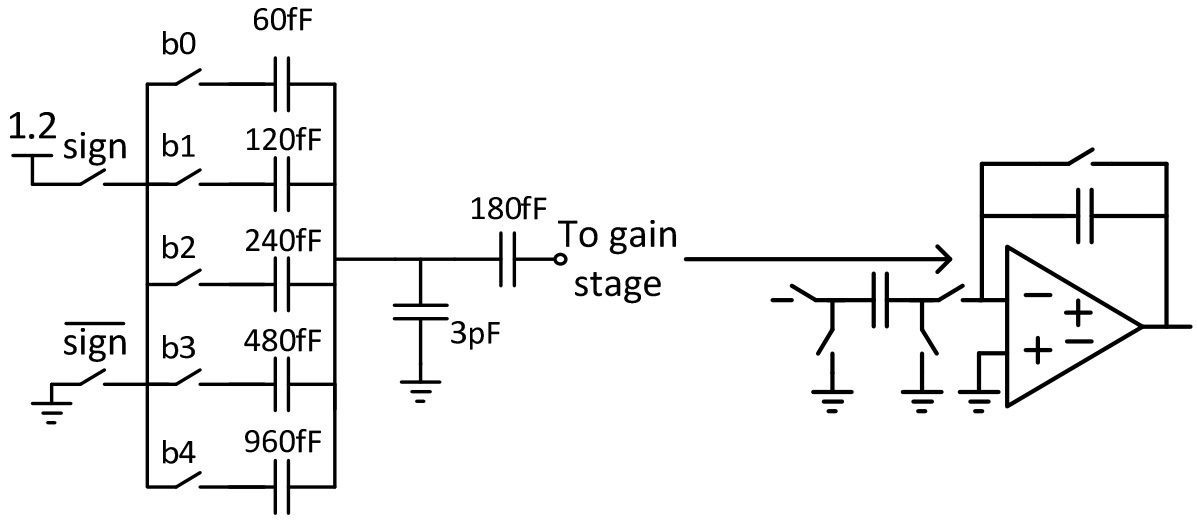

Fig. 3.26: Offset Removal Network

Note that switches to ground on the left of the digitally controlled capacitor were omitted; although this squeezes the range at the upper end of offset that can be applied, it was found to be sufficient so these were removed for simplicity. In addition to this offset, there was also extra headroom to ensure that the amplifiers did not saturate. Table 3.7 shows the output offset voltage with respect to the control bits.

Table 3.7: Offset Removal Over Different Control Settings

Control Bit Setting (Cos4:Cos1)	Output Offset With Sign=0 (mV)	Input Referred Offset (fF)	Output Offset With Sign=1 (mV)	Input Referred Offset (fF)
0001	66.76	0.41	-66.37	0.41
0010	192.5	1.2	-192.1	1.2
0011	309.7	1.93	-309.2	1.93
0100	419.3	2.62	-418.8	2.62
0101	521.3	3.25	-520.8	3.25
0110	617.7	3.85	-617.2	3.85
0111	793.2	4.95	-792.6	4.94
1000	872.2	5.44	-871.6	5.44
1001	948.3	5.92	-947.7	5.91
1010	1.02	6.36	-1.019	6.36
1011	1.088	6.79	-1.087	6.78
1100	1.152	7.19	-1.151	7.18
1101	1.214	7.57	-1.213	7.57
1110	1.272	7.93	-1.271	7.93
1111	1.328	8.28	-1.327	8.28

3.8 Stage-2 Amplifier

The 2^{nd} stage amplifier is equivalent to a single slice of the 1^{st} stage amplifier. Note that it is also possible to provide power scaling on this amplifier, but since the power of a single slice is quite small, only 1 unscaled slice was used. The output loading is significantly smaller, as this is after the amplification of the 1^{st} gain stage. As a result, the compensation capacitance C_c is smaller, as well as the compensation resistor R_c. A bode plot shows the frequency response below with a DC gain of 86.08dB, a unity gain frequency of 5.226MHz, and a phase margin of 87.09 degrees.

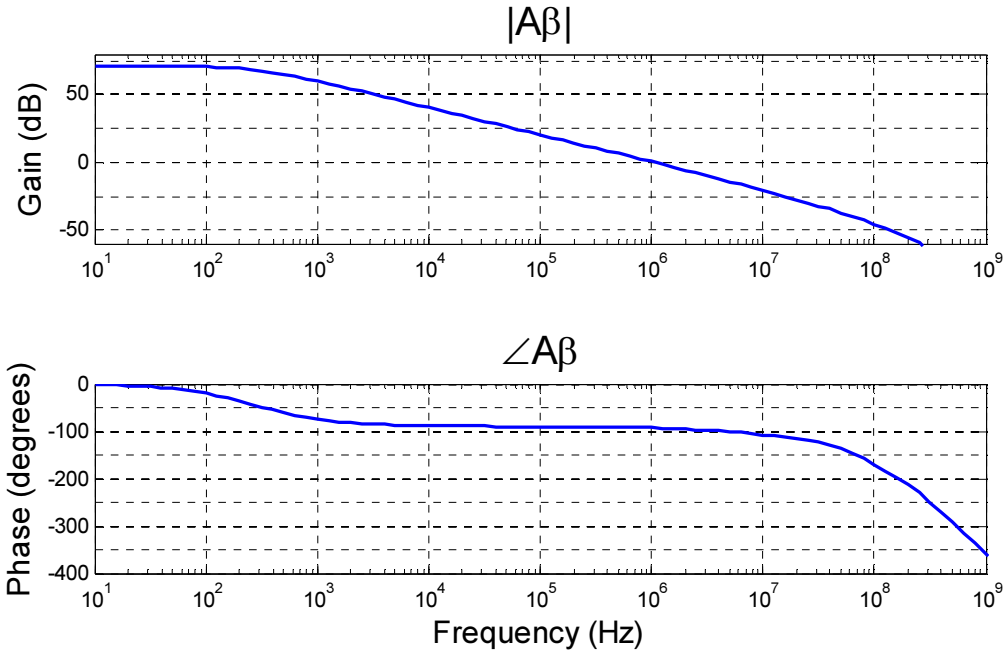

Fig. 3.27: 2nd Stage Amplifier Bode Plot

3.9 Output Buffers

In order to ensure that the 0.13µm chip could support the output capacitance load, 2 single ended buffers were used on each output line. The buffer has 10.28MHz unity gain frequency, 76.9dB DC gain, and 86.46 degrees of phase margin. Less gain was required since the feedback factor is simply 1, reducing the gain error 1/Aβ.

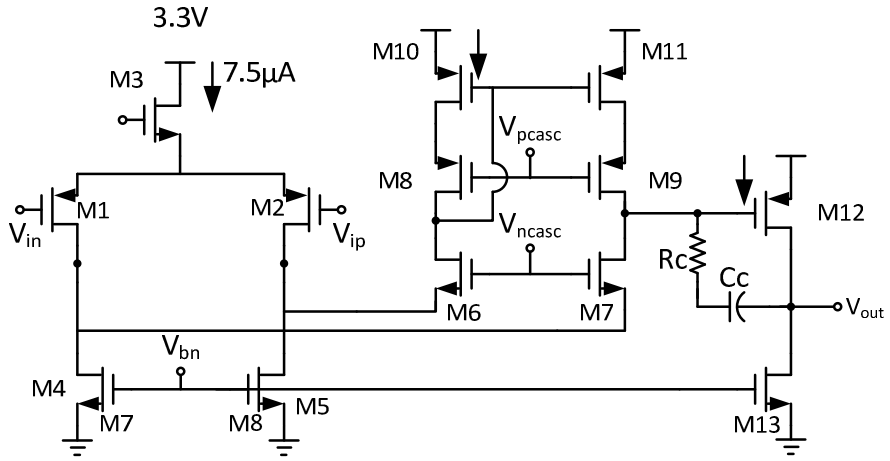

Fig. 3.28: Output Buffer Schematic

Table 3.8: Device Sizes for Output Buffer

Transistor/Part	Size (μm/μm)
M1,M2	28x2/0.4
M3	12x2/0.4
M4-M7	16x2/0.4
M8-M12	20x2/0.4
M13	8x2/0.4
R_c	3.4k
C_c	8pF

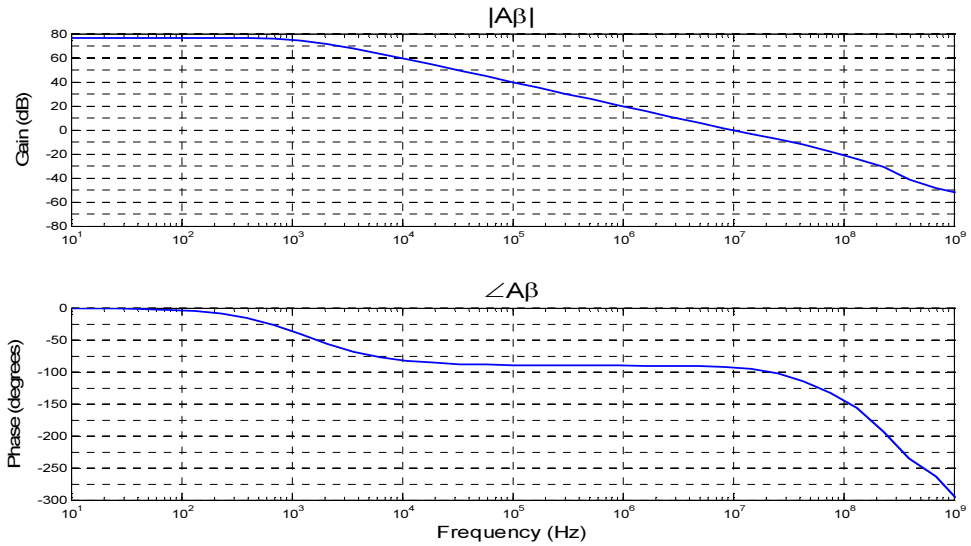

Fig. 3.29: Bode Plot of Loop Gain for Output Buffer

3.9.1 Output Loading

Since the output load capacitance may vary depending on the chip connected at the output and the PCB trace length, the output buffer is able to handle different output load capacitances. The DC gain of the amplifier is 76.89 dB. With a 1pF, 4pF, and 8pF load, the unity gain frequencies are 10.85MHz, 8.99MHz, and 7.39MHz, respectively. With the same 1p, 4p, and 8p loads, the phase margins are 95.65, 73.13, and 57.81 degrees, respectively.

3.10 Clocking and Digital Control

The clock generator was created by making use of a standard two phase non overlapping clock generator shown in Fig. 3.30.

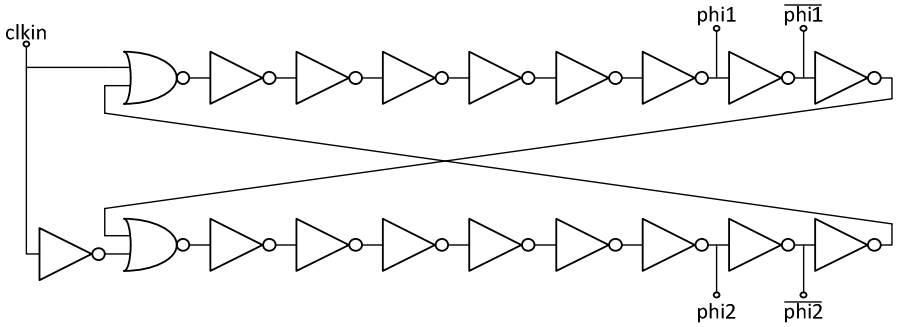

Fig. 3.30: Simplified Non-Overlapping Clock Generator

These clocks were the major building blocks in creating all the other thick oxide and delayed versions of the clocks. Nonoverlapping and digital control of the clocks was guaranteed using a long nonoverlap time with current starved inverters as well as digital logic control. The details will not be discussed here.

The digital control was done via parallel flip flops. These flip flops are latched depending on the value of the decoded signal select and a digital input. By doing this, any individual bit can be changed without the need to write every single control bit in sequence, as would be required with a shift register. A picture of the circuit is shown below in Fig. 3.31.

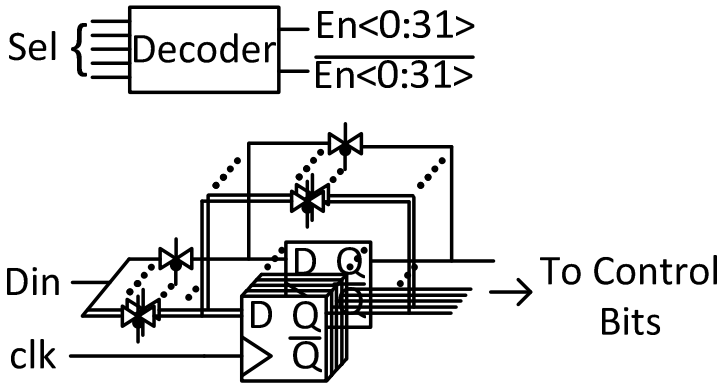

Fig. 3.31: Digital Control Signal Circuitry

Chapter 4

Measurement Results

This section concerns the measurement results of the 0.13um chip that was created. Section 1 shows the chip and the major considerations of the design of the PCB. Section 2 goes through the test setup. Finally, the last section goes through the results.

4.1 Chip and PCB

This section will briefly describe the chip, the chip packaging, and the pinout. A block diagram of the PCB will also be presented.

4.1.1 Chip and Chip Packaging

The chip and chip pad frame are shown below in Fig. 4.1. A list of the signals is shown in Table 4.1. The 0.13um chip and the MEMS die were combined in a CQFP 44 pin package, thus avoiding large parasitic capacitances from pads and PCB parasitics. The dies were connected together and to the package through bond wires. Fig. 4.2 shows a picture of an open CQFP package.

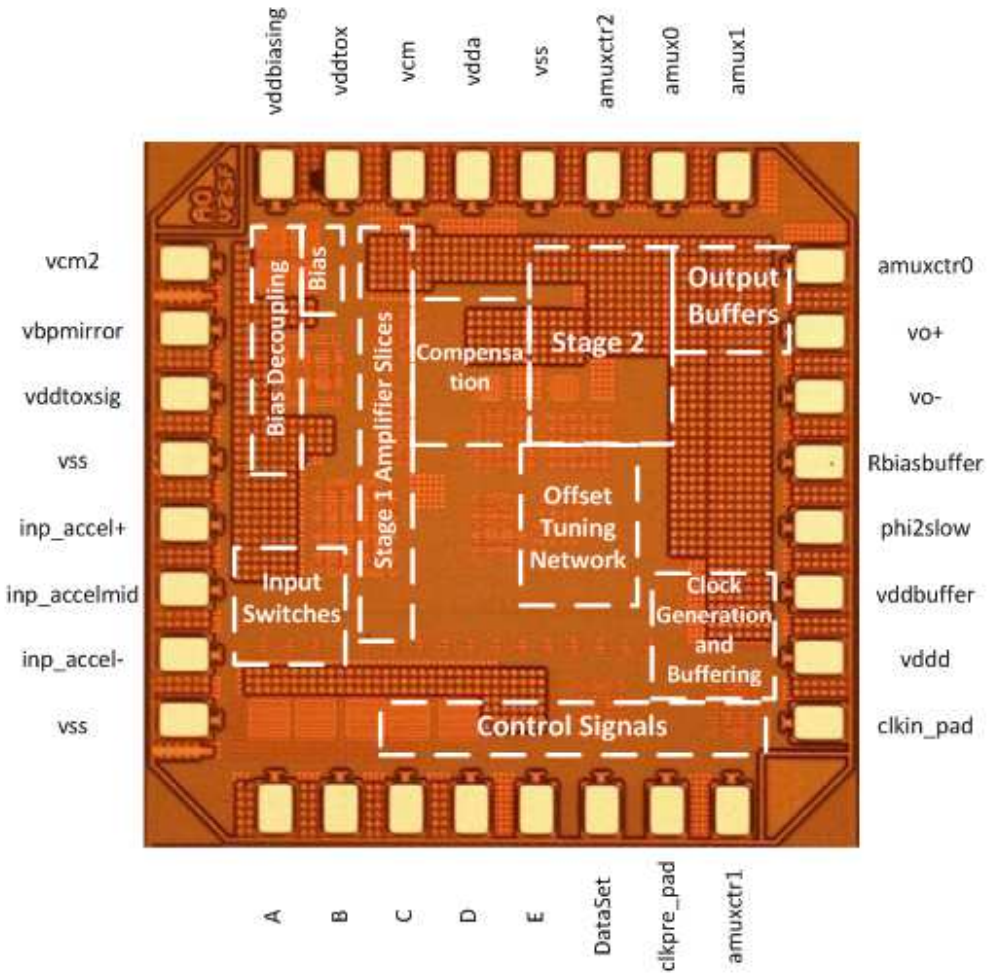

Fig. 4.1: 0.13μm Chip Die Photo

Table 4.1: Signal list for 0.13 μm Chip

Signal	Description
A-E, DataSet	Control bit signals
clkpre_pad	Clocking for control signals
vdda, vddbiasing, vddtox, vddbuffer, vddd	Supply voltages and grounds
clkin_pad	Input clock
amuxctr[2:0]	Analog mux control signals
amux1, amux0	Analog MUX output
Rbiasbuffer, vbpmirror	Biasing nodes for external current source
vo+, vo-	Switched capacitor (buffered) analog output
inp_accel+, inp_accelmid, inp_accel-	Accelerometer input connections

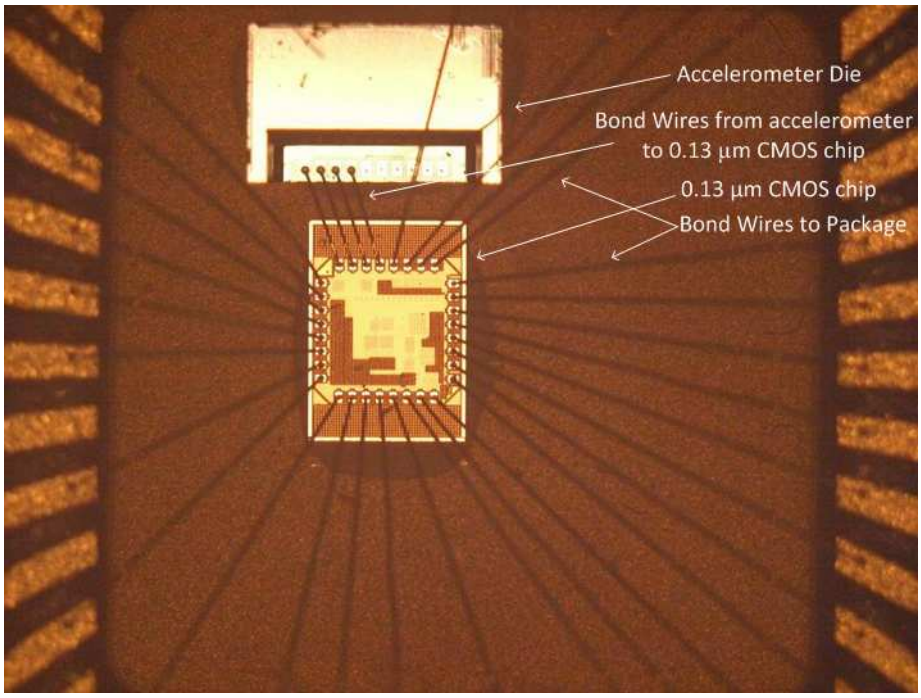

Fig. 4.2: Connections between MEMS Accelerometer, Chip Die, and Package

4.1.2: PCB

In order to ensure a constant load, output buffers were placed at the analog output of the chip. These outputs are connected to an ADC, which is digitally controlled by and outputs to a National Instruments NI6534 test card.

Potentiometers and various regulators are used in order to ensure tunability for bias voltages and voltage supplies for the chip. A block diagram of the PCB schematic is shown in Fig. 4.3, while the PCB layout is shown below in Fig. 4.4.

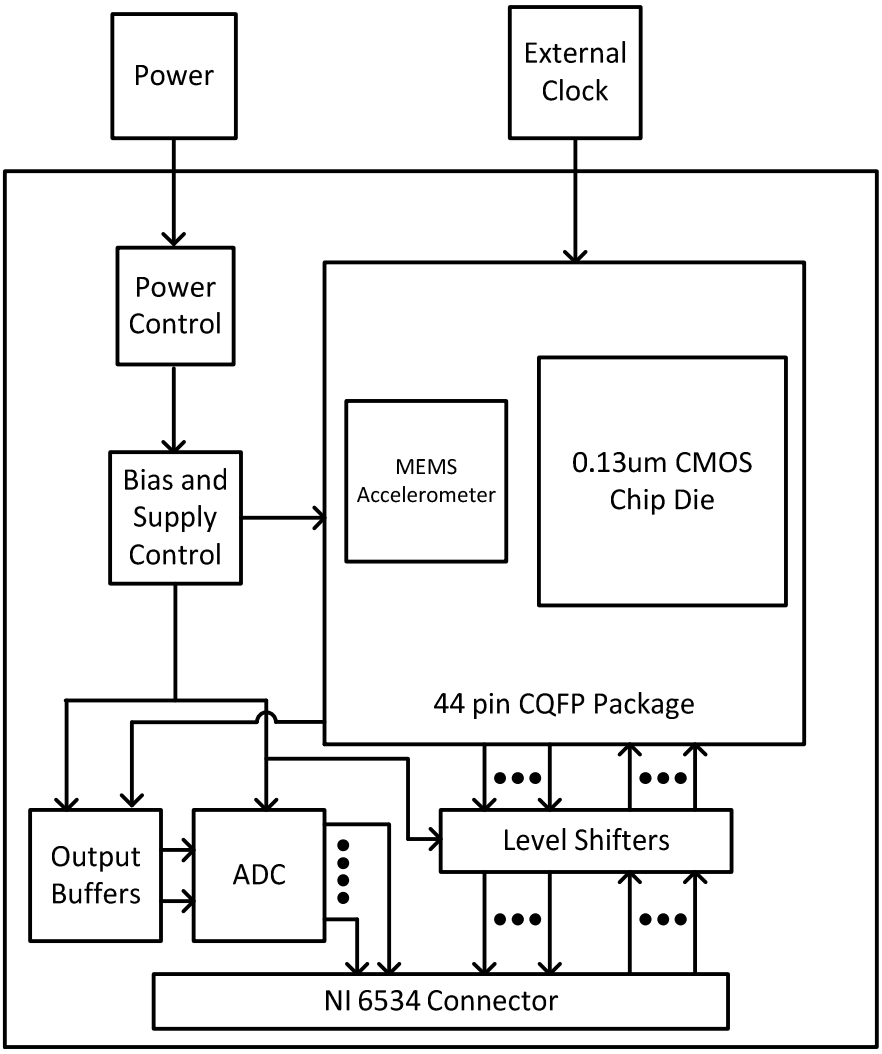

Fig. 4.3: PCB Block Diagram

4.2 Test Setup

As the NI 6534 card had a problem with acquiring data, a real time sampling oscilloscope was used to capture data, while the NI 6534 was used to change control bits on the chip. A real time sampling scope was used to capture the analog data. The test setup is shown in Fig. 4.5.

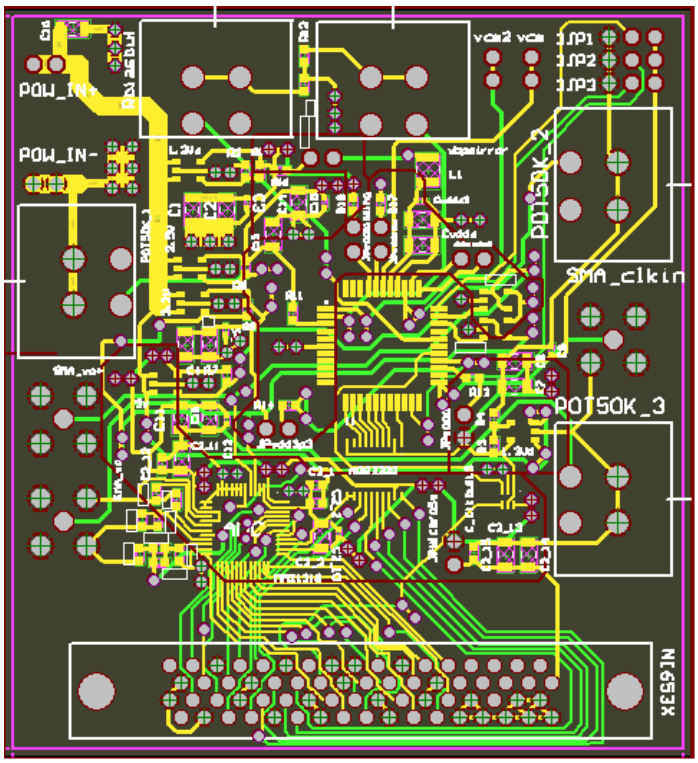

Fig. 4.4: PCB Board Layout

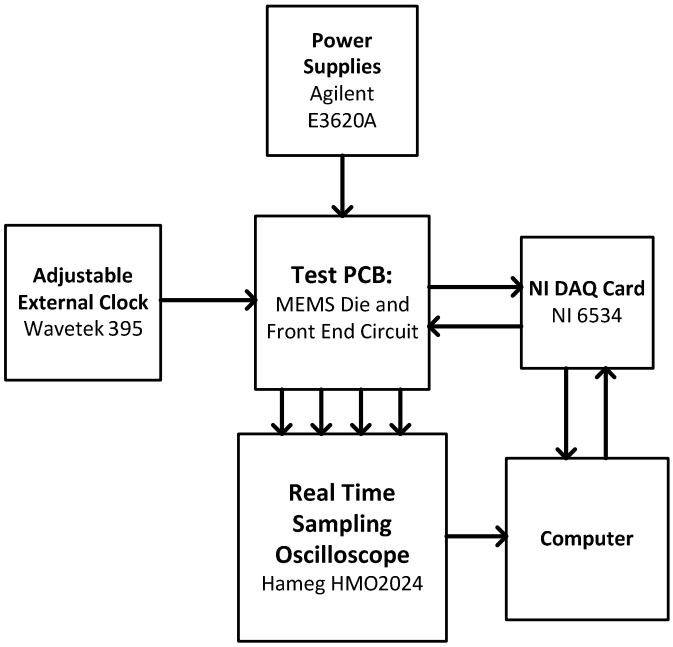

Fig. 4.5: Test Setup

4.3 Measurement Results

Due to a diode connection issue, some of the higher supply voltages needed to be lowered to about 1.7V to avoid forward biasing a diode strongly. Due to this lowering, the effective voltage placed across the accelerometer capacitors was decreased from 2V to 1.2V, meaning about half the signal level. However it is still possible to achieve the 9 bit resolution target across the different full scale ranges because of the overdesign.

Using the test setup above, it was found that the MEMS sensors had issues with stiction (static friction). The sensor itself was stuck to one side; as a result, any tilting or excitation of the accelerometer was not registered, and the switched capacitor output could not vary as a function of the tilt angle. Despite this issue, it is still possible to ensure that the appropriate power scaling occurred by measuring the power consumption levels of the analog circuitry and noise floor associated with each of the power scaling levels. Fig. 4.6 shows how the power varies versus the number of amplifier slices experimentally and via simulation.

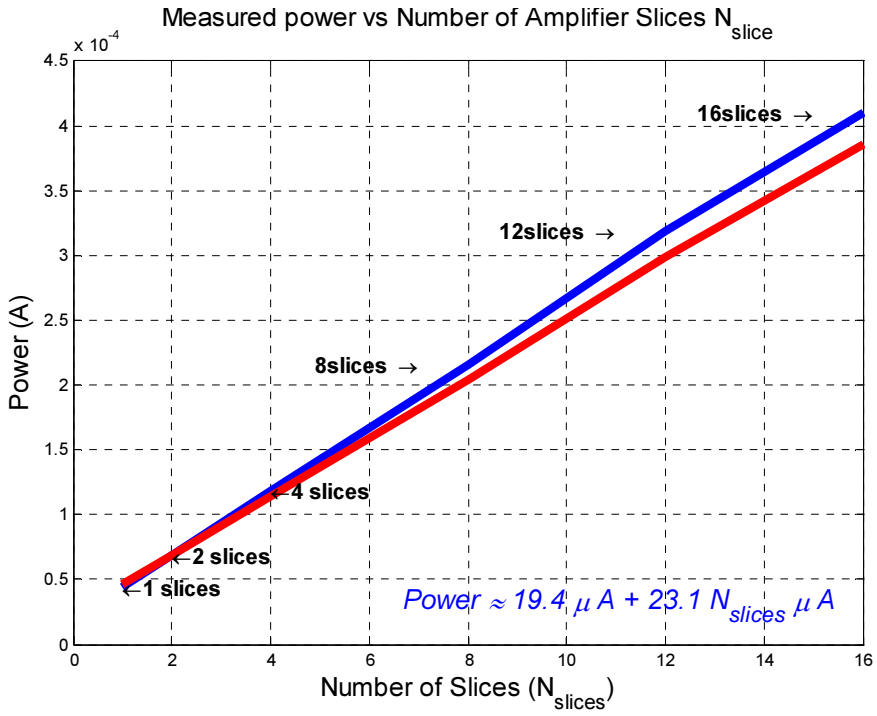

Fig. 4.6: Power Consumption Variation versus Number of Amplifier Slices

The measured power levels are quite close to the simulated power levels. Notice that the measured power is actually slightly lower in the single slice case. The reason for this is due to the diode supply connection mentioned earlier; as a slightly forward biased diode exists in the circuit (after reduction of the high vdd), there are actually a few μA of current being drawn from the larger supplies. As some of the higher voltages drive the output buffer and digital circuitry, it was not possible to lower them further without hurting the performance of the output buffer. The reason for the slight variation in the slopes of the two graphs is due to a slight mismatch between simulation and measurement in the current of a single slice of the amplifier.

Due to the stiction issue, a full SNDR measurement could not be done. However, some simple noise measurements could be performed.

The output full scale is a constant as a function of the different input full scales. However, since the output rate is different depending on the full scale and number of integrations (Table 3.1), we expect the noise level to vary such that the effective noise is approximately the same due to different oversampling rates. This ensures that the overall SNR remains the same as the full scale is varied. Table 4.2 shows the rms noise levels as a function of the full scale range. As mentioned earlier, the number of integrations is selected such that the output full scale range is identical. Similarly, the number of slices is selected to perform the appropriate power scaling for a given full scale setting. We expect identical RMS noise after the effect of oversampling since the full scale of the output remains the same.

Table 4.2: Noise Across Varying Full Scale Ranges

Full Scale (g)	Number of Slices	Number of Integrations	Effective Output Clock (kHz)	RMS Noise after OSR (μV)
1	16	16	125	63.01
2	4	8	62.5	68.09
4	1	4	31.25	63.62

Note that these values are quite consistent, and are reasonably close to the expected value of 59μV.

Offsets removed by the offset network were also measured. Table 4.3 shows both the simulated offsets (identical to Table 3.7) and the measured offsets for comparison.

Table 4.3: Table of Offset Values

Offset Bits (Sign, Cos<4:1>)	Measured Offset	Simulated Offset
10001	874 mV	-66.37mV
10010	700 mV	-192.1mV
10011	512 mV	-309.2mV
10100	326 mV	-418.8mV
10101	188 mV	-520.8mV
10110	-75 mV	-617.2mV
10111	-220 mV	-792.6mV
11000	-260 mV	-871.6mV
11001	-376 mV	-947.7mV
11010	-476 mV	-1.019
11011	-536 mV	-1.087
11100	-622 mV	-1.151
11101	-720 mV	-1.213
11110	-890 mV	-1.271
11111	-988 mV	-1.327

A plot of both the measured and simulated offsets in Fig. 4.7 shows variation in the slopes between the two offsets with respect to the control bit index.

As the capacitors in the offset network and the feedback capacitor in the second amplifier were not matched very well, this is the reason for the variation in the offset in the slopes. Despite this, the slopes are still quite similar. Since the measured output was nonzero with a zero g input, the curves above are also offset. Due to symmetry, this was not the case in simulation so the curves have their midpoint around 0V of offset without the offset network. This is the reason for the vertical shift between the two curves.

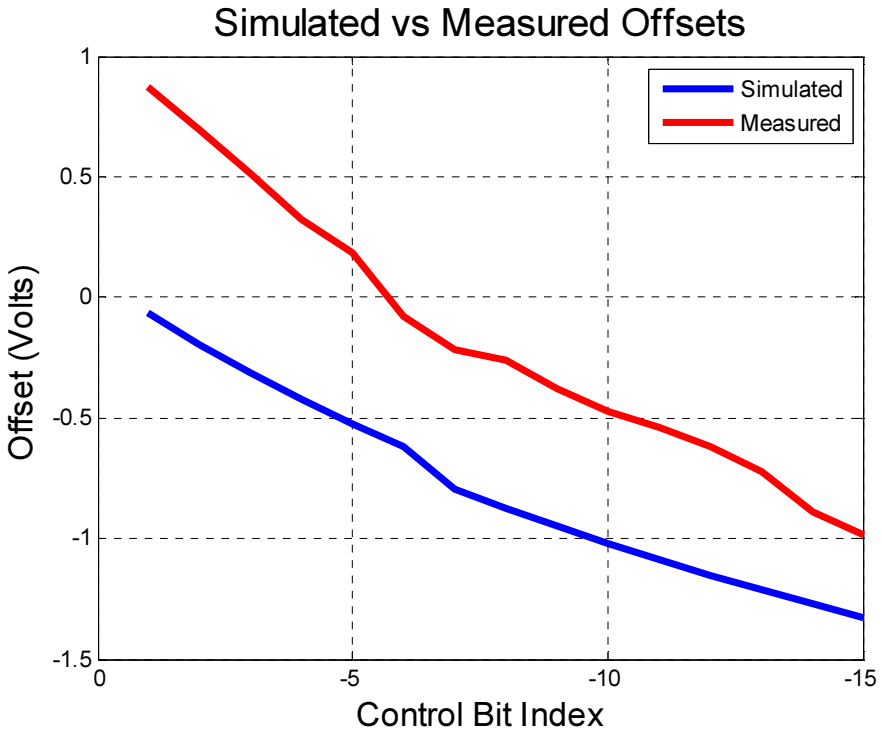

Fig. 4.7: Plot of Offset Values Over Control Bits

Chapter 5

Conclusions and Future Work

This chapter summarizes the conclusions of the work and discusses improvements and potential future work.

5.1 Conclusions

The 0.13um die and the MEMS accelerometer showed the clean power scaling of the front end analog circuitry with respect to the full scale. This clean power scaling is very practical due to the various full scale ranges used in commercial accelerometers. Each slice of the main amplifier consumed approximately 23uA of current on the 1.2V supply. The noise levels were measured and were quite close to the estimated levels that the design was based on. Additionally, the new offset network that was presented was shown to remove the expected amounts of offset. This offset network is also smaller than the typical networks used, and adds almost no power to the overall circuit.

5.2 Future Work

A few changes would improve the design and performance of the accelerometer front end circuit that was built:

- Adding a small circuit that compensates for potential MEMS issues if the accelerometer is stuck: an electrostatic force could be applied on the appropriate side of the MEMS accelerometer in order to pull the MEMS circuit back into its nominal equilibrium position, ensuring that the circuit would still be functional in the case that the MEMS accelerometer had stiction problems.

- Instead of using a full 16 single sliced amplifiers, a better technique would have been to use a single 1x slice and a single 4x slice to scale from 1 to 16 slices. Specifically, not using too many slices at once (for instance, 4 single 4x slices for a total of 16) would heavily improve interconnect capacitance due to decreased physical size of the layout. This would decrease variation in phase margin and other ac parameters across the number of amplifier slices that were used.

- Finally, power scaling of the 2^{nd} stage and the ICMFB was also possible, since the speed at which these stages operated varied. Note that the second stage actually would only scale at a rate of 2 times for every reduction in the first stage speed of 4x. This is because of the change in the number of integrations causes the downsampling rate from the first to second stage to change by a factor of 2 as shown in Table 3.1. However, this is not a major concern since the second stage amplifier power is already significantly smaller.

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