A Variable Gain Direct Digital Readout System for Capacitive Inertial Sensors

by

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A thesis submitted in conformity with the requirements
for the degree of Doctor of Philosophy
Graduate Department of Electrical and Computer Engineering
University of Toronto

The Edward S. Rogers Sr. Department
of Electrical & Computer Engineering
UNIVERSITY OF TORONTO

published by department of electrical and computer engineering, university of toronto

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First printing, May 2017

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Abstract

High fidelity interface circuits for capacitive accelerometers make use of feedback for signal detection but these feedback systems are limited by the sense capacitance and sensitivity of the accelerometers. This problem is addressed by a variable gain delta sigma based interface circuit that time multiplexes the accelerometer sense capacitance between the feedforward gain stage and feedback digital to analog (DAC) stage.

Interfaced with a commercial accelerometer with sensitivity of 4.5 fF/g, the circuit achieves 40.6 dB SNDR in the x-direction and 42.5 dB SNDR in the y-direction due to limitations of the available testing equipment. With proper equipment, the system has the potential to achieve 53.0 and 54.9 dB SNDR in the x and y direction respectively while significantly reducing harmonics associated with the non-linear variable sense capacitors. Other interface circuits using the same sensor at comparable power would achieve linearity below 40 dB due to the limitation of the feedback structure.

1
Introduction

The premise of this work is on the readout or interface circuits for capacitive accelerometers[1]. As this is a broad topic, this introductory section puts the body of work in context giving motivation for the work and the main problem it aims to solve.

Section 1.1 motivates the work by giving an overview of analog signal processing and narrows the scope of the problem. The organization of the thesis is then outlined.

Section 1.2 gives a historical background on microsensors and the emergence of the capacitive inertial sensor and its limitations.

Section 1.3 gives some important specifications for accelerometers that are often cited in publications. This is a motivation for the literature review section.

Section 1.4 proposes a new figure of merit for interface circuits and provides a literature review of recent work in the area.

[1] The terms "interface" and "readout" are used interchangeably in literature and also in this dissertation.

1.1 Motivation

1.1.1 Overall Picture of Analog Microelectronics Design

In the past decade, a novice view in the microelectronics field has been that everything is either digital or is being digitized and as such, analog processing is a dying field. Looking around us, perhaps this may seem like a reality; however, whenever you have an electronic signal that must interface with the real world, inherently you will have a significant analog front end. This front end can be summarized at a block level as shown in Fig. 1.1.

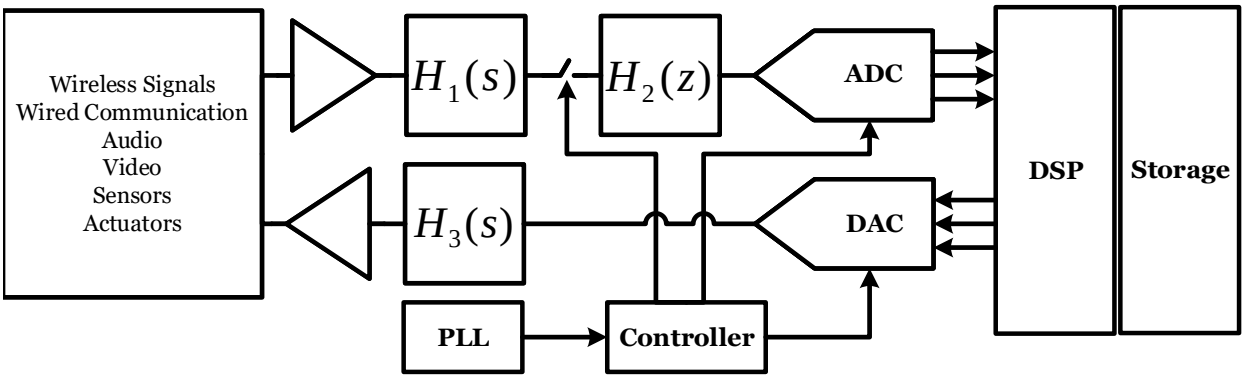


Figure 1.1: An overview of analog-mixed-signal (AMS) design.

There are two paths shown in Fig. 1.1. The top path is for signals that are coming from the real world. Ultimately, we would like to get our signal to the digital signal processing (DSP) block. Once here, we have a plethora of powerful and efficient digital signal processing algorithms that we can apply to the signal. We can store the data efficiently and send it across the world in seconds[2]. Truly, a world of possibilities open up with DSP and combined with inexpensive, small form factor storage that exists today, there are endless possibilities and applications for our data. Machine learning has been a topic that now exploits the ever expanding available data to identify patterns for decision making. But nevertheless, the real world will always be analog and before we can interpret the data we have, we must somehow digitize the information. Therefore, although analog design is at the bottom of the information chain, it is an integral part that cannot be taken away.

[2] From a human perception, realistically we can transmit data in Giga Hertz for wireline or wireless applications.

At first glance, digitization seems rather trivial. All we need is an analog to digital converter (ADC). The problem is that the signals coming from the physical world (for example from an antenna) are very small and often corrupted by interference and noise. To then perform an analog to digital conversion on this noisy signal directly would require such a high precision ADC that implementation would either be impossible or at least very expensive in terms of power and area.

Therefore, it turns out that rather than attempt direct digitization,

what we end up doing is preceding the analog to digital converter with blocks such as amplifiers (to make the signal bigger), filters (to eliminate noise and interference), and of course, the ADC to pass on the information to the digital world.

Inherent to the figure above is a sampling process somewhere along the chain. This is needed to go from a continuous time analog signal to a discrete time analog signal. Signals in the chain can be divided into three stages. First, there are the analog signals that represent physical phenomena and can take any value and are valid at any time. Once the signal is sampled, it becomes an analog discrete time signal. It can still take any value but its value is only interpreted at discrete periods in time. Finally, a discrete time analog signal is then converted with an ADC to become a digital signal - a signal which is valid at discrete times and its value is also quantized[3]. Where sampling occurs in the chain of Fig. 1.1 and how much of the signal processing is performed in the analog discrete time domain versus the analog continuous time domain is in of itself an application specific design choice.

[3] continuous time digital signals do exist but are rather an academic curiosity [1]

So it is clear that somewhere along the chain of Fig. 1.1 we need to sample our signal. And to sample signals, we need a clock that must be provided by a phase-locked loop (PLL). Interestingly, the digitization of this block has itself been a very active research area [2] [3]. Finally, important to the above but not specifically contained in the diagram, are biasing circuits, reference circuits, voltage regulators, digital compensation blocks - components that are needed to keep the system working at required specifications. For completeness, we can also look at the bottom path where a digital signal is converted to an analog signal which in turn will drive some kind of an actuator[4]. Again, similar arguments can be made as to why a digital signal cannot directly be converted to an analog continuous time signal, and some processing is needed. Once more, inevitability somewhere in this chain we must make a transition from the discrete time domain to the continuous time domain. It may be as simple as a single node, but that transition must exist.

[4] a motor for example for heating/cooling or an antenna that sends data

Therefore, although the drive for digitization is valid, nevertheless, analog signal processing is a fundamental part of this effort. Most importantly, the first element of the chain, where a transducer converts a

real world signal into an electrical one is critical. This transition from the physical domain to the electrical domain and the subsequent need for digitization is the general domain of this thesis.

1.1.2 Scope of the Thesis

In the previous section, we have described in broad terms the field of analog mixed signal processing or AMS [5]. Research in analog electronics is often at specific blocks such as amplifiers, filters, PLLs, ADCs or auxiliary circuits that accompany them.

[5] this is a widely used industry term although somewhat of misnomer.

However, the previous section also demonstrated that at a system level, trying to capture an analog signal and convert it to a digital signal is very application specific. Depending on the specific application, the signal processing components in our path and transitions between signal domains can be widely different. For a specific application, we may forgo the use of amplifiers as the signals may be large enough. For others, there may not be a need for interference cancellation. Therefore, this thesis is not particularly interested in pushing the boundaries of any specific block, but rather proposing an application specific system level design with the end goal of digitization.

The application that is aimed for is capacitive accelerometers. There are a variety of reasons for choosing these types of sensors. They are relatively inexpensive to manufacture due to a streamlined manufacturing process driven by having large volume applications[6]. Thanks to an interdigitated or comb drive structure proposed in 1980's [4], the sensitivity of these accelerometers can be relatively large. Capacitive accelerometers also provide good noise and temperature immunity [5]. Finally, they are quite flexible in the environmental variables that they can detect. Although an accelerometer can only detect force, there are many physical phenomena that induce a force and hence, the range of physical signals that can be detected with accelerometers is quite diverse. If the force being detected is the result of an acceleration, then it can also be used to deduce velocity and distance, and many applications can be thought of in each of these categories[7].

[6] Automotive industry makes extensive use of these sensors in cars

[7] We will use the term acceleration to mean force going forward. It should be clear, however, that acceleration does not necessary mean movement depending on the context.

Every application has its challenges, but for a system level design as illustrated in Fig. 1.1, the input to the system becomes a major obstacle.

Designs for specific blocks will always assume a perfectly linear input for testing purposes. A PLL designer assumes that a crystal with negligible phase noise (for the intended application) exists. An ADC or filter designer will design and characterize their system based on a perfect input sine wave [8]. In a system level design, the input itself then becomes the most underpinning design criteria that must closely mimic the physical device. No matter how well other blocks are designed, if the input to this system is not characterized and considered in the system level design, then the design does not achieve its purpose.

[8] or at least, a signal whose performance is above the performance of the ADC

Thus, this thesis proposes a system level design for digitizing signals from capacitive accelerometers. As such, the characterization of the mechanical accelerometer and its limitations becomes very important in design. To help with the flow of the manuscript, this topic is explored in Appendix D and E and the results used in making system level design choices. We will state these results here to narrow the scope and outline the organization of the thesis.

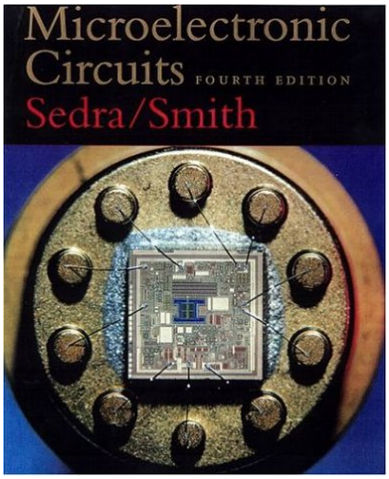


Figure 1.2: A closed loop or force feedback accelerometer (ADXL050) as shown in front cover of an electronics textbook. ADXL050 was a closed loop or force feedback accelerometer marketed by Analog Devices (circa 1992).

1.1.3 Open Loop versus Closed Loop

ASICs for capacitive accelerometers can be divided into two broad areas. The areas are based on whether the electronic circuitry actively tries to reduce the mechanical movement of the sensor through feedback. Mechanical closed loop systems have been a recent idea, first established in 1990 [6]. The first commercial product in this area was the ADL050 from Analog Devices (see Fig. 1.2). Both these techniques have tradeoffs and these are discussed in some detail in Appendix E. The proposed design in this thesis, however, focuses on an open loop implementation mainly because open loop systems operate at lower power, are less complex, less costly and therefore, have a broader application basis. Improvements in open loop design can therefore have a larger impact.

1.1.4 Dual Chip versus Single Chip

A second category organization for interface circuits is to whether to incorporate the sensor and the interface circuit together (single chip) or to manufacture each separately and bondwire them together (dual chip). There are tradeoffs to each approach. Incorporating a single chip solu-

tion requires a process that can implement electronic components along with fabricating the mechanical structure of the sensor. These processes are surprisingly quite prevalent. A trend in the microelectronics industry has been for older CMOS or Bipolar processes to be modified for MEMS fabrication in order to expand the lifetime of these foundries and achieve additional revenue. Generally, however, the quality of the electronic parts manufactured in mixed processes is rather poor. Temperature and processes needed to create mechanical structures are in many ways incompatible with CMOS and Bipolar processes [7]. This in turn means that either specialized steps are needed (driving up costs), or the choice and quality of circuit elements is limited. On the other hand, single chip solutions have better noise immunity and less parasitics which generally are beneficial to interface circuits. This thesis focuses on a two chip solution. The accelerometers are manufactured and designed by a commercial vendor and the electronic circuitry is fabricated in a 0.13 μm CMOS technology and bonded together in a QFN package.

1.1.5 Organization of Thesis

The field of interface circuits is quite broad, and this manuscript aims to narrow the scope in an intuitive manner and arrive at the problem for which a solution was implemented. We have already narrowed our scope considerably. As discussed in the previous section, from a practical standpoint, the focus is on capacitive accelerometers that are interfaced separately with an ASIC and operated in open loop.

Section 1.2 gives a mechanical overview of these sensors by highlighting the historical events that led to their development. The major problem with these sensors is then highlighted; mainly that the capacitance change due to an external force is extremely small and inherently nonlinear. The rest of the dissertation then focuses on how interface circuits can be used to overcome these problems.

Having established the mechanical structure and the associated problem, in Chapter 2, the field of open loop interface circuits for capacitive accelerometer is further organized[9]. We make a distinction between displacement measurements and velocity measurements in Section 2.1 which is very often overlooked in sensor analysis. We then focus on

[9] To be more specific, techniques outlined are equivalently applicable to closed loop systems but the emphasis will be on open loop details.

displacement measurements and organize this area into three broad categories: current, voltage and charge measurements. Each of these circuit types is examined and the theoretical resolution of these circuits is analyzed. Based on this analysis, we conclude that for open loop capacitive sensors that are implemented in a two chip solution, a *switched capacitor charge based circuit* is the most appropriate. Finally, Section 2.6 looks at the possible outputs that the various circuit topologies can achieve. The analysis shows that the best results are obtained with a ratiometric charge balanced output.

In Chapter 3, the proposed solution is laid out based on the results of the previous section; mainly that for a two chip solution in open loop configuration, the best possible fidelity based interface circuit is one that achieves ratiometric output and is charge balanced. This result leads to the use of delta sigma modulators (DSM) as capacitive ratio circuits that easily adapt to the digital domain with the use of a decimation filter. As a solution using a DSM is laid out, a problem arises. Due to the unique structure of the sense capacitors, the feedback signal often overpowers the feedforward signal leading to what we call the *low signal tone* problem. This is very unique to capacitive accelerometers due to their physical construction and more importantly, arises in any system that makes use of feedback to achieve ratiometric charge balanced outputs. The solution then lies in using a separate time multiplexed feedback and feedforward signal path which allows us to independently adjust the signal gain and feedback gain overcoming the low tone signal problem. Finally, precision signal processing techniques for the circuit including adaptation to differential signal processing are discussed in Section 3.5.

Finally, chapter 4 details the measurement of the fabricated circuit as a regular delta sigma modulator (Section 4.1), with generated accelerometer signals (Section 4.2) and finally with an integrated accelerometer (Section 4.3). Fig. 1.3 summarizes the above described organization.

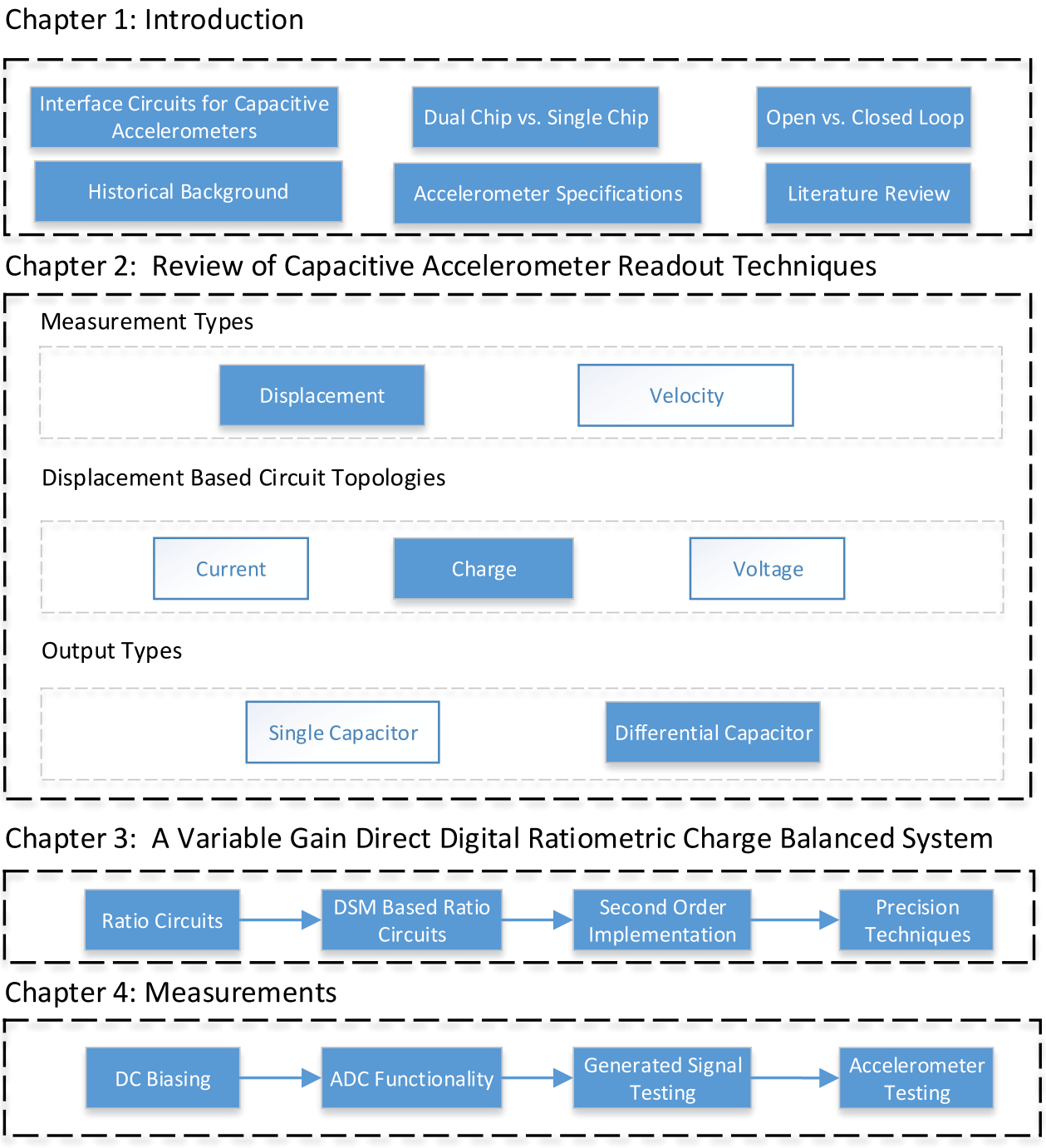


Figure 1.3: Organization of dissertation. Blank boxes are areas that are not extensively analyzed.

1.2 Physical Construction of Capacitive Accelerometers

The acronym MEMS - micro-electro-mechanical sensors or systems - was first introduced in 1989 [8]. The term was used to distinguish between newly developed and commercialized microsensors (built using semiconductor fabrication technology) and traditional miniaturized sensors (built using lathe machining technology). The history on how this new field developed parallels that of the microelectronics industry and it is worthwhile to briefly go over this development, as it leads directly to the invention of the capacitive accelerometer.

One of the more popular early machined sensors was the strain gauge sensor as shown in Fig. 1.4. In these sensors, a material was deposited on a surface such that a strain caused a physical change in the material. This change then resulted in a change in resistance that could be detected electronically. The sensitivity of these sensors greatly depended on the rate of physical deformation as given by the material's Young modulus.

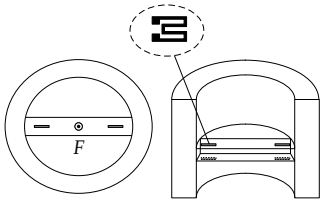


Figure 1.4: A miniaturized strain gauge sensor.

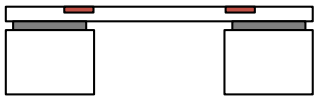


Figure 1.5: The first miniaturized piezoresistive sensor using silicon.

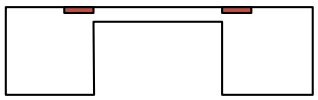


Figure 1.6: A miniaturized piezoresistive sensor without the use of epoxy.

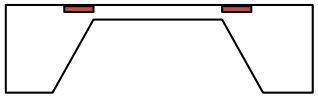


Figure 1.7: A piezoresistive microsensor. The cavity is formed by wet etching of silicon.

In 1954, long before semiconductor microelectronics had gained popularity, a mechanical engineer published a paper reporting that the change in resistance of germanium and silicon was much larger than counterpart metal strain gauges [9]. He had discovered that this large change in resistance was dominated by change in resistance and gave some arguments as to why a mechanical change in the material can lead to a change in resistivity - a property that until then was thought to be largely inherent to the material. This property was termed the piezoresistive effect and it led to research into building strain gauges with semiconductor material.

After the discovery and analysis of the piezoresistive effect in the 1950's, the first step in making microsensors was to use silicon as a mechanical material for the sensor. The first piezoresistive sensor making use of silicon as a structure was reported in 1962 by Tufte [10]. It consisted of a silicon diaphragm with piezoresistors (p-doped silicon) introduced into it by diffusion. The diaphragm was bonded to a glass or metal substrate using an epoxy (Fig. 1.5).

This was the first time a mechanical sensor used silicon both as the sensing and structural material. The next milestone was the use of

drilling techniques to create complete structures in silicon without the need for an epoxy (Fig. 1.6).

Finally, in the mid 1970's, anisotropic etching techniques were used to create a microfabricated piezoresistive sensor [11]. *This was the first "microsensor"* where for the first time in history, a functional device was completely fabricated using (borrowed) semiconductor fabrication technology (Fig. 1.7).

Although piezoresistive pressure sensors dominated the commercial industry in the 1980's and early 1990's, from the very outset, there was active research into finding alternatives. This was mainly due to the limitations of piezoresistors which include:

- Piezoresistive effect is largely due to stress rather than physical deformation of the material. This became an issue because packages created stress or thermal mismatch resulting in an offset and temperature drift in the output.
- The temperature coefficient of piezoresistors is in the order of 10^{-3} (percentage change in resistance due to temperature) which is quite large and unacceptable for many applications. To overcome this, careful calibration and temperature compensation techniques were used leading to higher costs.

These issues led to research throughout the 1970's and 1980's into other sensing techniques and at the forefront was capacitive sensing. Capacitive sensors do not rely on the mechanical properties of the material and therefore are much more stable than piezoresistors but have drawbacks as we will discuss shortly. Following on the footsteps of the piezoresistor, a capacitive pressure sensor was first developed similar to the one shown in Fig. 1.8 [12].

In this configuration, the silicon diaphragm serves as one electrode and the aluminum film in the cavity as the second non-moving electrode. The cavity must be a vacuum to measure absolute pressure accurately. If not, then the pressure measured becomes a strong and complicated function of air with poor control. The operation is straight forward. The pressure displaces the diaphragm and changes the capacitance. Therefore, pressure is dependent on the capacitance between the plate and

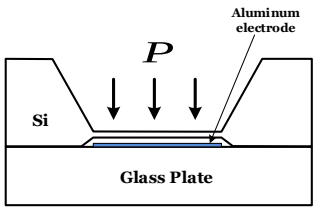


Figure 1.8: An early capacitive pressure sensor making use of silicon fabrication technology.

aluminum electrode. There are, however, many practical issues with capacitive pressure sensors [13] and these sensors have failed to be widely accepted in the market.

Where the capacitive pressure sensor has failed, the capacitive accelerometer has been very successful. Following the structure of a pressure sensor, an early adaptation of theses sensors used two parallel plates that would deform from some physical force being applied to it. This is shown Fig. 1.9 [14]. The capacitance change is given by

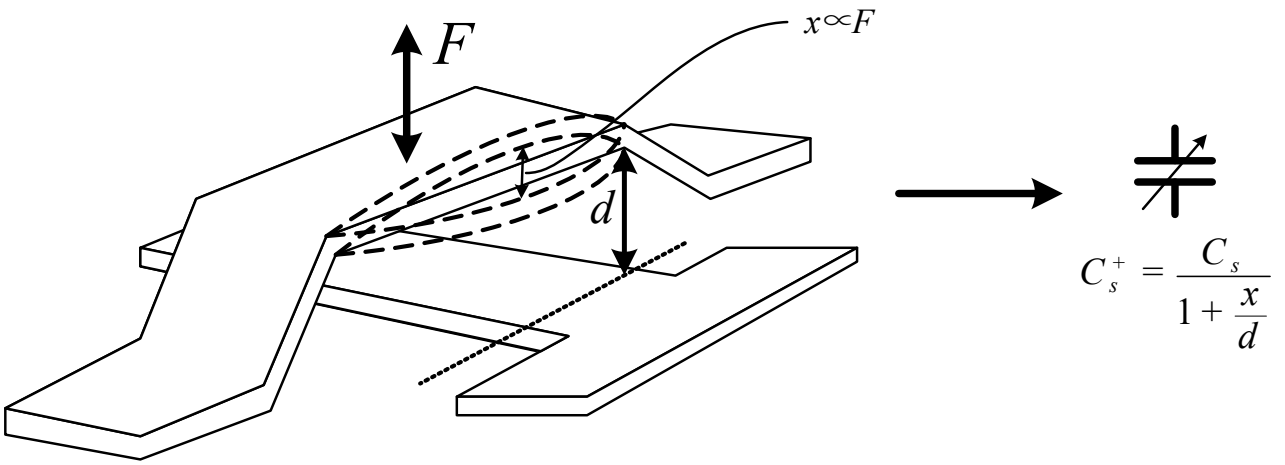


Figure 1.9: An early capacitive accelerometer and the equivalent simplified electrical model. Note that a more robust model would include parasitic capacitances at each node as well as the equivalent series resistances.

$$C_s^+ = \frac{C_s}{1+\frac{x}{d}} \ , \tag{1.1}$$

where C_s is the equivalent capacitance of the structure at rest (zero force), d is the nominal distance between the parallel plates (at rest), and x is the displacement under the force $F(t)$. For small displacement, $x << d$, the displacement is proportional to $F(t)$ according to

$$x(t) = \frac{1}{k}F(t) \ , \tag{1.2}$$

where k is the spring constant associated with the moving plate. The above equations highlight the clear drawback of capacitive sensing. Capacitive sensing is *inherently non-linear* because the capacitive change is a nonlinear function of the measurand $x(t)$ and conversely $F(t)$. Moreover, the capacitance change is very small[10] making detection difficult especially in the presence of parasitic and stray capacitances and elec-

[10] in the order of attofarads!

tromagnetic interference from the environment.

The next major advancement in mechanical sensors[11] occurred in the 1980's. It was proposed to build mechanical sensors in a planar fabrication process. This structure became known as the interdigitated or comb drive [12] as shown in Fig. 1.10 [15].

[11] and arguably the reason for their market acceptance

[12] The main application was to drive the structure to create motion, in which case the sensor is now an *actuator*

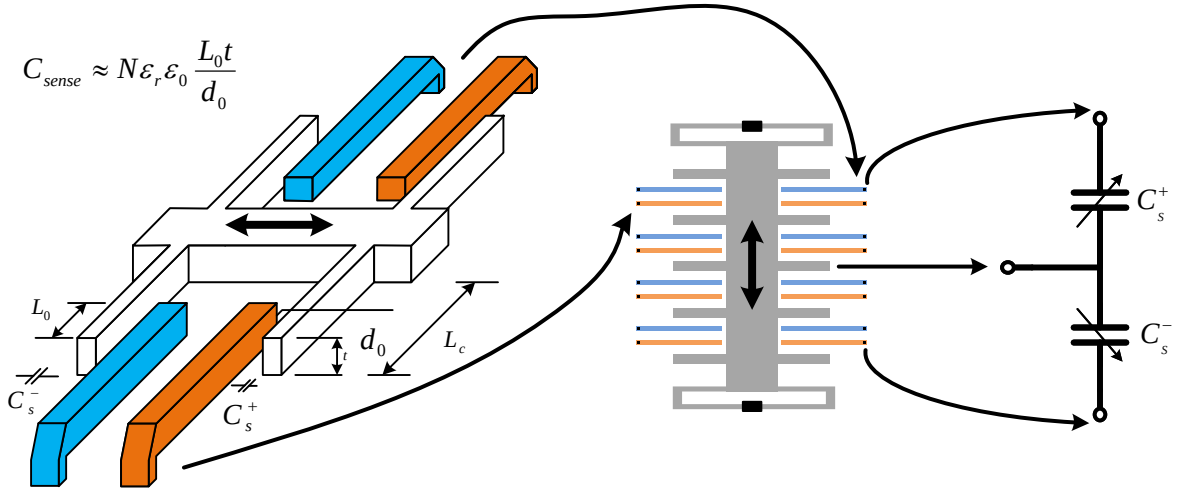


Figure 1.10: A surface micromachined capacitive accelerometer using an interdigitated structure.

This structure has several benefits. Previous structures such as the one shown in Fig. 1.9 used the entire bulk of silicon and as such were called *bulk micromachined*. The structure of Fig. 1.10 can be built on a planar or *surface micromachined* process similar to how semiconductor circuits are built. This has a lower cost than its bulk micromachined counterpart as well as being more adaptable to fabricating electronic circuitry on the same die.

Furthermore, the interdigitated structure allows for differential capacitive sensors where capacitors change in opposite directions according to

$$C_s^+ = \frac{C_s}{1-\frac{x}{d}} \qquad \text{and} \qquad C_s^- = \frac{C_s}{1+\frac{x}{d}} \ . \tag{1.3}$$

This has several advantages including lower non-linearity as will be discussed further in Chapter 2.

Finally, the structure allows for a compact way of increasing total sense capacitance. Static capacitance associated with the fringe electric fields reduces the sensitivity of devices[13]. The interdigitated structure allows for large sense capacitors relative to fringe capacitance in a comparatively smaller area. For completeness, Fig. 1.11 shows an interdigitated structure using bulk micromachined fabrication.

[13] The amount of capacitance change per unit of force

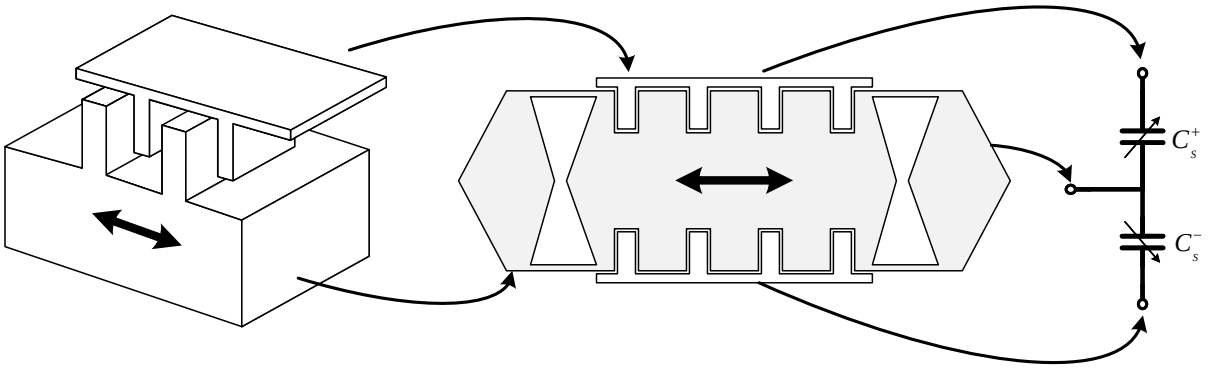


Figure 1.11: A bulk micromachined capacitive accelerometer using an interdigitated structure.

Recent advancements in manufacturing of capacitive accelerometers focus on optimizing manufacturing steps for lower costs [16], and reducing stress induced movements associated with fabrication and packaging [17] [18] [19]. Challenges also exist in fabricating dual or tri-axial accelerometers. For many applications, force detection is needed in lateral directions (x, y) or all three directions (x, y and z). This makes manufacturing a challenge[14] and fabrication techniques have been developed in creating such structures in both bulk and surface micromachined technologies [20] [21]. All these techniques have a tradeoff with cost as additional mask layers or post processing is required to achieve different structures.

[14] especially if differential structures such as the one shown in Fig. 1.10 are needed

For the rest of this dissertation, we will focus on interface circuits for accelerometers that are differential in nature (either achieved through interdigitated structure or otherwise) with capacitance change given as shown in Eq. (1.3). Before we delve into this topic, however, we need to discuss specifications for accelerometers and develop a figure of merit for interface circuits.

1.3 Accelerometer Specifications

This section summarizes some of the most commonly used specifications for accelerometers. The detailed analysis of the mechanical operation of accelerometers is given in Appendix D. The definitions in this section are used for the literature review and throughout the manuscript.

1.3.1 Sensitivity

Sensitivity[15] is defined as a sensor's electrical output to the mechanical input. For accelerometers, this is volts/g where g is the unit of gravity equal to 9.8 m/s^2. Sensitivity is only valid at a specific frequency (typically 100 Hz) and temperature range (typically 25 ± 5°C). It is also, strictly speaking, only valid at a specific input (for example 2 g). Sometimes the sensitivity is cited with a tolerance ($\pm 5\%$) to specify that it is not constant with input.

[15] Also called Responsivity or Scale Factor

Since the sensitivity of a sensor depends both on the readout circuitry and the sensor itself, it is useful to define two other sensitivity terms. *Sensor sensitivity* is the rate of transducer change to mechanical input (capacitance per unit of g for capacitive accelerometers) and the *readout sensitivity* as the rate of electrical output change to transducer change (voltage per unit of capacitance for capacitive accelerometers).

Sensitivity plays a major role in determining the fidelity of an accelerometer system as will be discussed in the next section. Although publications in the area of sensor interface circuits are not consistent in reporting sensitivity values, values can be fairly accurately estimated using the static capacitance of the sensor and an estimation of the displacement x under acceleration.

1.3.2 Frequency Response and Bandwidth

Frequency response is the sensitivity over the entire frequency range and often exhibits a low pass behaviour as is the case for accelerometers. Bandwidth is defined as the frequency at which the sensitivity falls 3 dB below the nominal sensitivity (defined by the sensitivity parameter). For capacitive accelerometers, frequency and bandwidth are closely tied to the natural frequency of the mechanical sensor, ω_n.

1.3.3 Range

Also called dynamic range, this is defined as the difference between the highest and lowest detectable input signal. The highest value is either set by the sensor physical limit or saturation of the electronic circuitry [16] and the lower limit is set by the noise floor or resolution (see Section 1.3.5). A related parameter is the full-scale range defined as the input range for the sensor. It is often cited in the descriptive title of the sensor, for example, a ±5 g three-axis surface micromachined accelerometer.

[16] There does not appear to be a rigorously defined "acceptable" upper range for interface circuits such as spurious free dynamic range (SFDR) that is seen with electronic blocks.

1.3.4 Linearity

Ideally the sensor's sensitivity should be the same across its input range but is often not the case. Linearity is then a measure of how far the sensor's output deviates from its ideal linear output. There are several methods to specify linearity. The most common is to define it as the maximum percentage deviation from the specified sensitivity over the entire range of the sensor. For example, 0.1% for ±5 g full-scale range. Since this definition is rather restrictive, and sensors often have worse linearity at higher inputs, another method is to specify piecewise linearity such as 0.1% for ±1 g, 0.5% ±(1 : 2) g, etc.

1.3.5 Resolution or Noise Floor

This is the system's noise floor or the smallest input value that can be detected. For accelerometers, noise is broken into mechanical thermal noise and electrical noise and often cited as $\mu g/\sqrt{\text{Hz}}$. Since these noise sources are uncorrelated, the total noise is given by

$$a_{\text{total}} = \sqrt{a_{nm}^2 + a_{ne}^2}\ , \tag{1.4}$$

where a_{nm} is the mechanical thermal noise and a_{ne} is the electrical noise. Publications often do not break the noise component into parts but it is clear that having an accelerometer with a lower mechanical noise floor allows for better overall system design. This issue must be taken into account when creating a figure of merit as will be discussed in the next section.

1.3.6 Resonant Frequency

Resonant frequency is the frequency at which the sensor exhibits maximum sensitivity due to the natural resonance of the mechanical device. There may be several resonant frequencies for a device in which case the lowest frequency is cited. For open loop systems, the resonant frequency can be a gauge for the maximum frequency the device can operate at. For closed loop or force feedback systems, resonant frequencies add additional poles to the overall system making stability an issue.

1.3.7 Cross-Axis Sensitivity

Cross-axis sensitivity is a measure of how much one axis of a device changes due to an input on an orthogonal axis. For example, x-axis cross sensitivity due to a y-axis acceleration may be sited as 3%. Therefore, for every g of acceleration in the y direction, the x-axis experiences a 0.03 g acceleration. For testing, cross sensitivity should be performed to ensure that measurements in one direction do not influence another. Mechanical design of accelerometers for low cross-axis sensitivity is also an active area of research [22].

1.4 Literature Review and Figure of Merit Construction

1.4.1 Developing a Figure of Merit for Comparison

When comparing two systems, it is very important to have a rigorous metric that is the property of the circuit, and not of external factors. In AMS design, several metrics exist for comparison and these metrics have had a history of revision mainly based on achieving an apple to apple comparison of designs. Some of these include maximum achievable SNDR, spurious free dynamic range (SFDR), and more commonly in high frequency system design the input/output referred third intercept points (IIP3, OIP3) and the 1-dB compression point.

Finding a fair figure of merit (FOM) for a sensor interfaced with electronics is challenging and an established FOM is yet to be found. The challenge lies in the fact that the structure of the mechanical devices will have a great effect on the signal fidelity and power consumption of the

underlying system. This is further complicated by the systems that do not provide all the necessary information regarding the type of sensor in use. In the following sections, some of these issues are discussed and a figure of merit is proposed to achieve a fair comparison for interface circuits.

SNDR and Device Sensitivity Tradeoff

Device sensitivity plays a major role in determining the fidelity of output signals. To demonstrate this, assume that there are two accelerometers and the exact same readout circuit is used for both systems. This scenario is shown in Fig. 1.12.

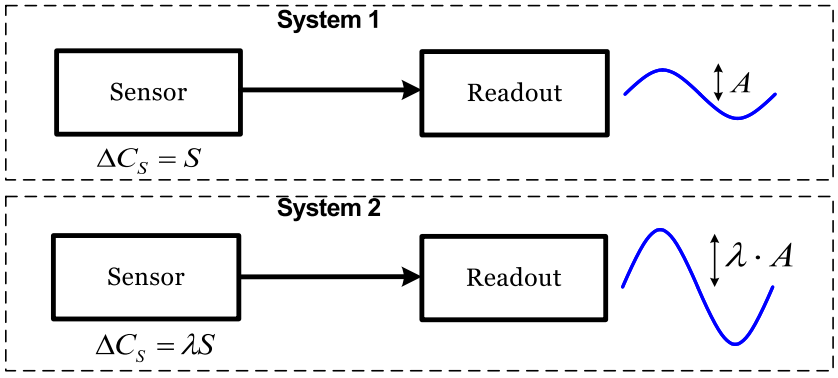


Figure 1.12: Two systems with different accelerometer sensitivities.

Now assume that the device sensitivity for one sensor is a factor λ larger than the other. Accordingly, the output of the first sensor would be λ higher than the other and the signal power would be λ^2 higher. Therefore, if the FOM for interface circuits only accounts for fidelity in the form of maximum SNDR, then circuits with higher sensitivity devices would have a clear advantage. Therefore, for the figure of merit to be only a function of the interface circuit, the fidelity must be discounted relative to the sensitivity. This problem is not an issue in other analog blocks because inputs are assumed to be coming in at the full scale of the power supply.

One issue with the above analysis is that it does not take into account the sensor's mechanical noise as it relates to the device sensitivity. The mechanical noise is inversely proportional to the mass of the de-

vice. However, it is clear from the physical construction of capacitive accelerometers as shown in Fig. 1.10 and Fig. 1.11 that to increase the mass of the device, we will inevitability have to increase the total sense capacitance. This in turn means that the noise is inversely proportional to sensitivity because if we want to double the capacitance we inevitably must double the volume[17]. Based on the above discussion, we can write that

$$a_{nm} = \frac{K}{S} \ . \tag{1.5}$$

[17] It is possible to design custom capacitive accelerometers that increase mass size without increasing capacitance, but this is a niche area. Once a manufacturing process has been established for accelerometers, sensitivity and mass would be proportional to each other.

where a_{nm} is the mechanical thermal noise of the sensor, S is the sensitivity of the sensor given in terms of pF/g and K is a constant of proportionality. The total noise of a system having a mechanical sensor and an electronic interface circuit is given by Eq. (1.4). Referring to Fig. 1.12 and Eq. (1.4), we can see that the advantage of a higher sensitivity device is not simply in the signal power but also the device mechanical noise. Therefore, we need a factor that accounts for both. Taking the ratio between the SNR of the first system compared to the second system we have

$$\begin{aligned} \text{SNR fraction} &= \frac{\text{Signal to noise ratio of system 1}}{\text{Signal to noise ratio of system 2}} \\ &= \frac{\lambda^2 A^2}{\sqrt{\frac{K}{\lambda^2 S^2} + a_{ne_1}^2}} \times \frac{\sqrt{\frac{K}{S^2} + a_{ne_2}^2}}{A^2} \ , \end{aligned} \tag{1.6}$$

where a_{ne_1} and a_{ne_2} are the interface electronic noise for system 1 and 2 respectively.

At this point, we need to make some simplification in regards to how the electronic noise will be designed relative to the mechanical noise. Since the noise sources are assumed to be uncorrelated, they add up as a sum of squares. Therefore, there is little incentive to aggressively reduce one noise source compared to the other. For example, if the electronic noise is reduced to 1/4 of the equivalent mechanical noise, then the electronic noise will only contribute 1/5 towards the total noise power. As a result, reducing the electronic noise beyond a certain percentage below the mechanical thermal noise (or vice versa) has diminishing returns. Let the thermal noise relative to the mechanical noise be given

by a factor β, as such we can simplify the above as

$$\text{SNR fraction} = \frac{\lambda^2}{\sqrt{\frac{(1+\lambda^2\beta)K}{\lambda^2 S^2}}} \times \sqrt{\frac{(1+\beta)K}{S^2}}$$
$$= \lambda^2 \sqrt{\left[\frac{(1+\beta)\lambda^2}{1+\lambda^2\beta}\right]} \,. \tag{1.7}$$

Taking the extremes, if $\beta = 0$, we have a noise free interface circuit. In this case, a device that has better sensitivity by a factor of λ would result in a better SNR by a factor of λ^3 [18]. Taking the opposite extreme, if the interface circuit is extremely noisy compared to the sensor mechanical noise ($\beta >> 1$), then the improvement to SNR is equivalent to λ^2 or completely due to an increase in the signal amplitude. A good design choice, as discussed above, is to choose $\beta = 1/4$. In this case, we can rewrite the above formula as

$$S_{\text{normalized}} = \lambda^2 \sqrt{\left[\frac{1.25\lambda^2}{1+0.25\lambda^2}\right]} \,. \tag{1.8}$$

Therefore, the signal fidelity should be normalized by the factor given by Eq. (1.8). When comparing several systems, we can choose one sensor as the reference device, and use its sensitivity to normalize all other device sensitivities.

[18] λ^2 factor is due to the improved signal and an additional λ factor is due to the lower noise from the larger device mass

SNDR and Input Force Tradeoff

Another factor that skews comparison of accelerometers systems is driving capability. Assume that two accelerometers with the same sensitivity and the same readout circuits are implemented but one accelerometer is driven harder by a factor α as shown in Fig. 1.13. In this case, there is an improvement in signal of α and in power of α^2. In an AMS system, this is akin to having two designs with different power supplies and FOM's generally do not take this into account [19]. The issue, however, is that this problem is much more pronounced for accelerometer systems especially for research purposes. For example, if a system is driven by 1 g versus another which is driven by 8 g, the second system will have a factor of 64 increase in signal power!

[19] For example, FOM's comparing ADCs

Therefore, to make a fair apple to apple comparison for accelerometers that have varying input ranges, the fidelity of these systems, as measured by the maximum SNDR, must be normalized to a unit of drive acceleration force.

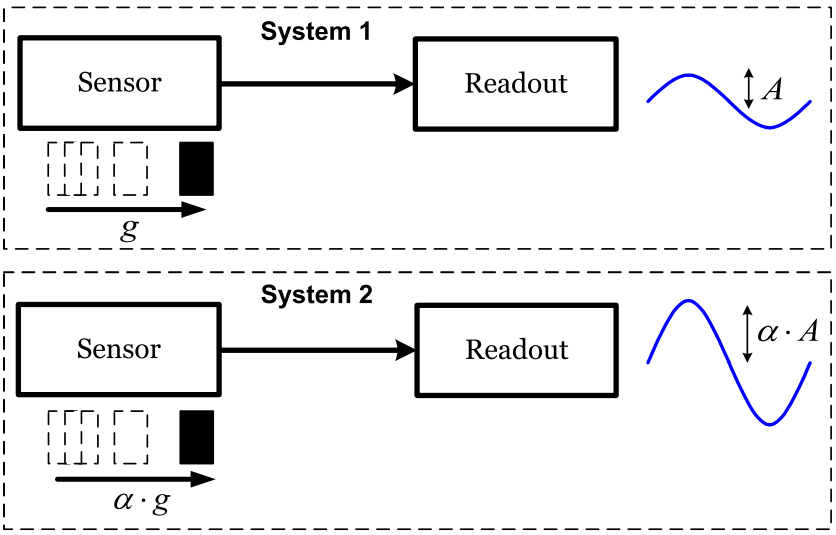


Figure 1.13: Two systems with different driving capabilities. The second system will have better simply for being driven by a higher force.

Based on the discussion of device sensitivity and input drive, we can normalize a reported system's maximum SNDR according to

$$SNDR_{\text{Normalized}} = \frac{SNDR_{\text{reported}}}{S_{\text{normalized}} \cdot \text{Full Scale}} , \tag{1.9}$$

where $S_{\text{normalized}}$ is the sensitivity factor given by Eq. (1.8) and Full Scale is the maximum force that the accelerometer is driven at.

Power and Sense Capacitance Tradeoff

Finally, apart from signal fidelity, power plays a major role in comparing different systems. It is well accepted that power trades off against bandwidth. For example, for a two stage op-amp, the bandwidth proportional to the transconductance g_m of the input pair which is directly proportional to current. When an interface must be combined with a mechanical sensor, power consumption is complicated from two viewpoints. To demonstrate this, assume that we have two sensors with all the same parameters except that the static capacitance, C_s, is different

in one by a factor of K as shown in Fig. 1.14.

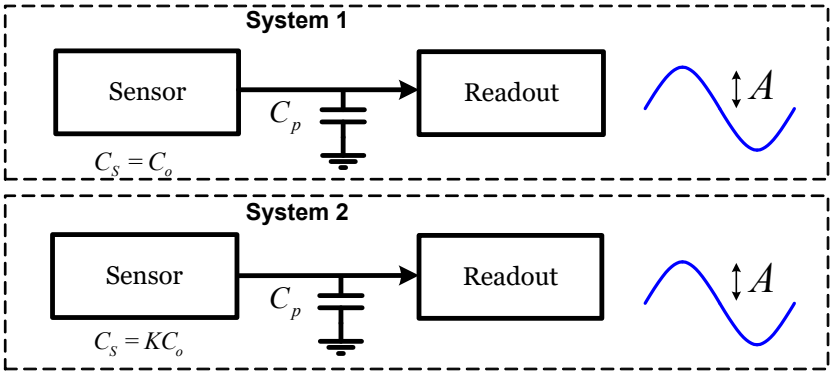


Figure 1.14: Two systems with different accelerometer sense capacitances but same sensitivity.

The effect of increased sense capacitance is not trivial and depends on the type of readout used. This topic is more readily discussed in Section 2 but the conclusion for power is rather straight forward: total capacitance at the input of the interface circuit is directly proportional to power consumption. Therefore, power must be normalized to the total sense capacitance.

As we discussed in the previous section, the total sense capacitance is directly proportional to sensitivity. Therefore, a system that has a large sensitivity will inevitably have a large capacitance that will consume more power. As a result, the power consumption must also be normalized by the sensitivity factor λ.

Power and Parasitic Capacitance Tradeoff

One final caveat is the parasitic capacitance associated with an interface circuit. This merits special attention because as discussed previously, parasitic capacitance for a two chip solution versus a single chip solution can be several orders of magnitude higher. As before, parasitic capacitance will directly tradeoff with power and as such, the power consumption must be normalized to the total parasitic capacitance. As we discussed previously, we prefer to work with the device sensitivity as this directly is proportional to sense capacitance[20].

We therefore need a method to convert the device parasitic capacitance to an equivalent sensitivity factor. This can be accomplished

[20] Since we have used the device sensitivity to normalize SNDR, it is prudent to use the same variables to minimize errors. Furthermore, not all parameters are reported in literature reviews but sensitivity is often documented.

by looking at the ratio of device sensitivity to sense capacitance. By comparing several devices, this ratio is determined to be approximately $100-200$. In other words, for every fF of capacitance change, a device nominal capacitance would be $100-200$ fF or there is a $0.5-1\%$ change in sense capacitance per unit of g. If we take an average of 150, then we can scale the power by the following factor:

$$\text{Power}_{factor} = \lambda + \frac{C_p}{150} \ . \tag{1.10}$$

Based on the discussion above, to get an apple to apple comparison, the

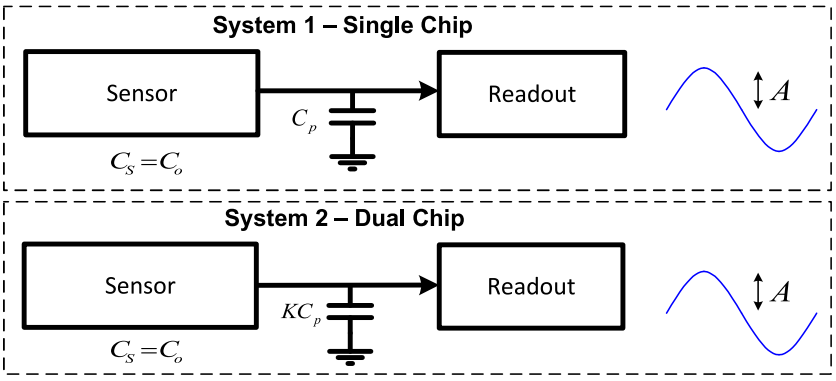


Figure 1.15: Two systems with different parasitic capacitance values between the accelerometer and the interface circuit. This would be expected in a dual chip versus single chip implementation.

power of an accelerometer system must be normalized to bandwidth and the sensitivity factor given by Eq. (1.10) [23]. As such, the normalized power is given by

$$\text{Power}_{\text{Normalized}} = \frac{\text{Power}_{\text{reported}}}{BW_{\text{system}} \cdot \text{Power}_{\text{factor}}} \ . \tag{1.11}$$

In lieu of the above discussion, we propose the following figure of merit:

$$\text{FOM} = \left(\frac{\text{SNDR}_{\text{Normalized}}}{\text{Power}_{\text{Normalized}}} \right) = \frac{\left(\frac{\text{dB}}{g} \right)}{\left(\frac{\mu W}{Hz} \right)} \ . \tag{1.12}$$

This FOM indicates that a *higher number* is better. However, since power and fidelity are very application dependent, it is better to look at this FOM graphically as is done in the literature review section.

1.4.2 Literature Review

A literature review for both open loop and closed loop systems is shown in Tables 1.1 and 1.2 respectively. This list only includes systems that successfully integrate an accelerometer with the interface circuit or report modeling of accelerometers. We avoid systems that are proposed for interfacing but do not include a sensor or a rigorous sensor model in reporting results. Unless specifically mentioned, parasitic capacitance for dual chip implementations are estimated to be 2500 fF and 100 fF for single chip implementations. The reference device sensitivity for calculating the normalized SNDR is 4.5 fF/g. The FOM value shown as a single number is a poor indicator and it is better to look at the FOM as a plot which is done in the next section.

Reference	Group	Year	Sensitivity (fF/g)	Full Scale (pk-pk g's)	Bandwidth (Hz)	SNDR (dB)	Power (mW)	FOM $\left(\frac{\text{dB}}{\text{g}}\right)\left(\frac{\text{Hz}}{\mu\text{W}}\right)$
[24]	Amini, S.B	2017	4.5	8	62.5	54	0.64	3.723
[25]	Wu, J.	2004	1.6	6	580	20	30.0	0.627
[26]	Amini, B.V.	2004	200	2	75	57.4	6.0	0.0871
[27]	Lee, W.F.	2008	20	100	500	45	10.0	0.0136
[28]a	Paavola, M.	2011	200	8	25	69	0.224	0.2336
[28]b	Paavola, M.	2011	200	8	1	72	0.02	0.1092
[29]	Tan, S.S.	2011	1.2	4	500	43.7	5.148	21.13

[24] Commercial surface micromachined accelerometer, dual chip implementation, parasitic capacitance of 2.5 pF.

[25] Single chip implementation, parasitic capacitance of 80 fF. Uses a custom accelerometer with two sets of changing sense capacitors (four sense capacitors in total). Full scale range of ± 6 g is harmonically limited with THD of -20 dB. No other SNDR information given, using this as the SNDR value. The resonant frequency of sensor cited as 5.8 KHz; as such, bandwidth is estimated at 580 Hz.

[26] Reports noise floor of 110 $\mu\text{g}/\sqrt{\text{Hz}}$ in a 1 Hz bandwidth. Using reported bandwidth of 75 Hz, SNDR is calculated to be 57.4 dB.

[27] Custom accelerometer with four sense capacitors. SNDR is distortion limited by the even harmonic and estimated (from graphs) to be 45 dB.

[28] Dual chip implementation, parasitic capacitance estimated to be 2.5 pF. Does not include any frequency measurements. Based on DC noise floor, claims 73 dB dynamic range. At full scale, assuming systems is not harmonically limited, this translates to 69 dB SNDR.

[29] Single chip with custom accelerometer but ambiguous on test setup. System noise floor at full scale from graphs estimated to be 200 $\mu\text{g}/\sqrt{\text{Hz}}$ (claims 54 $\mu\text{g}/\sqrt{\text{Hz}}$) giving 43.7 dB SNR.

Table 1.1: Open loop systems literature review.

Reference	Group	Year	Sensitivity (fF/g)	Full Scale (pk-pk g's)	Bandwidth (Hz)	SNDR (dB)	Power (μW)	FOM $\left(\frac{\text{dB}}{\text{g}}\right)\left(\frac{\text{Hz}}{\mu\text{W}}\right)$
[30]	Lemkin, M.	1999	6.1	24	100	74	135.0	0.0046
[31]	Petkov, V.	2005	22.5	2	100	53.5	13.0	0.0549
[32]	Kulah, H.	2006	19400	2.2	1000	120	7.2	0.9324
[33]	Amini, B.V.	2006	5000	1	500	95	4.5	2.368
[34]	Condemine	2005	210	6	50	50	2.64	0.0763
[35]	Pastre	2009	393	11	300	96	12.0	0.0509
[36]	Sönmez	2014	168	40	250	101	16.7	0.0215

[30] Paper is missing some information, SNDR results obtained from the author's thesis [37]. Sensitivity found by using device dimensions.

[31] Design is extensively tested for gyroscopes with mention of use for accelerometers. For accelerometers, system noise floor is cited as 150 $\mu\text{g}/\sqrt{\text{Hz}}$ for 1 g DC input and 100 Hz bandwidth resulting in 53.5 dB SNR. Used sensor mass of 7.5 μgrams to estimate sensitivity.

[32] Bandwidth is ambiguous, resonant frequency of accelerometer given as 1 KHz, taking half this for the bandwidth. Group uses a very specialized post process custom bulk accelerometer extensively reported in [38] where device sensitivity value was obtained.

[33] Only measures dynamic range of 95 dB and unclear how this was measured. Used dynamic range value as SNDR although likely overestimating system linearity.

[34] Sensitivity of device estimated based on the noise floor and sensitivity of similar devices. SNDR and full scale range are not specifically reported; therefore, values are estimated from Fig. 13.6.2 of paper.

[35] Sensitivity of device estimated based on the noise floor and sensitivity of similar devices.

[36] Uses a bulk micromachined accelerometer to lower mechanical noise floor below electronic noise floor.

Table 1.2: Closed loop systems literature review.

1.4.3 *Figure of Merit Comparison*

A graphical representation of the figure of merit is shown in Fig. 1.17 with normalized fidelity on the x-axis and normalized power on the y-axis. The better performing interface circuits are those that achieve a higher relative fidelity compared to power consumption and are at the lower right corner of the plot.

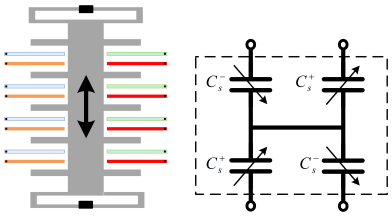


Figure 1.16: Dual differential accelerometer with two sets of changing sense capacitors.

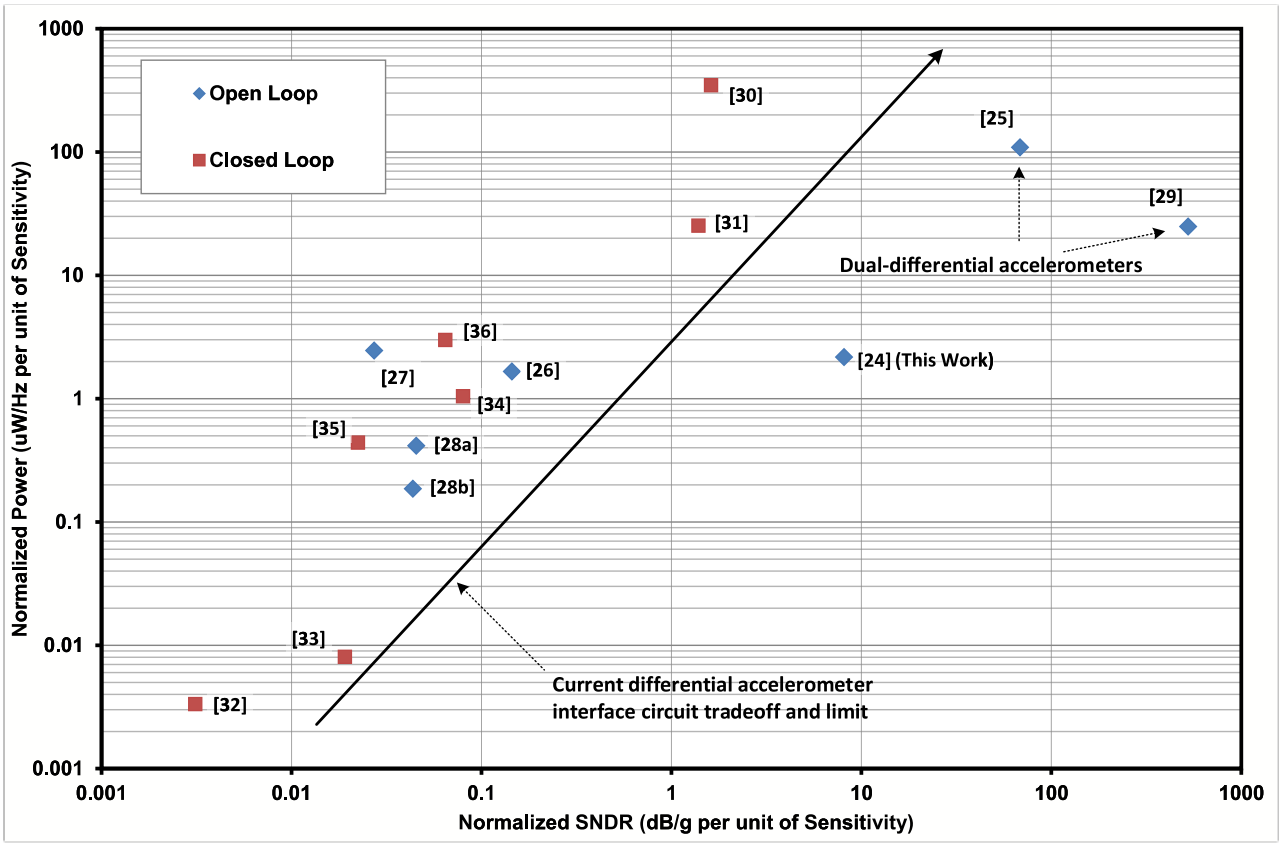


Figure 1.17: Literature review in graphical form.

This plot shows that regardless of the type of interface circuits used, when normalized for device sensitivity, current interface circuits follow a defined tradeoff between power and fidelity for differential accelerometers. References [25] and [29] are dual-differential accelerometers as shown in Fig. 1.16 and the better performance can be attributed to the better adaptability of these sensors to high precision circuitry. These sensors are also expensive to manufacture and not easily adaptable to dual direction (x, y) and three direction (x, y and z) sensing[21].

[21] For example, one may be able to build the sensor as shown in Fig. 1.16 in the x-direction but resort to a simple single-ended structure in the y-direction.

As shown, the architecture proposed and prototyped in this work [24] fundamentally shifts the tradeoff of the curve to the right achieving a better fidelity at comparable power.

2

Review of Capacitive Accelerometer Readout Techniques

Capacitive accelerometers make use of variable capacitors to detect accelerations. Since the capacitance is not fixed, then signals generated by these capacitors have two components, namely displacement measurement and velocity measurement. Depending on the type of sensor, the circuitry should ensure that one of these components dominates. For capacitive accelerometers, displacement measurement must dominate over velocity measurement. These concepts are explored in more detail in **Section 2.1**.

Readout circuits can be organized into three broad areas. These are current detection, voltage detection, and charge detection. Each of these circuit techniques has many design choices and active areas of research which are briefly reviewed in **Sections 2.2-2.4**. For each readout type, the minimum detectable signal or the capacitive resolution is developed based on the parasitic and sense capacitances. The analysis indicates that for accelerometers with low sense capacitance[1], current and voltage based measurements bode well in low parasitic capacitance environments and charge based circuits are superior when high parasitic capacitances are present. Since the proposed solution is dual chip, which we expect will have high parasitic capacitances, our proposed solution in Chapter 3 will be charge based.

[1] as is expected of low cost surface micromachined accelerometers

The format of the output signal generated through an interface circuit has direct effect on the fidelity of the signal. **Section 2.6**

looks at the possible outputs that interface circuits can achieve and the limitations and benefits of each. It is shown that *a ratiometric charge balanced* design achieves the best possible signal fidelity and this is the ideal output to aim for in any circuit implementation.

2.1 The Subtleties of Capacitance Measurement

As discussed in the previous section, all capacitive sensors consist of a variable capacitor or a set of differential variable capacitors which change in response to a measurand. To measure the measurand, we require to take this change in capacitance and convert it into a voltage or current and do some more processing before we output a value. Often this measurand is acceleration but can be any other environmental factor that causes acceleration. We can intuitively understand the process by taking the fundamental equation for a capacitor, mainly

$$\Delta Q = C\Delta V \ , \tag{2.1}$$

where ΔQ is the charge placed on a capacitor C due to a potential difference ΔV. We can convert this charge to an equivalent current by noting that electrical current is the time derivative of charge. Therefore, we have

$$\begin{aligned} i_c(t) &= \frac{\delta\left[C(x)V\right]}{\delta t} \\ &= C(x)\frac{\delta V(t)}{\delta t} + V(t)\frac{\delta C(x)}{\delta t} \ , \end{aligned} \tag{2.2}$$

where $C(x)$ is now a variable capacitor depending on a displacement x. As it can be seen, the current that a capacitor exhibits has two components: a component based on the change in voltage and proportional to the nominal capacitance value and a component dependent on the changing capacitance and proportional to the supply voltage

We pause here and make a few observations about these two components. The first term above is the component of current due to a changing voltage and this term is encountered often in linear circuit analysis. We call this term the *displacement measurement*. The displacement measurement is proportional to the nominal capacitance and

therefore, it is always advantageous from a mechanical point of view to design devices with as large of a nominal capacitance as possible[2].

[2] larger capacitance means larger output signal which would then be easier to detect and measure.

The second term in the equation above is called the *velocity measurement*. It is the component of current due to a changing capacitance and this term is rarely seen in linear circuit analysis because we generally assume the capacitance to be constant and hence, the change in capacitance term will be zero. The velocity measurement is also proportional to the bias voltage which the capacitance is under. This suggests that we can make the bias voltage arbitrary large and get larger current and better performance. There is, however, a fundamental limit to this voltage known as the pull-in effect [13] as well as the supply voltage of our system.

The term velocity measurement may be peculiar to the reader but it can be more clearly demonstrated if we expand the second term. If we split the second term into two parts we will have

$$i_c(t) = C(x)\frac{\delta V}{\delta t} + V\frac{\delta C(x)}{\delta x}\frac{\delta x}{\delta t} \ . \tag{2.3}$$

Now working out the capacitive derivative we get

$$\begin{aligned}\frac{\delta C(x)}{\delta x} &= \frac{\delta\left(\frac{A\epsilon\epsilon_o}{d-x}\right)}{\delta x} \\ &= -\frac{A\epsilon\epsilon_o}{(d-x)^2} \ ,\end{aligned} \tag{2.4}$$

where A is the effective parallel plate area of the capacitor, d is the nominal distance between the parallel plates, ϵ_o is the permittivity of free space and ϵ is the relative permittivity of the medium. If we assume $d \gg x$, then we can simplify the capacitive derivative to an almost constant term

$$\frac{\delta C(x)}{\delta x} \approx -\frac{A\epsilon\epsilon_o}{d^2} \ , \tag{2.5}$$

and the current then simplifies to

$$i_c(t) = C(x)\frac{\delta V}{\delta t} - V\frac{A\epsilon\epsilon_o}{d^2}\frac{\delta x}{\delta t} \ . \tag{2.6}$$

Therefore, the second term is approximately proportional to the ve-

locity of the moving mass. This type of measurement is useful for certain type of sensors that work on measuring mechanical frequency - environmental variables causing a specific desired frequency. The perennial example for this is a mechanical microphone. Generally though, most acceleration based sensors rely on displacement measurement. To see this more clearly, we expand the term $C(x)$ as follows:

$$C(x) = \frac{C_s}{1 - \frac{x}{d}} \tag{2.7}$$

$$\approx C_s(1 + \frac{x}{d}) \tag{2.8}$$

$$\approx C_s + \frac{C_s}{d}x \ . \tag{2.9}$$

Therefore, a displacement measurement is proportional to acceleration which is what we would like to measure. The key takeaway from the above analysis is that depending on the sensor, one of the measurement types (displacement or velocity) must dominate. If we assume that we are interested in displacement measurement, then we need to maximize the ratio

$$\max\left(\frac{C(x)\frac{\delta V}{\delta t}}{V\frac{A\epsilon\epsilon_o}{d^2}\frac{\delta x}{\delta t}}\right) \tag{2.10}$$

$$= \frac{\frac{\delta V}{\delta t}}{\frac{V}{d}\cdot\frac{\delta x}{\delta t}} \ . \tag{2.11}$$

Generally, accelerometers are designed for low frequency applications (see Appendix D). Therefore, by choosing a relatively large modulation frequency, the displacement current dominates and errors from velocity measurement are minimized[3]. The conclusion of this section is that in capacitive accelerometer readout circuits, the displacement measurement must be dominant. This often is not specifically mentioned in literature but is well documented if correct analysis is performed.

[3] To the extend of being lower than the intended fidelity of the readout circuit

In the following sections, we look at various displacement based measurement circuit topologies and the minimum signal that each can detect.

2.2 Current Sensing

2.2.1 Theory of Operation

In current sensing, each sense capacitor electrode is driven by an anti-phase modulating signal with frequency f_m and amplitude V_m. The current induced by a change in capacitance due to acceleration is then converted to a voltage. Fig. 2.1 shows a single-ended configuration of this setup.

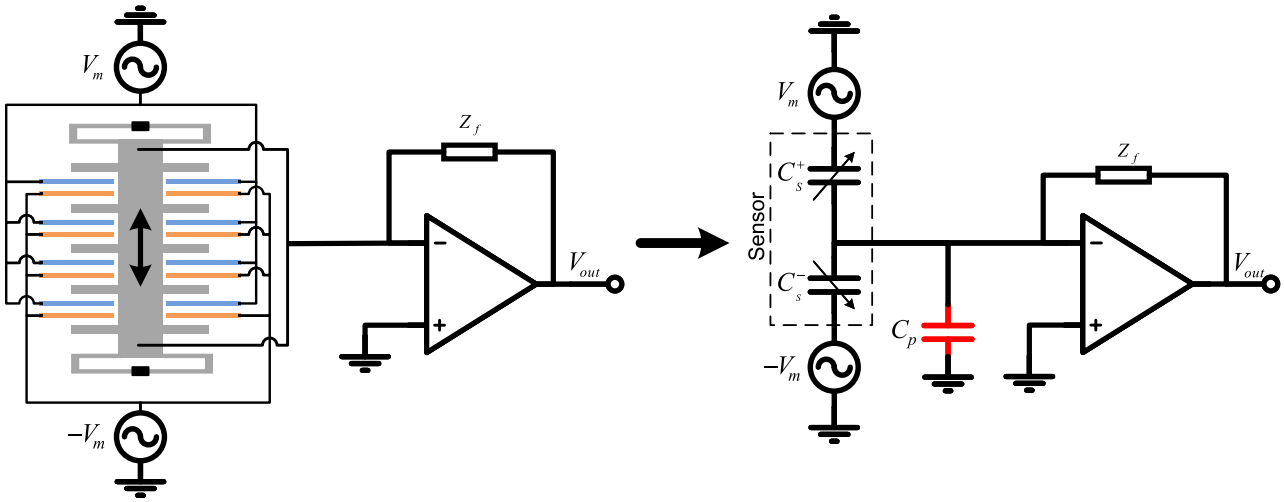


Figure 2.1: Simplified current based interface circuit for differential accelerometers.

The feedback impedance, Z_f, is generally a resistance and a capacitance in parallel. Assuming an ideal op-amp, the output of this circuit in the time domain is given by

$$\begin{aligned} V_{out}(t) &= \Delta C Z_f \frac{\delta V_m \sin(2\pi f_m t)}{\delta t} \\ &= \Delta C Z_f V_m \frac{\delta \sin(2\pi f_m t)}{\delta t} \\ &= 2\pi f_m \Delta C Z_f V_m \cos(2\pi f_m t) \ . \end{aligned} \tag{2.12}$$

where $\Delta C = C_s^+ - C_s^-$. Therefore, the output is an amplitude modulated signal as shown in Fig. 2.2. When combined with an ADC, the system takes the form shown in Fig. 2.3.

The envelope represents the change in capacitance which is also changing in time forming an amplitude modulated (AM) signal. Note that it is possible that the change in capacitance is constant (representing a

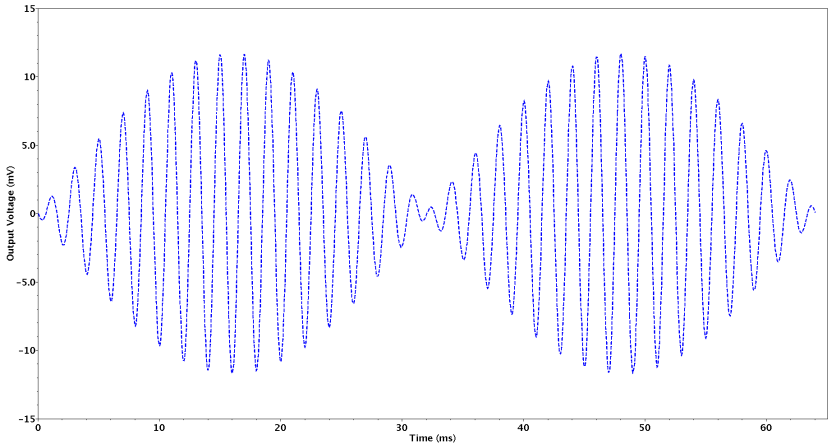


Figure 2.2: Transient response of a transimpedance interface circuit for a differential accelerometer.

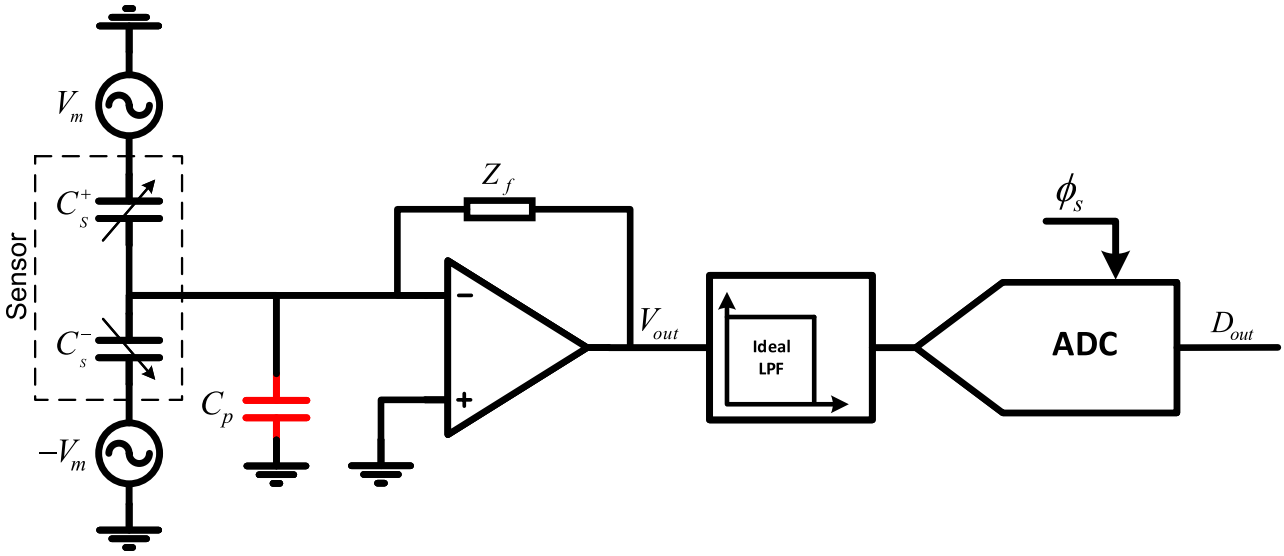


Figure 2.3: Simplified current based interface circuit with an ADC stage for digitization.

constant acceleration). In such a case, the output is simply a sine wave whose amplitude is proportional to acceleration.

The current sensing can further be divided into transresistance amplifiers (TRA's) where the feedback resistance dominates over the capacitance or the transcapacitance or charge-sensitive amplifiers (CSA's) where the feedback capacitance dominates over the resistance. CSA's are more prevalent because integrated capacitors offer better linearity compared to their resistor counterparts. With a CSA, the resistance value must be maximized to lower noise [39]. The implementation of a resistor then becomes a challenge because polysilicon based resistors

consume a large area as well as having large parasitic capacitances associated with them. Typical solutions then involve using a MOSFET in the cutoff region [40].

2.2.2 Minimum Detectable Signal - Current Based

Determining the minimum detectable capacitance for transimpedance amplifiers is involved and we will only work on a simplified circuit as shown in Fig. 2.4. More details on this can be found in [41].

As before, we have the sense capacitors driven by two anti-phase signals. The output voltage is then given as

$$|V_{out}| = 2\pi f_m V_m Z_f \Delta C \ . \tag{2.13}$$

However, the pole associated with Z_f limits the bandwidth. Moreover, the amplifier dominant pole creates an inductive effect resulting in a potential resonance and larger bandwidth. The maximum output voltage is obtained at the resonance which yields the optimal drive frequency and minimum detectable capacitance as

$$f_{\text{drive optimal}} = \sqrt{\frac{\text{GBW}}{2\pi Z_m \left(2C_s + C_p\right)}} \ , \tag{2.14}$$

$$\Delta C_{min} = \frac{\sqrt{\text{BW}}}{V_m} \sqrt{\frac{2k_B T(2C_s + C_p)}{\pi \cdot \text{GBW}}} \tag{2.15}$$

where k_B is Boltzmann's constant, BW is the bandwidth of the system and GBW is the gain bandwidth product of the op-amp used. The minimum detectable signal for the TRA is plotted in Fig. 2.5.

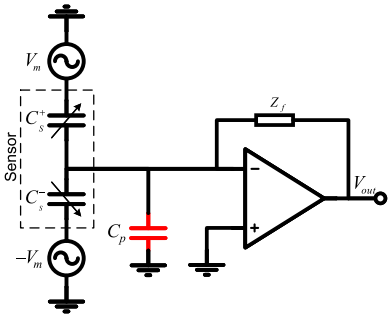


Figure 2.4: Current based interface circuit used for noise analysis.

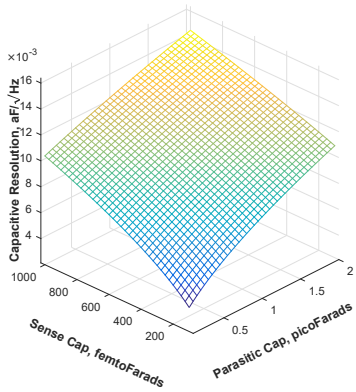


Figure 2.5: Minimum detectable capacitance as a function of parasitic and sense capacitance for the transimpedance amplifier where GBW = 50 MHz and V_m = 1.0 V

2.3 Voltage Sensing

2.3.1 Theory of Operation

In a displacement based voltage sensing configuration, both ends of the fixed electrodes are driven with a high frequency AC signal and the moving mass is connected to a unity gain buffer. An acceleration then

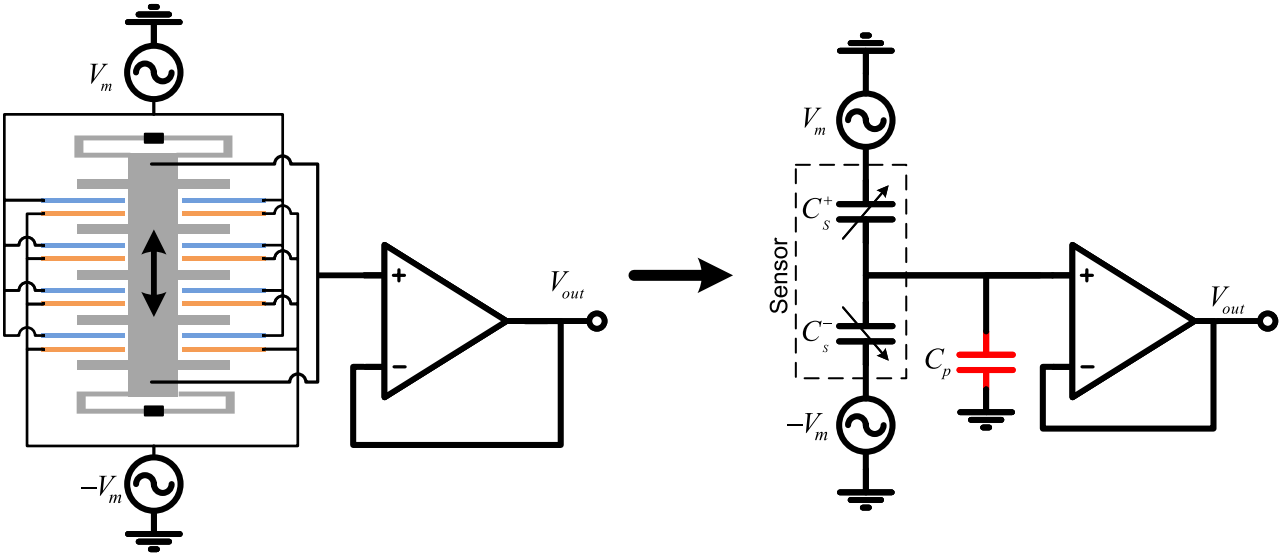


Figure 2.6: Simplified voltage based interface circuit for differential accelerometers.

causes a differential current to flow to the buffer such that

$$i_c^+ + i_c^- = 0 \ . \tag{2.16}$$

Recall that for capacitive sensors, the current is given by two components:

$$i_c(t) = C(x)\frac{\delta V(t)}{\delta t} + V(t)\frac{\delta C(x)}{\delta t} \ . \tag{2.17}$$

For our purposes, we assume that the velocity portion[4] is relatively small. Therefore,

[4] as contained in $\frac{\delta C(x)}{\delta t}$ according to Eq. (2.3)

$$\frac{\delta\left[C_s^+(x)\left(V_m\sin(\omega t) - V_{out}\right)\right]}{\delta t} + \frac{\delta\left[C_s^-(x)\left(-V_m\sin(\omega t) - V_{out}\right)\right]}{\delta t} = 0 \tag{2.18}$$

$$\frac{\delta(V_{out})}{\delta t}\left(C_s^+(x) + C_s^-(x)\right) = V_m\cos(\omega t)\cdot\omega(C_s^+(x) - C_s^-(x)) \tag{2.19}$$

$$\int\frac{\delta(V_{out})}{\delta t} = \int\left[V_m\cos(\omega t)\cdot\omega\left(\frac{C_s^+ - C_s^-}{C_s^+ + C_s^-}\right)\right] \tag{2.20}$$

$$V_{out} = \frac{C_s^+ - C_s^-}{C_s^+ + C_s^-}V_m\sin(\omega t) \ , \tag{2.21}$$

where $V_m\sin(\omega t)$ is termed the modulating signal and as with the case

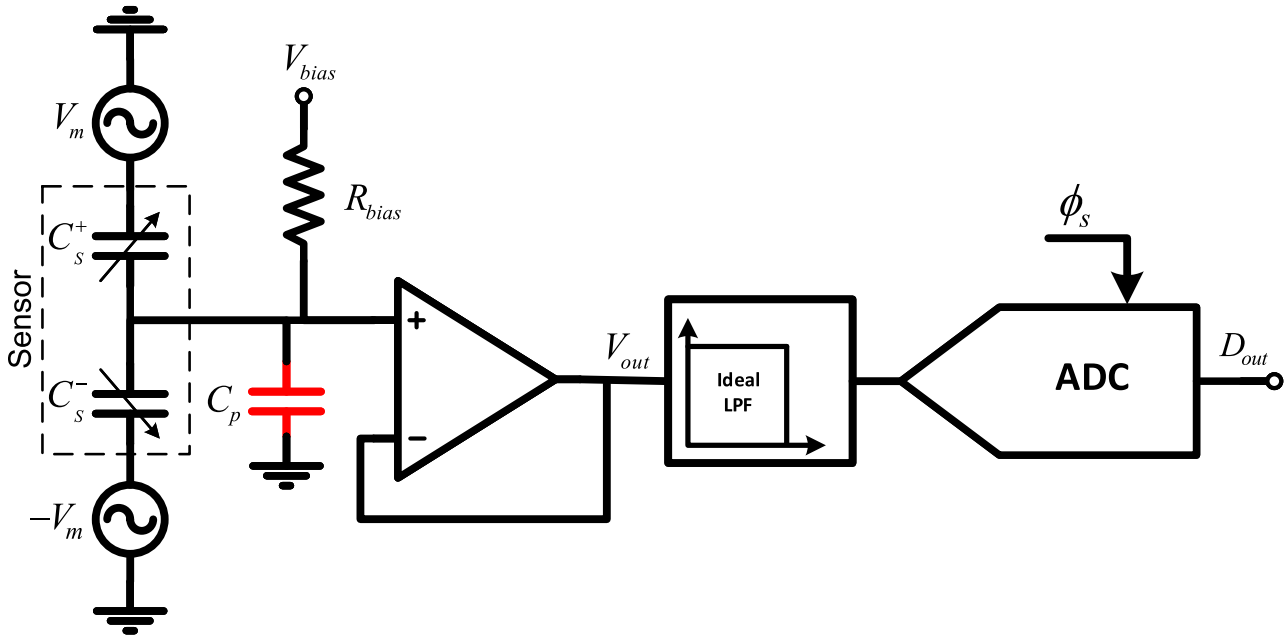


Figure 2.7: Simplified voltage based interface circuit with an ADC stage for digitization.

of the current based readout, the output is an amplitude modulated signal. Accordingly, the outline of the curve represents the input acceleration which can be obtained using a demodulation technique. Note that the above formula is exact and no simplifications have been made in its development. Therefore, for a differential accelerometer, the ideal output is perfectly linear[5] even though the capacitance change is not. The displacement x is also linearly proportional to acceleration as long as the frequency of acceleration is well below the resonant frequency and is given by

$$x(t) = \frac{m}{k}a(t) = \frac{1}{\omega_n^2}a(t) \ . \tag{2.22}$$

where $a(t)$ is the acceleration, k is a spring constant associated with the mass m of the accelerometer and ω_n is the natural frequency of the device.

The situation presented above has rather been idealized. Two very important details have been left out: the biasing for the op-amp and the parasitic capacitance at the input of the op-amp. A typical biasing scheme with the associated parasitic capacitance is shown in Fig. 2.7. Taking into account these two parameters, we can rederive the output

[5] to a first order

equation as

$$V_{out} = \frac{s(C_s^+ - C_s^-)R_{bias}}{1 + s(C_p + C_s^+ + C_s^-)R_{bias}} V_m \ . \tag{2.23}$$

where C_p is the parasitic capacitance at the moving electrode of the accelerometer and R_{bias} is a biasing resistor to set the DC voltage for the operation of the amplifier. The output now represents a high pass filter with corner frequency at $f_c = \frac{1}{(Cp+C_s^+-C_s^-)R_{bias}}$ and a zero at the origin. The corner frequency therefore shifts lower with larger biasing resistance. For maximum sensitivity, we would like to operate on the flat region of the curve where the gain is maximum and given as

$$V_{out} = \frac{C_s^+ - C_s^-}{C_p + C_s^+ + C_s^-} V_m \ . \tag{2.24}$$

To be on the flat region of the curve, we must have $s(C_p + C_s^+ + C_s^-)R_{bias} \gg 1$. This can be achieved by either having higher frequency for the modulating signal V_m or higher biasing resistance, R_{bias}. Therefore, there is a tradeoff between the size of the biasing resistor and the frequency of the modulating signal. With a higher modulating signal, a smaller resistor can be used but this leads to higher power consumption. A smaller frequency can be use with higher biasing resistance but this leads to implementation issues using on-chip poly-resistors [42]. To overcome this problem, reverse connected diodes [43] or subthreshold MOSFETs [44] [45] [46] can be used. Examples where poly-resistors are used (at high modulation frequencies) can be seen in [47] and [48].

Assuming that a proper biasing resistor and modulating frequency are chosen so that we are operating in the flat region of the output curve, there is still a major issue with the parasitic capacitance that heavily reduces the sensitivity. Two possible solutions are available. One technique is known as bootstrapping where the parasitic capacitance is fed back to the output of the amplifier as shown in Fig. 2.8 [49] [50]. This technique can only be used for single chip applications where the parasitic capacitance of the bulk is accessible to the electronic circuitry. The other option requires the use of a high negative gain in the forward path as shown in Fig. 2.9 [51]. Other topics in this area include challenges in demodulation [6] [52] [25] [53] which we will not delve into but are active

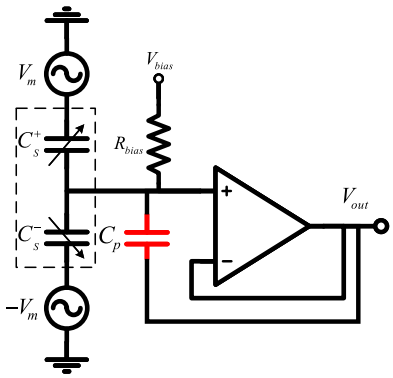


Figure 2.8: Bootstrapping technique to reduce the effect of parasitic capacitance

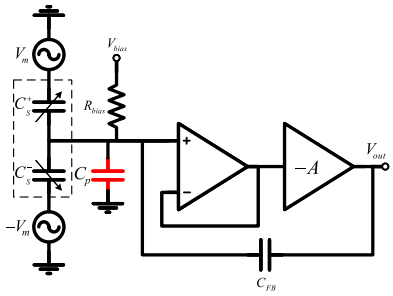


Figure 2.9: Feedforward gain technique to reduce the effect of parasitic capacitance

[6] Also applicable to current based circuits

areas of research.

2.3.2 Minimum Detectable Signal - Voltage Based

For simplicity, we will use the basic configuration of the voltage amplifier as shown in Fig. 2.10 to develop a model for the minimum detectable capacitance of these circuits. The output of the buffered signal for this simplified circuit is given by

$$V_{out} = V_m \frac{\Delta C}{2C_s + C_p} \ . \tag{2.25}$$

The above output is achieved after a demodulation step; therefore, to increase the minimum detectable capacitance, we need to increase the AC signal beyond the 1/f noise frequency of the amplifier as well as increase V_m. It is rather straightforward to define the minimum detectable voltage based measurements as

$$\Delta C_{min} = \left[\frac{2C_s + C_p}{V_m}\right] V_{n,rms}\sqrt{BW} \ , \tag{2.26}$$

where $V_{n,rms}$ is the input-referred thermal noise floor of the amplifier given by

$$V_{n,rms} = \frac{16k_BT}{3g_{m1}} n_f \ . \tag{2.27}$$

Here, g_{m1} is the transconductance of the input pair and n_f is a noise factor meant to capture the noise due to other transistors and stages of the op-amp. n_f typically ranges from 1-5 depending on the op-amp topology used. Based on the above, the minimum detectable capacitance for the voltage amplifier is plotted in Fig. 2.11.

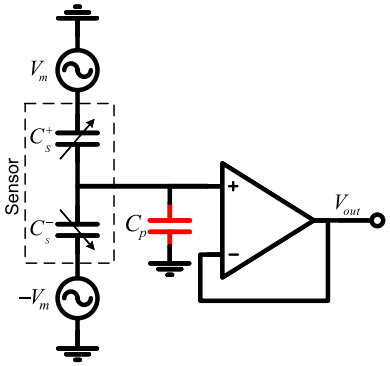


Figure 2.10: Voltage based interface circuit used for noise analysis.

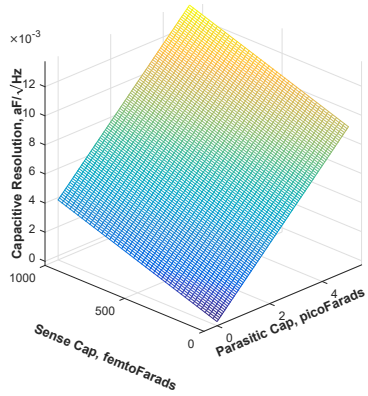


Figure 2.11: Minimum detectable capacitance as a function of parasitic and sense capacitance for the voltage amplifier where $g_m = 0.1$ mA/V and $V_m = 1.0$ V.

2.4 Charge Sensing

2.4.1 Theory of Operation

It can be argued that charge sensing is well adapted for interfacing with capacitive sensors. The basic charge sensing structure can be defined as a switched capacitor resetting integrator as shown in Fig. 2.12. Without feedback, an integrator output grows indefinitely in theory and to the rails in practice. To overcome this problem, the integrator is "reset"

every N cycles. The resetting essentially biases the op-amp periodically for proper operation. Without this periodic reset, DC current cannot flow in the circuit and operating points of the transistors cannot be set to the correct mode.

It is important to note that switched capacitor circuits such as the one shown in Fig. 2.12 transform a continuous time signal to a discrete time signal in which case the bandwidth is no longer unlimited but limited by the Nyquist criterion $f_s/2$ [54]. This is generally not an issue when it comes to accelerometer applications where bandwidths range from a few Hertz to a few hundreds of Hertz.

When the resetting is equal to half the sampling frequency, the integrator becomes a switched capacitor amplifier. The design approach for these circuits is to then maximize the output voltage to ensure that the ADC following the conversion is relatively low power. The feedback capacitor, C_f, would then be implemented with a programmable capacitor array that based on the input level adjusts the output to get the

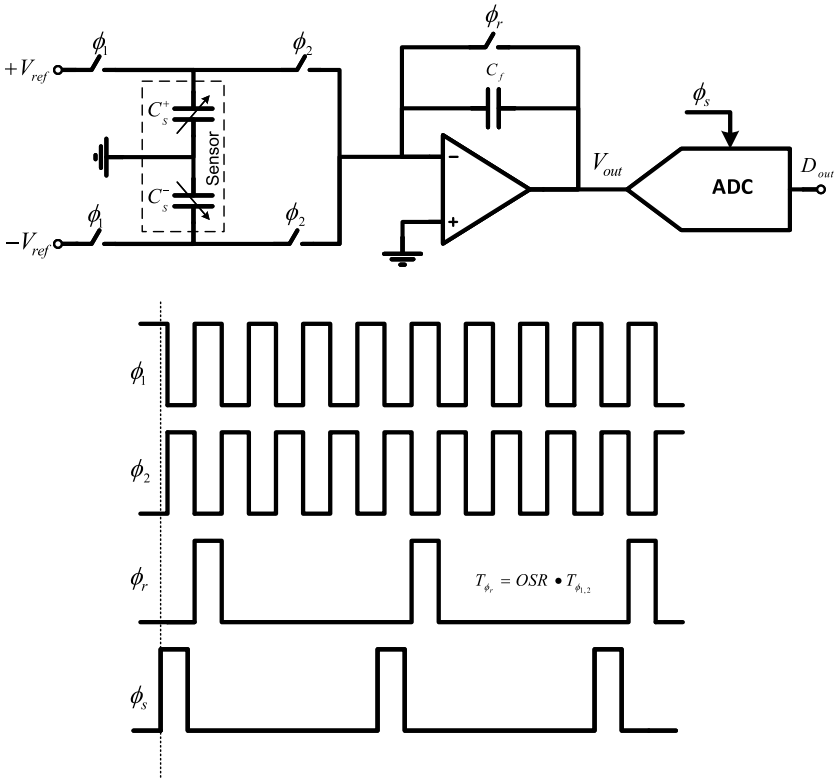


Figure 2.12: A resetting integrator with sense capacitors used as sampling capacitors. *Notice that this interface circuit is not parasitic capacitance insensitive.*

same peak to peak voltage. With SC circuits, the main challenge lies in removing low frequency noise using either chopper stabilization or correlated double sampling [55]. These techniques become difficult to implement with the physical structure of the accelerometer that limits accessibility to nodes of the sense capacitors.

2.4.2 Minimum Detectable Signal - Charge Based

By re-arranging the equation for the output of a charge amplifier, the change in capacitance is given by

$$\Delta C = \frac{V_{\text{out}}}{V_m} C_f \ , \tag{2.28}$$

where C_f is the feedback capacitor shown in Fig. 2.12. To find the minimum detectable capacitance, the output voltage must be replaced by the output noise voltage of the circuit. The total noise of a switched capacitor amplifier can be written as the sum of the noise due to switch resistances and noise due to the amplifier. For the switch noise, the robust noise analysis is complex and would need to include the bandwidth limitations of the op-amp. A good approximation, however, is to assume that the switch noise in both ϕ_1 and ϕ_2 phases add equally [56] [57]. In this case we have

$$V^2_{\text{no, switches}} = 2 \times \left(k_B T \frac{2C_s}{C_f^2} + k_B T \frac{C_p}{C_f^2} + \frac{k_B T}{C_f} \right) \ , \tag{2.29}$$

where the factor two indicates the two phases and the three components are due to the input and feedback switches. The input-referred op-amp noise is given by [54]

$$V^2_{ni,op-amp} = \frac{16 k_B T}{3 g_m} n_f \left(\frac{1}{4\tau} \right) , \tag{2.30}$$

where $1/\tau$ is the effective bandwidth of the op-amp given by $\frac{\beta g_m}{C_o}$. For a Miller compensated op-amp, C_o is equivalent to the compensation capacitor C_c. For a single stage op-amp, it is the load capacitance given by

$$C_o = \frac{(2C_s + C_p) C_f}{2C_s + C_f + C_p} \ , \tag{2.31}$$

and β is the feedback coefficient given by

$$\beta = \frac{C_f}{2C_s + C_p + C_f} \ . \tag{2.32}$$

Assuming a load capacitance given by Eq. (2.31)[7], the noise due to amplifier simplifies to

$$V^2_{ni,op-amp} = \left(\frac{4}{3}\right) \frac{k_B T}{2C_s + C_p} n_f \ , \tag{2.33}$$

and the minimum detectable capacitance is given by

$$\Delta C_{min} = \sqrt{\frac{1}{f_s}\left[\frac{4}{3}\frac{k_B T G^2}{2C_s + C_p} n_f + 2\frac{k_B T}{C_f}\left(1 + \frac{2C_s}{C_f} + \frac{C_p}{C_f}\right)\right]} \tag{2.34}$$

where $G = \left(1 + (2C_s + C_p)/C_f\right)$ is the gain from the input to the output. Although the above equation is accurate, there are many techniques that can significantly reduce several of the noise components. The noise due to the feedback capacitor, for example, can be sampled and deducted from the output with correlated double sampling [59]. As such assuming that the switch noise is lowered significantly below the amplifier noise, then the minimum detectable signal can be simplified to

$$\Delta C_{min,CDS} = \sqrt{\frac{1}{f_s}\left[\frac{4}{3}\frac{k_B T G^2}{2C_s + C_p} n_f + 2\frac{k_B T}{C_f}\left(\frac{2C_s}{C_f} + \frac{C_p}{C_f}\right)\right]} \ . \tag{2.35}$$

Using Eq. (2.35), the minimum detectable capacitance with respect to parasitic and sense capacitance is plotted in Fig. 2.13.

[7] Regardless of the op-amp architecture, the Miller compensation capacitor and the effective load capacitance will be in the same range [58]. Using Eq. (2.31) leads to a better closed form equation for total noise of the op-amp.

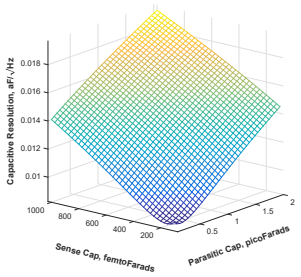


Figure 2.13: Minimum Detectable capacitance as function of parasitic and sense capacitance for a switched capacitor amplifier.

2.5 *Analysis of Interface Circuit Topologies*

Fig. 2.14 plots the minimum detectable capacitance for the three types of interface circuits for a low sensitivity accelerometer where $C_s = 500$ fF. There is an inflection point around 1.2 pF which is very close to the bondwire parasitic capacitances that is present in dual chip interface circuits. The voltage amplifier provides the best performance for low parasitic capacitance applications which would be expected from single packaged interface circuits. On the other hand, for large parasitic capacitance applications, such as two chip implementations, switched

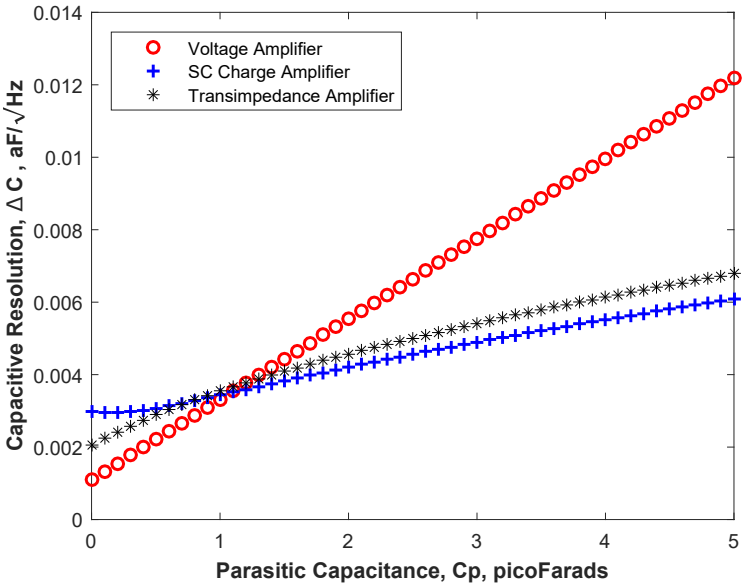


Figure 2.14: Comparison of the minimum detectable capacitance for the three interface topologies as a function of parasitic capacitance. Notice that for large parasitic capacitance, the switched capacitor topology achieves the best results. The crossing point for the three topologies will highly depend on the design choices, but the general form of these crossings will always be consistent.

capacitor circuits achieve the best performance.

Therefore, although this analysis has been greatly simplified[8], a general conclusion can be made that switched capacitors circuits are an attractive solution where large parasitic capacitances are expected.

[8] The topic of this section by itself can serve as a self containing project

2.6 Displacement Based Measurement Output Types

This section looks at the various types of displacement based measurements. Recall that in displacement based measurements, the rate of change of the voltage placed on the sense capacitors should be large enough to dominate over the frequency of acceleration.

2.6.1 Single Capacitor Output

Certain types of accelerometers rely on a single variable capacitor for force detection. A current based interface circuit for this type of accelerometer is shown in Fig. 2.15. In this case, using a displacement measurement, the output is given by

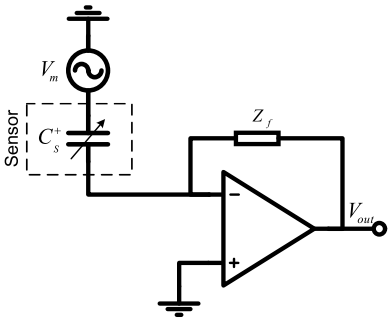


Figure 2.15: A TIA based interface circuit for single capacitor accelerometers.

$$\begin{aligned} V_{out} &= KC_s^{\pm} \\ &= K\frac{C_s}{1 \mp \frac{x}{d}} \\ &= KC_s\left(1 \mp \frac{x}{d} \mp \frac{x^2}{d^2} \mp \frac{x^3}{d^3} \mp \dots\right) \\ &\approx K\left[C_s\left(1 \mp \frac{x}{d}\right)\right] \\ &\approx K\left[C_s \mp C_s\frac{x}{d}\right] \ , \end{aligned} \tag{2.36}$$

where K is an interface circuit dependent gain factor and equal to $2\pi f_m Z_f V_m$ for the TIA shown in Fig. 2.15. A simulation of the output of the circuit is shown in Fig. 2.16. Key observations from the equation above and the simulation are:

- the desired signal is x, therefore, there is an offset proportional to C_s
- The offset is a problem. Since the signal is contained in $C_s\frac{x}{d}$, it needs to be amplified. With a large offset, this amplification will result in the saturation of the output and therefore, the offset must be removed beforehand.
- In general, it is easier and less complex to design a readout that gets rid of the offset right away rather than to try to remove it later.
- Although we simplified the output using a Taylor series, 2nd, 3rd, 4th etc harmonics exist and can potentially reduce the output linearity.

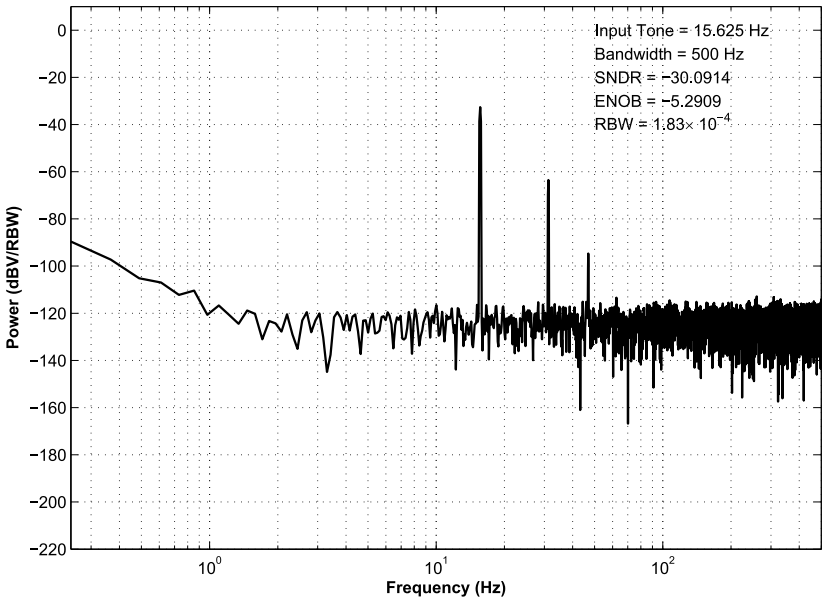


Figure 2.16: Output spectrum of a TIA interface circuit for a single capacitor accelerometer. Notice the large DC content at low frequencies.

- In single capacitor based accelerometers, the second order harmonic dominates[9].

[9] Manufacturers will often not specify whether they use single-ended structures but presence of even order harmonics in the output spectrum is a good indicator.

2.6.2 *Single Capacitor Output with Reference*

This technique tries to remedy some of the previous issues with the offset by including a reference capacitor C_R with the sense capacitor C_s^+. The same circuit can now be used by driving both capacitors with anti-phase modulating signals as shown in Fig. 2.17. The output of this circuit is now given by

$$V_{out} = K\left(C_s^{\pm} - C_R\right) \tag{2.37}$$

$$= K\left[\left(C_s - C_R\right) \mp C_s \frac{x}{d}\right] \ . \tag{2.38}$$

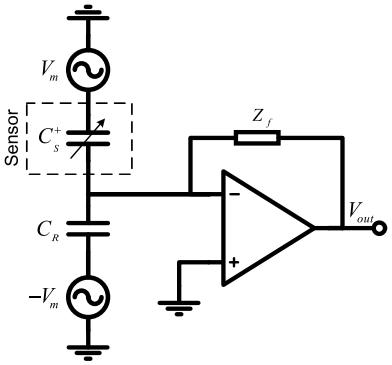


Figure 2.17: A TIA based interface circuit for single capacitor accelerometers using a reference capacitor for offset cancellation.

A simulation of the circuit is shown in Fig. 2.18. From the above

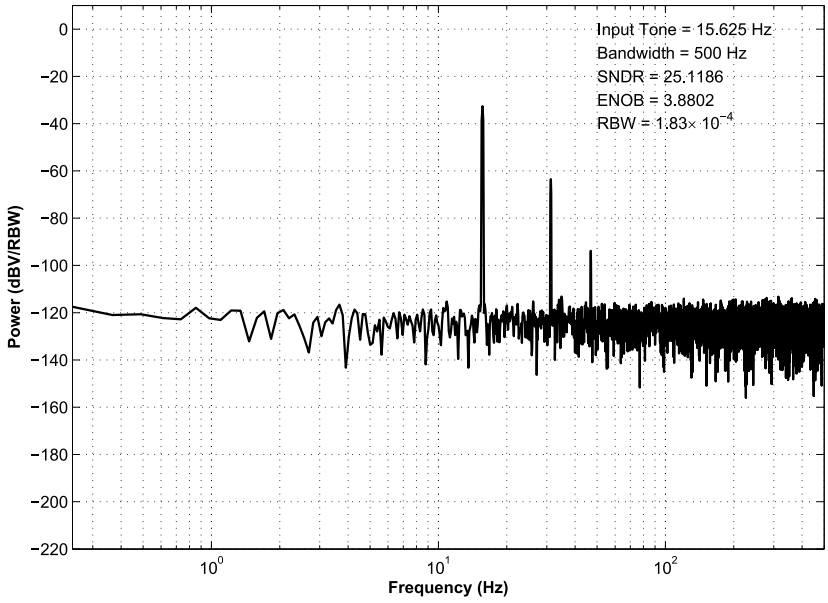


Figure 2.18: Output spectrum of a TIA interface circuit for a single capacitor accelerometer with a reference capacitor. Notice that the low frequency content (offset) is now removed.

equation and simulation results we can see that:

- The offset is greatly reduced if C_R is chosen to be approximately equal to C_s
- Harmonics still exist

2.6.3 Differential Capacitance Output

With single sense capacitor accelerometers, options are limited regarding the harmonics generated. However, single-ended accelerometers are also easier to manufacture and hence popular for low cost applications. The next step is the use of differential accelerometers. In this situation, there is a set of sense capacitors that change differentially and the difference in sense capacitors is proportional to displacement. A current based TIA interface circuit for differential accelerometers is shown in Fig. 2.19. Accordingly, the output of this circuit is given by

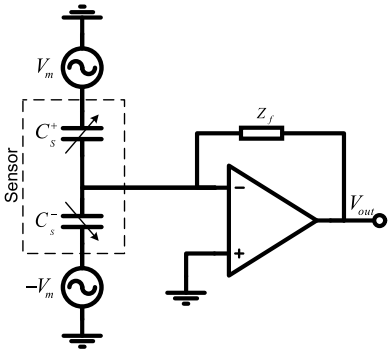


Figure 2.19: A TIA based interface circuit for differential accelerometers.

$$
\begin{aligned}
V_{out} &= K\left[C_s^+ - C_s^-\right] \\
&= K\left[\frac{C_s}{1-\frac{x}{d}} - \frac{C_s}{1+\frac{x}{d}}\right] \\
&= K\left[\frac{C_s\left(1+\frac{x}{d}\right) - C_s\left(1-\frac{x}{d}\right)}{1-\left(\frac{x}{d}\right)^2}\right] \\
&= K\left[\frac{2C_s\frac{x}{d}}{1-\left(\frac{x}{d}\right)^2}\right] \\
&= K\left[2C_s\left(\frac{x}{d}+\left(\frac{x}{d}\right)^3+\left(\frac{x}{d}\right)^5+\left(\frac{x}{d}\right)^7+\ldots\right)\right] \\
&\approx 2KC_s\frac{x}{d}\ . \qquad (2.39)
\end{aligned}
$$

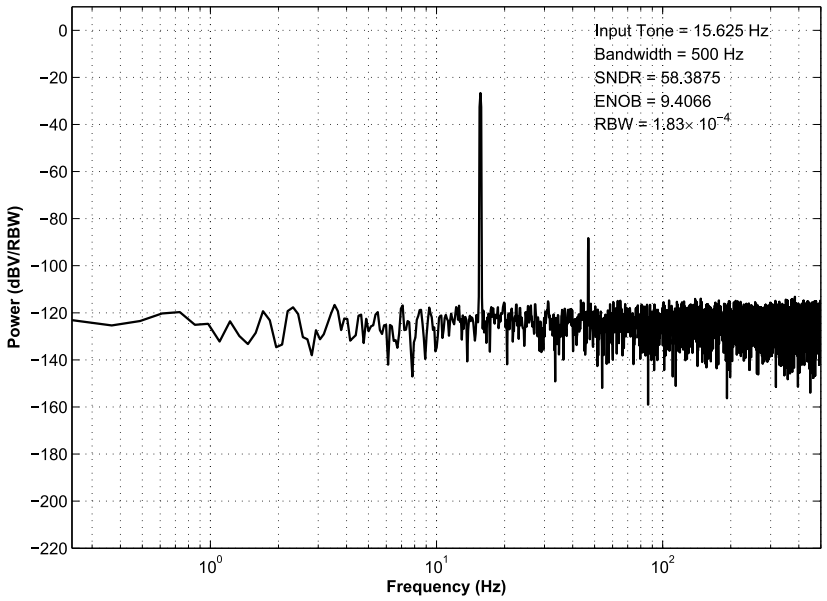


Figure 2.20: Output spectrum of a TIA interface circuit for a differential accelerometer.

A simulation of the circuit's output is shown in Fig. 2.20. The key observations from the above equations and the simulation are that:

- There is no offset in this implementation
- Even order harmonics are eliminated
- Odd order harmonics exist but are smaller compared to the single capacitor case because the power of the denominator is squared
- The gain of the circuit is effectively doubled compared to the single capacitor case

2.6.4 Ratiometric Output

Ratiometric output is an output type where the output signal is proportional to the ratio of the difference in the differential sense capacitances over the sum of sense capacitances. A voltage based circuit that achieves ratiometric output is shown in Fig. 2.21. Accordingly, the output is given by

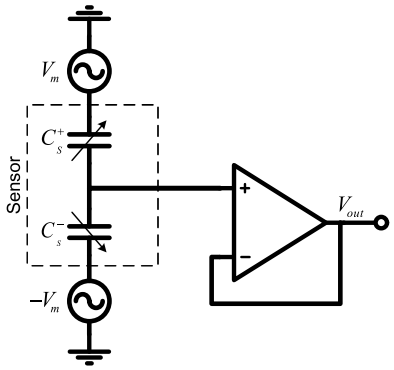


Figure 2.21: A voltage based interface circuit for differential accelerometers used to achieve a ratiometric output.

$$V_{out} = K\frac{C_s^+ - C_s^-}{C_s^+ + C_s^-} \tag{2.40}$$

$$= K\frac{\frac{2C_s\frac{x}{d}}{1-(\frac{x}{d})^2}}{\frac{2C_s}{1-(\frac{x}{d})^2}}$$

$$= K\frac{x}{d}\ . \tag{2.41}$$

Here K is equal to V_m for the circuit implementation shown. A simulation of the circuit is shown in Fig. 2.22. Eq. (2.41) is an exact formula[10]; therefore, based on this as well as the simulation results we can see that:

[10] no approximation have been made in its derivation

- There is no offset in the output
- No harmonics exist, even or odd (to a first order approximation)

The story may end here; however, the problem with the above analysis is that it assumes that the plate movement is not affected by voltages/currents placed on the capacitor plates. The results shown in Eq. (2.40) and the simulation shown in Fig. 2.22 do not take into account the electrostatic force that is caused by the bias and modulating

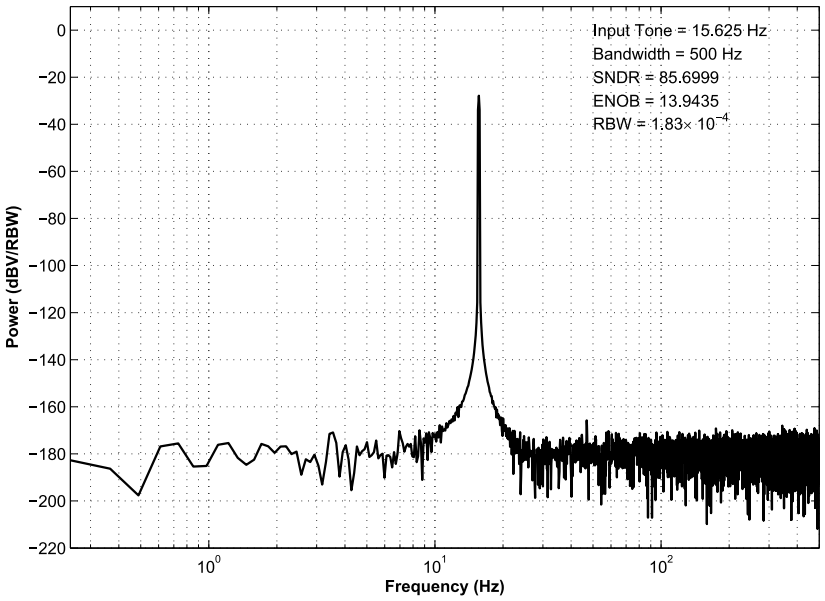


Figure 2.22: Output spectrum of the ratiometric voltage based interface circuit for a differential accelerometer.

voltages and currents. The electrostatic force causes unwanted movements that cause nonlinearities negating the benefits of the ratiometric output as shown in the next section.

2.6.5 Ratiometric Output without Charge Balance

Charge balance is a technique whereby feedback is used to make the voltage and hence the charge on a sense capacitor on average zero. A circuit that achieves ratiometric output without charge balance does not provide better linearity as the electrostatic forces create harmonics mitigating any benefits. To prove this, the sense capacitance values C_s^+ and C_s^- must take into account the force being exerted by the electrostatic charge placed on the plates as well as the external force that the device is designed to measure. This would in turn require an equation for displacement that takes into account the electrostatic force given by

$$F_e^{\pm} = \frac{A\epsilon_r\epsilon_o}{2(d \pm \hat{x})^2} \ , \tag{2.42}$$

where A is the equivalent area of the capacitor plates, ϵ_o is the permittivity of free space and $\hat{x}$ is the displacement due to the external and electrostatic force. The problem with this approach is that the displace-

ment $\hat{x}$ no longer has a closed form solution and graphical techniques must be used [60] [61]. These graphical techniques cannot provide analytical formulas for the harmonics that are generated. An approximate method to obtain closed form solution for the harmonics is to assume that the force is only a function of displacement x[11]. As such, the electrostatic force formulas become

[11] due to the external force only

$$F_s^+ = \frac{A\epsilon_r\epsilon_0 V^2}{2(d-x)^2} \qquad \text{and} \qquad F_s^- = \frac{A\epsilon_r\epsilon_0 V^2}{2(d+x)^2} \ , \tag{2.43}$$

where F_s^+ and F_s^- are the electrostatic forces being exerted on capacitors C_s^+ and C_s^- respectively. These forces in turn create parasitic displacements given by

$$\alpha^+ = \frac{F_s^+}{m}\frac{1}{\omega_n^2} \qquad \text{and} \qquad \alpha^- = \frac{F_s^-}{m}\frac{1}{\omega_n^2} \ , \tag{2.44}$$

where α^+ and α^- are the electrostatic force displacements on capacitor plates C_s^+ and C_s^- respectively. It should be noted that the electrostatic force on either sense capacitor is *always positive* and as such acts to *reduce* the gap distance. Therefore, the sense capacitance values are now given by

$$C_s^+ = \frac{C_s}{1-\frac{x+\alpha^+}{d}} \qquad \text{and} \qquad C_s^- = \frac{C_s}{1+\frac{x-\alpha^-}{d}} \ . \tag{2.45}$$

Substituting Eq. (2.45) into Eq. (2.40) we have

$$V_{out} = K\frac{\left(\frac{x}{d}+\frac{\alpha^+-\alpha^-}{2d}\right)}{\left(1-\frac{\alpha^++\alpha^-}{2d}\right)} \ . \tag{2.46}$$

Using a Taylor series approximation of Eq. (2.46) around $\frac{x}{d}=0$, we can show that the output is now given by

$$\begin{aligned} V_{out} \approx K\Bigg[& \frac{d^3-2F_o}{d\left(d^3-F_o\right)}x \\ & -\frac{\left(d^3F_o+2F_o^2\right)}{d^3\left(d^3-F_o\right)^2}x^3 \\ & +\frac{\left(-d^6F_o-6d^3F_o^2-2F_o^3\right)}{d^5\left(d^3-F_o\right)^3}x^5\Bigg] \ , \end{aligned} \tag{2.47}$$

where F_o is a factor given by

$$F_o = \frac{A\epsilon_r\epsilon_o}{m\omega_n^2} \ . \tag{2.48}$$

To put this formula in perspective, for an 8 g input acceleration, and average voltage of 1 V^2, the ratio of the fundamental tone to the third harmonic is 56 dB for a typical surface micromachined differential accelerometer. A simulation of the circuit in Fig. 2.21 taking into account the electrostatic forces[12] is shown in Fig. 2.23. From the graph and Eq. (2.47) we can observe that:

[12] For details of modeling setup, see Section D.4

- There is an offset in the output
- Even and odd order harmonics exist

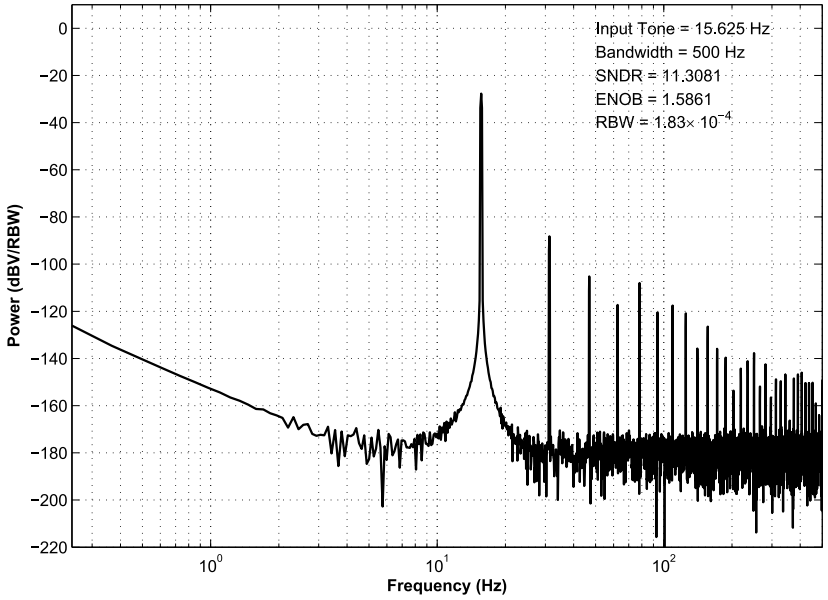


Figure 2.23: Output spectrum of a ratiometric voltage based interface circuit for a differential accelerometer with electrostatic forces modeled.

2.6.6 Ratiometric Output with Charge Balance

It can be proven through simulations and analysis that a charge balanced output reduces displacement and hence harmonics observed at the output. As before, when taking into account electrostatic forces, the displacement x no longer has a closed form solution but an approximation can be made to get a sense of the level of the harmonics. With charge balance, the electrostatic force on each sense capacitor will, on average, be equal. For this to occur, we must have

$$\begin{aligned} F_s^+ &= F_s^- \ , \\ \frac{A\epsilon_r\epsilon_0 V_+^2}{2(d-x)^2} &= \frac{A\epsilon_r\epsilon_0 V_-^2}{2(d+x)^2} \ . \end{aligned} \tag{2.49}$$

Here V_- and V_+ are the average dynamically adjusted voltages. For the above equation to hold, we need

$$V_+ \propto (d-x) \qquad \text{and} \qquad V_- \propto (d+x) \ . \tag{2.50}$$

Therefore, on average, the force due to the electrostatics is not a function of the displacement x. The output as given by Eq. (2.46) now simplifies to

$$\begin{aligned} V_{out} &= K\frac{\left(\frac{x}{d} + \frac{\alpha^+ - \alpha^-}{2d}\right)}{\left(1 - \frac{\alpha^+ + \alpha^-}{2d}\right)} \\ &= K\frac{\left(\frac{x}{d}2d\right)}{\left(1 - \frac{\alpha^+ + \alpha^-}{2d}\right)} \\ &= K\frac{x}{d}\left(1 + \text{constant}\right) \ . \end{aligned} \tag{2.51}$$

Therefore, there is a gain error associated with the ratiometric charge balanced output but the harmonics are significantly reduced [61]. There is still a problem associated with charge balanced ratiometric circuits that will be explored in the next chapter and a solution proposed. As we established in the previous section, charge based interface circuits will also provide the best resolution in our intended application. This will be the starting point in Chapter 3 where the problem and proposed solution is analyzed.

3

A Variable Gain Direct Digital Ratiometric Charge Balanced System

In Chapter 2, we argued that given that for practical purposes, our system will be dual chip, then from a fidelity perspective, switched capacitor designs are the best option as they offer the highest resolution with large parasitic capacitances as would be expected in dual chip implementations. This chapter then serves to develop capacitive readout circuits based on displacement measurements and use of charge based switched capacitor principles.

Readout circuits for capacitive accelerometers are in reality *capacitive ratio circuits* and a large body of electronics has already been developed in this area. Therefore, **Section 3.1** develops the idea based on existing capacitive ratio circuits and specifically delta sigma based ratio circuits. This section also explores the problem that the proposed circuit aims to rectify. Delta sigma ADC's are feedback systems that require an appropriately sized feedback signal level compared to the input signal level. This task is complicated for capacitive accelerometers as the signal coming into the ADC is proportional to the difference in sense capacitance whereas the feedback must be proportional to the sum or individual sense capacitances. A single-ended topology is proposed to rectify this problem.

Precision analog signal processing requires the use of differen-

tial circuits and offset and noise cancellation techniques. After developing a single-ended version of the circuit, **Section 3.5** then adds complexities for precision analog design including adaptation to differential circuitry and noise cancellation. These techniques are well developed for individual blocks, but the physical structure of the accelerometer limits circuit topologies that can be implemented. A novel technique is introduced to create a pseudo differential output while at the same time canceling offset and low frequency noise which is essential for low bandwidth applications.

3.1 Ratio Measurement Circuits

To restate out problem, acceleration causes a change in capacitance and we need to measure this change. Ideally, we would like to measure this acceleration with a differential accelerometer and achieve a ratiometric charge balanced output such that

$$V_{out} = K\frac{C_s^+ - C_s^-}{C_s^+ + C_s^-} \ , \tag{3.1}$$

where K is a gain factor. Therefore, readout circuits for capacitive sensors[1] are capacitive ratio measurement circuits. Fortunately, many capacitive ratio circuits exist and have been reported in literature [62] [63]. These circuits are often used in characterizing the precision of capacitor ratios in CMOS processes which set limitations on the precision of switched capacitor amplifiers, integrators, and data converters. Since capacitive sensor readout circuits are based on relative ratio of change in capacitance to a reference capacitance, it is possible to modify ratio-measurement circuits for this purpose. Our approach is then to use these circuits and modify them for capacitive accelerometers. We will forgo many of the traditional ratio circuits and focus on a delta sigma based version of the circuit which the final solution will be based upon.

[1] In any form not necessarily just ratiometric outputs

3.2 Delta Sigma Based Ratio Circuits

A variety of capacitive ratio circuits rely on delta sigma modulators and this approach is attractive for interface circuits. To begin with, the low frequency application of accelerometers bodes well for delta sigma

modulators that rely on oversampling. Furthermore, as we discussed in Section 1.1, for most applications, we ultimately would like to achieve digitization of our analog acceleration signal. A delta sigma modulator has the potential to extract and digitize the acceleration signal[2], a simplification that can lead to lower cost and lower power consumption.

[2] with the addition of a decimation filter

To demonstrate how a delta sigma modulator can be used as a ratio circuit, we can analyze a first order system as shown in Fig. 3.1. This circuit samples the input u in ϕ_1 and integrates the charge onto the capacitor C_f in ϕ_2. The output of the integrator then changes depending on the input value in each clock cycle. The quantizer then compares this signal to a threshold value and outputs a discrete time signal v. The signal v is then combined with the clock ϕ_2 to sample one of the reference voltages onto C_2 and subsequently discharge this value onto the feedback capacitor, C_f. Accordingly, the output of the integrator is either reduced (if the output of quantizer is higher than the threshold) or increased (if the output of the quantizer is lower than the threshold)[3]. So for example, if the value of v is high, $+V_{ref}$ is sampled onto C_2 and the output is reduced by $-V_{ref}C_2/C_f$.

[3] In other words, there is negative feedback around the loop but in discrete time and in fixed values

Here, if we choose C_1 and C_2 to be equal to C_f, then the noise transfer function of the modulator is given by $NTF(z) = 1 - z^{-1}$ (a high pass filter), and the signal transfer function $STF(z) = z^{-1}$ (a delay). Therefore, this is a first order delta sigma modulator, the signal $u(t)$ is passed through and the noise introduced by the quantizer is high pass filtered. Therefore, at the output we have a discrete time signal that can easily be digitized. We are interested in creating a ratio of the capacitors C_1 and C_2 rather than filtering the input $u(t)$ as a normal delta sigma modulator would do. We may surmise to change the input $u(t)$ to one of the reference voltages. If we do this, then for a set number of clock cycles, N, the total charge contributed by C_1 is $NV_{ref}\ C_1$ and assuming there are n high cycles, the charge contributed by C_2 is $-(N-n)V_{ref}C_2 + nC_2V_{ref}$.

The discrete pulse density feedback ensures that over a long period of time, the total charge injected into the integrator must be zero [4]. Ac-

[4] Otherwise the circuit would be unstable

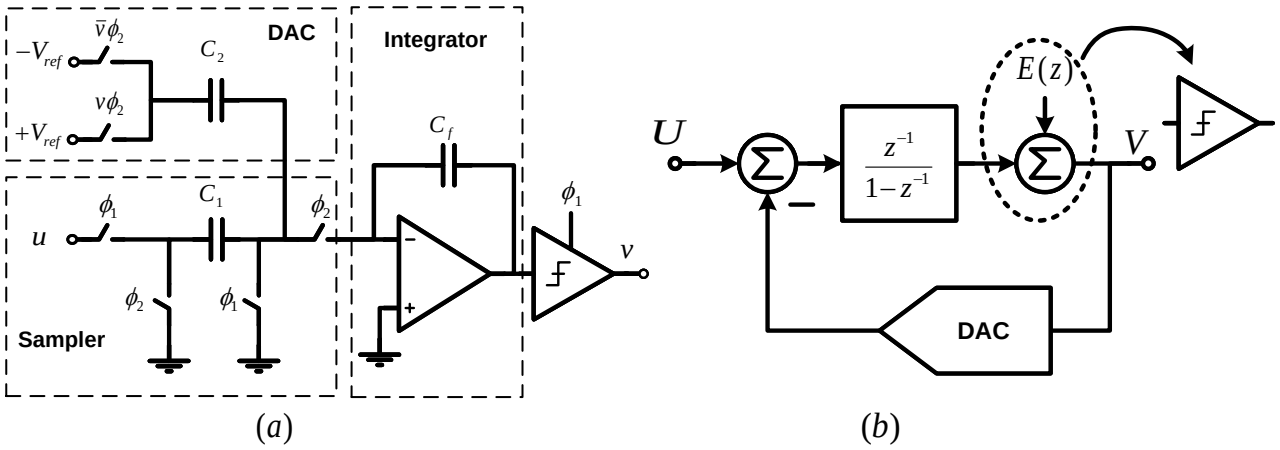


Figure 3.1: Switched capacitor implementation of a first order delta sigma modulator.

cordingly, we can write

$$NV_{ref}C_1 = -(N-n)V_{ref}C_2 + nC_2V_{ref}$$
$$C_1 + \left(1 - 2\frac{n}{N}\right)C_2 = 0\ . \tag{3.2}$$

Therefore, the ratio of the capacitances can be given as

$$\frac{C_1}{C_2} = 2B_{ave} - 1\ , \tag{3.3}$$

where B_{ave} is the DC value of the output pulse stream. Therefore, a delta sigma modulator can be used to find the capacitive ratio of say a single-ended capacitive sensor such as a pressure sensor.

For a differential sensor, we need an output proportional to the difference of the output, $C_1 - C_2$[5]. More importantly though, we would prefer to have a ratiometric output of $(C_1 - C_2)/(C_1 + C_2)$ to achieve better linearity [6]. Therefore, we need to modify the above circuit to achieve at a minimum an output that is a the difference in capacitance $(C_1 - C_2)$, and ideally ratiometric.

[5] In other words, $C_s^+ - C_s^-$ which would be proportional to input force as discussed in Section 2.6

[6] along with achieving charge balance as discussed in Section 2.6 but this is a given when using an integrator and the feedback nature of a delta sigma modulator

3.2.1 Achieving Summation of Two Capacitors

Since the DAC capacitor C_2 appears in the denominator, and we wish to achieve a summation, we can simply split this capacitor into two parts called C_s^+ and C_s^- representing the sense capacitors under acceleration. Similarly, since the capacitor C_1 appears in the numerator and we aim

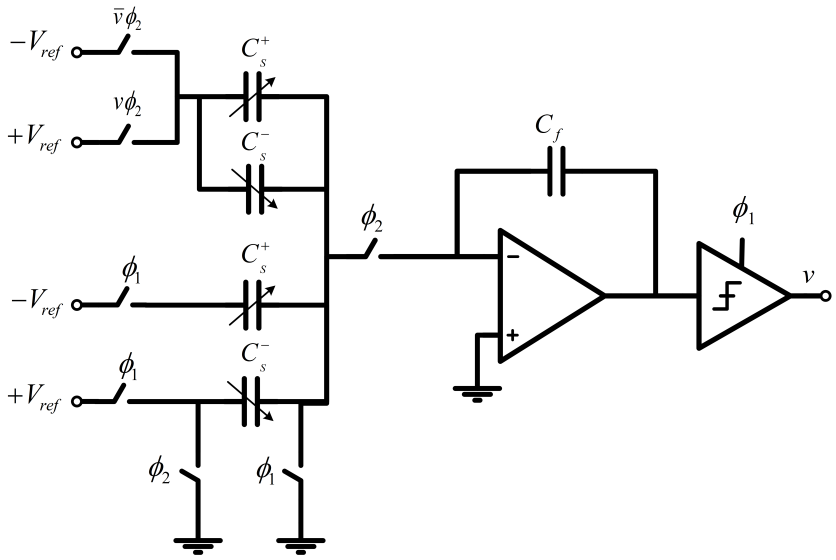


Figure 3.2: A delta sigma modulator used to obtain a ratiometric output.

to achieve subtraction, we can use opposite polarity voltages[7]. We end up with the circuit of Fig. 3.2.

[7] We will exploit another technique later on to achieve subtraction

It is trivial to show that this circuit achieves a ratiometric output. We can simply replace C_1 in Eq. (3.2) with $C_s^+ + C_s^-$ and C_2 with $C_s^+ - C_s^-$.

The problem with the above implementation as it relates to capacitive accelerometers is that we do not have two separate sets of capacitors [8]. Therefore, for the architecture of Fig. 3.2 to work, we need to simultaneously have access to capacitors C_s^+ and C_s^-. This can be achieved in a time multiplexed way as will be shown in the next section.

[8] At least when using commercial differential accelerometers. Certain special accelerometers exist that have four sets of sense capacitors but these are not common

3.2.2 Time Multiplexed DSM Systems for Ratio Measurement

The solution to the above problem is to time multiplex the input and feedback signals. Since the output of a charge balanced system is time averaged, as long as the rate of change is well above the bandwidth of the signal (in this case the acceleration), then the output of the system between two time constants does not change and can be assumed to be constant. Going through several iterations of this process, we can arrive at the circuit of Fig. 3.3 [64] [65].

The circuit operates in two phases. Depending on the output v, during each phase one capacitor is biased to a voltage V_{ref} in such a way that either a positive or negative charge is passed on to the integrator[9].

[9] This is accomplished by simply using a delaying and non-delaying integrator

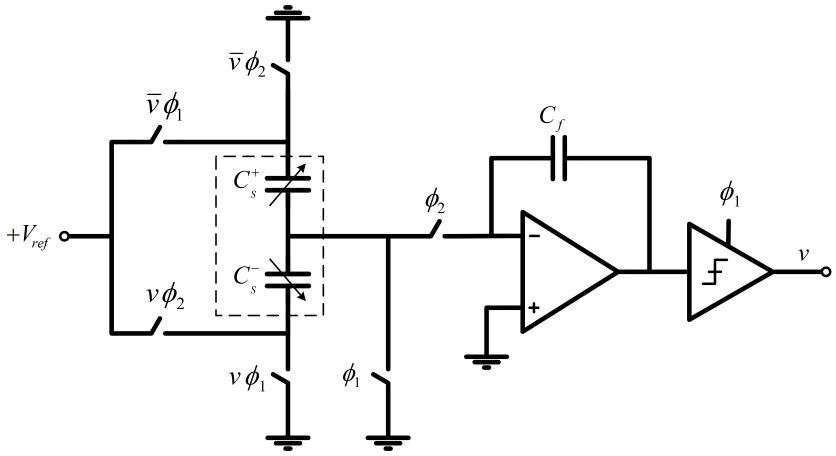


Figure 3.3: A delta sigma modulator that achieves ratiometric output through time multiplexing of the sense capacitors.

The comparator then compares this value and outputs a new v value aimed to reduce the output of the integrator. If the operation is considered for a long time, the average current to the integrator must be zero. Therefore,

$$n\frac{C_s^-}{C_f}V_{ref} = (N-n)V_{ref}\frac{C_s^+}{C_f} \ . \tag{3.4}$$

Re-arranging the above equation,

$$\begin{aligned} nC_s^- &= (N-n)C_s^+ \\ n(C_s^+ + C_s^-) &= NC_s^+ \\ \frac{C_s^+}{C_s^+ + C_s^-} &= \frac{n}{N} = B_{ave} \\ \frac{C_s^+ - C_s^-}{C_s^+ + C_s^-} &= 2B_{ave} - 1 \\ B_{ave} &= \frac{1}{2}\frac{C_s^+ - C_s^-}{C_s^+ + C_s^-} + \frac{1}{2} \ . \end{aligned} \tag{3.5}$$

Therefore, at first glance this circuit achieves our purpose. We may at this point then focus on precision analog techniques including how to make the system differential, and reduce low frequency noise. However, this circuit has a fundamental problem as it relates to capacitive accelerometers.

3.3 Second Order Delta Sigma and Gain Coefficients

To demonstrate the problem with delta sigma based interface circuits, we need to review the design of basic delta sigma modulators. We will jump directly to a second order system as shown in Fig. 3.4.

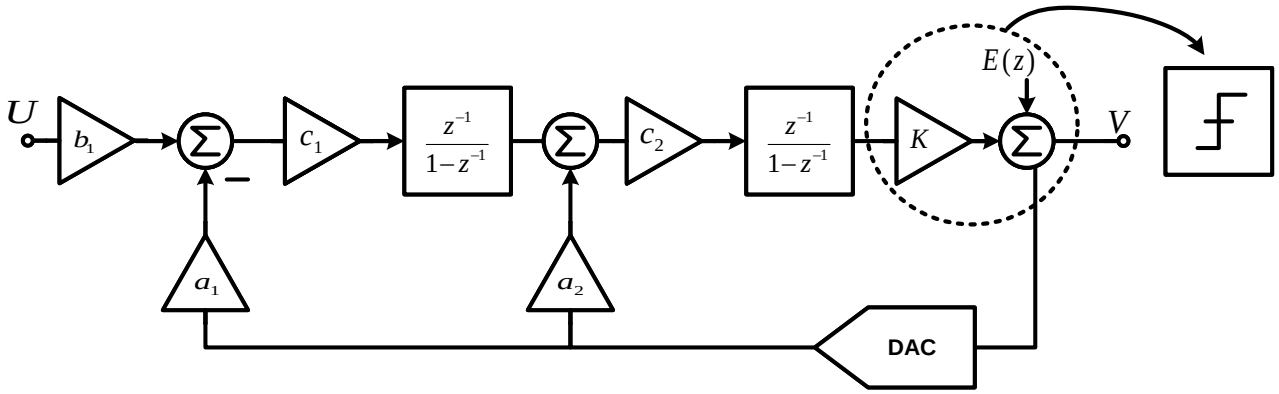


Figure 3.4: Block diagram of a second order delta sigma modulator with quantizer replaced by a summer and signal $E(z)$ that mimics operation of the quantizer.

The key to the analysis of a delta sigma modulator is to replace the quantizer with a linear summer and additive quantization noise $E(z)$ and assume a gain K for the quantizer. Doing this creates an LTI system and performing a linear analysis using the system of Fig. 3.4 results in the following equation:

$$\left[c_1\left(b_1U(z)-a_1V(z)\right)\frac{z^{-1}}{1-z^{-1}}-a_2V(z)\right]c_2\frac{z^{-1}}{1-z^{-1}}K+E(z)=V(z)\ . \tag{3.6}$$

Re-arranging, we get the following NTF and STF transfer functions:

$$STF(z)=\frac{Kb_1c_1c_2}{z^2+\left(Ka_2c_2-2\right)z+\left(1-Ka_2c_2+Ka_1c_1c_2\right)}\ , \tag{3.7}$$

$$NTF(z)=\frac{(z-1)^2}{z^2+(Ka_2c_2-2)z+(1-Ka_2c_2+Ka_1c_1c_2)}\ . \tag{3.8}$$

The design of delta sigma modulators at this stage boils down to finding coefficient values such that the noise transfer function and the signal transfer function have desirable frequency response. It can be shown that for the structure above, the effective gain around the loop must be very close to one [66]. This in turn means that the value of $K\approx\frac{1}{a_1c_1c_2}$ [67].

Substituting this value in the above equation and solving for $V(z)$ in terms of $U(z)$ and $E(z)$ will give us the noise and signal transfer functions for the above system. If we then choose $a_2 = 2a_1c_1$, then the NTF and STF have the desirable form given by

$$STF = \frac{b_1}{a_1} z^{-2} \ , \tag{3.9}$$

$$NTF = \left(1 - z^{-1}\right)^2 \ . \tag{3.10}$$

The system above demonstrates the issue that delta sigma modulators face when incorporated within an accelerometer. The signal transfer function above depends on the coefficients a_1 and b_1. For the system presented in Fig. 3.2 above, what are these coefficients proportional to? Noting that the coefficients always represent the gains *being fed into* the integrators, in our system feed forward gain or b_1 is proportional to

$$b_1 \propto (C_s^+ - C_s^-) \ . \tag{3.11}$$

Similarly, the feedback signal is proportional to:

$$a_1 \propto C_s^{\pm} \ . \tag{3.12}$$

This is problematic because the difference in change in capacitance is often a fraction of actual capacitance. For example, for the accelerometer that was tested, the nominal change in capacitance was 5 fF/g whereas the actual capacitance is nominally at 350 fF[10]. This represents almost a two order of magnitude difference in feedback and feedforward signals. The consequence is that the power spectral density of the output would result in a signal that is below the full scale by:

$$\begin{aligned} \text{Signal Power} &= 20 \log \left(\frac{C_s^+ - C_s^-}{C_s^+ + C_s^-} \right) \\ &< -36 \text{ dBFs} \ . \end{aligned} \tag{3.13}$$

This equation assumes an input acceleration of 1 g but in general very few applications require such high g forces[11]. Furthermore, it is a function of mechanical accelerometer systems to suffer linearity issues

[10] Certain ratiometric charge balanced outputs have $a_1 \propto C_s^+ + C_s^-$ which further aggravates the problem

[11] To have an intuitive feeling for *g forces*, fighter pilots are required to withstand acceleration forces of up to 8 g in combat maneuvering; therefore, for normal day to day activities where accelerometers may be of use, acceleration ranges are typically much smaller than this.

at higher deflections [68]. Therefore, from a linearity perspective, we might be tempted to only use a small fraction of the mechanical limit of the accelerometer.

All these reasons highlight the fact that in accelerometer applications using feedback, systems achieving ratiometric output and charge balance are fundamentally limited by the mechanical specifications of the sensor. This issue rarely comes into play in designing signal processing delta sigma modulators for example in audio applications. Sampling and DAC capacitors are chosen appropriately to maximize output signal fidelity and achieve proper noise and signal transfer functions.

Finally, it is important to note that the issue highlighted above is not specific to delta sigma modulators. DSM's are special cases of feedback systems. Even traditional continuous time feedback systems face this issue as highlighted in the next section.

3.3.1 Other Charge Balanced Ratiometric Systems

One often forgets that delta sigma modulators are simply special cases of feedback systems. Therefore, the problem exposed in the previous section is not unique to delta sigma systems. A popular circuit that uses a continuous time feedback to achieve charge balanced and ratiometric output was first proposed in 1990 [69]. A simplified version of the circuit is shown in Fig. 3.5.

An analysis of this circuit shows that the output is given by

$$V_o(z) = V_{ref} \frac{C_s^+ - C_s^-}{\frac{C_f}{C_4} C_3} \frac{z}{z - (1 - \frac{C_s^+ + C_s^-}{C_f} \frac{C_4}{C_3})} , \qquad (3.14)$$

where V_{ref} is a DC reference voltage. Note that at DC ($z = 1$), the output is perfectly ratiometric.

This system is different from the delta sigma based system above because the feedback is continuous. Nevertheless, this system can potentially suffer from a low output signal because the signal is the difference in sense capacitances whereas the feedback is the sum of those sense capacitances. To demonstrate this, a simulation of the system using a commercial surface micromachined accelerometer is shown in Fig. 3.6. For these types of accelerometers, typical values for the sensitivity and

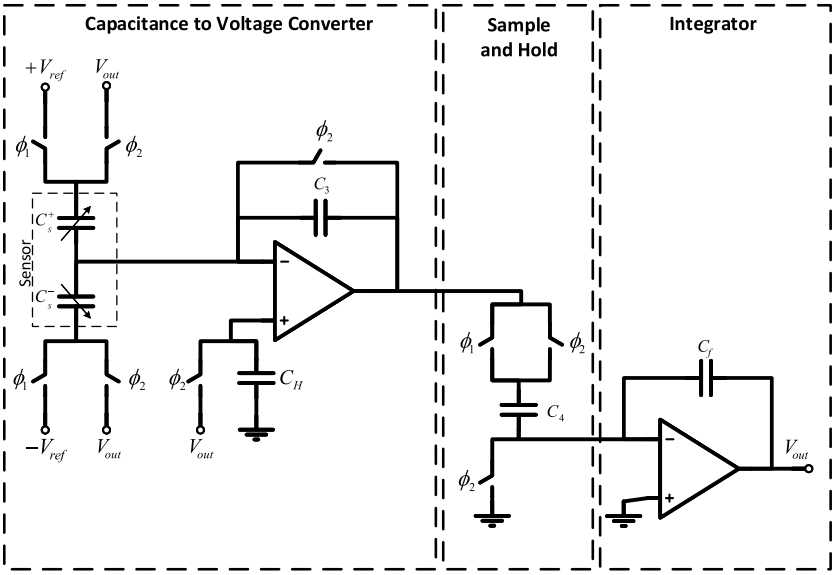


Figure 3.5: A continuous time feedback system achieving charge balanced and ratiometric output (Leuthold integrator).

sense capacitance are 2.5 fF/g and 500 fF respectively [70].

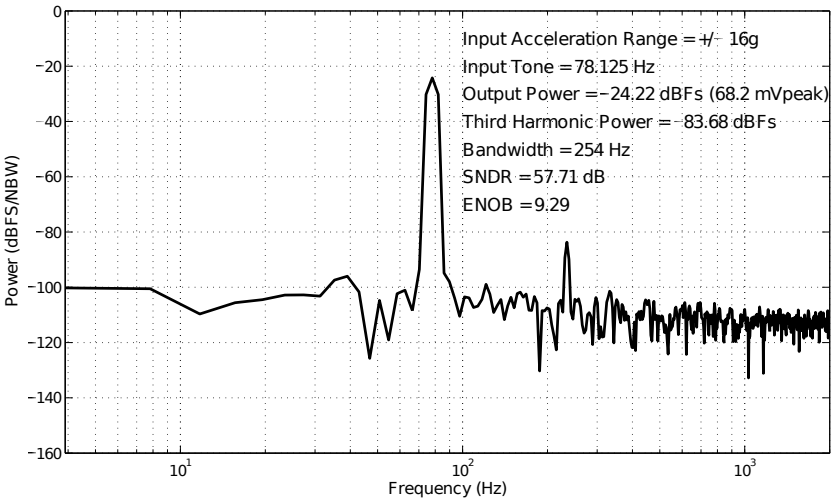


Figure 3.6: Simulated output spectrum of the Leuthold integrator (Fig. 3.5). Notice that despite using a very high acceleration range (±16 g), the output signal is well below full scale

The simulation shows that despite being ratiometric and charge balanced, the system only achieves 56 dB SNDR. The problem is the small power level in the fundamental tone which is −25 dB full scale (dBFS). Intuitively, this small power level can be explained by the fact that the signal is proportional to the difference in sense capacitors while the feedback is proportional to *sum* of the sense capacitors. Therefore, depending on the sensitivity and size of the sense capacitors, the feedback

may be too large and reduce the output signal level.

Notice that this system is more robust than the DSM shown in Fig. 3.3 because the output signal can be increased with the reference voltage V_{ref}. The extend to which the reference voltage can be increased, however, is limited both from the perspective of the available on-chip supply and more importantly, pull-in phenomena associated with the mechanical capacitors [13]. A gain stage, at the front of the integrator does not improve the SNDR as this will amplify the signal as well as the noise.[12] Fig. 3.7 and Fig. 3.8 summarize the problem of charge balanced ratiometric readout circuits for continuous time analog feedback and pulse density feedback respectively.

[12] Another way to understand this is to note that the output signal is proportional to the feedback signal regardless of the gain of the feedforward path.

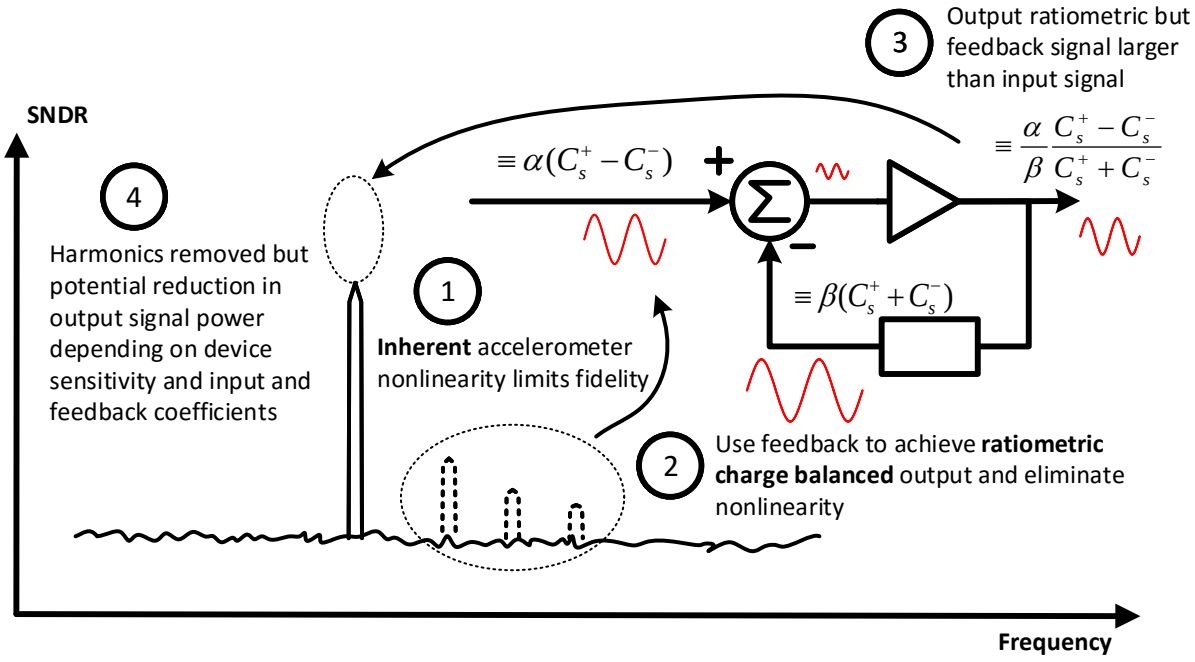


Figure 3.7: The problem of ratiometric charge balanced readout demonstrated for an analog continuous time feedback system.

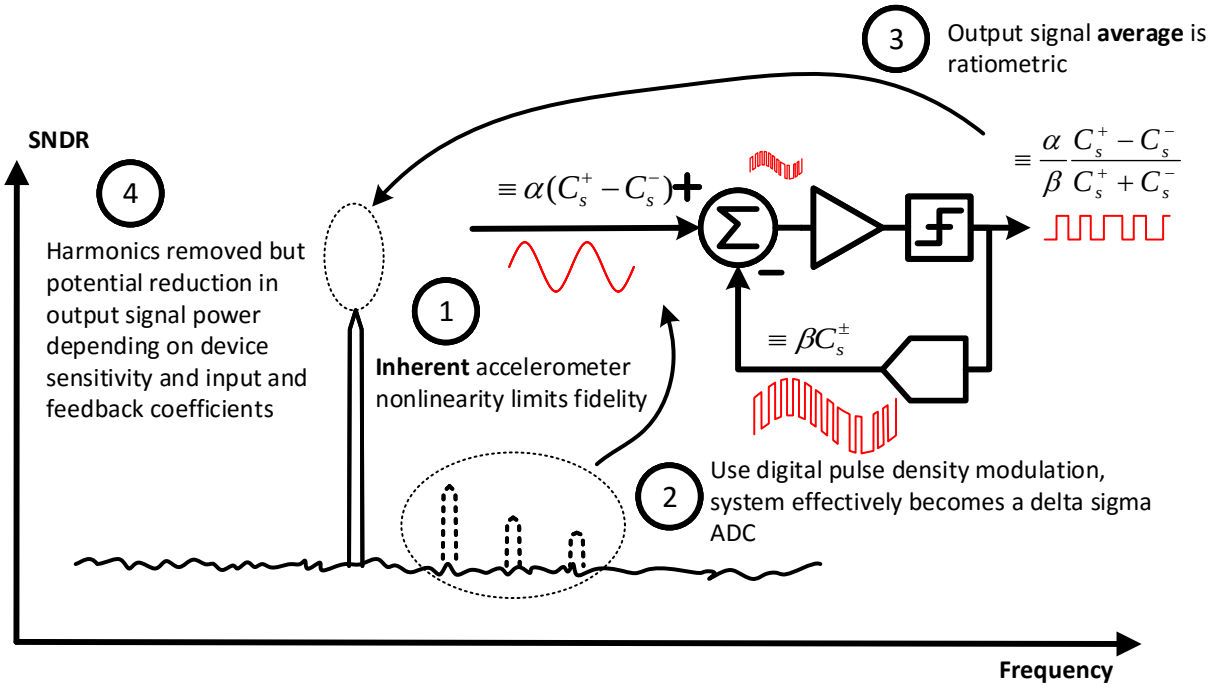


Figure 3.8: The problem of ratiometric charge balanced readout demonstrated for an analog discrete time (pulse density modulation) feedback system.

3.4 Variable Gain Delta Sigma Modulator Design

3.4.1 Dual Phase Input and Feedback

The previous sections highlighted the problem with interfacing accelerometer in delta sigma modulators. To achieve a ratiometric output, inevitably the feedback over compensates the input signal. There are many options that can be pursued at this stage but recognizing that the difference in feedback and feedforward gains can be substantial, we need to maximize the flexibility of the system.

The most robust approach would be to decouple the feedback mechanism from the input such that its value can be adjusted independently. This is essential as it allows us to change the feedback and feedforward gain factors independently and have more freedom in choosing an optimal NTF and STF. It is not simply enough to increase feedback and feedforward gain factors as these factors also play a role in the NTF.

To separate the feedback, we sample the signal in four phases. In one set of phases, a signal proportional to the difference in sense capacitors is sampled and amplified as is the case with many charge balance ratiometric systems. This value is held while we resolve our feedback value.

In the next set of phases, the feedback value is decided. Depending on whether the previous output of the delta sigma was high or low, *one* of the sense capacitors is sampled and a value proportional to the sense capacitor is outputted through a charge-to-voltage converter.

The sampled value from the previous phase and the new feedback value are then inputed to an integrator. This adjusts the output of the quantizer accordingly and the system adjusts in a negative feedback manner lowering or increasing the input to the quantizer based on the previous value.

Conceptually this system is not very different from the system presented in Fig. 3.2. The difference is that by separating the feedback, a large flexibility is ensured in getting the correct coefficient values that will optimize the signal fidelity of the system regardless of the sensitivity of the sensor device or its static capacitance values[13].

[13] Of course, op-amps must be designed to settle within the required bandwidth depending on the static capacitance.

3.4.2 Implementation and Analysis

A block diagram of the *first order* system is shown in Fig. 3.9 and the corresponding circuit implementation of the system is shown in Fig. 3.10 [71]. The system can also be extended to higher order delta sigma loops, but the process is not trivial and requires analysis on the structure of the second order system. This is discussed after the analysis of the first order system.

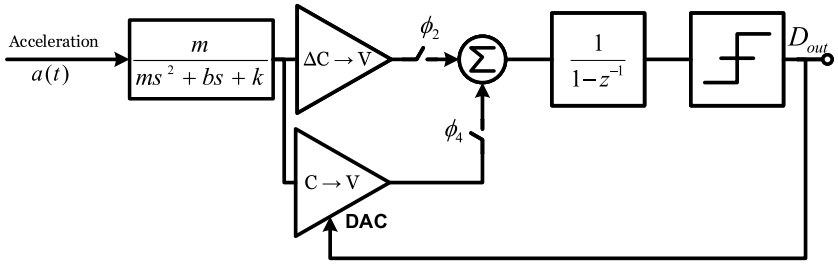


Figure 3.9: System level block diagram of the proposed system.

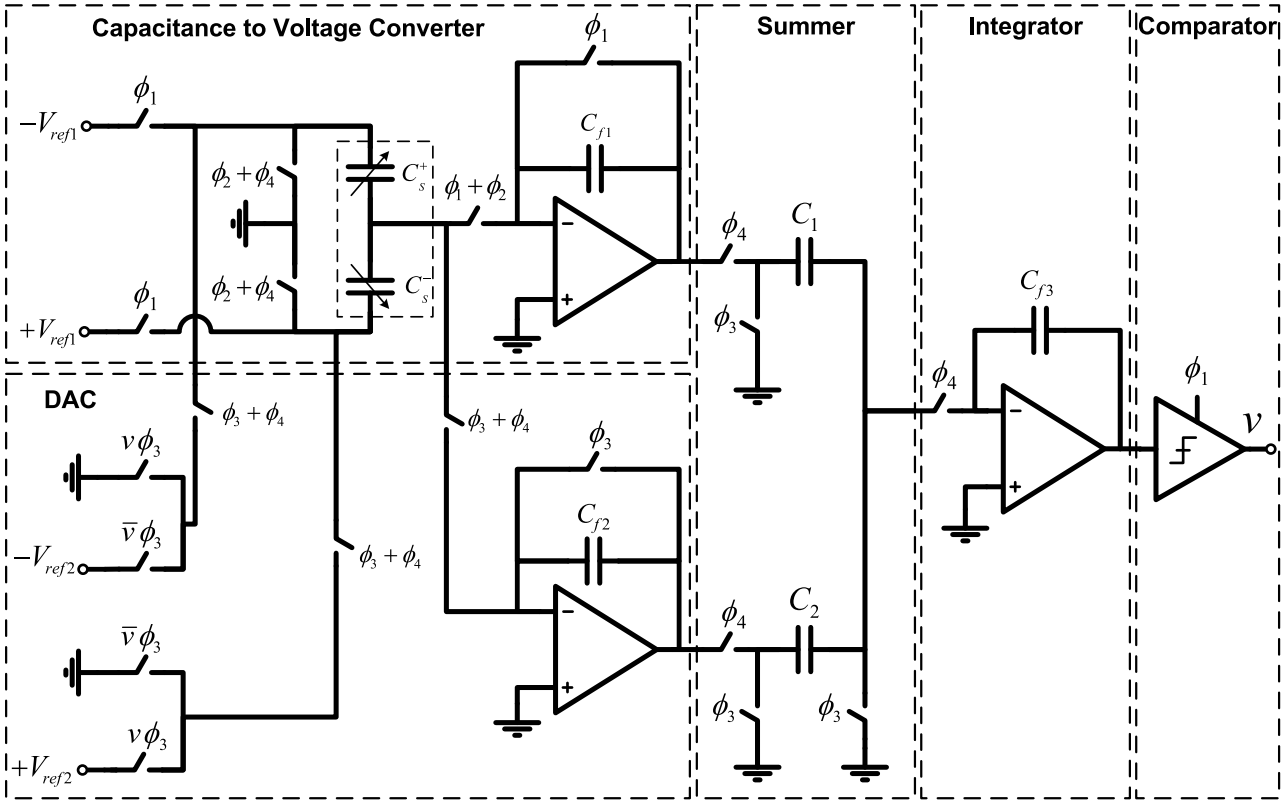


Figure 3.10: Single-ended first order delta sigma modulator with separate feedback and feedforward signal paths.

As with any delta sigma modulator, the operation of the circuit at low frequencies can be analyzed from a charge balance equation. Over a period of N cycles, the feedback will be high for n cycles and low for $N-n$ cycles. The negative feedback of the loop ensures the total charge at the input of the integrator to be zero; therefore, the following equations can be applied:

$$-nV_{ref_2}C_s^- \frac{C_2}{C_{f_2}} + (N-n)V_{ref_2}C_s^+ \frac{C_2}{C_{f_2}} + NV_{ref_1}(C_s^+ - C_s^-)\frac{C_1}{C_{f_1}} = 0$$

$$NV_{ref_1}(C_s^+ - C_s^-)\frac{C_1}{C_{f_1}} = V_{ref_2}\frac{C_2}{C_{f_2}}(nC_s^- + nC_s^+ - NC_s^+)$$

$$NV_{ref_1}\frac{C_s^+ - C_s^-}{C_s^+ + C_s^-}\frac{C_1}{C_{f_1}} = V_{ref_2}\frac{C_2}{C_{f_2}}\left(n - N\frac{C_s^+}{C_s^+ + C_s^-}\right)$$

$$\frac{C_s^+ - C_s^-}{C_s^+ + C_s^-} = \frac{V_{ref_2}}{V_{ref_1}}\frac{C_2}{C_1}\frac{C_{f_1}}{C_{f_2}}\left(\frac{n}{N} - \frac{C_s^+}{C_s^+ + C_s^-}\right)$$

$$B_{ave} = \frac{C_s^+}{C_s^+ + C_s^-} + \frac{V_{ref_1}}{V_{ref_2}}\frac{C_1}{C_2}\frac{C_{f_2}}{C_{f_1}}\frac{C_s^+ - C_s^-}{C_s^+ + C_s^-}$$

$$B_{ave} = \frac{1}{2} + \left(\frac{V_{ref_1}}{V_{ref_2}}\frac{C_1}{C_2}\frac{C_{f_2}}{C_{f_1}} + \frac{1}{2}\right)\frac{C_s^+ - C_s^-}{C_s^+ + C_s^-}\ . \qquad (3.15)$$

where $B_{ave} = \frac{n}{N}$ and is the average value of the bit stream.

The difference here compared to other charge balanced ratiometric techniques is that the signal transfer function can now be adjusted widely by three ratios allowing the input tone power to be maximized for a variety of dynamic ranges and sensitivities. This would involve adjusting the noise and signal transfer functions to ensure an appropriate gain as well as ensuring the noise shaping property of the modulator.

3.4.3 Limitation of Analysis

It is important at this point to make a comment regarding the circuit presented and its analysis in the traditional sense. The analysis of the above system has been performed for a DC input and is valid for low frequency inputs. One may be tempted to perform a full frequency analysis of the above system. This is in fact *intractable* for the proposed system. In continuous time, the notion of time invariant is very well

known. The equivalent notion in sampled time which includes switched capacitor circuits is shift invariant. Shift invariant means that regardless of the time at which an input is fed into the system, the output is the same but shifted in time.

In the system proposed, this concept quickly runs into a problem. Since the input signal is held while the feedback is resolved, then this negates shift invariance. If a signal comes in at a time while the feedback is being resolved, this signal must wait until the next cycle. This is a contradiction of shift invariance.

Overall, the lack of shift invariance does not pose a large problem. The delta sigma modulator itself is a nonlinear system whose analysis is often ad-hoc and confirmed through extensive simulations. Simulations in later sections show that the separation of the DAC feedback makes the proposed circuit more sensitive to stability. This is intuitive, since with a delayed feedback, more time is required to update the outputs of the integrators. The end result of this is that the architecture requires the use of non-delaying integrators which in turn increase the power requirements of the op-amps employed.

3.4.4 Implementation of Higher Order Systems

Looking at the performance of the proposed system from the perspective of a delta sigma modulator only [14], with an OSR of 512, the maximum possible SNDR for a first, second and third order modulators are 85 dB, 123 dB and 155 dB respectively [67]. Third order systems are hard to stabilize and the linearity is often limited by the sensor component. Therefore, a second order system will suffice in achieving maximum possible SNDR for the system.

[14] In other words not including the mechanical thermal noise of the accelerometer

3.4.5 Architecture of Second Order System

To extend the architecture shown in Fig. 3.10 to a second order system is itself not trivial. There are many second order systems that can be chosen. The key tradeoff for the present application is simplicity of noise and signal transfer functions. We would prefer an architectural choice where the NTF is relatively independent from the STF. In other words, we would prefer a design where by changing gain of the STF

does not require a significant change in the NTF transfer function as this would minimize the complexity of implementation. A secondary issue is to choose an architecture that bodes well to differential implementation. The ubiquitous second order DSM shown in Fig. 3.4 is not a good choice because the coefficient of the signal transfer function directly affects the noise transfer function. To use this architecture would require that several coefficients be adjusted dynamically adding to the complexity of the system. A better architecture involves replacing the second integrator of the regular second order DSM with a bilinear stage as shown in Fig. 3.11

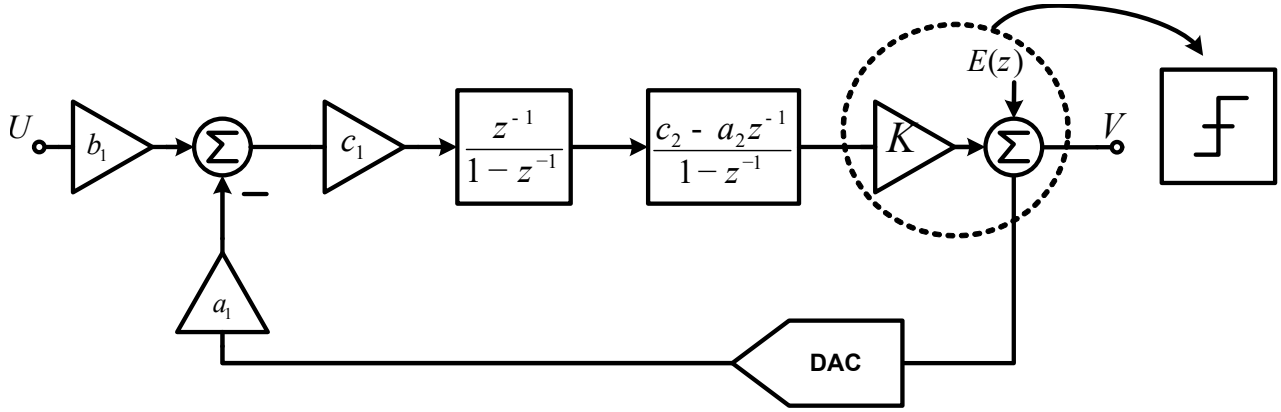


Figure 3.11: A second order DSM with a bilinear integrator stage eliminating one of the feedback coefficients. This architecture better buffers the noise transfer function from changes to the signal transfer function.

The output of this system is given by

$$V(z) = \left(c_1 \left(b_1 U(z) - a_1 V(z) \right) \frac{z^{-1}}{1 - z^{-1}} \right) \frac{c_2 - b_2 z^{-1}}{1 - z^{-1}} K + E(z) \ . \quad (3.16)$$

As before, we can assume that for proper operation $K \approx \frac{1}{a_1 c_1 c_2}$. Substituting this value in the above equation and solving for $V(z)$ in terms of $U(z)$ and $E(z)$ will give us the noise and signal transfer functions of the above system. Accordingly

$$\mathbf{V(z)} = \left[\frac{\frac{c_2 b_1}{a_1 a_2} z - \frac{b_1}{a_1}}{(z-1)^2 + \left(\frac{c_2}{a_2} z - 1 \right)} \right] \mathbf{U(z)} + \left[\frac{(z-1)^2}{(z-1)^2 + \left(\frac{c_2}{a_2} z - 1 \right)} \right] \mathbf{E(z)} \ , \quad (3.17)$$

where the coefficients to $U(z)$ and $E(z)$ represent the signal transfer function and noise transfer function respectively. What remains is to find coefficient values to achieve desirable transfer functions. If we choose $\mathbf{c_2 = 2a_2}$, then the STF and NTF are given by

$$\text{STF} = \frac{b_1}{a_1} \left(2z^{-1} - z^{-2} \right) \ , \quad (3.18)$$

$$\text{NTF} = \frac{1}{(1 - z^{-1})^2} \ . \quad (3.19)$$

Therefore, as before, we can achieve desirable noise and signal transfer functions. The key difference, however, is that with the architecture of Fig. 3.11, the choice of integrator gains c_1 and c_2 can be set rather arbitrarily[15]. Therefore, coefficients c_1 and c_2 can then be used to adjust the outputs of the integrators within a desired linear range to maximize the output fidelity. This is important for the present application as the adjustment in input and feedback gains must be accompanied by scaling in the subsequent stages. The circuit level design of the architecture of Fig. 3.11 is shown in Fig. 3.12.

[15] the only constraint is that the ratio of c_2 to a_2 must be $\frac{1}{2}$

3.4.6 Simulations

To demonstrate the effectiveness of the system in suppressing harmonics and achieving high linearity, a circuit level thermal noise simulation of the second order system is performed. The result is obtained by running a transient noise simulation [16]. This simulation includes 1.5 pF

[16] For details on the simulation setup refer to Appendix B

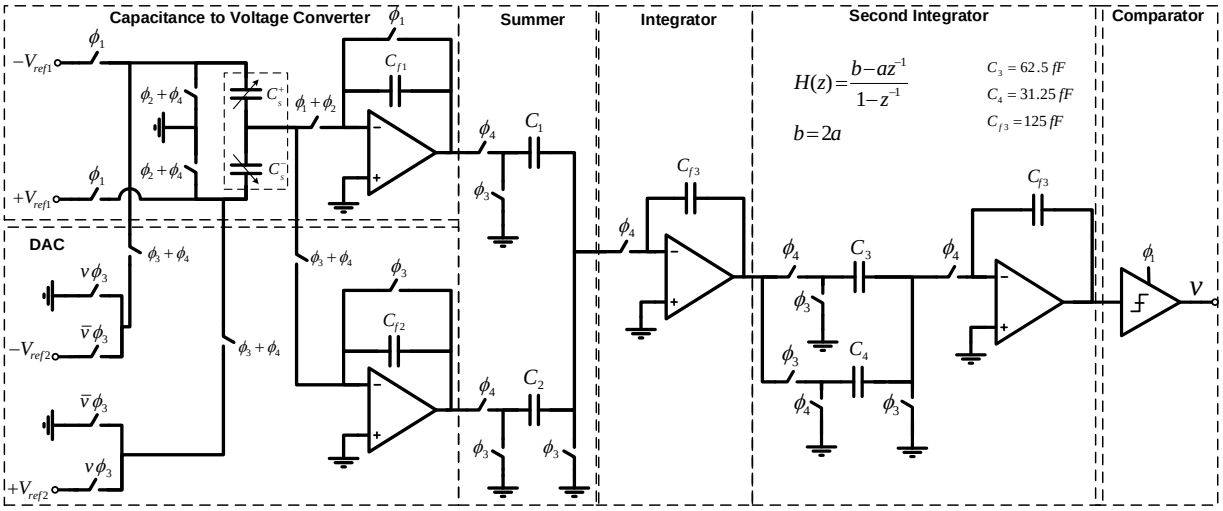


Figure 3.12: Circuit implementation of the second order DSM with a bilinear integrator stage.

of parasitic capacitance at each node of the accelerometer representing the pad and bondwire capacitance. The op-amps used are optimized for noise and power [72]. The same accelerometer as the one used for the Leuthold integrator is used with the same dynamic range of ±16 g corresponding to a differential capacitance ($C_s^+ - C_s^-$) of approximately 114 fF. The capacitor values used are $C_{f_1} = 800$ fF, $C_{f_2} = 800$ fF, $C_1 = 1000$ fF, $C_2 = 1000$ fF, $C_{f_3} = 700$ fF. The reference voltage for the converter stage is $V_{ref_1} = 600$ mV and for the DAC feedback stage $V_{ref_2} = 300$ mV. The sampling frequency is $F_s = 1024$ KHz and the signal bandwidth is 250 Hz.

To begin with, we look at the output spectrum of the capacitance to voltage converter by itself (the feedback DAC is disabled) as shown in Fig. 3.13. The output at this stage is neither ratiometric nor charge balanced and as a result has a large third order harmonic. Fig. 3.14 then shows the spectrum of the output bitstream for the proposed system. The feedback system creates a charge balanced and ratiometric output that eliminates the third order harmonic to below the noise floor.

3.4.7 Summary of the Single-Ended Architecture

The single-ended architecture proposed creates a charge balanced ratiometric output where the signal gain can be widely programmable

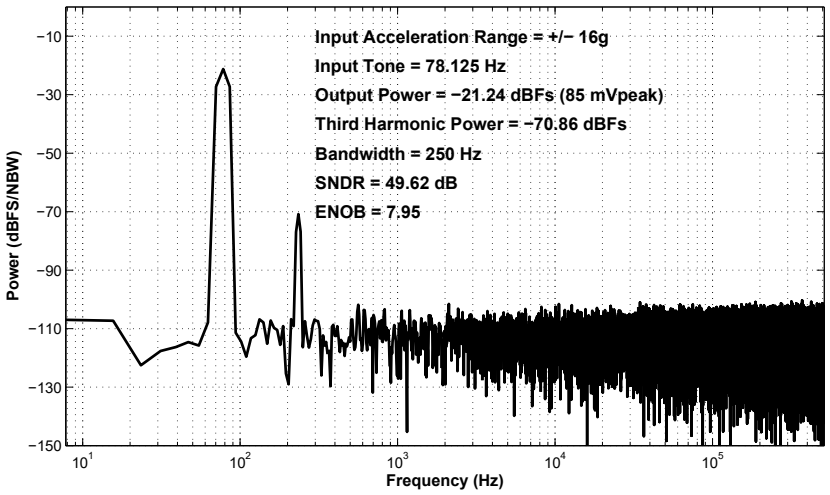


Figure 3.13: Power spectral density at the output of the charge to voltage converter shown in Fig. 3.12 with the feedback DAC disabled. Number of points used for FFT is 2^{18} and uses a Hanning window.

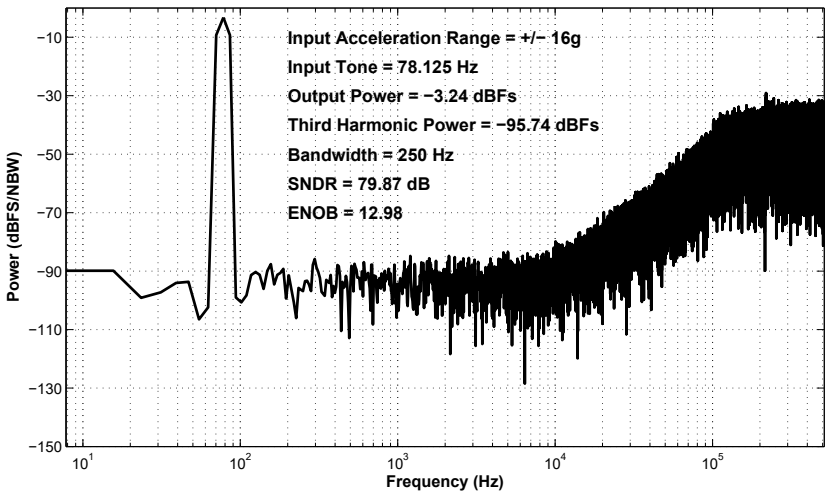


Figure 3.14: Power spectral density of the output bit stream for a second order system with thermal noise. Number of points used for FFT is 2^{18} and uses a Hanning window.

through the reference voltages and feedback capacitors. Simulations confirm that as long as oversampling is relatively high, the effect of the delayed feedback is not noticeable. What remains is to adapt the present single-ended system to high precision analog circuits - mainly noise reduction and differential signal processing. This in itself is not trivial and requires more specialized circuitry as explained in the next section.

3.5 Differential and High Purpose Circuitry

3.5.1 Motivation for Fully Differential Circuits

There are several benefits to having differential circuits and performing signal processing on differential signals. The major benefit is that differential processing greatly improves on nonlinearity associated with the circuit components. If we assume that differential signals pass through the same non-linearity, then the even order distortions or harmonics are in phase. Although the harmonics are still present, if the following stage is an amplifier, then the high common mode rejection ratio of the differential pair will significantly reduce the in phase harmonics. Even if there is no further stages[17], if we interpret the output differentially, then we will still get rid of the even order harmonics.

[17] for example in the last stage

The second major benefit of differential processing is that it doubles the signal swing compared to its single-ended counterpart leading to improved signal to noise ratio[18]. Differential circuits also *cause* less nonlinearity in a manner similar to how even order distortions are removed.

[18] The noise also increases but since noise sources are uncorrelated, they add as a sum of squares, leading to a 3 dB improvement in SNR for the differential case

Any one of the above benefits is reason to choose a differential architecture over its single-ended counterpart. As a result, high precision analog signal processing almost always makes use of differential signal processing when permitted. Without it, a system that looks very promising may never be fully utilized in commercial applications. For example, the Leuthold integrator discussed in the previous section has been traditionally underused as it does not have a straightforward differential implementation with some recent attempts to remedy this [73].

Apart from the need to create differential signal processing, the present system also makes use of complementary voltage references V_{ref_1} and V_{ref_2}. Any imbalance in these signals will cause the signal at the output to have a common mode signal saturating the output. Finally, low frequency noise sources such as $1/f$ noise can limit linearity and must be reduced. Therefore, this section looks at ways to enhance the single-ended circuitry developed in the previous section. As usual, the challenge lies in overcoming the physical limitations of the accelerometer.

3.5.2 Creating Differential Output For Input and Feedback Stage

Under normal circumstances, differential signaling from a design perspective is not a major issue as a large body of literature exists in this area. The challenge for the present application lies in the fact that we are severely limited in the techniques that we can employ due to the physical constraints of the accelerometer as shown in the Fig. 3.15.

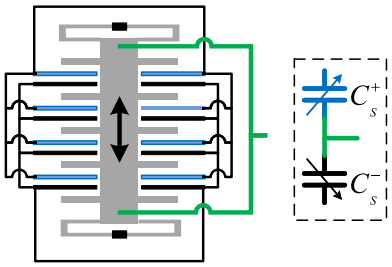


Figure 3.15: Physical construction of the differential accelerometer and corresponding model. The node connecting the two capacitors is fixed, complicating circuit topologies that can be achieved.

As the figure shows, since the sense capacitors are connected by the middle electrode, many of the traditional differential techniques are not easily adaptable since they rely on using each sense capacitor separately.

Certain applications modulate the middle electrode and connect the outside electrodes to the input terminals of an op-amp to create a differential output [30]. This topology, however, will have an input common mode that is no longer fixed and shifts, requiring an input common mode feedback circuit. Other solutions proposed including using two sets of sense capacitors and combining them in a differential manner [74]. Both these techniques add complexity to the circuit and increase power consumption[19].

[19] For more details on accelerometer interfacing options see Appendix F.

In this work, a novel approach that works well for the present architecture is a form of chopper stabilization as shown in Fig. 3.16 for the feedforward signal stage. The chopper stabilization works by inverting the reference voltage at certain intervals. A typical design choice and one that is easy to implement is to choose chopping frequency to be half the sampling frequency. As long as the sampling frequency is much larger than the bandwidth of the signal, the sample and hold capacitors create a differential signal to be processed by the following stages. Any low frequency noise or offset or mismatch between the reference voltages will be common mode to the differential signal and will be removed in the subsequent stages. The feedback stage also makes use of this technique as shown in Fig. 3.17. This stage is more complex because to create a differential signal in the feedback stage, the sense capacitors must be chopped in two stages. This makes the op-amp of this stage four times more power hungry than that of the single-ended structure.

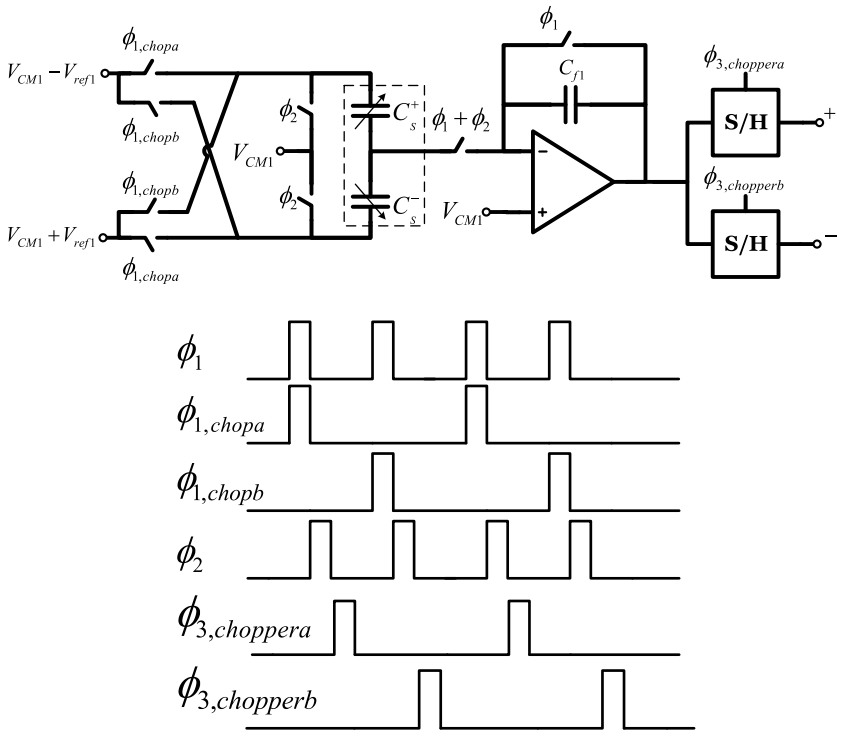


Figure 3.16: The feedforward gain stage of the proposed architecture adapted for differential circuitry

3.5.3 Static Capacitance Offset Cancellation

Although the architecture presented in the previous section is parasitic insensitive, the structure is still prone to offset errors. To demonstrate this, Fig. 3.18 shows the front end of the DAC feedback stage with parasitic capacitances when the output bitstream is high. There are two types of capacitance modeled: a capacitance to ground at each node representing the bondwire and pad capacitance and a parallel static capacitance across each plate. Due to the parasitic insensitive design of the circuitry, parasitic capacitance contribution due to the bondwire and pads do not harmonically limit the output. The static capacitance, however, can cause large harmonics because the charge amplified is no longer just due to the signal portion but rather to a signal portion and static portion. To overcome this problem, digital offset calibration techniques can be used to minimize these harmonics. To do this, a 5-bit programmable capacitor array (PCA) is used to estimate the static capacitance of the sensor. Then in each sampling phase of the feedback, the PCA is charged to a polarity opposite to that of the sense capaci-

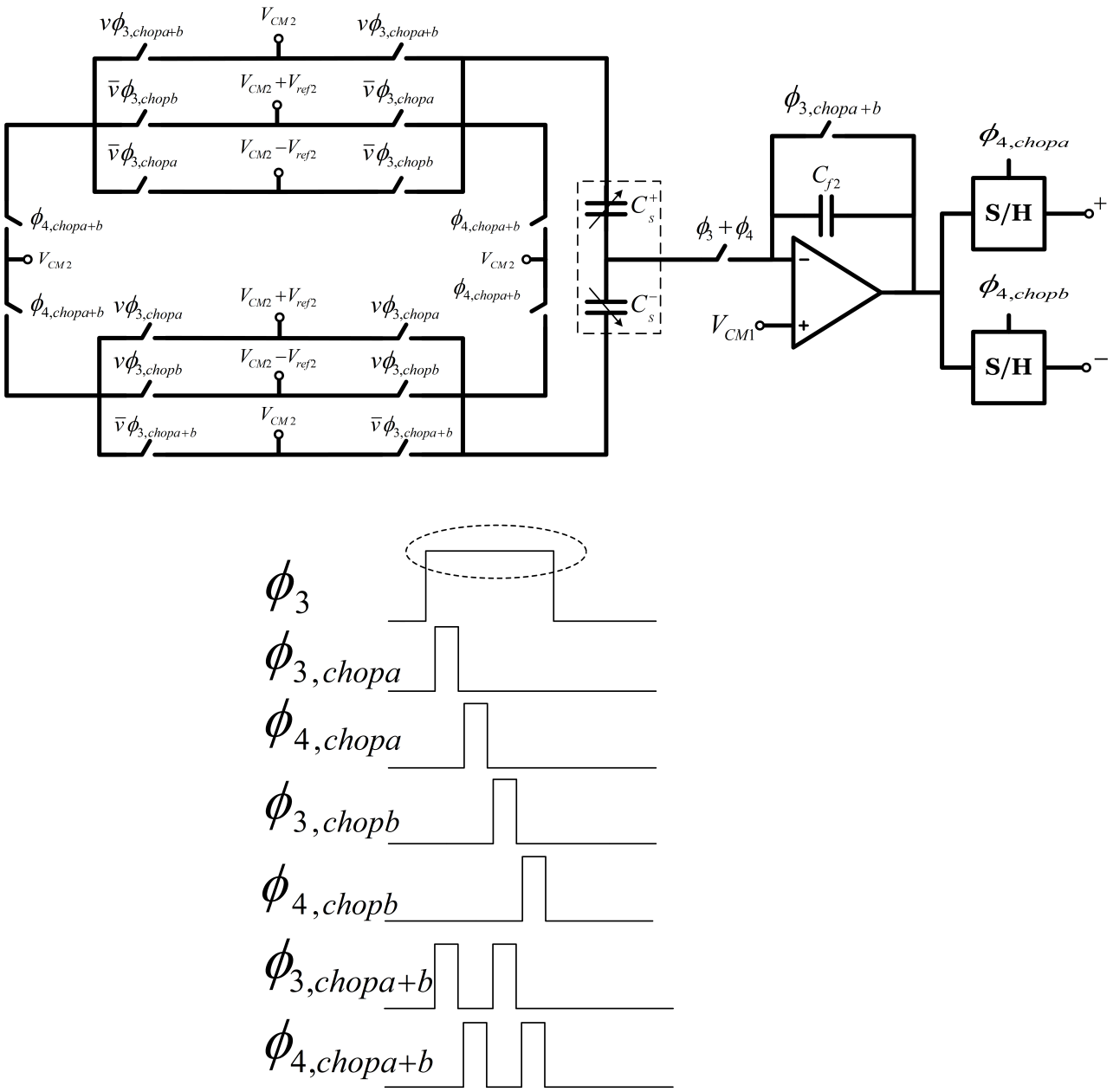


Figure 3.17: The feedback DAC stage of the proposed architecture adapted for differential circuitry. Notice that the power consumption of this stage is four times that of a the single-ended version.

tor. When the charge is then pushed to the output in the amplification phase, the static capacitance charge is largely offset by the charge on the PCA.

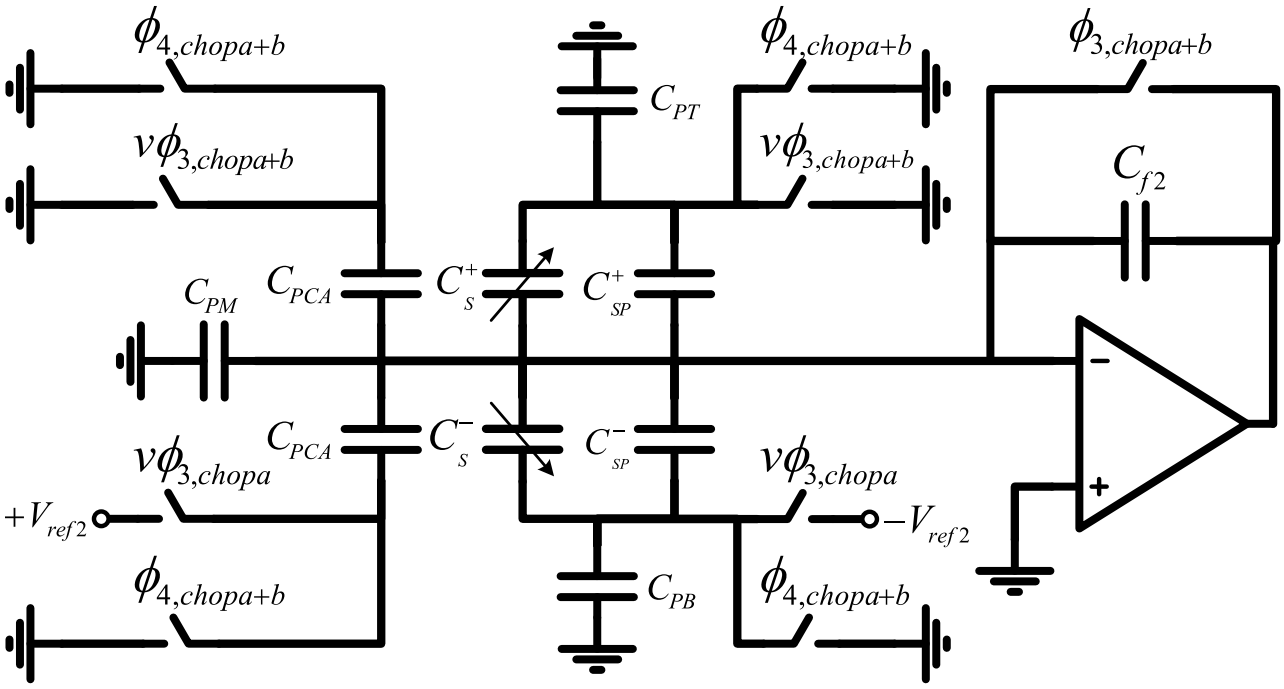


Figure 3.18: Offset cancellation technique demonstrated for the feedback DAC. Note that the switch clocks shown are for the case of a high quantizer output.

3.5.4 Common Mode Signal Boost

A final improvement to the design involves a subtle point regarding common mode signals. The output of the capacitance to voltage converter is proportional to V_{ref_1} and therefore, to a first degree, a higher V_{ref_1} can achieve a higher signal power and better SNDR. However, to increase V_{ref_1}, this also has to be accompanied by a higher common mode voltage for the op-amps of the amplifier. Since the implementation of the system uses a 1.2 and 0 volt supplies [20], the front end amplifier is therefore made with an NMOS differential pair to have a higher common mode, V_{CM_1}, ranging from 900 mV - 1000 mV. At the same time, however, to turn on the switches for the input stage, the clock signals must switch from 0 to at least $V_{CM_1} + V_{ref_1}$. Rather than make all the clocks high voltage, a level shifter circuit is used to change the signal for the amplifier chopping clocks from 1.2 V supply to 3.3 V supply. A simplified version of the circuit used for this is shown in Fig. 3.19.

[20] IBM 0.13 μm technology

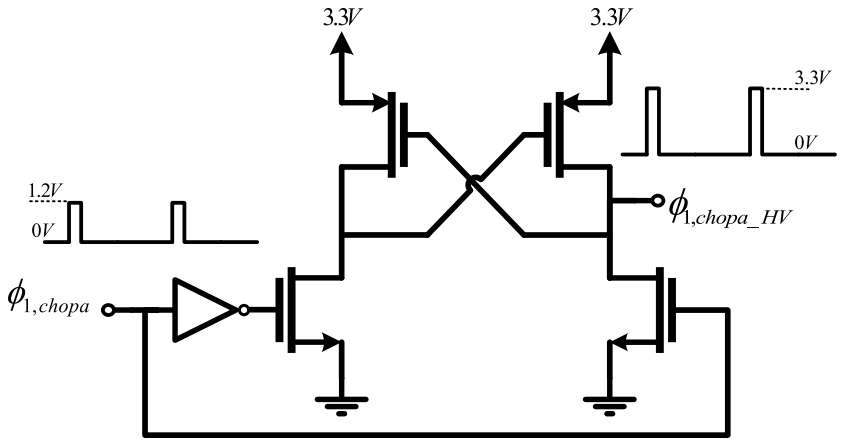


Figure 3.19: Level shifter used to change the clock level for the reference voltage sampling switches.

3.5.5 *Full System*

A differential first order system taking into account the above improvements is shown in Fig. 3.20.

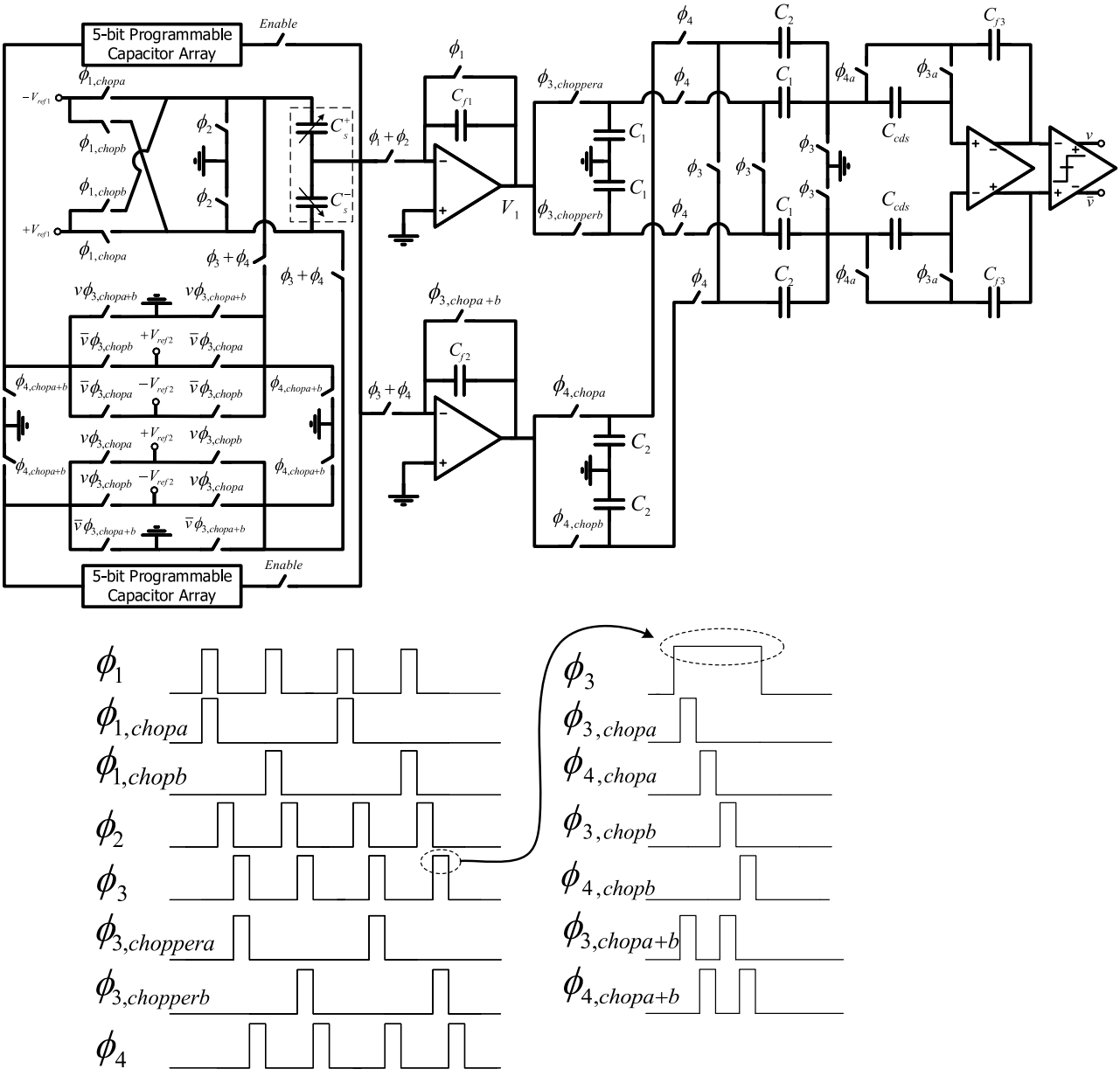


Figure 3.20: Practical implementation of the proposed system shown in Fig. 3.10 with offset cancellation network, chopper stabilization and correlated double sampling. The chopper stabilization also creates a pseudo differential signal for later stages.

3.5.6 Simulations and Analysis

To demonstrate the effectiveness of the system in suppressing harmonics and achieving high linearity, a circuit level thermal noise simulation of the second order system is performed. The system is similar to the block diagram in Fig. 3.9 and circuit of Fig. 3.20 with an additional integrator and feedback stage. The results shown are obtained by running a transient noise simulation. This simulation includes 1.5 pF of parasitic capacitance at each node of the accelerometer representing the pad and bondwire capacitance as well as 50 fF of static capacitance. The static capacitance is matched with a programmable capacitor array of 47.5 fF. The op-amps used are optimized for noise and power [72]. The accelerometer used has the parameters as shown in Table 3.1 and operated with a dynamic range of ±10 g corresponding for a differential capacitance ($C_s^+ - C_s^-$) of approximately 134 fF. The capacitor values used are $C_{f_1} = 800$ fF, $C_{f_2} = 800$ fF, $C_1 = 900$ fF, $C_2 = 900$ fF, $C_{f_3} = 900$ fF. The reference voltage for the converter stage is $V_{ref_1} = 950$ mV and for the DAC feedback stage $V_{ref_2} = 480$ mV. The sampling frequency is $F_s = 1024$ KHz and the signal bandwidth is 250 Hz.

Parameter	**Symbol**	**Value**
Capacitance at rest	C_s	600 fF
Capacitive sensitivity	$\frac{C_s^+ - C_s^-}{a}$	4.5 fF/g
Natural frequency	ω_n	3.0 KHz
Displacement at rest	d	2.50 μm
Accelerometer mass	m	2.0 $\times 10^{-8}$ kg
Spring constant	k	7.1 N/m
Damping coefficient	b	7.2 $\times 10^{-4}$ Ns/m

Table 3.1: Accelerometer specifications used for simulations. Notice that these coefficients are different than ones used for the single-ended simulations.

We look at the output spectrum in two places at the same time. Fig. 3.21 shows the output at the front end of the voltage to capacitance converter (node V_1 in Fig. 3.20). The output at this stage is neither ratiometric nor charge balanced and as a result has a large third order harmonic. Fig. 3.22 then shows the spectrum of the output bitstream (output of the comparator). The feedback creates a charge balanced ratiometric output that eliminates the third order harmonic to below the noise floor.

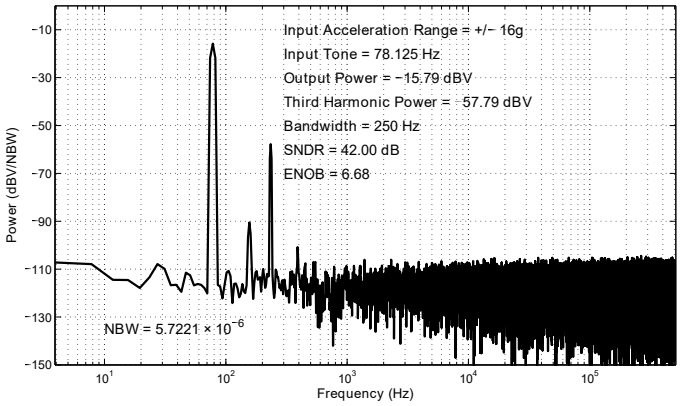


Figure 3.21: Power spectral density at the output of the capacitance to voltage converter (node V_1 in Fig. 3.20) with thermal noise.

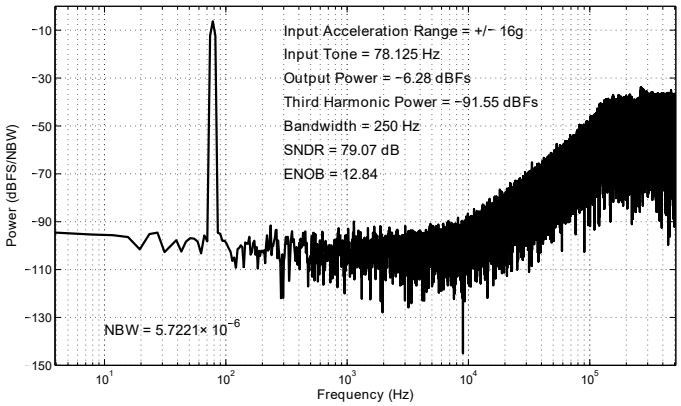


Figure 3.22: Power spectral density of the output bit stream for the proposed system with thermal noise.

Circuit Block	**Current Consumption**	**Power**
Front End (Converter and DAC)	275 μA	330.0 μW
First Integrator Stage	75 μA	90.0 μW
Second Integrator Stage	54 μA	64.8 μW
Auxiliary Circuits	130 μA	156.0 μW
Total Power	534 μA	640.8 μW

Table 3.2: Simulated power consumption for the proposed system.

Table 3.2 summarizes the simulated power consumption for the implemented system in 0.13 μm CMOS technology. Auxiliary circuits include the comparator, the clock generation, and the biasing circuitry. The circuit consumes 640 μW (2.6 μW/Hz) of power from a 1.2 V supply.

3.5.7 Gain Coefficients Flexibility

To have a circuit that has correct NTF and STF, we need to have some flexibility in the parameters of the design. Fig. 3.23 shows the circuit

with variable capacitors that are manually adjusted to allow for gain of the NTF and STF to be set separately. The feedback and feedforward capacitors in the initial stage make use of 2-bit array (with majority of adjustment performed though the reference voltages). The integrator stage capacitors make use of 3-bit capacitor array as to better adjust the full scale range of the output of the integrators. In each case, the op-amps were then designed to handle the worst case scenarios (maximum capacitive load).

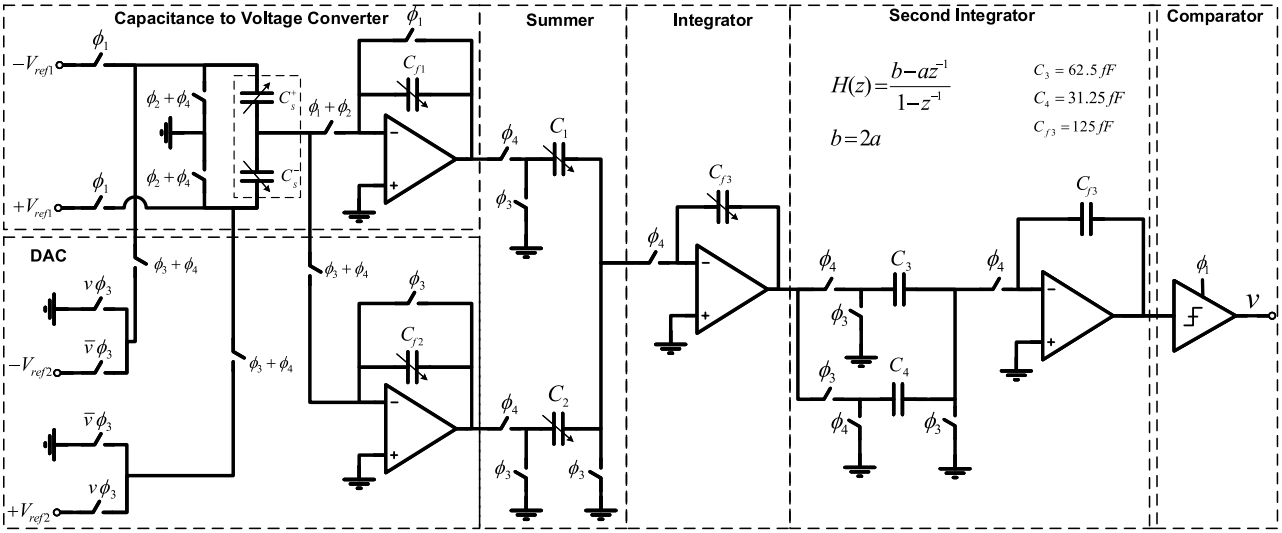


Figure 3.23: Single-ended version of the design showing gain coefficient flexibility using adjustable capacitor arrays (as well as reference voltage flexibility).

3.6 Dynamic Range Simulations

Dynamic range simulations for the architecture are shown in Fig. 3.24. The total harmonic distortion (THD) averages around −80 dB up to 3.75 g of acceleration or −0.56 dBFS owing to the robustness of the second order delta sigma architecture.

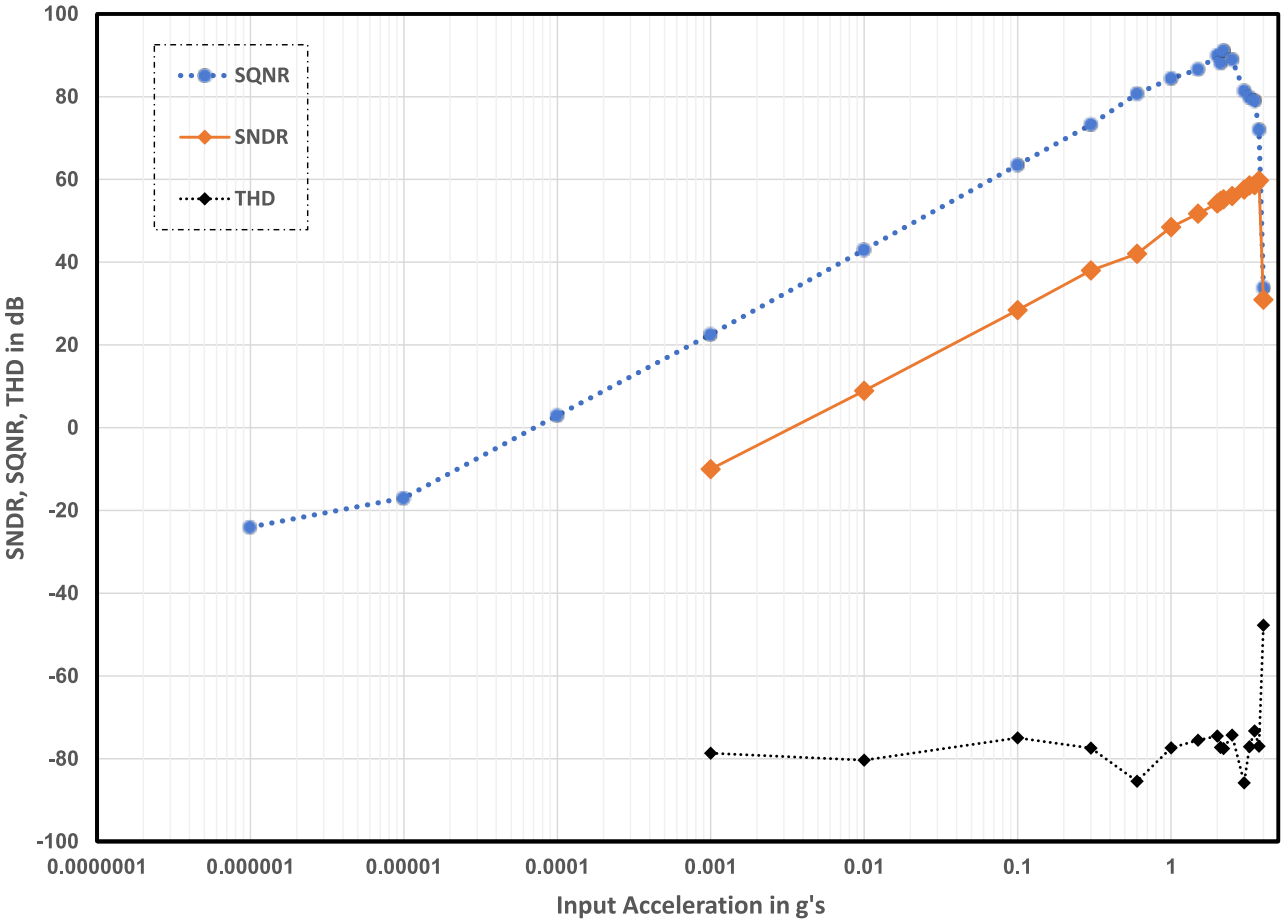


Figure 3.24: SNDR, SQNR and THD simulations for a 4 g full scale input.

The system can resolve at the low end 0.003 g and up to 3.75 g at the upper end[21] equaling to a spurious free dynamic range of 61.9 dB. It is important to note, however, that beyond an acceleration of 2.5 g the delta sigma modulator behaviour becomes erratic. The noise shaping, for example, no longer follows a second order response (40 dB/decade) but rather a first order response (20 dB/decade). Although the single tone tests above may indicate functionality, this is not guaranteed for

[21] large harmonics exists beyond 3.75 g

a band-limited signal[22]. Therefore, we will limit the usefulness of our system up to 2.5 g.

[22] A delta sigma modulator is a nonlinear system and linear theory should not be relied upon in all regions.

3.7 Conclusion

A novel charge balanced readout technique and system for capacitive accelerometers has been developed with adaptation to pseudo-differential output and direct digitization. Simulations show high output linearity at lower power consumption compared to recent open loop readout systems. Furthermore, the system can accommodate a wide range of sensor specifications and inputs by changing the gains of the transfer function to optimize fidelity. The system was implemented in 0.13 μm design and bondwired to a commercial accelerometer. The measurements of the design are discussed in Chapter 4.

4

Measurements

MEASUREMENTS in this chapter follow a natural progression towards proving the functionality of the proposed architecture. The measurements are divided into three sections as follows:

- **Section 4.1** treats the proposed system as a regular delta sigma modulator and characterizes its minimum detectable signal (noise floor) and linearity (SNDR). The results show that despite the non-conventional structure of the modulator (four phase clocks, different DAC feedback capacitor based on output, pseudo differential structure), the modulator functionality is preserved with fidelity and noise floors above 60 dB. This is encouraging as we proceed in testing the concept of the design (harmonic reduction) in Sections 4.2 and 4.3.
- **Section 4.2** aims to prove the concept of the system without specifically making use of an accelerometer. This is done by measuring the modulator functionality as before but introducing harmonics both in the DAC reference voltages and the feedforward reference voltages that closely mimic what would be expected from an accelerometer. The results show a high reduction in harmonics if correct coefficients are used for the harmonic terms.
- **Section 4.3** measures the system with a commercial surface micromachined accelerometer in x, y and z directions. The major challenge in these measurements is the production of a high fidelity acceleration signal at a precise frequency. By using a step motor, an accurate signal can be generated with some high frequency components (likely

due to environmental vibrations). These high frequency components do not cause issues as they do not interfere with the harmonics of the fundamental tone. The measured results from this test confirm that the proposed architecture achieves a ratiometric and charge balanced output reducing harmonics below the thermal noise floor.

For each measurement, the corresponding simulation is performed using transient noise analysis and compared to the measurements. The details of the simulation setup are discussed in Appendix B.

4.1 ADC Functionality Testing

Although the designed system has a very specific application for measuring differential accelerometer signals, the ASIC is first characterized as a regular ADC. This helps in determining the noise floor of the system and gives assurances that the proposed architecture is functional. Some modifications are required to generate signals that are appropriate for testing the ADC. These modifications and the results are discussed in this section first for a DC input (Section 4.1.1) and then for an AC input (Section 4.1.6).

The DC test results show that the system achieves a noise floor of 7.65 $\mu V/\sqrt{Hz}$ with sampling capacitors of 0.96 pF and 1.44 pF compared to a simulated value of 5.45 $\mu V/\sqrt{Hz}$. Conversely, the AC measurements achieve a SNDR of 62.9 dB compared to 66.4 dB in simulations.

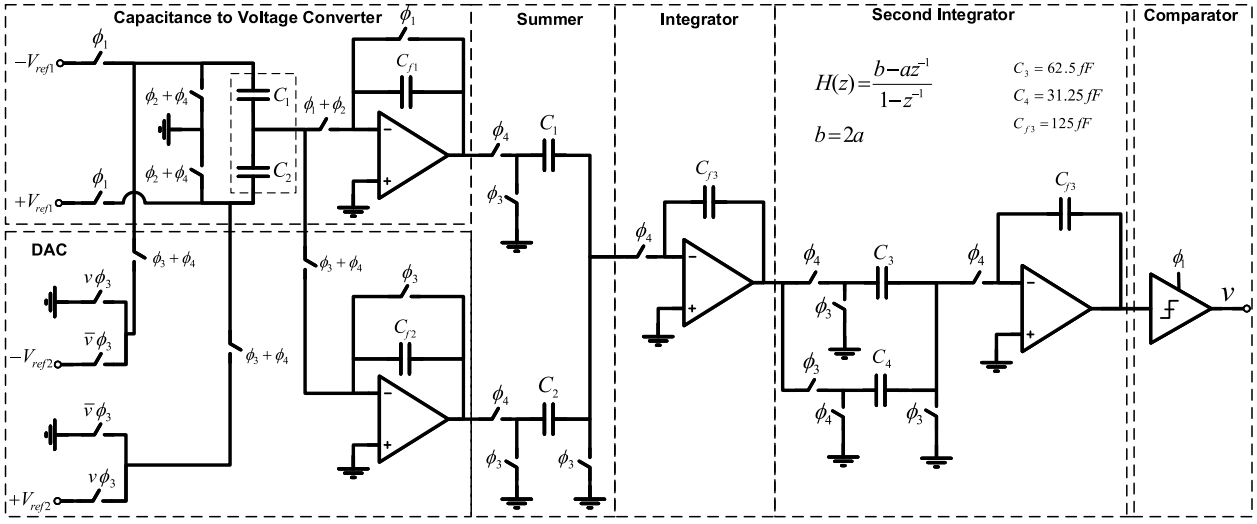


Figure 4.1: Circuit for DC testing. Note that the DC signals can be in or out of phase. In phase, the capacitor values add up, out of phase the capacitor values are subtracted.

4.1.1 DC Testing

DC testing is the process of placing two static capacitors, C_1 and C_2 in place of the accelerometer and intending to use the ASIC as a regular $\Delta\Sigma$ ADC without a signal. Due to the unconventional architecture of the system, however, some consideration is needed on how to generate these signals.

4.1.2 Generating a DC Value on Differential Branches

We are looking to have a DC output in both chopping phases. Depending on the values of input capacitors and the input reference voltages chosen, the output of the voltage converter will have the following values:

$$V_{out,\phi_{1,chopa}} = \frac{C_1 V_{ref_1^-} + C_2 V_{ref_1^+}}{C_{f1}} \ , \tag{4.1}$$

$$V_{out,\phi_{2,chopb}} = \frac{C_1 V_{ref_1^+} + C_2 V_{ref_1^-}}{C_{f1}} \ . \tag{4.2}$$

If the two reference voltages are *antiphase*, we hav

$$V_{ref_1^-} = -V_{ref_1} \ , \tag{4.3}$$

$$V_{ref_1^+} = +V_{ref_1} \ . \tag{4.4}$$

We can then write

$$V_{out,\phi_{1,chopa}} = V_{ref_1} \frac{C_1 - C_2}{C_{f1}} \ , \tag{4.5}$$

$$V_{out,\phi_{2,chopa}} = V_{ref_1} \frac{C_2 - C_1}{C_{f1}} \ . \tag{4.6}$$

This is somewhat undesirable for a DC test because the DC values for each branch of the differential circuit are now different. What we desire is to have the same DC value in both phases. To overcome this problem, we place the same voltage for both branches. In other words,

$$\begin{aligned} V_{ref_1^-} &= V_{ref_1^+} \\ &= V_{ref_1} \ . \end{aligned} \tag{4.7}$$

In this case, our output in each phase will be the same and given by:

$$V_{out,\phi_1} = V_{ref_1} \frac{C_1 + C_2}{C_{f1}} \ , \tag{4.8}$$

$$V_{out,\phi_2} = V_{ref_1} \frac{C_1 + C_2}{C_{f1}} \ . \tag{4.9}$$

This would work but by placing the same V_{ref} on both branches we have now effectively disabled the chopping capability of the system. This is not a major concern as we are using the DC test to get a gauge on the noise floor of the system.

4.1.3 DC Test Using Capacitive Array

Having devised a way to generate DC signals, we need to also have a flexible way to include sampling and feedback capacitors C_1 and C_2 without constantly soldering components onto the PCB board. One easy way to generate the different capacitors is to use the capacitor array system intended for offset cancellation. The capacitor array makes use of two sets of static capacitors with a 5-bit programmable array of variable capacitors. If we input a 00000 code for the capacitor array, one branch of the array will have a capacitance of $C_1 = 2 \times 470$ fF $= 940$ fF. The other branch will have a capacitance of $C_2 = 2 \times 470$ fF $+31 \times 16$ fF $= 1436$ fF. Using this combination for the sense capacitors, we get the power spectral density shown in Fig. 4.2.

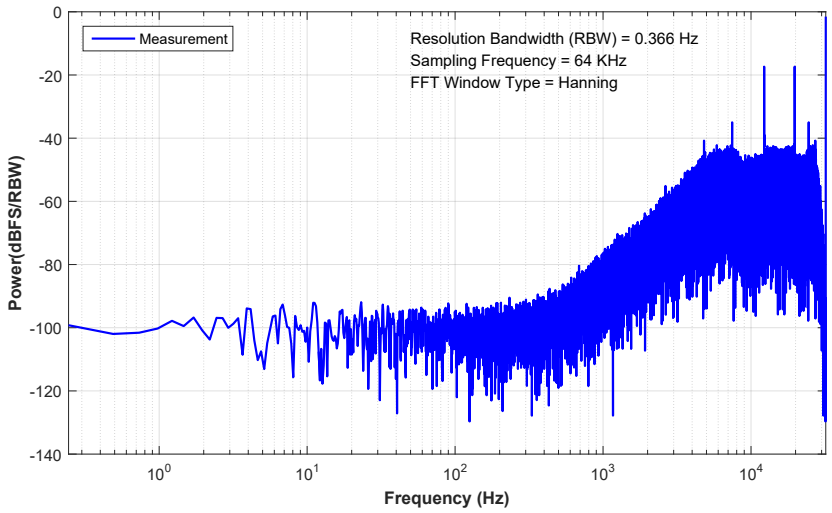


Figure 4.2: Measured output spectrum of the proposed architecture with DC input showing second order noise shaping. Reference voltages used are as follows: $V_{ref1+} = V_{ref1-} = 600$ mV, $V_{ref2+} = 800$ mV, $V_{ref2-} = 400$ mV, $V_{ref1,CM} = 600$ mV, $V_{ref2,CM} = 600$ mV.

4.1.4 Total Noise Floor and Expected SNDR

The total noise floor density can be calculated from the FFT graphs such as the one shown in Fig. 4.2. However, we must first determine the equivalent maximum input that the DAC output represents. Input-referred DAC outputs are found by determining the ADC input voltages which result in the same first integrator input as the DAC outputs.

Accordingly, we need to satisfy the following equation:

$$\frac{\Delta C}{C_{f1}} \cdot V_{ref_1^{\pm}} = \frac{C_{1,2}}{C_{f2}} \cdot V_{ref_2^{\pm}} \ , \tag{4.10}$$

where $\Delta C = C_1 - C_2$, C_{f1} is the feedback capacitance for the voltage converter and C_{f2} is the feedback capacitor for the DAC. Re-arranging the above and noting that the feedback capacitors are the same, the input-referred DAC output is equal to

$$V_{ref_1^{\pm}} = \frac{C_{1,2}}{\Delta C} \cdot V_{ref_2^{\pm}} \ . \tag{4.11}$$

Based on this, the *peak to peak* amplitude of the input corresponding to the FFT of Fig. 4.2 is approximately 0.95 volts. We can now use this value to obtain the noise floor as

$$\begin{aligned} \text{Noise Floor measured} &= \frac{\text{FFT Noise Floor Power} \times \text{Full Scale Power}}{\text{Resolution Bandwidth}} \\ &= \left(10^{\frac{-105}{10}}\right) \left(\frac{0.95}{2\sqrt{2}}\right)^2 \text{V}^2 \left(\frac{2^{20}}{64 \text{ KHz}}\right) \\ &= 5.8449 \times 10^{-11} \text{ V}^2/\text{Hz} \\ &= 7.645 \ \mu\text{V}/\sqrt{\text{Hz}} \ . \end{aligned} \tag{4.12}$$

To put this in perspective, assume that we have an input sinewave at half fullscale or with amplitude of 0.2375 V[1]. Therefore, the maximum expected SNDR at a bandwidth of 62.5 Hz will be

[1] As would be the necessary for a second order delta sigma modulator to be stable

$$\begin{aligned} \text{SNDR}_{\text{Max, measured}} &= \frac{\frac{0.2375^2}{2}}{5.8449 \times 10^{-11} \times 62.5 \text{ Hz}} \\ \boxed{\text{SNDR}_{\text{Max, Measured}} \approx 68.89 \text{ dB}} \ . \end{aligned} \tag{4.13}$$

4.1.5 DC Comparison to Simulation

The transient noise simulation of the above system is shown in Fig. 4.3. Based on this, the noise floor and maximum SNDR are given by:

$$\begin{aligned} \text{Noise Floor Simulation} &= \left(10^{\frac{-105.1}{10}}\right) \left(\frac{0.95}{2\sqrt{2}}\right)^2 V^2 \left(\frac{2^{19}}{64 \text{ KHz}}\right) \\ &= 2.8559 \times 10^{-11} \text{ V}^2/\text{Hz} \\ &= 5.3441 \ \mu\text{V}/\sqrt{\text{Hz}} \ , \end{aligned} \tag{4.14}$$

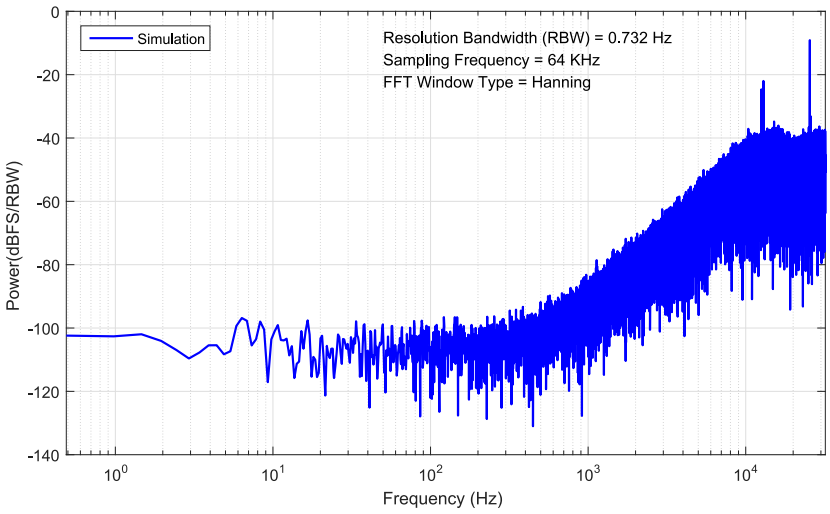


Figure 4.3: Simulated output spectrum of the proposed architecture with DC input.

$$\mathrm{SNDR}_{\text{Max, simulation}} = \frac{\frac{0.2375^2}{2}}{2.8559 \times 10^{-11} \times 62.5 \text{ Hz}}$$

$$\boxed{\mathrm{SNDR}_{\text{Max, simulation}} \approx 71.99 \text{ dB}} \,. \tag{4.15}$$

Therefore, there is a 3.1 dB discrepancy between the measured and simulated DC noise floors. There are several sources of error that can account for this. From the simulation perspective, the transient noise simulation bandwidth is limited to 100 MHz for speed purposes and this can underestimate the total noise of the system by 10%[2]. From the measurement perspective, noise sources from the power supply and reference voltages among others exist that must be carefully characterized. These sources become the limiting factor as the SNDR boundary is pushed above a 70 dB range. In other words, it becomes increasingly more difficult to measure high fidelity signals due to many noise sources that can come into effect. We expect to see the same discrepancy in the AC analysis as detailed in the next section.

[2] See Appendix B for details of noise simulation

4.1.6 AC Testing

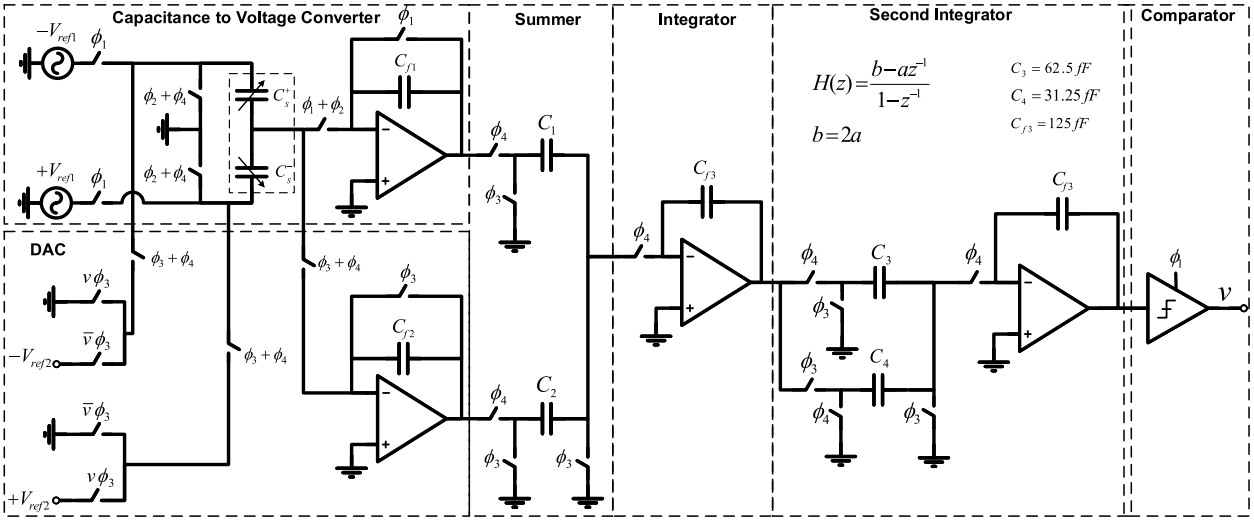


Figure 4.4: Circuit for AC testing. Note that the AC signals can be in or out of phase. In phase, the output signal is proportional to the sum of the capacitor. Out of phase, the output signal is proportional to the difference in input capacitors.

In AC testing, unlike DC testing, we require that the output of the amplifier stage be a signal that is differential. The capacitive accelerometer is a differential system with the capacitor values changing differentially according to:

$$C_s^+ = C_s \left(\frac{1}{1 - \frac{x}{d}} \right) , \tag{4.16}$$

$$C_s^- = C_s \left(\frac{1}{1 + \frac{x}{d}} \right) . \tag{4.17}$$

This shows that if we put a sinewave on one branch and the negative of the differential on the other branch, then as long we have perfectly matched capacitors C_1 and C_2, then the output, with the help of the chopper system, is pseudo differential. This situation, however, is not practical. It is very difficult and expensive to obtain accurate discrete capacitors that match well. Furthermore, even a slight difference is problematic and can saturate the amplifier.

The solution then is to put two different capacitors and feed them with differential signals. The differential signals are given by

$$V_{ref_1^+} = V_{ref_1,CM} + V_A \cdot \sin(2\pi f t) , \tag{4.18}$$

$$V_{ref_1^-} = V_{ref_1,CM} - V_A \cdot \sin(2\pi f t) . \tag{4.19}$$

Then using Fig. 4.4 as a reference, we can see that the output signal in each chopper phase will be given by

$$V_{out,AC\phi_{1,chopa}} = V_A \frac{C_1 - C_2}{C_{f1}} \ , \tag{4.20}$$

$$V_{out,AC\phi_{2,chopa}} = V_A \frac{C_2 - C_1}{C_{f1}} \ . \tag{4.21}$$

This is a differential signal and meets our purposes. The spectrum of the output with the above signals is shown in Fig. 4.5 achieving 62.9 dB SNDR and demonstrating the functionality of the ADC. A simulation of the system with the same reference voltages is shown in Fig. 4.6. As expected from DC characteristics, the simulations have a better SNDR by 3.5 dB and same reasoning as outlined previously can explain this discrepancy.

4.1.7 Conclusion

The results in this sections show that despite the unconventional structure, the proposed delta sigma modulator still preserves the noise shaping characteristics of a second order modulator and achieves fidelity above 60 dB. Having established the correct operation of the system, in the next two sections we look at determining whether the system is capable of reducing harmonics through charge balance.

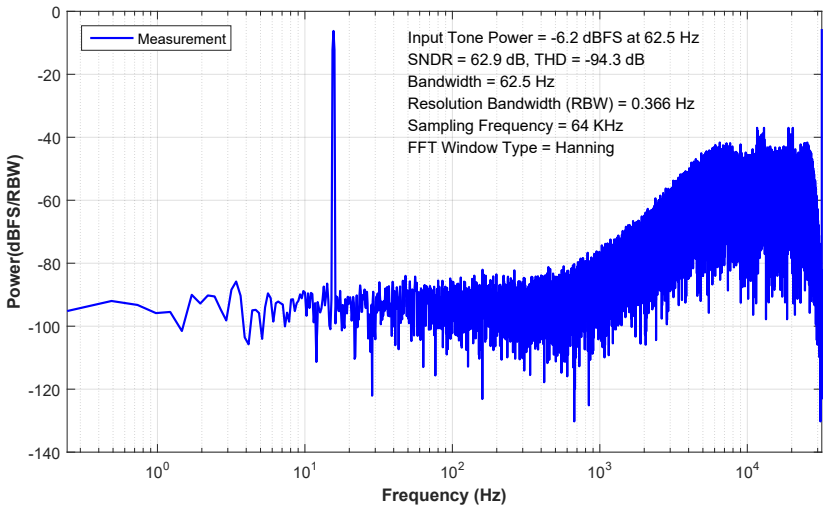


Figure 4.5: Measured output spectrum of the proposed architecture with input tone at 15.625 Hz showing second order noise shaping. Reference voltages used are as follows $V_{ref1+} = -V_{ref1-} = 0.25\sin(2\pi \cdot 15.625)$, $V_{ref2+} = 700$ mV, $V_{ref2-} = 500$ mV, $V_{ref1,CM} = 600$ mV, $V_{ref2,CM} = 600$ mV

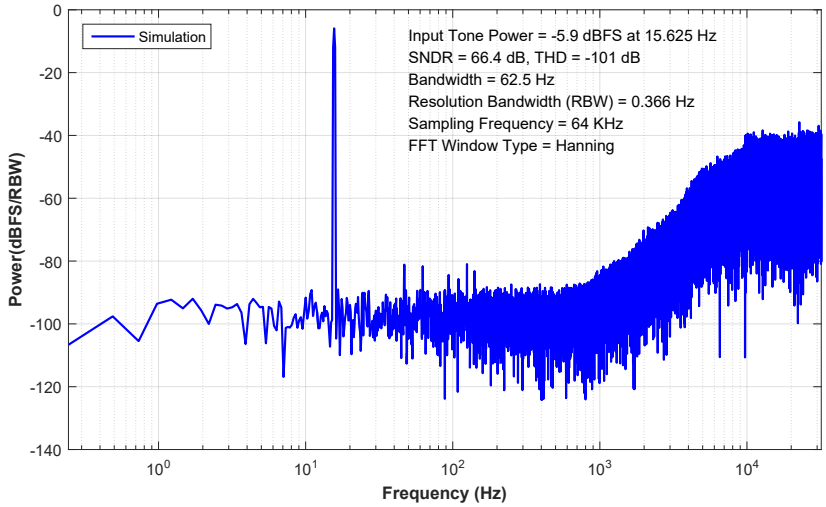


Figure 4.6: Simulated output spectrum of the proposed architecture with input tone at 15.625 Hz showing second order noise shaping.

4.2 Testing Using Generated Accelerometer Signals

Testing the proposed system with an accelerometer is challenging as it requires the additional cost of packaging the ASIC with accelerometers, as well as purchasing testing equipment for generating acceleration signals. Therefore, it is prudent to test the concept of the ASIC[3] before further effort in testing takes place.

[3] mainly harmonic reduction

The harmonic reduction capability of the ASIC can be proved by generating accelerometer signals electronically. In such a case, the roles

of the capacitor and voltage references are reversed. In an accelerometer, the voltage references are constant while the capacitance changes in a sinusoidal manner. In this case, the voltage references for both the signal and feedback stage are sinusoidal and capacitors are fixed. What remains is then to generate the correct reference voltages that closely match our model of the accelerometer. This is discussed further in the next section.

4.2.1 Generating Appropriate Voltage References to Model Accelerometer Signals

Recall that an accelerometer undergoing acceleration can be modeled as two varying capacitances according to

$$C_s^+ = \frac{C_s}{1-\frac{x}{d}} \qquad \text{and} \qquad C_s^- = \frac{C_s}{1+\frac{x}{d}} \ , \tag{4.22}$$

where C_s is the accelerometer capacitance at rest, x is the displacement [4] and d is the separation of capacitor plates. We like to mimic the above variable capacitor by having a fixed capacitor and a variable voltage. Expanding the equation for the positive sense capacitor C_s^+ we have

[4] sinusoidal or static

$$C_s^+ = \frac{C_s}{1-\frac{x}{d}} \tag{4.23}$$

$$= C_s\left(1+\frac{x}{d}+\left(\frac{x}{d}\right)^2+\left(\frac{x}{d}\right)^3+\ldots\right) \ . \tag{4.24}$$

Similarly for the negative capacitor we have

$$C_s^- = \frac{C_s}{1+\frac{x}{d}} \tag{4.25}$$

$$= C_s\left(1-\frac{x}{d}+\left(\frac{x}{d}\right)^2-\left(\frac{x}{d}\right)^3+\ldots\right) \ . \tag{4.26}$$

Now substituting the generic differential signals into the ratiometric

equation and expanding we have

$$\begin{aligned} V_o &= \frac{C_s\left[1+\frac{x}{d}+\left(\frac{x}{d}\right)^2+\left(\frac{x}{d}\right)^3+\ldots\right]-C_s\left[1-\frac{x}{d}+\left(\frac{x}{d}\right)^2-\left(\frac{x}{d}\right)^3+\ldots\right]}{C_s\left[1+\frac{x}{d}+\left(\frac{x}{d}\right)^2+\left(\frac{x}{d}\right)^3+\ldots\right]+C_s\left[1-\frac{x}{d}+\left(\frac{x}{d}\right)^2-\left(\frac{x}{d}\right)^3+\ldots\right]} \\ &= \frac{2\frac{x}{d}\left[1+\left(\frac{x}{d}\right)^2+\left(\frac{x}{d}\right)^4+\ldots\right]}{2C_s\left[1+\left(\frac{x}{d}\right)^2+\left(\frac{x}{d}\right)^4+\ldots\right]} \\ &= \frac{x}{d}\frac{1}{C_s}\,, \end{aligned} \tag{4.27}$$

where x is our desired signal (for example a single tone sinusoid for testing purposes). Therefore, as long as we can generate a signal that has harmonic coefficients as shown above, the proposed system will remove them. Is it possible to generate such a signal? Assume we have a differential signal, then this signal has the attribute that

$$V_D^+ = V_{DC} + v_{ac} \qquad \text{and} \qquad V_D^- = V_{DC} - v_{ac}\,, \tag{4.28}$$

where v_{ac} is a single tone sinusoidal signal. Any active circuitry has a non-linearity associated with it that is often modeled as a memoryless Taylor series[5]. Using the Taylor series approximation, we have

$$V_o^+ = V_{DC} + a_1 v_{ac} + a_2 v_{ac}^2 + a_3 v_{ac}^3 + \ldots \tag{4.29}$$

$$V_o^- = V_{DC} - a_1 v_{ac} + a_2 v_{ac}^2 - a_3 v_{ac}^3 + \ldots\,. \tag{4.30}$$

[5] If a circuit has any capacitive elements, then strictly speaking a memoryless non-linearity model is not appropriate. In that case, a Volterra series expansion is needed.

Now assume we put the above expression into the familiar ratiometric form of Eq. (4.27). Our aim is to see the relationship between the harmonic coefficients that allow us to have cancellation. First, let's manipulate the equation so it is in the same form as that shown in Eq. (4.27):

$$V_{ref_1}^+ = V_{DC}\left[1+\frac{a_1}{V_{DC}}v_{ac}+\frac{a_2}{V_{DC}}v_{ac}^2+\frac{a_3}{V_{DC}}v_{ac}^3+\ldots\right] \tag{4.31}$$

$$V_{ref_1}^- = V_{DC}\left[1-\frac{a_1}{V_{DC}}v_{ac}+\frac{a_2}{V_{DC}}v_{ac}^2-\frac{a_3}{V_{DC}}v_{ac}^3+\ldots\right]\,. \tag{4.32}$$

Now placing the above equation into the ratiometric output that we

expect from the system, we have

$$V_{\text{out}} = \frac{V^{+}_{differential} - V^{-}_{differential}}{V^{+}_{differential} + V^{-}_{differential}} \tag{4.33}$$

$$= \frac{V_{DC}\left[1 + \frac{a_1}{V_{DC}}v_{ac} + \frac{a_2}{V_{DC}}v_{ac}^2 + \frac{a_3}{V_{DC}}v_{ac}^3 + \ldots\right] - V_{DC}\left[1 - \frac{a_1}{V_{DC}}v_{ac} + \frac{a_2}{V_{DC}}v_{ac}^2 - \frac{a_3}{V_{DC}}v_{ac}^3 + \ldots\right]}{V_{DC}\left[1 + \frac{a_1}{V_{DC}}v_{ac} + \frac{a_2}{V_{DC}}v_{ac}^2 + \frac{a_3}{V_{DC}}v_{ac}^3 + \ldots\right] + V_{DC}\left[1 - \frac{a_1}{V_{DC}}v_{ac} + \frac{a_2}{V_{DC}}v_{ac}^2 - \frac{a_3}{V_{DC}}v_{ac}^3 + \ldots\right]} \tag{4.34}$$

$$= \frac{\left[2\frac{a_1}{V_{DC}}v_{ac} + 2\frac{a_3}{V_{DC}}v_{ac}^3 + 2\frac{a_5}{V_{DC}}v_{ac}^5 + \ldots\right]}{V_{DC}\left[2 + 2\frac{a_2}{V_{DC}}v_{ac}^2 + 2\frac{a_4}{V_{DC}}v_{ac}^4 + \ldots\right]} \tag{4.35}$$

$$= \frac{2\frac{a_1}{V_{DC}}v_{ac}\left[1 + \frac{a_3}{a_1}v_{ac}^2 + \frac{a_5}{a_1}v_{ac}^4 + \ldots\right]}{2V_{DC}\left[1 + \frac{a_2}{V_{DC}}v_{ac}^2 + \frac{a_4}{V_{DC}}v_{ac}^4 + \ldots\right]} \tag{4.36}$$

$$= \frac{a_1}{V_{DC}^2}v_{ac}\frac{\left[1 + \frac{a_3}{a_1}v_{ac}^2 + \frac{a_5}{a_1}v_{ac}^4 + \ldots\right]}{\left[1 + \frac{a_2}{V_{DC}}v_{ac}^2 + \frac{a_4}{V_{DC}}v_{ac}^4 + \ldots\right]} \tag{4.37}$$

$$= \frac{a_1}{V_{DC}^2}v_{ac}\left[1 + \frac{a_3}{a_1}v_{ac}^2 + \frac{a_5}{a_1}v_{ac}^4 + \ldots\right]\left[1 - \frac{a_2}{V_{DC}}v_{ac}^2 - \frac{a_4}{V_{DC}}v_{ac}^4 + \ldots\right] \tag{4.38}$$

$$= \frac{a_1}{V_{DC}^2}v_{ac}\left[1 - \frac{a_2}{V_{DC}}v_{ac}^2 - \frac{a_4}{V_{DC}}v_{ac}^4 + \frac{a_3}{a_1}v_{ac}^2 - \frac{a_2}{V_{DC}}\frac{a_3}{a_1}v_{ac}^4 - \frac{a_4}{V_{DC}}\frac{a_3}{a_1}v_{ac}^6 + \frac{a_5}{a_1}v_{ac}^4 - \frac{a_2}{V_{DC}}\frac{a_5}{a_1}v_{ac}^6 - \frac{a_4}{V_{DC}}\frac{a_5}{a_1}v_{ac}^8\right] \tag{4.39}$$

$$= \frac{a_1}{V_{DC}^2}v_{ac}\left[1 + \left(\frac{a_3}{a_1} - \frac{a_2}{V_{DC}}\right)v_{ac}^2 - \left(\frac{a_4}{V_{DC}} - \frac{a_2}{V_{DC}}\frac{a_3}{a_1} - \frac{a_5}{a_1}\right)v_{ac}^4 - \left(\frac{a_4}{V_{DC}}\frac{a_3}{a_1} - \frac{a_2}{V_{DC}}\frac{a_5}{a_1}\right)v_{ac}^6 - \frac{a_4}{V_{DC}}\frac{a_5}{a_1}v_{ac}^8\right] . \tag{4.40}$$

In order for the terms in the brackets to cancel out, we need the following equations to hold:

$$a_1 = V_{DC}\frac{a_3}{a_2} \qquad \text{and} \qquad a_1 = V_{DC}\frac{a_5}{a_4} . \tag{4.41}$$

The moral of this derivation is that there is no circuit element that we can built to give us precise known values of harmonic coefficients. As such, to have harmonics with correct coefficients, we need to specifically generate signals and add them together to create the desired output harmonics. One solution to the above is to make $a_2 = a_3 = a_4 = a_5 = 1$. In this case, then $a_1 = V_{DC}$ or the gain of the circuit would be equivalent

to the DC magnitude. Other arrangements can also be made where the gain is made larger or smaller than V_{DC} using the equations above.

Another complication is that we cannot generate all harmonics due to limitations of the test equipment. However, the ratiometric equation still holds as long as an odd number of harmonics are present. For example, if we have a signal that includes the second and third harmonic (with correct coefficients), then the ratiometric output will still remove both harmonics. This is the approach taken.

Finally, one caveat to the above analysis is that it has been performed for a single-ended circuit and does not expand well to the pseudo-differential structure. The differential version would require four different voltage sources that is impractical to generate and requires changes to the differential circuit. Therefore, to test harmonic reduction, a single-ended version of the circuit was used.

4.2.2 Simulations with Generated Accelerometer Signals

Based on the analysis above, a set of input signals that will mimic the output signal of an accelerometer[6] is given by

[6] at DC and low frequencies

$$\begin{aligned} V^{+}_{ref_1} = \quad & + V_{ref_1} + V_{ref_1} A \sin(2\pi \cdot ft) \\ & + V_{ref_1} \frac{A^2}{2} \left[1 - \cos(2\pi t)\right] \\ & + V_{ref_1} \frac{A^3}{4} \left[3\sin(2\pi \cdot ft) - \sin(2\pi \cdot 3ft)\right] \ , \end{aligned} \tag{4.42}$$

$$\begin{aligned} V^{-}_{ref_1} = \quad & - V_{ref_1} + V_{ref_1} A \sin(2\pi \cdot ft) \\ & - V_{ref_1} \frac{A^2}{2} \left[1 - \cos(2\pi t)\right] \\ & + V_{ref_1} \frac{A^3}{4} \left[3\sin(2\pi \cdot ft) - \sin(2\pi \cdot 3ft)\right] \ . \end{aligned} \tag{4.43}$$

For the feedback reference voltages, the structure would be the same,

but we may need to change the DC values. As such, we can write

$$\begin{aligned} V^{+}_{ref_2} = \quad & + V_{ref_2} + V_{ref_2} A \sin(2\pi \cdot ft) \\ & + V_{ref_2} \frac{A^2}{2} [1 - \cos(2\pi t)] \\ & + V_{ref_2} \frac{A^3}{4} [3\sin(2\pi \cdot ft) - \sin(2\pi \cdot 3ft)] \ , \end{aligned} \tag{4.44}$$

$$\begin{aligned} V^{-}_{ref_2} = \quad & - V_{ref_2} + V_{ref_2} A \sin(2\pi \cdot ft) \\ & - V_{ref_2} \frac{A^2}{2} [1 - \cos(2\pi t)] \\ & + V_{ref_2} \frac{A^3}{4} [3\sin(2\pi \cdot ft) - \sin(2\pi \cdot 3ft)] \ . \end{aligned} \tag{4.45}$$

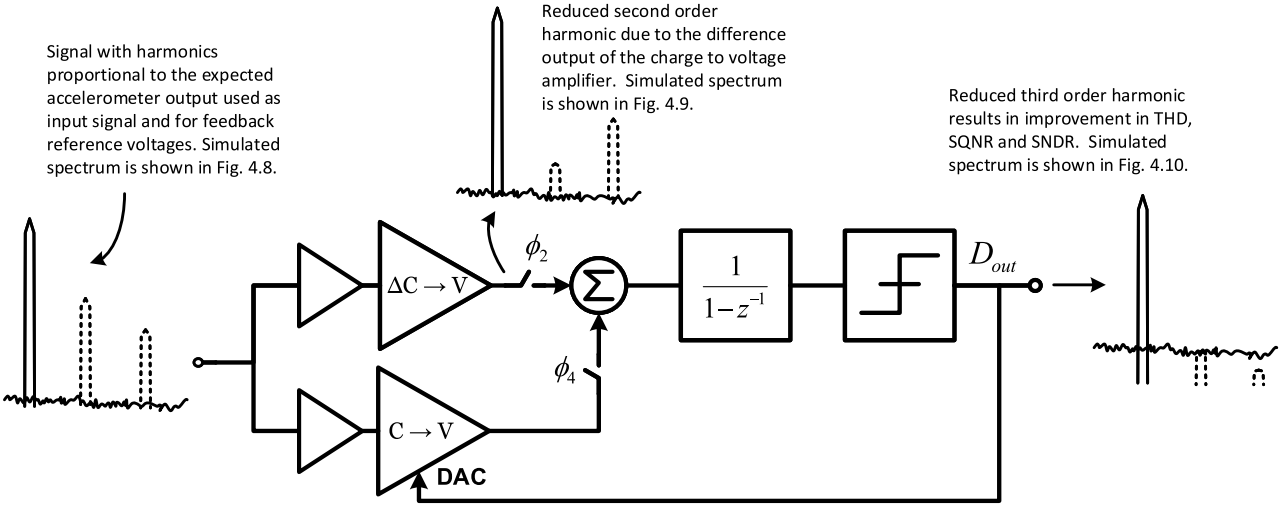


Figure 4.7: Simulation and test setup to demonstrate the harmonic reduction capability of the proposed system.

The simulation setup is demonstrated in Fig. 4.7. Only the second and third order harmonics are used for the signals as we are limited by the test equipment setup. The output of the capacitive voltage converter (Fig. 4.9) reduces the second order (and even order) harmonics. The output of the ADC (Fig. 4.10) then reduces the third harmonic below the noise floor.

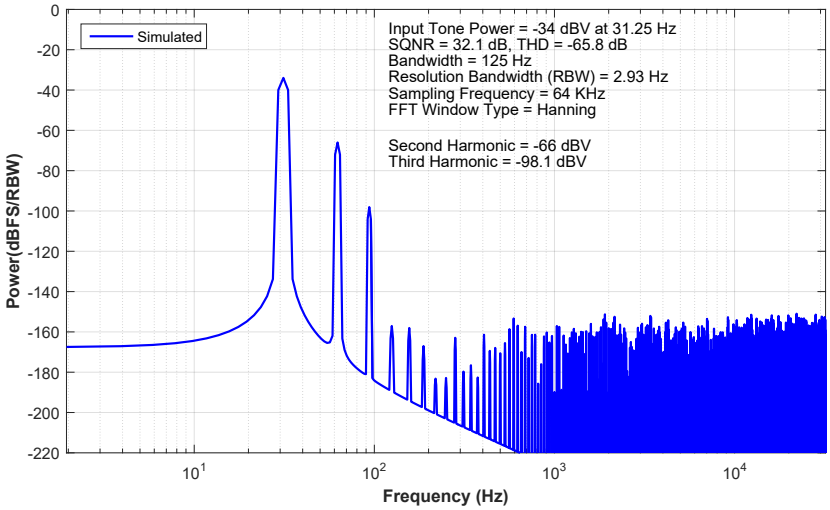


Figure 4.8: Spectrum of the signal with harmonics proportional to the expected accelerometer output. This signal is used as an input signal to the system and for the feedback reference voltages.

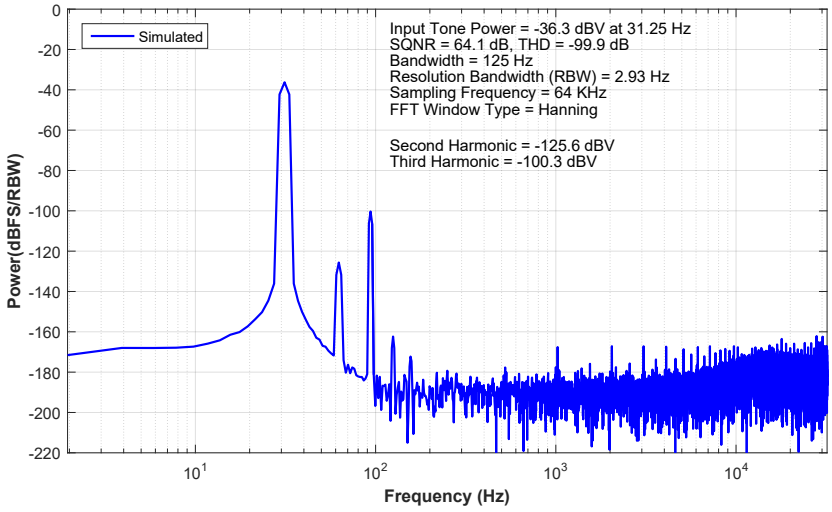


Figure 4.9: Simulated spectrum at the output of the capacitance to voltage converter with the input signal and reference voltages chosen to mimic the accelerometer output. Notice that this stage significantly reduces the second order harmonic.

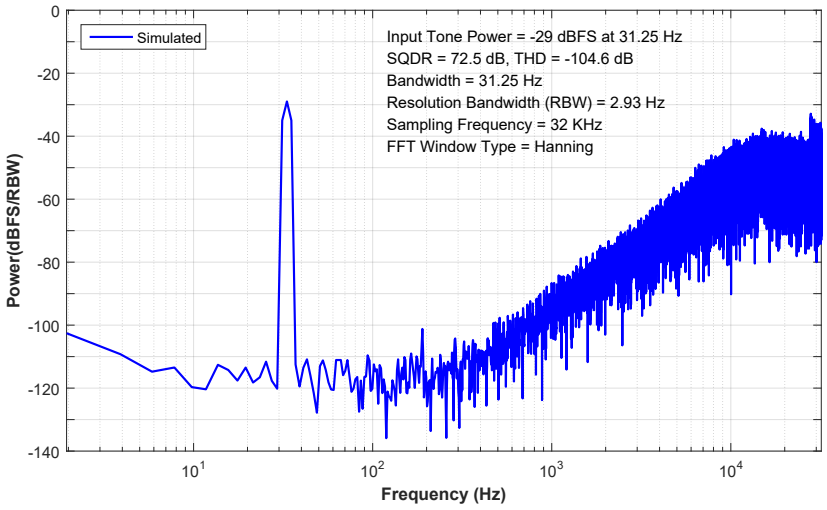


Figure 4.10: Simulated output spectrum of the proposed system with input signal and reference voltages chosen to mimic the accelerometer output.

4.2.3 Measurements with Generated Accelerometer Signals

Test setup for measurements was similar to the previous simulations. To observe the harmonics, we change the feedforward or input references to the voltages shown in Eq. (4.42) and (4.43) and use static DC references for the DAC. The resulting output spectrum is shown in Fig. 4.11[7]. Note that the second order harmonic is reduced below the noise floor due to the differential output of the voltage converter but the third harmonic remains as expected and confirmed through simulations.

[7] This technique allows us to observe the output harmonic of the capacitance to voltage converter without capturing the data specifically at this node.

Fig. 4.12 then shows the output of the ADC with the DAC reference voltages replaced by their AC counterparts shown in Eq. (4.44) and (4.45). Although having a changing reference voltage is unconventional, this setup with harmonic coefficients chosen correctly, reduces the output third harmonic to below the noise floor improving on the SNDR.

These results confirm that the proposed system, *with correct harmonic coefficients*, reduces the third harmonic below the noise floor. Theoretically, this concept can be expanded to higher order harmonics with proper test equipment but regardless, the results are encouraging enough to continue testing with a bondwired accelerometer.

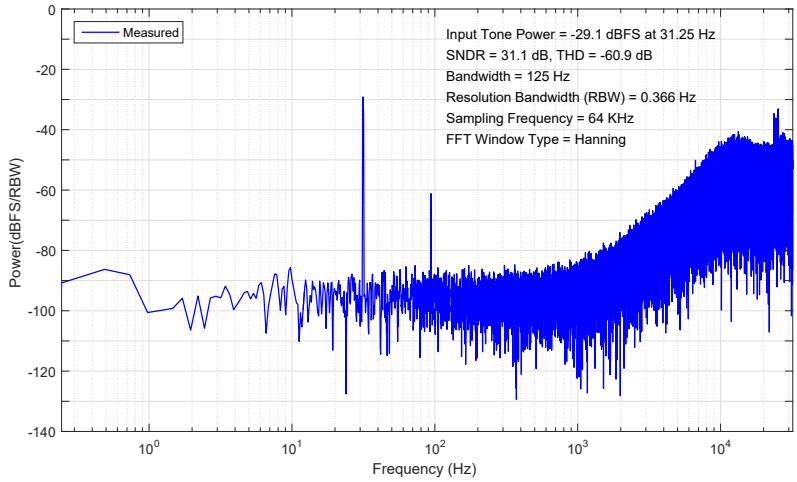


Figure 4.11: Measured output spectrum of the system with input references given by Eq. (4.42) and (4.43) and DC feedback references.

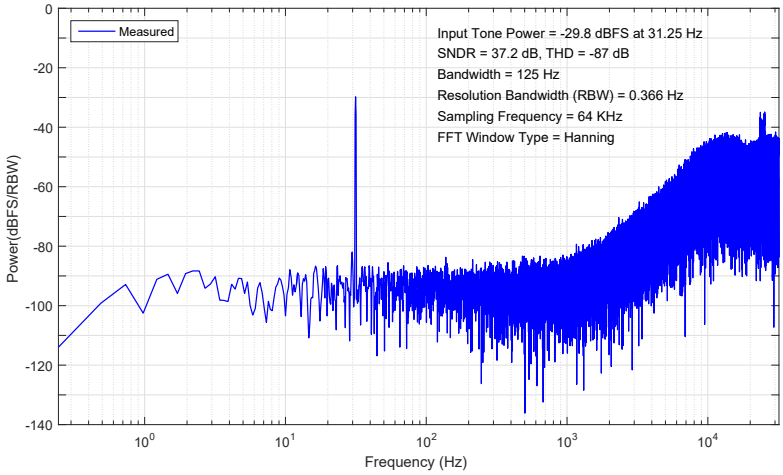


Figure 4.12: Measured output spectrum of the system with input references given by Eq. (4.42) and (4.43) and AC feedback references given by Eq. (4.44) and (4.45).

4.3 Accelerometer Testing

Accelerometer testing was performed by co-packaging a raw commercial accelerometer with the ASIC in a QFN package. A die photograph of one package is shown in Fig. 4.13.

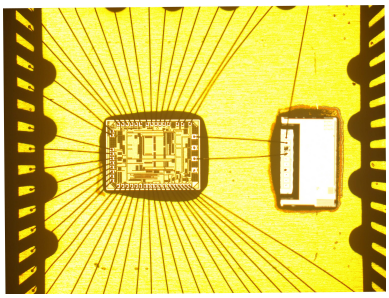


Figure 4.13: QFN package with bond-wired IC chip and accelerometer.

4.3.1 Overcoming Challenges in Accelerometer Testing

Two main challenges in testing the accelerometer are generating a pure tone for testing and dealing with the relatively low g forces that can be achieved with the test equipment available. These challenges and solutions are described below.

4.3.2 Generating a Pure Sinusoidal Acceleration

One of the main challenges in testing the accelerometer is generating a pure sinusoidal acceleration needed to drive the accelerometer. As the ASIC is designed for harmonic reduction, it is important to have a properly characterized acceleration signal. This is very challenging as many environment conditions (wind, foot steps, car movement) create small unwanted vibrational signals.

Testing was further challenged by the large PCB size and wiring required for powering the ASIC and reading out the data. Many different architectures and test setups were attempted including the use of a pendulum, 3D printer, and clay pottery spinners. These setups failed either due to impracticality or high noise characteristics of the generated vibrations. The best compromise was achieved by using a step motor. Details of the setup and programming are shown in Appendix H.

To test the purity of the generated acceleration signal, we make use of a commercial acceleration tracker [75]. Due to the limitations of the step motor torque, and the requirement to have tones that fall within a band, only two acceleration frequencies could be generated at 3.90625 Hz and 7.8125 Hz. These signals in the time domain are shown in Fig. 4.14 and Fig. 4.15 respectively.

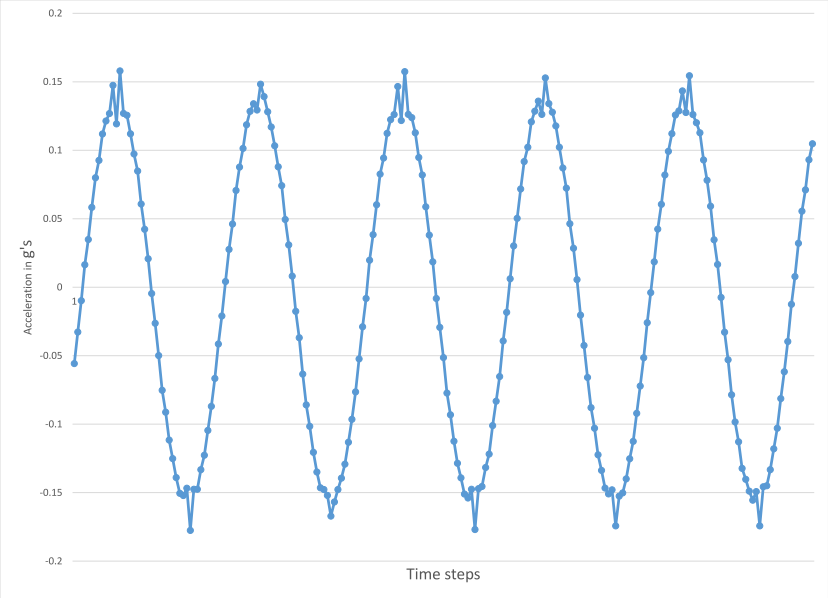


Figure 4.14: Sinusoidal acceleration signal generated using a step motor at 3.90625 Hz with magnitude of ±0.15 g. Notice the irregularity at the top and bottom of the sine wave indicating a change in direction of the motor.

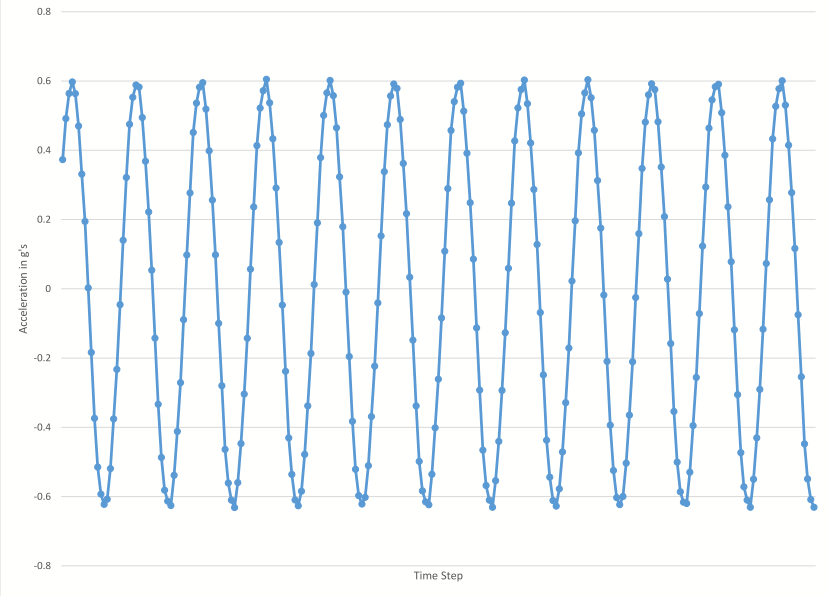


Figure 4.15: Sinusoidal acceleration signal generated using a step motor at 7.8125 Hz with magnitude of ±0.6 g.

4.3.3 Overcoming Problems with the Small Signal Tone

The previous section showed that with the use of a step motor, a relatively pure acceleration tone can be achieved. The structure of the motor setup also makes it ideal for a test setup with the large PCB[8]. However, a second issue is the low acceleration achievable with the step

[8] 20 cm x 20 cm

motor which is below ±1 g. Fortunately, the architecture proposed is specifically designed to maximize signal fidelity by choosing an appropriate set of feedforward and feedback reference voltages. Assume that we choose the DAC reference voltages to be $\pm V_{ref_2}$. Then the full scale input that is associated with these reference voltages is related to the signal reference voltages, $\pm V_{ref_1}$ such that the following equality holds:

$$\frac{\Delta C}{C_{f1}} \cdot V_{ref_1^{\pm}} = \frac{C_s}{C_{f2}} \cdot V_{ref_2^{\pm}} \ , \tag{4.46}$$

where ΔC is the *maximum* amplitude of capacitance change for the intended application[9], C_{f1} is the feedback capacitance for the voltage converter and C_{f2} is the feedback capacitor for the DAC. Re-arranging the above we get

[9] This value can change significantly in x, y and z directions and as well across dies in the same direction as will be shown later.

$$V_{ref_1^{\pm}} = \frac{C_s}{\Delta C} \cdot V_{ref_2^{\pm}} \ . \tag{4.47}$$

Now assume that we choose the maximum acceleration (0 dBFS) to be 4 g or a change in capacitance of $\Delta C = 4 \times 4.5$ fF/g = 18 fF. Accordingly, we need to find a voltage combination that satisfies the above equation. Since the right hand side of the above equation is much larger due to the presence of the small ΔC value, we need to choose a relatively small DAC reference voltage. Assume as a first pass, we choose $V_{ref_2^{\pm}} = \pm 25$ mV, then

$$\begin{aligned} V_{ref_1^{\pm}} &= \frac{320 \text{ fF}}{18 \text{ fF}} \cdot \pm 25 \text{ mV} \\ &= \pm 400 \text{ mV} \ , \end{aligned} \tag{4.48}$$

with a common mode of 600 mV this equates to a reference voltages of $V_{ref_1^{+}} = 1000$ mV and $V_{ref_1^{-}} = 200$ mV. In the following sections, these reference voltages are slightly changed to accommodate different sensitivities (fF/g) associated with x, y and z direction sensors.

4.3.4 X Direction Testing

4.3.5 X Direction Specifications

The full parameters for the x-direction are shown in Table 4.1. The key take away from this this table is the large variance across the dies. Therefore, for optimal results, the static capacitance of the die should be measured and reference voltages adjusted accordingly.

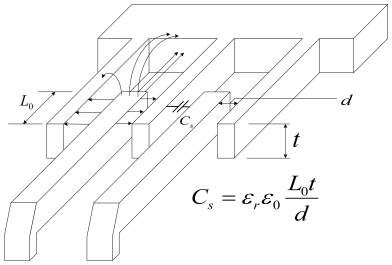


Figure 4.16: Interdigitated structure of the x-direction accelerometer.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Maximum Acceleration	a_{max}				g
Mass weight	m				μg
Spring Constant	k				N/m
Mechanical Resonance	f_n				kHz
Damping Coefficient	D				1
Displacement at rest	d				nm
Deflection for 1g	x_g				nm
Deflection for 30g	x_n				nm
Normalized Deflection	x_n/d				1
Resting Capacitance[a]	$C_{0,x}$				fF
Capacitive sensitivity [b]			4.5		fF/g
Sensor parasitic capacitance	C_{PS1_x}				fF
Relative Change in Capacitance[b,c]	E_{c_x}				1
Offset of X-element	$\lvert C_{\text{off}_x} \rvert$			$0.5 \cdot E_c \cdot C_0$	fF
Linearity error	F_L				%

[a] Excluding parasitic capacitance, measured at zero acceleration

[b] Differential difference in capacitance due to 1g acceleration $\frac{C_s^+ - C_s^-}{a}$

[c] Considering parasitic capacitance at maximum 30g, $E_c = \frac{(C_{s2}+C_{ps2})-(C_{s1}+C_{ps1})}{(C_{s2}+C_{ps2})-(C_{s1}+C_{ps1})}$.

Table 4.1: Specifications for the x-direction capacitive accelerometer. Structure is based on an interdigitated structure.

4.3.6 X-Direction DC Testing

The resting capacitance can be found by observing the feedback of the system. This measurement is demonstrated for the x-direction and subsequently reported for the y and z directions. By knowing the resting capacitance, we can estimate the sensitivity of the accelerometer according to the data in Table 4.1 and subsequently adjust reference voltages according to Eq. (4.47).

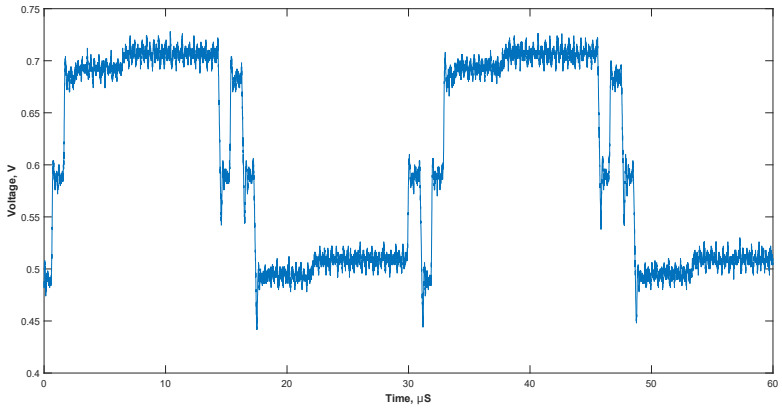


Figure 4.17: DAC output as observed through an on-chip buffer.

Based on the graph, the high and low point of feedback is approximately $\pm$**90** mV with respect to the common mode voltage of 600 mV. Accordingly we can write

$$\begin{aligned} C_s &\approx \frac{Vout_{DAC} - V_{ref_2,CM}}{V^+_{ref_2} - V_{ref_2,CM}} C_{f2} \\ &\approx \frac{90}{200} \times 832 \text{ fF} \\ &\approx 375 \text{ fF} \ . \end{aligned} \tag{4.49}$$

This is within the higher range of values found in Table 4.1 and indicates a sensitivity closer to 5.5 fF/g. Therefore, the reference voltages

to optimize the output for 4 g acceleration is given by

$$V_{ref_1^{\pm}} = \frac{375fF}{4g \times 5.5fF/g} \cdot \pm 25 \text{ mV} \tag{4.50}$$
$$= \pm 426 \text{ mV} .$$

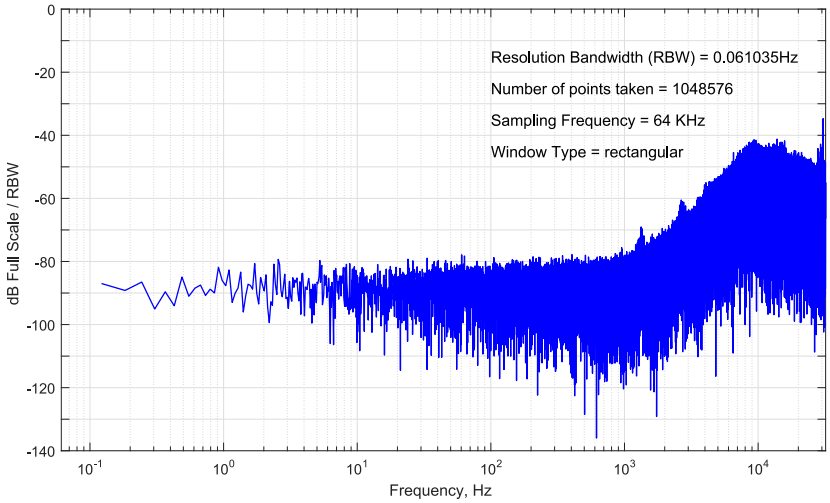


Figure 4.18: Measured x-direction DC output spectrum. Reference voltages are $V^{+}_{ref1} = 1026$ mV, $V^{-}_{ref1} = 174$ mV, $V^{+}_{ref2} = 625$ mV, $V^{-}_{ref2} = 575$ mV

The DC output spectrum based on $V_{ref1^{\pm}} = \pm 426$ mV is shown in Fig. 4.18. From this, the noise floor of the accelerometer readout in the x-direction can be calculated as

$$\text{Noise Floor Measured} = \frac{\text{FFT Noise Floor Power} \times \text{Full Scale Power}}{\text{Resolution Bandwidth}}$$
$$= \left(10^{\frac{-90}{10}}\right)\left(\frac{0.426}{\sqrt{2}}\right)^2 V^2 \left(\frac{2^{20}}{64 \text{ KHz}}\right) \tag{4.51}$$
$$= 1.4867 \times 10^{-9} \text{ V}^2/\text{Hz}$$
$$NF_x = 38.56 \ \mu\text{V}/\sqrt{\text{Hz}} \text{ ..}$$

The above is the noise floor at the *output* of the modulator. But based on our linear model of the delta-sigma modulator, this output is simply the input at the first integrator[10]. Therefore, we can say that our *capacitive resolution* or the minimum detectable change in capacitance is the capacitance value that results in the above noise floor at the output

[10] The signal transfer function was simply a delay

of the charge to voltage amplifier or the input to the first integrator. Using the charge to voltage amplifier transfer function, we can solve for the capacitive resolution as

$$V_{out} = \frac{\Delta C}{C_{f1}} V_{ref_1} \tag{4.52}$$

$$\begin{aligned} \Delta C_{min,x} &= \frac{V_{out,min}}{V_{ref_1}} C_{f1} \\ &= 72.41 \text{ aF}/\sqrt{\text{Hz}} \ . \end{aligned} \tag{4.53}$$

Equivalently, we can convert the capacitive resolution into an equivalent minimum detectable acceleration. Given that the sensitivity for this accelerometer is 5.5 fF/g, then this equates to

$$\Delta C = G \times S \tag{4.54}$$

$$\begin{aligned} G_{min,x} &= \frac{\Delta C_{min,x}}{S} \\ &= \frac{75.3 \text{ aF}/\sqrt{\text{Hz}}}{5.5 \text{ fF/g}} \\ &= 13.7 \text{ mg}/\sqrt{\text{Hz}} \ . \end{aligned} \tag{4.55}$$

Note that $G_{min,x}$, $\Delta C_{min,x}$ and NF_x are all equivalent in the above derivations and can be used interchangeably.

Comparison to Theory and Simulations

The theoretical noise floor can be calculated based on the orthogonal combination of the mechanical noise floor and the electronic noise floor. The electronic noise is dominated by the capacitance to voltage converter, the DAC feedback stage and the first integrator[11]. Accordingly, we can write

$$NF_{x,t} = \sqrt{\frac{4k_B T \omega_n}{m^2 Q} + \frac{\overline{V^2}_{conv} + \overline{V^2}_{DAC} + \overline{V^2}_{int}}{OSR}} \ . \tag{4.56}$$

[11] More details on formulas for the noise sources is provided in Appendix A.1.4 and details are omitted here for brevity

Here k_B is Boltzmann's constant, ω_n is the natural resonant frequency of the accelerometer, m is the mass in Kg and Q is the quality factor of the complex poles governing the second order mechanical accelerometer. For the accelerometer used for testing, the small mass makes the mechanical noise much larger than the electronic noise, as such we can write

$$NF_{x,t} \approx \sqrt{\frac{4k_BTb}{9.8^2m^2}} \left(\frac{5.5 \text{ fF/g}}{800 \text{ fF}} 0.426\right)^2 \tag{4.57}$$
$$\approx 26.90 \ \mu\text{V}/\sqrt{\text{Hz}} \ .$$

Therefore the theoretical results match the output fairly well. A simulation of the system with an accelerometer model[12] is shown in Fig. 4.19 using transient noise simulation. The frequency range for the transient noise is 2.048 Hz to 100 MHz which captures the low frequency noise and up to $5-10$ times the 3 dB bandwidth of the front-end op-amps.

[12] for details of accelerometer modeling see Appendix D.

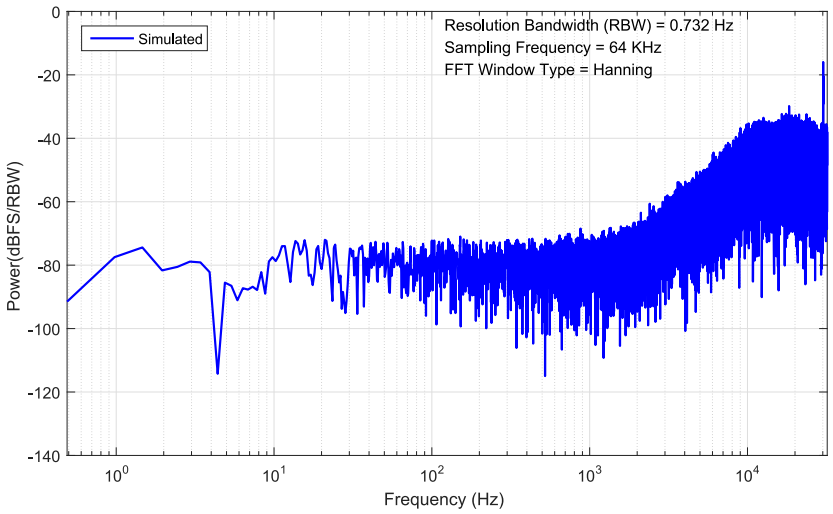


Figure 4.19: Simulated x-direction DC output spectrum. Reference voltages same as measurements.

The noise floor of this simulation is calculated as:

$$\begin{aligned}\text{Noise Floor Simulated} &= \frac{\text{FFT Noise Floor Power} \times \text{Full Scale Power}}{\text{Resolution Bandwidth}} \\ &= \left(10^{\frac{-81}{10}}\right)\left(\frac{0.426}{\sqrt{2}}\right)^2 \text{V}^2 \left(\frac{2^{17}}{64 \text{ KHz}}\right) \qquad (4.58) \\ &= 1.4761 \times 10^{-9} \text{ V}^2/\text{Hz} \\ NF_{x,s} &= 38.42 \ \mu\text{V}/\sqrt{\text{Hz}} \ ,\end{aligned}$$

and the minimum detectable capacitance is given by

$$\Delta C_{min,xs} = 72.15 \text{ aF}/\sqrt{\text{Hz}} \ .$$

This matches within a few percentage error to the measured and theoretical values indicating that our model of the accelerometer is very accurate. The larger error in the standalone modulator testing does not translate here because the mechanical noise of the accelerometer is dominating.

4.3.7 X-Direction AC Testing

To generate a pure sinusoidal excitation signal for the accelerometer, a step motor is used in a master slave configuration to produce a sinusoidal distance movement. Since acceleration is the integral of velocity, which in turn is the integral of displacement, as long as we have a sinusoidal displacement, then sinusoidal acceleration should follow. The output spectrum for an acceleration force of ±0.15 g at 3.90625 Hz input[13] is shown in Fig. 4.20. The SNDR for this test is 28.4 dB with a bandwidth of 62.5 Hz. This bandwidth is used for all accelerometer AC tests. Assuming a full scale value of 2.5 g, we expect the SNDR to increase to 52.8 dB.

[13] Frequency is chosen to fall within a bin and avoid skirts [76]

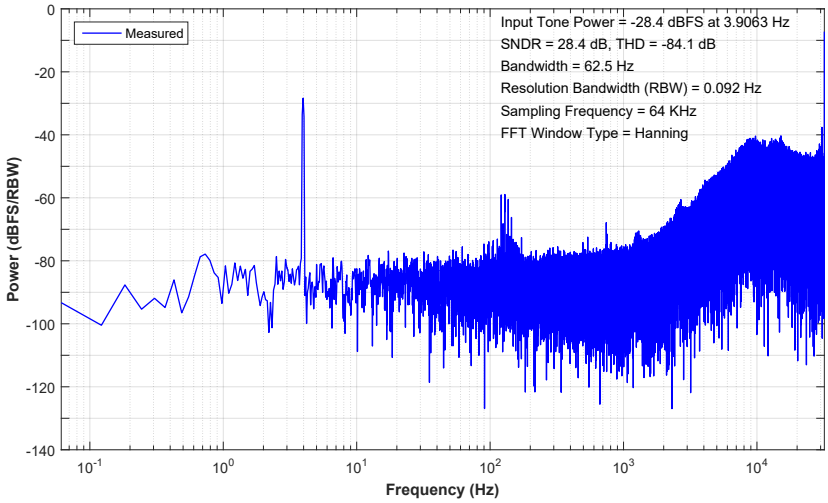


Figure 4.20: Measured x-direction AC output spectrum at 3.90625 Hz with magnitude of ±0.15 g. Reference voltages are $V^{+}_{ref1} = 1026$ mV, $V^{-}_{ref1} = 174$ mV, $V^{+}_{ref2} = 625$ mV, $V^{-}_{ref2} = 575$ mV

A simulation of the system[14] is shown in Fig. 4.21.

[14] using transient noise simulation

The 1.2 dB higher SNDR from simulations is not significant. It can be attributed to the low number of points taken for the transient noise simulation relative to the measured results. Also, device parameters can vary significantly and we have only estimated these values based on the output of the feedback DAC as shown in Fig. 4.17.

Notice that in the measurements, there is significant environmental noise around and above 100 Hz. These tones are unwanted but do not pose a problem as harmonics of our fundamental fall at 7.8125 Hz, 15.625 Hz and 31.25 Hz, well below the high frequency environmental noise[15]. From the analysis of the harmonics as shown in the previous section,

[15] To confirm that these spurs are not due to the input signal, cross sensitivity testing has been performed and results are shown in Appendix C.1.

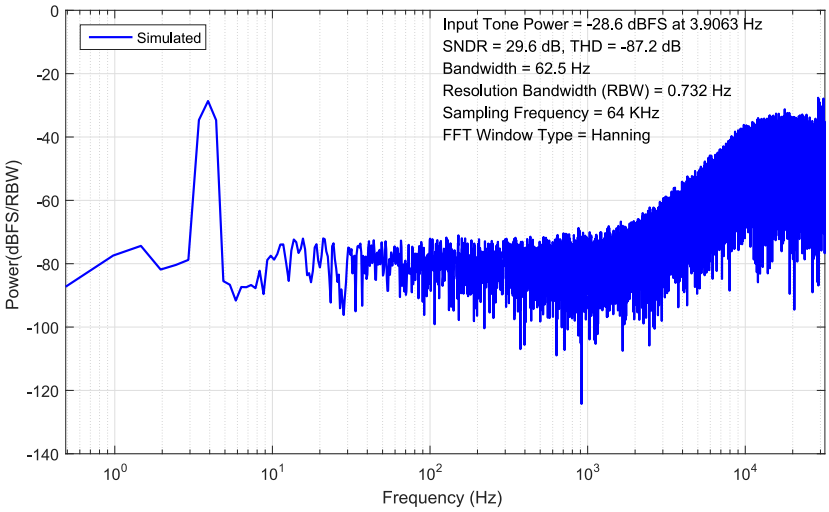


Figure 4.21: Simulated x-direction AC output spectrum simulation at 3.90625 Hz with magnitude of ±0.15 g.

we expect the second harmonic to be reduced significantly and a 3rd harmonic to fall around −80 dBFs. Since this is very close to the noise floor, we cannot conclusively prove that the system can reduce harmonics from the test at this frequency.

To better observe the third harmonic, the acceleration frequency is doubled to 7.8125 Hz. This higher frequency then corresponds to a force of ±0.6 g or an increase by a factor of 4. The output spectrum is shown in Fig. 4.22 and highlighted with the fact that we expect a 3rd harmonic at 23.4375 Hz at −68 dBFs. The charge balanced architecture has reduced the harmonic to below the noise floor. The SNDR for this test is 45.5 dB. Assuming that the acceleration can be increased to the full scale range of 2.5 g, the SNDR should improve to 53.0 dB.

For comparison, a simulation of the system is shown in Fig. 4.23 using a transient noise simulation. There is a 1 dB discrepancy between the measured and simulation results that can be attributed to errors in FFT as well precise dynamic models of the accelerometer under test.

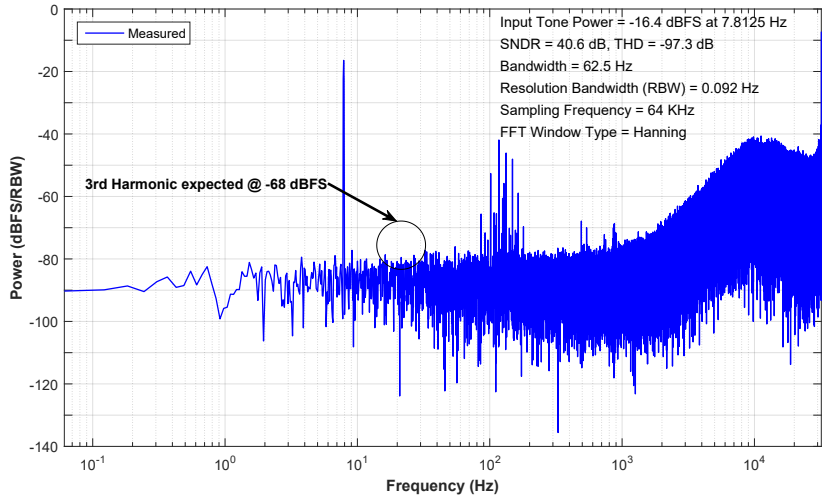


Figure 4.22: Measured x-direction AC output spectrum with acceleration at 7.8125 Hz with magnitude of ±0.6 g. Reference voltages are $V^{+}_{ref1} = 1026$ mV, $V^{-}_{ref1} = 174$ mV, $V^{+}_{ref2} = 625$ mV, $V^{-}_{ref2} = 575$ mV.

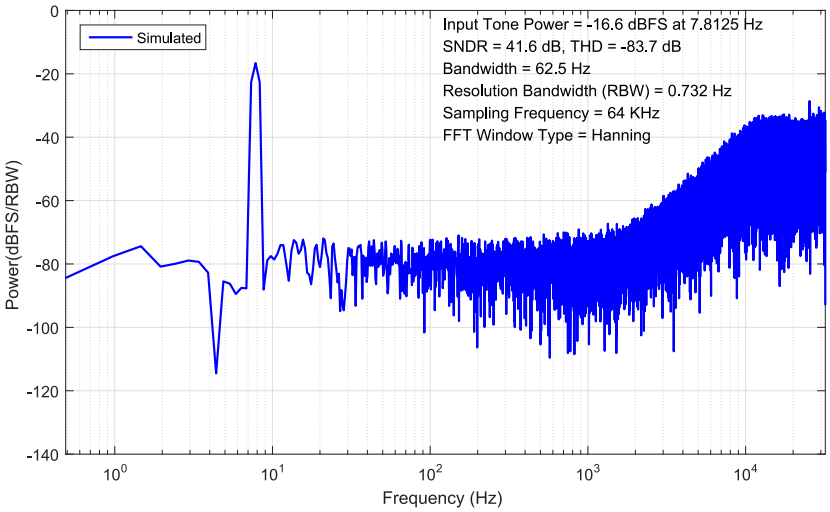


Figure 4.23: Simulated x-direction AC output spectrum at 7.8125 Hz with magnitude of ±0.6 g. voltages are the same as used in the measurement of Fig. 4.22.

4.3.8 Y Direction Testing

4.3.9 Y-Direction Specifications

The y-direction parameters are similar to the x-direction parameters with slight differences in parasitic capacitance, and sensitivities. Full parameters are shown in Table 4.2.

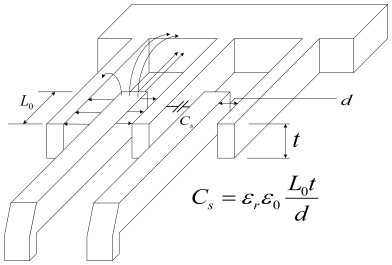


Figure 4.24: Interdigitated structure of the y-direction accelerometer.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Maximum Acceleration	a_{max}				g
Mass weight	m				μg
Spring Constant	k				N/m
Mechanical Resonance	f_n				kHz
Damping Coefficient	D				1
Displacement at rest	d				nm
Deflection for 1g	x_g				nm
Deflection for 30g	x_n				nm
Normalized Deflection	x_n/d				1
Resting Capacitance[a]	$C_{0,y}$				fF
Capacitive sensitivity [b]			4.5		fF/g
Sensor parasitic capacitance	C_{PS1_y}				fF
Relative Change in Capacitance[b,c]	E_{c_y}				1
Offset of X-element	$\lvert C_{\text{off}_y} \rvert$			$0.5 \cdot E_c \cdot C_0$	fF
Linearity error	F_L				%

[a] Excluding parasitic capacitance, measured at zero acceleration

[b] Differential difference in capacitance due to 1g acceleration $\frac{C_s^+ - C_s^-}{a}$

[c] Considering parasitic capacitance at maximum 30g, $E_c = \frac{(C_{s2}+C_{ps2})-(C_{s1}+C_{ps1})}{(C_{s2}+C_{ps2})-(C_{s1}+C_{ps1})}$.

Table 4.2: Specifications for the y-direction capacitive accelerometer. Structure is based on an interdigitated structure as shown in Fig. 4.24.

4.3.10 Y-Direction DC Testing

The rest capacitance for the y-direction, C_{s_y}, was measured to be 330 fF resulting in a reference voltage of ±430 mV to accommodate a full scale range of ±4 g. The spectrum of the output is shown in Fig. 4.25. The noise floor and minimum detectable capacitance are then given by

$$\begin{aligned} NF_y &= \left(10^{\frac{-90}{10}}\right)\left(\frac{0.430}{\sqrt{2}}\right)^2 \mathrm{V}^2 \left(\frac{2^{20}}{64\ \mathrm{KHz}}\right) \\ &= 1.5147 \times 10^{-9}\ \mathrm{V}^2/\mathrm{Hz} \\ &= 38.92\ \mu\mathrm{V}/\sqrt{\mathrm{Hz}} \Rightarrow \Delta C_{min,y} = 72.41\ \mathrm{aF}/\sqrt{\mathrm{Hz}}\ . \end{aligned} \tag{4.59}$$

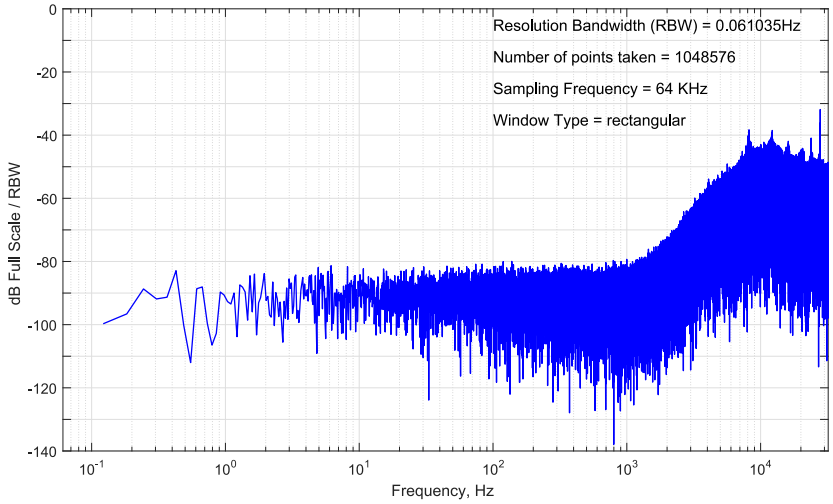


Figure 4.25: Measured y-direction DC output spectrum. Reference voltages are $V^+_{ref1} = 1030$ mV, $V^-_{ref1} = 170$ mV, $V^+_{ref2} = 625$ mV, $V^-_{ref2} = 575$ mV

A simulation of the system is shown in Fig. 4.26 with good matching to measurements as shown below.

$$\begin{aligned} NF_{y,s} &= \left(10^{\frac{-81}{10}}\right)\left(\frac{0.43}{\sqrt{2}}\right)^2 V^2 \left(\frac{2^{17}}{64\ \mathrm{KHz}}\right) \\ &= 37.88\ \mu V/\sqrt{Hz} \\ \Delta C_{min,ys} &= 70.47\ aF/\sqrt{Hz} \end{aligned} \tag{4.60}$$

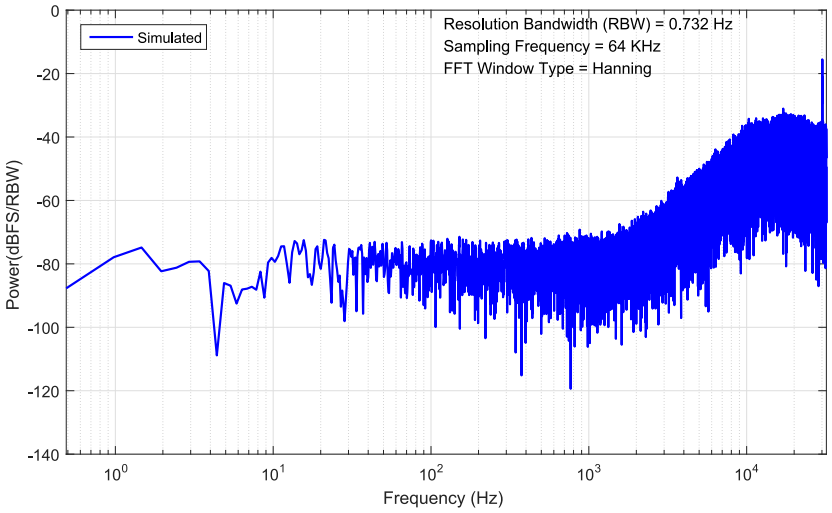


Figure 4.26: Simulated y-direction DC output spectrum. Reference voltages are the same as used in the measurement of Fig. 4.25.

4.3.11 Y-Direction AC Testing

As with the x-direction testing, we perform two tests for the y-direction. One test is with an acceleration force of $\approx \pm 0.15$ g at a frequency of 3.90625 Hz. This is shown in Fig. 4.27 resulting in an SNDR of 30.2 dB and a maximum possible SNDR of 54.6 dB. The second test increases the frequency to 7.8125 Hz at an acceleration of ± 0.6 g (Fig. 4.29) showing again the reduction in harmonics below the noise floor. The SNDR is measured to be 42.5 dB with a maximum possible SNDR of 54.9 dB at full scale. The corresponding simulations with frequency of 3.90625 Hz and 7.8125 Hz are shown in Fig. 4.28 and Fig. 4.30 respectively, matching the measurement results within less than 1 dB. Note that the number of points used for the simulations is lower due to the long simulation times required to accurately model transient noise.

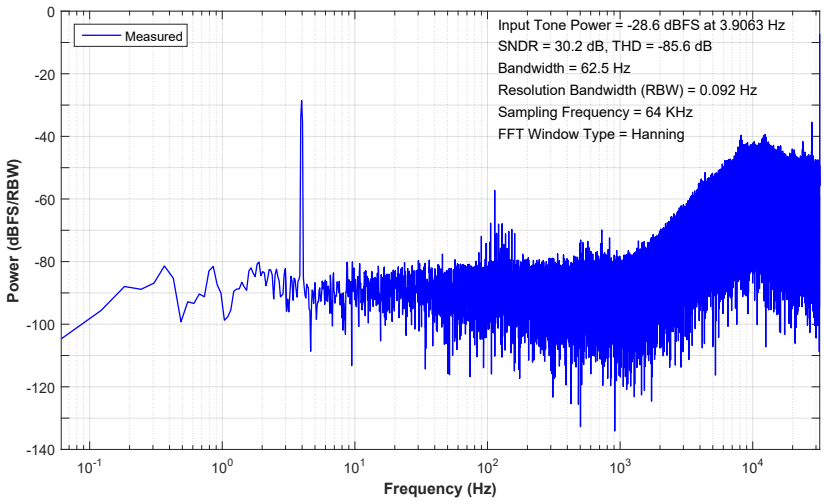


Figure 4.27: Measured y-direction AC output spectrum with acceleration at 3.90625 Hz with magnitude of ± 0.15 g. Reference voltages are $V^+_{ref1} = 1030$ mV, $V^-_{ref1} = 170$ mV, $V^+_{ref2} = 625$ mV, $V^-_{ref2} = 575$ mV

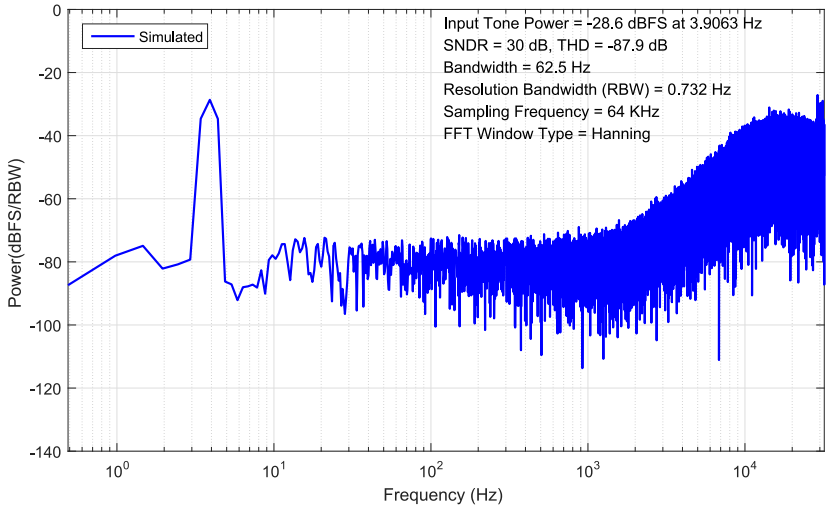


Figure 4.28: Simulated y-direction AC output spectrum with acceleration at 3.90625 Hz with magnitude of ±0.15 g. Reference voltages are $V_{ref1}^{+} = 1030$ mV, $V_{ref1}^{-} = 170$ mV, $V_{ref2}^{+} = 625$ mV, $V_{ref2}^{-} = 575$ mV

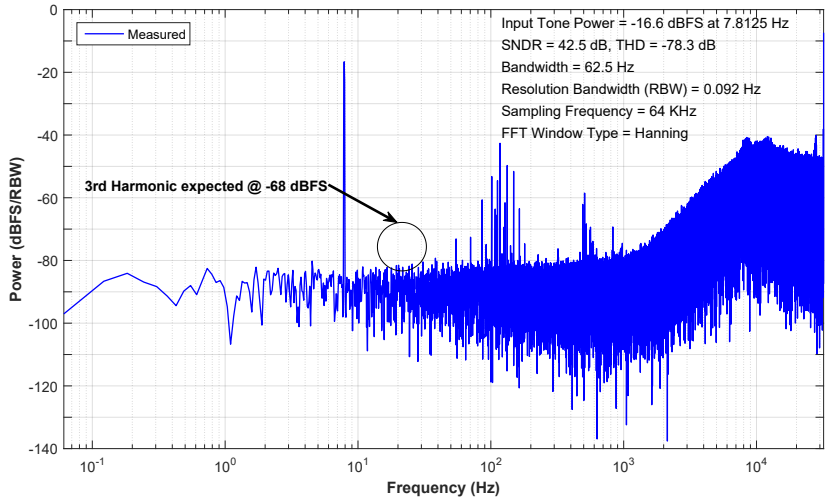


Figure 4.29: Measured y-direction AC output spectrum with acceleration at 7.8125 Hz with magnitude of ±0.6 g. Reference voltages are $V_{ref1}^{+} = 1030$ mV, $V_{ref1}^{-} = 170$ mV, $V_{ref2}^{+} = 625$ mV, $V_{ref2}^{-} = 575$ mV

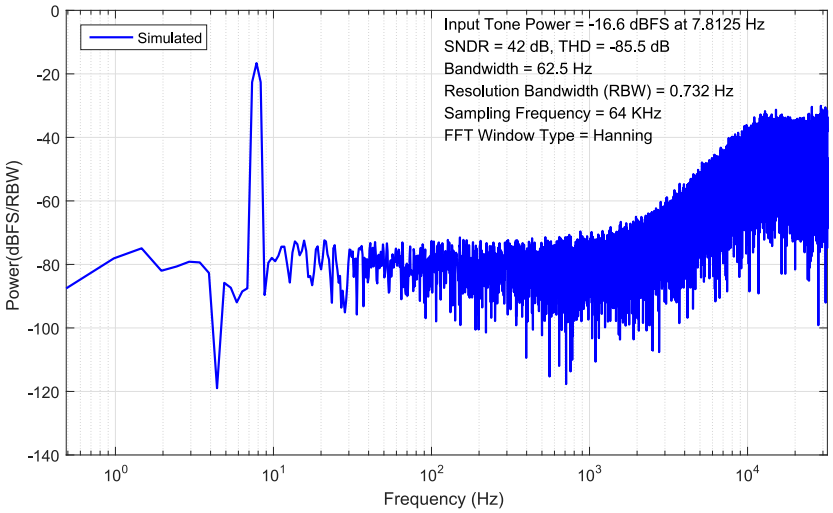


Figure 4.30: Simulated y-direction AC output spectrum with acceleration at 7.8125 Hz with magnitude of ±0.6 g. Reference voltages are $V_{ref1}^{+} = 1030$ mV, $V_{ref1}^{-} = 170$ mV, $V_{ref2}^{+} = 625$ mV, $V_{ref2}^{-} = 575$ mV

4.3.12 Z-Direction Testing

4.3.13 Z Direction Specifications

The z-direction accelerometer uses a cantilever structure and as such the sensitivity and bandwidth are lower in this direction. Full specifications are shown in Table 4.3.

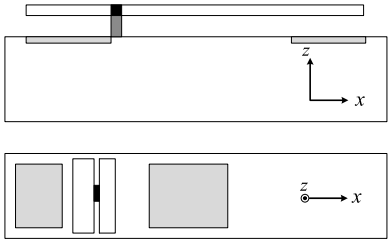


Figure 4.31: Physical structure of the z-direction accelerometer.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Maximum Acceleration	a_{max}				g
Mass weight	m				μg
Tortion Constant	k_t				μNm/rad
Mechanical Resonance	f_n				kHz
Damping Coefficient	D				1
Rotation for 1g	α_g				mrad
Rotation for 30g	α_n				mrad
Resting Capacitance[a]	$C_{0,y}$				fF
Capacitive sensitivity [b]			4.5		fF/g
Sensor parasitic capacitance	$C_{PS1,2_z}$				fF
Relative Change in Capacitance[b,c]	E_{c_z}				1
Offset	$\lvert C_{\text{off}_z}\rvert$			$0.5 \cdot E_c \cdot C_0$	fF
Linearity error	F_L				%

[a] Excluding parasitic capacitance, measured at zero acceleration

[b] Differential difference in capacitance due to 1g acceleration $\frac{C_s^+ - C_s^-}{a}$

[c] Considering parasitic capacitance at maximum 30g, $E_c = \frac{(C_{s2}+C_{ps2})-(C_{s1}+C_{ps1})}{(C_{s2}+C_{ps2})-(C_{s1}+C_{ps1})}$.

Table 4.3: Specifications for the z-direction capacitive accelerometer. Structure is that of a parallel plate (see Fig. 4.31)

4.3.14 Z-Direction DC Testing

The input-referred DAC output for the z-direction tested was ±350 mV and from the spectrum of Fig. 4.32, the estimated noise floor and minimum detectable capacitance are given by

$$\begin{aligned} NF_z &= \left(10^{\frac{-89}{10}}\right)\left(\frac{0.350}{\sqrt{2}}\right)^2 V^2 \left(\frac{2^{20}}{64\text{ KHz}}\right) \qquad (4.61)\\ &= 35.54\ \mu\text{V}/\sqrt{\text{Hz}}\ , \\ \Delta C_{min,z} &= 81.23\ \text{aF}/\sqrt{\text{Hz}}\ . \end{aligned}$$

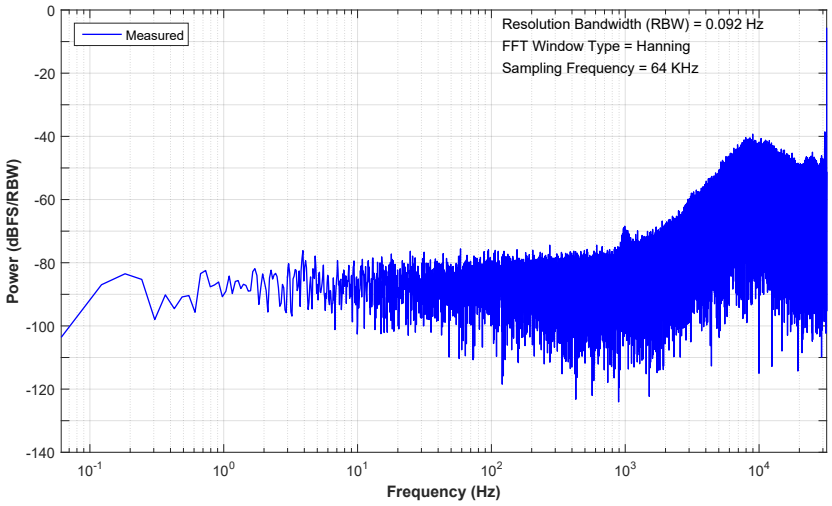


Figure 4.32: Measured z-direction DC output spectrum. Reference voltages are $V^+_{ref1} = 950$ mV, $V^-_{ref1} = 250$ mV, $V^+_{ref2} = 625$ mV, $V^-_{ref2} = 575$ mV

A simulation of the system is shown in Fig. 4.26 with good matching to measurements as shown below.

$$\begin{aligned} NF_{z,s} &= \left(10^{\frac{-81}{10}}\right)\left(\frac{0.35}{\sqrt{2}}\right)^2 V^2 \left(\frac{2^{17}}{64\text{ KHz}}\right) \qquad (4.62)\\ &= 31.56\ \mu V/\sqrt{Hz} \\ \Delta C_{min,zs} &= 72.13\ aF/\sqrt{Hz} \end{aligned}$$

4.3.15 Z-Direction AC Testing

Due to the limitations of the test equipment, it was not possible to accurately perform a frequency test in the z-direction.

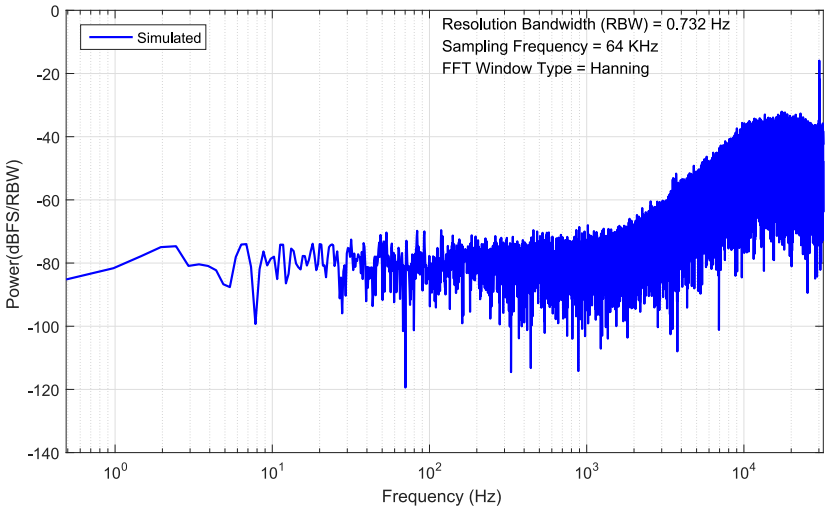


Figure 4.33: Simulated z-direction DC output spectrum. Reference voltages are $V_{ref1}^{+} = 950$ mV, $V_{ref1}^{-} = 250$ mV, $V_{ref2}^{+} = 625$ mV, $V_{ref2}^{-} = 575$ mV

4.4 Summary of Measurement Results

Process	IBM 0.13 μm technology with MIM capacitors			
Supply Voltage	1.2 V			
Configuration	Switched capacitor based Delta Sigma Modulator			
Active Area	0.35 mm^2 [a]			
	Delta Sigma Test			
Sampling frequency	64 KHz			
Bandwidth	62.5 Hz			
Total Power consumption	630 μW			
Peak SNDR	62.9 dB			
FOM Delta Sigma[b]	4.42 nJ/step			
	Accelerometer Testing			
	x-axis	y-axis	z-axis	Units
Noise Floor	38.56	38.92	31.68	μ V/$\sqrt{\text{Hz}}$
SNDR[c]	53.0	54.9	–	dB
Capacitive Resolution	72.41	72.41	81.23	aF/$\sqrt{\text{Hz}}$
Harmonic Reduction	> 12	> 12	–	dB
x-axis Cross Sensitivity[d]	–	> 60	> 60	dB
y-axis Cross Sensitivity[d]	> 60	–	> 60	dB
z-axis Cross Sensitivity[d]	> 60	> 60	–	dB

[a] Excludes area for pads.
[b] FOM= $\frac{\text{Power}}{2\times \text{BW} 2^{\text{ENOB}}}$
[c] At 7.8125 Hz assuming proper equipment to achieve $\pm$2.5 g of acceleration. Current tests with step motor resulted in $\pm$0.6 g maximum acceleration.
[d] See Appendix C.1

Table 4.4: Summary of Results

4.5 *Comparison to the State of the Art*

The measurements in the previous section confirm that the proposed architecture is functional and has the ability to overcome problems associated with low sensitivity devices. This property is key and the distinguishing factor of the proposed architecture. Raw fidelity parameters such as SNDR and capacitive resolution only provide half of the picture as discussed in the opening chapter. To clarify this further, Fig. 4.34 shows the SNR tradeoff for three types of ratiometric charge balanced readout circuits: the analog feedback circuit as first introduced in [69], the digital feedback circuit used in [28] and the proposed architecture [24].

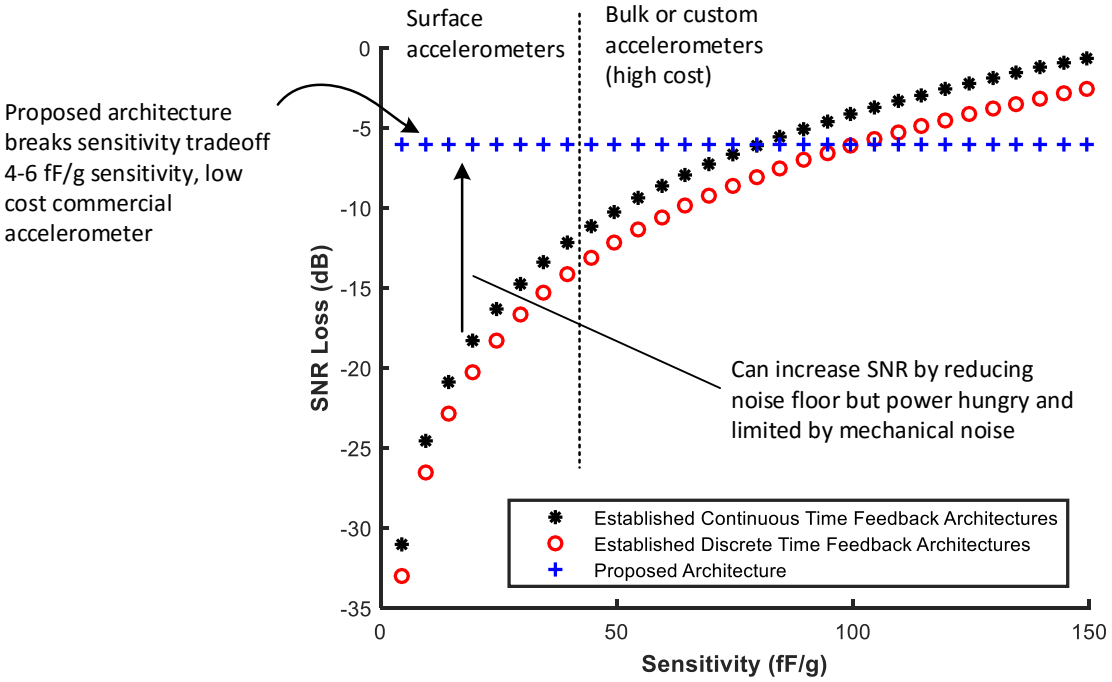


Figure 4.34: Comparison of the SNR loss with respect to device sensitivity for the two types of charge balanced open loop ratiometric readout circuits and the proposed system.

This plot emphasizes the tradeoff between device sensitivity and SNR loss due to the structure of the readout circuit. As the sensitivity of devices is reduced, all other things being equal, the fidelity decreases for traditional charge balanced ratiometric readout circuits. Accelerometers

that go beyond a few 10's of fF/g are either bulk-micromachined or custom made. Therefore, readouts based on high sensitivity accelerometers would then suffer if replaced with a low sensitivity accelerometer. These challenges are rarely acknowledged in research based papers.

It is of course possible for lower sensitivity devices to still achieve high fidelity but this comes at the cost of higher power consumption. For example, publication in [27] and [29] are targeted for low sensitivity devices of 1.6 and 1.2 fF/g. However power consumption for these systems is 5.2 mW and 10 mW respectively and of limited use for practical applications[16].

[16] and as discussed previously, these systems are custom dual differential structures.

In conclusion, work in the area of low power high fidelity interface circuits bypasses the low signal problem inherent to charge balance operation by choosing high sensitivity custom accelerometers whose sensitivity is a large fraction of the static capacitance. This allows for the SNR loss as shown Fig. 4.34 to be small and not adversely affect the specifications of these circuits. The proposed architecture, by having several gain factor knobs, can accommodate a wide range of device sensitivities without sacrificing output fidelity.

5

Conclusion and Future Work

This thesis provided a theoretical development of capacitive accelerometer readout circuits and detailed the problem encountered when incorporating capacitive accelerometers in feedback systems. Feedback systems rely on an appropriately sized feedback signal within the range of the input signal. Large differences in feedback and input signals can significantly reduce signal fidelity. This concept is rarely a design constraint in other applications but manifests itself in accelerometer signal processing. As discussed, for best fidelity, a ratiometric approach is needed for accelerometer readouts. In this case, the input signal is the difference in sense capacitance while the feedback signal is proportional to the sense capacitance causing a significant mismatch in feedback and feedforward signals that cannot readily be resolved with current architectures.

An architecture that decouples the feedback and feedforward gains was designed and implemented through a delta sigma modulator. The simulations and measurements confirm that the accelerometer system proposed is robust and reduces harmonic outputs below the noise floor without the need for look-up tables or other complex techniques.

The main contributions of the thesis can thus be summarized as follows:

- A direct digital architecture that is ratiometric and charge balanced and allows for flexibility in adjusting the gain of the feedback signal relative to the input signal. Variants of this technique are now employed by other researchers [77] [78].
- A technique for differential readout making use of half-bridge interfac-

ing and adaptation to pseudo differential output through chopping. The technique has been adopted recently and analyzed in [79].

- A simplified testing procedure for accelerometers through the use of a step motor and master-slave programming.

Having proven the concept of the system, several improvements can be made to this architecture for future designs. These include:

1. **Multibit DAC**

   Although the structure of the proposed system does not allow for multi-bit DACs due to linearity issues, a 1.5 bit DAC is possible. In this case, the high and low outputs function as before, but there is a midband range where we do not do anything. This three level DAC would still be inherently linear but the extra half bit lowers quantization noise at the same power consumption.

2. **Automatic Gain Control**

   The flexibility discussed in this system has been performed manually by adjusting capacitor values and reference voltages. An extension of this work is to build a full ADC (DSM and decimation filter) and use the output to automatically adjust the gain of the circuit for maximum fidelity.

3. **Common Mode Voltage Testing**

   In Section 3.5.4, we discussed that since the output of the charge-to-voltage converter is proportional to the input reference voltage, then a higher reference voltage would result in better signal fidelity. This higher signal voltage, however, has to be accompanied by a higher common mode voltage for the front-end accelerometer. These tests were hard to perform due to the limited acceleration force and equipment at hand. Future work in this area would require use of more advanced equipment (higher g forces) to confirm the simulations in this area.

4. **Accelerometer Modeling and Testing**

   In all our simulations, we have assumed a basic model of the accelerometer and then added non-linearities. These non-linearities

generally involve using nonlinear models of damping factor and spring constant. The proposed system had a MUX and a buffer placed at the output of the charge-to-voltage converter that can be used to characterize the accelerometer and test the validity of models used in simulations.

A

Circuit Level Designs

A.1 Op-Amp Design

Op-amp design is influenced by many factors[1]. This includes the proper transistor sizing, gain and bandwidth requirements, and topology choice. These factors are all considered in this section.

[1] Strictly speaking, the correct term to use is OTA or operational transconductance amplifier as we will not be making use of an output buffer

A.1.1 Transistor Sizing

The first major design choice in op-amp design is making use of correct transistor sizes. There are two parameters that influence transistor sizing in analog design: the intrinsic gain and intrinsic speed. The intrinsic gain of a MOSFET is the maximum gain of a single transistor using a simulation (and test) setup as shown in Fig. A.1.

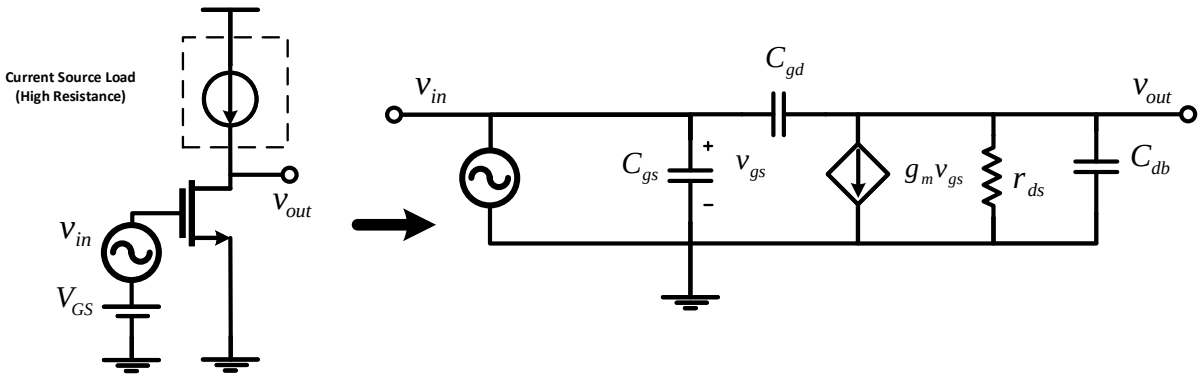


Figure A.1: Test setup for determining the intrinsic gain of a transistor.

Using the above figure, the maximum gain at low frequencies is given

by

$$A_v = g_m r_{ds} \tag{A.1}$$
$$= \frac{2I_D}{V_{eff}} \frac{1}{\lambda I_D} \tag{A.2}$$
$$= \frac{2}{\lambda V_{eff}} , \tag{A.3}$$

where V_{eff} is the effective or overdrive voltage and λ is a technology dependent factor that is weakly inversely proportional to length L. Therefore, to a first order, the gain of a transistor is independent of the current and inversely proportional to the effective or overdrive voltage and proportional to the length L. We can increase overdrive voltage by either increasing the size ratio of the transistor or decreasing the current I_D.

Given the above, we would also like to have a metric that measures the speed of a single transistor. The metric is simulated by the circuit shown in Fig. A.2. It is the frequency at which the transistor has unity current gain.

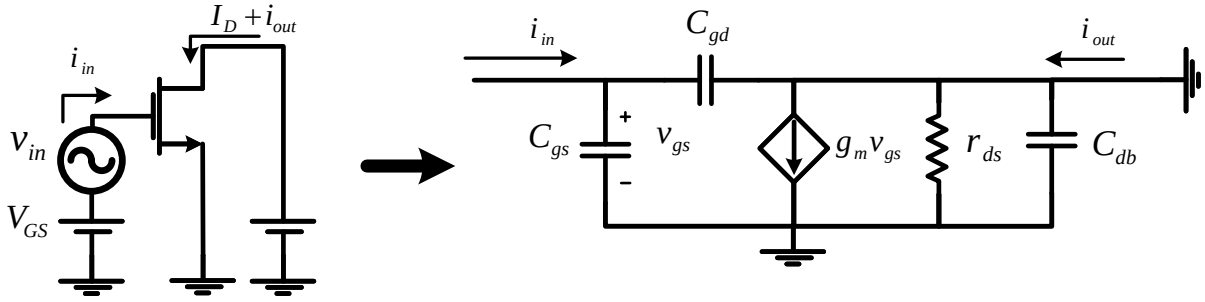


Figure A.2: Test setup for determining the intrinsic speed of a transistor.

From Fig. A.2, if the magnitude of the AC current goes up with frequency, the output impedance reduces by $1/j\omega C$ and we need more current to charge and discharge the capacitor. Eventually, at some point, as we sweep the frequency, the input and output current are equal and then we are putting as much AC current into the transistor as we are getting out[2]. We can, therefore, use this frequency as a proxy for what is the fastest speed for which the MOSFET does something useful. It

[2] At which point we may ask what is the point of having a transistor?

can be shown that this frequency is approximately equal to

$$f_t \approx \frac{g_m}{2\pi(C_{gs}+C_{gd})} \ , \tag{A.4}$$

where C_{gs} is the gate source capacitance and C_{gd} is the gate drain capacitance of the MOSFET. Using a formula for g_m in terms of transistor size and effective voltage, we have

$$\begin{aligned} f_t &\approx \frac{\mu_n C_{ox}(W/L)V_{eff}}{2\pi C_{ox}W(2/3)L} \\ &\approx \frac{3\mu_n V_{eff}}{4\pi L^2} \ . \end{aligned} \tag{A.5}$$

According to Eq. (A.5), speed is inversely proportional to length L and proportional to V_{eff} which confirms our original intuition. Therefore, to increase intrinsic speed you either increase L or increase V_{eff}. You can increase V_{eff} by either driving more current into the transistor or reducing W[3]

[3] There is a limit to this of course. At some point, with large enough V_{eff} (and subsequently V_{ds} to stay in the active region), we get to mobility degradation and then g_m becomes a constant.

Therefore, the intrinsic gain expression is telling us that we get maximum gain at low V_{eff} and low λ. The intrinsic speed equation tells us to increase V_{eff}. Clearly, there is an optimal width that would maximize the product of the intrinsic gain and intrinsic speed and this is often used as a metric to choose an optimal size for transistors.

Intrinsic speed, however, as defined above is dependent on parasitic capacitances only and there are many circuits that are not limited by parasitic capacitances. In most switched capacitor circuits, for example, the load that we are driving is generally large [4]. In these applications, changing the size of the transistor is not going to make a big difference to the speed. In other words, the savings that we get by reducing the parasitic capacitances of transistors would be trivial compared to the load that we have to drive.

[4] Determined, among other things, by noise requirements

As such, for the transistor sizing for the proposed application, only the intrinsic gain parameter will be used. To do this, we plot a graph of the transconductance per unit of current or g_m/I_D versus a size ratio W/L while sweeping the effective voltage. This is shown for an NMOS in Fig. A.3 with $W = 3$ μm and $L = 600$ nm.

From Fig. A.3, we can see that for $V_{eff} = 165$ mV, the maximum transconductance per unit of current is achieved. Increasing the size of

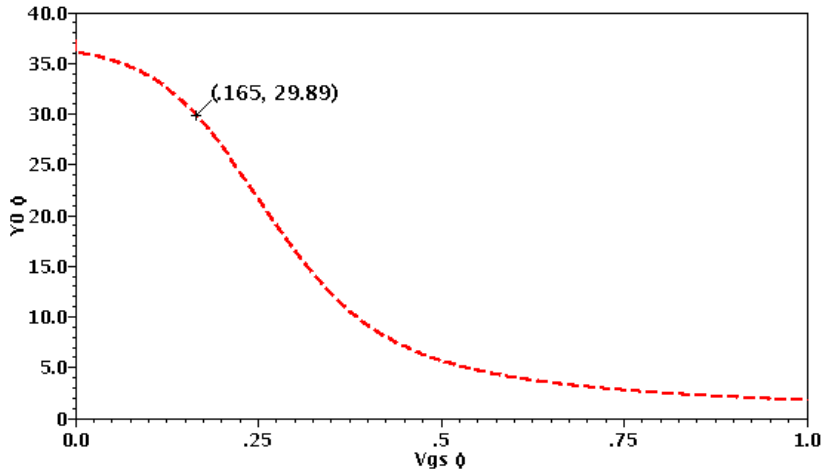


Figure A.3: Transconductance per unit of current versus effective voltage for an NMOS. Sizing for the transistor is $W = 3$ μm and $L = 600$ nm.

the transistor beyond this has diminishing returns. For completeness, the PMOS transistor sizing is shown in Fig. A.4 showing a $V_{eff} = 140$ mV as achieving the best tradeoff.

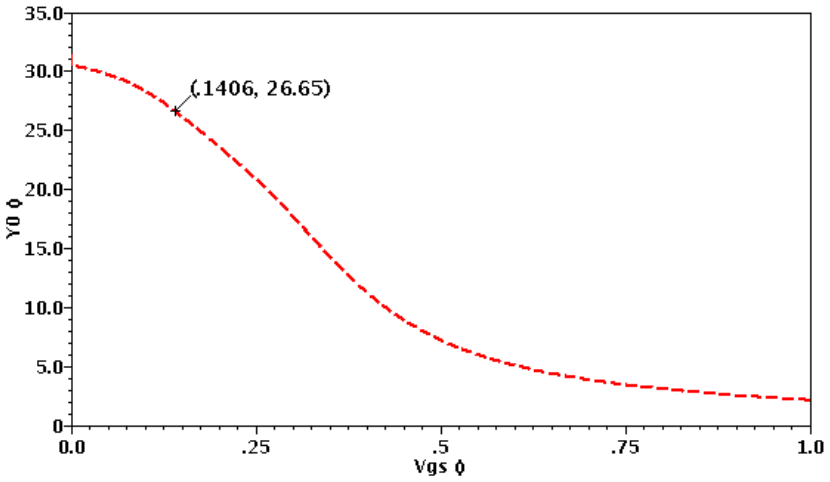


Figure A.4: Transconductance per unit of current versus effective voltage for a PMOS. Sizing for the transistor is $W = 3$ μ m and $L = 600$ nm.

These sizes will later be used for amplifier designs. For example, we know the bandwidth of a two-stage op-amp is given as

$$BW = \frac{g_m}{C_c} \,, \tag{A.6}$$

where C_c is the compensation capacitor and g_m is the transconductance of the input stage. Knowing the bandwidth requirements from settling

time behaviour and an approximate value for the compensation capacitance, a g_m value can be obtained. Knowing the g_m value, we can then obtain a power efficient current by using the formula

$$gm = \frac{2I_D}{V_{eff}} \ , \tag{A.7}$$

where V_{eff} is a power efficient voltage obtained by graphs similar to Fig. A.3 and A.4. The current then can be used as a first pass to solve for transistor ratio by using the equation of the MOSFET in saturation

$$\frac{W}{L} = \frac{\mu_n C_{ox} V_{eff}^2}{I_D} \ . \tag{A.8}$$

The sizing for a transistor is more of a heuristic argument. We know that intrinsic gain is inversely proportional to λ and λ is proportional to $1/L$. Therefore, for analog design we often do not use minimum size transistor and choose lengths that are two or more times the minimum. We cannot generalize too much, however, because the larger length also results in more parasitic capacitance and for high speed applications this may be detrimental. For sensor applications, bandwidth requirements are quite tame, and a size of five times the minimum length, or 600 nm has been used. The width size is then chosen to be $5-10$ times larger than the length for layout purposes[5].

[5] In this case, we have chosen a width of $3\mu m$ for all transistors.

For any given design, we may have several "unit" size transistors that are chosen based on the above analysis. We may choose a transistor that is two times the length, one that is five times the length and so on. The number of unit size transistors is then given by the size obtained by equations above and rounded up or down to a whole number[6].

[6] Square law equations are not accurate at small node sizes such as 0.13 μm so this rounding should not worry us. Designs must be validated by simulations regardless.

A.1.2 Gain

There are several factors that determine the gain that is required for op-amps at different stages of the $\Delta\Sigma$ modulator. These factors are reviewed here with the end goal of choosing a topology and specifications for op-amps in the design. As will be shown, only certain factors place a constraint on gain.

The finite gain of the op-amps changes the transfer function of the integrators by moving the pole locations[7] and therefore, changes the

[7] Pole locations of integrators then determine the zero location of the noise transfer function

behaviour of the delta sigma loop. The loop can normally tolerate some change, but how much can be tolerated depends on design and type of loop used. In this case, extensive simulations must be performed to make sure the performance of the system is met. To analytically determine whether the gain of the amplifier will be significant, we can relate it to the bandwidth of the system given as

$$\begin{aligned} \text{Bandwidth} &= 2\pi f_B \\ &= 2\pi \frac{f_s}{2 \cdot OSR} \\ &= \pi \frac{f_s}{OSR} \ , \end{aligned} \tag{A.9}$$

where f_B is the system bandwidth, f_s is sampling frequency and OSR is the oversampling ratio. If we take a simple integrator, and assume that the op-amp gain is finite, then we can show that the pole of this integrator will be equal to

$$z_p = 1 - \frac{1}{A}\frac{C_i}{C_f} \ . \tag{A.10}$$

A logical but still heuristic argument is then to surmise that we would like the poles of the integrator to be within the bandwidth of the system. Otherwise, the zero of the NTF will be outside the band of interest and degrade the noise shaping property of the loop. Based on this, we can write the gain requirement as

$$A > \frac{C_i}{C_f}\frac{OSR}{\pi} \ . \tag{A.11}$$

For a typical value of $C_f = 400$ fF and $C_i = 100$ fF, this indicates a gain of 32 dB which is relatively easy to achieve with two stage op-amp topologies. These insights can also be confirmed through simulations. Therefore, in general, the gain of integrators are not a limiting factor.

The gain of the DAC and converter op-amp, however, require more stringent specifications because they serve as the signal conditioning blocks for the input and feedback DAC. In a regular modulator, the input is directly sampled onto the first integrator. In the proposed architecture, the input must first be made available through a charge-to-voltage converter. In a regular modulator, the feedback DAC gain and

offset error are not detrimental to the output fidelity. In the proposed architecture, the output of the DAC is proportional to one of the sense capacitors and it must closely match the input difference in sense capacitors. As such, gain error is a limiting factor for both the input and feedback op-amps. The gain error can be given as

$$\text{Gain Error} = \frac{1}{1 + A\beta} \ , \tag{A.12}$$

where β is the feedback factor and A is the open loop low frequency gain of the amplifier. Since inputs to the first stage amplifier feed directly to the output [8], then if we are aiming for n-bit resolution, then gain error has to be less than $1/2^n$. This translates to an open loop gain of

[8] The signal transfer function is 1.

$$A > \frac{2^n}{\beta} \ . \tag{A.13}$$

Applying this equation to the first stage amplifier we have:

$$A > 2^n \frac{C_{f_1}}{(C_{f_1} \ + \ C_{p_1} + \ 2C_s)} \ . \tag{A.14}$$

where C_{p_1} is the parasitic capacitance at the inverting node of the op-amp. As we will show later, the parameter C_{f_1} will determine the noise contribution and signal power but it also has an effect on gain error as shown above. A compromise has to be made between gain error of the front end and the noise contribution as determined by C_{f1}. The chosen value [9] is 800 fF.

[9] as shown later in the noise section

A.1.3 Bandwidth and Current Requirements

The bandwidth requirement of the op-amp depend on the settling time requirements. For a switched capacitor circuit, the op-amp must be designed to settle within the required error for all clock phases. For the proposed architecture, the integration or gain phase are the worst case scenarios. In the gain stage, the switched capacitor circuit has the structure shown in Fig. A.5.

A properly compensated op-amp can be approximated as an integra-

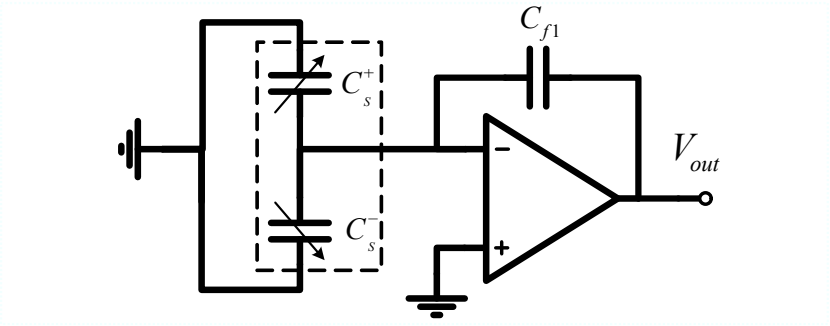


Figure A.5: The amplification phase of the feedforward and feedback stage used for settling analysis.

tor with transfer function

$$A(s) = \frac{g_m}{SC_o} \ , \tag{A.15}$$

where g_m is typically the transconductance associated with input stage transistors and C_o is either the Miller compensation capacitor or the equivalent load capacitance at the output of a one stage op-amp. Accordingly, the closed loop system of Fig. A.5 will have a pole given by

$$S = -\frac{\beta gm}{C_o} \ . \tag{A.16}$$

This will in turn give rise to an exponential settling time behaviour given by the time constant

$$\tau = \frac{C_o}{\beta g_m} \ , \tag{A.17}$$

and consequently for n-bit settling we require

$$\begin{aligned} e^{\frac{-t}{\tau}} &< 2^{-(n+1)} \\ t &> (n+1)\ln(2) \ . \end{aligned} \tag{A.18}$$

With a clock frequency of f_s, we have a period of T_s and half of the period is normally designated for each phase. Therefore, we would need to settle within $T_s/2$ but to give ourselves some margin, we may increase this to $T_s/4$. As such, the frequency requirements for the op-amp is given

as

$$\begin{aligned} \tau &< \frac{T_s}{4\ln(2)(n+1)} \\ \frac{C_o}{\beta g_m} &< \frac{T_s}{4\ln(2)(n+1)} \\ g_m &> \frac{4\ln(2)(n+1)C_o}{\beta T_s} \ . \end{aligned} \tag{A.19}$$

The value of C_o can then be determined from noise analysis as shown in the next section.

A.1.4 Noise analysis

Noise analysis on the delta-sigma loop combined with settling time behavior allows us to get a tolerance on the capacitor values needed for the system specifications (SNR). It is convenient for the proposed architecture to choose the *input* of the first integrator as the point to refer all noise sources [10]. The total noise is then given by the contribution of the capacitance to voltage converter, DAC and the first integrator and reduced by the oversampling ratio OSR. Accordingly, we can write

$$\overline{V^2}_{total} \approx \frac{\overline{V^2}_{conv} + \overline{V^2}_{DAC} + \overline{V^2}_{int}}{OSR} \ , \tag{A.20}$$

[10] This is how generally the design of a "normal" delta sigma is performed. The difference here is that our input needs to be conditioned first whereas in a delta-sigma, we are assuming that a signal is available at the appropriate level - a level close to the power supplies taking into consideration stability of the modulator.

Any noise after the first integrator is heavily attenuated by the high gain of the first integrator as well as the noise shaping property of the delta-sigma loop [67] and can be neglected.

The noise bandwidth plays a large part in determining the total noise for any of the above stages. In the integration or amplification phases, this noise bandwidth is a combination of the switch resistance and op-amp transconductance [72]. For the following derivations, it is assumed that, by design choice, the noise bandwidth is dominated by that of the op-amp as would be the case for a power efficient design. As such, noise due to the switches that are band limited by the op-amps are considered small compared to other terms and neglected in the following analysis for simplicity.

Accordingly, for the capacitance to voltage converter, the total noise

at the input to the first integrator is given by

$$\overline{V^2}_{conv} \approx \left[\frac{kT}{C_{f_1}} + \frac{16kTn_f}{3g_{m_1}} \frac{\beta_1 g_{m_1}}{4C_{o_1}} \left(1 + \frac{2C_s + C_{p_1}}{C_{f_1}} \right)^2 \right] , \tag{A.21}$$

where k is Boltzmann's constant, T is temperature in Kelvins, $\beta_1 = C_{f_1}/(C_{f_1} + C_{p_1} + 2C_s)$, C_{p_1} is the parasitic capacitance at the inverting stage of the op-amp, g_{m_1} is the transconductance of the converter stage op-amp as determined by the settling time requirements and $n_f \geq 1$ is a noise factor for the converter stage op-amp that depends on the architecture of the op-amp used.[11]

[11] A single stage differential pair op-amp would have a noise factor of 1.

The term C_{o_1} requires further explanation. It is the effective load capacitance that limits the bandwidth of the op-amp. For a Miller compensated op-amp, C_{o_1} is equivalent to the compensation capacitor C_c. For a single stage op-amp, it is the load capacitance given by

$$C_{o_1} = \frac{(2C_s + C_{p_1})C_f}{2C_s + C_{f_1} + C_{p_1}} . \tag{A.22}$$

Similarly, for the DAC feedback stage, the total noise due to the DAC switches and op-amp is given by

$$\overline{V^2}_{DAC} \approx \left[\frac{kT}{C_{f_2}} + \frac{16kTn_f}{3g_{m_2}} \frac{\beta_2 g_{m_2}}{4C_{o_2}} \left(1 + \frac{2C_s + C_{p_1}}{C_{f_2}} \right)^2 \right] , \tag{A.23}$$

where $\beta_2 = C_{f_2}/(C_{f_2} + C_{p_1} + 2C_s)$, C_{o_2} is the effective op-amp load, and g_{m_2} is the transconductance of the DAC op-amp.

Finally, the integrator noise is given by

$$\overline{V^2}_{int} \approx \left(\frac{kT}{C_1} + \frac{4}{3} \frac{kT}{C_{o_3}} n_f \beta_3 \right) , \tag{A.24}$$

where $\beta_3 = C_{f_3}/(C_{f_3} + C_{p_2} + C_2 + C_1)$, C_{o_3} is the effective op-amp load, g_{m_3} is the transconductance of the integrator op-amp and C_{p_2} is the parasitic capacitance at the inverting input of the integrator.

Regardless of the op-amp topology, the load capacitance in the form shown in Eq. (A.22) or the Miller compensation capacitance will be of the same order of magnitude. This is because in both cases, the capacitance determines the dominant pole of the op-amp. As such, in the analysis that follows, we will make use of Eq. (A.22) [12] which allows us to determine the tradeoff between the various capacitance values.

[12] and it's variants for the DAC and integrator stage

Brownian Noise And Limitations of Oversampling

Brownian noise is the name of the thermal noise associated with mechanical structures and given by

$$a_{nb}^2 = \frac{4k_BT}{9.8^2 m^2} \ , \tag{A.25}$$

where a_{nb} is noise force in units of gravity (1 g = 9.8 m/s^2). Although the noise is broadband much like thermal noise, the accelerometer's second order system filters this noise to a few KHz as determined by the natural frequency of the mechanical system, ω_n. As a result, oversampling in the electronic front end has limited effect on the Brownian noise. This is demonstrated in Fig. A.6.

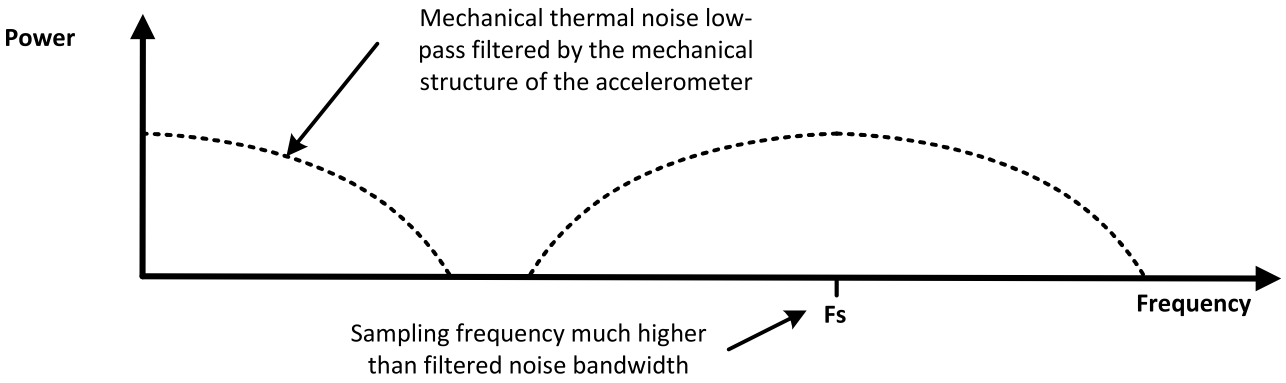


Figure A.6: Sampled mechanical thermal noise spectrum. Oversampling of thermal noise can have minimum effect depending on sampling frequency.

For the accelerometer used ($\omega_n \approx 4$ KHz), the sampling frequency of 64 KHz is well beyond the bandwidth and as such, oversampling has a negligible effect. Therefore, the mechanical noise as given by Eq. (A.25) contributes entirely to the total noise of the system and is not reduced by the oversampling ratio.

Total Noise

Based on the above discussion, the total noise of the system is given by the orthogonal combination of the Brownian noise and the electronic noise. The thermal noise will be reduced by the oversampling ratio, but as we have just discussed, the Brownian or mechanical thermal noise will not be. As such, we can write the total noise at the input of the

first integrator as

$$\text{Total Noise} = \frac{4k_BT}{9.8^2m^2}\left(\frac{2C_s}{C_{f1}}\right)^2 + \frac{\overline{V^2}_{conv} + \overline{V^2}_{DAC} + \overline{V^2}_{int}}{OSR} \quad . \quad \text{(A.26)}$$

Using the above equation, we can then determine a value for C_{f1}, the feedback capacitor for the feedforward (and feedback DAC) stage. The larger capacitance lowers the output signal but also has an effect on the total noise of the system. The feedback capacitor also determines the gain requirements of the op-amp as discussed in the previous section. The gain and SNDR tradeoff is plotted in Fig. A.7. Based on this plot, a realistic value of feedback capacitor is between $400 - 800$ fF.

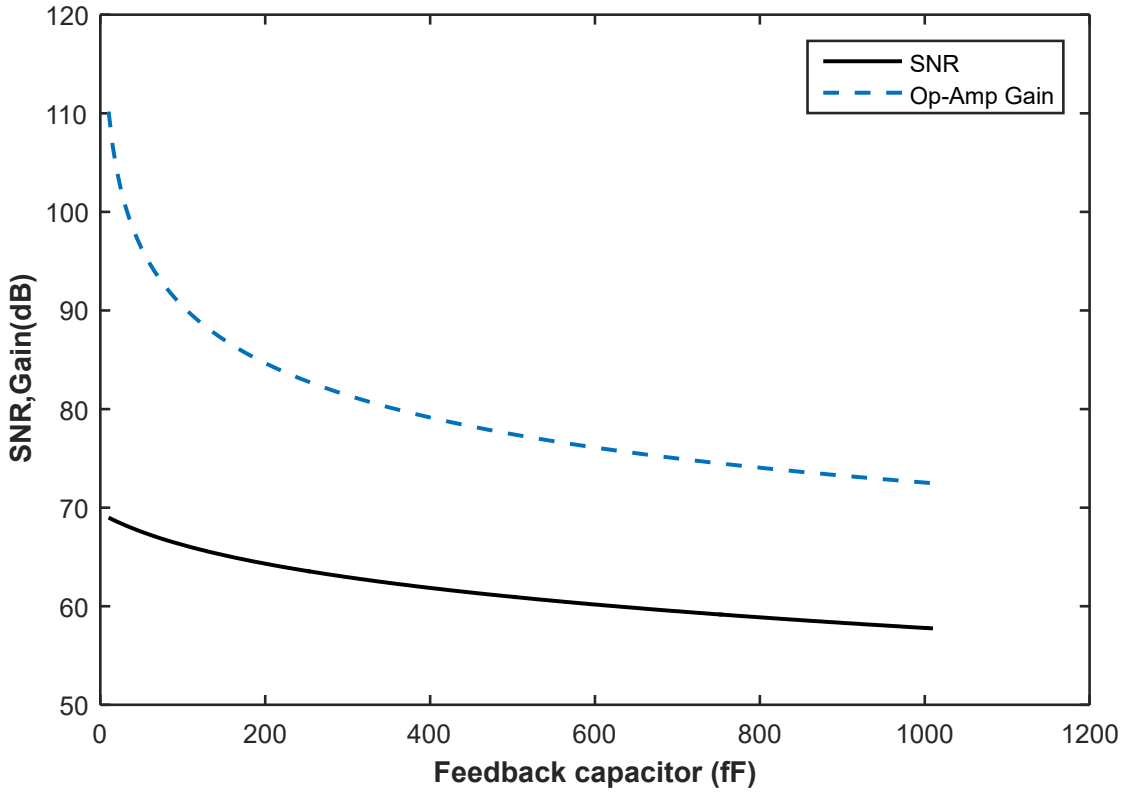


Figure A.7: DAC and charge amplifier feedback capacitance tradeoff versus op-amp gain and system fidelity.

Using the value of C_f obtained above, we can then calculate the value of g_m required for linear settling as discussed in Section A.1.3. This then leads directly to op-amp sizes given the bandwidth requirements for the application.

A.1.5 Single-Ended Op-Amp

Based on the gain error and noise analysis in the previous section, a gain of 75 dB is required for the op-amps in the front-end stage. The bandwidth requirements for the given applications are not stringent[13] and as such, the architecture chosen is a folded cascode with a common source output stage. Another reason for this choice of architecture is that it allows us to independently set the output and input common modes which can be beneficial given the architecture's emphasis on flexibility in setting the reference voltages. The op-amp at the transistor level with sizing is shown in Fig. A.8.

[13] In open loop, the bandwidth is determined by the mechanical resonance of the accelerometer which is limited to a few KHz due to fabrication tolerances.

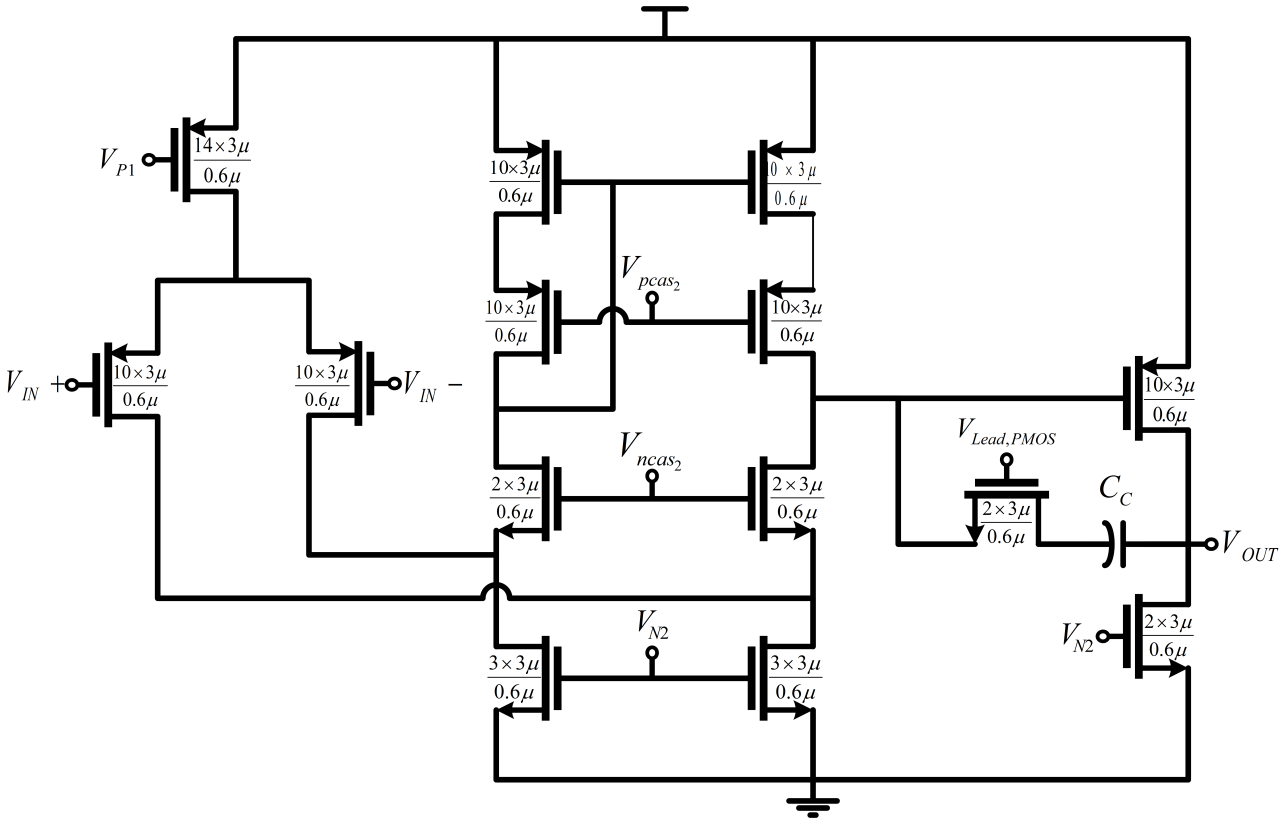


Figure A.8: Front-end op-amp sizing. Sizes shown are for the capacitance to voltage stage. The DAC stage sizes are a multiple of the above.

A.1.6 Differential Op-amp

The differential version of the folded cascode plus common source output is chosen for the differential op-amp as well. The design is shown in Fig. A.9.

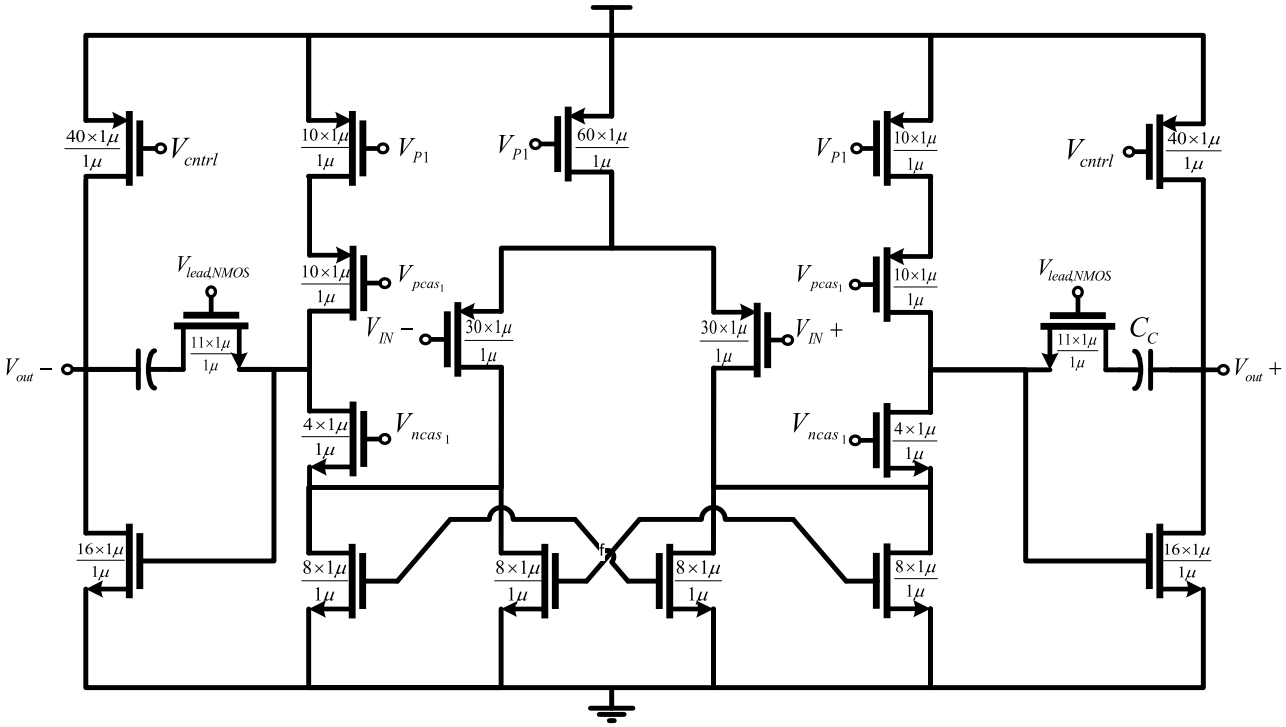


Figure A.9: Differential op-amp sizing.

A.1.7 Common Mode Feedback

The common mode feedback for the differential amplifier is shown in Fig. A.10. The difference in the current output DC component compared to an ideal reference is sampled onto capacitor C_1. This value is then used to update the output voltage. Note that C_2 purpose is only to dampen the charge placed onto C_1 for updates to have a smoother transition.

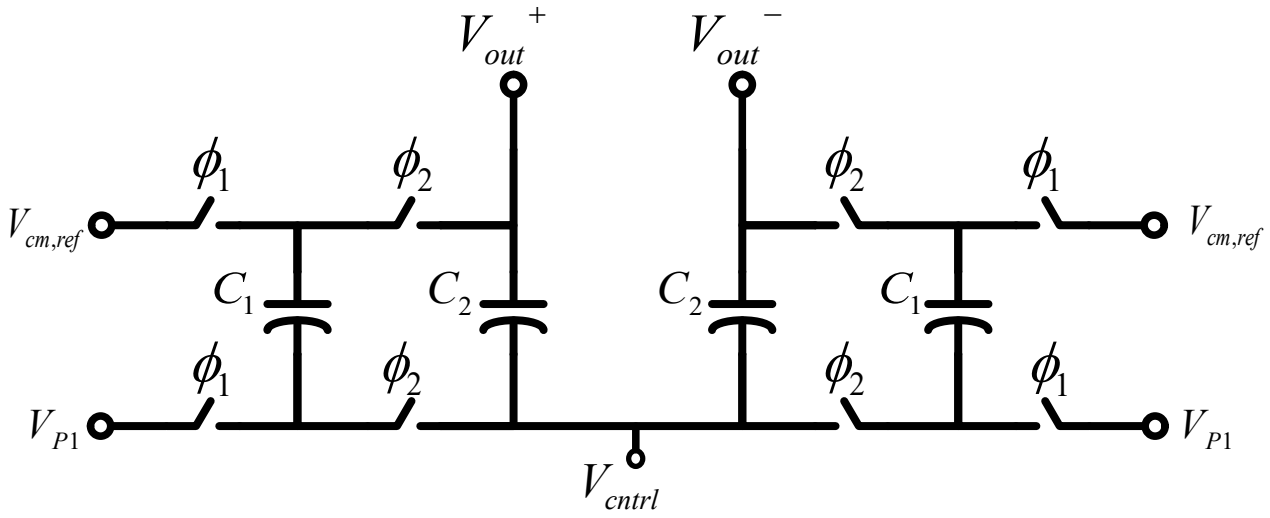


Figure A.10: Common mode feedback circuit.

A.2 Clock Generation

Clock generation for the present application is extremely important given the many phases required. The overall functionality of the system highly depends on error free clock signal generation. This sections details the necessary steps in creating glitch free clocks.

Feeding the clock directly from outside of the chip to a clock generator on chip can cause many problems. To illustrate this, assume that a clock from outside the chip is being fed into some logic[14] as shown in Fig. A.11. This is a poor method of clock generation as shown in the timing diagrams.

[14] that will create the none-overlapping clocks

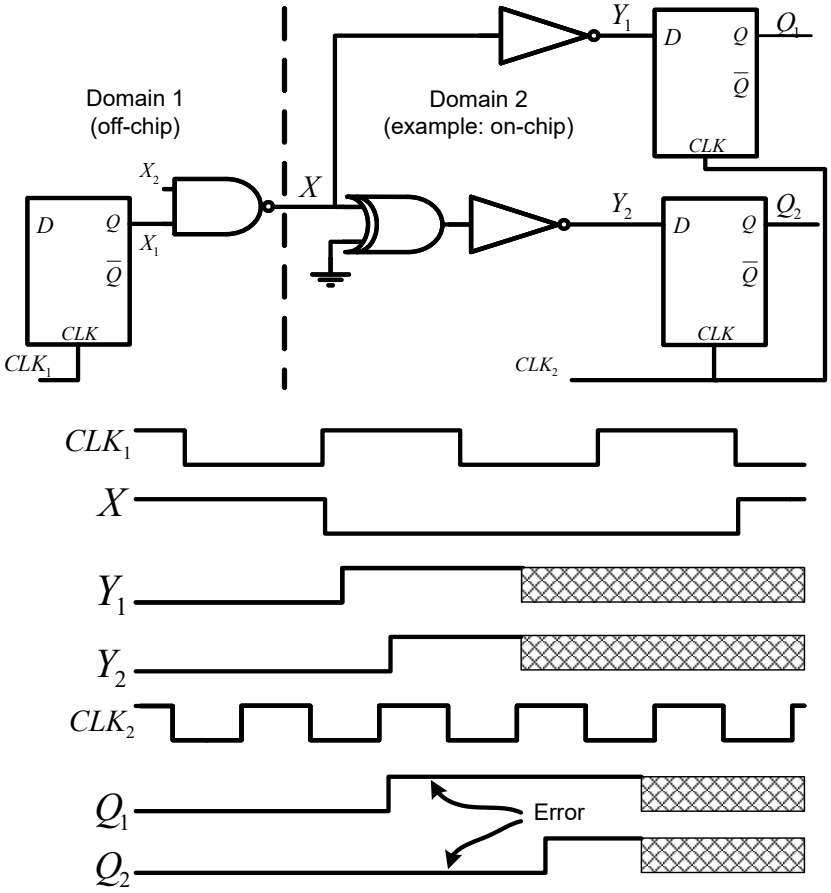


Figure A.11: A poor method of clocking between two domains.

Referring to Fig. A.11, assume that the flip flops are triggered on the rising edge and there is a transition on node X. This transition propagates to nodes Y_1 and Y_2 but due to the different logic that each

signal path goes through, one signal is delayed compared to the other. Now assume that CLK_2 then triggers the signals between the delay. Therefore, Q_1 and Q_2 resolve to different values and for a whole clock period Q_1 and Q_2 are different when they should have been exactly the same. This error essentially arises from the fact that the two clock signals are asynchronous. Even if the clocks were from the same source, delays in their paths can cause this problem.

To solve this issue, we can add a flip flop as shown in Fig. A.12, and delay the signal X by one clock cycle. This will fix the asynchronous problem just discussed but will lead to another problem.

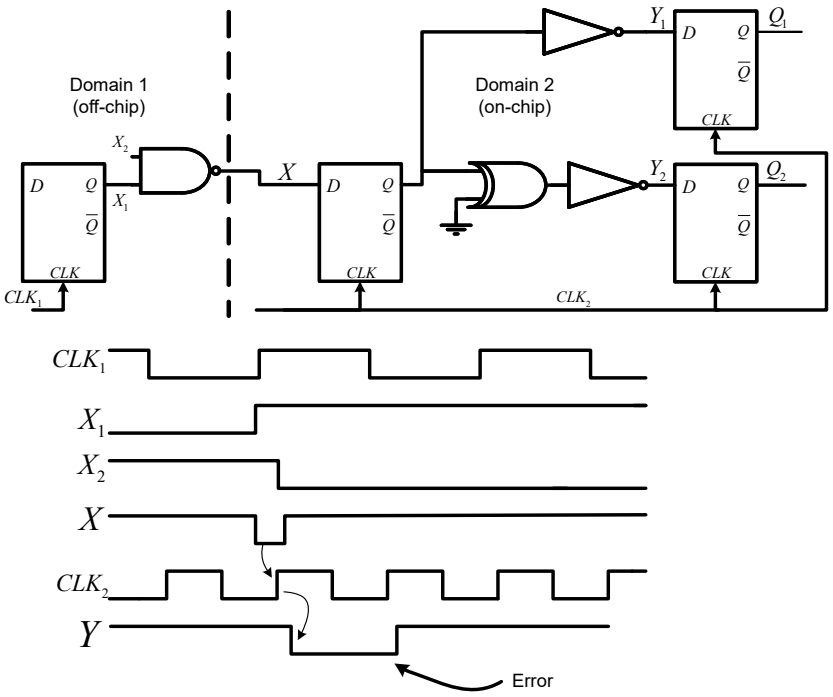


Figure A.12: An improved clock generation scheme.

Assume that X_1 and X_2 are going through separate logic delays and as such, a glitch occurs as shown in the timing diagram of Fig. A.12. As a result, CLK_2 may sample the result in the region of the glitch and cause an error. So how do you get rid of this problem? You have to make sure that you never get a glitch on the node X and we do this by adding another latch. Therefore, by having a latch before and after the domain transition (on-chip and off-chip), we eliminate the possibility of either of the above described errors.

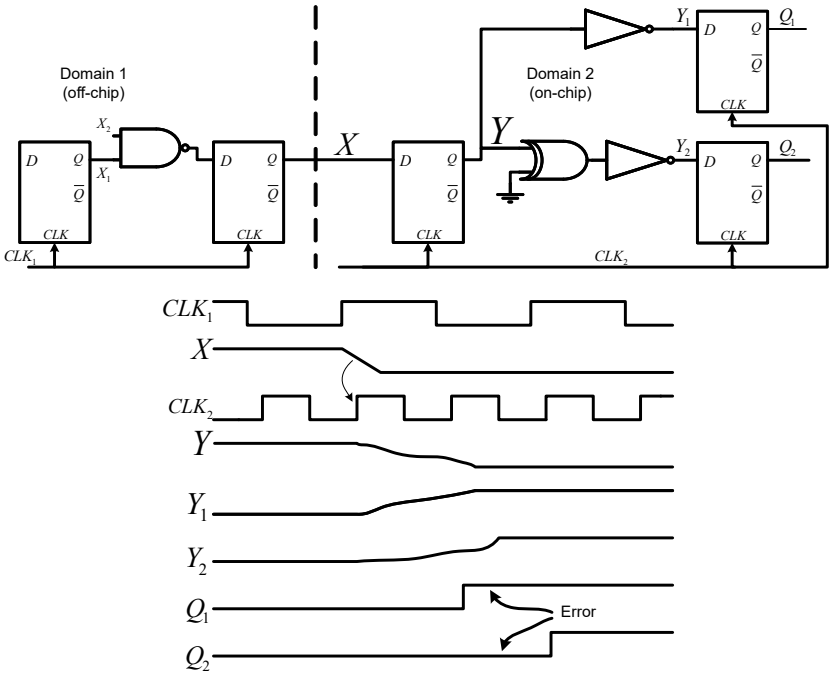


Figure A.13: Further improvement to clock generation.

The last issue is metastability and this is an issue that you can never eliminate but you can reduce it. The issue is shown in Fig. A.13. As with any digital signal, clocks do not have infinite rise and fall times. As such, nodes such as X also have finite rise and fall times. If CLK_2 happens to catch node X in a transition, then node Y will either toggle up or down because it has been sampled in the middle of a transition[15]. It does not matter how the node is resolved, we need to make sure that one is chosen before the next clock trigger. However, as before, since Y_1 and Y_2 have different delays, a situation could arise where the flip-flops will resolve one to a high value and the other resolves to a low value.

[15] In other words, the setup time of the latch has been violated.

The solution is then to clock node Y again to make sure that it gets resolved. So we add another flip flop at the second clock domain. This does not solve metastability but now, flip flop 1 can sample in the middle of a transition, but flip flop 2 will then allow another full cycle for the signal to resolve the output. You can also add a third flip flop to give even more time for any metastability to resolve but generally two is enough[16].

[16] But one is not enough!

Based on the above discussion, the clocks for the systems are gen-

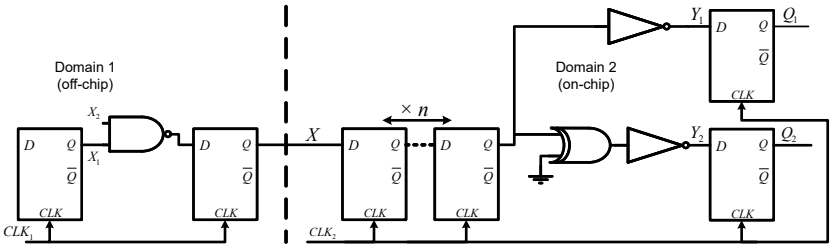


Figure A.14: Final solution for clock distribution between two domains.

erated from a single clock as shown in Fig. A.15. We feed in a clock that is 16 times our sampling frequency. The reason for this is that the DAC feedback requires clocks to be 4 times faster, and by the above reasoning, we require 3 flip flips before hand to eliminate errors and reduce metastability. The logic gates generating the clock phases may seem complicated but they are simply using differences in signal paths to create none-overlapping clock phases.

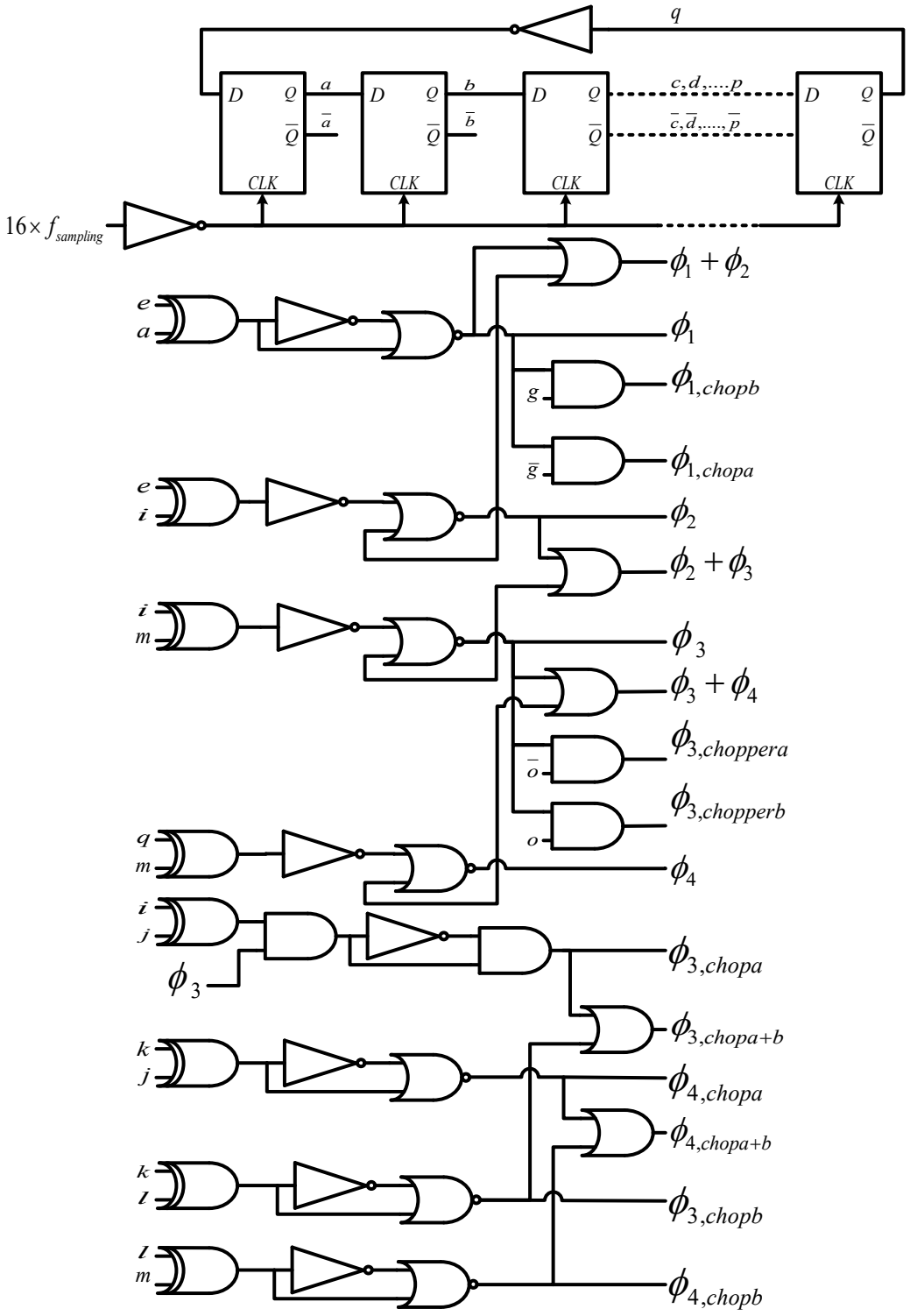


Figure A.15: On-chip clock generation circuitry.

A.3 Comparator Design

Comparators for delta sigma modulators with a one-bit quantizer do not have rigorous requirements on noise or offset since the output is only being placed onto two levels. As long as the offset and noise is not time varying or input dependent, then the noise shaping property of the loop is preserved by the quantizer. The major criteria is then to choose a low power comparator for the present application . As such, we make use of a dynamic comparator with zero static current [80]. The design is shown in Fig. A.16. In ϕ_1, the capacitor C_{in} is charged to the difference in the input value compared to a reference[17]. The output is then compared to the input and a regenerative latch resolves the difference. The choice of capacitors influences the offset error and power consumption as the loading of the capacitors directly increases the output power of the integrator stage driving it. In this design, $C_{in} = C_{ref} = 150$ fF.

[17] a good choice for the reference is half the supply voltage as this maximizes the output swing of the last integrator.

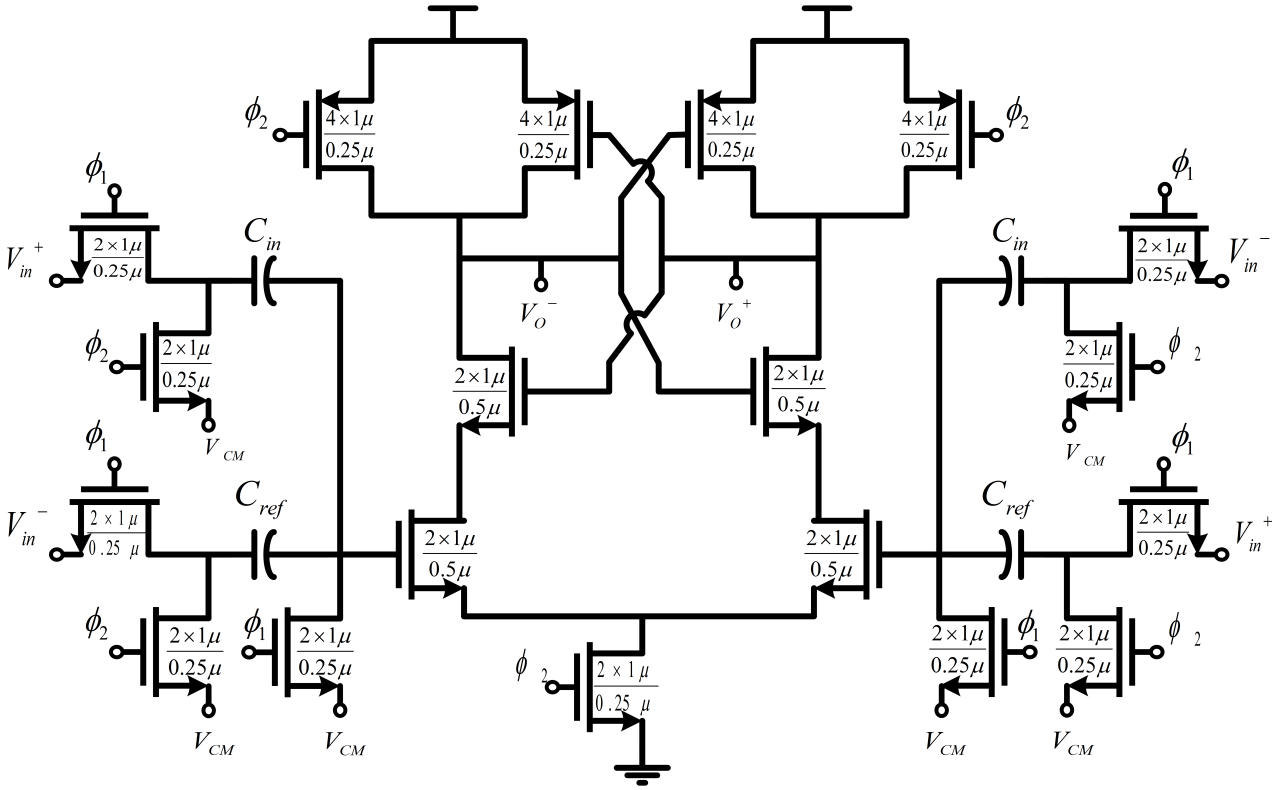


Figure A.16: Schematic of dynamic comparator used in the delta sigma modulator.

B

Noise Simulation

B.1 Introduction

Noise simulation in CAD tools is a very circuit dependent. If a circuit is linear, then noise analysis can be performed by linearizing the system around an operating point and performing AC analysis around this operating point. However, for switched capacitor circuits, since the steady state is always changing between two or more phases, linearization around an operating point does not work. A solution to this is to use periodic steady state (PSS) and PNOISE simulation. The details of these setups are not discussed within here, but as the name suggests, periodic steady state assumes that a circuit has steady states in certain periods. A settling time is allowed for these states, and the noise taken at each period during the steady state.

PSS+PNOISE will often be more efficient way of simulating the noise in a periodic circuit. For delta-sigma ADC's, the circuits are neither linear or periodic. A possible solution to this is to use quasi-period steady state (QPSS) followed by QPNOISE simulation. These kind of simulations would require the linearization of the delta sigma loop [81].

B.2 Transient Noise Setup

If a circuit has a large signal response to the noise, then QPSS and QPNOISE can often be inaccurate or may not converge at all. This is the case with delta sigma ADCs where the noise has an influence on the loop. As such, transient noise simulation is a technique that can be

used for any circuit and results can be trusted more readily. Even if the steady state noise technique is used, designers are advised to confirm this with a transient noise simulation. The parameters for the transient noise using the Cadence Spectre simulator are chosen as follows:

- **Noise Fmax**: This parameter sets the maximum frequency that the circuit can expect. With Fmax, the noise density at the Fmax is calculated[1] and this noise is then treated as *white* noise at all frequencies.

  Due to noise folding that is often prevalent in switched capacitor circuits, a good rule of thumb is to choose this parameter to be 5X to 10X the corner frequency of the fastest op-amps in use. Since this parameter greatly affects simulation time, it is worthwhile to perform multiple simulations with different Fmax values and compare the output noise. The result is then used to choose an optimal value of Fmax that minimizes the simulation time and is fairly accurate.

- **Noise Fmin**: If it is desired to have coloured noise such as flicker noise in the simulation, then this is set by the parameter Fmin. With Fmin set, the simulator will include coloured noise between Noise Fmax to Noise Fmin.

- **Noise Seed**: This is a parameter that sets the noise random generation. Choosing the same seed for the same circuit should (all else being equal) result in exact same output. Leaving this parameter blank results in different transient for each invocation of the simulation.

- **Noise Scale**: This parameter scales the noise level by the factor given. It can be used as a way to overdesign, for example, in a case where the noise models are thought to be over-simplified.

- **Noise Tmin**: This is the time step between noise source updates and set to by default to 0.5/(Noise Fmax). Smaller values produce a more smooth noise profile but also greatly increase circuit simulation time.

- **Noise Update**: This sets the evaluation time of the bias-dependent device noise sources (such as MOSFETs) to a certain step length

[1] Using all noise generating devices

defined by Noise Tmin parameter (Step option) or the maximum noise frequency (Fmax). For a switched capacitor circuit, a step length of 1/10 the sampling frequency may suffice and choosing a correct time step can greatly reduce simulation time.

- **Noise Contributors**: This parameter can be used to set or disable a certain set of noise sources in the schematic. It is useful for debugging purposes in determining noise contribution from different sources.

C

Other Measurements

C.1 Cross Sensitivity Testing

Cross sensitivity testing measures the response or sensitivity of the sensor to an acceleration in an orthogonal direction. The purpose of these tests is two fold:

- It confirms that there is enough isolation between an accelerometer axis to not cause errors in other directions.
- For the particular test setup, it confirms that harmonics seen at higher frequencies are due to background mechanical noise and not the input acceleration force.

There are four cross sensitivity measurements performed: x-y, y-x, z-y and z-x. The first letter refers to the direction of measurement and the second letter refers to the direction of input acceleration force. Each cross sensitivity is measured at two frequencies of 3.90625 Hz and 7.8125 Hz corresponding to 0.15 g and 0.6 g accelerations respectively[1]. For all tests, reference voltages are $V^{+}_{ref1} = 950$ mV, $V^{-}_{ref1} = 250$ mV, $V_{ref2^{+}} = 625$ mV, $V^{-}_{ref2} = 575$ mV. The test results show cross sensitivity in all directions of better than 60 dB. The environment noise components are confirmed to be at higher frequencies and constant in all directions.

[1] Two frequencies were measured due to the limitation of the test equipment

C.1.1 X to Y cross-sensitivity

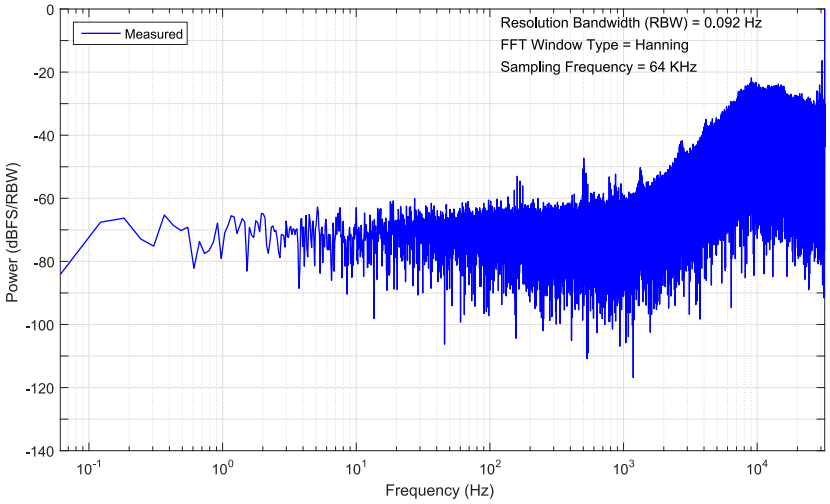


Figure C.1: X-direction cross sensitivity to acceleration in the y-direction at 3.90625 Hz with magnitude of ±0.15 g.

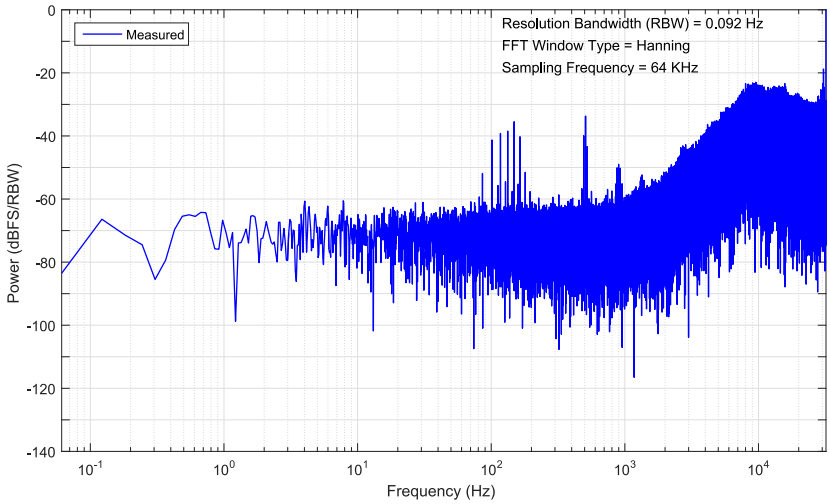


Figure C.2: X-direction cross sensitivity to acceleration in the y-direction at 7.8125 Hz with magnitude of ±0.6 g.

C.1.2 Y to X cross-sensitivity

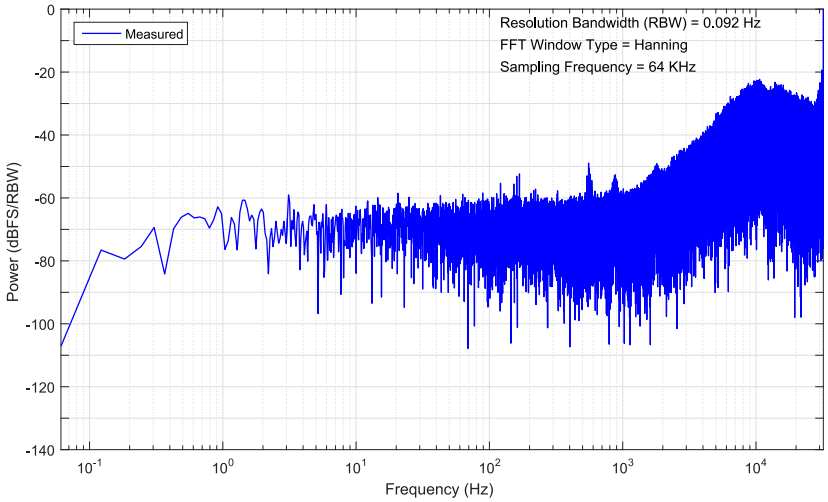


Figure C.3: Y-direction cross sensitivity to acceleration in the x-direction at 3.90625 Hz with magnitude of ±0.15 g.

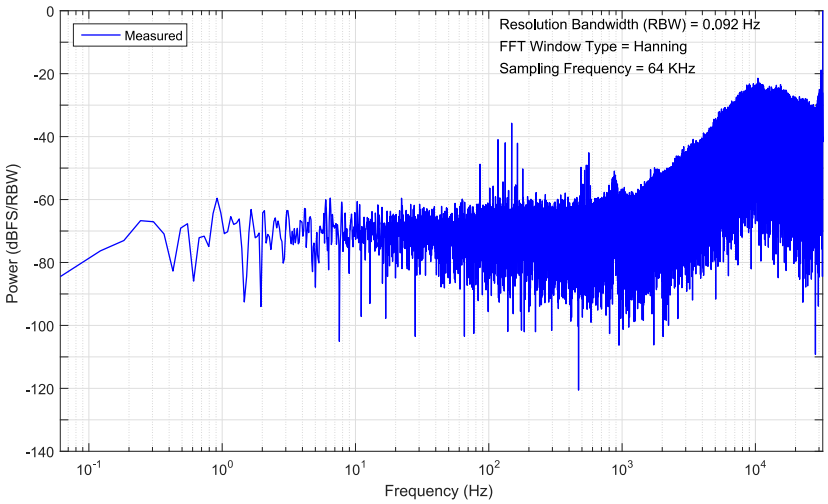


Figure C.4: Y-direction cross sensitivity to acceleration in the x-direction at 7.8125 Hz with magnitude of ±0.6 g.

C.1.3 Z to X Cross-Sensitivity

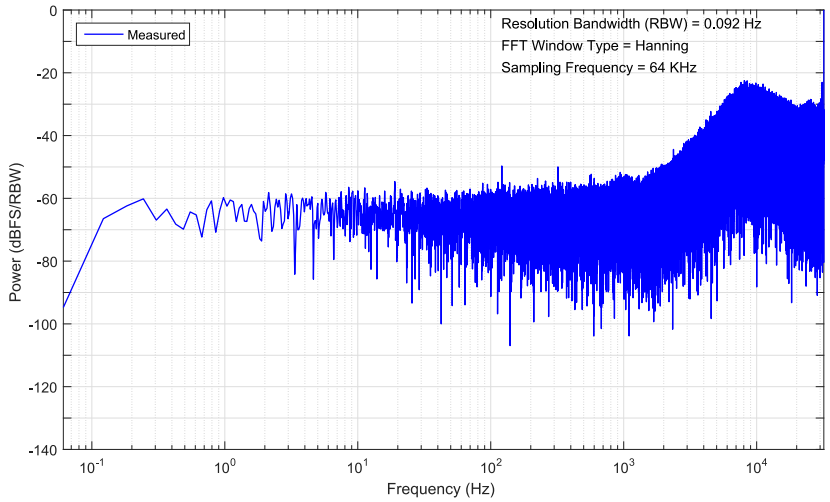


Figure C.5: Z-direction cross sensitivity to acceleration in the x-direction at 3.90625 Hz with magnitude of ±0.15 g.

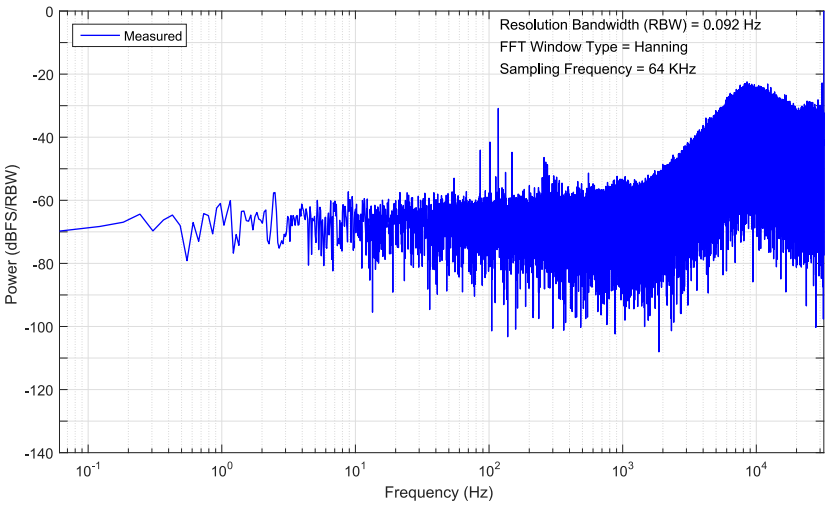


Figure C.6: Z-direction cross sensitivity to acceleration in the x-direction at 7.8125 Hz with magnitude of ±0.6 g.

C.1.4 Z to Y Cross-Sensitivity

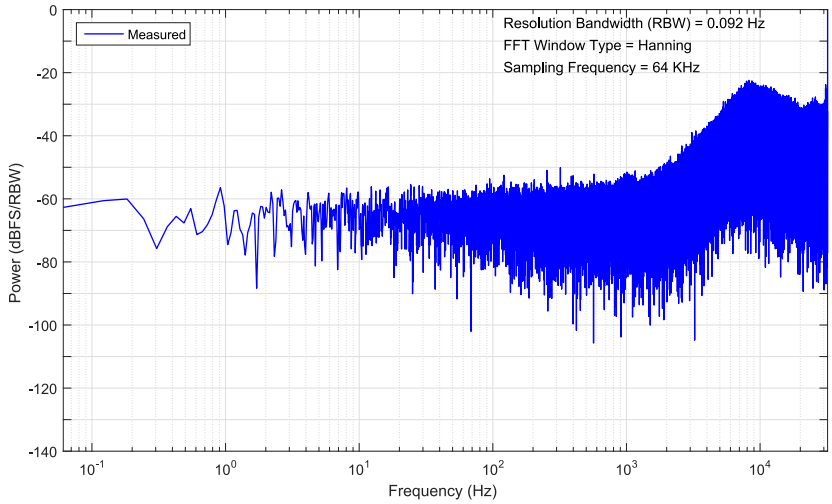


Figure C.7: Z-direction cross sensitivity to acceleration in the y-direction at 3.90625 Hz with magnitude of ±0.15 g.

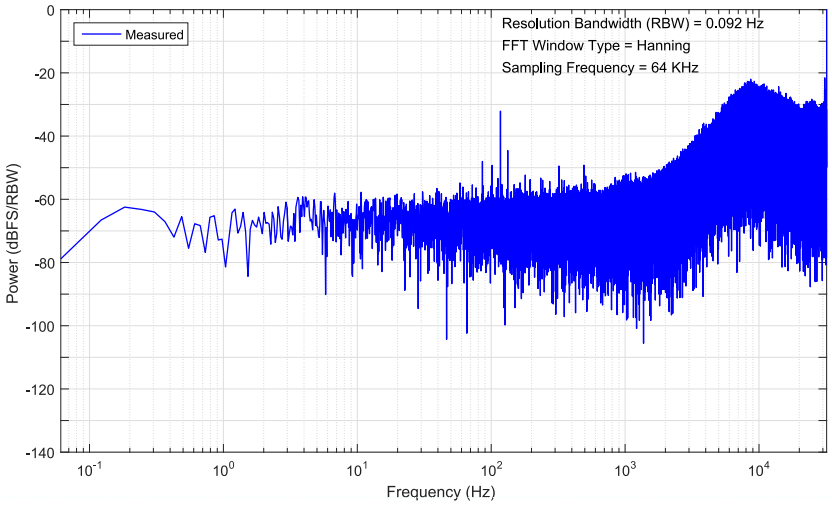


Figure C.8: Z-direction cross sensitivity to acceleration in the y-direction at 7.8125 Hz with magnitude of ±0.6 g.

D

Accelerometer Theory and Principles of Operation

There are several physical processes that can be used to measure an acceleration force and in turn velocity and position[1]. In general, an accelerometer either directly measures the acceleration or measures rotation and deduces acceleration from it. In the former cases, such sensors are called accelerometers and the principle of their operation is based on Newton's second law. To measure rotation on the other hand, devices make use of what is called Coriolis force and are called rate accelerometers or gyroscopes. Readout circuits for gyroscopes are not discussed in this thesis although some concepts can be extended. Our focus is therefore accelerometers and their operation. In the following derivation, the force to be detected is due to an accelerating object; however, an external force may not necessarily be the result of an acceleration[2].

[1] If the acceleration force results in a movement.

[2] For example, an object placed on a table experience a force of 1 g due to the Earth's gravity but clearly it is not accelerating because it is stationary.

D.1 Development of the Accelerometer Model

An accelerometer is often modeled as the ubiquitous mass connected to a spring and attached to a casing as shown in the Fig. D.1. Most literature will then delve into the analysis of the accelerometer by writing equations for this mass-spring system. However, it is more intuitive to treat the accelerometer as a black box and try to develop the need for the spring-mass system.

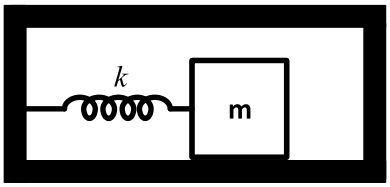


Figure D.1: Accelerometer modeling using a mass and spring.

We begin our analysis by assuming that the accelerometer (for now treated as a black box) is placed on an object which is undergoing an acceleration a_f. We are interested in measuring the acceleration of the

object and in turn use this information to obtain the velocity as well as the position in order to make certain observations about our environment. Therefore, we want to know from first principles what should be placed inside the shaded region of Fig. D.2.

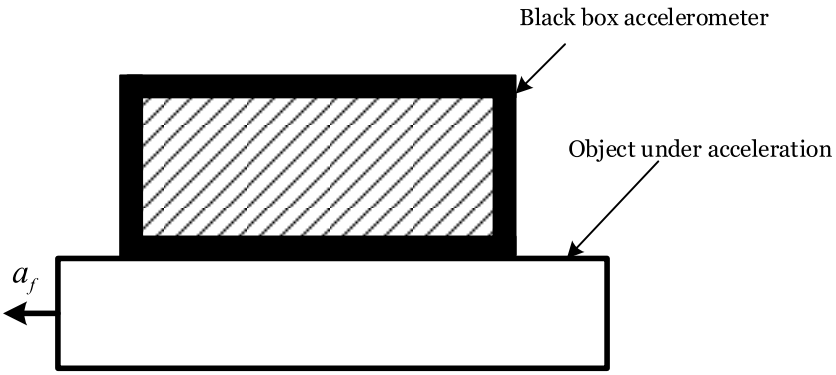


Figure D.2: A black box accelerometer undergoing acceleration.

We may wonder that perhaps the accelerometer can simply be a solid block of material. To test this hypothesis, we look at the forces being exerted on the object and the accelerometer using the familiar Newton's laws and try to deduce the acceleration a_f. We can look at the accelerometer and object under acceleration in two ways: as one object or as two separate objects [82]. Since we are ultimately interested in the forces exerted on the accelerometer, a two object approach is more useful.

According to Newton's second law, if an object is experiencing an acceleration, a_f, then a force of $m \cdot a_f$ must be acting upon it. The accelerometer, however, will also exert a force on the object of opposite polarity. The forces acting on the object under acceleration can be given as

$$F_{applied} - F_{accelerometer} = m_{object} \cdot a_f \ . \tag{D.1}$$

At the same time, the forces acting on the accelerometer dictate that

$$F_{accelerometer} = m_{accelerometer} \cdot a_f \ . \tag{D.2}$$

We can combine Eq. (D.1) and (D.2) to find the acceleration as

$$a_f = \frac{F_{applied}}{m_{accelerometer} + m_{frame}} \ . \tag{D.3}$$

This equation, however, is not useful. To find acceleration, we need to know both the mass of the object and the force being applied to it. But if we know these terms, then we already know the acceleration. Therefore, clearly having an accelerometer that is a block of material does not provide any useful information.

Then how can we determine the acceleration of an unknown object? The solution is to place within the casing of the accelerometer another mass with the weight of m. For the moment, assume that this mass is not attached to the casing and is free to move. When the object attached to the accelerometer accelerates, the mass, according to Newton's first law, will remain stationary and move to one side of the casing where the wall then provides the necessary force to accelerate the object at the rate as the frame. If friction is taken into account, not much changes, as friction provides an additional force to accelerate the object. This situation is still not useful for measuring the acceleration.

Now assume that we attach a spring to the mass, and attach the spring to the casing of the accelerometer. Now, when the casing accelerates, the spring will advance to provide the necessary force on the mass to accelerate it as shown in Fig. D.3.

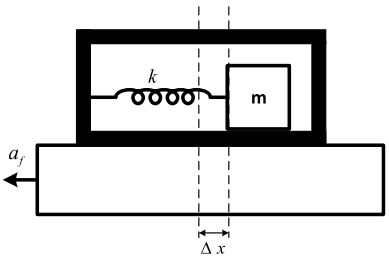


Figure D.3: Accelerometer modeled with a mass and spring undergoing acceleration. Notice that for analysis, we assume a *frictionless surface.*

As it can be seen, the mass has moved by Δx to the right side, and the spring has stretched. In this case, the force on the seismic mass must be equal to the force of the spring give by Hooke's law. Therefore, we can write that

$$ma = -k\Delta x \ . \tag{D.4}$$

We can generalize the above equation by assuming that the acceleration is some variable of time and making a change in variable by letting $x = \Delta x$. Therefore,

$$ma(t) = -kx(t) \ , \tag{D.5}$$

and knowing that the acceleration is a second derivative of position we have

$$m\frac{d^2x(t)}{dt^2} = -kx(t) \ . \tag{D.6}$$

For better visualization, we will use the dot format to represent the first and second derivatives and drop the time notation such that time will be implicitly implied with the equation. Thus our equation becomes

$$m\dot{x} + kx = 0 \ . \tag{D.7}$$

We have finally arrived at an equation that relates the acceleration of an object (table) to the mass of the accelerometer to which to object is attached to[3]. This is a second order homogeneous linear differential equation and what remains is to solve the equation for an answer. Recalling techniques for solving LDE's, we begin by writing the auxiliary equation for Eq. (D.7), mainly

[3] we do not know the mass of the object, but we certainly know (or should know) the mass of the device we attach to the object to detect its acceleration

$$mr^2 + kr = 0 \ . \tag{D.8}$$

The roots of the auxiliary equation are $r = \pm\omega_n i$, where $\omega_n = \sqrt{\frac{k}{m}}$. Since the roots are imaginary, then the general solution for the equation is

$$x(t) = C_1 \cos(\omega_n t) + C_2 \sin(\omega_n t) \ , \tag{D.9}$$

where C_1 and C_2 are arbitrary constant that are dependent on the initial conditions (location and velocity of the internal mass at $t = 0$). We can write the above equation in a more compact form as

$$x(t) = A \cos(\omega_n t + \phi) \ , \tag{D.10}$$

where

$$A = \sqrt{C_1^2 + C_2^2} \ , \tag{D.11}$$

and the phase angle ϕ satisfies

$$\cos(\phi) = \frac{C_1}{A} \ , \tag{D.12}$$

$$\sin(\phi) = -\frac{C_2}{A} \ . \tag{D.13}$$

An astute reader may be puzzled by Eq. (D.10) and rightly so. What Eq. (D.10) indicates is that any initial force that moves the mass from its initial position will cause the mass to oscillate with frequency ω_n indefinitely. The input only affects the maximum amplitude that the mass achieves or in other words, the values of C_1 and C_2.

This type of motion is known as *simple harmonic motion* and although mathematically correct, it does not have a bearing in the real

world. Something is missing from our original equation. The reader may quickly guess that what is missing is the friction that the mass will face with the air or fluid and/or the surface with which it is encased in as it oscillates back and force. This friction tends to "dampen" the oscillation until it completely stops. We call this force the damping force and model it as a linear dependence on velocity according to

$$\text{damping force} = -b\frac{dx(t)}{dt} \ . \tag{D.14}$$

To model the air or fluid friction, we introduce a dashpot to the system. The dashpot is in fact a physical device used and modeled in many mechanical systems. In this particular case, it is meant to act as a model for the resistance that the mass faces. Our new model is shown in Fig. D.4.

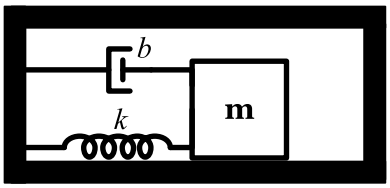


Figure D.4: Complete accelerometer model with a mass, spring and dashpot.

Although in Fig. D.4 we have made the dashpot coefficient b a constant, this is only an approximation and in general, the air for fluid damping is dependent on many factors including the range of input vibration expected. A more general formula for the damping is then given by [83] [84]

$$b(x) = \mu A^2 \left[\frac{1}{(d_1 - x)^3} + \frac{1}{(d_2 - x)^3}\right] \ , \tag{D.15}$$

where x is the mass deflection, d_1 and d_2 are the distance from the mass to each electrode, μ is the viscosity of air and A is the area of the plates. For our purposes, however, a constant will suffice at this point in time.

D.2 Unforced Vibrations

If we apply newton's second law again to the accelerometer only, then it will have a restoring force caused by the spring and a damping force caused by the dashpot. Assuming for now that there is no external force being applied, we can write

$$m\frac{d^2x(t)}{dt^2} = \text{restoring force} + \text{damping force} \ , \tag{D.16}$$

$$= -kx(t) - b\frac{dx(t)}{dt} \ . \tag{D.17}$$

Therefore,

$$m\frac{d^2x(t)}{dt^2} + kx(t) + b\frac{dx(t)}{dt} = 0 \ , \tag{D.18}$$

or in dot notation

$$m\ddot{x} + b\dot{x} + kx = 0 \ . \tag{D.19}$$

The equation above is a second order homogeneous equation that is prevalent in many fields of engineering and used to model a wide variety of phenomena. The solution to the equation again requires looking at the characteristic equation, in this case

$$mr^2 + br + k = 0 \ . \tag{D.20}$$

And the solution is therefore given as

$$r_1 = \frac{-b + \sqrt{b^2 - 4mk}}{2m} \ , \tag{D.21}$$

$$r_2 = \frac{-b - \sqrt{b^2 - 4mk}}{2m} \ . \tag{D.22}$$

Depending on the value of $b^2 - 4mk$ three situations are possible. These situations are discussed in the next few sections.

D.2.1 $\mathbf{b^2 - 4mk > 0}$ - *Overdamped system*

In this case, the response of the system is given by

$$x(t) = C_1 e^{r_1 t} + C_2 e^{r_2 t} \ . \tag{D.23}$$

The response of the above system will be such that the output amplitude of the mass drops rapidly from its initial position. This is a desirable effect in systems that are vulnerable for excessive vibrations.

D.2.2 $\mathbf{b^2 - 4mk = 0}$ - *Critically damped*

In this case, the characteristic equation simplifies to

$$r_1 = -c/2m \ , \tag{D.24}$$

and the response of the system is given by

$$x(t) = (C_1 + C_2 t) e^{-b/2mt} \tag{D.25}$$

This response is similar to overdamped systems with vibrations de-

creasing initially and then increasing slightly before a final decay. This is desirable and as will be shown later, the step response is also well behaved in this case.

D.2.3 $\mathbf{b^2 - 4mk < 0}$, *Underdamped system*

The response of the system in this case is given by

$$x(t) = e^{-\frac{b}{2m}t}\left[C_1 \cos\left(\frac{\sqrt{4mk-b^2}}{2m}t\right) + C_2 \sin\left(\frac{\sqrt{4mk-b^2}}{2m}t\right)\right] . \tag{D.26}$$

The response of the above system has ringing associated with it. Although the amplitude of vibration decays continuously, the mass remains in an oscillatory motion for an indefinite amount of time. This situation is the least desirable as far as mechanical design is concerned and the step response is also equally undesirable.

D.3 Forced Vibrations

The previous section dealt with the initial conditions associated with the inertial mass. Regardless of which position the mass starts at, eventually the displacement will decay to zero. The more interesting case for us is when the accelerometer, in addition to the restoring and damping force, is also undergoing an acceleration force $F(t)$. The acceleration force is what we are interested in determining when using an accelerometer. Making use of Newton's second law once more, we can write

$$m\ddot{x} + b\dot{x} + kx = F(t) . \tag{D.27}$$

The equation above is still a linear second order differential equation but now it is non-homogenous. From basic theory, the solution to the above equation is

$$x(t) = x_c(t) + x_p(t) , \tag{D.28}$$

where $x_c(t)$ is the solution to the homogeneous equation just discussed and called the complementary solution. $x_p(t)$ is the solution to the above equation and is called the particular solution. There are two methods in finding the particular solution: the method of undetermined

coefficients and the method of variation of variables. For our purposes, the method of undetermined coefficients suffices. In this method, we assume a general form for the answer similar to the force being applied to the accelerometer. A common type of external force is a periodic force function

$$F(t) = F_o \cos(\omega t) \ . \tag{D.29}$$

To find the solution, assume that the solution has the general form

$$x_p(t) = A\cos(\omega t)t + B\sin(\omega t) \ . \tag{D.30}$$

Then the first and second derivatives are

$$\dot{x}_p(t) = -A\omega \sin(\omega t) + B\omega \cos(\omega t) \ , \tag{D.31}$$

$$\ddot{x}_p(t) = -A\omega^2 \cos(\omega t) - B\omega^2 \sin(\omega t) \ . \tag{D.32}$$

Substituting into the differential equation we get

$$\begin{aligned} & m\left[-A\omega^2\cos(\omega t) - B\omega^2\sin(\omega t)\right] \\ & + b\left[-A\omega\sin(\omega t) + B\cos(\omega t)\right] \\ & + k\left[A\cos(\omega t) + B\sin(\omega t)\right] = F_o\cos(\omega t) \ . \end{aligned} \tag{D.33}$$

Collecting the like terms we have

$$\begin{aligned} & (-mA\omega^2 + bB\omega + kA)\cos(\omega t) \\ & \quad +(-mB\omega^2 - bA\omega + kB)\sin(\omega t) = F_o\cos(\omega t) \ . \end{aligned} \tag{D.34}$$

And simplifying the above, we achieve the final general solution as

$$x_p(t) \quad = \quad X_P\cos(\omega t + \phi) \ , \tag{D.35}$$

where

$$X_p \quad = \quad \sqrt{A^2 + B^2} \ , \tag{D.36}$$

$$X_p \quad = \quad \sqrt{-\frac{F_o}{m\omega^2 + \frac{b^2\omega^2}{m\omega^2 - k} - k} + \frac{F_o}{m\omega^2 + \frac{b^2\omega^2}{m\omega^2 - k}\frac{b\omega}{m\omega^2 - k}}} \ . \tag{D.37}$$

Similarly, the angle is given by

$$\theta = \arctan\left(-\frac{B}{A}\right), \tag{D.38}$$

$$\theta = \arctan\left(\frac{b\omega}{m\omega^2 - k}\right). \tag{D.39}$$

The above equations will be discussed in the following chapter where open and closed loop dynamics are discussed and a design choice is made between them.

D.4 Accelerometer Modeling for Simulations

Accelerometer modeling is performed in Verilog-a by modeling three external forces. First is the actual input force that causes a displacement as discussed in the analysis above. The basic second order model mass-spring-damper model can be expanded to include more complex modeling of parameters such as damping coefficient as given by Eq. (D.15).

To more realistically model the movement of the plate, two other external forces must also be taken into account: the noise equivalent force of the mechanical accelerometer and the electrostatic forces caused by the voltage on each capacitor plate. These parameters are calculated using a feedback system as shown in Fig. D.5. The three forces are then used to measure a displacement for both the positive and negative capacitor. The capacitors are then updated using the basic non-linear capacitor model given by

$$C_s^{\pm} = \frac{C_s}{1 \pm \frac{x}{d}}, \tag{D.40}$$

where d is the displacement between the capacitors with zero input force, C_s is the nominal capacitance and x is the displacement. Care should be taken to correctly model the change in capacitance in Verilog-a as discussed in [85]. Lumped elements can then be added at external nodes to model parasitic capacitances and line resistances as needed.

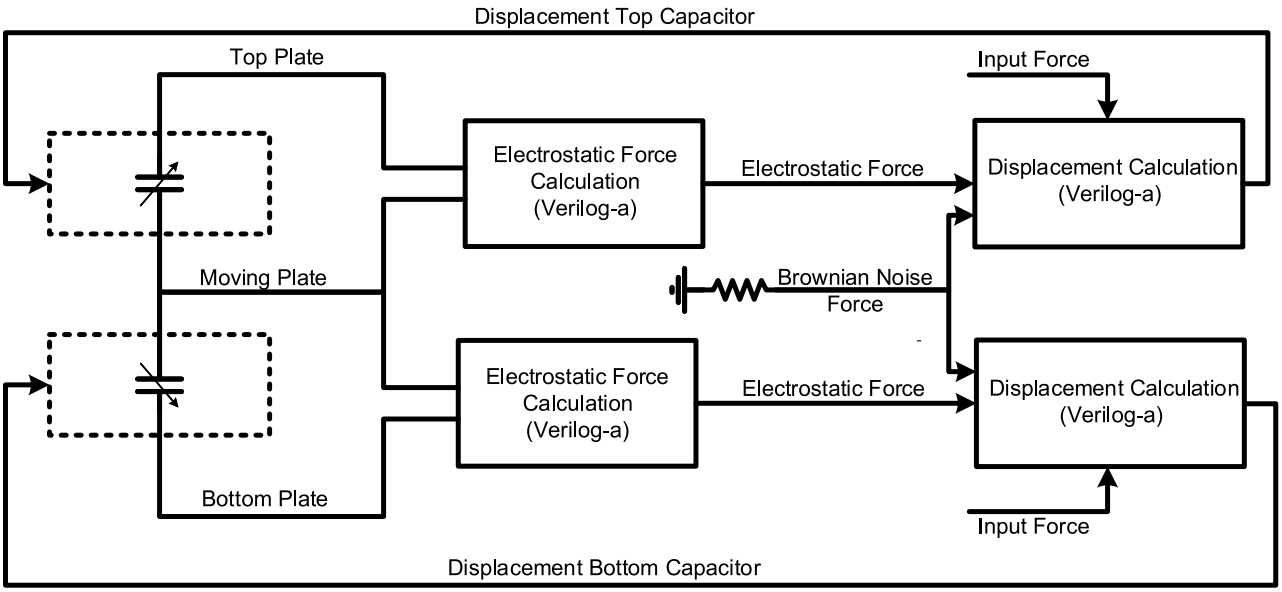


Figure D.5: Verilog-a modeling of an accelerometer including the effect of noise and electrostatic force.

E

System Level Analysis of Open and Closed Loop Systems

In the following sections, using the model developed in the previous section, open loop and closed loop response of accelerometer systems will be discussed.

E.1 Open Loop Systems Analysis

Fig. E.1 shows a capacitive accelerometer system with an interface circuit in open loop. The steady state, frequency and transient response of this system will give insight into design choices.

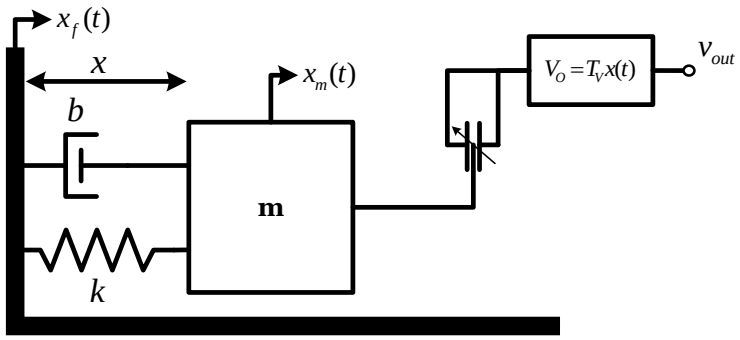


Figure E.1: Block diagram of open loop readout systems

E.1.1 Open Loop Steady State Response

When a constant acceleration is applied to the system, the forces acting on the proof mass will balance and therefore, the mass is stationary with respect to the frame. In other words, $\ddot{x} = \dot{x} = 0$. Using this property, Eq. (D.27) simplifies to

$$\frac{x}{a} = \frac{m}{k} \ . \tag{E.1}$$

Therefore, displacement is proportional to the acceleration and the sensitivity of the system is inversely proportional to the resonant frequency (at DC and low frequencies).

E.1.2 Open Loop Frequency Response

Frequency response is the output when a sinusoid (one frequency tone) is inputted to the system. We have already developed this equation in previous section. The sensitivity in this case can be thought of as the frequency response and is plotted in Fig. E.2. This graph confirms that accelerometers must be operated below the resonant frequency where $x \approx a/\omega_n$.

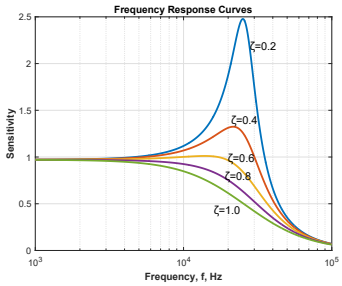


Figure E.2: Frequency response of an open loop system with varying damping factors.

E.1.3 Open Loop Transient Response

For transient response, we make a sudden change in acceleration and see the output response. This is also known as "step response" and given by

$$x(t) = \frac{m}{k} x_f \left[1 - \frac{e^{\zeta \omega_n t}}{\sqrt{1-\zeta^2}} \sin\left(\sqrt{1-\zeta^2}\omega t + \phi \right) \right] \ . \tag{E.2}$$

The transient response based on the equation above is shown in Fig. E.3. Notice that as discussed previously, to avoid overshoot requires a damping factor of below 0.5.

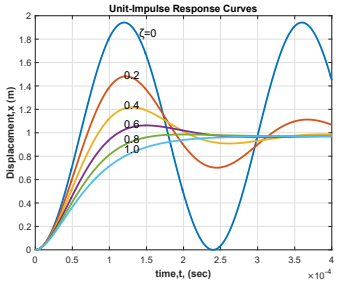


Figure E.3: Step response of an open loop system with varying damping factors.

E.2 Closed Loop Systems Analysis

Fig. E.4 shows a closed loop system. The system has a feedforward stage and a feedback stage. The feedforward stage is the same as one

explained in previous section for the open loop system, where T_v is a product of the accelerometer sensitivity and the electronic gain.

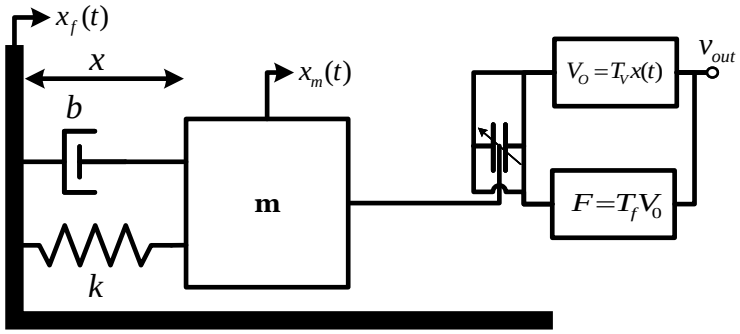


Figure E.4: Block diagram of closed loop readout systems

Due to feedback, the proof mass is virtually stationary in closed loop systems. The output is now proportional to the feedback signal rather than the proof mass displacement as in an open loop design. In IC's, electrostatic forces are used for restoring the movement of the capacitive plate but there is two problems: the force is none-linear and is always attractive. There are many solutions to overcome this, including the use of pulse width modulation and pulse density modulation (PDM). PDM feedback systems are the most common and in this case, the closed loop system is in effect a delta sigma modulator with the sensor element being part of the loop.

E.2.1 Closed Loop Steady State Response

As before, $\ddot{x} = \dot{x} = 0$ in steady state and the equation for output simplifies. However, unlike before, the system now includes the feedback force which is ideally dependent on electronic components only according to

$$ma = kx + T_f V_o \ , \tag{E.3}$$

where T_f is the gain of the feedback path. Electrical feedback force is often much larger than the mechanical restoring force. As such, the

above equation simplifies to

$$V_o = \frac{m}{T_f} a \ . \tag{E.4}$$

Therefore, this equation shows that the output voltage is independent of the forward path gain and is inversely dependent on the feedback gain. Therefore, the steady-state response is independent of the displacement of the proof mass which is beneficial as proof mass displacement can exhibit non-linearity.

E.2.2 Closed Loop Dynamic Response

The equation of motion for forced feedback systems is very similar to open loop systems. We can write the governing equation as

$$m\ddot{x}_m + b\dot{x} + kx = -\alpha x - \beta\dot{x} \ , \tag{E.5}$$

where $\alpha = T_v \times T_f$, the electrical feedback force per unit of displacement (N/m) and is often called the *electrical spring*. $\beta = T_v \times \gamma$ is the electrical damping force per unit speed (N/(m/s)) and often called the *electrical damper*.
Rearranging the above we get

$$\ddot{x} + \frac{b+\beta}{m}\dot{x} + \frac{k+\alpha}{m}x = -\ddot{x}_f \ , \tag{E.6}$$

Eq. (E.6) can be written in standard form as

$$\ddot{x} + 2\zeta_c\omega_{nc}\dot{x} + \omega_{nc}^2 x = -\ddot{x}_f \ , \tag{E.7}$$

where ζ_c and ω_{nc} are the damping coefficient and natural frequency of the *closed loop* system and given by

$$\omega_{nc} = \sqrt{\frac{k+\alpha}{m}} \ , \tag{E.8}$$

$$\begin{aligned} \zeta_c &= \frac{(b+\beta)}{(2m\omega_n)} \\ &\approx \frac{\beta}{2m\omega_n} \end{aligned} \tag{E.9}$$

These equations show that the closed loop transient response takes the same form as the open loop response with the above adjusted natural frequency and damping factor. As such, closed loop equations are very similar to the open loop case and the graphs of sensitivity are similar to those shown in the previous section. The difference is that the closed loop system's characteristics are now dominated by the electronic components which are often better controlled and more easily changed. This gives force feedback systems a robustness that has garnered much interest in this area. However, the merits of closed loop systems compared to their open loop counterparts is more involved than this simple observation. A more rigorous comparison is made in the next section.

E.3 Comparison of Closed Loop and Open Loop Systems

Both open and closed loop systems can be modeled as second order systems as the analysis in the previous section has shown. The key difference lies on the components that make up the sensitivity, bandwidth and linearity of the system. In open loop systems, these components are mechanical whereas in closed loop systems these are determined by the electrical feedback components. Therefore, as a first pass, closed loop systems appear to be more robust compared to open loop systems.

However, the comparison of these systems highly depends on the application they are intended for. When applications are taken into account, the advantages that closed loop systems have begins to falter and open loops system become a better choice. To demonstrate this, various design parameters for both open and closed loop systems are discussed separately in the following sections.

E.3.1 Noise and Dynamic range

Perhaps the biggest drawback to force feedback systems is the mechanical noise of accelerometers. Both force feedback and open loop systems' noise limit is the orthogonal combination of the mechanical noise and the electronic noise. This in turn puts limits on the usefulness of closed loop systems. Literature review in this area indicates that many force

feedback accelerometers rely on custom made bulk micromachined accelerometers with large masses to bring the mechanical noise low enough for force feedback to be useful. Therefore, although 120 dB dynamic range systems have been reported [32], these systems require custom made large mass accelerometers driving up costs (Fig E.5).

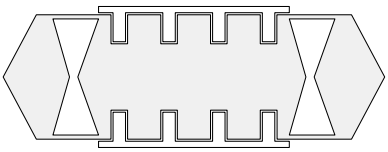


Figure E.5: Cross sectional view of a bulk micromachined accelerometer. Low noise design are limited by the mechanical thermal noise of the accelerometer and require custom made accelerometers driving up costs.

E.3.2 Damping

Apart from the mechanical suspension, open loop systems will also suffer from other mechanical issues. Damping in accelerometers is generally achieved with squeeze film damping and this is a function of the gas pressure. As it can be imagined, gas damping is non-linear and highly dependent on environmental and temperature variations. In closed loop systems, damping can be made to be a function of the electronics.

Damping non-linearity, however, becomes an issue at large accelerations which cause large displacements. For most applications, displacement is a fraction of the intended design of the mechanical sensor, making displacement non-linearity moot.

E.3.3 Flexibility

Flexibility of closed loop systems can be changed by using variable gains in the feedback path. Traditionally, open loop systems were designed for a specific accelerometer. The proposed system tries to mitigate this effect.

E.3.4 Bandwidth

The bandwidth of open loop systems is set by the mechanical components. In contrast, closed loop systems' bandwidth can be changed based on the electronics which can have higher frequency ranges. However, many applications for accelerometers have low bandwidth requirements [86] and this limitation of open loop systems may not be a limiting factor in choosing closed loop systems.

E.3.5 Stability and Complexity

Since closed loop systems include the second order mechanical accelerometer with the electronics in a closed loop, additional poles and zeros are encountered causing stability issues. Moreover, characterization of these poles and zeros is difficult. Open loop systems generally do not have this issue. Accordingly, force feedback systems are more complex requiring additional circuitry to monitor and stabilize the performance of the loop.

E.3.6 Power Consumption

The final and the biggest drawback of closed loop systems is their high power consumption. The necessity to continuously mitigate the force of acceleration[1] as well as additional circuitry needed for these systems makes their power consumption an order of magnitude higher than their open loop counterparts. This is a large drawback, especially for consumer applications such as smartphones where accelerometers are used for many functionalities and battery life is a factor in marketing.

[1] requiring charging and discharging of large capacitors

E.4 Conclusion

A rigorous analysis of of open and closed loop systems shows that the benefits of closed loop are very application specific. A closed loop system's main benefit is to limit the movement of the proof mass in theory to zero. As such, the linearity is no longer a function of the spring constant of the mass (as it is with open loop systems) but the electronic feedback components. Many application however require very little movement. Looking at the datasheets of available commercial accelerometers, accelerometers often operate in a range of several g's, for example ± 2 g, ± 4 g or ± 16 g but applications such as train hopping, or smart phone applications require force measurement of less than 1 g and often below 0.1 g. Therefore, the benefits of closed loop or force feedback systems only manifest themselves if an application that operates at full range of the accelerometer exists. For many applications, this is not the case and an open loop system's mechanical linearity may not be the limiting factor.

Furthermore, mechanical noise often limits the achievable fidelity of

systems. This in turn makes force feedback systems either moot or requiring large expensive bulk micromachined accelerometers. Finally, power consumption of force feedback systems is well above open loop systems making them ill-affordable for large volume consumer applications.

Therefore, open loop systems offer more incentives for commercial production. The work presented aims to break the tradeoffs of these systems compared to their closed loop counterparts by making them flexible (variable gain) and improve their linearity (harmonic reduction) without increasing power consumption or complexity.

F

Accelerometer Interfacing Options

F.1 Interfacing Types

Depending on the type of accelerometers being used, there are several methods for interfacing. We focus specifically on differential accelerometers consisting of a movable proof mass and a set of fixed electrodes. The simplest type of interfacing is known as the half bridge structure as shown in Fig. F.1.

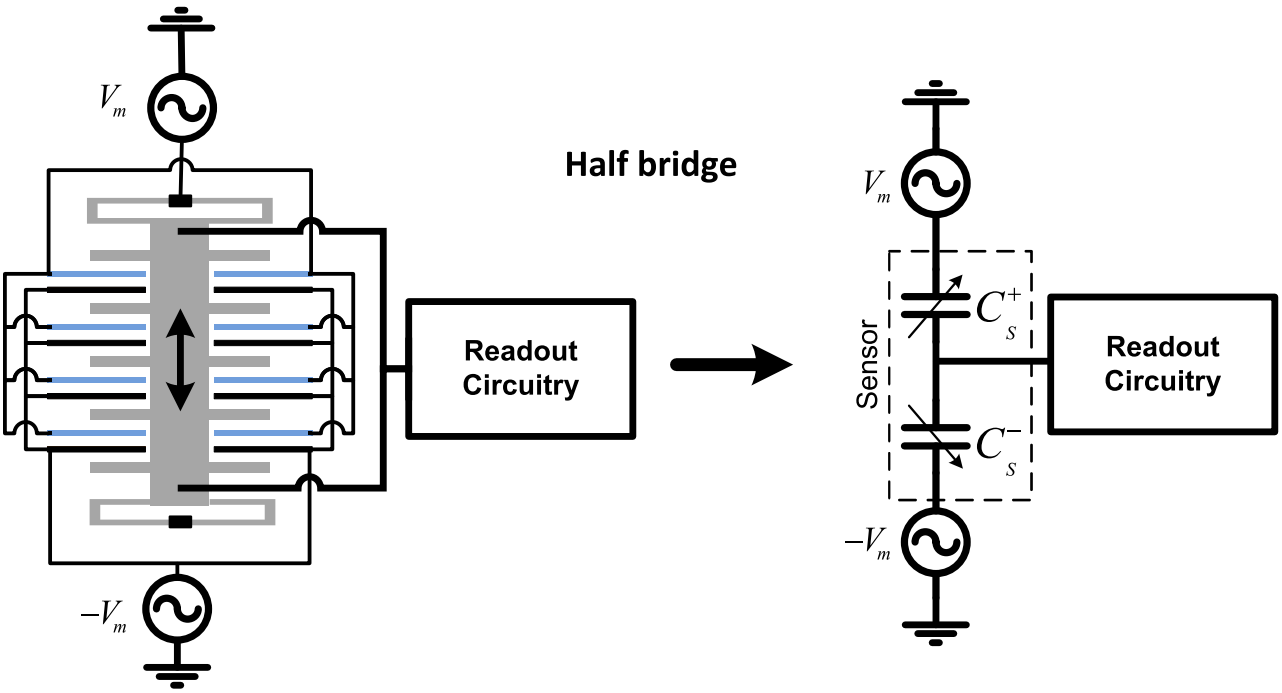


Figure F.1: Half bridge interfacing with a differential accelerometer by driving the static plates. Note that the output of this structure is single-ended and techniques are needed to transform the signal to differential.

In this implementation, the fixed electrodes shown by the blue and

orange metal layers on the left hand side are connected to a modulating signal. For simplicity, the modulation signal is a sinusoidal signal for analog implementation but can be changed to a switching network if a switched capacitor readout scheme is being used. This structure, although popular, can only lead to single-ended outputs and therefore techniques are required to make the output differential [87].

To make the system differential or a full bridge, several techniques can be used. One method would require access to a differential accelerometer with two sets of sense capacitors [88] [89]. A generic version of this setup is shown in Fig. F.2.

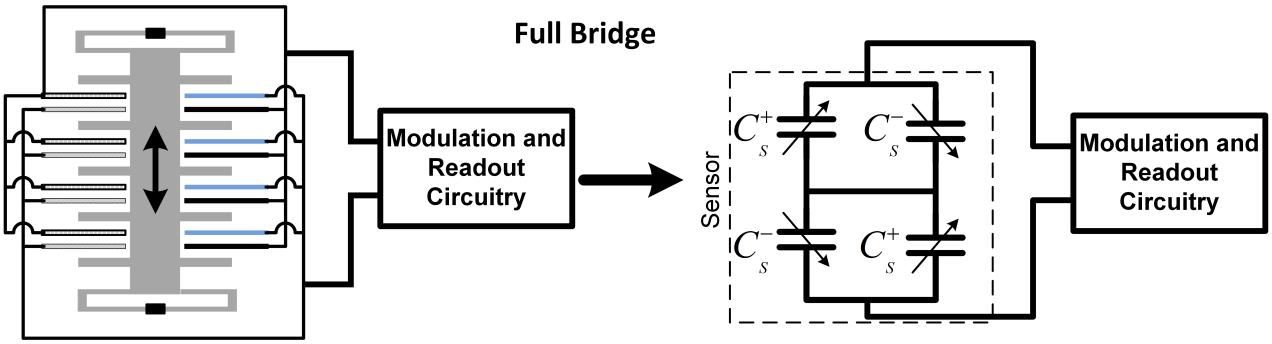


Figure F.2: Full bridge interfacing with a dual differential accelerometer.

This structure is robust, but we often do not have access to a differential accelerometer with two sets of sense capacitors.

Another option that is often used to create a full bridge structure is to employ a set of fixed capacitors along with the sense capacitors to create what is known as a pseudo full bridge [90] as shown in Fig. F.3. One issue with this structure is that the reference capacitors must be very close to the sense capacitors (at rest) which often requires the use of programmable reference capacitors, adding to circuit complexity.

A final approach is to use the middle electrode of the accelerometer to drive the capacitive sensors and use the other electrodes as the differential outputs. The issue with this setup is that the input common mode is not well defined and any mismatch can cause the output to saturate to the rails [30]. This in turn requires the use of a common mode feedback structure, adding to complexity and power consumption of the design [25].

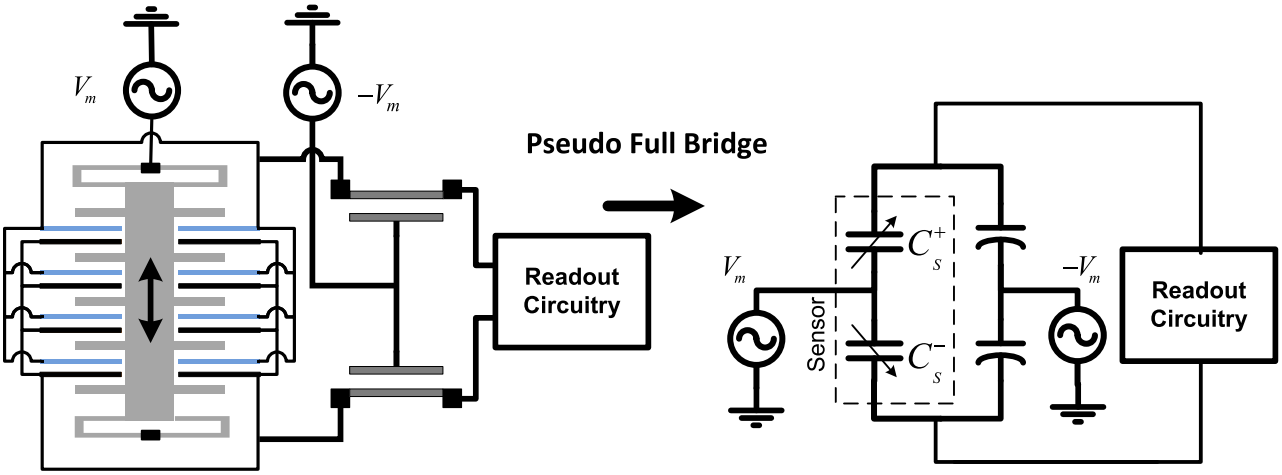


Figure F.3: Pseudo full bridge interfacing with a differential accelerometer. This setup requires reference capacitors that are fairly close to the sense capacitors.

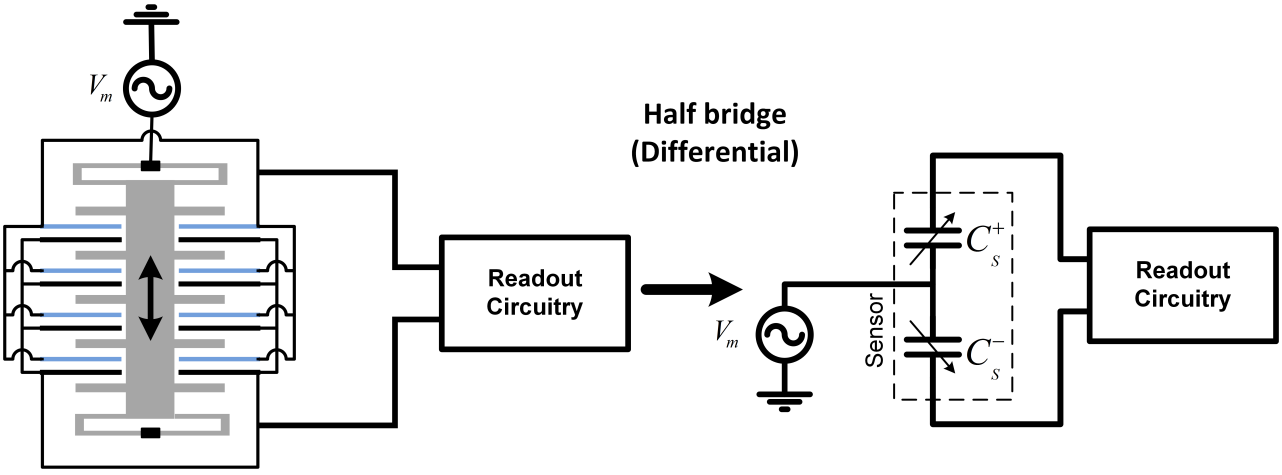


Figure F.4: Half bridge interfacing with a differential accelerometer by driving the moving plate. This setup can achieve differential output but requires a common mode feedback circuit to define the input common mode voltage.

F.2 Conclusion

When it comes to interfacing with a differential accelerometer, there are several choices. All structures have shortcomings that require additional circuitry which adds to the complexity and power consumption of the system. The choice then generally comes down to more practical issues such as the type of readout circuitry that has been used (charge, current or voltage based).

G

PCB Design

This Appendix gives a general overview of the PCB design and method of generating bias voltages, currents, control signals and clocks for testing purposes.

G.1 System Level Design

The block level design of the PCB is shown below. Each of these blocks are explained in Table G.1

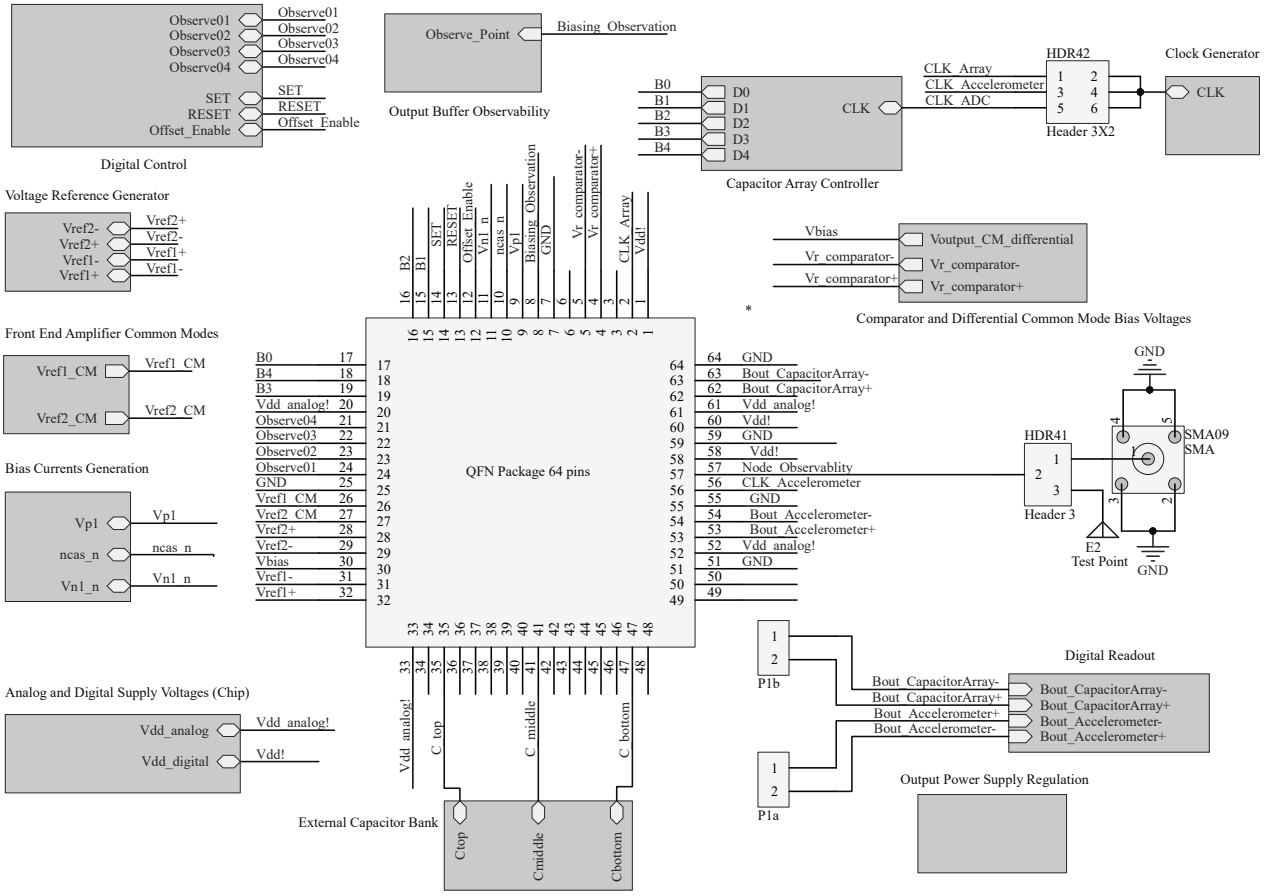


Figure G.1: System level block diagram of the PCB board. Implemented PCB is shown in Fig. I.9

G.1.1 Description of System Blocks

The following is the list of blocks and their description. Each bock is further explained in the following sections.

PCB Block Diagram		
#	Block Name	Functionality Description
1	QFN Package	Contains the fabricated chip with (see Fig. I.4) and without MEMS (see Fig. I.5) accelerometer
2	Digital Control	Contains a switches to set controllability values
3	Output Buffer Observability	Uses a unity gain buffer to view various nodes on the circuit
4	Capacitor Array Controller	Uses an ADC to convert a sinusoid signal into a parallel bitstream to mimic accelerometer movement through the on-chip capacitor array
5	Clock Generator	Contains several clock options for clocking the test chip as well as other parts.
6	Comparator Voltages	Voltages for the on-chip comparator achieved through a bandgap reference and unity gain buffer.
7	Digital Readout	Connection to NI instruments data acquisition box.
8	Power Supply Regulation	Contain several power options including battery and wall outlet, converted to appropriate levels using a regulator
9	External Capacitor Bank	A set of capacitors used for DC and AC testing of accelerometer
10	Analog/Digital Power Supply	Block that generates the analog power and the digital power for the test circuit. Makes use of a regulator with bypass capacitor for low noise.
11	Bias Current Generation	Generates the currents for on-chip current mirrors using a bandgap reference and a variable resistor.
12	Front End Amplifier Common Modes	Generates common mode signals $V_{ref1,CM}$ and $V_{ref2,CM}$ for the front end amplifiers used in the DAC and charge-to-voltage converter.
13	Voltage reference generator	Generates voltages $+V_{ref1}$,$-V_{ref1}$, $+V_{ref2}$ and $-V_{ref2}$.

Table G.1: Block level descriptions of the PCB board, see Fig. G.1

G.2 Clock Generation

Clock generation relied on three techniques to generate the clock signal for the ASIC as well as the on board peripherals. This included an external clock generator connected through an SMA, a daughter board clock generator, as well as a clock from the FPGA board used for data capture.

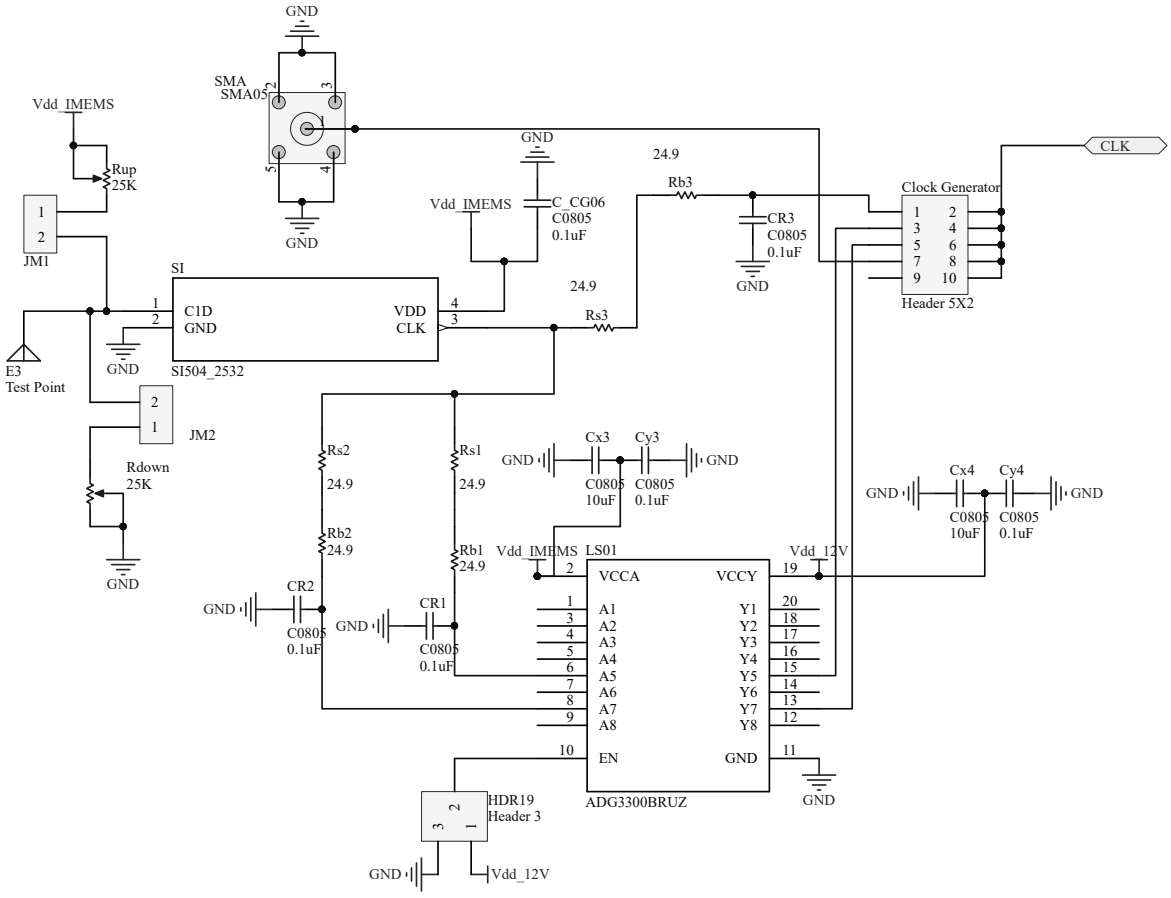


Figure G.2: Schematic of clock generation

G.2.1 External Clock Generation

G.2.2 CMEMS Clock Generation

For testing the ADC functional as a standalone accelerometer, a method was needed to generate the clock signal without the use of an external power supply. This was to avoid the wires that can impede the movement

External Clock Generation				
Component	Function	Specification	Manufacturer	Part Number
CLK	External Clock	$0 - 15$ MHz	Hewlett Packard	33120A

Table G.2: External clock generation specifications

of the sensor. For this purpose, a MEMS based PLL was used with power supply.

Battery Operated MEMS based PLL				
Component	Function	Specification	Manufacturer	Part Number
LDO	On-chip Clock	1.8 V, LVCMOS	Silicon Labs	SI504
LS01	Level Shifter	$1.8 - 1.2$ V, LVCMOS	Analog Devices	ADG3300

Table G.3: CMEMS PLL used for generating clock signals.

G.2.3 FPGA Based Clock Generation

The FPGA used to capture data readout also allowed an external clock to be used.

Battery Operated FPGA based Clock				
Component	Function	Specification	Manufacturer	Part Number
FPGA	FPGA	Spartan-6	Opal Kelly	XEM6310
CLOCK	FPGA clock	$0.5 - 300$ MHZ, LVCMOS	Opal Kelly	–

Table G.4: Opal Kelly FPGA board specifications

G.3 Power Supply Generation

Often in high performance analog circuits, noise from power supplies, above all other sources, is the limiting factor in fidelity. As this design relied on a highly linear output, special care must be taken in power supply generation.

G.3.1 Input Power Supply

To begin, the digital and analog power supplies were separated to limit disturbances from clock spikes in affecting critical circuits. The power supply generates two five volt supplies, one for the digital blocks and one for the analog blocks.

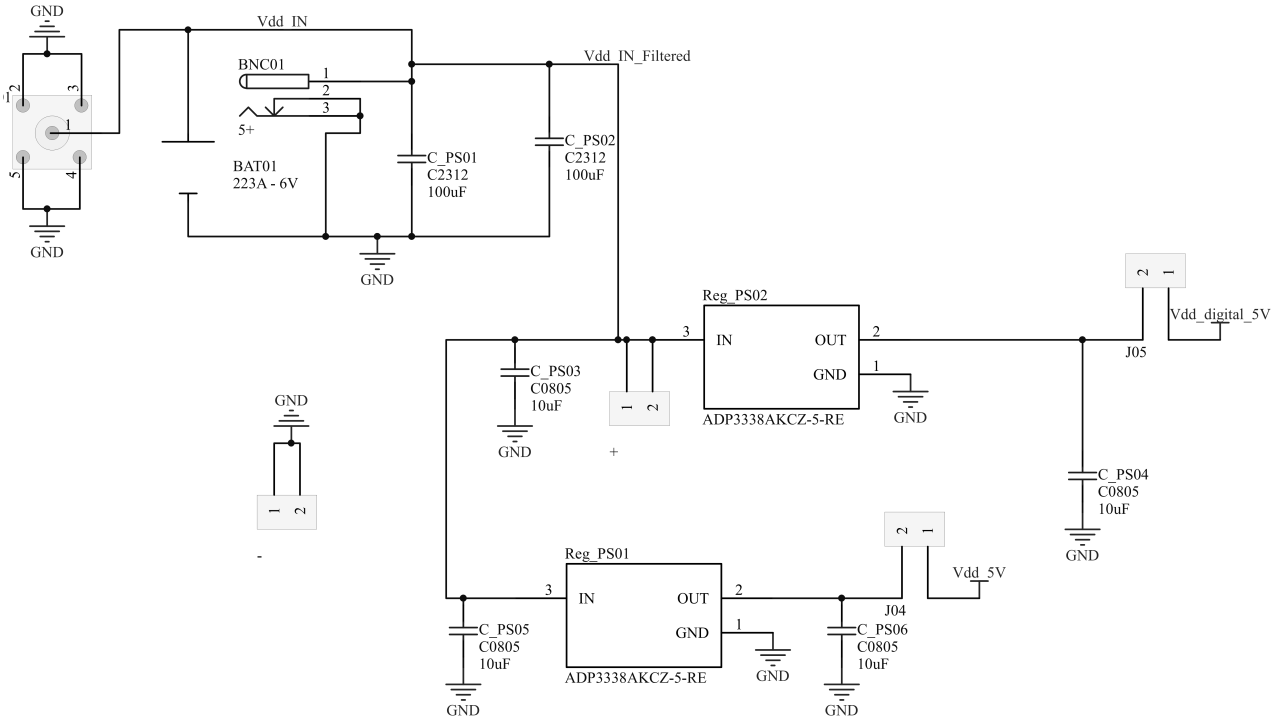


Figure G.3: Schematic of power supply generation

Input Power Supply Components				
Component	Function	Specification	Manufacturer	Part Number
LDO	Power supply	5.0 V, LVCMOS	Analog Devices	ADP3338
Capacitor	Bypass, filtering	X5R, 10 μF	Daeong	–
Capacitor	Bypass, filtering	Titanium, 100 μF	–	–

Table G.5: Power supply components

G.3.2 Analog and Digital Power

Each 5 volt power supply was then used to supply a linear dropout regulator to generate the 1.2 V power supply for the ASIC. The output of the regulator was heavily filtered with capacitors of a decade apart to cover a broad frequency spectrum[1].

[1] In general, larger capacitors have poor performance at high frequencies

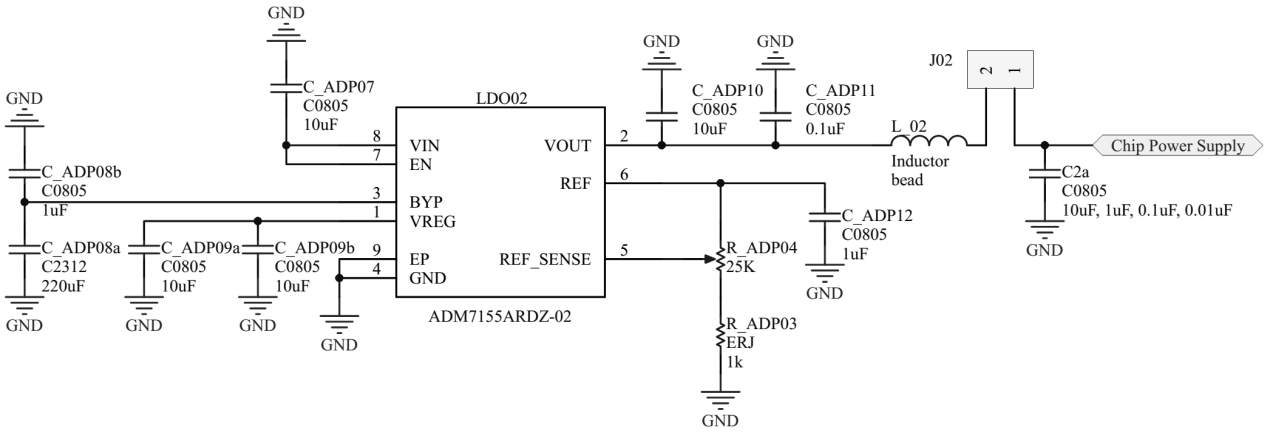


Figure G.4: Schematic of analog and digital power supply generation

Analog and Digital Power Supply				
Component	Function	Specification	Manufacturer	Part Number
LDO	Power supply	1.2 V, LVCMOS	Analog Devices	ADM7155
Capacitor	Bypass, filtering	X5R, 10, 0.1 μF	Daeong	–
Capacitor	Bypass, filtering	Titanium, 220 μF	–	–

Table G.6: On-chip power supply generation components

G.4 Reference Voltage Generation

In ADC testing, reference voltage are limiting factors as noise in these sources directly couples to the output[2]. The general approach to creating these sensitive voltages was to use an ultra low noise band gap reference followed by a unity gain buffer for adequate current drive capability.

[2] In other words, there is no noise shaping or noise transfer function is one

G.4.1 DC Reference Voltage Generation

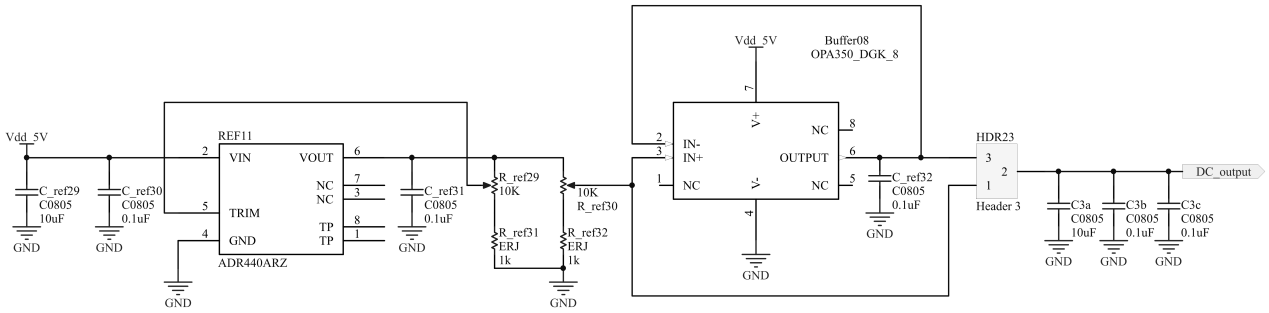


Figure G.5: Schematic of DC signal generation

DC Reference Voltage Generation

Component	Function	Specification	Manufacturer	Part Number
Amplifier	Unity Gain Buffer	3.3 V, LVCMOS	Texas Instruments	OPA350
Bandgap Reference	Fixed voltage	2.048 ± 3 mV , $1\mu V^2/Hz$	Analog Devices	ADR440

Table G.7: Component specifications for DC voltage generation

G.4.2 AC Signal Generator

In certain tests, the references are used as input signals and the ASIC used as a conventional ADC. Driving ADC inputs has several challenges and requires the use of an ADC driver [91]. The schematic of the setup with the driver is shown below.

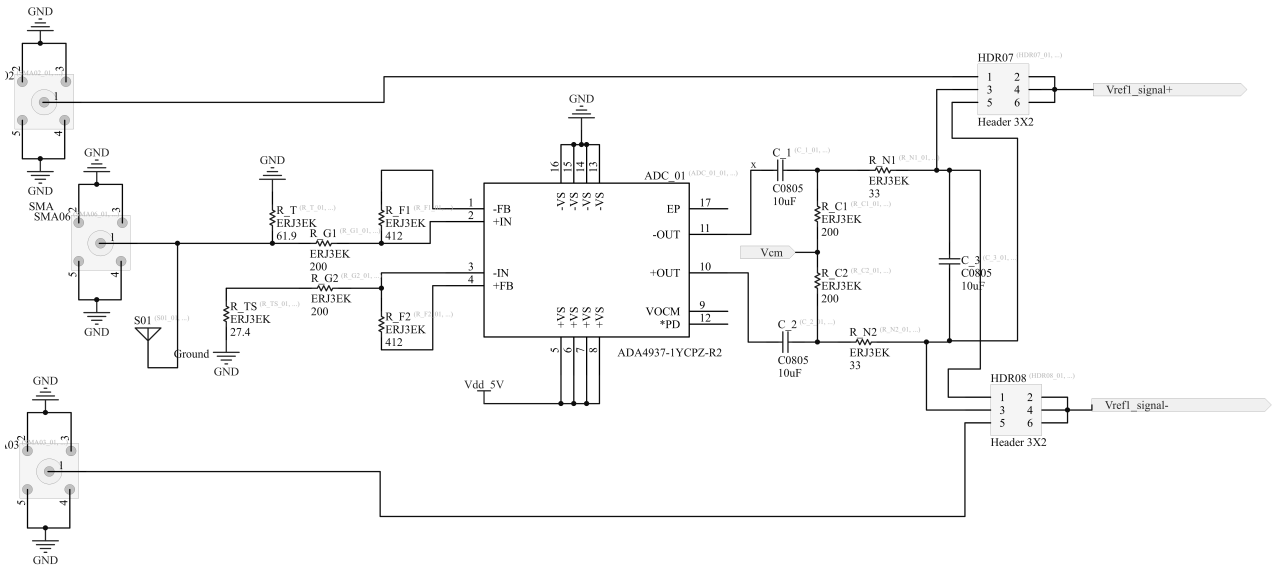


Figure G.6: Schematic of AC signal generation

ADC Driver				
Component	Function	Specification	Manufacturer	Part Number
ADC01	ADC driver	ultra low noise	Analog Devices	ADA4937

Table G.8: Component specification for the ADC driver.

G.5 Bias Currents

The bias currents are again a limiting factor in fidelity. Noise in the current generated can directly couple to the input stages of op-amps and couple through to the output. Special care must be taken to ensure noise in these circuits is below the intended design. Bias currents for the chip were designed with an ultra-low noise bandgap reference and an adjustable potentiometer as shown in Fig. G.7.

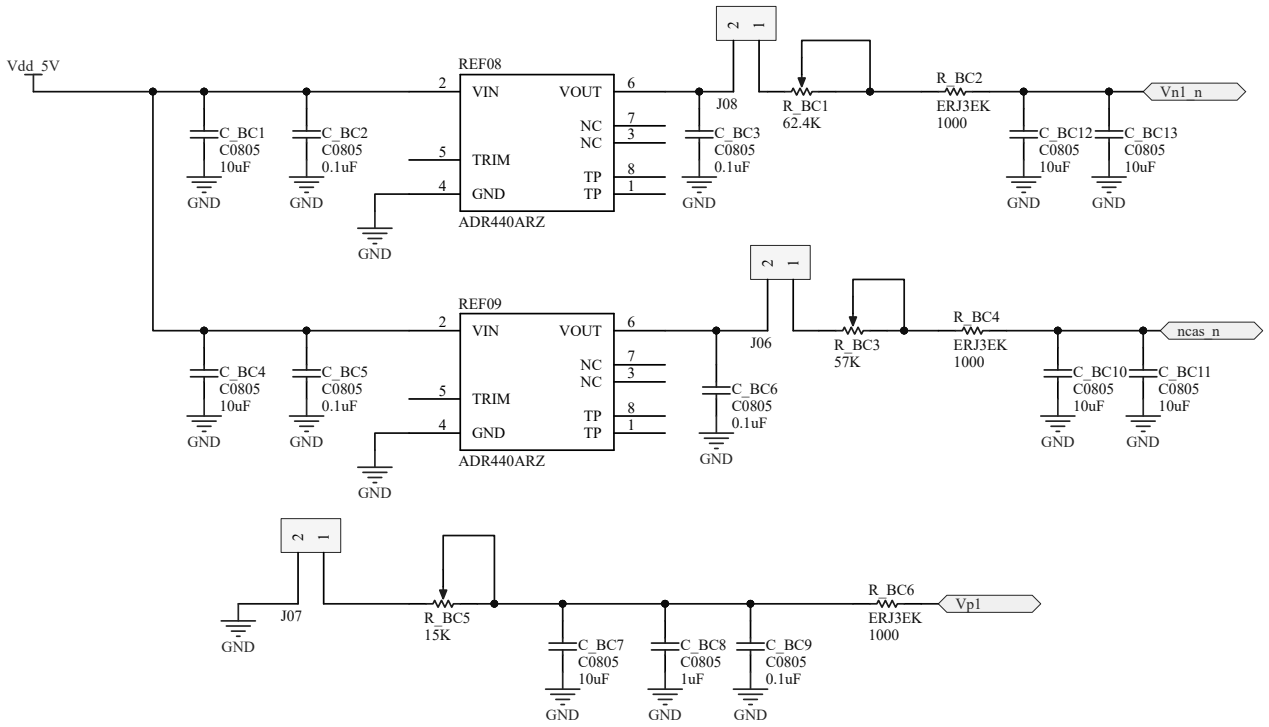


Figure G.7: Schematic of bias current generation

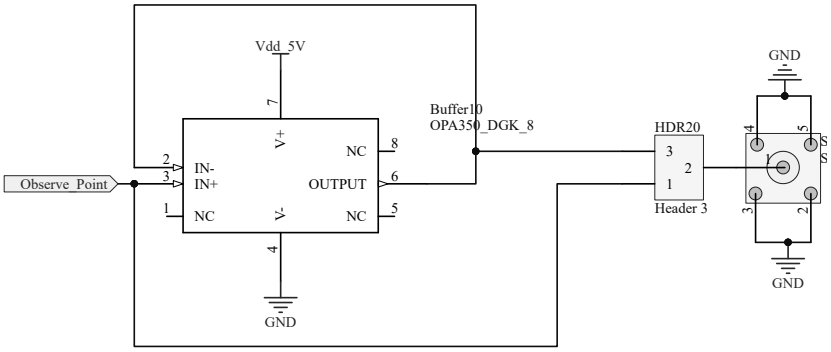
Bias Current Generation				
Component	Function	Specification	Manufacturer	Part Number
Bandgap Reference	Fixed voltage	2.048 ± 3 mV , 1 $\mu V^2/Hz$	Analog Devices	ADR440

Table G.9: Component specifications for DC bias currents generation.

G.6 Output Buffer

For debugging purposes, certain on-chip signals were observed using a unity buffer.

Figure G.8: Schematic of output buffer



Output Buffer				
Component	Function	Specification	Manufacturer	Part Number
Amplifier	Unity Gain Buffer	3.3 V, LVCMOS	Texas Instruments	OPA350

Table G.10: Component specifications for buffer stage

G.7 Capacitive Array Controller

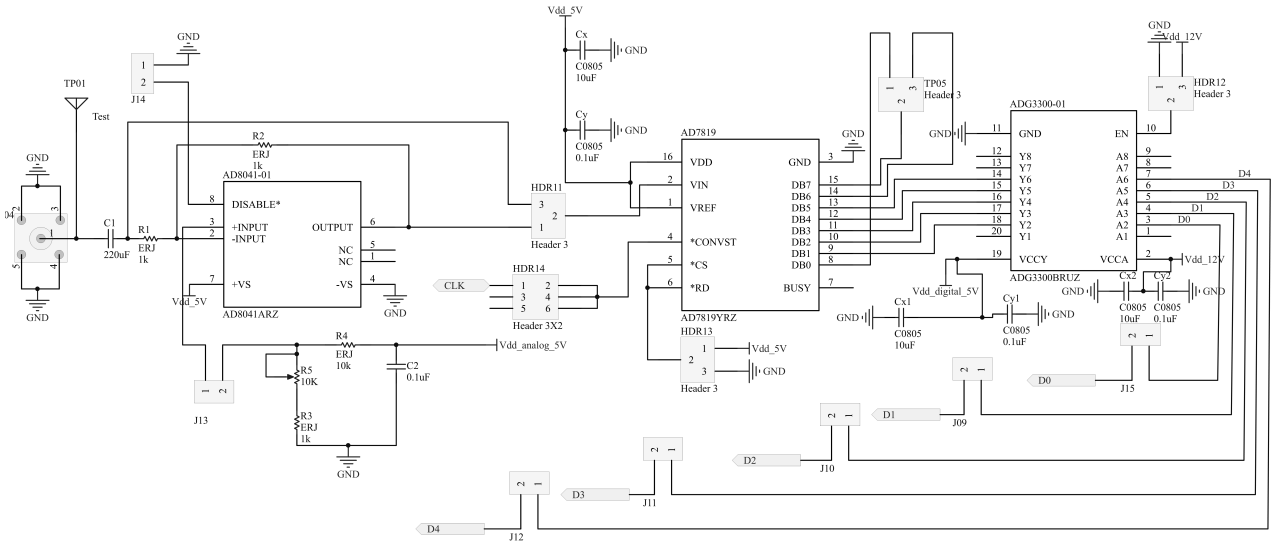


Figure G.9: Schematic of capacitive array controller

Capacitive Array Controller				
Component	Function	Specification	Manufacturer	Part Number
AD8041	Amplifier Gain stage	3.3 V, LVCMOS	Analog Devices	AD8041
AD7819	ADC Converter	5V, LVCMOS	Analog Devices	AD7819
ADG3301	Level Shifter	$5 - 1.2$ V, LVCMOS	Analog Devices	ADG3301

Table G.11: Component specifications for the capacitive array controller

G.8 Digital Readout

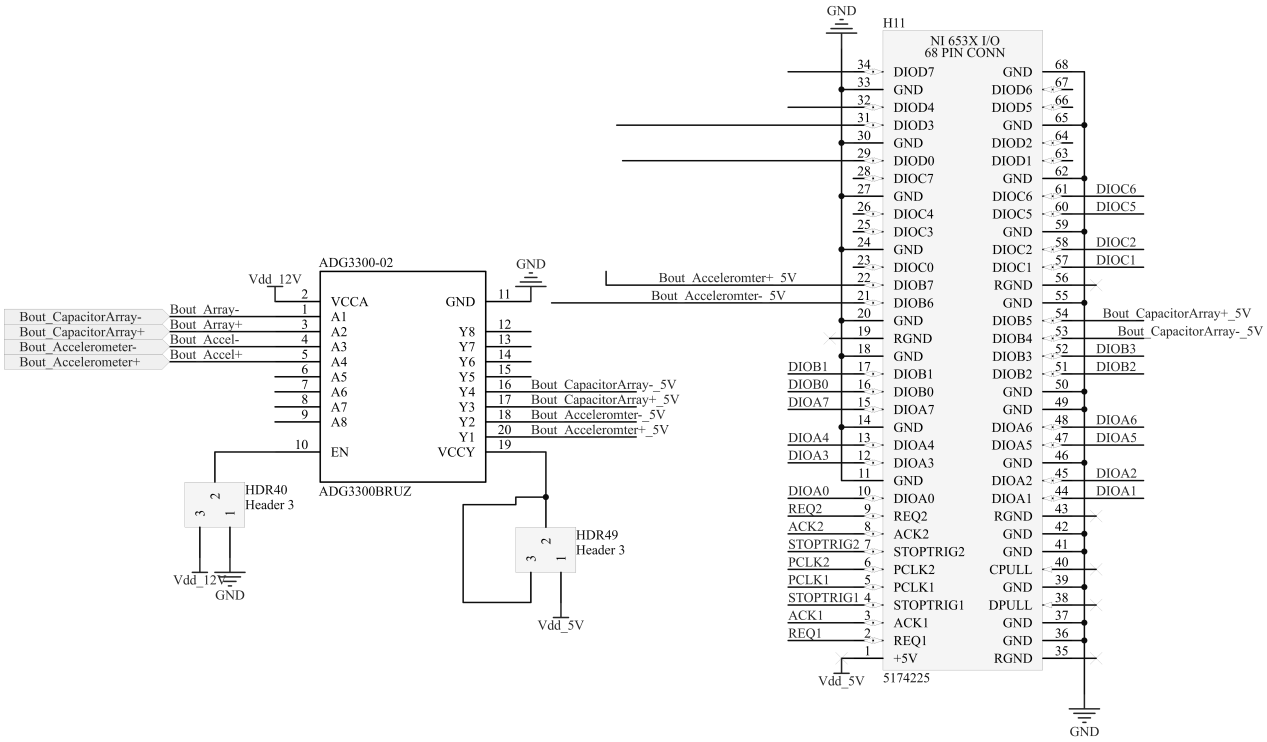


Figure G.10: Schematic of digital readout

Digital Readout				
Component	Function	Specification	Manufacturer	Part Number
H11	Digital Pin Readout		Tyco	ADR440
ADG3300	Level Shifter	1.2 V $\rightarrow$ 5.0 V	Analog Devices	ADG3300BRUZ

Table G.12: Component specifications for digital readout

G.9 Digital Control

Digital control uses a switch to turn on signals for flip flops as well as the capacitor offset network.

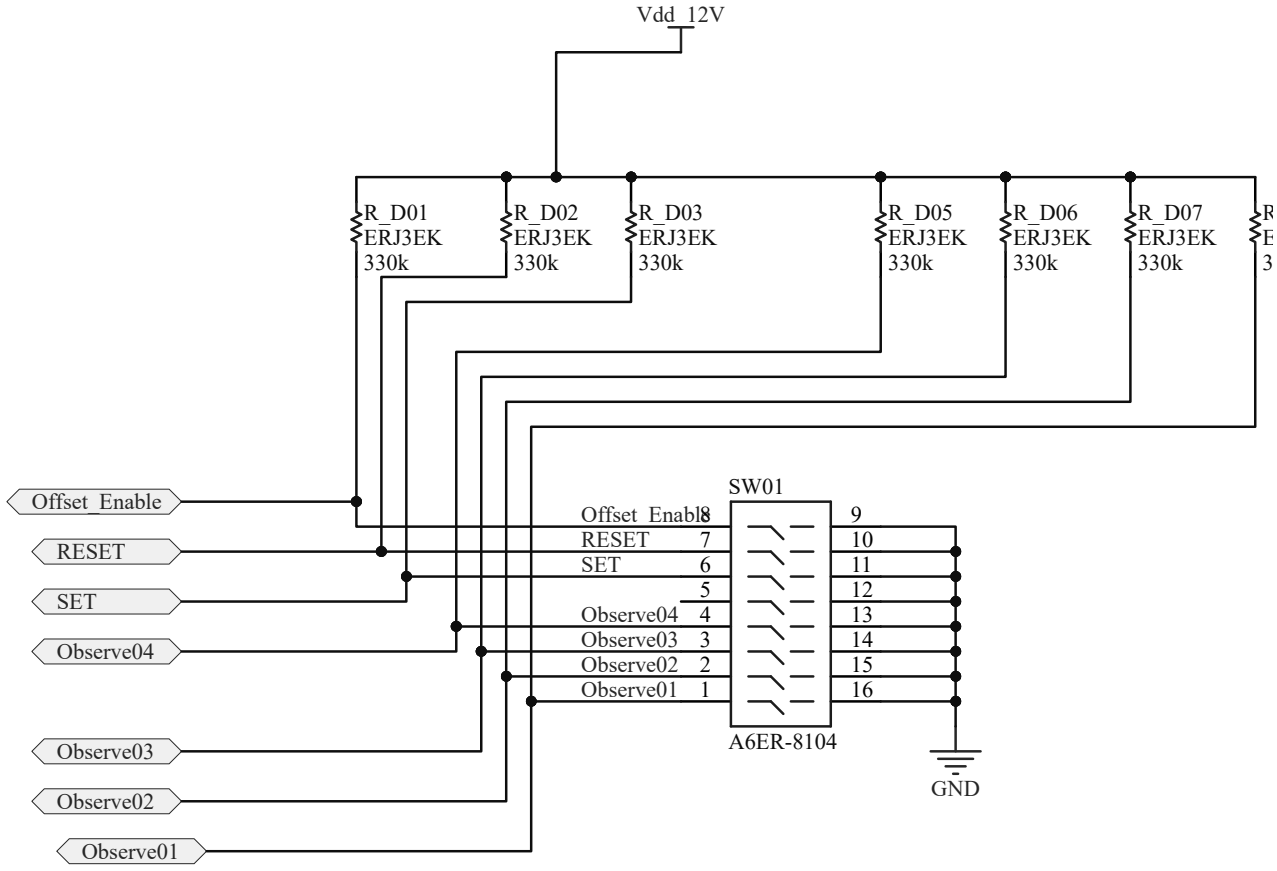


Figure G.11: Schematic of digital control generation

Digital Control				
Component	Function	Specification	Manufacturer	Part Number
SW01	Mechanical Switch	–	Juju	A6ER-81601

Table G.13: Component specifications for digital control generation

G.10 External Capacitor Bank

The external capacitor bank is used to place fixed capacitors as inputs for the accelerometer. These are used in functionality testing of the ADC.

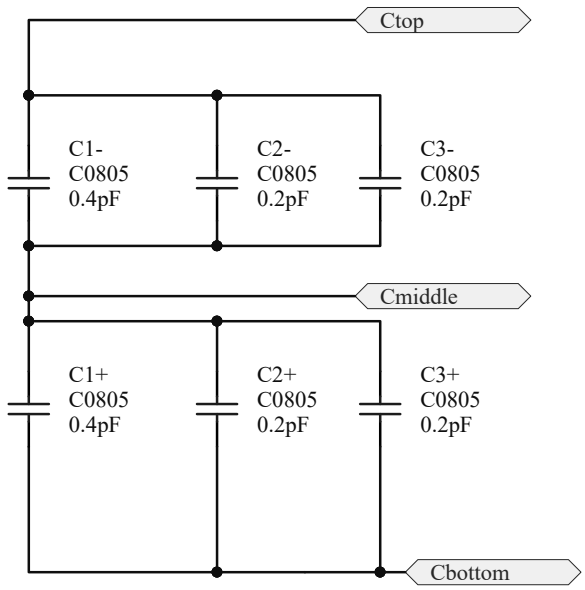


Figure G.12: Schematic of external capacitor bank

H

Step Motor Dynamics and Programming

Accelerometers are generally tested using rate tables. As these equipment can run into the tens of thousands of dollars in cost, a lower cost option was implemented using a step motor. Table H.1 shows the programming steps for the motor to generate a sinusoidal displacement that in turn leads to a sinusoidal velocity and acceleration.

Zeta 6104 motor code		
#	Code snippet	Description
1	COMEXC1	Continue command processing during motion
2	D50000	Establish desired bottom of oscillation
3	MC1	Put axis into preset move mode
4	GO1	Move axis to desired centre location
5	FOLMAS16	Axis 1 follows sine 1
6	FOLRN1	Set master slave ratio to 1:1
7	FOLRD1	Return ratio
8	FOLEN1	Put axis into following mode
9	MC1	Put axis into continuous mode
10	SINAMP8096	Establish center to peak amplitudes
11	FVMFRQ3600	Establish frequency, start small and build up to reduce strain on motor
12	@FVMACC999999	Reach frequencies rapidly
13	SINANG270	Start angles at bottom of cycle
14	GO1	Lock slaves to master (not started yet)
15	SINGO1	Start sine waves (and hence slave motion)

Table H.1: Coding example to generate a sinusoidal movement which will in turn create sinusoidal velocity and acceleration.

I

Pictures and Micrographs

This Appendix provides pictures and/or micrographs of various circuits and ASICs used in testing.

I.1 IC Prototype Micrographs

Prototyping was done with IBM 0.13 μm technology. A photodie of this is shown in I.1.

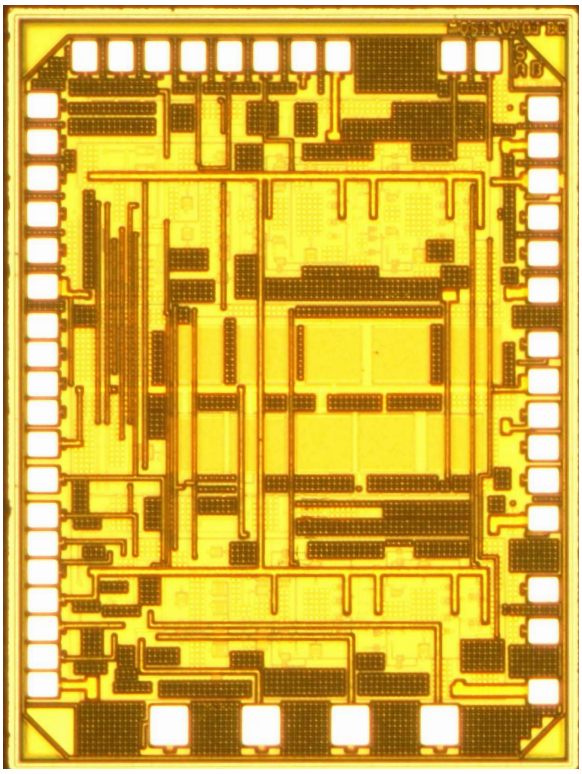


Figure I.1: Loose die photo of fabricated chip in IBM 0.13 μm

There are two distinct set of circuits implemented in the IC. In the top half, the system uses a capacitor array for its input while the bottom half connects to an external accelerometer. The capacitor array is meant to mimic an accelerometer as well as to cancel parasitic capacitances for the accelerometer system.

I.2 Packaging

I.2.1 QFP Package

Some dies were bonded using a QFP80 pin package from Kyocera[1].

[1] This package is now obsolete

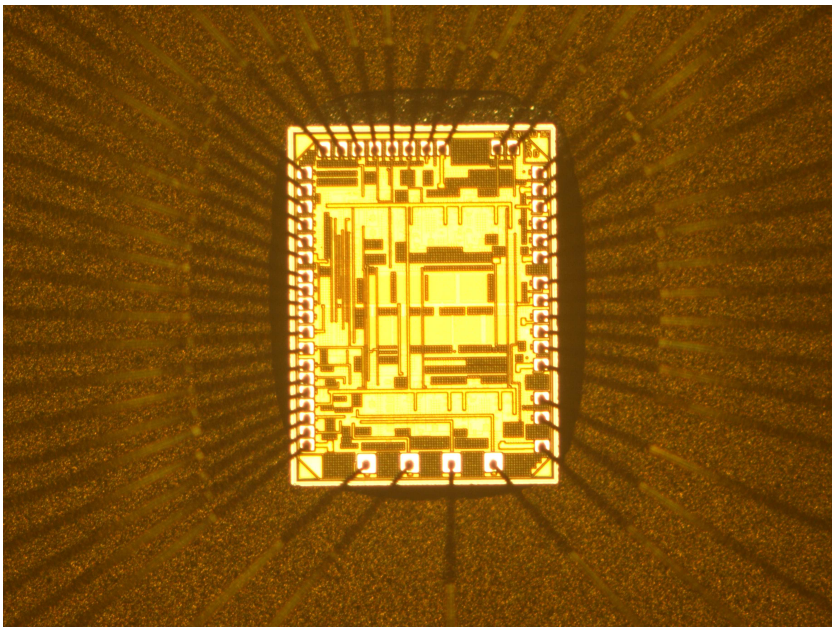


Figure I.2: Die photo in Kyocera 80 pin package.

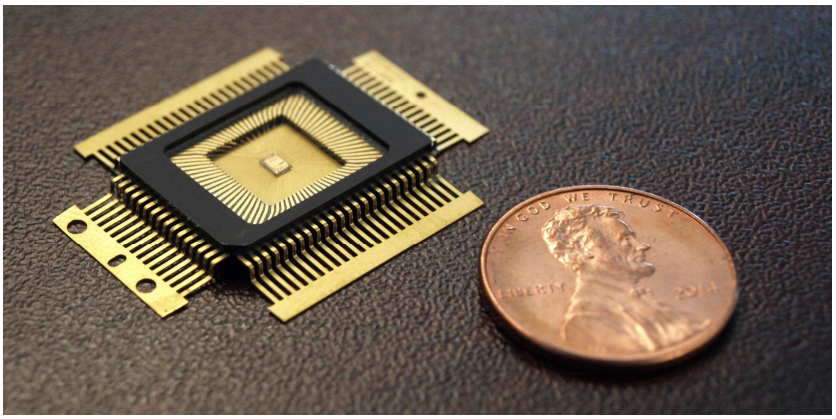


Figure I.3: Bonded Die with 80 pin QFP package relative to a coin.

I.2.2 QFN 9 x 9 package

Since the Kyocera package required soldering, it was not practical in testing different accelerometers. A new board based on a QFN package was designed. The QFN package included the MEMS as well as the standalone die. Fig. I.4 shows the micrograph of the package with the MEMS die. Fig. I.5 shows the standalone IBM 0.13 μm die bonwired to the package.

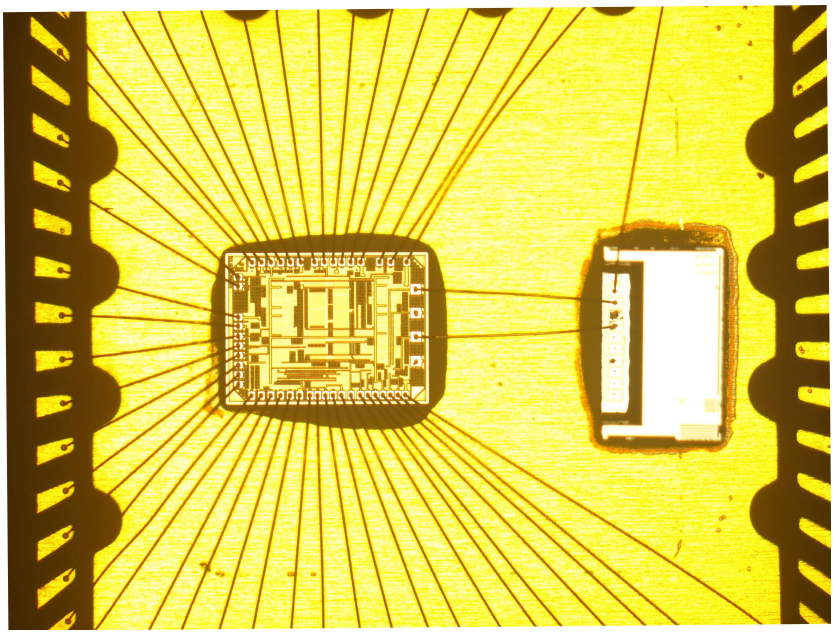


Figure I.4: QFN Package with bonded IC and commercial accelerometer.

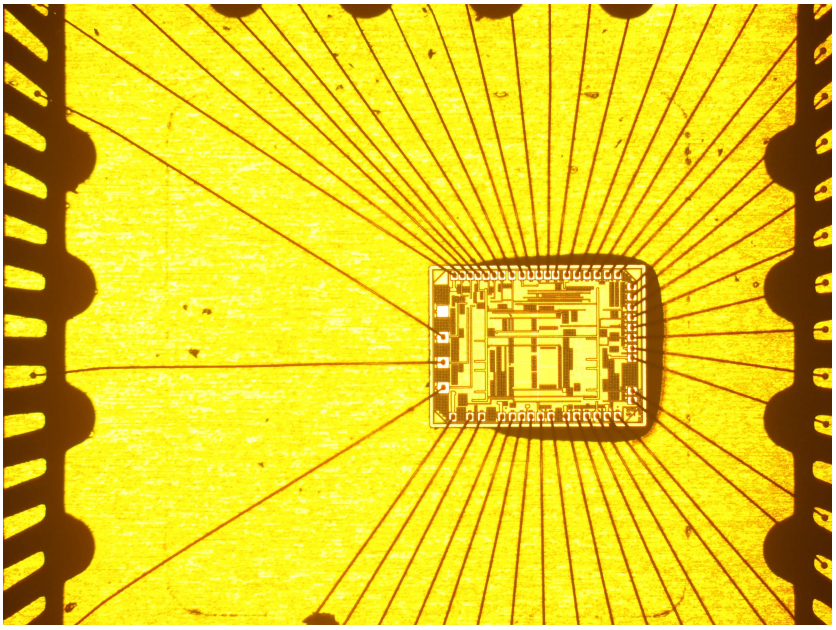


Figure I.5: QFN Package with bonded IC only.

I.3 PCB Boards

I.3.1 First Version of the PCB Board

A 20 cm x 20 cm four layer printed circuit board was designed for testing purposes. The layout and soldered board of the first version of this design is shown in Fig. I.6 and Fig. I.7 respectively.

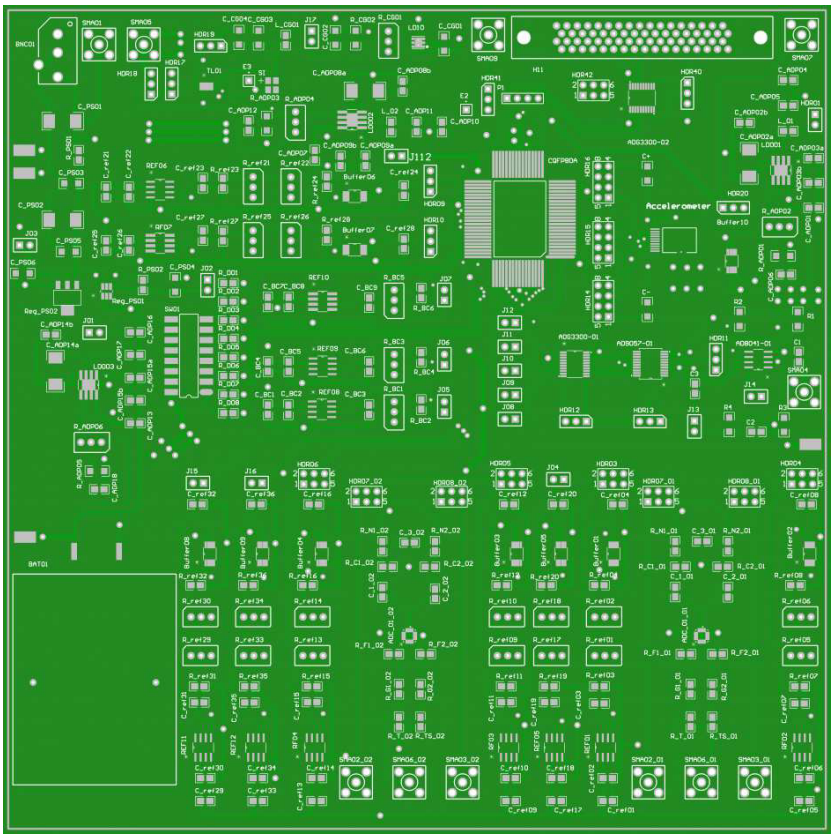


Figure I.6: Prototyped PCB board using a Kyocera package.

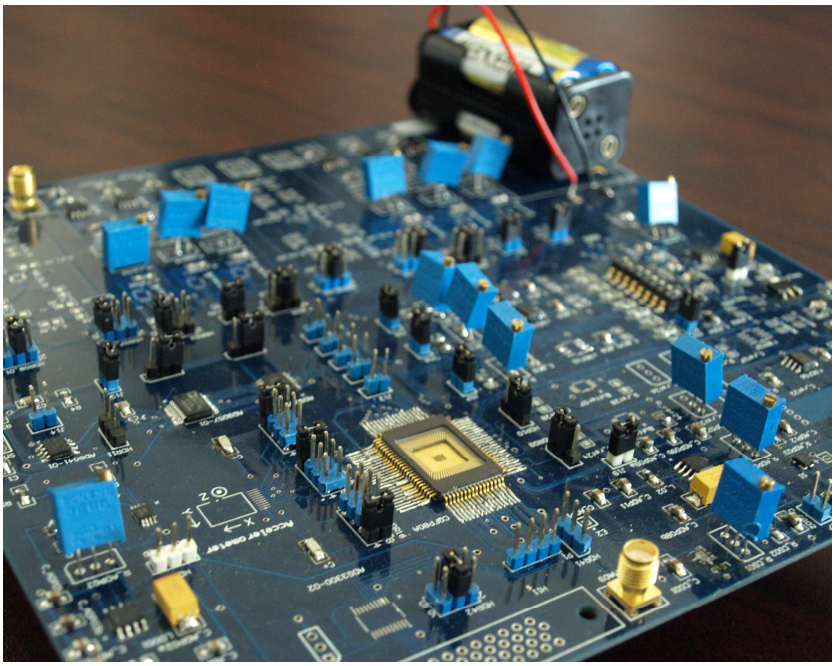


Figure I.7: Image of the first test PCB board using a Kyocera package.

I.3.2 Second Version of the PCB Board

To allow for testing of different dies and accelerometers, a second version of the board was designed with a QFN package[2] and improvements to signal conditioning and components were made based on the test results of the first version of the PCB. Fig. I.8 shows the PCB layout and Fig. I.9 shows the board with components soldered.

[2] Dies are not soldered but make contact through high pressure springs

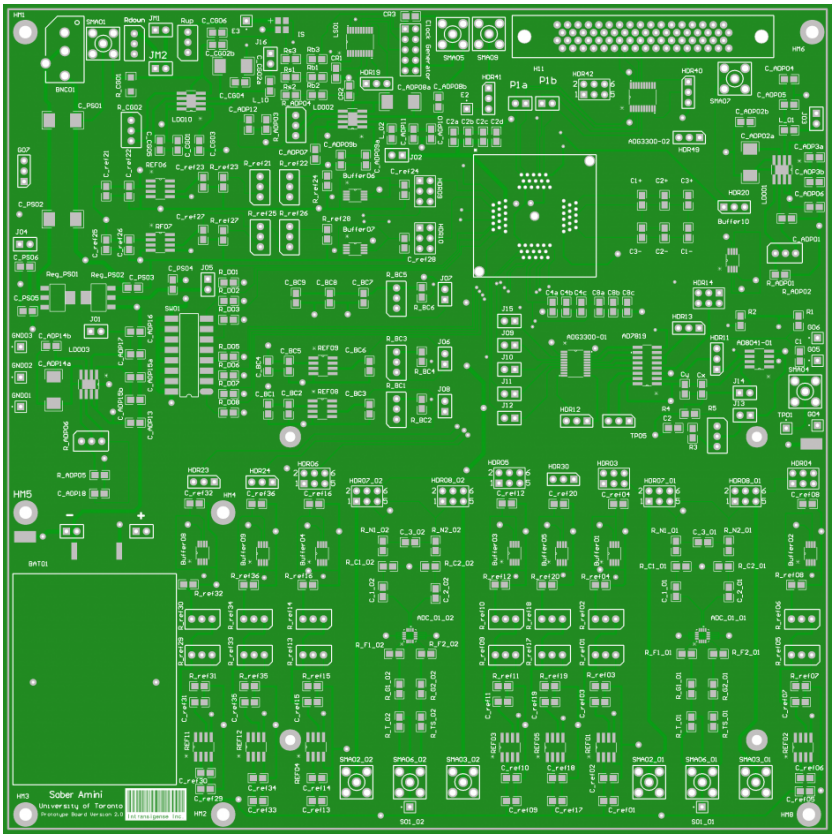


Figure I.8: Prototype PCB board using a Kyocera package.

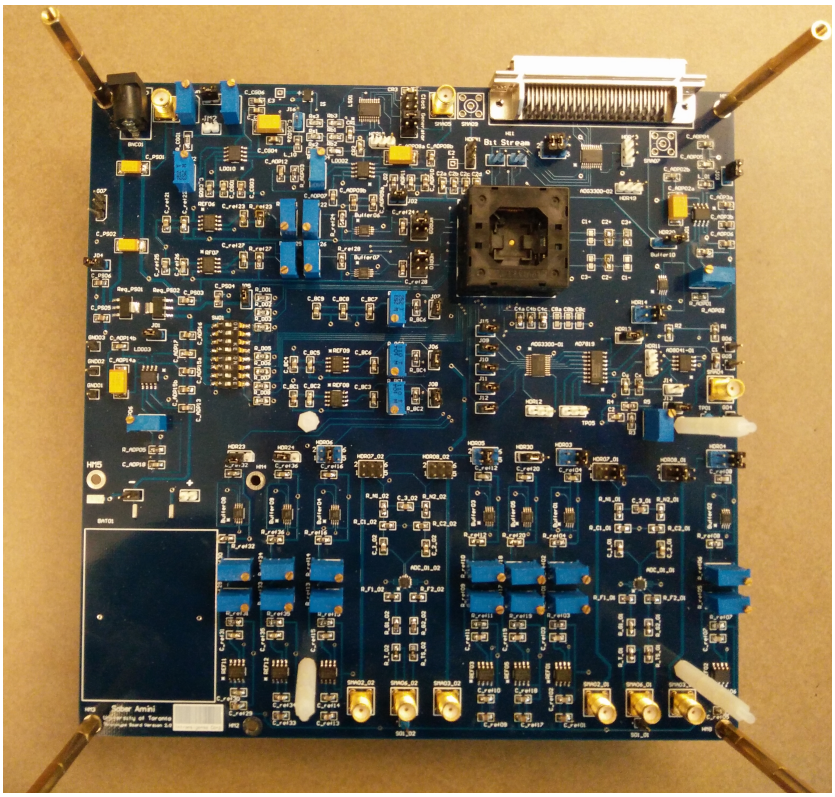


Figure I.9: Image of second test PCB board using a QFN package.

I.4 Accelerometer

The accelerometer used for the design was a commercial accelerometer without interface circuitry. A micrograph of the raw accelerometer is shown in Fig. I.10 and the relative size is shown in Fig. I.10.

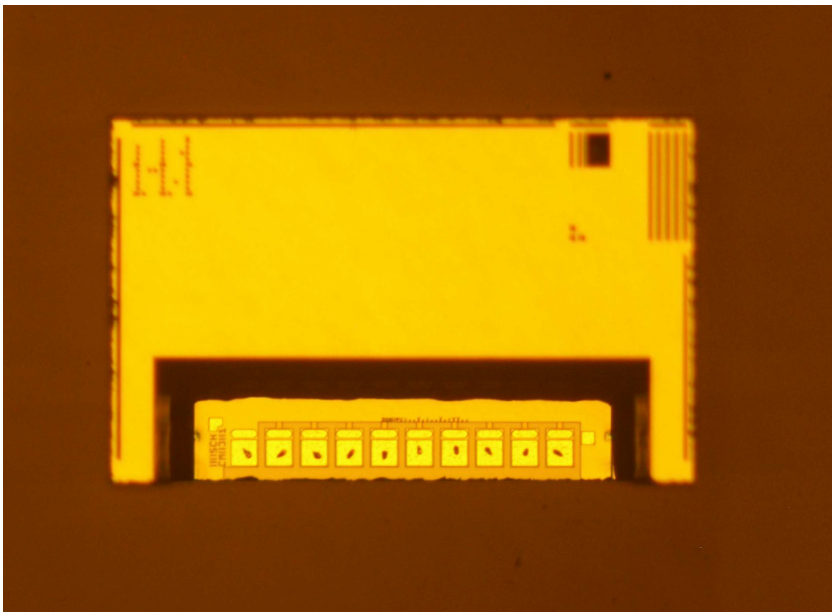


Figure I.10: A commercial surface micromachined accelerometer.. This is a raw accelerometer without readout circuitry or packages.

Figure I.11: Commercial accelerometer relative size to a coin.

I.5 Daughter Boards

Several external ready to be used boards were used along with the PCB in testing. These are shown in this section.

I.5.1 FPGA Readout

The Xilinx Spartan-6 was used primarily for reading data. A commercial board was used for programming and synchronization of the data [92].

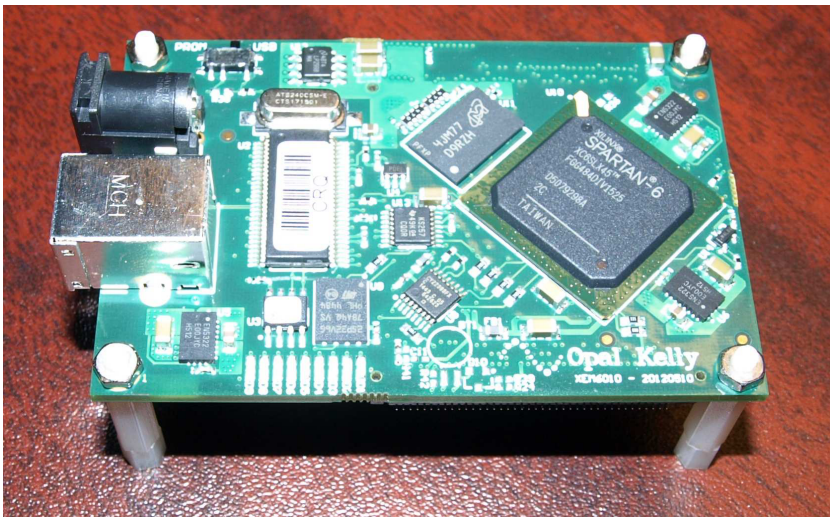


Figure I.12: Opal Kelly board used for data acquisition

I.5.2 Clock Generation

The board makes use of a MEMS based PLL for clock generation. This is an option to use for accelerometer testing to minimize wires.

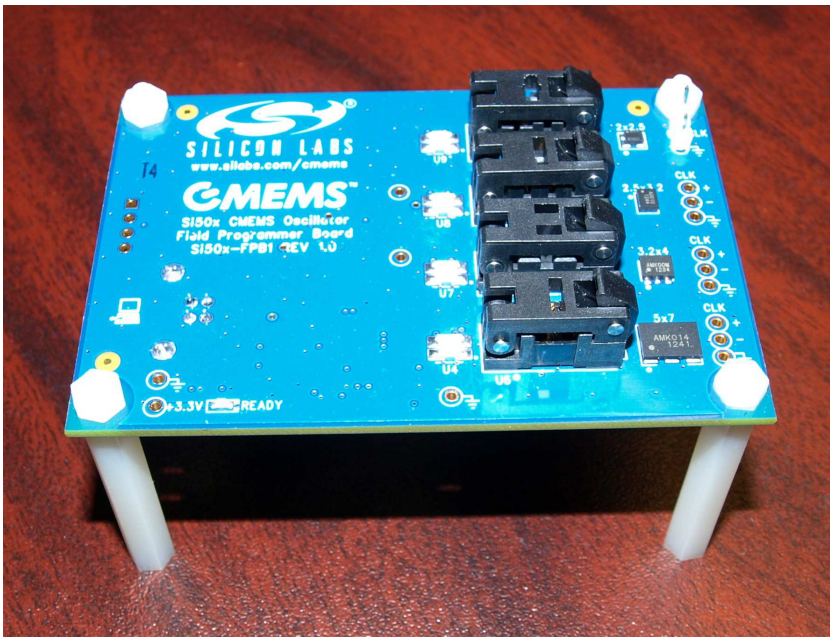


Figure I.13: Silicon Labs MEMS based clocks.

I.6 Step Motor

A step motor was used to generate sinusoidal acceleration movement. The test setup is shown in Fig. I.14 and I.15.

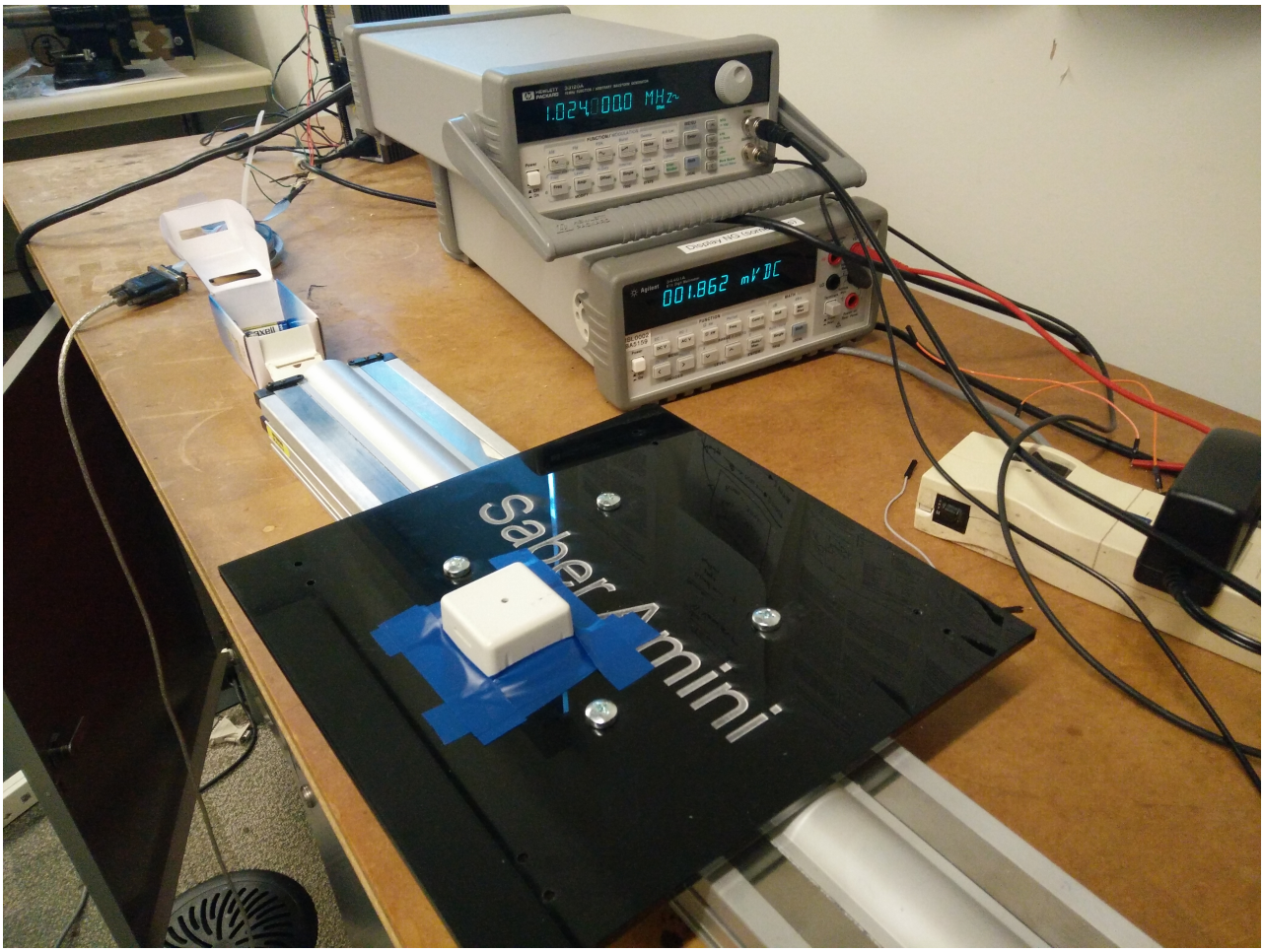


Figure I.14: Step motor with platform and acceleration tracker for analyzing the purity of sinusoidal movement.

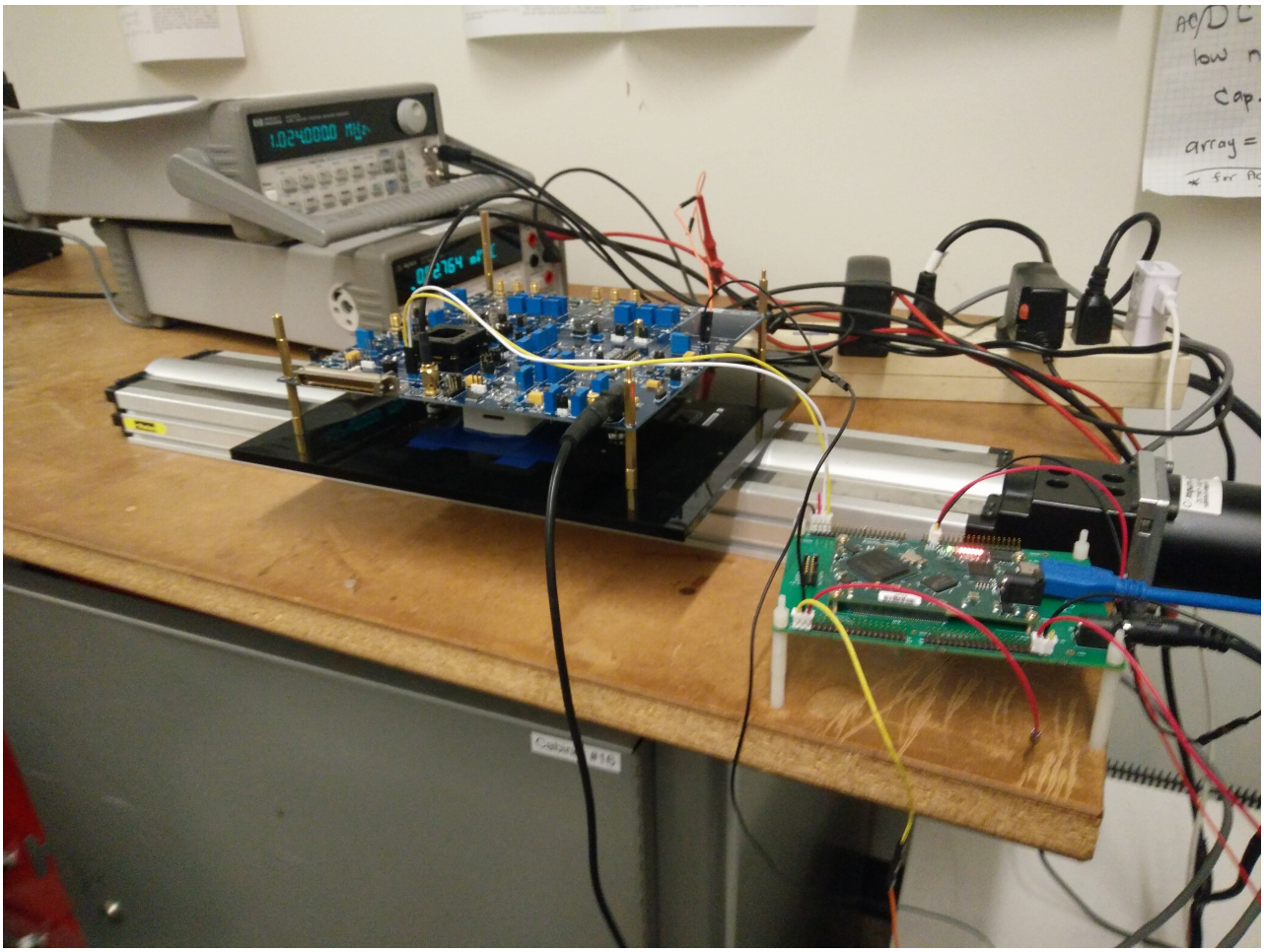


Figure I.15: Step motor with platform and data acquisition board.

Bibliography

[1] Y. Tsividis, "Continuous-time digital signal processing," *Electronics Letters*, vol. 39, pp. 1551–1552, Oct 2003.

[2] M. Hekmat, F. Aryanfar, J. Wei, V. Gadde, and R. Navid, "A 25 GHz Fast-Lock Digital LC PLL With Multiphase Output Using a Magnetically-Coupled Loop of Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 50, pp. 490–502, Feb 2015.

[3] A. Samarah and A. Carusone, "A Digital Phase-Locked Loop With Calibrated Coarse and Stochastic Fine TDC," *Solid-State Circuits, IEEE Journal of*, vol. 48, pp. 1829–1841, Aug 2013.

[4] W. Tang, *Electrostatic Comb Drive for Resonant Sensor and Actuator Applications*. PhD thesis, University of California Berkeley, 1990.

[5] C. Liu, *Foundations of MEMS*. New York: Pearson, 2 ed., 2011.

[6] W. Henrion, L. DiSanza, M. Ip, S. Terry, and H. Jerman, "Wide dynamic range direct accelerometer," in *Solid-State Sensor and Actuator Workshop, 1990. 4th Technical Digest., IEEE*, pp. 153–157, June 1990.

[7] S. Senturia, *Microsystem Design*. New York: Springer, 2 ed., 2004.

[8] K. D. Wise, "Integrated microelectromechanical systems: A perspective on MEMS in the 90s," in *[1991] Proceedings. IEEE Micro Electro Mechanical Systems*, pp. 33–38, Jan 1991.

[9] C. S. Smith, "Piezoresistance Effect in Germanium and Silicon," *Phys. Rev.*, vol. 94, pp. 42–49, Apr 1954.

[10] O. N. Tufte, P. W. Chapman, and D. Long, "Silicon Diffused-Element Piezoresistive Diaphragms," *Journal of Applied Physics*, vol. 33, pp. 3322–3327, Nov. 1962.

[11] W. H. Ko, J. Hynecek, and S. F. Boettcher, "Development of a miniature pressure transducer for biomedical applications," *IEEE*

Transactions on Electron Devices, vol. 26, pp. 1896–1905, Dec 1979.

[12] S. K. Clark and K. D. Wise, "Pressure sensitivity in anisotropically etched thin-diaphragm pressure sensors," *IEEE Transactions on Electron Devices*, vol. 26, pp. 1887–1896, Dec 1979.

[13] M. Bao, *Analysis and Design Principles of MEMS Devices*, ch. Capacitive Sensing and Effects of Electrical Excitation, pp. 226–242. New York: Elsevier, 2005.

[14] F. Rudolf, "A micromechanical capacitive accelerometer with a two-point inertial-mass suspension," *Sensors and Actuators*, vol. 4, pp. 191 – 198, 1983.

[15] W. C. Tang, T. C. H. Nguyen, and R. T. Howe, "Laterally driven polysilicon resonant microstructures," in *Micro Electro Mechanical Systems, 1989, Proceedings, An Investigation of Micro Structures, Sensors, Actuators, Machines and Robots. IEEE*, pp. 53–59, Feb 1989.

[16] A. Kourepenis, J. Borenstein, J. Connelly, R. Elliott, P. Ward, and M. Weinberg, "Performance of MEMS inertial sensors," in *IEEE 1998 Position Location and Navigation Symposium (Cat. No.98CH36153)*, pp. 1–8, Apr 1998.

[17] T. H. Yen, M. H. Tsai, C. I. Chang, Y. C. Liu, S. S. Li, R. Chen, J. C. Chiou, and W. Fang, "Improvement of CMOS-MEMS accelerometer using the symmetric layers stacking design," in *2011 IEEE SENSORS Proceedings*, pp. 145–148, Oct 2011.

[18] Y. C. Liu, M. H. Tsai, T. L. Tang, and W. Fang, "Improvement of CMOS-MEMS accelerometer using post-CMOS selective electroplating technique," in *2011 16th International Solid-State Sensors, Actuators and Microsystems Conference*, pp. 1002–1005, June 2011.

[19] H. Lakdawala and G. K. Fedder, "Temperature control of CMOS micromachined sensors," in *Technical Digest. MEMS 2002 IEEE International Conference. Fifteenth IEEE International Conference on Micro Electro Mechanical Systems (Cat. No.02CH37266)*, pp. 324–327, Jan 2002.

[20] J. Chae, H. Kulah, and K. Najafi, "A monolithic three-axis micro-g micromachined silicon capacitive accelerometer," *Journal of Microelectromechanical Systems*, vol. 14, pp. 235–242, April 2005.

[21] H. Takao, H. Fukumoto, and M. Ishida, "A CMOS integrated three-axis accelerometer fabricated with commercial submicrometer

CMOS technology and bulk-micromachining," *IEEE Transactions on Electron Devices*, vol. 48, pp. 1961–1968, Sep 2001.

[22] M. H. Tsai, Y. C. Liu, and W. Fang, "A Three-Axis CMOS-MEMS Accelerometer Structure With Vertically Integrated Fully Differential Sensing Electrodes," *Journal of Microelectromechanical Systems*, vol. 21, pp. 1329–1337, Dec 2012.

[23] S. Amini and D. Johns, "A Figure of Merit for Capacitive Inertial Sensor Interface Circuits," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 99, pp. 00–00, Submitted 2017.

[24] S. Amini and D. Johns, "A Variable Gain Delta-Sigma Modulator for Differential Capacitive Accelerometers," *Sensors, IEEE Journal of*, vol. 99, p. 00, Submitted. 2017.

[25] J. Wu, G. K. Fedder, and L. R. Carley, "A Low-Noise Low-Offset Capacitive Sensing Amplifier for a 50 $\mu g/\sqrt{Hz}$ Monolithic CMOS MEMS Accelerometer," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 722–730, 2004.

[26] B. V. Amini and F. Ayazi, "A 2.5-V 14-bit $\Sigma\Delta$ CMOS SOI Capacitive Accelerometer," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 2467–2476, 2004.

[27] W. F. Lee and P. K. Chan, "A Capacitive-Based Accelerometer IC Using Injection-Nulling Switch Technique," *IEEE Trans. Circuits Syst. I*, vol. 55, pp. 980–989, 2008.

[28] M. Paavola, M. Kamarainen, E. Laulainen, M. Saukoski, L. Koskinen, M. Kosunen, and K. Halonen, "A Micropower $\Delta\Sigma$-Based Interface ASIC for a Capacitive 3-Axis Micro-Accelerometer," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 3193–3210, 2009.

[29] S. S. Tan, C. Y. Liu, L. K. Yeh, Y. H. Chiu, M. S. Lu, and K. Y. J. Hsu, "An Integrated Low-Noise Sensing Circuit With Efficient Bias Stabilization for CMOS MEMS Capacitive Accelerometers," *IEEE Trans. Circuits Syst. I*, vol. 58, pp. 2661–2672, 2011.

[30] M. Lemkin and B. E. Boser, "A Three-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and Digital Offset-Trim Electronics," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 456–468, 1999.

[31] V. P. Petkov and B. E. Boser, "A Fourth-Order Delta-Sigma Interface for Micromachined Inertial Sensors," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 1602–1609, 2005.

[32] H. Kulah, J. Chae, N. Yazdi, and K. Najafi, "Noise Analysis and Characterization of a Sigma-Delta Capacitive Microaccelerometer," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 352–360, 2006.

[33] B. V. Amini, R. Abdolvand, and F. Ayazi, "A 4.5-mW Closed-Loop $\Delta\Sigma$ Micro-Gravity CMOS SOI Accelerometer," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 2983–2991, 2006.

[34] C. Condemine, N. Delorme, J. Soen, J. Durupt, J. Blanc, M. Belleville, and A. Besançon-Voda, "A 0.8mA 50Hz 15b SNDR $\Delta\Sigma$ closed-loop 10g accelerometer using an 8^{th}-order digital compensator," in *Dig. Tech. Papers. IEEE Int. Solid-State Circuits Conf*, (San Francisco, California), pp. 248–249, Feb. 2005.

[35] M. Pastre, M. Kayal, H. Schmid, A. Huber, P. Zwahlen, A. M. Nguyen, and Y. Dong, "A 300 Hz 19b DR Capacitive Accelerometer based on a Versatile Front End in a 5^{th}-order $\Delta\Sigma$ loop," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC 2009)*,, (Athens, Greece), pp. 289–292, Sept. 2009.

[36] U. Sönmez, H. Külah, and T. Akın, "A $\Delta\Sigma$ micro accelerometer with 6 $\mu g//\sqrt{Hz}$ resolution and 130 dB dynamic range," *Analog Integrated Circuits and Signal Processing*, vol. 81, no. 2, pp. 471–485, 2014.

[37] M. Lemkin, *Micro Accelerometer Design with Digital Feedback Control*. PhD thesis, University of California, Berkeley, 1997.

[38] N. Yazdi and K. Najafi, "An all-silicon single-wafer micro-g accelerometer with a combined surface and bulk micromachining process," *IEEE Journal of Microelectromechanical Systems*, pp. 544–550, 2000.

[39] M. Saukoski, L. Aaltonen, T. Salo, and K. Halonen, "Readout Electronics with Bandpass Delta-Sigma A/D Converter for a Bulk Micromachined Capacitive Gyroscope," in *2005 IEEE Instrumentationand Measurement Technology Conference Proceedings*, vol. 2, pp. 769–774, May 2005.

[40] J. Raman, E. Cretu, P. Rombouts, and L. Weyten, "A Closed-Loop Digitally Controlled MEMS Gyroscope With Unconstrained Sigma-Delta Force-Feedback," *IEEE Sensors Journal*, vol. 9, pp. 297–305, March 2009.

[41] M. Steyaert, Z. Y. Chang, and W. Sansen, "Low-noise monolithic amplifier design: Bipolar versus cmos," *Analog Integrated Circuits and Signal Processing*, vol. 1, no. 1, pp. 9–19, 1991.

[42] B. E. Boser, "Electronics for Micromachined Inertial Sensors," in *Solid State Sensors and Actuators, 1997. TRANSDUCERS '97 Chicago., 1997 International Conference on*, vol. 2, pp. 1169–1172 vol.2, Jun 1997.

[43] F. Ayazi and K. Najafi, "A HARPSS polysilicon vibrating ring gyroscope," *Journal of Microelectromechanical Systems*, vol. 10, pp. 169–179, Jun 2001.

[44] H. Luo, G. Zhang, L. R. Carley, and G. K. Fedder, "A post-CMOS micromachined lateral accelerometer," *Journal of Microelectromechanical Systems*, vol. 11, pp. 188–195, Jun 2002.

[45] J. M. Tsai and G. K. Fedder, "Mechanical noise-limited CMOS-MEMS accelerometers," in *18th IEEE International Conference on Micro Electro Mechanical Systems, 2005. MEMS 2005.*, pp. 630–633, Jan 2005.

[46] S. E. Alper and T. Akin, "A Single-Crystal Silicon Symmetrical and Decoupled MEMS Gyroscope on an Insulating Substrate," *Journal of Microelectromechanical Systems*, vol. 14, pp. 707–717, Aug 2005.

[47] S. J. Sherman, W. K. Tsang, T. A. Core, R. S. Payne, D. E. Quinn, K. H. L. Chau, J. A. Farash, and S. K. Baum, "A low cost monolithic accelerometer; product/technology update," in *Electron Devices Meeting, 1992. IEDM '92. Technical Digest., International*, pp. 501–504, Dec 1992.

[48] K. H. L. Chau, S. R. Lewis, Y. Zhao, R. T. Howe, S. F. Bart, and R. G. Marcheselli, "An Integrated Force-balanced Capacitive Accelerometer For Low-G Applications," in *Solid-State Sensors and Actuators, 1995 and Eurosensors IX.. Transducers '95. The 8th International Conference on*, vol. 1, pp. 593–596, Jun 1995.

[49] W. Yun, R. T. Howe, and P. R. Gray, "Surface micromachined, digitally force-balanced accelerometer with integrated CMOS detection circuitry," in *Solid-State Sensor and Actuator Workshop, 1992. 5th Technical Digest., IEEE*, pp. 126–131, June 1992.

[50] B. E. Boser and R. T. Howe, "Surface micromachined accelerometers," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 366–375, Mar 1996.

[51] L. K. Baxter, *Capacitive Sensors: Design and Applications* . New York: Wiley-IEEE Press, 1 ed., 2002.

[52] M. Tavakoli and R. Sarpeshkar, "An offset-canceling low-noise lock-in architecture for capacitive sensing," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 244–253, Feb 2003.

[53] L. Aaltonen, P. Rahikkala, M. Saukoski, and K. Halonen, "High resolution analog interface for micromachined capacitive accelerometer," in *Circuit Theory and Design, 2007. ECCTD 2007. 18th European Conference on*, pp. 96–99, Aug 2007.

[54] D. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley, 2 ed., 2011.

[55] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, pp. 1584–1614, Nov 1996.

[56] A. Acharya, P. J. Hurst, and S. H. Lewis, "Thermal noise from switches in a switched-capacitor gain stage," in *Mixed-Signal Design, 2003. Southwest Symposium on*, pp. 121–126, Feb 2003.

[57] X. Wang, Z. Shi, and B. Xu, "Noise analysis of a CDS circuit with offset canceling," in *2015 IEEE 11th International Conference on ASIC (ASICON)*, pp. 1–4, Nov 2015.

[58] D. Johns, "Lecture notes for ECE 1371: Advanced Analog Circuits," February 2011.

[59] N. Wongkomet and B. E. Boser, "Correlated double sampling in capacitive position sensing circuits for micromachined applications," in *Circuits and Systems, 1998. IEEE APCCAS 1998. The 1998 IEEE Asia-Pacific Conference on*, pp. 723–726, 1998.

[60] R. Puers and D. Lapadatu, "Electrostatic forces and their effects on capacitive mechanical sensors," *Sensors and Actuators A: Physical*, vol. 56, no. 3, pp. 203 – 210, 1996.

[61] M. Bao, H. Yang, H. Yin, and S. Shen, "Effects of electrostatic forces generated by the driving signal on capacitive sensing devices," *Sensors and Actuators A: Physical*, vol. 84, no. 3, pp. 213 – 219, 2000.

[62] K. Martin, "A voltage-controlled switched-capacitor relaxation oscillator," *IEEE Journal of Solid-State Circuits*, vol. 16, pp. 412–414, Aug 1981.

[63] H. Tuinhout, H. Elzinga, J. Brugman, and F. Postma, "Accurate capacitor matching measurements using floating gate test structures," in *Microelectronic Test Structures, 1995. ICMTS 1995. Proceedings of the 1995 International Conference on*, pp. 133–137, Mar 1995.

[64] Y. Cao and G. C. Temes, "High-accuracy circuits for on-chip capacitance ratio testing or sensor readout," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 41, pp. 637–639, Sep 1994.

[65] B. Wang, T. Kajita, T. Sun, and G. Temes, "High-accuracy circuits for on-chip capacitive ratio testing and sensor readout," *IEEE Transactions on Instrumentation and Measurement*, vol. 47, pp. 16–20, Feb 1998.

[66] L. A. Williams and B. A. Wooley, "Third-order cascaded sigma-delta modulators," *IEEE Transactions on Circuits and Systems*, vol. 38, pp. 489–498, May 1991.

[67] S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*, ch. Higher-Order Delta-Sigma Modulators, p. 83. New Jersey: Wiley-IEEE Press, 2 ed., 2017.

[68] D. H. B. John A. Pelesko, *Modeling MEMS and NEMS*. New York: Wiley, 1 ed., 2002.

[69] H. Leuthold and F. Rudolf, "An ASIC for High-resolution Capacitive Microaccelerometers," *Sensors and Actuators A*, vol. 21, pp. 278–281, 1990.

[70] C. Lu, M. Lemkin, and B. E. Boser, "A Monolithic Surface Micromachined Accelerometer with Digital Output," in *Dig. Tech. Papers. IEEE Int. Solid-State Circuits Conf.*, (San Francisco, California), pp. 160–161, Feb. 1995.

[71] S. Amini and D. Johns, "A Flexible Charge-Balanced Ratiometric Open-Loop Readout System for Capacitive Inertial Sensors," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 62, pp. 317–321, April 2015.

[72] R. Schreier, J. Silva, J. Steensgaard, and G. C. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 11, pp. 2358–2368, 2005.

[73] M. Yücetas, L. Aaltonen, and K. Halonen, "Linearity study of a self-balancing capacitive half-bridge sensor interface," in *2010 12th Biennial Baltic Electronics Conference*, pp. 115–118, Oct 2010.

[74] F. Zhu and J. Spronck, "A capacitive tactile sensor for shear and normal force measurements," *Sensors and Actuators A: Physical*, vol. 31, no. 1, pp. 115 – 120, 1992.

[75] "AG-1 Data Logger (Accelerometer and Gyroscope)." http://www.icewire.ca/. Accessed: 2016-07-30.

[76] R. Lyons, *Understanding Digital Signal Processing*. New York: Prentice Hall, 2 ed., 2010.

[77] D. D. Dorigo, S. Rombach, M. Maurer, M. Marx, S. Nessler, and Y. Manoli, "Q-enhancement of a low-power gm-C bandpass filter for closed-loop sensor readout applications," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 678–681, May 2015.

[78] J. Jun, C. Rhee, and S. Kim, "A 386-μW, 15.2-bit Programmable-Gain Embedded Delta-Sigma ADC for Sensor Applications," in *Proceedings of the 2016 International Symposium on Low Power Electronics and Design*, pp. 278–283, ACM, 2016.

[79] Y. M. Wang, P. K. Chan, H. K. H. Li, and S. E. Ong, "A Low-Power Highly Sensitive Capacitive Accelerometer IC Using Auto-Zero Time-Multiplexed Differential Technique," *IEEE Sensors Journal*, vol. 15, pp. 6179–6191, Nov 2015.

[80] L. Sumanen, M. Waltari, V. Hakkarainen, and K. Halonen, "CMOS dynamic comparators for pipeline A/D converters," in *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*, vol. 5, pp. V–157–V–160 vol.5, 2002.

[81] K. K. Manolis Terrovitis, "Device Noise Simulation of $\Delta\Sigma$ Modulators," May 2006.

[82] D. Halliday, R. Resnick, and J. Walker, *Fundamentals of Physics*. John Wiley & Sons, 2010.

[83] T.-R. Hsu, *MEMS and Microsystems: Design, Manufacture, and Nanoscale Engineering*. New York: Wiley, 2011.

[84] E. Peeters, S. Vergote, B. Puers, and W. Sansen, "A highly symmetrical capacitive micro-accelerometer with single degree-of-freedom response," *Journal of Micromechanics and Microengineering*, vol. 2, no. 2, p. 104, 1992.

[85] K. Kundert, "Modeling Varactors." http://www.designers-guide.org/modeling/varactors.pdf. Accessed: 2011-01-27.

[86] H. Weinberg, "Accelerometers - Fantasy Reality." http://www.analog.com/en/analog-dialogue/articles/accelerometers-fantasy-and-reality.html. Accessed: 2016-06-20.

[87] S. Amini and D. Johns, "A Pseudo-Differential Charge Balanced Ratiometric Readout System for Capacitive Inertial Sensors," in *Circuits and Systems (MWSCAS), 2015 IEEE 58th International Midwest Symposium on*, pp. 306–309, Aug 2015.

[88] T. Kajita, U.-K. Moon, and G. C. Temes, "A noise-shaping accelerometer interface circuit for two-chip implementation," in *Instrumentation and Measurement Technology Conference, 2001. IMTC 2001. Proceedings of the 18th IEEE*, vol. 3, pp. 1581–1586 vol.3, 2001.

[89] B. V. Amini, S. Pourkamali, M. Zaman, and F. Ayazi, "A new input switching scheme for a capacitive micro-g accelerometer," in *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on*, pp. 310–313, June 2004.

[90] H. Kulah and K. Najafi, "A low noise switched-capacitor interface circuit for sub-micro gravity resolution micromachined accelerometers," in *Solid-State Circuits Conference, 2002. ESSCIRC 2002. Proceedings of the 28th European*, pp. 635–638, Sept 2002.

[91] J. Ardizzoni, "Driving Miss ADC." http://www.analog.com/en/analog-dialogue/raqs/raq-issue-84.html. Accessed: 2016-06-20.

[92] O. Kelly, "FPGA Integration Modules." https://www.opalkelly.com/products/. Accessed: 2016-05-11.