A Continuous-Time Modelling and Design Approach for Oversampled Passive Switched-Capacitor Filters

by

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Abstract

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Integrated technology advances towards shorter length transistors with faster operation frequencies and lower supply and threshold voltages. While these trends are pushed by digital performance, analog and RF designs do not necessarily benefit from them. Traditional high gain and high bandwidth operational amplifiers become harder to design, and thus topologies based on "digital friendly" components such as switches and capacitors can become preferable. In terms of filter design, these trends favour passive switched-capacitor networks, where active components (such as operational amplifiers) are not needed to transfer charge in between capacitors.

This thesis proposes a simplified continuous-time approach for modelling, design, analysis, and simulation of oversampled switched-capacitor circuits focusing on the passive switched-capacitor filters. The model provides an intuitive understanding of these structures by letting designers reach transfer functions and noise characteristics with good accuracy and without the need to go through complicated charge-balance equations. The aim of the model is mainly to give designers a tool that can lead to innovations through intuitive understanding. It is applicable to a variety of topologies including multi-phase passive switched-capacitor filters, switched-capacitor integrators, as well as switched-capacitor DC/DC converters.

With the proposed model, for the first time, complex-conjugate poles are integrated

on silicon by using only switches and capacitors. A continuous-time approach is reported to implement low-pass transfer functions with a sharper frequency profile compared to the passive switched-capacitor topologies present in the literature. Theory and simulation results are verified with measurements performed on the filter prototype integrated in a 0.13 µm CMOS technology. The prototype has a cut-off frequency of 470 kHz, 150 µW power consumption from a 1.2 V power supply, 92 dB SFDR, and an active area of 0.06 mm^2.

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Chapter 1

Background

1.1 A Very Brief History

1.1.1 Switched-Capacitor Circuits

In the literature, the switched-capacitor implementation and its behaviour as an equivalent resistance can be found as early as 1873, in the book of "A Treatise on Electricity and Magnetism" by J. C. Maxwell [1]. Maxwell states that if the connections of a condenser, which is connected in between the ends of a wire, are reversed at regular intervals of time, T, then the quantity of electricity transmitted by the wire in each interval is equal to 2EC, where E is the electromotive force, and C is the capacity of the condenser. Fig. 1.1 visualizes this behaviour. He also states that this behaviour is only valid if the interval T is sufficiently long to allow of the complete discharge of the condenser. Thus, the condenser with the periodically reversing connections acts like an equivalent resistor:

$$\frac{E}{R} = \frac{2EC}{T}; \quad \text{or} \quad R = \frac{T}{2C}. \tag{1.1}$$

Approximately 100 years after Maxwell's book, switched-capacitor implementations reached popularity in electronics design due to the invention of MOS integrated cir-

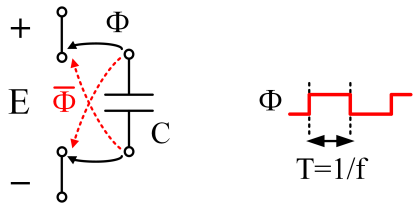


Figure 1.1: A condenser whose connections are reversed at regular intervals of time [1].

cuits [9–16]. Traditionally used active-RC topologies suffered from inaccurate transfer functions due to the mismatch in between integrated resistor and capacitor values (such as filter corner frequencies can vary up to 40 % over process and temperature variations [17]). Passive filters, which are composed of capacitors and inductors, were not an alternative as inductors were not possible to integrate at that time. On the other hand, switched-capacitor based filters became attractive due to their characteristics depending on capacitor ratios, which have higher accuracy for fabricated devices (down to 0.1 % [18]). Fabricated devices based on MOS technology decreased required cost and area of the circuits, and thus switched-capacitor based circuits and more specifically filters gained popularity. Since then, switched-capacitor filters have been widely used in signal processing by replacing the resistors in the equivalent active-RC implementations [6, p. 417]. Moreover, switched-capacitor based circuits have been used in various integrated circuits such as analog-to-digital (A/D) [19, 20] and digital-to-analog (D/A) converters [21, 22], mixers and samplers [23, 24], and power converters [25, 26].

Issues and the Return of Continuous-Time Filters

Inevitably, switched-capacitor circuits came along with some limitations. In terms of design, the synthesis of filters in z-domain was challenging for circuit designers. Moreover, several issues accompanying switched-capacitor circuits such as signal and noise aliasing, charge injection, opamp settling time, and slew rate limitations led designers to continue to work on improving the accuracy of continuous-time filters. There were many developments in the area of tunable and programmable continuous-time filters, which

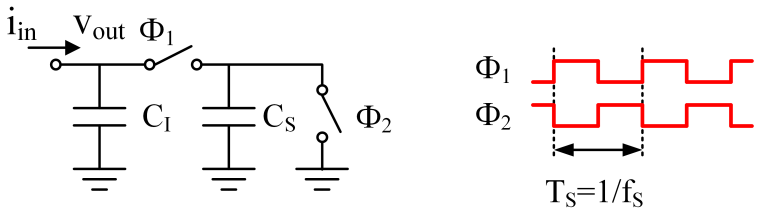


Figure 1.2: 1^{st}-order PSC filter with its clocking scheme [2].

include active-RC [27], MOSFET-C [28], and gm-C [29,30] filters that can address some of the issues of the early continuous-time filter attempts. Afterwards, around the 1990s, inductors became practical at $1GHz$ and above, leading to the use of passive filters.

Today, both continuous-time filters and switched-capacitor filters find applications in integrated circuit design [31–35], [36–40]. Switched-capacitor filters are preferred due to their accurate transfer functions depend on capacitor ratios and clock frequency with no requirement for calibration and tuning over changing process-voltage-temperature (PVT) variations. However, the existing operational amplifier for the charge transfer and requirement of oversampling can limit the speed of these filters.

1.1.2 Passive Switched-Capacitor Circuits

Passive switched-capacitor (PSC) circuits, whose variations can be found early as 1978 [41–48], are a particular subset of switched-capacitor networks that do not rely on active elements to transfer charge between capacitors [3]. As a basic example, the current input voltage output 1^{st}-order filter is shown in Fig. 1.2 can be considered as a passive switched-capacitor structure as there is no active component. In other words, there is no amplifier used to transfer charge between capacitors C_I and C_S. (Although, the switch is generally implemented using a transistor, the transistor is biased in triode (linear) region. Thus, it acts as a passive element, i.e., resistor.)

Elimination of the active elements may allow one to increase the maximum operating frequency up to the settling time required by the passive charge sharing paths, to reduce

the consumed power, and to improve the linearity due to the fewer number of active components. PSC filters also inherit the advantages of switched-capacitor filters such as the corner frequencies are defined as capacitors ratios. This property also leads to PVT independent corner frequencies. Moreover, similar to switched-capacitor filters, corner frequencies can also be easily programmable by changing the clock frequency [3].

In the 1980s, in parallel to the advances in switched-capacitor topologies, passive switched-capacitor structures also had their fair share of interest. The advantages of the passive switched-capacitor filters were mainly pointed out as the lower power supply and power consumption requirements due to the elimination of the operational amplifiers. Moreover, the simple structure of filters that are only composed of switches and capacitors were easy to implement using integrated technology. During that time, various filter and even resonator structures with complex-conjugate poles were studied [41, 44]. However, having no operational amplifiers resulted in limitations on the number of cascaded stages as well as limiting the quality factor (Q) of the poles. Thus, realizable filter characteristics become restricted [44].

1.2 Renewed Interest

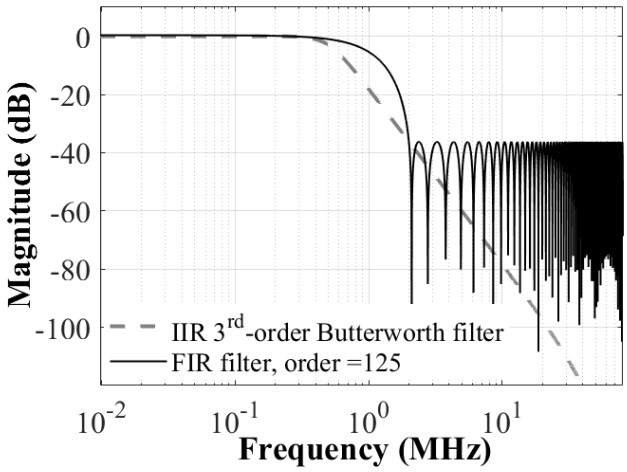
As integrated circuit technology advances towards shorter length transistors, analog designers need to reconsider the conventional implementations. Advanced transistors require lower power supply voltages and make the design of high-gain high-bandwidth amplifiers challenging to design. However, switch and capacitor based circuits work well in modern technologies due to lower parasitic components and fast clocking circuits. In terms of filter design, these trends favour passive switched-capacitor architectures, where the charge transfer between capacitors do not require the presence of an active element [3]. Passive switched-capacitor circuits are discrete-time circuits that are closest to the digital implementation. They are composed of switches, capacitors, and phase generators, all of

which benefit technology scaling. They are generally driven by inverter-based transconductors (g_m-cells), which are compatible with digital technology with improving g_m over bias current [4,5,49]. Moreover, these passive switched-capacitor infinite impulse response (IIR) filters can be advantageous compared to the finite impulse response (FIR) implementations, especially for large oversampling ratio applications. For instance, consider an oversampled filter with a sampling frequency of 160 MHz and 3 dB cut-off frequency of 500 kHz. An example FIR filter design can need more than 100 taps to approximate the transfer function of a 3^rd-order IIR Butterworth filter (Fig. 1.3a). Although this design achieves around 40 dB attenuation and mimics the Butterworth behaviour close to the band-edge, it fails to achieve high attenuation values at higher frequencies. If FIR filter design is modified to match also the high attenuations at higher frequencies, then we can end up with a more than 250-tap filter (Fig. 1.3b).

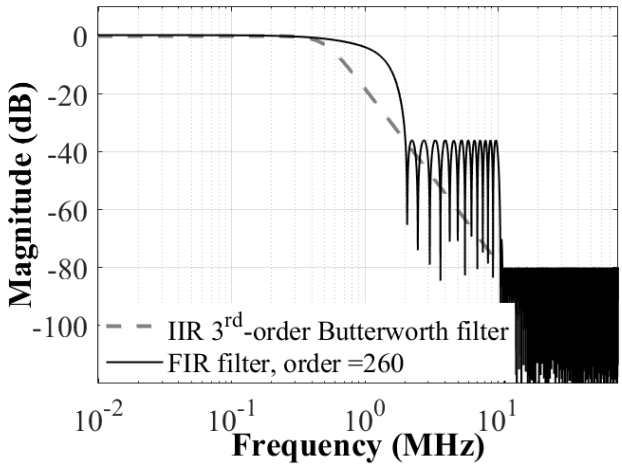
In recent literature, passive switched-capacitor topologies were used as an anti-aliasing integration sampler [2, 24], a channel-selection filter for receivers [4, 5, 8, 50–54], a decimation filter before an ADC [55], and a charge-based DAC for transmitters [21]. This section covers the operation and properties of passive switched-capacitor filters from recent literature.

1.2.1 Integration Sampler

The integration sampler shown in Fig. 1.4a was employed in a software-defined wireless receiver prototype to create discrete samples of the down-converted signal before fed into an ADC [24]. This 1^{st}-order sampler integrates the input signal on an integration capacitor, C_I, for a sampling period of T_S before sampling it on C_S with a gain of $g_m/(C_I + C_S)$. The integration sampling results in notches at the integer multiples of the sampling frequency, f_S (Fig. 1.4b). These notches attenuate the blockers that are folding on the desired channel. Moreover, C_I and C_S form a discrete-time infinite impulse response (IIR) filter with a single real pole at $z_p = C_I/(C_I + C_S)$. This pole leads to the



(a)



(b)

Figure 1.3: 3^{rd}-order IIR Butterworth filter magnitude response compared with a) 125-tap FIR filter and b) 260-tap FIR filter.

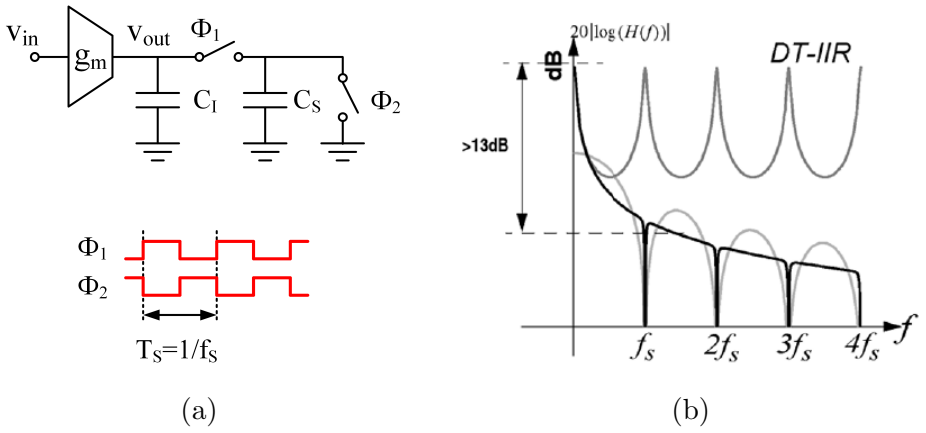


Figure 1.4: a) 1^{st}-order anti-aliasing integration sampler, and b) its transfer function [2].

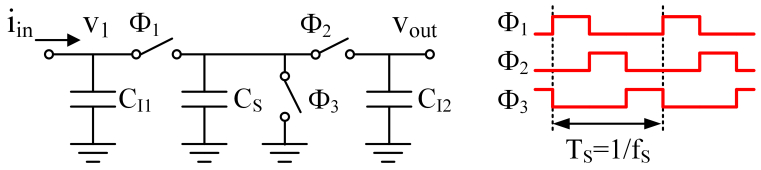


Figure 1.5: 2^{nd}-order PSC filter with three clock phases [3, p. 228].

attenuation of the adjacent channels due to the discrete-time IIR low-pass filter behaviour (Fig. 1.4b). Attenuation of the side-lobes releases the dynamic range requirements of the following ADC. Since both anti-aliasing notches and discrete pole depends on f_S, this integration sampler can be configurable to handle different bands only by changing f_S [2]. This sampler shows that the continuous input current integration on the filter capacitor, C_I, prior to sampling results in build-in 1^{st}-order anti-aliasing filtering, which is a property that is also inherited by subsequent high-order filters.

1.2.2 2^{nd}-Order Discrete-Time IIR Low-Pass Filter

The anti-aliasing integration sampler discussed above can only realize 1^{st}-order filtering. However, it is possible to modify the integration sampler to have a 2^{nd}-order discrete-time IIR low-pass filter characteristics by connecting C_S to a second integrating capacitor, C_{I2}, before resetting it to ground (Fig. 1.5) [3, p. 228]. The transfer function of the filter can be calculated first by writing charged-domain equations as follows:

$$\begin{aligned}(C_{I1}+C_S)V_1[n] =& C_{I1}V_1[n-1]+Q_{in}[n]\\ (C_{I2}+C_S)V_{out}[n+1/3] =& C_{I2}V_{out}[n-2/3]+C_SV_1[n+1/3]\\ \text{where } Q_{in}[n] =& \int_{(n-1)T_S}^{nT_S} g_mV_{in}(t)dt\end{aligned} \tag{1.2}$$

where n represents any sampling period with ϕ_1, ϕ_2, and ϕ_3, and $n-1$ represents the preceding sampling period. From Eqn. 1.2, z-domain equations can be written as:

$$\begin{aligned}(C_{I1}+C_S)V_1(z) =& C_{I1}V_1(z)z^{-1}+Q_{in}(z)\\ (C_{I2}+C_S)V_{out}(z)z^{1/3} =& C_{I2}V_{out}(z)z^{-1}z^{1/3}+C_SV_1(z)z^{1/3}\end{aligned} \tag{1.3}$$

Then, the z-domain transfer function becomes:

$$\frac{V_{out}(z)}{Q_{in}(z)}=\frac{1}{C_S}\frac{(1-\alpha_1)(1-\alpha_2)}{(1-\alpha_1z^{-1})(1-\alpha_2z^{-1})} \tag{1.4}$$

where $\alpha_i = C_{Ii}/(C_{Ii}+C_S)$. From the transfer function, it can be seen that there exist two real poles at $z_{p1}=\alpha_1$ and $z_{p1}=\alpha_2$. The DC gain can also be found as $1/C_S$ for $z=1$. The bilinear approximation can be used to find the corresponding s-domain pole locations as:

$$s_{pi}=\frac{2}{T_S}\frac{z_{pi}-1}{z_{pi}+1}=\frac{2}{T_S}\frac{\alpha_i-1}{\alpha_i+1}=\frac{2}{T_S}\frac{-C_S}{2C_{Ii}+C_S}\bigg|_{C_{Ii}\gg C_S}\approx-\frac{C_S}{T_SC_{Ii}} \tag{1.5}$$

1.2.3 High-Order Discrete-Time IIR Low-Pass Filter

To further increase the order of the low-pass passive switched-capacitor filter described in the previous part, a passive charge rotating filter structure was reported [4, 50]. It is possible to increase the order of the filter by adding more integrating capacitors and clock phases, such that a single C_S shares its charge with integrating capacitors sequentially before being reset to the ground in the last phase (Fig. 1.6). The number of the inte-

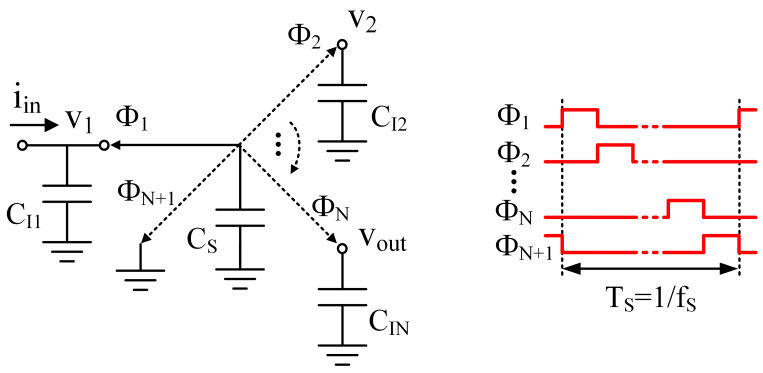


Figure 1.6: N^{th}-order PSC filter with all real poles [4].

grating capacitors in the filter determines the number of real poles created. The transfer function can be written similar to the 2^{nd}-order low-pass filter, starting from the charge balance equations (1.2). Then, the z-domain transfer function becomes:

$$\frac{V_{out}(z)}{Q_{in}(z)} = \frac{1}{C_S} \frac{(1-\alpha_1)(1-\alpha_2)...(1-\alpha_N)}{(1-\alpha_1 z^{-1})(1-\alpha_2 z^{-1})...(1-\alpha_N z^{-1})} \tag{1.6}$$

where $\alpha_i = C_{Ii}/(C_{Ii}+C_S)$. From the transfer function, it can be seen that there exist N real poles at $z_{pi} = \alpha_i$ with $i \in \mathbb{Z}[1, N]$. The DC gain can also be found as $1/C_S$ for $z = 1$. The bilinear approximation can be used to find the corresponding s-domain pole locations as:

$$s_{pi} = \frac{2}{T_S}\frac{z_{pi}-1}{z_{pi}+1} = \frac{2}{T_S}\frac{\alpha_i - 1}{\alpha_i + 1} = \frac{2}{T_S}\frac{-C_S}{2C_{Ii}+C_S}\bigg|_{C_{Ii} \gg C_S} \approx -\frac{C_S}{T_S C_{Ii}} \tag{1.7}$$

This high-order filter can only create real poles.

1.2.4 Passive Switched-Capacitor Filter with Active Feedback

Complex-conjugate pole implementation leads to sharper roll-off around band-edge and can lead to lower filter order for the same band-pass and band-stop specifications. A recent work adds an active feedback path from the output node to the input node of the passive switched-capacitor filter discussed above to generate complex-conjugate poles

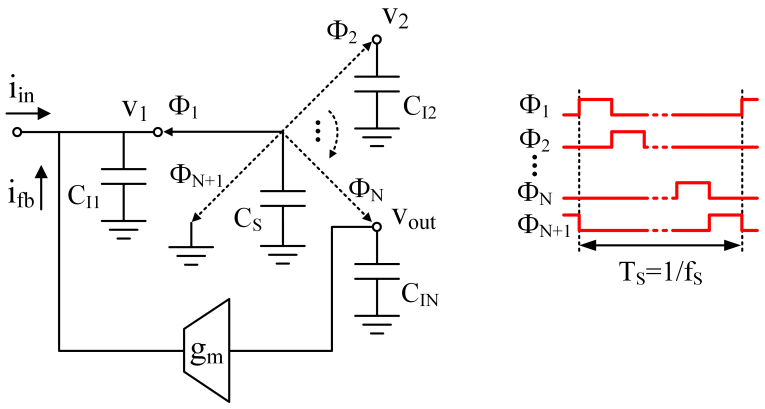


Figure 1.7: N^{th}-order PSC filter with active feedback. [5]

(Fig. 1.7) [5]. Although this approach achieves better roll-off close to the band edge due to the realized complex-conjugate poles, it eliminates some of the fundamental properties of the passive switched-capacitor filters. Most importantly, the transconductance realizes the active feedback leads to filter characteristics that are no longer only depends on capacitor ratios. Moreover, the feedback transconductance adds additional noise and non-linearity to the system.

1.3 Continuous-Time Modelling

Switched-capacitor circuits have linear time-varying characteristics requiring charge balance equations and z-domain analysis for the exact representation of their behaviour in discrete-time [6, p. 398]. However, under specific conditions, it is possible to analyze these structures with good accuracy using linear time-invariant components. For instance, as mentioned earlier, it is well known that a capacitor, C_S, connected to two voltage sources V_1 and V_2 in two different clock phases, ϕ_1 and ϕ_2, respectively, can be modelled using an equivalent resistance as shown in Fig. 1.8 (where R is equal to T_S/C_S with T_S corresponds to the clock period) [6, p. 399] [1]. This equivalence is derived by assuming ideal DC voltage sources connected to V_1 and V_2 nodes and by calculating the average current transfer in one clock period.

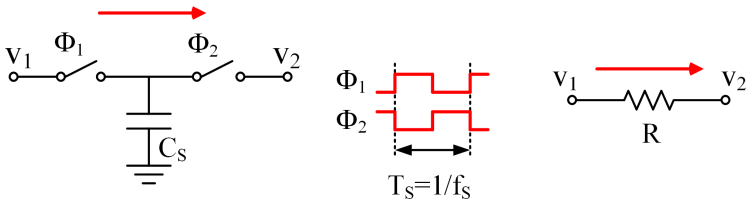


Figure 1.8: Basic two-phase switched-capacitor topology modelled with the traditional equivalent resistance [6, p. 399].

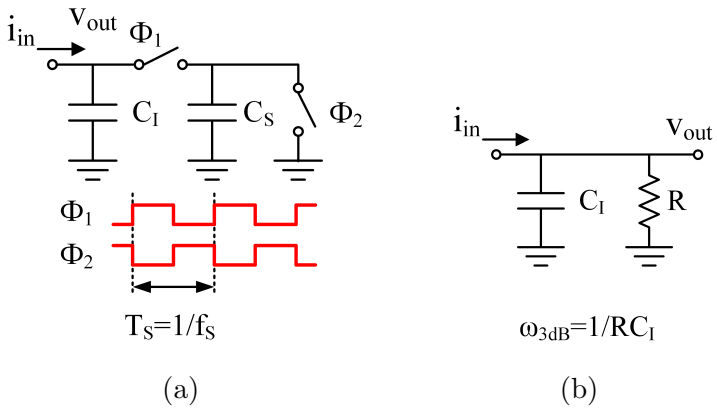


Figure 1.9: a) 1^{st}-order PSC filter and b) its continuous-time model with the traditional equivalent resistance approach [2].

This simple modelling approach helps one intuitively understand the operation of oversampled switched-capacitor circuits. For example, Fig. 1.9a shows the integration sampler (shown earlier in Fig. 1.4a) with current input and voltage output by focusing on the 1^{st}-order filtering. In this filter, C_S is switching in between a grounded integrating capacitor, C_I, and the ground node. C_I can be treated as a voltage source for C_I values much larger than C_S. Thus, the switching parts can be replaced by an equivalent resistor with a value of $1/f_S C_S$ (Fig. 1.9b) [2]. By using this model, the approximate DC gain ($R = 1/fsCs$) and bandwidth of the filter ($\omega_{3dB} = 1/RC_I = f_S C_S/C_I$) can be written intuitively without the need of charge-balance equations and z-domain transfer functions. However, there is no intuitive way to apply the equivalent resistor approach to the three-phase 2^{nd}-order switched-capacitor filter, which was shown in Fig. 1.5.

1.4 Motivation

Complex-Conjugate Poles

The passive switched-capacitor filters mentioned in the previous section rely on real poles preventing the synthesis of sharp filtering profiles such as the ones obtained by using Butterworth and Chebyshev filters. The one filter that can produce sharp filtering profile uses active feedback, which eliminated the advantages of the passive structure. In the literature, there also exists a complex passive switched-capacitor filter; however, it can only create a single complex pole by making use of an in-phase and a quadrature current inputs with two g_m-cells and four phases [8]. Implementation of complex-conjugate poles to realize Butterworth and Chebyshev filter responses may result in better suppression of the blockers compared to the real pole filters with the same orders. These sharper filtering profiles may help, for example, releasing the dynamic range requirements of the following stages. Moreover, it can result in lower power consumption as the filter order can be decreased for the same selectivity of the filter.

A Simplified Continuous-Time Model

Another issue with passive switched-capacitor filters covered so far is that the analysis of such filters is not intuitive and requires tedious charge-balance equations to obtain z-domain transfer function. Although rigorous analyses do not create a problem for the design of known structures, since it is a one-time effort, it can complicate the invention of new topologies. Moreover, noise analysis becomes even more complicated and requires long simulation times. A simplified continuous-time model that addresses these issues can lead to an intuitive understanding of the filter operation as well as the invention of new structures.

1.4.1 Organization of the Thesis

This thesis is organized as follows: Chapter 2 describes the proposed continuous-time modelling approach that can address multi-phase oversampled switched-capacitor structures together with examples. Chapter 3 shows how to implement complex-conjugate poles using the proposed model and only with switches and capacitors. Chapter 4 describes the noise analysis using the proposed model and goes through some of the practical limitations. Chapter 5 covers the implementation of the 3^{rd}-order passive switched-capacitor filter prototype with complex-conjugate poles. Finally, Chapter 6 summarizes contributions, on-going, and future work.

Chapter 2

From Discrete to Continuous-Time Modelling

In this section, the proposed continuous-time modelling of the oversampled switched-capacitor circuits is explained. A new model is developed, starting from the traditional equivalent resistance, for non-reciprocal multi-phase switched-capacitor structures, leading to an intuitive modelling and design approach. Several examples are also included to demonstrate the modelling approach and to address common misconceptions.

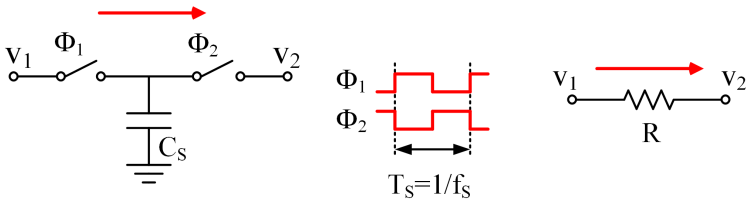


Figure 2.1: Basic two-phase switched-capacitor topology modelled with the traditional equivalent resistance [6, p. 399].

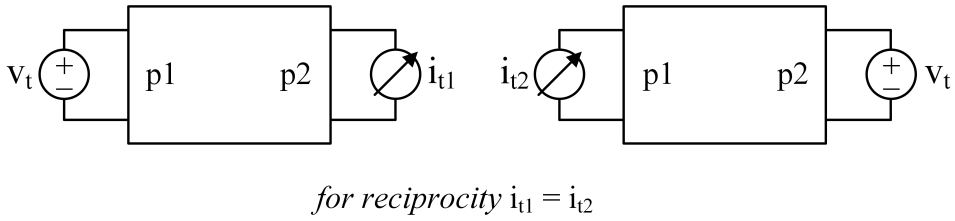


Figure 2.2: A reciprocity test for a continuous-time two-port network [7, p. 4].

2.1 Proposed Continuous-Time Model

2.1.1 Theory

It is known that a capacitor, C_S, connected to two voltage sources V_1 and V_2 in two different clock phases, ϕ_1 and ϕ_2, respectively, can be modelled using an equivalent resistance, R, as shown in Fig. 2.1 and as discussed in Section 1.1. Although this model can lead to an intuitive understanding of oversampled switched-capacitor structures [6, p. 399], it is limited to two-phase topologies with reciprocal low frequency behaviour.

2.1.2 Reciprocity

The reciprocity theorem is traditionally defined for continuous-time circuits. However, the reciprocity definition can come in handy to understand the shortcomings and applicability of the switched-capacitor equivalent resistor model. A continuous-time two-port network is defined as reciprocal if a test voltage source, v_t, applied to the first port generates a short circuit current on the second branch, i_{t1}, which is the same as the short circuit current generated on the first branch, i_{t2}, if the same test voltage source, v_t, is applied to the second port, as shown in Fig. 2.2 (i.e., $Z_{12} = Z_{21}$). A network that contains only ideal R, L, and C elements is reciprocal [7, p. 6]. In light of the reciprocity definition, we can conclude that a network of equivalent resistors can only model switched-capacitor topologies with a reciprocal low frequency behaviour.

Switched-capacitor circuits are time-varying circuits. Thus, a reciprocity test applied

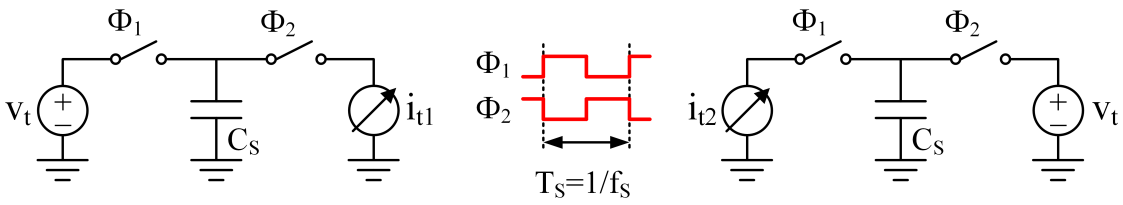


Figure 2.3: A reciprocity test for the two-phase switched-capacitor circuit.

on a switched-capacitor circuit fails. However, we are interested in the low frequency behaviour of these structures. We want to understand if this behaviour is "reciprocal" or not, such that we can have more clues on how to model these structures correctly.

Fig. 2.3 shows one "modified" reciprocity test applied to the conventional two-phase switched-capacitor circuit (Fig. 2.1). In this "modified" test, applied voltages are DC sources, and observed currents are average currents. Thus, effectively, we are checking the reciprocity of these circuits for DC signals.

Two average currents produced (i_{t1} and i_{t2}) as the result of the test voltage (v_t) applied to nodes V_1 and V_2, respectively are derived to be equal to each other:

$$i_{t1} = \frac{\Delta Q}{T_S} = \frac{C_S.V_t}{T_S} \tag{2.1}$$

$$i_{t2} = \frac{\Delta Q}{T_S} = \frac{C_S.V_t}{T_S} \tag{2.2}$$

where T_S is the sampling period. Thus, the two-phase switched-capacitor circuit can be defined to have a reciprocal low frequency behaviour. (It should be noted here that although the averaged behaviour is checked for simplicity, it is also possible to extend this approach for low frequency behaviour, where the frequency of interest is much smaller than the sampling frequency.) Thus, using an equivalent resistor to model the reciprocal low frequency behaviour of a two-phase switched-capacitor circuit makes sense.

Now, we can check the reciprocity of the three-phase switched-capacitor circuit shown

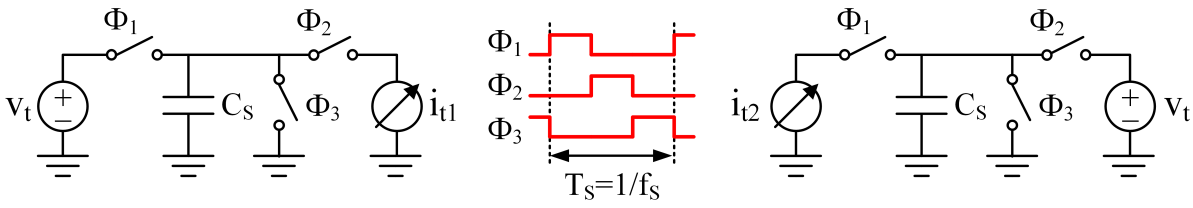


Figure 2.4: A reciprocity test for a three-phase switched-capacitor circuit.

in Fig. 1.5. Fig. 2.4 shows the reciprocity test applied to the switching parts of the circuit. Two average currents produced (i_{t1} and i_{t2}) as the result of test voltage (v_t) applied to nodes V_1 and V_{out}, respectively can be derived as follows:

$$i_{t1} = \frac{\Delta Q}{T_S} = \frac{C_S.V_t}{T_S} \tag{2.3}$$

$$i_{t2} = \frac{\Delta Q}{T_S} = \frac{C_S.0}{T_S} = 0 \tag{2.4}$$

where T_S is the sampling period. Although i_{t1} has the same non-zero value as Eqn. 2.2, i_{t2} has a zero value since C_S is reset to the ground in ϕ_3. Thus, the three-phase switched-capacitor circuit can be defined to have a non-reciprocal low frequency behaviour. Thus, we can conclude that using only bilateral elements such as R, L, and C to model the low frequency behaviour of this multi-phase circuit do not work out.

The Proposed Unilateral Model

To develop a new continuous-time model that can address multi-phase topologies with non-reciprocal low frequency behaviour, we can start by examining the derivation of the traditional equivalent resistance model in detail.

The resistance equivalence is derived by assuming ideal DC voltage sources connected to V_1 and V_2 nodes and by calculating the average current transfer in one clock period as follows:

$$\Delta Q = C_S.(V_1 - V_2) \tag{2.5}$$

$$I_A = \frac{\Delta Q}{T_S} = \frac{C_S.(V_1 - V_2)}{T_S} \tag{2.6}$$

$$R = \frac{V_1 - V_2}{I_A} = \frac{T_S}{C_S} = \frac{1}{f_S.C_S} \tag{2.7}$$

where I_A corresponds to the average current flowing from V_1 node to V_2 node in one sampling period, T_S. It is straight forward to show that the average current flowing from node V_1 is equal to the average current flowing into node V_2. Thus, a single $1/f_S C_S$ valued resistance is enough to model the average current behaviour and the loading of the nodes. (The derivation of the switched-capacitor equivalent resistance for low frequency inputs is covered in Appendix A, which results in the same $1/f_S C_S$ value.)

If we want to extend this modelling approach to multi-phase or non-reciprocal structures, a network of resistors is not helpful, as discussed earlier. Thus, a different perspective is necessary to address the issue. A unilateral approach is required to model the non-reciprocal behaviour.

To create a unilateral model, we can start by examining the average current flow at each node independently from the other nodes in the system. For example, for the two-phase switched-capacitor topology we have been working on (Fig. 2.1), rather than considering the average current flowing from V_1 to V_2, let us first solely model the average current flowing into V_2, which can be written as follows:

$$I_{A,2} = \frac{V_1 - V_2}{R} \tag{2.8}$$

where $I_{A,2}$ corresponds to the average current flowing into the node V_2, and R has the same value as the one derived in Eqn. 2.7. Basically, we are focusing on the behaviour

from the end of ϕ_1 until the end of ϕ_2. An ideal voltage buffer can be employed as shown in Fig. 2.5a to model $I_{A,2}$ without affecting the other nodes (i.e., V_1 node). The ideal voltage buffer does not load the node V_1 and realizes the desired unilateral behaviour. The loading of the node V_1 should also be accounted for to complete the model. The average current into the node V_1 can be written as follows using a similar approach:

$$I_{A,1} = \frac{V_2 - V_1}{R} \tag{2.9}$$

With this equation, we are focusing on the behaviour from the end of ϕ_2 until the end of ϕ_1 to complete the one sampling period. Thus, a second buffer + R branch can be placed, as shown in Fig. 2.5b. By combining two branches, the complete continuous-time model is obtained (Fig. 2.5c).

From this derivation, it follows that each phase change corresponds to a buffer + R branch, where C_S transfers voltage information from the previous node to the present node (modelled with the buffer), meanwhile charging itself to the present node voltage (modelled with R). Thus, the number of phases determines the number of buffer + R branches needed to complete the model. Once the model is complete, each node is connected to both a buffer and a resistor. (The derivation for low frequency inputs is covered in Appendix B, which results in the same buffer + R branch based model.)

The two buffer + R branches can be combined into a single R branch by using the Substitution Theorem, which leads back to the initial single equivalent resistance model (Fig. 2.1). This combination shows the compatibility of the new approach with the traditional one. This example also shows that it is possible to create a bilateral network by using multiple unilateral branches.

Although two buffer + R branches may seem redundant for a two-phase switched-capacitor topology, the primary motivation of this work is to address topologies with non-reciprocal low frequency behaviour with multiple phases. Thus, this new approach provides us the tool that is needed to create unilateral continuous-time models.

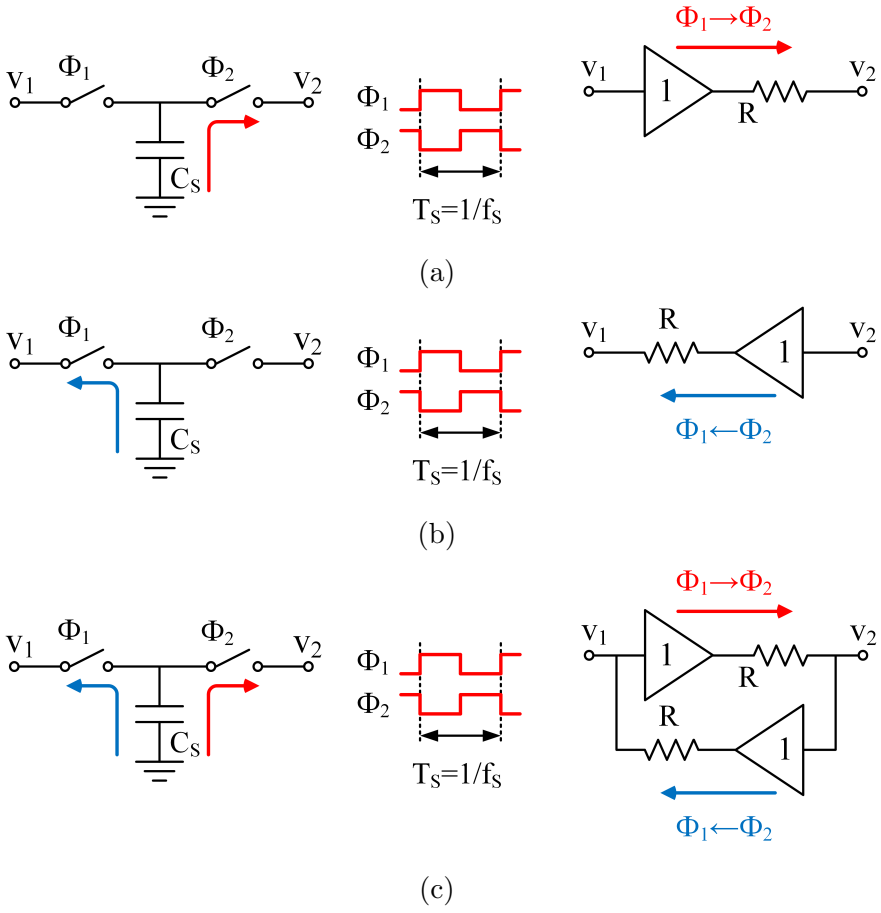


Figure 2.5: Two-phase switched-capacitor topology a) with the average current into V_2 is modelled, b) with the average current into V_1 is modelled, and c) with its complete proposed continuous-time model.

2.1.3 Examples

2^{nd}-Order Passive Switched-Capacitor Low-pass Filter with Real Poles

The 2^{nd}-order passive switched-capacitor filter shown in Fig. 2.6a has three phases, where C_S is connected to C_{I1}, C_{I2}, and ground nodes, respectively [3]. Three phases correspond to three buffer + R branches, which can be cascaded to create a loop as shown on the left side of Fig. 2.6b. Because C_S is connected to ground during ϕ_3, further simplifications[1] can be performed on the model as shown on the right-hand side of Fig. 2.6b. The resulting continuous-time model clearly shows the low-pass filter operation with two real poles at $1/RC_{I1}$ and $1/RC_{I2}$ without the need for any further analysis.

Fig. 2.7 shows the simulated transfer function of the PSC filter discrete-time implementation and continuous-time model with $C_S = 200fF, C_I = 8pF, f_S = 160MHz$. PSC simulations are performed with SpectreRF periodic steady state and sampled periodic AC analyses [56]. Model simulations are performed with ac simulations. It can be seen that both transfer function curves closely follow each other until the Nyquist rate, i.e., $f_S/2$.

Fig. 2.8 shows the simulated step response of the PSC filter discrete-time implementation and the continuous-time model. The bottom plot shows the difference between the discrete-time implementation sampled response and the continuous-time model response. The error is dominant (with less than 5mV) during the initial transient phase, which corresponds to the high-frequency response with limited model accuracy. As the step response settles, i.e., for the DC response, the error becomes zero.

High-Order Passive Switched-Capacitor Low-Pass Filter with Real Poles

It is possible to increase the order of this filter simply by increasing the number of clock phases and C_I's to which C_S is connected to before getting reset to ground. Fig. 2.9a

[1] These further simplifications eliminate a buffer + R branch that is connected to the ground node. If the ground current of interest, the initial model can be kept as it is.

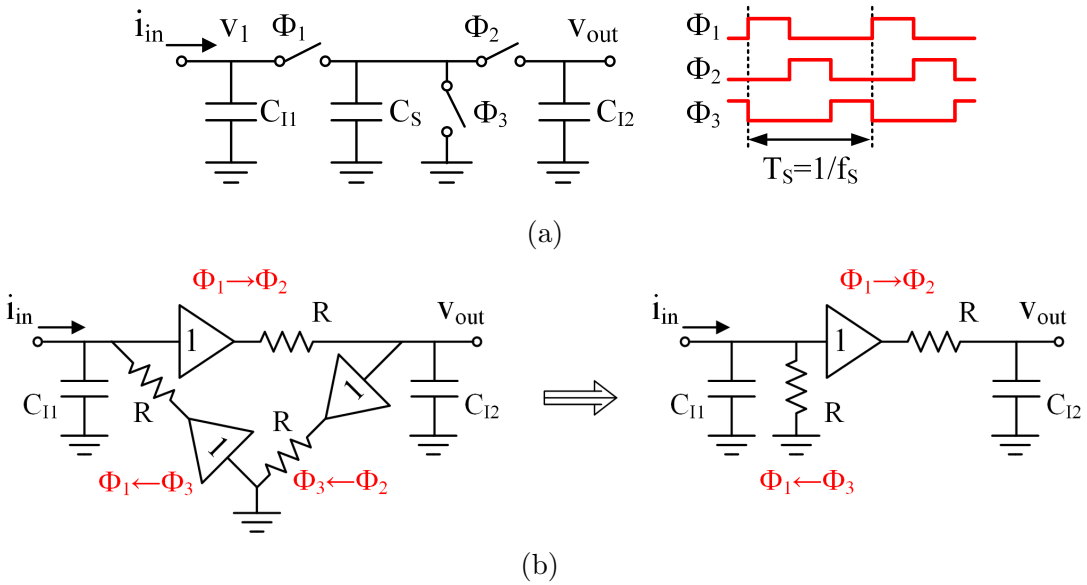


Figure 2.6: a) 2^{nd}-order PSC filter with three clock phases [3, p. 228], b) its continuous-time model.

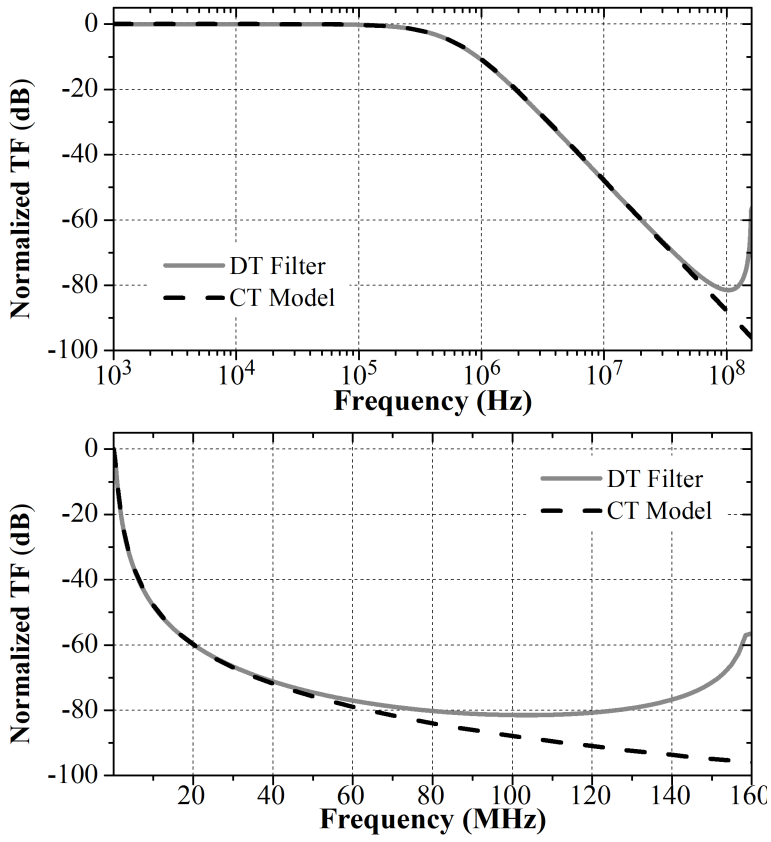


Figure 2.7: 2^{nd}-order PSC filter simulated discrete-time implementation and continuous-time model frequency responses with logarithmic and linear scale frequency axes.

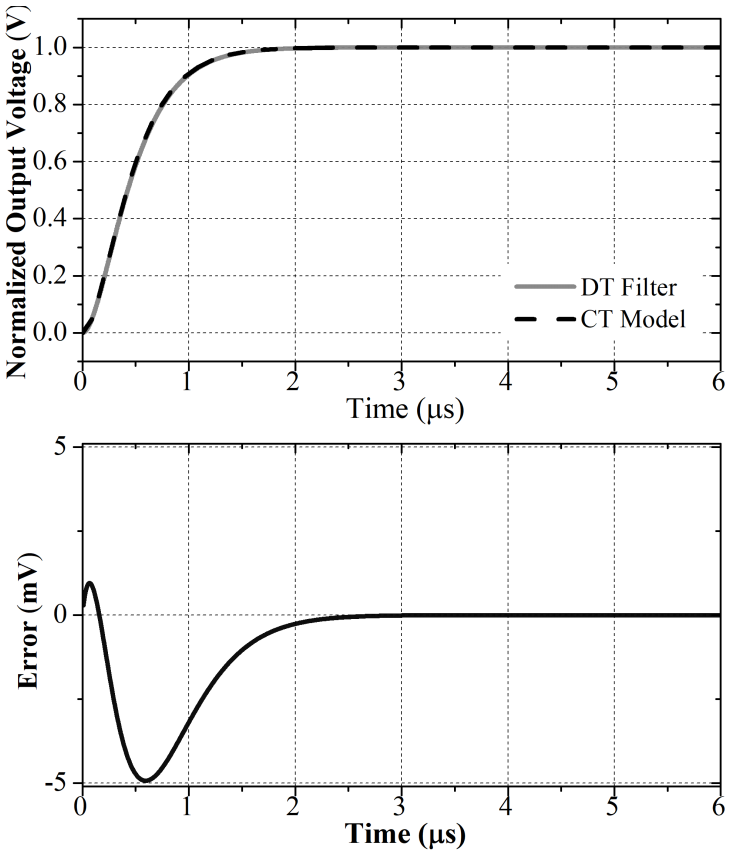


Figure 2.8: 2^{nd}-order PSC filter simulated discrete-time implementation and continuous-time model step responses, and the error between the step responses.

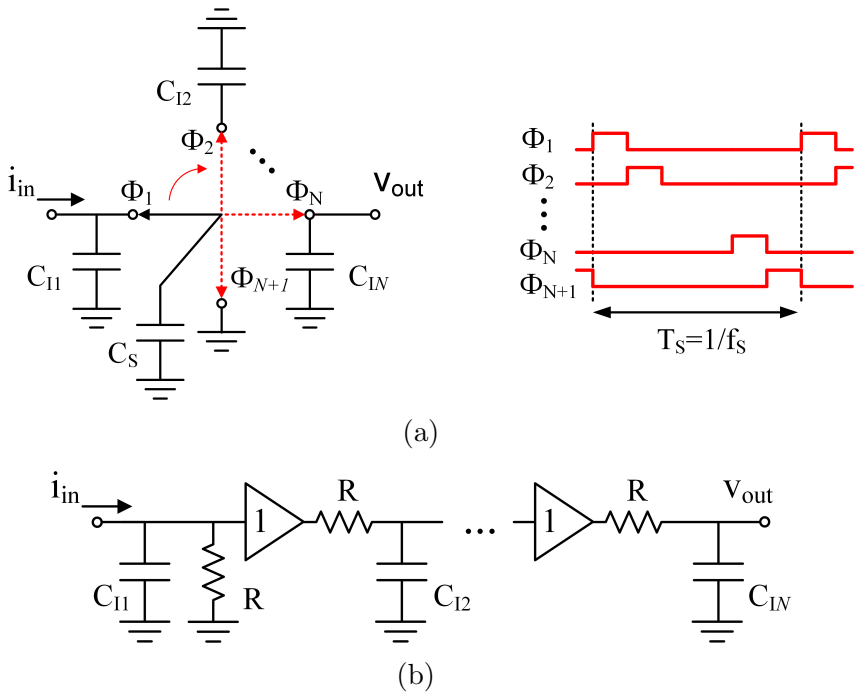


Figure 2.9: a) N^{th}-order PSC filter with $N+1$ clock phases [4], b) its continuous-time model.

shows an N^{th}-order PSC filter schematic [4], and its continuous-time model is presented in Fig. 2.9b.

It should be noted that in this example, the model is applied to a topology where C_S is not only connected to the zero impedance voltage sources as ground but also to other capacitors (C_I's). However, since C_I's are integrating capacitors with values much larger than C_S [57] [4], they can be treated as low impedance nodes, and the model works with good accuracy. Chapter 4 provides further details on the applicability and limitations of the model.

2.2 The Continuous-Time Model for Non-Grounded Sampling Capacitors

The proposed modelling approach that is defined in Section 2.1 can address multi-phase switched-capacitor structures, which can also have non-reciprocal low frequency be-

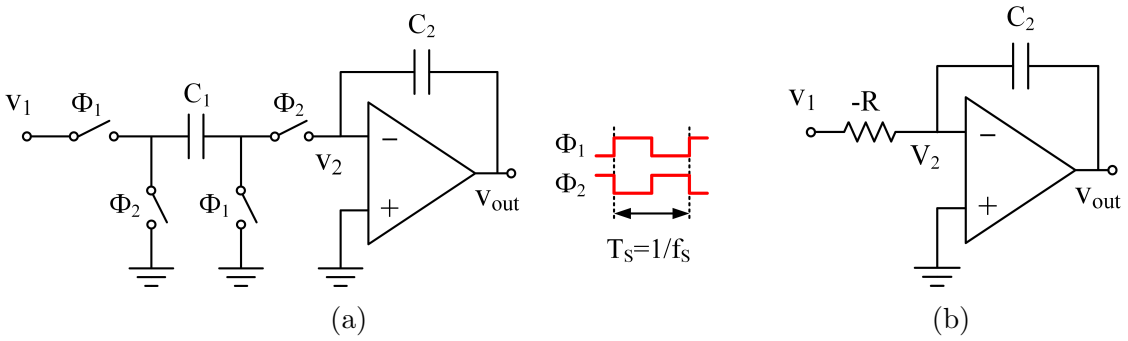


Figure 2.10: a) Parasitic insensitive switched-capacitor integrator, and b) its incorrect continuous-time model.

haviour. However, it relies on grounded sampling capacitors. There are a variety of switched-capacitor circuit implementations that employ sampling capacitors with both plates switching in between different nodes. One typical example is the parasitic insensitive switched-capacitor integrator shown in Fig. 2.10a. Conventionally, the switching parts are modelled using negative resistance, $-R$, as shown in Fig. 2.10b [6, p. 417]. Although this model can capture the correct positive voltage gain value, $-R$ indicates that for positive V_1 values, the current flows into the V_1 node from the virtual ground, which is not the case. Moreover, if this continuous-time approach is used to analyze the effect of the finite amplifier gain or the offset voltage, the analysis may result in false or inaccurate values together with a fictitious right-half plane pole at $+1/[(1+A)RC]$ rad/s, where A is the finite amplifier gain defined by $v_{out}/(v_+ - v_-)$. Apart from the parasitic insensitive switched-capacitor integrator, DC/DC converters with flying capacitors and even passive switched-capacitor filters can include sampling capacitors with non-grounded switching plates. This section generalizes the proposed continuous-time model for switched-capacitor circuits with non-grounded sampling capacitors to address the structures mentioned above.

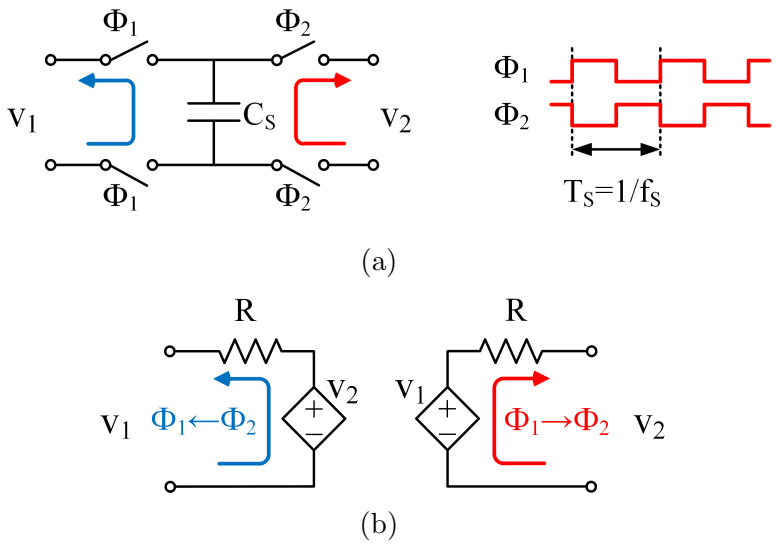


Figure 2.11: a) Two-phase switched-capacitor topology with non-grounded sampling capacitor and b) its proposed continuous-time model.

2.2.1 Theory

A two-phase switched-capacitor topology where both plates are non-grounded is shown in Fig. 2.11a. The average current flows into the port V_2 in one clock period, I_{A2}, can be written using charge balance equations as:

$$I_{A2} = \frac{\Delta Q}{T_S} = \frac{C_S.(V_1 - V_2)}{T_S} = (V_1 - V_2) f_S C_S \tag{2.10}$$

This current equation can be modelled using a voltage controlled voltage source (VCVS) whose value is equal to V_1, connected in series with an equivalent resistance of R with the value of $1/f_S C_S$. Another branch of VCVS and R is necessary to model the average current flowing into the port V_1 to complete the model, as shown in Fig. 2.11b. This model can be easily adapted to multi-phase switched-capacitor structures by merely increasing the number of VCVS + R branches, similar to the approaches in Section 2.1. Then, the number of VCVS + R branches should be equal to the number of clock phases in the topology. A similar model for switched-capacitor structures with two phases was also previously investigated [58]. (The derivation of the model for voltage

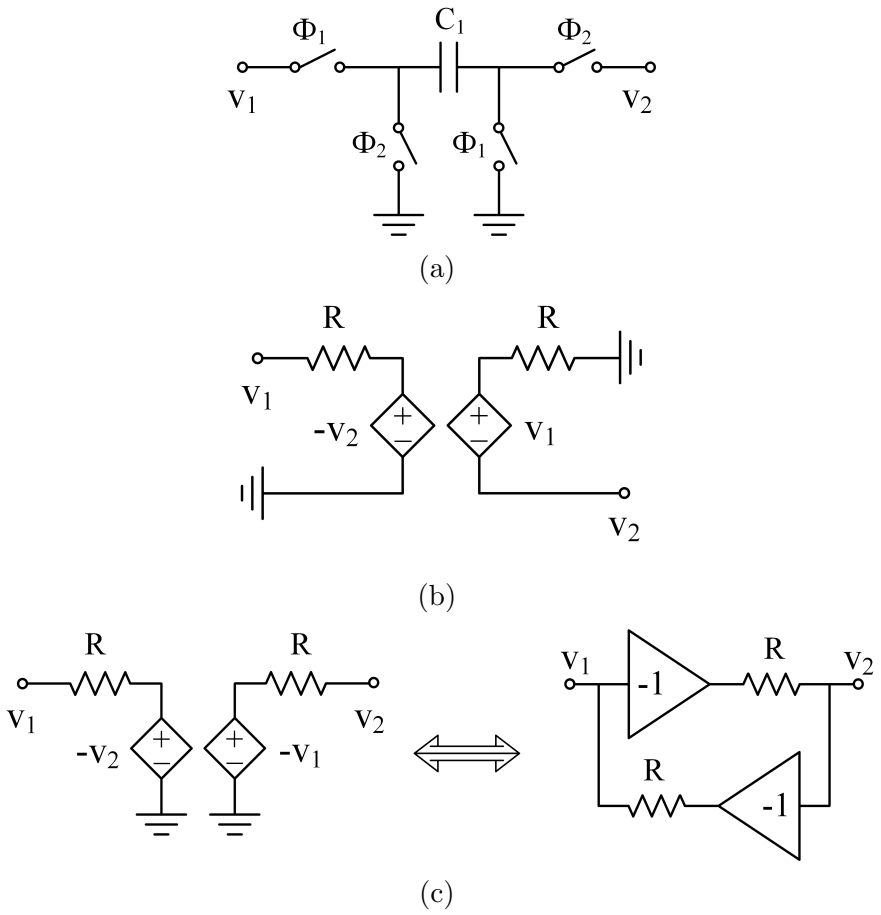


Figure 2.12: Parasitic insensitive switched-capacitor integrator a) switching parts, b) its continuous-time model, and c) rearranged continuous-time model.

sources with input frequencies much smaller than the sampling frequency is similar to the proofs given in Appendices A and B.)

2.2.2 Examples

Parasitic Insensitive Switched-Capacitor Integrator

The generalized continuous-time model can be used to analyze the parasitic-insensitive switched-capacitor integrator with a non-grounded sampling capacitor. Fig. 2.12a shows the switching parts of the integrator, where V_1 corresponds to the input voltage, and V_2 corresponds to the virtual ground of the amplifier shown in Fig. 2.10a.

In Φ_1, C_1 is connected between V_1 and ground nodes; this sampled voltage value,

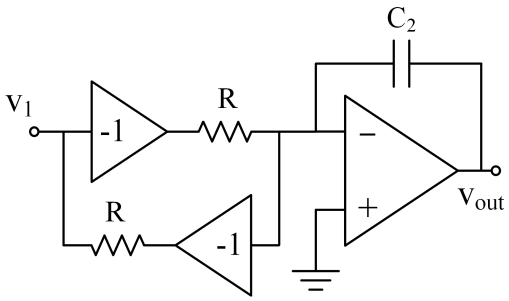


Figure 2.13: The continuous-time model of the parasitic insensitive switched-capacitor integrator.

$(V_1 - 0)$, becomes the value of the VCVS on the second branch (Fig. 2.10b). Whereas during Φ_2, C_1 is connected between ground and V_2 nodes. Thus, the VCVS value in the first branch becomes $-V_2$. Since there exist two ground nodes, it is possible to rearrange the continuous-time model, as shown in Fig. 2.12c, where VCVSs can be shown by ideal inverting voltage buffers to have a more intuitive schematic. Fig. 2.13 shows the parasitic insensitive integrator, where the switching parts are replaced with the model.

It should be noted that this continuous-time SC integrator model can capture the correct sign of the voltage transfer function by the use of inverting voltage buffers rather than having a negative resistance. Furthermore, the model captures the correct input current direction. Thus, it can also be used to analyze the effects of finite amplifier gain and offset voltages without resulting in a fictitious right-half plane pole.

Flying Capacitor DC/DC Converter

The switched-capacitor DC/DC converter structure shown in Fig. 2.14a can be analyzed using the differential continuous-time model to determine the Thévenin equivalent of the switching parts. This structure involves a flying capacitor, C, and large capacitors, C_M's for storing the DC value of the output voltage. The frequency of interest is much smaller than the sampling frequency [25, 26]. During ϕ_1, C is connected between V_{DD} and V_{out} nodes, sampling a voltage of $V_{DD} - V_{out}$. Whereas, during ϕ_2, C is connected between V_{out} and the ground node sampling a voltage of $V_{DD} - 0$ across itself. The top

left schematic in Fig. 2.14b shows the differential switched-capacitor continuous-time model, where $R = 1/f_S C$. It is possible to further simplify the continuous-time structure by starting from the initial model and obtaining the Thévenin equivalent circuit shown in Fig. 2.14c. In order to find v_{out} from $2v_{out}$, the open circuit voltage, V_{DD}, and the output resistance, $R/2$, are divided by half. The conventional approach is to use a DC transformer model, as shown in Fig. 2.14d [26]. The conversion ratio, (m:n), and the output resistance, R_{OUT}, can be calculated to be the same as Fig. 2.14c. However, this approach is not intuitive, and the derivation is cumbersome.

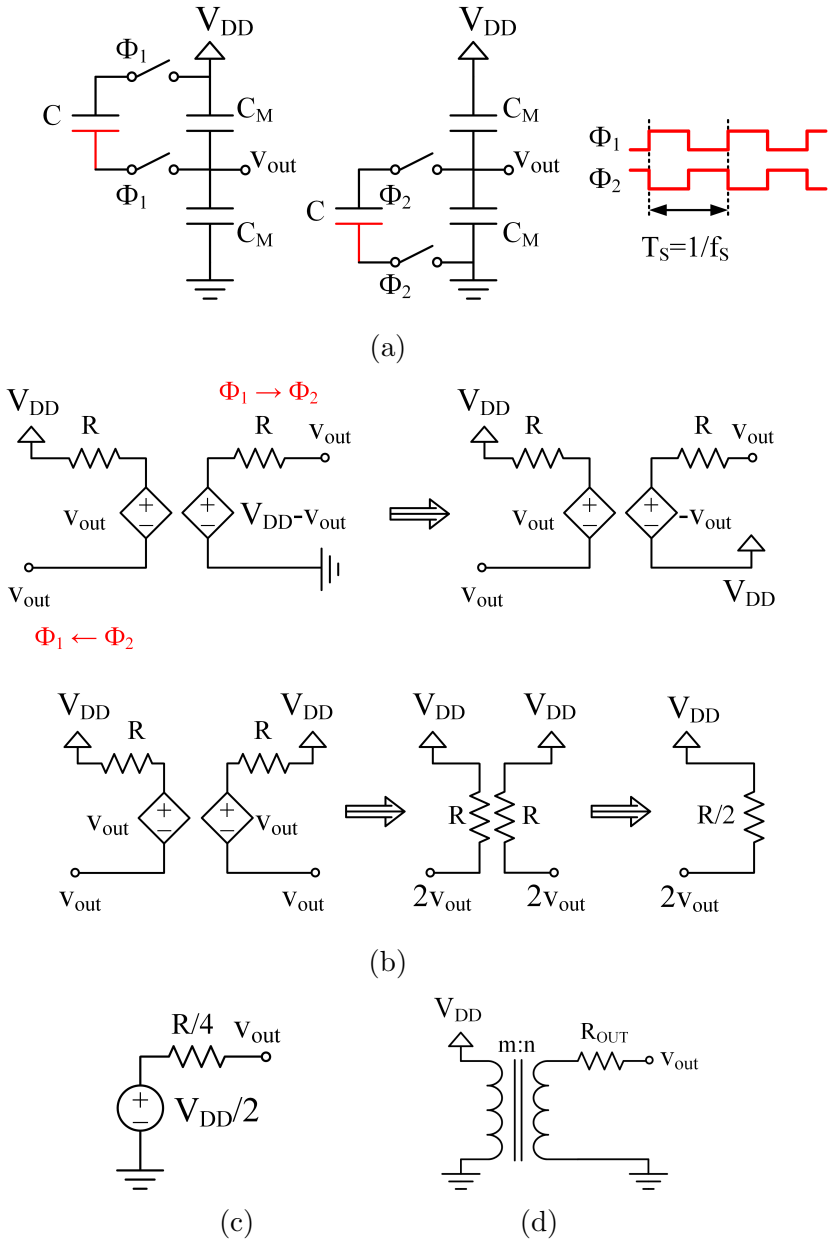


Figure 2.14: a) Switched-capacitor DC/DC voltage converter, b) its simplified continuous-time model, c) the Thévenin equivalent of v_{out} obtained with the continuous-time model, d) conventionally used switched-capacitor converter transformer model.

Chapter 3

Complex-Conjugate Poles using Switches and Capacitors

The proposed continuous-time model offers an intuitive understanding of oversampled switched-capacitor topologies. The intuition provided by the continuous-time approach can also be used to develop new switched-capacitor topologies. In this section, complex-conjugate poles are realized using passive switched-capacitor networks with the help of the continuous-time approach.

3.1 Passive Switched-Capacitor Butterworth Biquad

3.1.1 From Real Poles to Complex-Conjugate Poles

It is well known that passive RC networks can only form real poles [7]. Similarly, the creation of complex-conjugate poles in switched-capacitor circuits generally involves the use of active components to create a feedback loop able to move the real poles in the complex plane. In this section, it is shown that such a feedback loop can be created with a passive switched-capacitor network by exploiting time-variance and unilaterality highlighted by the proposed model.

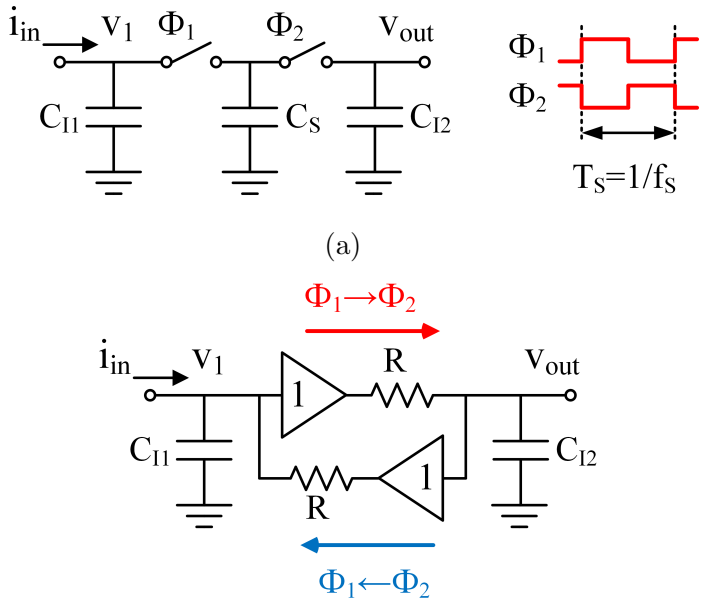


Figure 3.1: a) Passive switched-capacitor filter with two real poles and b) its continuous-time model.

In Fig. 3.1a, a switched-capacitor low-pass filter with two real poles is shown. Although, in this case, two switches and the sampling capacitor, C_S, could be substituted by a simple resistor, the proposed continuous-time model is used to highlight the presence of a virtual loop (Fig. 3.1b).

The real poles of the circuit shown in Fig. 3.1b can be transformed into complex-conjugate ones just by inverting the gain of the buffer in the return path (Fig. 3.2). This inversion creates a non-reciprocal network with a feedback path, which makes it possible to obtain complex-conjugate poles. These new poles have a natural oscillation frequency (ω_0) and a quality factor (Q) given by:

$$\omega_0 = \frac{\sqrt{2}}{R\sqrt{C_{I1}C_{I2}}} \tag{3.1}$$

$$Q = \frac{\sqrt{2C_{I1}C_{I2}}}{C_{I1}+C_{I2}} \leq \frac{1}{\sqrt{2}} \tag{3.2}$$

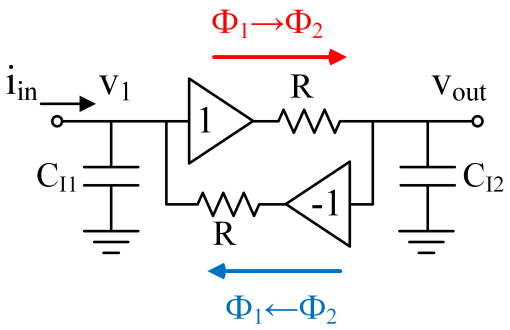


Figure 3.2: Low-pass filter with complex-conjugate poles involving a negative feedback loop.

When Q becomes greater than 0.5 (assuming a C_{I1}/C_{I2} ratio in between 0.17 and 5.83), poles become complex-conjugate. For $C_{I1} = C_{I2}$, Q reaches its maximum value of $1/\sqrt{2}$ that corresponds to a 2^{nd}-order Butterworth filter transfer function. The reason for an upper bound in the achievable Q is due to the loop gain being limited to 1 in the given structure.

3.1.2 Implementation of the Passive Switched-Capacitor Filter

At this point, we have the continuous-time model of the filter with 2^{nd}-order Butterworth characteristics. How can we transfer this idea from the continuous-time model to an actual discrete-time filter implementation? One way to create the inverting behaviour is to use a differential structure, where the charge of the sampling capacitor, C_S, is cross-transferred between positive and negative terminals. This operation can be realized by the circuit shown in Fig. 3.3 based on four phases, two of which are labeled as ϕ_1 and ϕ_2, and two of which are labeled negatively as ϕ_{1N} and ϕ_{2N}. During ϕ_1 and ϕ_2 phases, the circuit behaves like Fig. 3.1a, while during the negative phases, charge inversion is obtained. The output is sampled on both ϕ_2 and ϕ_{2N}. Thus, the circuit behaves as a two-phase system from the output perspective. This topology is similar to the one obtained in [44], where, however, four sampling capacitors are used.

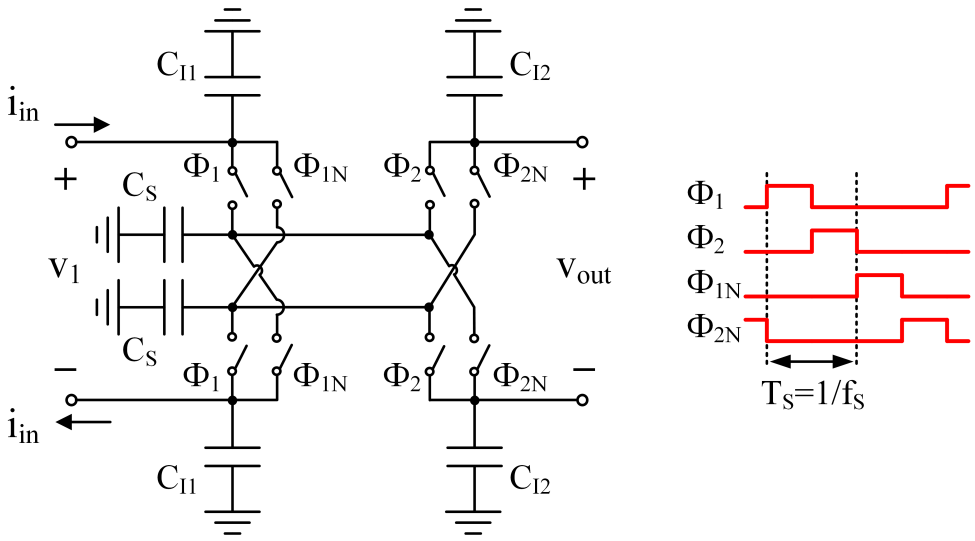


Figure 3.3: Differential 2^{nd}-order passive switched-capacitor filter with complex-conjugate poles.

Sanity Check with Four-Phase Continuous-Time Model

The filter shown in Fig. 3.3 has four phases and a cross-coupled structure. At first glance, it is not easy to verify the filter's operation and intuitively understand that the filter can give the desired characteristics dictated by the continuous-time model shown in Fig. 3.2. However, by applying the proposed model, the four-phase filter can be transformed into a continuous-time topology as a sanity check. A continuous-time model can be built by using buffer + resistor branches corresponding to each phase change ($\phi_1 \rightarrow \phi_2, \phi_2 \rightarrow \phi_{1N}, \phi_{1N} \rightarrow \phi_{2N}, \phi_{2N} \rightarrow \phi_1$) as shown in Fig. 3.4a. The resistance value, R, is equal to $1/(f_S C_S)$, where f_S is defined for two phases, as the output is sampled at every two phases. This model can be simplified by merging parallel branches (Fig. 3.4b). Moreover, cross-coupled buffer branches can be replaced with inverter branches to obtain Fig. 3.4c, since the circuit operation is differential. Fig. 3.4c is the fully differential version of the circuit reported in Fig. 3.2. It should be noted here that if the common-mode analysis is required, cross-coupled branches should be left as they are (Fig. 3.4b).

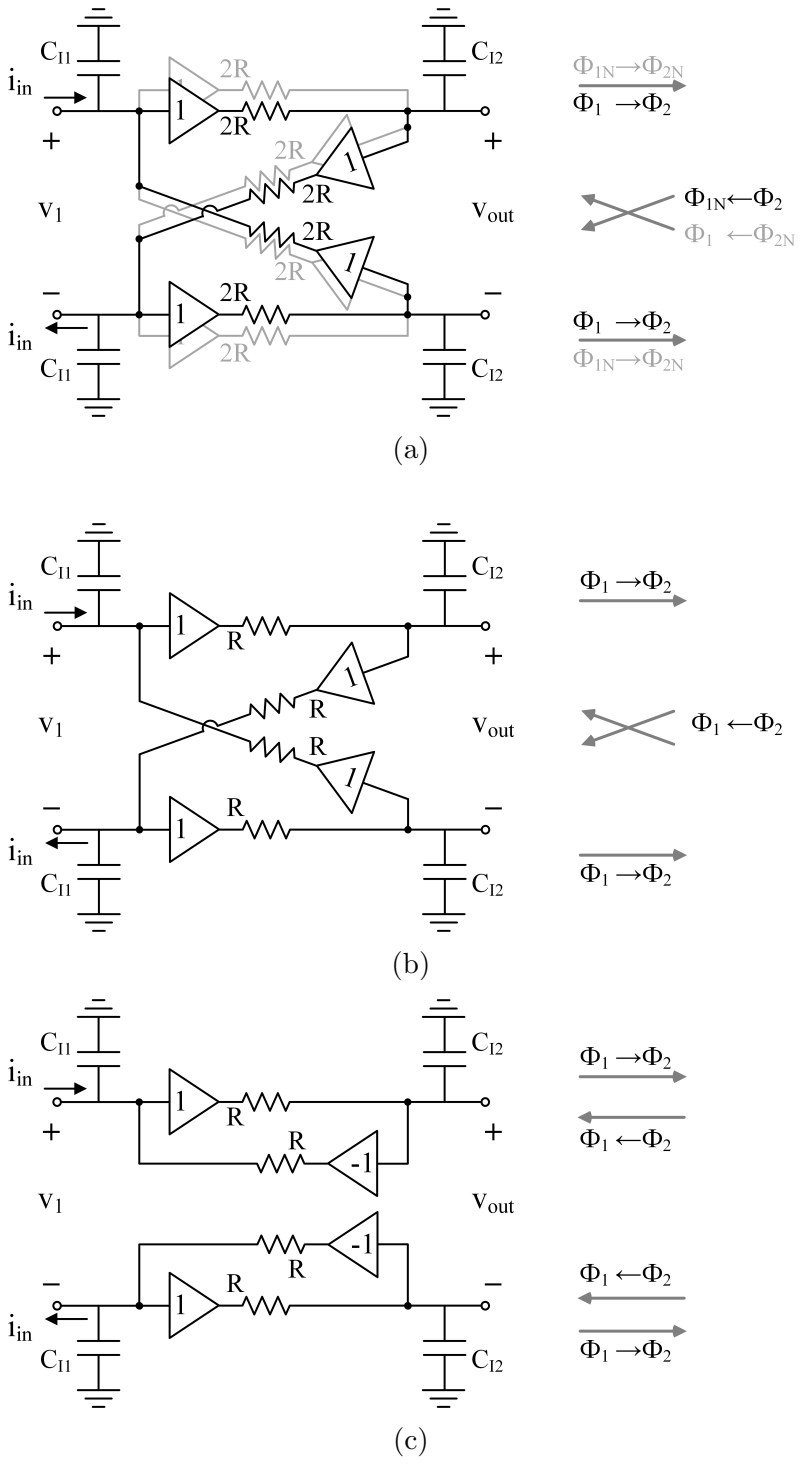


Figure 3.4: Differential 2^{nd}-order Butterworth biquad continuous-time model: a) Direct representation of four phases, b) with parallel branches merged, c) cross-coupled buffers are replaced by inverter branches.

Conventional Discrete-Time Analysis

The pole locations of the differential 2^{nd}-order Butterworth passive switched-capacitor filter can be found by first deriving the filter transfer function in the z-domain and later obtaining the s-domain transfer function by using the bilinear approximation. The z-domain transfer function can be derived by writing the charge-domain equations as follows:

$$\begin{aligned}(C_{I1}+C_S)V_1\left[n-\frac{1}{3}\right] =& C_{I1}V_1\left[n-\frac{4}{3}\right]-C_SV_{out}+Q_{in}[n]\\ (C_{I2}+C_S)V_{out}[n] =& C_{I2}V_{out}[n-1]+C_SV_1\left[n-\frac{1}{3}\right]\\ \text{where } Q_{in}[n] =& \int_{(n-1)T_S}^{nT_S} g_mV_{in}(t)dt\end{aligned} \tag{3.3}$$

where n represents the sampled value at the end of ϕ_2. The resulting z-domain transfer function can be written as:

$$\frac{V_{out}(z)}{Q_{in}(z)}=\frac{z^2[\frac{C_S}{(C_S+C_{I1})(C_S+C_{I2})}]}{z^2-z[\frac{C_{I1}(C_S+C_{I2})+C_{I2}(C_S+C_{I1})-C_S^2}{(C_S+C_{I1})(C_S+C_{I2})}]+\frac{C_{I1}C_{I2}}{(C_S+C_{I1})(C_S+C_{I2})}} \tag{3.4}$$

ω_0 and Q of the filter can be determined by using the bilinear approximation, $z=\frac{1+sT_S/2}{1-sT_S/2}$, as follows:

$$\omega_0 =\left.\frac{2f_SC_S}{\sqrt{C_{I1}C_S+C_{I2}C_S+2C_{I1}C_{I2}}}\right|_{C_{I1,I2}\gg C_S/2}\approx\frac{\sqrt{2}}{R\sqrt{C_{I1}C_{I2}}} \tag{3.5}$$

$$Q =\left.\frac{\sqrt{C_{I1}C_S+C_{I2}C_S+2C_{I1}C_{I2}}}{C_{I1}+C_{I2}+C_S}\right|_{C_{I1,I2}\gg C_S/2}\approx\frac{\sqrt{2C_{I1}C_{I2}}}{C_{I1}+C_{I2}}\leq\frac{1}{\sqrt{2}} \tag{3.6}$$

The calculated s-domain ω_0 and Q of the discrete-time filter become the same as the values derived by the continuous-time model in Eqn. 3.1 and 3.2 under the assumption of $C_{I1,I2}\gg C_S/2$.

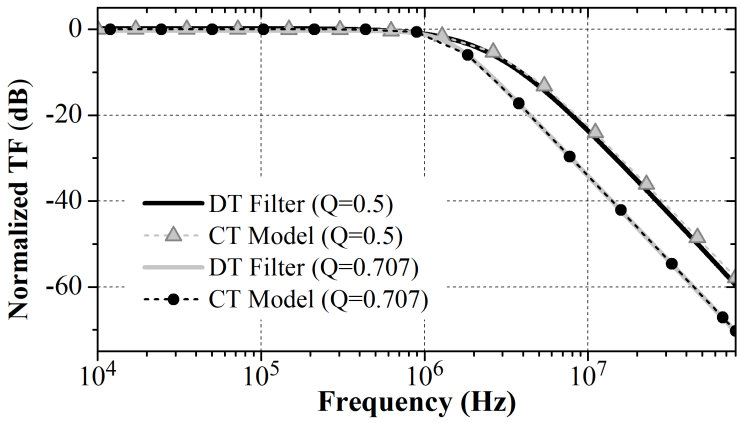


Figure 3.5: Simulated magnitude responses for $1dB$ droop at $1MHz$ with $f_S = 160MHz$ of the two-real-pole and 2^{nd}-order Butterworth biquads.

3.1.3 Filter Transfer Function Simulations

The 2^{nd}-order Butterworth passive switched-capacitor biquad, the two-real-pole passive switched-capacitor biquad (Fig. 2.6), and their continuous-time models were simulated in 65 nm CMOS technology by using SpectreRF periodic steady state (pss) and periodic AC (pac) analyses. A sampling frequency of $160MHz$ was chosen for a filter passband of $1MHz$. MOSFET transmission gates were used as switches with on resistances, R_{SW}, of $1k\Omega$ and off parasitic capacitance, C_{Prs}, of $1.8fF$.

The simulated normalized magnitude transfer function with $C_{I1} = C_{I2} = 3.56pF$ and $C_S = 400fF$ for the real-pole filter and that with $C_{I1} = C_{I2} = 5.14pF$ and $C_S = 200fF$ for the Butterworth filter are reported in Fig. 3.5. The small discrepancy between the proposed model and the switched-capacitor implementation is due to the parasitic capacitances of the transmission gates, which shift the expected pole frequencies and also the DC gain ($\propto 1/(f_S C_S)$) of the filters. Note that the Butterworth filter provides more than $10dB$ suppression for frequencies above $7MHz$ compared to the real-pole filter. This additional suppression is thanks to the Butterworth's complex-conjugate poles resulting in sharper band edge filtering characteristics.

3.1.4 Effect of Parasitic Capacitances

The switches and capacitors (C_I and C_S) introduce parasitic capacitances C_{Prs} to the circuit. The top and bottom-plate parasitic capacitances of each capacitor are added on itself. C_{Prs} associated with switches, on the other hand, are added both on C_I and C_S.

For both of the filters, any C_{Prs} that was added only on C_I shifts the desired pole locations. For the Butterworth filter, as long as C_{I1} and C_{I2} values change similarly, the Q value is not affected by the added C_{Prs} (Eqn. 3.2), whereas the C_{Prs} of the switches added on C_S limits the minimum value of C_S. Choosing smaller size switches results in lower C_{Prs}. However, switch size is also determined by the required switch resistance R_{SW}, where R_{SW} is limited by the settling error. For a lower settling error, R_{SW} should be small, which requires larger switches. Thus, there is a trade-off between the settling error and minimum capacitance value. Moreover, the C_{Prs} of the switches changes with the signal level and introduces nonlinearity for large signal amplitudes.

The 2^{nd}-order Butterworth filter and the two-real-pole biquad were simulated using Spectre pss and pac with two tones at 10 and $19MHz$ in order to compare their nonlinearity performances. The intermodulation tone was placed close to the filter cut-off. Switch capacitances were the primary source of nonlinearity since ideal g_m-cells were used. The out-of-band 3^{rd}-order input intercept point (IIP3) of the 2^{nd}-order Butterworth was simulated at $29dBm$, which compares favourably with the out-of-band IIP3 of the two-real-pole biquad that was simulated at $13dBm$.

3.1.5 Single Pole Passive Switched-Capacitor Complex Filter

It is interesting to note that the proposed filter structure with complex-conjugate poles shown in Fig. 3.3 is very similar to the complex filter shown in Fig. 3.6 with quadrature inputs and a single sampling capacitor. Fig. 3.6a shows the complex passive switched-capacitor filter reported by *Madadi et al.* that realizes a single complex pole by exploiting the in-phase (I), and quadrature (Q), i.e., 90° phase shifted input signals [8]. The current

input of the filter is defined as $i_{in} = i_{in,I} + j.i_{in,Q}$, whereas the voltage output of the filter is defined as $v_{out} = v_{out,I} + j.v_{out,Q}$ [8]. The filter has four phases during which C_S rotates in between positive and negative I and Q nodes.

To derive the filter transfer function (v_{out}/i_{in}), the continuous-time model can be developed as shown in Fig. 3.6b including four branches. Then, Kirchhoff's current law can be applied at the positive $V_{out,I}$ and $V_{out,Q}$ nodes:

$$i_{in,I} = \frac{v_{out,I}}{2}.sC_I + (\frac{v_{out,I}}{2} - \frac{-v_{out,Q}}{2})\frac{1}{R}, \quad i_{in,Q} = \frac{v_{out,Q}}{2}.sC_I + (\frac{v_{out,Q}}{2} - \frac{v_{out,I}}{2})\frac{1}{R} \quad (3.7)$$

where R is equal to T_S/C_S. By using Eqn. 3.7, it is possible to write the filter transfer function as follows:

$$(i_{in,I} + j.i_{in,Q}).2R = (v_{out,I} + jv_{out,Q})sRC_I + (v_{out,I} + jv_{out,Q}) + (v_{out,Q} - jv_{out,I}) \quad (3.8)$$

$$TF(s) = \frac{v_{out,I} + jv_{out,Q}}{i_{in,I} + j.i_{in,Q}} = \frac{2R}{sRC_I + 1 - j} \quad (3.9)$$

From Eqn. 3.9, the single complex pole of the filter can be written as $(-1+j)/RC_I$ rad/s. Fig. 3.7 shows simulated normalized transfer functions of the discrete-time passive switched-capacitor filter and the continuous-time model with a sampling frequency of $160MHz$, C_S of $200fF$, and C_I of $8pF$.

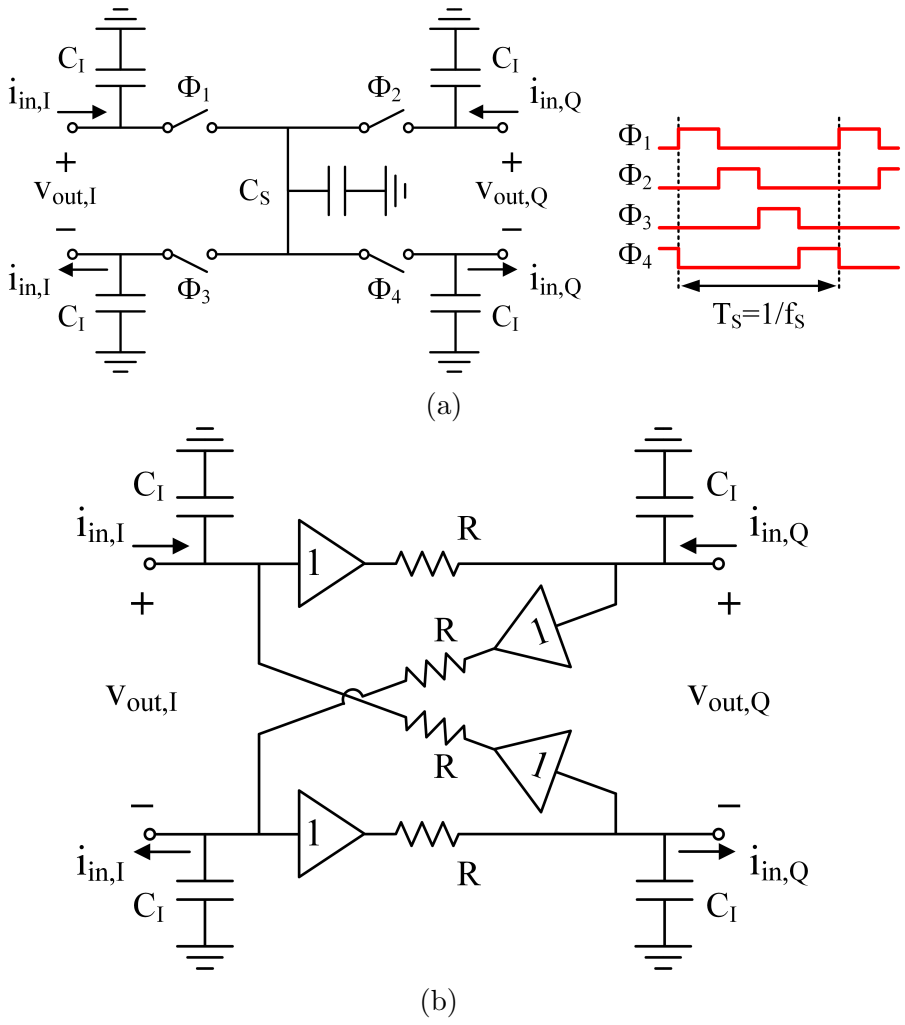


Figure 3.6: Single pole complex PSC filter a) discrete-time implementation [8] and b) its continuous-time model.

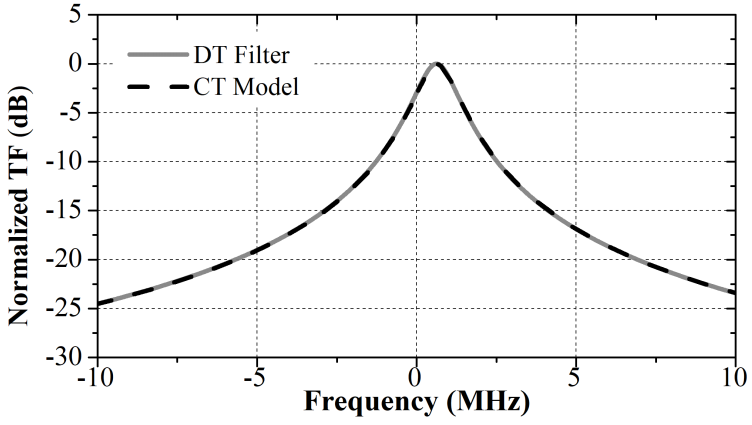


Figure 3.7: Simulated normalized frequency responses of PSC complex filter discrete-time implementation and its continuous-time model.

3.2 High-Order Filtering with Complex-Conjugate Poles

To achieve high-order low-pass filtering, designers traditionally cascade biquads having complex-conjugate pole pairs with different quality factors. However, for any filter order higher than 2, complex-conjugate poles with a quality factor greater than $1/\sqrt{2}$ are needed to generate for example Butterworth filter characteristics (the same is also valid for Chebyshev and Elliptic filters). However, this approach is not an option for the passive switched-capacitor biquad described in the previous section (Section 3.1) because the maximum achievable quality factor is limited to $1/\sqrt{2}$. One way to realize high-order filtering with larger than $1/\sqrt{2}$ quality factor is to use active devices, for example, g_m-cells, in the feedback path [5]. However, this solution increases the noise and adds non-linearity to the system along with the increased power consumption. Moreover, it may not be easy to scale the filter for newer technologies when we start to introduce active components. Thus, a new approach is needed to realize a sharp higher than 2^{nd}-order filtering characteristics implemented only with capacitors and switches.

3.2.1 Continuous-Time Design and Optimization

It is known that complex-conjugate poles can be generated by closing a feedback path around a cascade of stages with real poles. In Fig. 3.8, the feedback is realized by connecting the output of the cascade to the input through an inverting buffer and an equivalent resistance, R. This structure is also the N^{th}-order realization of the 2^{nd}-order Butterworth biquad filter reported previously in Section 3.1. Thanks to the continuous-time approach, it is easy to analyze how the number of branches affects the pole locations and changes the associated quality factors. To determine the pole locations, the transfer function of the filter shown in Fig. 3.8 can be written as follows:

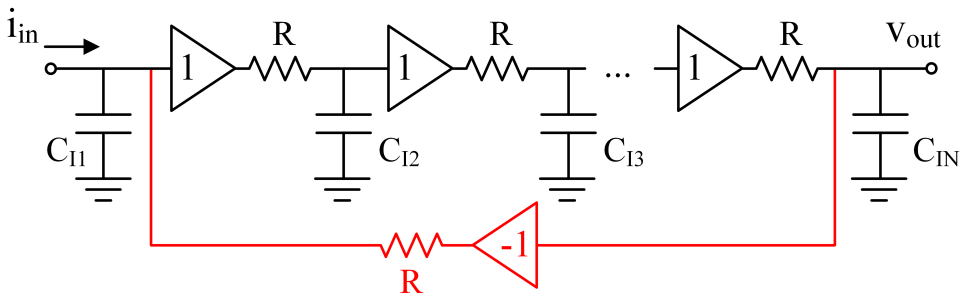


Figure 3.8: The proposed high-order low-pass PSC filter with complex-conjugate poles.

$$\frac{v_{out}(s)}{i_{in}(s)} = \frac{R}{(1+sRC_{I1})(1+sRC_{I2})(1+sRC_{I3})...(1+sRC_{IN})+1} \tag{3.10}$$

Fig. 3.9 shows the locations of the poles generated by a cascade of 2, 3, and 4 elements with the same valued C_I's for each stage. For a loop gain equal to one, which is the maximum achievable with a passive switched-capacitor network, the maximum quality factor is obtained starting from a cascade of real coincident poles, which demands identical C_I's. The generated poles have the same quality factors as the poles of a Butterworth filter but with different frequencies (Fig. 3.9). The shift in the pole frequencies leads to in-band peaking in the filter transfer function that increases with the order of the filter. A recent independent work decreases the feedback coefficient -1 to reduce the in-band peaking. However, this solution results in a smoother filter transfer function close to the band edge [54]. Actually, from Fig. 3.8, it can be observed that if the feedback coefficient -1 is decreased until 0, the resulting filter becomes the same as the previously discussed all real pole filter (Fig. 2.9b).

3.2.2 Implementation of the High-Order Passive Switched-Capacitor Filter

A 3^{rd}-order filter is chosen to be designed as it can approximate the Butterworth filter behaviour with less than $1dB$ in-band peaking. Fig. 3.10 shows the continuous-time

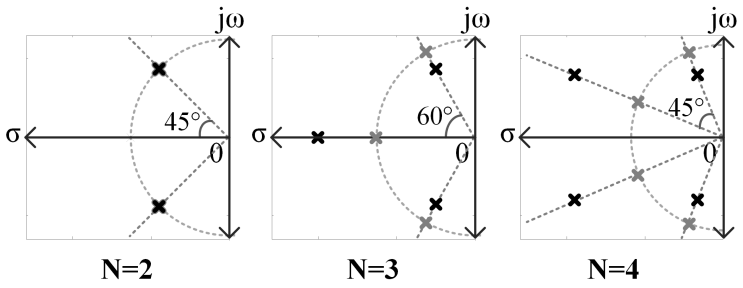


Figure 3.9: Pole locations of the 2^{nd}, 3^{rd}, and 4^{th} -order filters, where the gray circles mark the same order Butterworth pole locations having the same $1dB$ cut-off frequency.

model of the 3^{rd}-order filter. An example of a 3^{rd}-order implementation is shown in Fig. 3.11. In this filter, C_S shares charge with C_{I1}, C_{I2}, and C_{I3} in ϕ_1, ϕ_2, and ϕ_3, respectively, creating a unilateral signal flow. During the phase change from ϕ_3 to ϕ_1, C_S is flipped to create the negative feedback. Note that Fig. 3.10 also shows the related phase changes corresponding to each branch.

The pole locations derived from the model can be verified by evaluating the z-domain transfer function of the filter shown in Fig. 3.11 as follows (assuming equal C_I's for simplicity):

$$\frac{V_{out}(z)}{Q_{in}(z)} = \frac{1}{C_S}\frac{z^3(1-\alpha)^3}{(z-\alpha)^3 + z^2(1-\alpha)^3} \tag{3.11}$$

where α is $C_I/(C_I + C_S)$ and Q_{in} is the amount of charge fed into the filter in one sampling period, T_S. Although the network shown in Fig. 3.11 is periodic with $2T_S$, T_S is defined for three phases because the output is sampled in every three phases. The quality factor of the created poles can be found by mapping z-domain poles to s-domain using the bilinear approximation. As C_I/C_S ratio increases, Q of the complex-conjugate pair approaches to 1, which is the Q value predicted by the continuous-time model used for the synthesis of the filter.

Simulations of the proposed filter and the 3^{rd}-order Butterworth response (with the same DC gain and $1dB$ droop frequency) are compared in Fig. 3.12. Although the pole

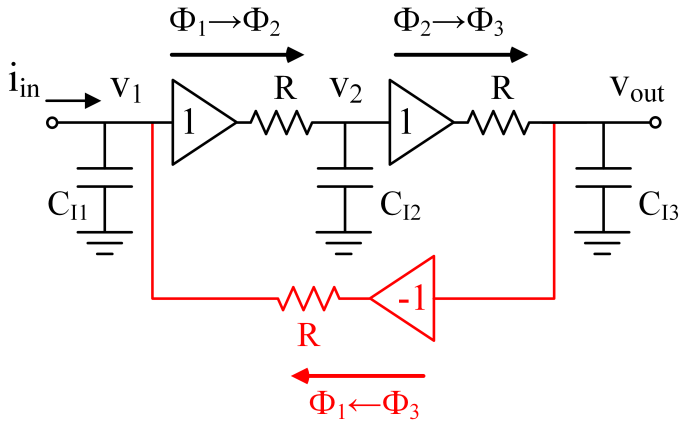


Figure 3.10: The continuous-time model of the 3^{rd}-order filter with complex-conjugate poles.

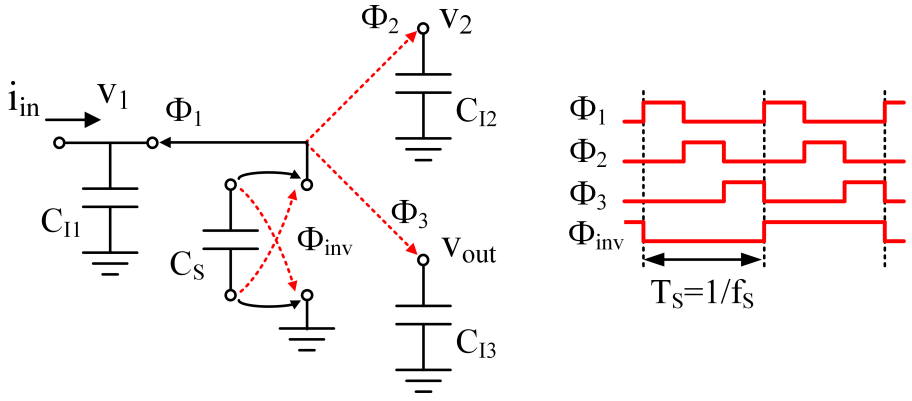


Figure 3.11: The PSC implementation of the 3^{rd}-order filter with complex-conjugate poles.

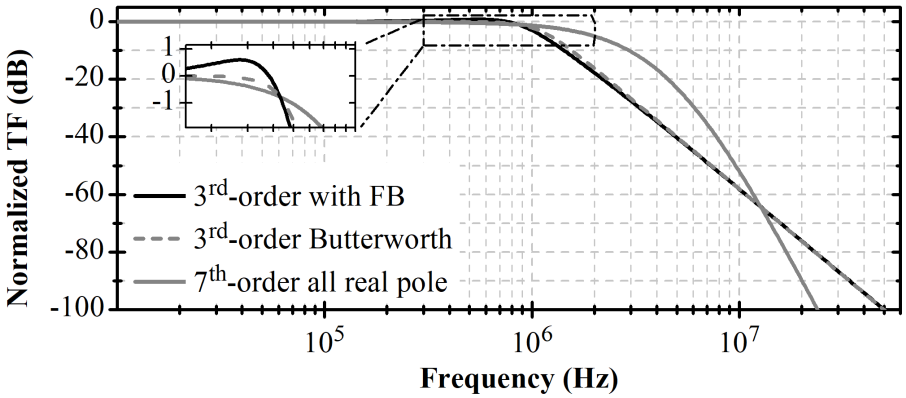


Figure 3.12: The transfer function of the PSC filter with complex-conjugate poles compared with the same order Butterworth and the 7^{th}-order real pole filter having the same $1dB$ droop frequency.

locations deviate from the ones of a Butterworth, the 3^{rd}-order filter maintains similar in-band flatness and selectivity. The figure inset shows that the response of the proposed filter deviates from the ideal Butterworth filter's response less than $1dB$ close to the filter band edge. Fig. 3.12 also compares the proposed solution with the 7^{th}-order all real pole passive switched-capacitor filter reported by Tohidian et al. [50] by assuming a maximum in-band drooping of $1dB$. Even though the proposed filter has a lower order, a higher selectivity is achieved over a decade close to the filter pass-band thanks to the presence of complex-conjugate poles.

Chapter 4

Noise Analysis and Practical Limitations of the Model

The proposed continuous-time model inherits the assumptions of the traditional two-phase switched-capacitor resistor equivalence: The driving node voltage should determine the voltage sampled by the sampling capacitor, C_S. As the sampling frequency goes to infinity, and the sampling capacitor value goes to zero, the equivalent resistor model works correctly. However, under practical conditions, limited settling time and charge sharing paths disturb this ideal behaviour. Moreover, as previously discussed in Chapter 2, the continuous-time model is only valid for input voltage sources with frequencies much smaller than the sampling frequency, i.e., for oversampled circuits. In this chapter, these limitations are studied to determine the accuracy of the proposed model when the conditions are only partially met.

4.1 Settling Time

A resistor in series with the sampling capacitor creates a non-zero time constant, which leads to settling error. This series resistance can be due to the switch on resistance or the source resistance. For a conventional switched-capacitor topology shown in Fig. 4.1,

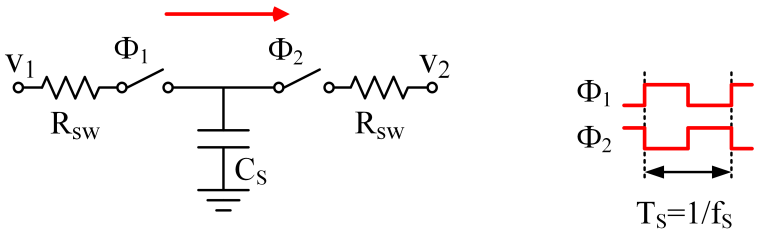


Figure 4.1: Basic two-phase switched-capacitor topology with series resistances.

when switches have on resistances of R_{SW}, the equivalent resistance seen can be derived as follows:

$$\begin{aligned} R =& \frac{V_1 - V_2}{I_A} = \frac{(V_1 - V_2)T_S}{\Delta Q} = \frac{(V_1 - V_2)T_S}{C\Delta V} \\ \text{with } \Delta V =& (V_1 - V_2)\frac{1 - e^{-\frac{1}{2f_S R_{SW} C_S}}}{1 + e^{-\frac{1}{2f_S R_{SW} C_S}}} \end{aligned} \tag{4.1}$$

$$R = \frac{1}{f_S C_S}\frac{1 + e^{-\frac{1}{2f_S R_{SW} C_S}}}{1 - e^{-\frac{1}{2f_S R_{SW} C_S}}} \tag{4.2}$$

where f_S is the sampling frequency and ΔV is the voltage difference on C_S between the end of ϕ_1 and the end of ϕ_2 phases. As R_{SW} goes to zero, R becomes $1/f_S C_S$, as expected. For example, if the settling time constant, $(R_{SW}C_S)$, is set to 15% of the sampling period, $1/f_S$, the error in the equivalent resistance becomes 7.40%, while if the time constant is set to 5% of the sampling period, the accuracy becomes 0.01%.

One way to relax this problem without requiring a higher clock frequency is to increase the sampling frequency of the switched-capacitor by introducing time-interleaved stages [46], as done in the presented prototype described in Chapter 5.

While the maximum clock frequency is limited due to the settling time of the switched capacitor circuit, the model's accuracy increases as the oversampling rate increases. Specifically, in the case where the clock frequency is fixed and satisfies the settling time requirement, then as the oversampling rate increases, the filter's bandwidth decreases and the accuracy of the model improves. However, a practical limitation here is that as

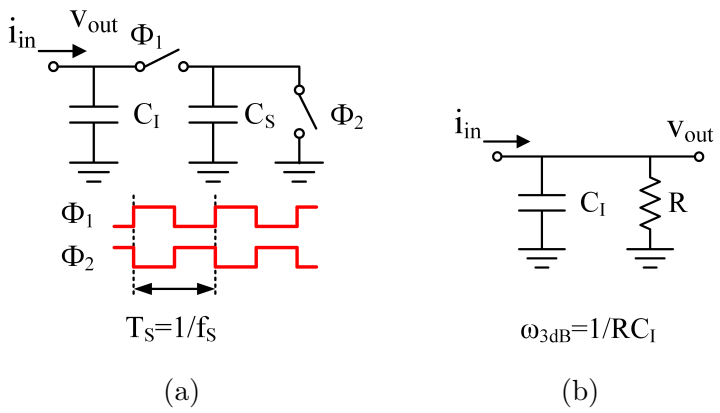


Figure 4.2: a) 1^{st}-order PSC filter and b) its continuous-time model with the traditional equivalent resistance approach [2].

the oversampling rate increases, the ratio of the sampling capacitors to the integrating capacitors will decrease and may lead to unreasonably small sampling capacitors.

4.2 Charge Sharing

In the case C_S is connected to a capacitive driving impedance, there is an issue of charge sharing between two capacitors that leads to an error in the equivalent resistor behaviour. For example, Fig. 4.2a shows the 1^{st}-order passive switched-capacitor filter with current input and voltage output, where C_S is switching between an integrating capacitor, C_I, and a ground node. As mentioned in Chapter 1, C_I capacitor can be treated as a voltage source for C_I values much larger than C_S, and thus the switching parts can be replaced by an equivalent resistor with a value of $1/f_S C_S$ (Fig. 4.2b). However, when C_S becomes comparable to the driving impedance, C_I, the charge stored in C_S is not an accurate representation of the initial voltage on C_I. Moreover, the pole created (proportional to C_S/C_I) moves toward the higher frequencies, where the model accuracy is limited.

It is possible to investigate the continuous-time model accuracy for this 1^{st}-order passive switched-capacitor filter. Fig. 4.3 shows the frequency transfer functions simulated using SpectreRF periodic steady state and periodic AC analyses for a sampling frequency

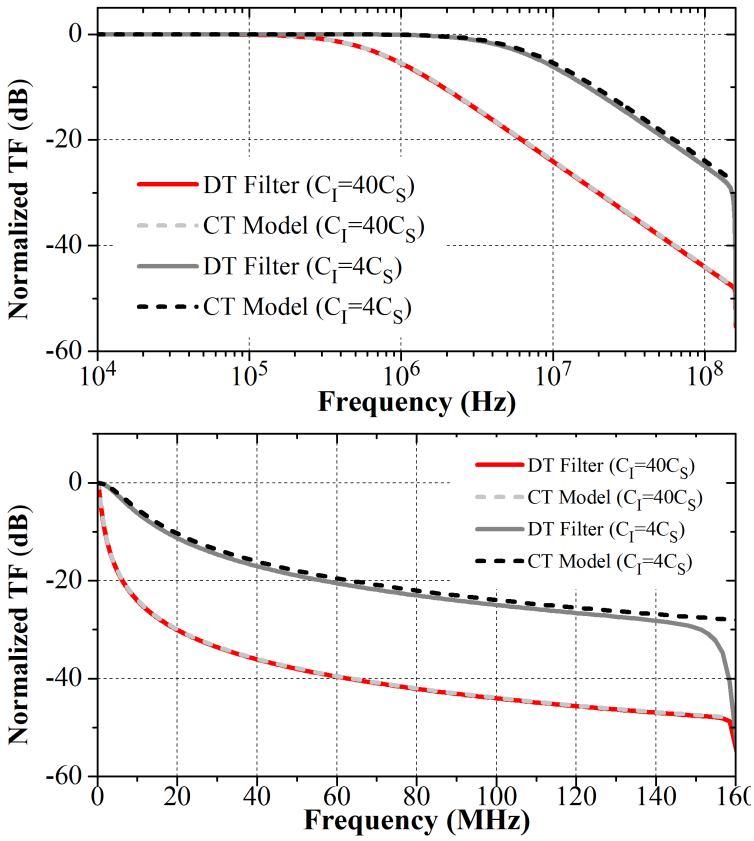


Figure 4.3: 1^{st}-order PSC filter discrete-time implementation and continuous-time model simulated frequency responses for $C_I/C_S = 40$ and $C_I/C_S = 4$ with logarithmic and linear scale frequency axes.

of 160 MHz, $C_S = 200fF$, and with C_I/C_S ratios of 40 and 4. For $C_I/C_S = 40$, the error in the 3dB cut-off frequency is 1%, whereas for $C_I/C_S = 4$ the error becomes 12%. (The notch at f_S is due to the inherent anti-aliasing property of the integration sampler [2].)

Fig. 4.5 shows the percentage error in the simulated $3dB$ cut-off frequency for changing C_S/C_I and f_{3dB}/f_S ratios. In Fig. 4.5a, the error approximately follows $C_S/2C_I$ for lower values of C_S/C_I, and as C_S becomes comparable to the driving impedance, C_I, the model accuracy decreases. For Fig. 4.5b, the error increases, as f_{3dB} becomes closer to the sampling frequency, f_S.

Fig. 4.4 shows the simulated step response of the PSC filter discrete-time implementation and the continuous-time model for C_I/C_S ratios of 40 and 4. The bottom plot shows the difference between the discrete-time implementation sampled and the

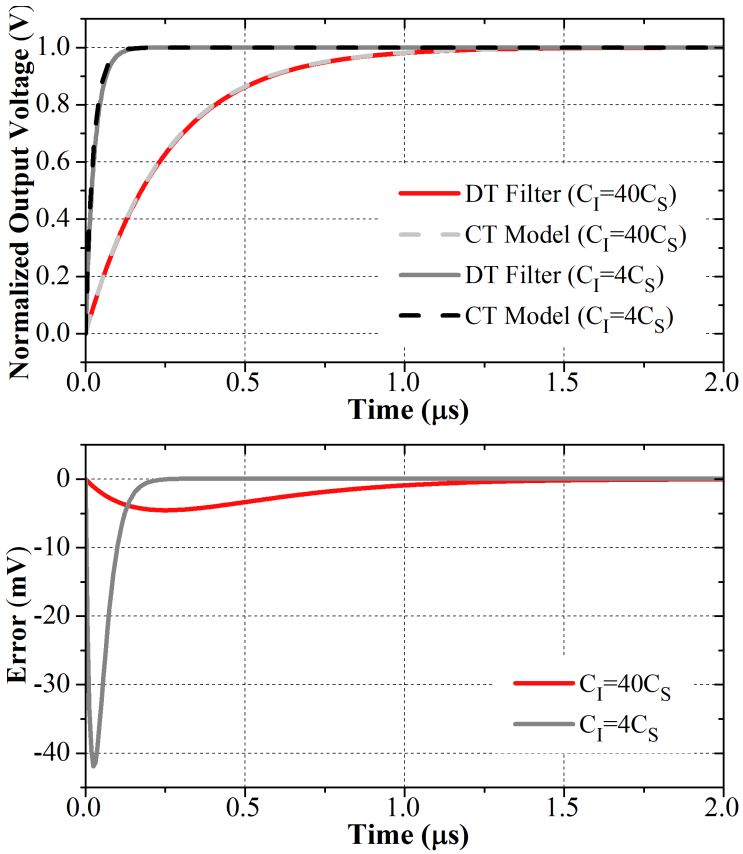
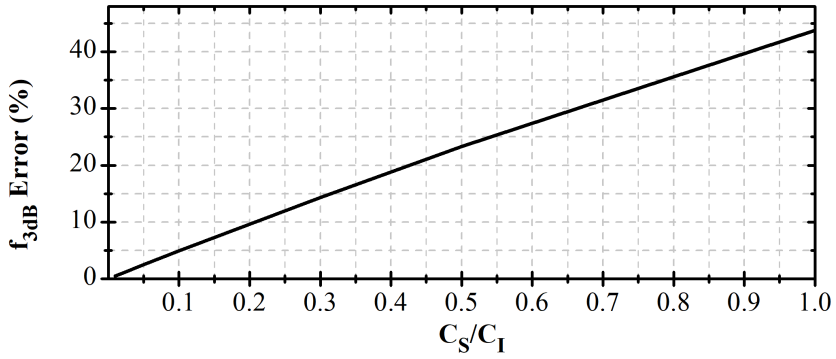


Figure 4.4: 1^{st}-order PSC filter discrete-time implementation and continuous-time model simulated step responses for $C_I/C_S = 40$ and $C_I/C_S = 4$.

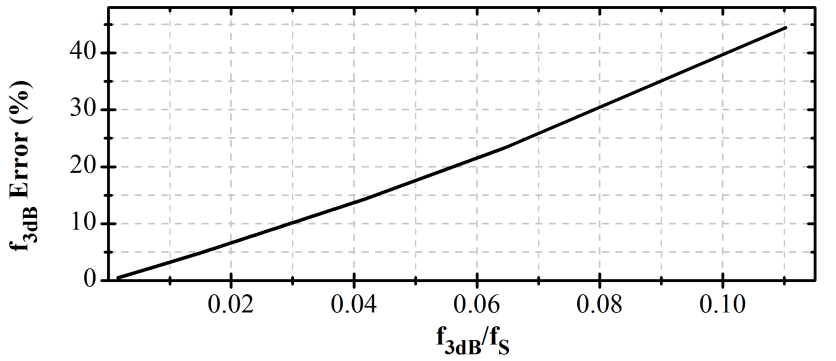
continuous-time model responses. The error is dominant during the initial transient phase, which corresponds to the high-frequency response with limited model accuracy. As the step response settles, i.e., for the DC response, error approaches to zero. As expected, the error is smaller for the C_I/C_S ratio equal to 40, when the model accuracy is better.

4.3 Accuracy of the Model in PSC Filter Response

The continuous-time model is valid for bandlimited sources with frequencies much smaller than the sampling frequency. However, it is shown that passive switched-capacitor filter frequency responses obtained using the continuous-time model closely follows the discrete-time analysis up to Nyquist frequency, $f_S/2$, as long as the pole frequencies are much



(a)



(b)

Figure 4.5: Error in the $3dB$ cut-off frequency calculation of a 1^{st}-order PSC filter using the continuous-time model for changing a) C_S/C_I and b) f_{3dB}/f_S ratios.

smaller than the sampling frequency [57, 59]. An example of this behaviour can also be seen in Fig. 4.3, where even at frequencies close to the sampling frequency of $160MHz$, the $-20dB/dec$ slope of the 1^{st}-order filtering profile continues. This is because when the model accuracy starts to decrease at higher frequencies, the dominant impedance is determined by the large integrating capacitors present in the system. As $C_I \gg C_S$ and $f_{3dB} \ll f_S$, the model can predict the pass-band gain and the pole frequency with high accuracy. For the input frequencies closer to $f_S/2$, i.e., for frequencies higher than the pole frequency, C_I impedance starts to be the dominant impedance determining the overall frequency response. Thus, although at those frequencies the continuous-time model of the switching parts is not accurate, the continuous-time model of the filter results in the correct transfer function.

4.4 Noise Analysis and Simulation Using the Model

The proposed continuous-time model can also be used to analyze noise without the need for complex discrete-time charge balance analysis like the one used in [3]. The noise introduced by each buffer + resistor branch, i.e., in each phase change, is equal to the noise associated with the equivalent resistance R_{Eqv} (i.e., $4kTR_{Eqv}$). However, since, in each phase change, two switches are involved, $4kTR_{Eqv}$ noise must be divided into two uncorrelated noise sources with a power spectral density equal to $2kTR_{Eqv}$. Furthermore, the noise created by the same switch in two consecutive phase changes must be represented by two correlated noise sources with inverse polarity. This inversion can be explained by considering the noise injected during a clock phase when a switch is conducting. When the switch is on, it connects two capacitors, which store the injected noise with opposite polarities, as shown in Fig. 4.6.

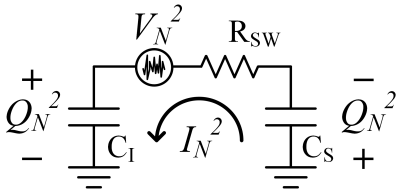


Figure 4.6: Correlated noise charge stored in two capacitors with opposite polarities.

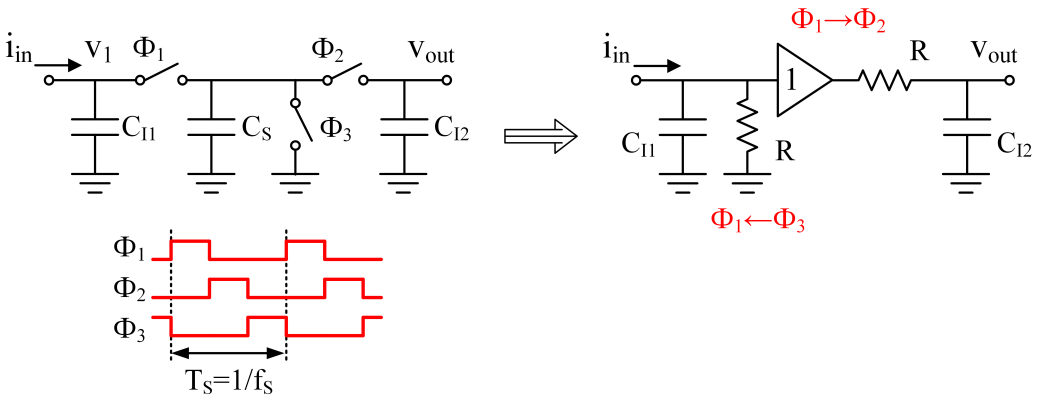


Figure 4.7: 2^{nd}-order PSC filter and its continuous-time model.

4.4.1 Examples

Passive Switched-Capacitor Low-pass Filter with Real Poles Analysis

As an example of the noise analysis, the 2^{nd}-order passive switched-capacitor filter with real poles is investigated. The filter's continuous-time model shown in Fig. 4.7 includes two resistors: one associated with the phase change from ϕ_1 to ϕ_2 and one associated with the phase change from ϕ_3 to ϕ_1.

Fig. 4.8 shows noise modelling. Each resistor is associated with two uncorrelated $2kTR_{Eqv}$ noise sources, which are generated by the switches that C_S is connected to during the three related phases. Note that the noise associated with the ϕ_1 switch appears in both of the branches, and the two ϕ_1 noise sources are fully correlated with inverse polarity. From the circuit in Fig. 4.8, the output noise spectral density can be written as follows:

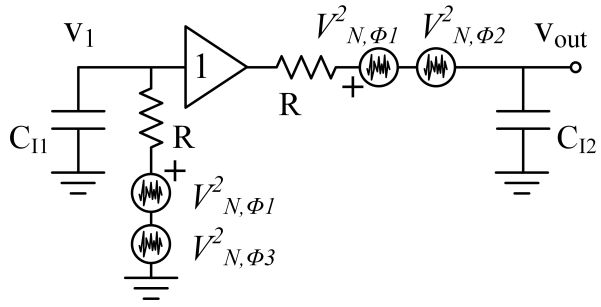


Figure 4.8: 2^{nd}-order PSC filter and its continuous-time model with noise sources, where the two ϕ_1 noise sources are fully correlated with inverse polarity.

$$V_{N,out}^2 = 2kTR_{Eqv}\Bigg[\overbrace{\left|\frac{1}{(1+j\omega R_{Eqv}C_{I1})(1+j\omega R_{Eqv}C_{I2})} - \frac{1}{1+j\omega R_{Eqv}C_{I2}}\right|^2}^{\phi_1} + \overbrace{\frac{1}{|1+j\omega R_{Eqv}C_{I2}|^2}}^{\phi_2} + \overbrace{\frac{1}{|1+j\omega R_{Eqv}C_{I1}|^2|1+j\omega R_{Eqv}C_{I2}|^2}}^{\phi_3}\Bigg] \tag{4.3}$$

There are a couple of interesting observations that can be extracted from this output noise spectral density equation. First of all, ϕ_1 switch does not contribute to the in-band noise spectral density, where $f < f_{3dB}$. Only ϕ_2 and ϕ_3 switches contribute to the output noise at those frequencies to a total value of $4kTR_{Eqv}$. ***Moreover, this observation can be extended to the all real pole high-order passive switched-capacitor filter shown in Fig. 2.9. The in-band noise spectral density is always equal to*** $4kTR_{Eqv}$ ***with equal contributions from*** ϕ_N ***and*** ϕ_{N+1} ***switches, where*** N ***is the filter order.*** Noise contribution from the other switches cancelled by inversely correlated noise sources in consecutive branches. This is also one of the advantages of the high-order charge-rotating passive switched-capacitor filter structure, i.e., as the filter order increases the noise contributions stays the same [4]. The second observation is that at higher frequencies, filter noise is dominated by the ϕ_2 and ϕ_1 switch noises, $2kTR_{Eqv}$ each, with a 1^{st}-order decaying behaviour. ***Again, this observation can be extrapolated for the*** N^{th}***-order filter, where dominant out-of-band noise***

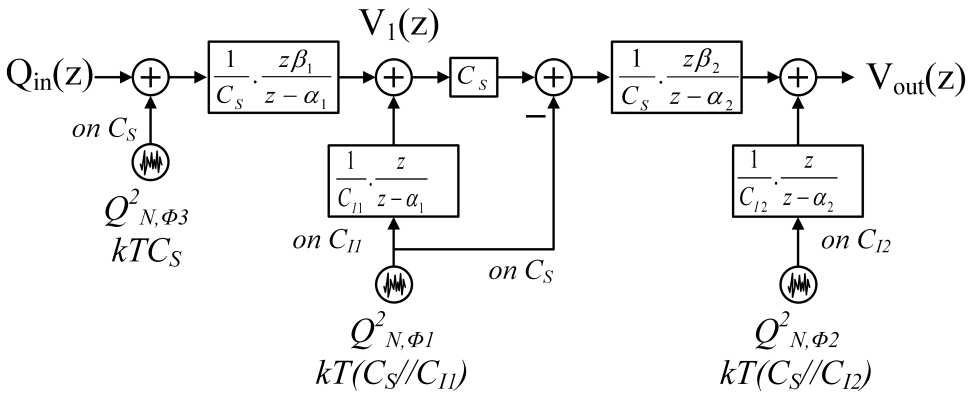


Figure 4.9: 2^{nd}-order PSC filter discrete-time noise analyzes signal flow diagram.

sources become the N^{th} ***and*** $N-1^{st}$ ***switches.***

Fig. 4.9 shows the discrete-time noise analysis signal flow graph for the 2^{nd}-order passive switched-capacitor filter with real poles [3, p. 237] (where $\alpha_i = C_{Ii}/(C_{Ii}+C_S)$ and $\beta_i = 1-\alpha_i$). It can be shown that the output noise spectral density obtained using the model is approximately equal to the value calculated using the discrete-time noise analysis when R_{Eqv} is replaced by $1/(f_S C_S)$.

Passive Switched-Capacitor Low-pass Filter with Real Poles Simulation

The continuous-time noise model can also be used for simulations. Especially for the design phase, the proposed noise modelling approach can shorten simulation times considerably.

Fig. 4.10 shows the schematic for the noise simulation. At first, noiseless resistors are used on the branches to generate two uncorrelated noise sources for a single resistor. Later, three separate noisy resistors are used to generate noise associated with each switch. Those noises are added to the model with the help of voltage controlled voltage sources. The polarity of the added noise sources only matters if the same noise source appears on more than one branches. In that case, it is important to reverse the polarity of the noise source on one of the consecutive branches. This inversion can be seen in between ϕ_1 noise sources in Fig. 4.10.

The model is simulated using ac noise analysis for $C_I = 8pF$ and $R = 1/(f_S C_S)$ with a sampling frequency of $160MHz$ and $C_S = 200fF$. The simulation took 1.06 seconds. Fig. 4.11 shows the simulated output noise spectral density, which closely follows passive switched-capacitor filter noise simulations.

Passive switched-capacitor noise simulations are performed using SpectreRF periodic steady state (pss) and periodic noise (pnoise) analyses [56]. Switches are implemented as ideal switches with resistors in series. Switch resistances are chosen to be $1.3k\Omega$, such that clock phase over settling time constant ($\sim R_{SW}.C_S$) ratio equals to 8, which leads to a low settling error of 0.03%. Although this simulation is mainly for verification purposes, choosing the switch resistance, R_{SW}, value is important. R_{SW} cannot be very large as that hurts the settling of the switched-capacitor. Also, for noise simulations, they cannot be too low. The reason is that to simulate the noise correctly for a sampled circuit, the folded noise should be accounted for correctly up to a couple of decades after the noise cut-off frequency ($1/2\pi R_{SW} C_S$). Thus, small R_{SW} values require long simulations times, or they may lead to incorrect results if simulation specifications entered poorly. With the given specifications, pss and pnoise simulations took around 12 minutes and 40 seconds. Compared to the previous 1.06 seconds, this simulation time is around 700 times longer (717 times longer to be exact), and with high-order filtering and time-interleaved structures, it can be even longer.

Table 4.1 shows the simulated spot noise contributions of each switch. 10 kHz and 6 MHz frequencies are chosen as values well below and well above the 3 dB cut-off frequency of the filter (410 kHz). Both ac noise and pnoise simulation results are aligned with the expected dominant noise sources.

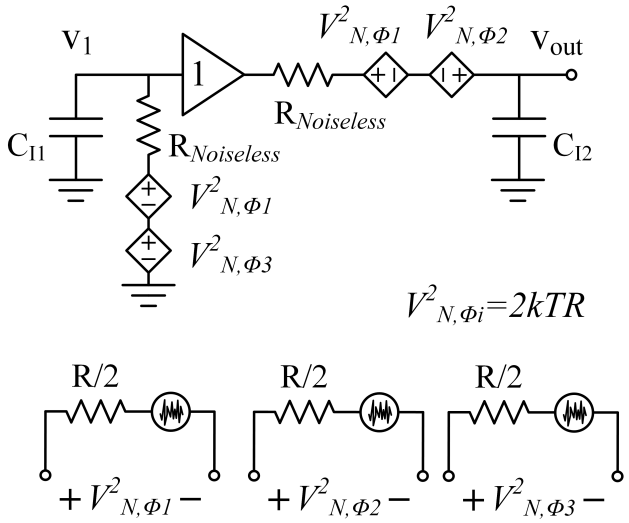


Figure 4.10: The continuous-time model of the 2^{nd}-order PSC filter for noise simulation.

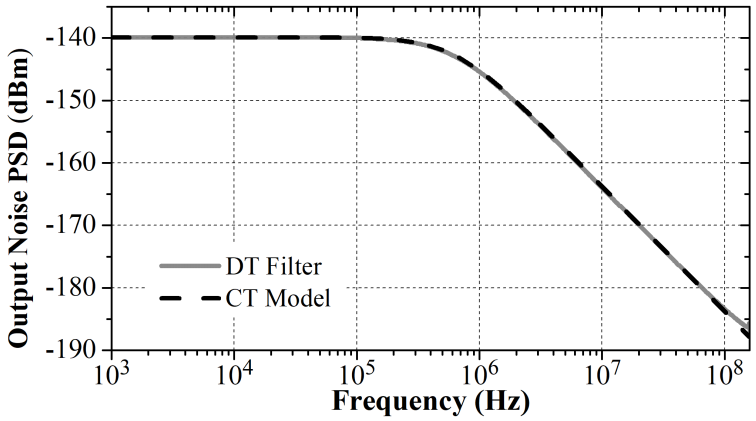


Figure 4.11: Simulated output noise power spectral densities of 2^{nd}-order PSC filter and its continuous-time model.

Table 4.1: Percentage spot noise contributions of switches.

	ac noise using CT model		pnoise using DT circuit	
	In-Band (10 kHz)	Out-of-Band (6 MHz)	In-Band (10 kHz)	Out-of-Band (6 MHz)
ϕ_1	0.01	49.44	0.01	49.09
ϕ_2	50.00	50.00	50.33	50.37
ϕ_3	49.99	0.56	49.66	0.54

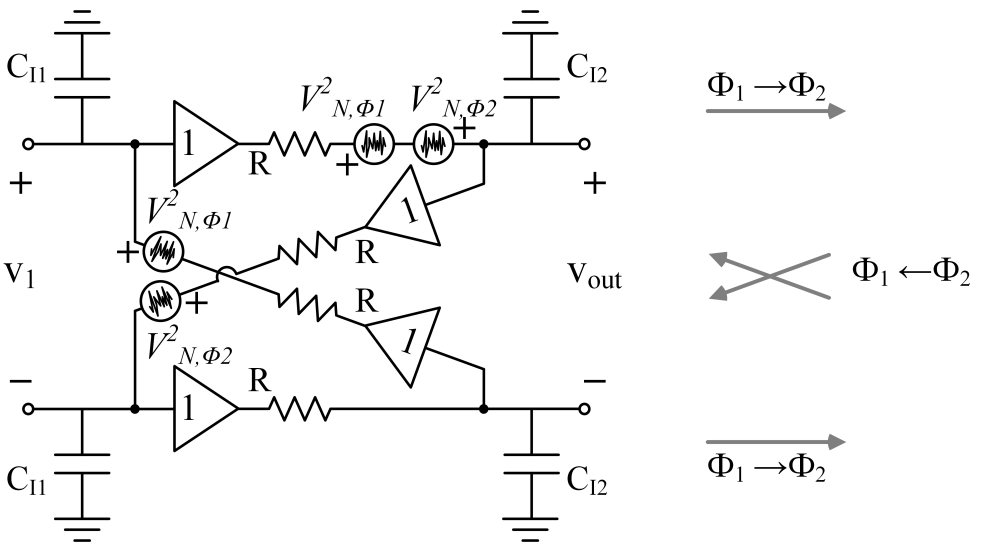


Figure 4.12: The 2^{nd}-order complex-conjugate-pole filter proposed model with noise sources, where noise sources associated with the same switch are fully correlated with inverse polarity.

Passive Switched-Capacitor Butterworth Filter Noise Analysis and Simulation

The noise analysis of the proposed 2^{nd}-order Butterworth biquad (Fig. 3.3) is performed by using the model in Fig. 4.12, which is developed as described in Section 4.4. Two of the four resistors presented in the model are associated with the phase change $\phi_1 \rightarrow \phi_2$ (for four-phase representation: $\phi_1 \rightarrow \phi_2$ or $\phi_{1N} \rightarrow \phi_{2N}$), and the other two resistors are associated with the phase change $\phi_2 \rightarrow \phi_1$ (for four-phase representation: $\phi_2 \rightarrow \phi_{1N}$ or $\phi_{2N} \rightarrow \phi_1$). Due to the differential nature of the filter, it is sufficient to investigate the noise associated with one of the ϕ_1 switches and one of the ϕ_2 switches. Later, the derived noise power can be multiplied by two to find the differential noise.

In Fig. 4.12, the noise sources associated with the ϕ_1 switch are placed in two consecutive branches that are connected to the V_1 positive terminal. Note that the two ϕ_1 noise sources are fully correlated with inverse polarity. Similarly, the noise sources associated with the ϕ_2 switch are placed in two consecutive branches that are connected to the V_{out} positive terminal. Note that the two ϕ_2 noise sources are fully correlated with inverse

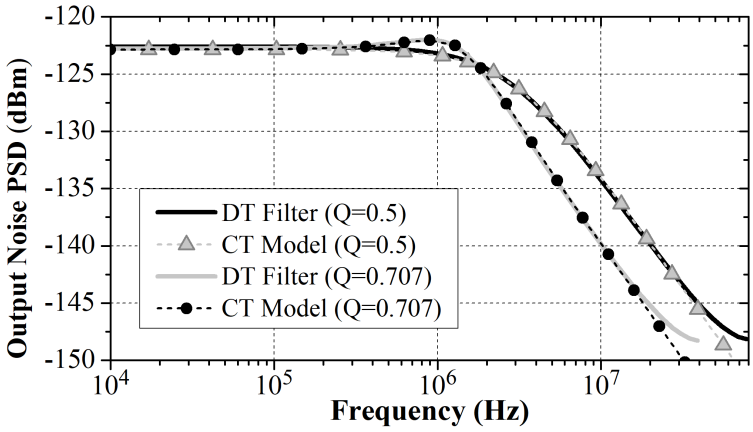


Figure 4.13: Simulated output noise spectral densities of the two-real-pole and 2^{nd}-order Butterworth biquads for $1dB$ droop at $1MHz$ with $f_S = 160MHz$.

polarity. Using Fig. 4.12, the noise analysis is straightforward, and the output noise spectral density can be written as follows:

$$V_{N,out}^2 = 2.2kTR_{Eqv}\left[\overbrace{\left|\frac{j\omega R_{Eqv}C_{I1}}{2-\omega^2 R_{Eqv}^2 C_{I1}C_{I2}+j\omega R_{Eqv}(C_{I1}+C_{I2})}\right|^2}^{\phi_1} + \overbrace{\left|\frac{2+j\omega R_{Eqv}C_{I1}}{2-\omega^2 R_{Eqv}^2 C_{I1}C_{I2}+j\omega R_{Eqv}(C_{I1}+C_{I2})}\right|^2}^{\phi_2}\right] \tag{4.4}$$

The coefficient 2 is added to include the effect of the differential switches' noise. It can be shown that, when R_{Eqv} is replaced by $1/(f_S C_S)$, the output noise spectral density obtained using the continuous-time model is approximately equal to the value calculated using discrete-time noise analysis.

The simulated output noise spectral densities are shown in Fig. 4.13 with both the two-real-pole biquad and the 2^{nd}-order Butterworth discrete-time biquad sized the same as in the previous subsection. For both the real-pole and Butterworth biquads, simulated noise spectral densities in the passband are approximately equal to each other. Moreover, the simulation results closely follow the calculation results.

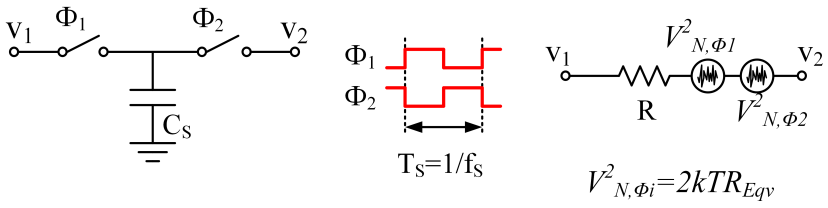


Figure 4.14: 2^{nd}-order PSC filter and its continuous-time model with noise sources, where two ϕ_1 noise sources are fully correlated with an inverse polarity.

Two-Phase Switched-Capacitor Structure

The proposed noise model can be applied to the conventional two-phase switched-capacitor structure. In this case, the model involves two uncorrelated noise sources, each having $2kTR_{Eqv}$ noise spectral density, as shown in Fig. 4.14. The resulting total $4kTR_{Eqv}$ noise spectral density value is different from the well-known $2kT/C$ integrated noise value of this structure. However, it is possible to reconcile these two values by calculating the noise spectral density over $0 - f_S/2$ bandwidth as below:

$$V_N^2 = \frac{2kT}{C}\frac{1}{f_S/2} = \frac{2kT}{C}\frac{2}{f_S} = \frac{4kT}{f_S C_S}\bigg|_{\frac{1}{f_S C_S}=R_{Eqv}} = 4kTR_{Eqv} \tag{4.5}$$

Chapter 5

Prototype Filter Design and Implementation

This chapter describes the implementation of a passive switched-capacitor filter prototype with complex-conjugate poles, whose theory was previously laid out in Chapter 3. The 3^{rd}-order filter has a transfer function resembling that of a Butterworth filter. To the author's knowledge with this prototype, for the first-time, switched-capacitor complex-conjugate poles were integrated on silicon without the need of any amplifier and only using switches and capacitors. Moreover, the proposed continuous-time model in Chapter 2 is verified with the provided measurement results.

5.1 Prototype Filter Differential Implementation

Chapter 3 described how complex-conjugate poles can be generated using only switches and capacitors. An example 3^{rd}-order low-pass filter implementation was also shown in Fig. 3.11. Due to practical purposes, a differential implementation is preferred for the prototype filter. A fully differential 3^{rd}-order passive switched-capacitor filter was designed and fabricated in 0.13 µm TSMC CMOS process.

Fig. 5.1 shows the passive switched-capacitor filter implementation. The charge

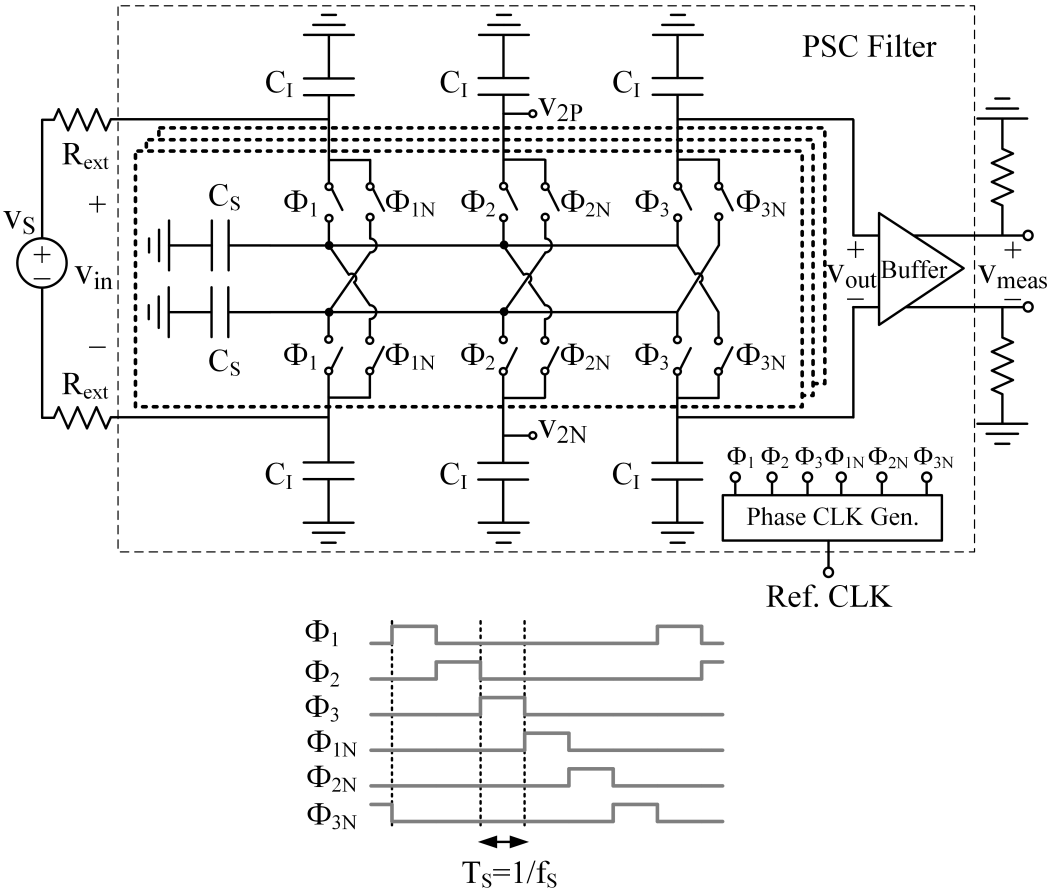


Figure 5.1: The fabricated 3^{rd}-order PSC low-pass filter schematic and the timing diagram.

inversion of C_S is realized by exploiting the differential structure and cross-coupling of positive and negative nodes. The filter uses six phases: Three non-inverting phases (ϕ_1, ϕ_2, and ϕ_3), when top C_S is connected to the top C_I's sequentially, while the bottom C_S is connected to the C_I's on the bottom differential side. During the following three inverting phases (ϕ_{1N}, ϕ_{2N}, and ϕ_{3N}), C_S's are connected to C_I's, on the opposite sides.

In order to increase the sampling rate, three time-interleaved blocks, which consist of C_S's and switches, are employed. Thus, the effective sampling period becomes the same as the period of a single phase.

The z-domain transfer function of the time-interleaved filter can be written as:

$$\frac{V_{out}(z)}{Q_{in}(z)} = \frac{2}{C_S} \frac{z(1-\alpha)^3}{(z-\alpha)^3 + (1-\alpha)^3} \tag{5.1}$$

where α is $C_I/(C_I + C_S)$, the coefficient 2 is due to the differential structure, and Q_{in} is the amount of charge that is fed into the filter in one sampling period. The z-domain transfer function reported in Eqn. 5.1 seems considerably different than the previously derived transfer function in Eqn. 3.11. The reason is that the sampling period, T_S, in Eqn. 5.1 is defined for a single phase due to the time-interleaved structure, whereas in Eqn. 3.11, T_S is defined for three phases. However, once mapped back to s-domain, it can be seen that Eqn. 3.11 and Eqn. 5.1 result in similar filtering characteristics for the same T_S.

The quality factor of the complex-conjugate pole pair can be calculated as 1 by mapping z-domain poles to s-domain using the bilinear approximation (assuming $C_I/C_S = 10$ and all C_I's are equal to each other). As C_I/C_S ratio increases, Q of the complex-conjugate pair approaches to 1. For a sampling frequency of $160MHz$, the filter $3dB$ bandwidth was designed to be $470kHz$. C_I's were chosen to be equal for a maximum Q. All capacitors, C_I's and C_S's, were used as MIM capacitors with values $12.6pF$ and $225fF$, respectively, together with the added parasitic capacitances. Each sampling capacitor, C_S, is directly connected to six switches (Fig. 5.1), and 20% of the C_S's are made of switch parasitic capacitances that are added on top of MIM capacitances. Although each integrating capacitor, C_I, is also directly connected to six switches, the effect of switch parasitic capacitances on C_I's is negligible due to larger capacitance sizes. Smaller switches can lead to lower switch parasitic capacitances; however, there is a minimum limit on switch sizes due to the settling. The switches in this prototype were implemented using transmission gates and sized for $1.5k\Omega$ maximum on resistances for the operation range. A ring counter was implemented to produce six non-overlapping clock phases using an external clock signal at $160MHz$. A g_m-cell was not included in the design in order not to dominate the noise and linearity responses of the passive

switched-capacitor filter. Thus, the noise model can also be verified. In the prototype, the passive switched-capacitor filter is followed by an on-chip open drain output buffer to drive the probe used for the measurements. In order not to affect the noise measurement, the output buffer was designed to have lower noise spectral density compared to the filter.

5.1.1 Component Mismatch Effect on the Quality Factor

Component mismatch in between C_I's or C_S's can affect the filter transfer function by changing the filter cut-off frequency and the quality factor of the poles. It is possible to analyze these effects using the continuous-time model. As an example, a single-ended 2^{nd}-order passive switched-capacitor filter can be investigated using the ω_0 and Q expressions previously derived in Section 3 as below (3.6):

$$\omega_0 = \left.\frac{2f_S C_S}{\sqrt{C_{I1}C_S + C_{I2}C_S + 2C_{I1}C_{I2}}}\right|_{C_{I1,I2} \gg C_S/2} \approx \frac{\sqrt{2}}{R\sqrt{C_{I1}C_{I2}}} \tag{5.2}$$

$$Q = \left.\frac{\sqrt{C_{I1}C_S + C_{I2}C_S + 2C_{I1}C_{I2}}}{C_{I1} + C_{I2} + C_S}\right|_{C_{I1,I2} \gg C_S/2} \approx \frac{\sqrt{2C_{I1}C_{I2}}}{C_{I1} + C_{I2}} \leq \frac{1}{\sqrt{2}} \tag{5.3}$$

From the above equations, it can be calculated that for example for a 10% mismatch in between C_{I1} (+5%) and C_{I2} (−5%), Q decreases by 0.13%, which corresponds to a change from 0.707 to 0.706, i.e., the phase of the complex-conjugate poles changes from 45° to 44.93°. C_S mismatch in between the time-interleaved stages affects the R value. However, it does not affect the quality factor (see Eqn. 5.3).

5.2 Measurement Results

For transfer function measurements, a voltage source was fed into the filter through large external resistors (R_{Ext}) in series (a similar practice was reported in [60]). The voltage

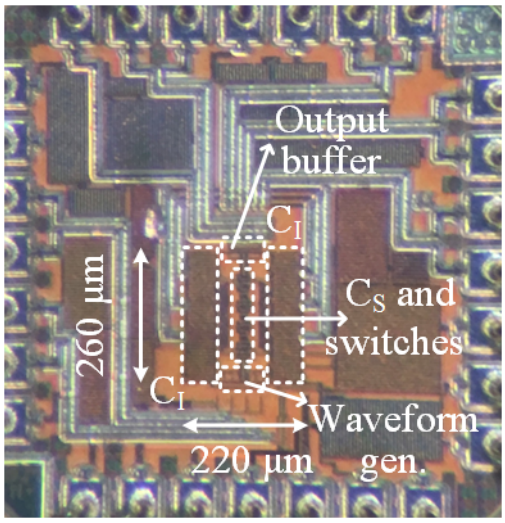


Figure 5.2: The fabricated 3^{rd}-order PSC low-pass filter chip micrograph.

source together with R_{Ext} models the Thévenin equivalent of a g_m-cell with a finite output resistance (Fig. 5.1). The total external resistance is $200k\Omega$ (where the filter input resistance is $27.8k\Omega$, $R_{Eqv} = 1/f_S C_S$). The filter consumes 125 µA from a $1.2V$ power supply, which is the power consumed by the phase clock generator. Fig. 5.2 shows the fabricated chip micrograph, where the active area of the chip is $0.06mm^2$ dominated by the integrating capacitors.

Fig. 5.3 shows the normalized transfer functions of the prototype measurements, post-layout schematic simulation, and the continuous-time model simulation. A good agreement is obtained between measurements, simulations, and the theory. For comparison, 7^{th}-order all real pole passive switched-capacitor filter simulation response is also added to the figure. The 7^{th}-order filter reported in [50] was designed to have the same DC gain and $1dB$ droop frequency. It can be observed that the 7^{th}-order filter transfer function has a much smoother roll-off around the cut-off frequency compared to other filter transfer functions, which causes more than $10dB$ attenuation loss around the band edge. Towards $10MHz$, the measured filter response shows a flattening caused only by leakage on the PCB used for testing. External resistors lead to around $18dB$ attenuation on the PCB, which worsen the filtering profile by elevating the leakage level.

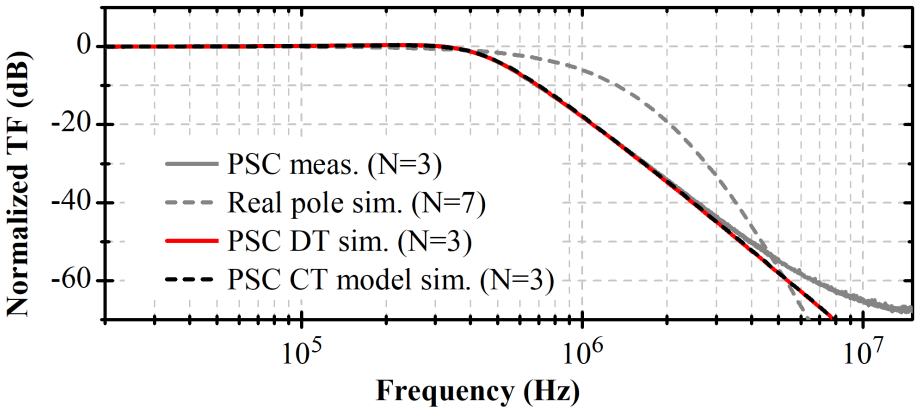


Figure 5.3: Transfer functions of the simulated and measured 3^{rd}-order low-pass PSC filter and the simulated 7^{th}-order all real pole filter.

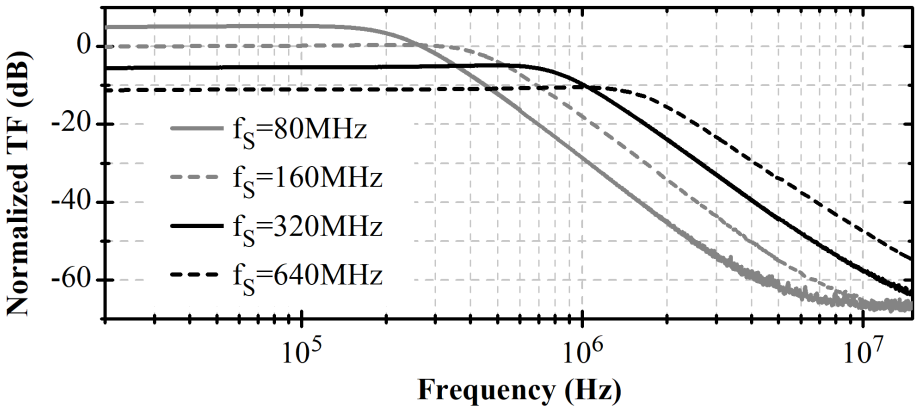


Figure 5.4: Measured low-pass prototype filter transfer functions for changing sampling frequencies, f_S.

Fig. 5.4 shows the normalized measured transfer function of the filter for changing sampling frequency, f_S. It can be seen that the filter passband gain decreases for increasing f_S values, because the equivalent switched-capacitor resistance, $R(= 1/f_S C_S)$, decreases, which is proportional to the low frequency gain of the filter as previously derived in Eqn. 3.10. Whereas, the filter cut-off frequency, which is proportional to the $1/RC_I(= f_S C_S/C_I)$, increases for increasing f_S values. Fig. 5.5 shows the first (v_{in}), the second ($v_{2P} - v_{2N}$), and the third (v_{out}) order filtering nodes normalized measured transfer functions together with the continuous-time model simulation results, which match with very good agreement.

Output noise spectral density measurement results are shown in Fig. 5.6 with a

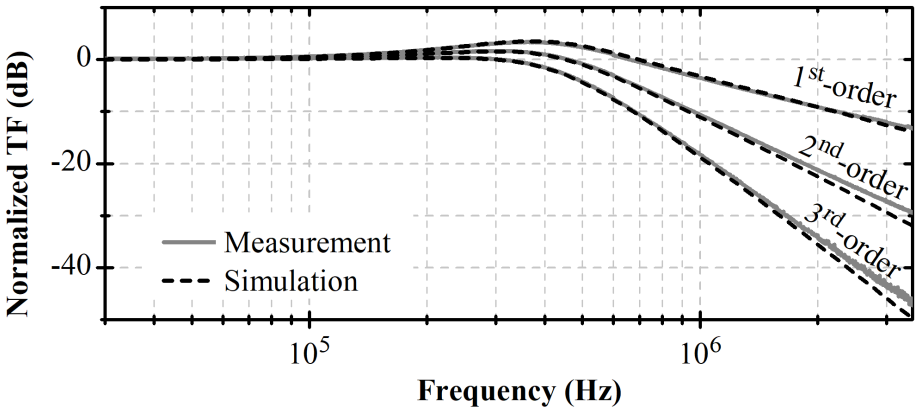


Figure 5.5: Measured low-pass prototype filter transfer functions for 1^{st}, 2^{nd}, and 3^{rd} -order output nodes for $f_S = 160MHz$.

resolution bandwidth of $1Hz$. The noise is measured at the output of the buffer and later referred to the output of the filter, v_{out}. At low frequencies, noise is equal to the noise of R_{Eqv} (i.e., $4kT/f_S C_S$). The solid black line shows the simulation result of the passive switched-capacitor filter, and the dashed line shows the continuous-time model simulation result. The noise spectral density was reported up to $1MHz$ due to the comparable noise floor of the spectrum analyzer. However, this measurement can show the in-band noise spectral density as well as the out-of-band decay close to the filter band edge. It can be seen that measured noise spectral density closely follows the simulations and the theory. The measured input referred noise is 15.8 µV, integrated between $10kHz$ and $470kHz$. Out-of-band IIP3 is extrapolated using two blockers at $3.4MHz$ and $6.7MHz$, creating an intermodulation product at $100kHz$. Fig. 5.7 shows the input signal power and the 3^{rd}-order intermodulation distortion measurement results referred to the chip input (V_{in} in Fig. 5.1). The out-of-band IIP3 extrapolated is $55.1dBm$ leading to $92dB$ spurious-free dynamic range (SFDR).

Table 5.1 summarizes the measurement results and compares them with the 7^{th}-order passive switched-capacitor filter [50] and also with the recently published 4^{th}-order passive switched-capacitor filter that uses an active feedback structure [5]. The SFDR obtained with this work is more than $20dB$ better with a much lower power consumption

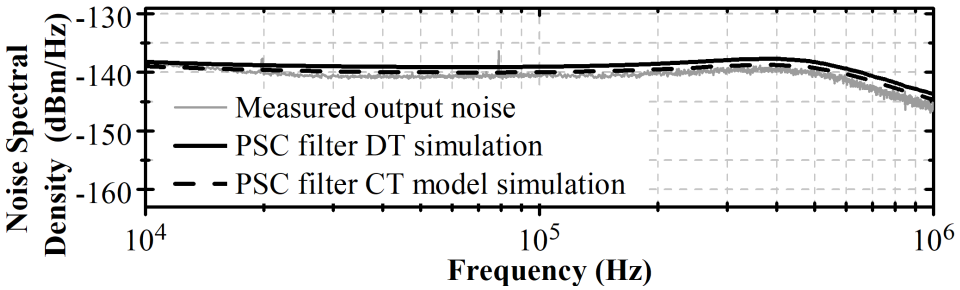


Figure 5.6: Measured output noise spectral density over the prototype filter bandwidth.

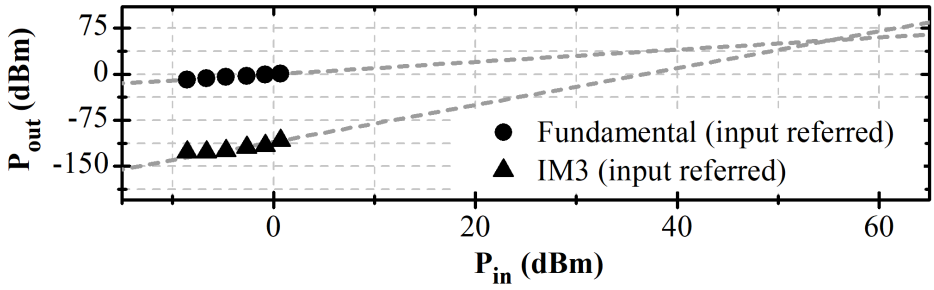


Figure 5.7: Out-of-band IIP3 measurements of the prototype filter with two tones.

partially thanks to the presence of complex-conjugate poles, which allowed to reduce the filter order without compromising the filter selectivity close to the cut-off frequency. However, it should be noted that both other works employ a transconductance at the input, and [5] also uses another transconductance as the active feedback, which degrades filters' linearity and increases power consumption. Although the transconductance on the feedback path is not needed in this work thanks to the passive feedback topology, the input g_m-cell is only avoided due to testing purposes. Thus, Table 5.1 should be reviewed considering these differences. However, it can be possible to come up with an analytical comparison in between the reported 3^{rd}-order filter and the 7^{th}-order all real pole filter [50] when the g_m-cell is omitted, i.e., both filters are considered as current input - voltage output.

Analytical Comparison

The reported differential 3^{rd}-order filter with passive feedback and the differential 7^{th}-order all real pole filter have the same input resistance, passband gain, in-band output

noise spectral density, if the sampling capacitor of the 3^{rd}-order filter is set half of the 7^{th}-order filter's sampling capacitor. This comparison is valid assuming the same sampling frequency for both of the filters with time-interleaving (Table 5.2).

Filters' noise and linearity performances should be considered to compare the SFDR. The same gain and output noise spectral density result in the same input referred noise. Moreover, since the current input filters both have the same input resistance and gain, they can be assumed to have similar linearity performance since the first-stage limits the linearity. Thus, the SFDR can be assumed to be the same for both of the filters.

As the final step, power consumption can be compared. The digital power consumption is proportional to the size and the number of switches and the sampling frequency assuming the same technology for both of the filters. The number of switches depends on the topology, and it is listed in Table 5.2 for differential implementations. The size of the switches can be assumed proportional to C_S, because C_I's are much larger than C_S, i.e., the settling is determined by the C_S. Thus, digital power consumption is proportional to $C_S V_{DD}^2 N_{SW} f_S$, where N_{SW} is the number of switches. For our case, V_{DD} and f_S are the same for both of the filters. Thus, $C_S N_{SW}$ multiplication determines the power consumption, which results in around ***86% power savings*** in the waveform generator for the proposed 3^{rd}-order filter compared to the 7^{th}-order all real pole implementation.

Table 5.1: Summary results and comparison.

	This Work	**[50]**	**[5]**
Technology (nm)	130	65	180
Order	3	7	4
Poles	1 real, 2 comp.-conj.	7 real	4 comp.-conj.
Power (mW)	0.15	1.98	4.3
Wavegen. power (mW)	*0.15*	*1.68*	*2.4*
G_m-cells power (mW)	-	*0.3*	*1.9*
Voltage supply (V)	1.2	1.2	1.8
3dB cut-off (MHz)	0.47	0.4-30	0.49-13.3
Sampling rate (MS/s)	160	800	65-300
OB IIP3 (dBm)	55.1	11.7	15.03
Int. noise (μV)	15.8*	13.7**	13.6***
IRN ($nV/\sqrt{Hz}$)	23.3	4.57	6.54
SFDR (dB)	92'	64	68
Active area (mm^2)	0.06	0.42	2.9

*Integrated over *10k-470kHz, **50k-9MHz, ***100k-4.4MHz*
' SFDR=2/3.(IIP3-Int. Noise)

Table 5.2: Analytical comparison of 3^{rd}-order filter with passive feedback and 7^{th}-order all real pole filter.

	This Work	**[50]**
Sample frequency	f_S	f_S
Sampling capacitor	$C/2$	C
Diff. input resistance	$2/f_SC$	$2/f_SC$
Gain (v_{out}/i_{in})	$2/f_SC$	$2/f_SC$
Output noise (V^2/Hz)	$8kT/f_SC_S$	$8kT/f_SC_S$
# of interleaved stages	3	8
Total # of switches	36	128

Chapter 6

Conclusions

This thesis reports a simplified model for oversampled passive switched-capacitor filters where the sampling parts of the circuit are replaced with continuous-time equivalents consisting of resistors and ideal buffers. The main advantage of the model is that it is composed of unilateral branches, and thus, it can address structures with non-reciprocal low frequency behaviour. Moreover, it can also be applied to structures with sampling capacitors with both terminals switching. The reported continuous-time model results in easy and intuitive analysis compared to the conventional charge-balance equations and leads to transfer function and noise analysis with good accuracy. Furthermore, the model can also be used for transfer function and noise simulations, which can require much shorter simulation times compared to conventional discrete-time simulations. An example noise simulation comparison in SpectreRF (pss+pnoise) and Spectre results in a decrease in the simulation time from 12 minutes 40 seconds to 1.06 seconds (around 700 times improvement). This thesis also covers some of the limitations and applicability of the model.

Through the use of this model, a passive switched-capacitor filter with complex-conjugate poles is realized, which results in a sharper filter profile compared to its real-pole counterparts. A 3^{rd}-order filter prototype with complex-conjugate poles was de-

signed and fabricated in 0.13 µm CMOS process. Measurements performed on the filter prototype result in state-of-the-art performance meanwhile verifying the continuous-time modelling and design approach. Noise measurements and model simulations matched with less than $1dB$ accuracy. With this prototype, for the first time, switched-capacitor complex conjugate poles have been integrated on silicon without the need of any active circuitry. This represents a remarkable result that makes it possible to obtain sharp filtering profiles using passive switched-capacitor filters while showing that the design approach can lead to the invention of novel structures.

6.1 Contributions

The contributions of this thesis can be summarized as below:

- A new continuous-time modelling approach for oversampled switched-capacitor circuits was introduced [59]. The model can be used for analysis, design, and simulations.
- The continuous-time modelling approach was generalized for topologies with non-grounded sampling capacitors [61].
- Limitations of the model were studied [61].
- A 2^{nd}-order passive switched-capacitor filter with passive feedback was introduced to realize complex-conjugate poles [59]. (Although, later we realized that there was a similar approach in the literature back in 1980 [44].)
- A 3^{rd}-order passive switched-capacitor filter prototype with complex-conjugate poles was designed, fabricated, and tested [57].
- The continuous-time modelling approach was verified with signal and noise measurements on the fabricated prototype [57].

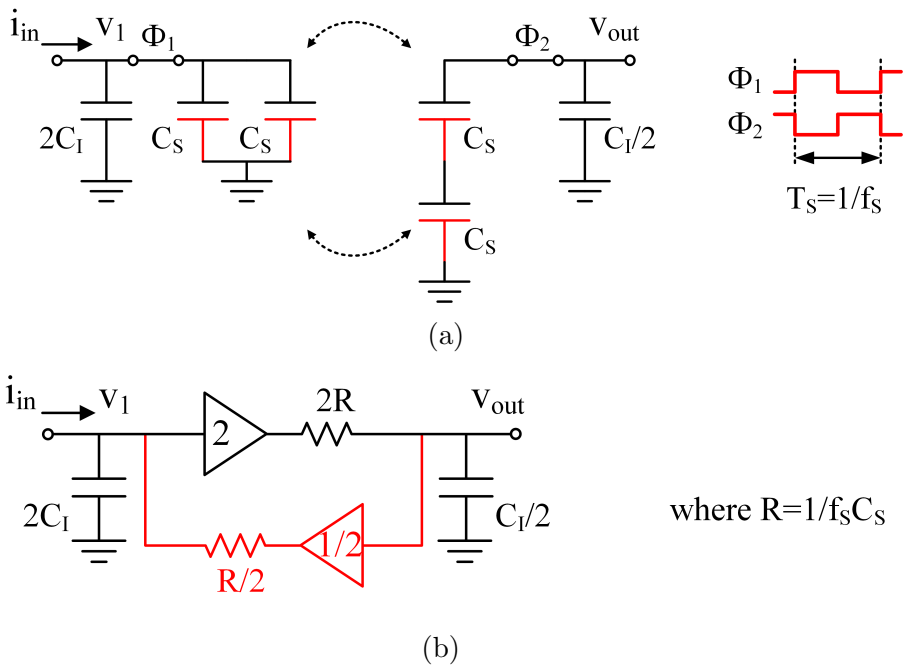


Figure 6.1: a) A symbolic passive switched-capacitor filter with a gain of 2 charge pump, and b) its continuous-time model.

6.2 On-Going and Future Work

6.2.1 Increasing Configurability and Linearity of the PSC Filter

There is on-going work together with Da Kang and QingNan Yu to increase the configurability and linearity of the passive switched-capacitor filter. As a capstone project, Da and QingNan (and also Yueqi Chen) designed a prototype passive switched-capacitor filter. The filter is configurable for 2^{nd} and 3^{rd}-order by only changing the clocking scheme and with the use of an external digital control bit. Moreover, the filter has gain and attenuation by two control, which is realized by making use of charge-pump structures within the sampling capacitor. Fig. 6.1a shows a symbolic passive switched-capacitor filter with the charge pump structure, where two sampling capacitors switch in between parallel and series configurations to provide a passive voltage gain of two from node v_1 to v_out. Fig. 6.1b shows the associated continuous-time model.

In order to increase the linearity of the filter, we focused on the input transconduc-

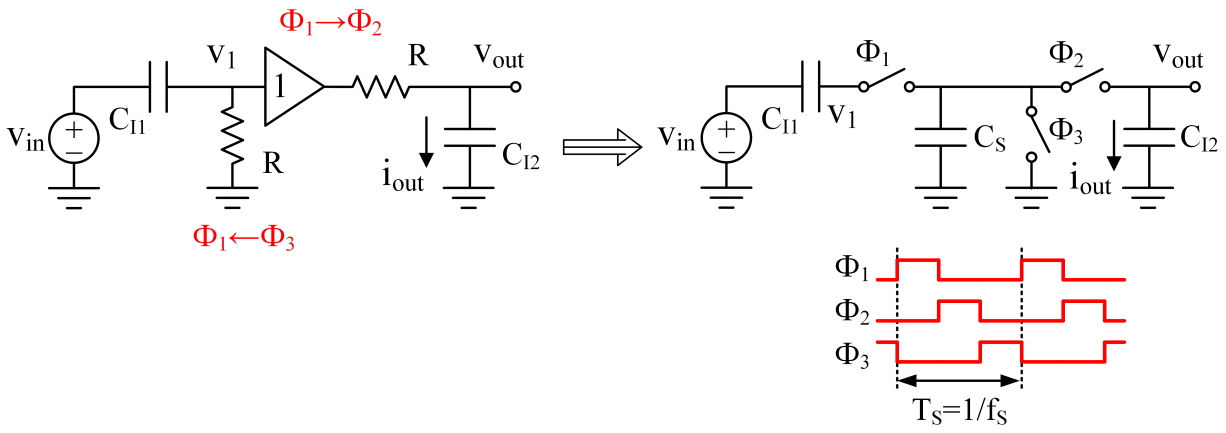


Figure 6.2: A voltage input voltage output passive switched-capacitor band-pass filter continuous-time model and its discrete-time implementation.

tance. Since the passive switched-capacitor filter is highly linear, the input transconductor becomes the linearity bottleneck. To address this issue with the contributions from Javid Musayev, we quantized the input g_m-cell and also the configurable passive switched-capacitor filter itself similar to the approach reported in [62].

The chip was fabricated in 0.18 µm CMOS process, and at this point measurements are on-going.

6.2.2 Band-Pass and High-Pass Passive Switched-Capacitor Filters

It is possible to obtain real pole band-pass and high-pass filters starting from the continuous-time model and then designing the passive switched-capacitor structures. An example band-pass filter with voltage input voltage output is shown in Fig. 6.2. If the output is defined as the current through C_{I2}, the structure shown in Fig. 6.2 becomes a voltage input current output 2^{nd}-order high-pass filter. These filters may find applications in biosensing, especially for applications where large undesired DC signals accompany small desired AC biosignals at the IC input. However, it should be noted that since these are voltage input filters, they do not have inherent anti-aliasing property, which is different

from the current input passive switched-capacitor filters (see Fig. 1.4).

6.2.3 Passive Switched-Capacitor Digital-to-Analog Converter

It is possible to use the passive switched-capacitor filter as a digital-to-analog converter with reconstruction filtering. The simple idea is shown in Fig. 6.3, which is comparable to the RF-DAC receiver reported in [21], but possibly may result in better performance due to the high-order passive switched-capacitor filtering. The number of gray boxes including C_S and switches depends on the number of bits in the DAC. In the first step, C_S's are either connected to the ground node or V_{DD} node depending on the digital control signals. In ϕ_2, all C_S's are connected to C_I1. Since all C_S's are also connected to each other at this phase, the charge sharing in between C_S's leads to the digital to analog conversion. Moreover, C_S's are connected to C_{I1} led to 1^{st}-order filtering of the resulting analog signal. By increasing the number of phases and C_I's, the filter order can be increased. In Fig. 6.3, the topology has 3^{rd}-order characteristics with all real poles. Konstantinos Vasilakopoulos has been expanding this idea for an RF-DAC in his Ph.D. thesis.

6.2.4 High-Order Butterworth Passive Switched-Capacitor Filter

To realize complex-conjugate poles, in this thesis, we have added a single global feedback path to the passive switched-capacitor structure. As a result, although we can get complex-conjugate poles with large quality factors for high filter orders (Fig. 3.8 and Fig.3.9), the in-band peaking limits the use of those high-order filters. However, using a single-feedback can be just the beginning. It may be possible to obtain Butterworth filter characteristics for higher than 2^{nd}-order filters by using multiple feedback and feedforward paths and by adding charge-pump structures. Fig. 6.4 shows an example continuous-

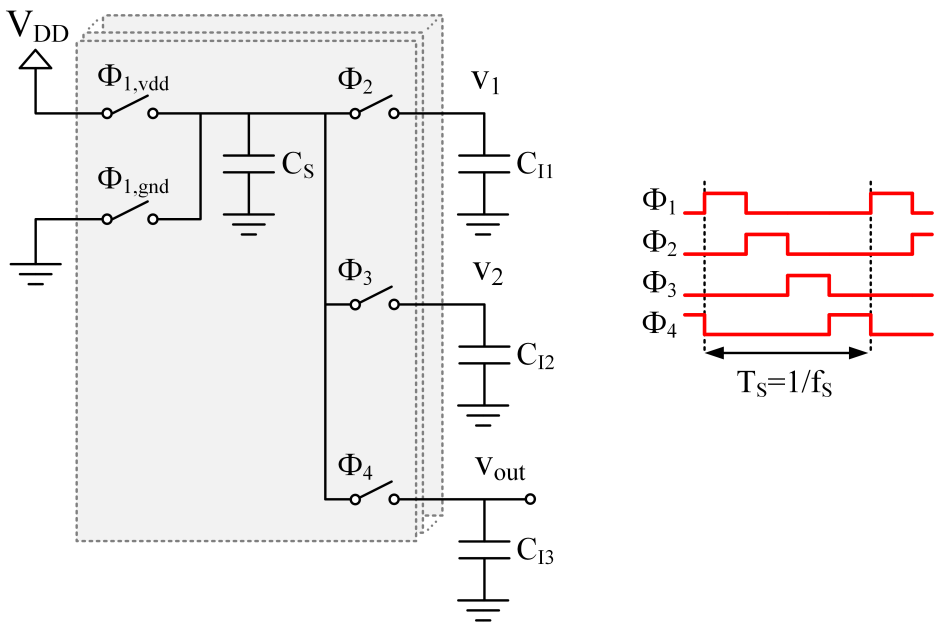


Figure 6.3: The basic idea for a passive switched-capacitor DAC with 3^{rd}-order reconstruction filtering.

time model drawing for a 3^{rd}-order filter with multiple feedback loops. Multiple feedback and feedforward loops are implementable using multiple C_S's. Also, the analysis can be possible using the reported continuous-time model rather than going through rigorous charge-domain analyses. Moreover, it may even be possible to use supervised learning to reach to a transfer function that can approximate the Butterworth filter behaviour. The author is planning to continue working on this idea as a hobby project.

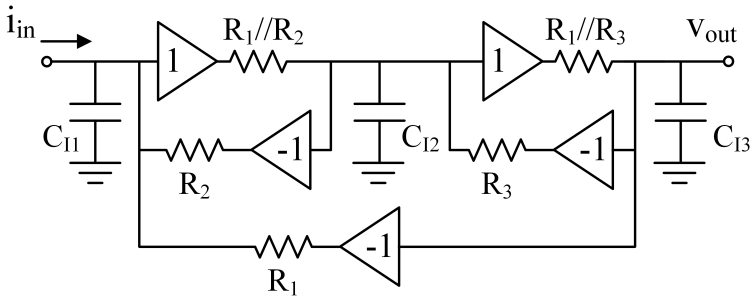


Figure 6.4: Passive switched-capacitor filter continuous-time model with multiple feedback loops.

Appendix A

Equivalent Resistance Derivation for Low Frequency

In Section 2.1 Eqn. 2.5 - 2.7 derive the equivalent switched-capacitor resistance by assuming ideal DC voltage sources connected to V_1 and V_2 nodes and by calculating the average current transfer in one clock period. While this derivation is quite well known for DC signals, to the author's knowledge, there is no equivalent derivation for low frequency ac signals. In this appendix, the equivalent impedance is derived for ac voltage sources with an input signal frequency much lower than the sampling frequency, f_S.

Assume that V_1 and V_2 nodes in Fig. 2.1 are connected to two voltage sources with maximum frequencies well below the sampling frequency, f_S, and switches are ideal with zero on resistances. Then, the current supplied by V_1 can be written as follows:

$$i_1(t) = i_{1pulse}(t) + i_{1cap}(t) \tag{A.1}$$

where $i_{1pulse}(t)$ is the current pulse occurs at the instant the switch is closed at ϕ_1, and $i_{1cap}(t)$ is the current supplied to the capacitor during ϕ_1, as the voltage V_1 slowly varies. These two components can be written as below:

$$
\begin{aligned}
i_{1pulse}(t) &= C_S[v_1(t) - v_2(t)] \sum_{n=-\infty}^{\infty} \delta(t - nT_S) \\
i_{1cap}(t) &= C_S \frac{dv_1(t)}{dt} \sum_{n=-\infty}^{\infty} a_n e^{jn\omega_S t} \\
\text{with } a_n &= \begin{cases} \frac{2}{n\pi}(-1)^{\frac{n-1}{2}} & \text{n is odd} \\ 0 & \text{n is even and n} \neq 0 \\ 0.5 & \text{n=0} \end{cases}
\end{aligned}
\tag{A.2}
$$

where $i_{1pulse}(t)$ is a series of current pulses whose area is equal to $C_S.\Delta V (= C_S v_1(nT_S) - C_S v_2(nT_S))$, and $i_{1cap}(t)$ is the capacitor current equation multiplied by the rectangular pulse train, which is represented by its Fourier series. Note that the rectangular pulse train has the same phase of ϕ_1 with an amplitude of 1.

To define an impedance to model the topology as a linear time-invariant (LTI) system, the resulting current in response to the V_1 and V_2 voltages should be examined. From equations A.1 and A.2, it is possible to write the Fourier transform of the produced current as:

$$
\begin{aligned}
I_1(\omega) = &\frac{C_S}{T_S} \sum_{k=-\infty}^{\infty} [V_1(j\omega - jk2\pi f_S) - V_2(j\omega - jk2\pi f_S)] \\
&+ j\omega C_S \sum_{k=-\infty}^{\infty} a_k V_1(j\omega - jk2\pi f_S)
\end{aligned}
\tag{A.3}
$$

where a_k are the Fourier series coefficients and equal to a_n for $n = k$. It can be observed from Eqn. A.3 that the current produced has a fundamental harmonic and also higher harmonics at the multiples of f_S. To model the circuit behaviour for low frequencies, only the fundamental harmonic would be of interest [63], which can be written as below:

$$
I_{1Fund}(\omega) = f_S C_S[V_1(j\omega) - V_2(j\omega)] + j\omega \frac{C_S}{2} V_1(j\omega) \tag{A.4}
$$

It can be seen that I_{1Fund} results in $1/f_S C_S$ resistance in between V_1 and V_2 nodes

and $C_S/2$ capacitance in between the V_1 node and ground. Although $C_S/2$ is needed for the exact representation at the fundamental frequency, for simplicity, it is ignored in the body of this thesis, as all the cases that are covered, sampling capacitors are connected to low impedance nodes, where the effect of $C_S/2$ becomes negligible. Moreover, it should be noted that $2/j\omega C_S$ impedance is much greater than $1/f_S C_S$ for the frequencies of interest ($\pi f << f_S$). For a small set of cases where C_S is comparable to C_I, including $C_S/2$ might help to get results with better accuracy, which is briefly covered in Appendix C.

The impedance seen from the V_2 node can be derived similarly by writing the current equation sunk into the V_2 node, $i_2(t)$. In this case, the Fourier Transforms of the current produced can be written as follows:

$$\begin{aligned} I_2(\omega) =& e^{-\frac{j\omega}{2f_S}} \frac{C_S}{T_S} \sum_{k=-\infty}^{\infty} [V_2(j\omega - jk2\pi f_S) - V_1(j\omega - jk2\pi f_S)] \\ &+ j\omega C_S \sum_{k=-\infty}^{\infty} b_k V_2(j\omega - jk2\pi f_S) \\ \text{with } b_k =& \begin{cases} \frac{2}{n\pi}(-1)^{\frac{n+1}{2}} & \text{n is odd} \\ 0 & \text{n is even and n} \neq 0 \\ 0.5 & \text{n=0} \end{cases} \end{aligned} \tag{A.5}$$

whose fundamental component becomes:

$$I_{2Fund}(\omega) = e^{-\frac{j\omega}{2f_S}} f_S C_S [V_2(j\omega) - V_1(j\omega)] + j\omega \frac{C_S}{2} V_2(j\omega) \tag{A.6}$$

The exponential term in I_{2Fund} expression is due to the sampling phase shift, and it can be ignored for the frequencies of interest ($\pi f << f_S$). Once the exponential term is ignored, it is seen that I_{2Fund} expression results in a $1/f_S C_S$ resistance in between V_1 and V_2 nodes and a $C_S/2$ valued capacitance in between V_2 node and ground. This capacitance can be ignored as well because the impedance of $2/j\omega C_S$ is much greater than $1/f_S C_S$ for the frequencies of interest ($\pi f << f_S$). Thus, the voltage and current relationship

between V_1 and V_2 voltage sources can be modelled by an equivalent resistance of $1/f_S C_S$ in between those two nodes. (As mentioned earlier, for a small set of cases where C_S is comparable to C_I, including $C_S/2$ might help to get results with better accuracy, which is briefly covered in Appendix C.)

Appendix B

Continuous-Time Model Derivation for Multi-Phase Topology

In Section 2.1, buffer + R model is derived by assuming ideal DC voltage sources connected to V_1 and V_2 nodes and by calculating the average current transfer in one clock period (Eqn. 2.9). In this appendix, the proposed multi-phase switched-capacitor continuous-time model is derived for ac voltage sources with an input signal frequency much lower than the sampling frequency, f_S.

Assume that V_1, V_2, and V_3 in Fig. B.1a are all connected to ideal voltage sources with input frequencies much smaller than the sampling frequency, f_S, and switches are ideal with zero on resistances. Then, the current supplied by V_1 can be written as follows:

$$\begin{aligned} i_1(t) &= i_{1pulse}(t) + i_{1cap}(t) \\ i_{1pulse}(t) &= C_S[v_1(t) - v_3(t)] \sum_{n=-\infty}^{\infty} \delta(t - nT_S) \\ i_{1cap}(t) &= C_S \frac{dv_1(t)}{dt} \sum_{n=-\infty}^{\infty} c_n e^{jn\omega_S t} \\ with\ c_n &= \begin{cases} -\frac{2}{n\pi}\sin(\frac{n\pi}{3}) & \text{n} \in \mathbb{Z} \\ \frac{1}{3} & \text{n=0} \end{cases} \end{aligned} \tag{B.1}$$

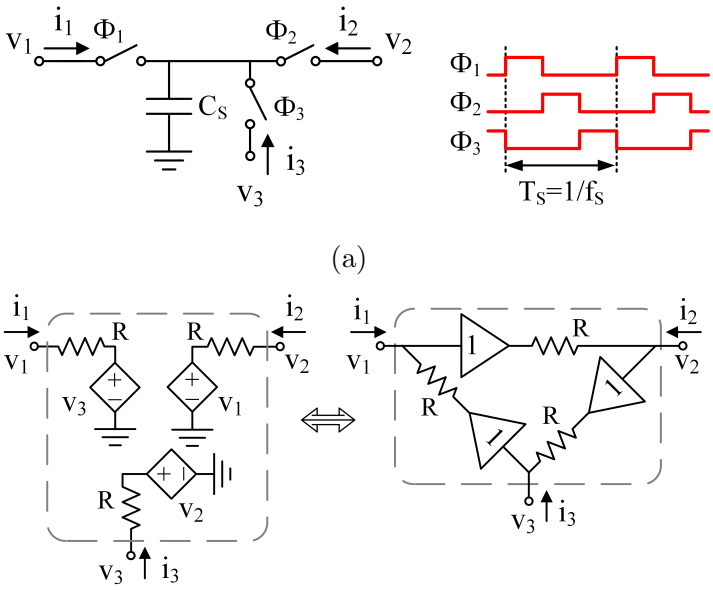


Figure B.1: A three-phase switched-capacitor topology, and b) its continuous-time model.

It can be shown that these current equations lead to a resistor between V_1 and V_3 nodes with a value of $1/f_S C_S$ for the frequencies of interest. Moreover, Eqn. B.1 also leads to a $C_S/3$ valued capacitance in between the V_1 node and ground (the derivation and assumptions are similar to the ones discussed previously in A).

To complete the model and to replace the switching parts, all current components (i_1, i_2, and i_3) should be considered. It can be shown that, for the frequencies of interest, there is a general current equation valid for i_1, i_2, and i_3 that can be written as follows in the Fourier domain:

$$I_k(\omega) = f_S C[V_k(j\omega) - V_{Prev}(j\omega)] \tag{B.2}$$

where I_k represents the Fourier transform of the current component sourced by V_k voltage source (where $k = 1, 2$, and 3), and V_{Prev} represents the voltage source that C_S is connected to in the prior phase before connecting to V_k. It is important to note that although there exist three voltage sources, the current component related to each node

only depends on two voltage sources that C_S is connected (one is at the relevant phase, and the other one is at the phase prior to the relevant phase).

Fig. B.1b shows the schematic representation of Eqn. B.2 employing ideal voltage controlled voltage sources (VCVS) in series with the $1/f_S C_S$ valued equivalent resistances. This schematic can be modified to have a more intuitive view, where VCVS's are replaced with ideal voltage buffers.

Appendix C

The Continuous-Time Model with Capacitance

As discussed in Appendices A and B, adding capacitance to the continuous-time model may lead to more accurate results, especially for the cases when C_S values are comparable to C_I. In this appendix, the two-phase 1^{st}-order passive switched-capacitor filter is investigated with and without the added capacitance to the model. Fig. C.1 shows the filter's discrete-time implementation together with the two continuous-time models. Due to the two-phase structure of the filter, $C_S/2$ valued capacitance is added in between node V_{out} and ground (see Appendix A).

Fig. C.2 shows the frequency transfer functions simulated using SpectreRF periodic steady state (pss) and periodic AC (pac) analyses for a sampling frequency of 160 MHz, $C_S = 200fF$, and with C_I/C_S ratios of 40 and 4. For the equivalent resistance model shown in Fig. C.1b with $C_I/C_S = 40$, the error in the $3dB$ cut-off frequency is 1%, whereas for the model with $C_S/2$ (Fig. C.1c), this error becomes almost 0%. For the equivalent resistance model with $C_I/C_S = 4$, the error in the $3dB$ cut-off frequency becomes 12%, whereas for the model with $C_S/2$, this error becomes 0.4%.

Fig. C.3 shows simulated step responses of the PSC filter discrete-time implementa-

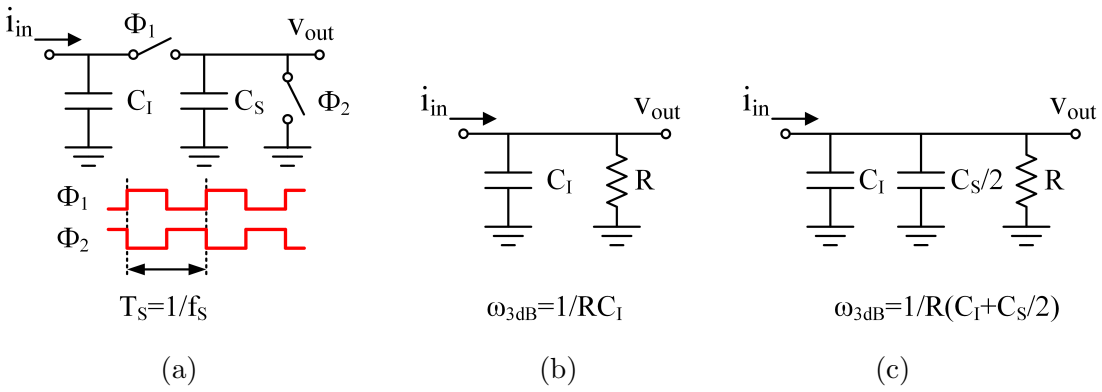


Figure C.1: a) 1^{st}-order PSC filter, b) its equivalent resistance continuous-time model, and c)its equivalent resistance continuous-time model with $C_S/2$ capacitance added.

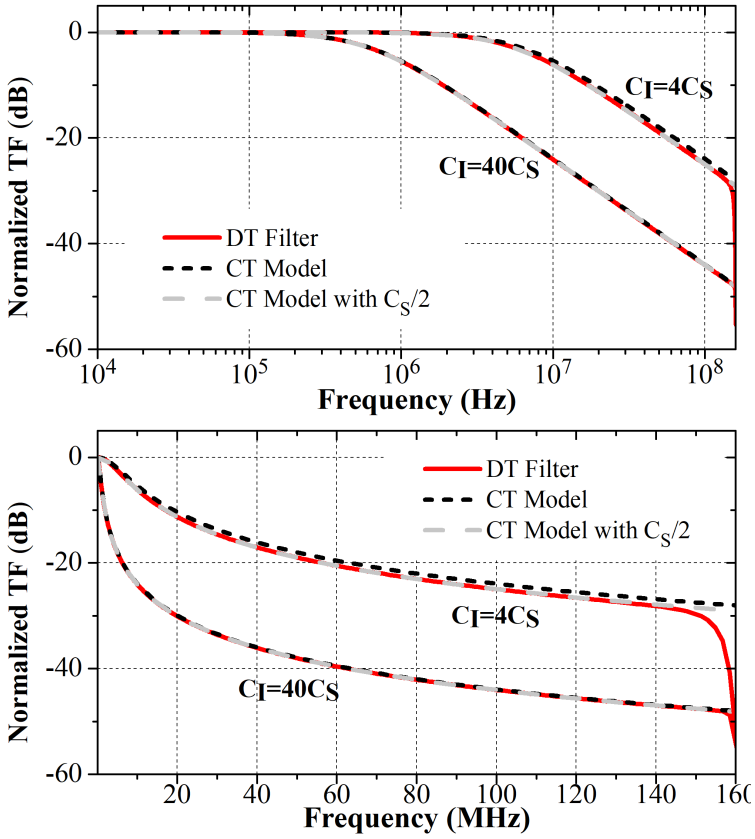


Figure C.2: 1^{st}-order PSC filter simulated frequency responses of discrete-time implementation and continuous-time models with and without $C_S/2$ for $C_I/C_S = 40$ and $C_I/C_S = 4$ (logarithmic scale frequency axis on top and linear scale frequency axis on bottom).

tion and continuous-time models with C_I/C_S ratios of 40 and 4. The mid and bottom plots show the difference between the discrete-time implementation sampled and the continuous-time model responses. The error is dominant during the initial transient phase, which corresponds to the high frequency response with limited model accuracy. Also, it should be noted that the model with $C_S/2$ results in a much smaller error compared to the equivalent resistor model without $C_S/2$.

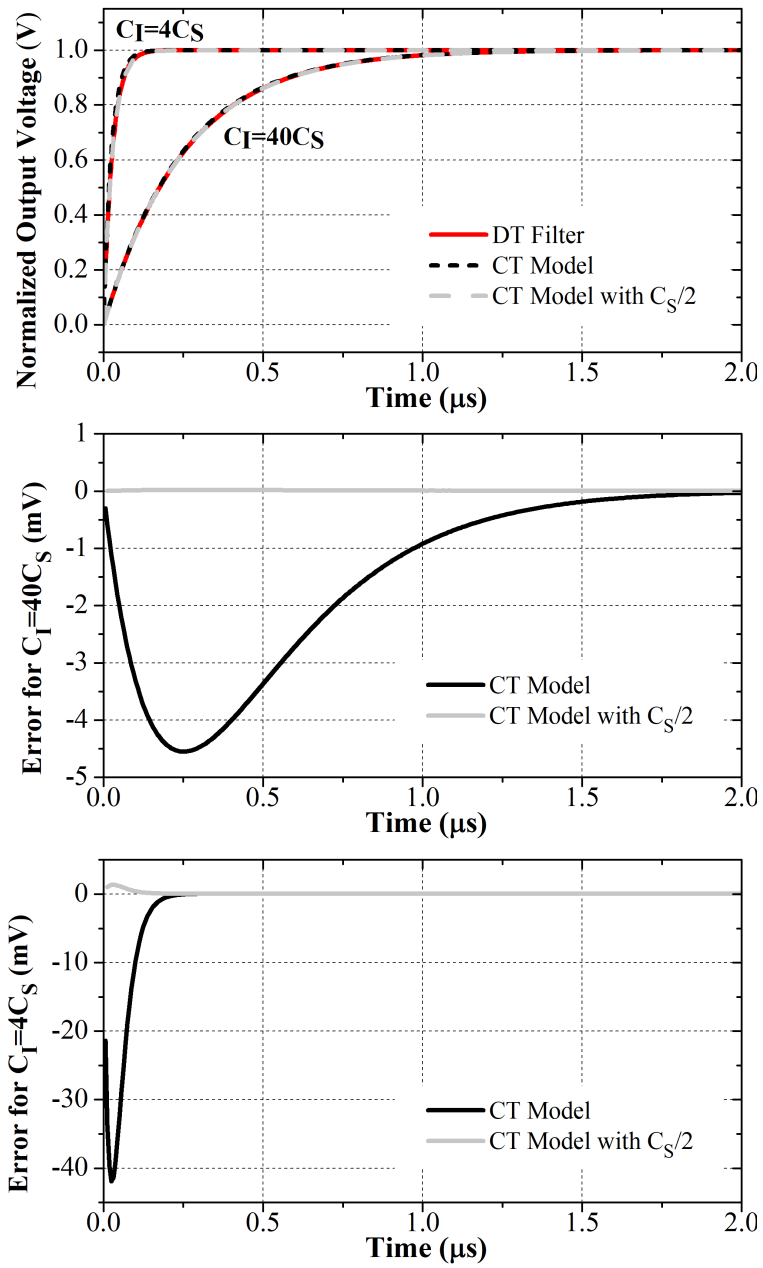


Figure C.3: 1^{st}-order PSC filter simulated step responses of discrete-time implementation and continuous-time models with and without $C_S/2$ for $C_I/C_S = 40$ and $C_I/C_S = 4$.

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