LOW POWER ANALOG FRONT END DESIGN FOR 112 GBPS PAM-4
SERDES RECEIVER

by

Mayank Aggarwal

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Graduate Department of Electrical and Computer Engineering
University of Toronto

Abstract

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Mayank Aggarwal

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This thesis proposes an analog front end (AFE) design of a 112 Gbps PAM-4 SERDES receiver in 16 nm FinFET technology. It consists of a front-end termination block and a CMOS inverter based continuous time linear equalizer (CTLE). The high transconductance of the CMOS inverter as an amplifier provides a low power equalization solution. The front end-termination network is exploited to achieve certain passive equalization. The common-mode feedback loop (CMFB) improves the common-mode rejection ratio (CMRR) of the CTLE and it is a low power biasing solution in comparison to a self-biased diode connected inverter load. The tunability in the CMOS tristate inverter cell enables power-scalability in the design. This also helps to track PVT variations. Using the CTLE as the only means of active equalization for a long reach channel (backplane) with 30 dB attenuation at 28GHz nyquist frequency, this AFE design achieves 17dB of equalization consuming 10 mW power with a 0.8 V supply voltage in post layout extracted results.

To my beloved mother, brother and bhabhi ♡

Acknowledgements

> Live as if you were to die tomorrow.
>
> Learn as if you were to live forever.
>
> _____
>
> *Mahatma Gandhi*

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List of Acronyms

ADC Analog to Digital Converter

ASIC Application Specific Integrated Circuit

BER Bit-Error Rate

BEOL Back-End-Of-Line

BGA Ball Grid Array

C4 Controlled Collapse Chip Connection

DCD Duty-Cycle Distortion

CDR Clock and Data Recovery

CML Current-Mode Logic

CRU Clock Recovery Unit

CTE Coefficient of Thermal Expansion

CTLE Continuous-Time Linear Equalizer

DFE Decision Feedback Equalizer

DNL Differential Non-Linearity

EMI Electromagnetic Interference

FEXT Far-end Crosstalk

FFE Feed-Forward Equalizer

HBM High-Bandwidth Memory

HMC Hybrid Memory Cube

IIR Infinite Impulse Response

ILO Injection Locked Oscillator

INL Integral Non-Linearity

ISI Inter-Symbol Interference

LDO Low-Dropout

LSB Least Significant Bit

MCM Multi-Chip Module

MSB Most Significant Bit

NEXT Near-end Crosstalk

NRZ Non-Return to Zero

PAM Pulse Amplitude Modulation

PCB printed circuit board

PD Phase Detector

PDN Power Distribution Network

PI Phase Interpolator

PRBS Pseudo-Random Binary Sequence

PSIJ power supply induced jitter

RDL ReDistribution Layer

RF Radio Frequency

SEM Scanning Electron Microscopy

SSO Simultaneous Switching Output

SST Source-Series-Termination

ToF Time-of-Flight

TSV Through Silicon Via

UBM Under Bump Metalization

UI Unit Interval

VCO Voltage Controlled Oscillator

VCSEL Vertical-Cavity Surface-Emitter-Laser

USR Ultra-Short Reach

VSR Very-Short Reach

1   Introduction

1.1. Motivation

There has been a continuous demand for increase in data consumption over the last several years all over the world. Figure 1.1 shows the trend in which global traffic has increased over the years. This demand comprises of consumer and business applications in the form of multimedia streaming, audio-video conferencing, internet surfing, cloud storage and other digital enterprise applications. As per the Cisco 2020 report, there will be nearly 5.3 billion total internet users (66 percent of global population) by 2023, up from 3.9 billion (51 percent of global population) in 2018 [1]. There will be $\sim 150\,\%$ increase in networked devices per capita by the year 2023 [1]. As a result, the need for data centers will rise exponentially. Especially, with the ongoing pandemic of corona-virus (COVID-19), businesses have become more dependant on cloud services. Foreseeing this situation, several big tech companies are investing heavily in worldwide digital transformation. This increasing need for data centers and cloud resources has led to the development of large-scale public cloud data centers called hyperscale data centers [1]. It is expected that by 2021 there will be ~ 628 hyperscale data centers globally, compared to 338 in 2016 [1].

The power consumption within the data centres has been consistent at a rate of nearly $1\,\%$ of the global electricity consumption since 2012 despite the continuous increase in demand for data [3]. This has been achieved by improving the efficiency in power
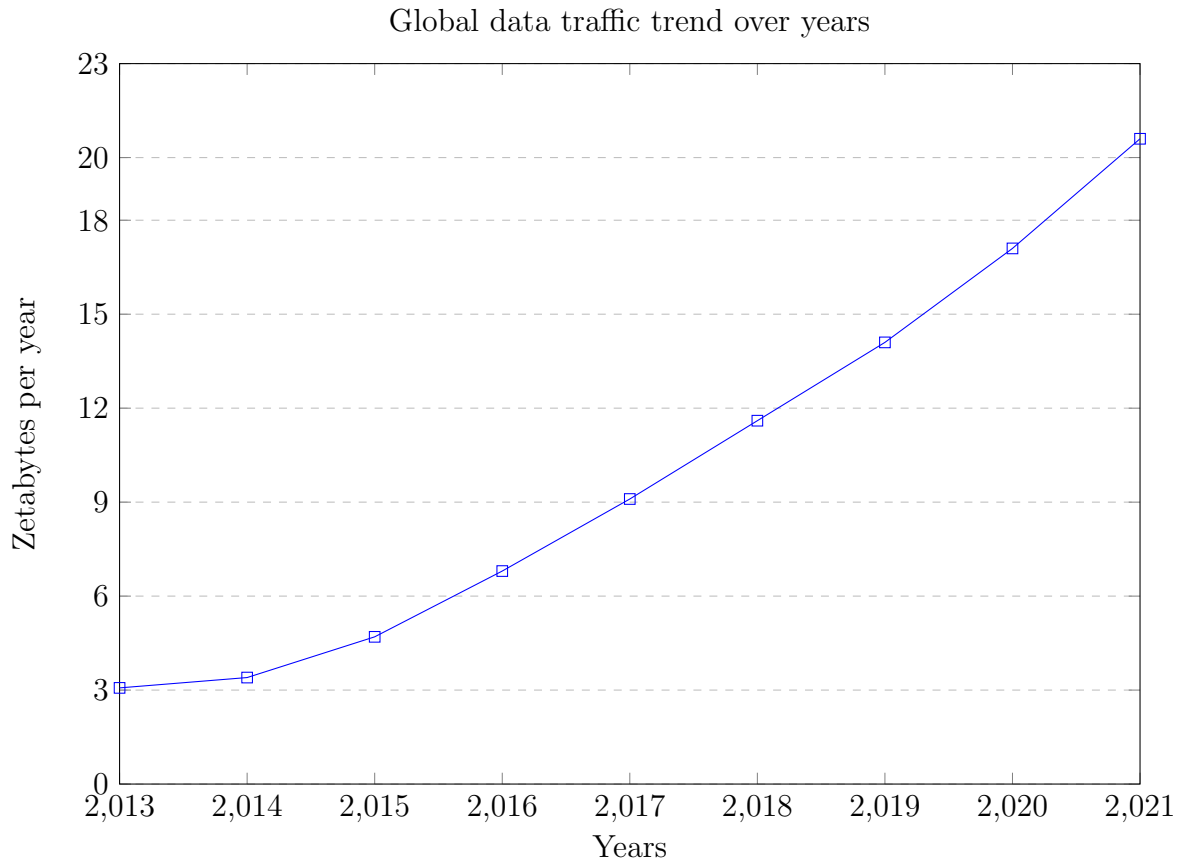
Figure 1.1: Global data traffic over years [2].

consumption due to transistor scaling in newer technologies. However recent trends indicate that transistor scaling no longer gives us more speed as per data demand, nor it can offset the further increase in power consumption by data centres. It is predicted that if data centres scale up to meet the data demand, they are likely to consume about 8 % of the global electricity consumption by 2030. This increased power consumption will also result in increased undesirable carbon emissions [3]. Hence, the present research focuses on developing high-speed, low power and low cost devices in data centres with good signal integrity.

Data centres comprise of routers, switches, storage, servers, firewalls and networking gear. These components exist in the racks and they are connected to each other through wireline links and need SERDES (Serializer De-serializer) transceivers for inter-communication. SERDES is a preferred choice as it can do efficient data communication

with fewer cables, low power, less number of ground isolators, terminations and low connector costs. Also, fewer cables help in better air-flow among components and subsequently reduces the cooling requirement for the servers. The wireline link can be treated as a channel with limited bandwidth, reflections and crosstalk issues. Apart from it, the performance of SERDES transceiver is also limited by noise, linearity, jitter, clock and data skew and bandwidth. At present, 112 Gbps links have been developed by several companies (Intel, Xilinx, Rambus, etc.) and still research is ongoing to find more power efficient wireline links for 100+ Gbps data rate. OIF (Optical Internetworking Forum) has characterized different channels based on their length or the attenuation they experience. These different types of channels are commonly categorized as MCM (multi chip module), XSR (extra short reach), VSR (very short reach), MR (medium reach) and LR (long reach) [4]. Application of these channels is shown in Figure 1.2. This research primarily focuses on the development of SERDES for LR channels. The LR channel considered in this research project is a backplane (may actually be a cable) with length $\sim$ 1m and offers channel attenuation of $\sim$ 30 dB (excluding package loss) at 28 GHz Nyquist frequency.

CEI-112G-MCM	3D Stack 2.5D Chip-to-Chiplet	CNRZ-5: up to 25mm package substrate No equalization/FEC Minimize power (pJ/bit)
CEI-112G-XSR	2.5D Chip-to-Chip Chip → Optics Chip to Nearby Optics Engine	PAM4: up to 50mm package substrate 6-10 dB at 28GHz Lite FEC, Rx CTLE
CEI-112G-VSR	Chip ← → Pluggable Optics Chip to Module	PAM4: 12-16 dB at 28GHz FEC to relax BER to 1e-6 Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE
CEI-112G-MR	Chip ← → Chip Chip-to-Chip & Midplane Applications	PAM4: 20dB at 28GHz FEC to relax BER to 1e-6 Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE
CEI-112G-LR	Chip ← → Chip Backplane or Passive Copper Cable	PAM4: 28-30dB at 28GHz FEC to relax BER to 1e-4 Multi-tap Tx FIR and Rx CTLE + multi-tap FFE or DFE

Figure 1.2: OIF CEI-112G Development Application Space [4].

1.2. Typical SERDES system
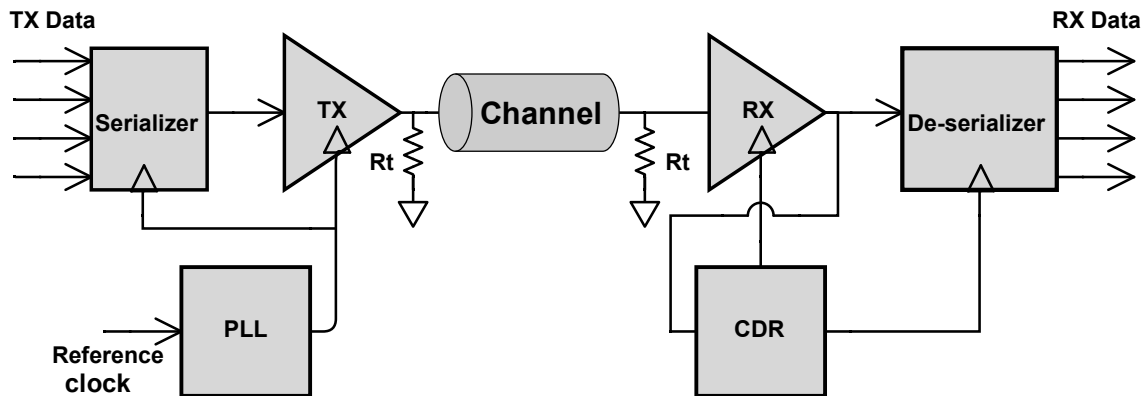
Figure 1.3: Typical SERDES transceiver system.

The block diagram of a typical SERDES transceiver system is shown in Figure 1.3. Parallel data stream goes into the serializer, which feeds the serialized data into the transmitter block. PLL (Phase Locked Loop) on the transmitter (TX) side scales up the clock frequency for the circuit as compared to low frequency external reference clock. Several data encoding techniques are used to modulate the data in the digital domain prior to the TX. The driver sends out the signals over the channel. The received analog signal gets attenuated by the channel and corrupted due to the noise and interference. Both TX and receiver (RX) should be terminated properly with the characteristic impedance of the channel transmission line to reduce reflections.

The receiver sub-system block includes RX core, CDR (Clock and Data recover block) and de-serializer. RX consists of equalization circuits (discussed in next section in detail) and DSP (Digital Signal Processing) unit to compensate for the signal attenuation. A CDR block at the receiver end helps to recover the clock frequency. The CDR block eliminates the need to feed-forward the clock signal through an additional channel from TX to RX. This has several advantages such as it is cost-effective as there is no need for an additional channel. Also, the clock can experience noise and attenuation like the received data stream and can also get skewed over the channel. Once the receiver produces the

digital data, the information can be retrieved by de-coding and de-modulation. Finally, de-serializer sends out the parallel data [5].

1.3. Thesis organization

The remaining thesis is organized as follows:

- **Chapter 2 - Background:** It provides the information about data modulation schemes and the need for equalization. It describes the latest trend in SERDES transceiver development with an emphasis on the state of the art Continuous Time Linear Equalizers (CTLE) . Later, it specifies the scope of this thesis.

- **Chapter 3 - Receiver Analog Front-end Design:** This chapter discusses the design considerations of the analog front end design in detail focusing towards low power operation while maintaining the key performance parameters.

- **Chapter 4 - Extracted Simulation Results:** This chapter presents the simulation results for extracted netlist of top-level layout. Further it compares the performance of the inverter based CTLE with other state of the art CTLEs and the conventional CML based CTLE.

- **Chapter 5 - Conclusion:** This chapter summarizes the thesis and discusses about the future directions for improvement in analog front end design.

2

Background

2.1. Data modulation techniques

The binary data is generally encoded with one of three modulation schemes - PAM-2, PAM-4 or Duobinary. PAM-2 (Pulse Amplitude Modulation with 2 levels) is also known as NRZ (Non Return-to-Zero) and maps the data bit to two symbols as $+V_p$ and $-V_p$ voltage levels. The PAM-4 modulation scheme combines the two consecutive bits into one symbol, resulting in four possible symbols or voltage levels (i.e. $+V_p$, $\frac{+V_p}{3}$, $\frac{-V_p}{3}$ and $-V_p$). So, PAM-4 has an advantage to transfer double data rate with same symbol rate as compared to PAM-2. But, there are certain disadvantages associated with PAM-4, which mainly includes less SNR (signal to noise ratio) and strict linearity requirements (beacause of the tigher spacing between voltage levels in PAM-4 as compared to PAM-2)

In Duobinary modulation, the modulator output is $w[n] = x[n]+x[n-1]$, where $x[n]$ is the present TX data bit and $x[n-1]$ is the previous data bit . In other words, the present bit at the modulator output is sum of present and previous data bit. So, it has some controlled ISI (Inter-Symbol Interference), which leads to low bandwidth requirement during equalization. However, there is a trade-off , design complexity of such modulators is comparatively high and it requires additional circuitry for detection/decoding of the received signals [6].

2.2. Need for equalization

All wireline links act as low pass filter by nature and exhibit significant attenuation at higher frequencies. As a result, the higher frequency signals are more attenuated and delayed as compared to lower frequency signals, which leads to ISI. ISI is the interference experienced by the current symbol that is caused by the previously transmitted symbol. The task of an equalizer is to invert the channel's frequency response and provide a flat frequency response till Nyquist frequency ($f = \frac{\text{symbol rate}}{2}$). Thus, most of the frequency components in the input signal will have same delay and gain/attenuation, leading to low ISI in time domain.

As an example, an LR channel model (IEEE channel) [7]) is chosen for analysis for 56 Gbps PAM-2 PRBS (Pseudo Random Bit Sequence) with PN-32 data sequence input data. Figure 2.1 shows the channel has an attenuation of $\sim$ 30 dB at 28 GHz Nyquist frequency. An approximate model of the CTLE in ideal scenario is realized which provides $\sim$ 18 dB equalization against the requirement of 30 dB equalization. This amount of linear equalization is practically realizable and beneficial (explained in the next section). Remaining equalization is expected from the further equalization stages.

The time-domain impact of this equalizer can be seen in Figure 2.2 through the pulse response at the channel and CTLE output. The channel's pulse response for 56 Gbps bit width shows a lot of pre and post cursors which leads to ISI and are thus undesirable. Ideally, we expect the pulse response to be a dirac-delta function. The equalizer model considered previously works fairly well in removing several pre and post cursors. Theoretically, the input signal to a channel convolves with its impulse response to produce the time domain output. The best way to visualize the medium's time domain response is through an 'eye-diagram'. An eye-diagram is realized by clipping the received signal into one unit interval time frame and superimposing each clipped block over each other. In the absence of ISI, we expect the eye to be wide-open, which corresponds to a
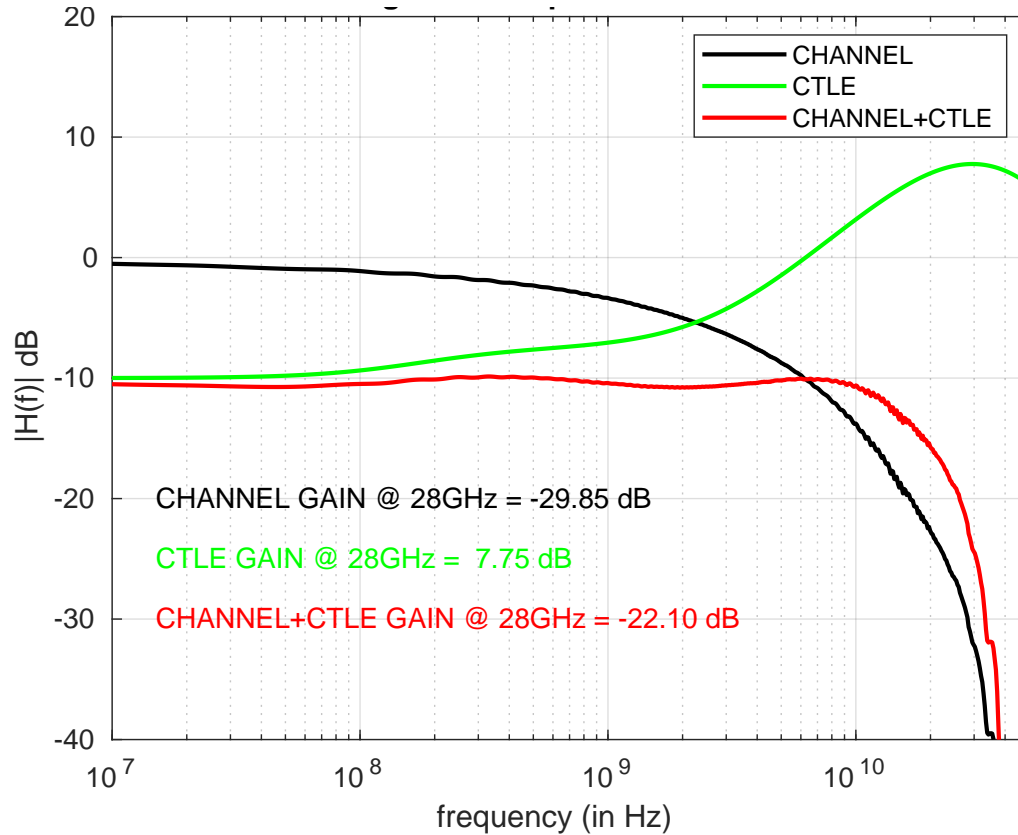
Figure 2.1: Backplane channel and CTLE magnitude response.

low bit-error-rate (BER). Figure 2.3 shows the effect of the equalizer in opening the eye as compared to the entirely closed eye at the channel's output.

Equalization can be achieved in either the continuous time or discrete-time mode. It can also be categorised into linear or non-linear mode of operation. The equalizer model explained earlier is an implementation of linear equalizer in continuous time mode . The issue with such equalizer (CTLE) is that it not only boosts high frequency signal content but also amplifies the noise. This poses a limitation on the amount of equalization that can be achieved through linear analog equalization. The discrete-time equalizer needs a clock signal and is jitter sensitive. So for these equalizers, it is expected to have minimal eye opening at their input in order for them to function properly. Typical examples of discrete-time equalizers are DFE (Decision Feedback Equalizer) and FFE (Feed-Forward Equalizer). The advantage with these equalizers is that they are easily programmable.
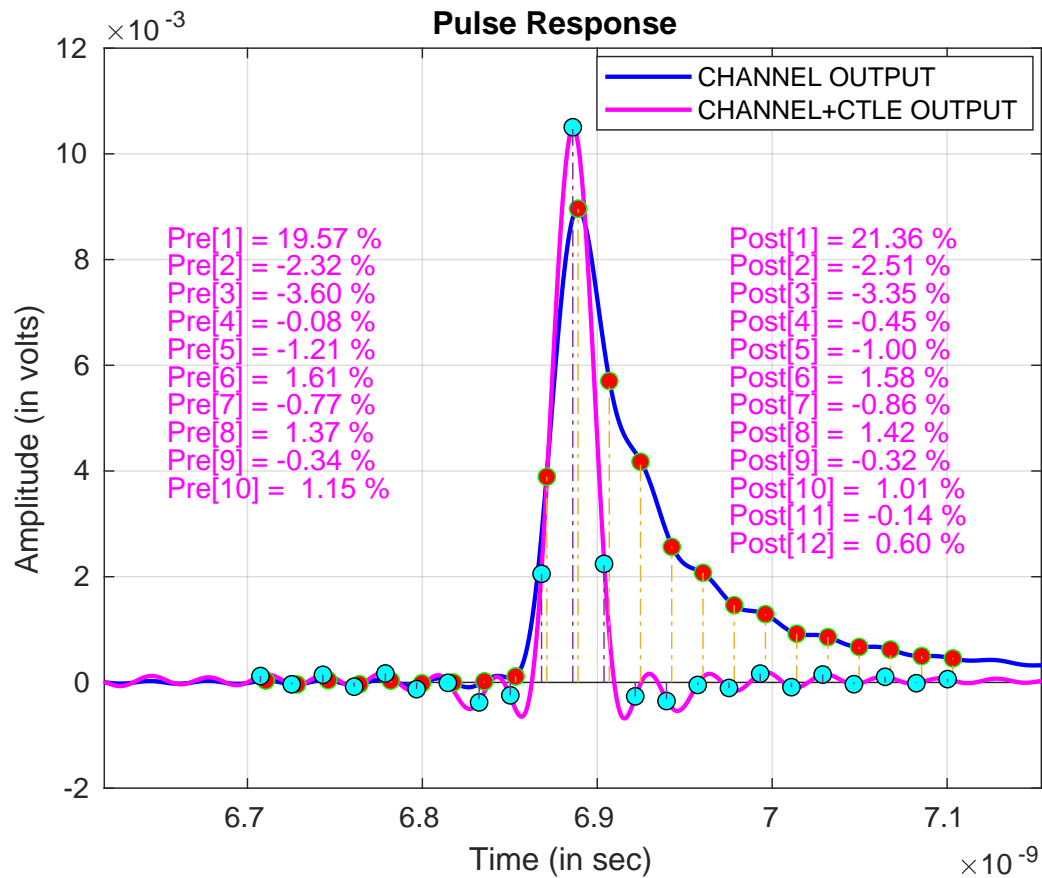
Figure 2.2: Pulse response at the channel and the CTLE output (with partial equalization).

DFE in particular, is a non-linear discrete time equalizer and it does not amplify the noise whereas linear equalizers do amplify the noise.

2.3. Recent trend in the development of LR 112 Gbps SERDES

The choice of data modulation is extremely important for LR channels. Traditionally, PAM-2 modulation technique used to be the preferred choice for data rates less than 56 Gbps, since it is more immune to noise and has lenient linearity requirements. But for higher data rates (112 Gbps) and with higher attenuated channels, PAM-4 modulation is preferred [8]. It is due to the fact that the Nyquist frequency in the case of PAM-4 data stream is the quarter of the data rate while in the case of PAM-2 modulation, it is half of the data rate. If we look at the magnitude response of the LR channel in Figure
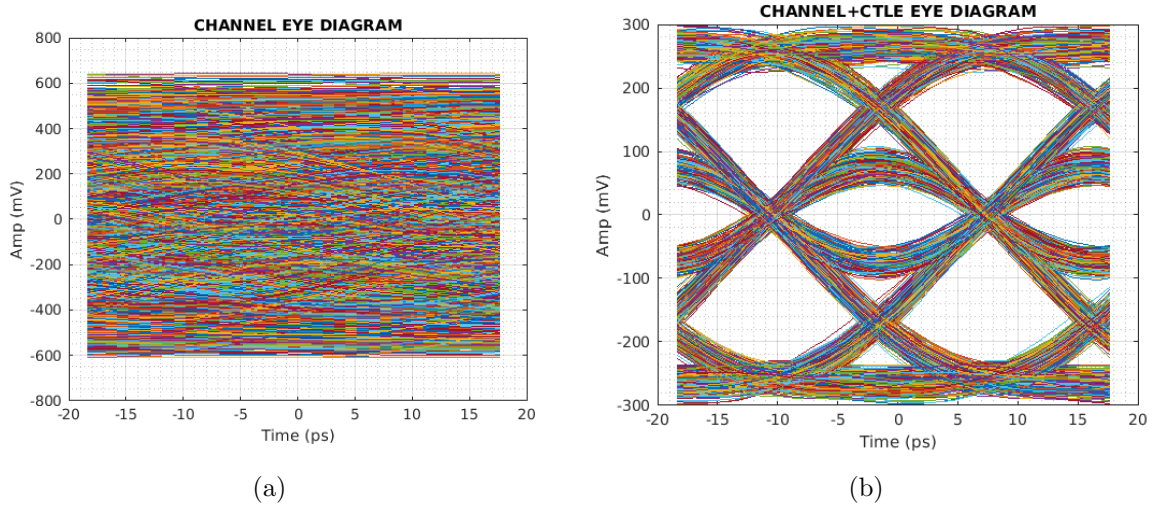
Figure 2.3: Eye diagram: (a) at channel output; (b) at CTLE output with partial equalization.

2.1, the equalizer needs to equalize till 56 GHz in case of PAM-2 modulation whereas in the case of PAM-4, it is 28 GHz. Since the channel roll-off is steep at higher frequencies, PAM-4 is the preferred choice. However, there are certain drawbacks associated with it which have been discussed in Section 2.1.

For an LR channel, single equalization stage is not capable enough to fully equalize the channel. Hence, equalization is achieved in multiple stages. Now, an important question to pose here is how much equalization should be achieved through each stage in order to have minimum area and power consumption while meeting adequate performance? Several circuit blocks have been reported in the literature in this regard [9].Generally, some fraction of equalization in carried out on the TX side while remaining equalization is done on the RX side. Table 2.1 shows that most of the equalization is done on the analog side for lower data rates [9]. However, with higher data rates (of 100+ Gbps), designers are moving towards an ADC based receiver which digitizes the analog signal using ADC post the CTLE stage and carries out digital signal processing to achieve the remaining equalization as shown in PPA (Power, Performance and Area) analysis in Table 2.2 [9]. This has been enabled due to the low power consumption for the digital circuits realized via transistor scaling. Figure 2.4 shows the conventional SERDES

transceiver architecture for lower data rates while Figure 2.5 shows a typical modern

SERDES transceiver architecture for higher data (100+ Gbps).

Table 2.1: Equalization component PPA analysis with data rates $\leq$ 56 Gbps [9].

	Power	Performance	Area
TX FIR	✓	✓	○
RX CTLE / VGA	✓	✓	✓
RX Analog DFE	○	✓	○
RX Analog FFE	✗	✗	✗
RX ADC	✗	○	✗
RX DSP FFE/DFE	✗	✓	✗

- Legends: ✓: good ✗: poor ○ : fair/medium
- ADC consumes power and area at larger process nodes.

Table 2.2: Equalization component PPA analysis with data rates $\geq$ 56 Gbps [9].

	Power	Performance	Area
TX FIR	✓	✓	○
RX CTLE / VGA	✓	✓	✓
RX ADC	○	○	✗
RX DSP FFE	✓	✓	✓
RX DSP FFE	✗	✓	✗

- Legends: ✓: good ✗: poor ○ : fair/medium
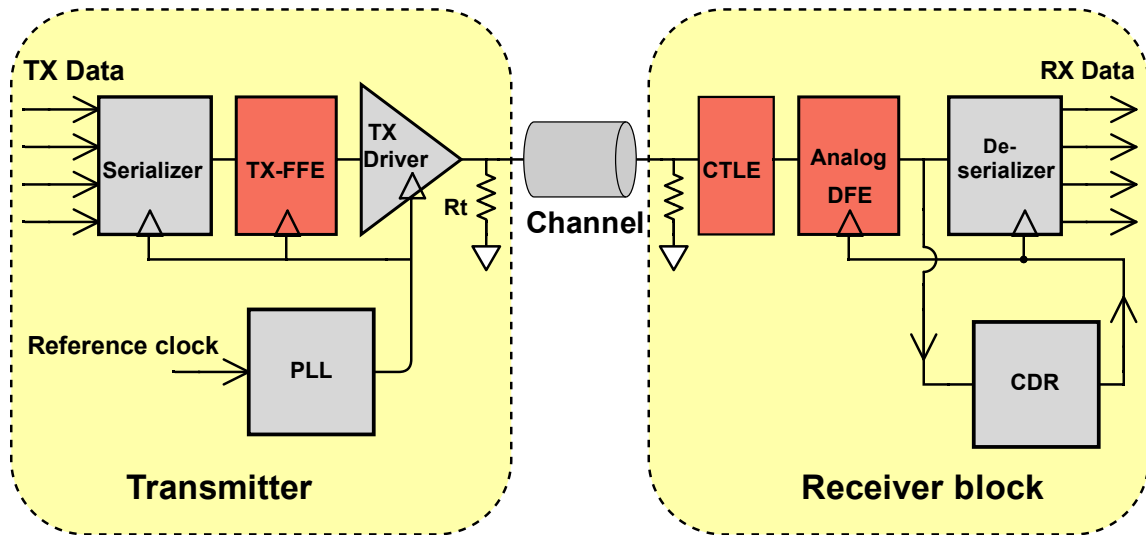
Figure 2.4: Conventional equalization architecture for data rates ≤ 56 Gbps (with equalizers highlighted in pink colour).
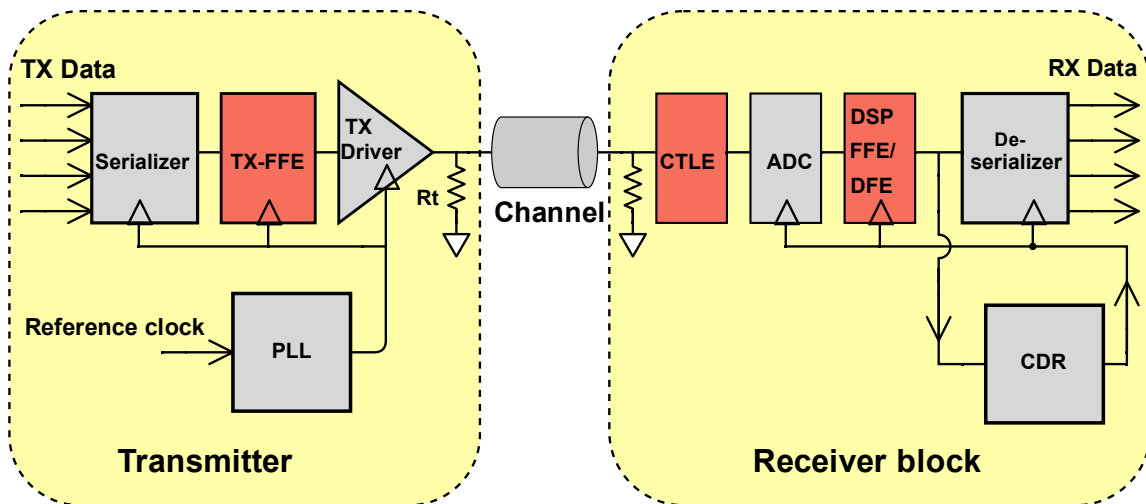
Figure 2.5: Next generation equalization architecture for higher data rates (100+ Gbps) (with equalizers highlighted in pink colour).

2.4.   State of the art : Previous CTLE architectures

The pre-ADC equalization becomes very important in modern SERDES architecture. Its function is not to fully equalize the channel but to relax the ADC and DSP design requirements [10]. PMR (Peak to main signal ratio) of a channel is defined as the ratio of the sum of all cursors to the main cursor in the pulse response [11]. Frans *et al* reported that a 6 dB improvement in PMR helps to save one bit of the ADC resulting in better power performance [12]. It also reduces the RX-FFE noise boosting due to the reduced FFE coefficients [10].

The conventional CML (current mode logic) based CTLE architecture is shown in Figure 2.6. The pole and zero locations of the CTLE are controlled by the source degeneration impedance. This architecture has been widely adopted over the past years [13–16]. But with the scaling of the transistors and the reduced power supplies, CML based architecture does not deliver power efficient solution. Moreover, this architecture utilizes passive inductors to push the bandwidth, which results in higher area consumption.
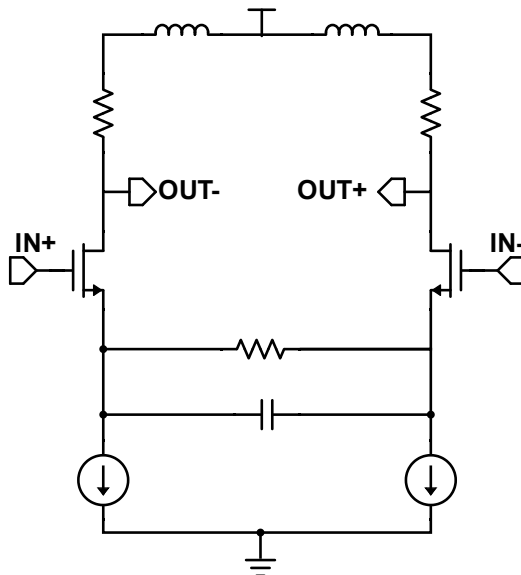
Figure 2.6: CML based conventional CTLE architecture.

In order to save some inductor area and extend the bandwidth, negative capacitance

circuit (NCC) has been used to reduce the load capacitance as shown in Figure 2.7 [17]. But this solution is again power hungry and challenging to realize high frequency negative capacitance.
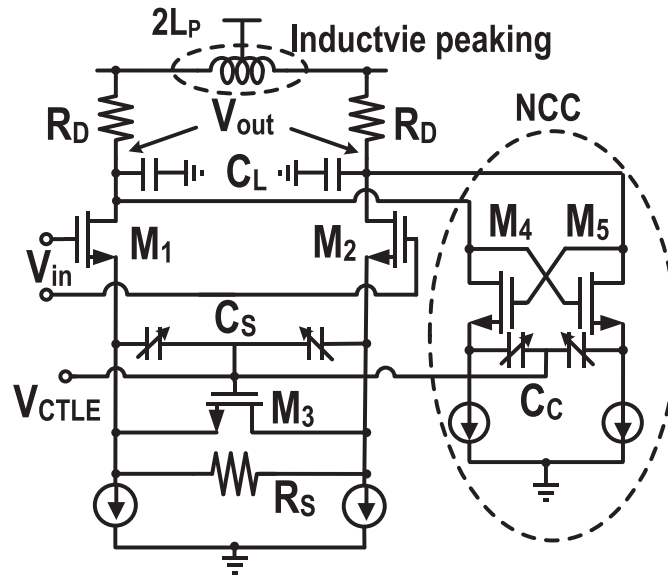
Figure 2.7: CML based conventional CTLE architecture with negative capacitance implementation [17].

However, CMOS inverter based architecture (shown in Figure 2.8) does in fact take the advantage of technology scaling and can offer power-efficient solutions (explained in the next chapter). It generally includes a cascade of passive equalizer and an active amplifier. It has shown potential benefits in terms of area and power reduction [18], [19]. A typical inverter based CTLE architecture [19] is shown in Figure 2.9.
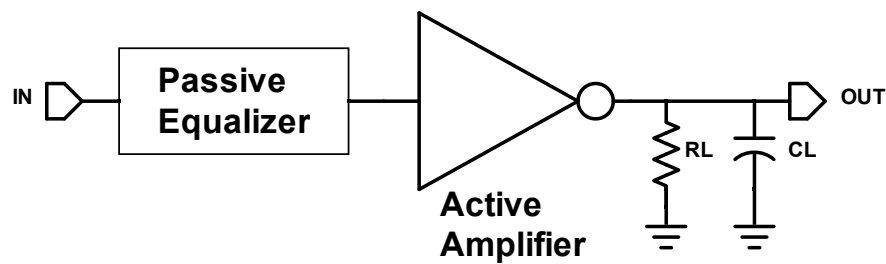
Figure 2.8: CMOS inverter based CTLE.
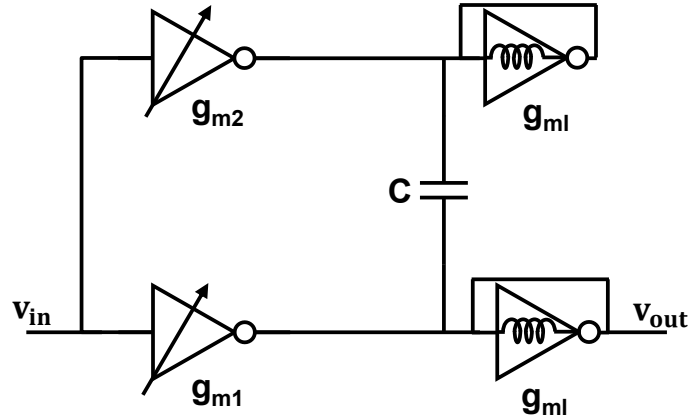
Figure 2.9: CMOS inverter based CTLE for PAM-2 application [19].

There is another CTLE architecture proposed in [20] which makes use of a combination of both CML and CMOS inverter based designs (shown in Figure 2.10). This design has good CMRR (Common mode rejection ratio) and low power consumption. The front high pass filter eliminates low frequency content and sets the low cutoff frequency for input data stream.
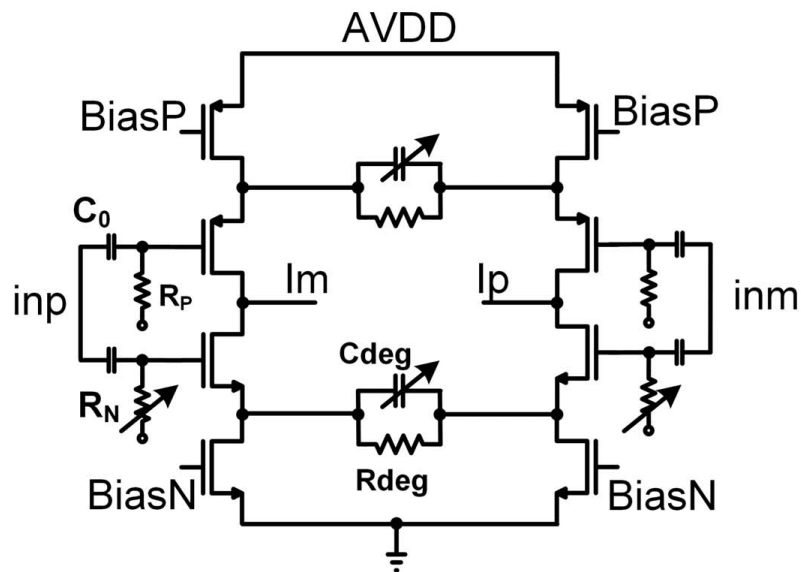
Figure 2.10: CML and CMOS inverter based CTLE [20].

2.5. Thesis scope

Driven by the trending research in the high speed SERDES development, this thesis focuses on developing a new CMOS inverter based architecture for analog front end design of a long-reach 112 Gbps PAM-4 SERDES receiver. It should provide energy-efficient equalization solution while maintaining satisfactory noise performance, linearity, power supply noise rejection and programmability options. The design will be implemented in 16nm FinFET CMOS technology which will land on a flip-chip BGA (Ball Grid Array) package substrate.

3 Receiver Analog Front-end Design

3.1. Long-reach channel

In this project, the RX application is designed for 1m long backplane channel, which provides ~ 30 dB attenuation at the Nyquist frequncy of 28GHz. Frequency and pulse response characteristic of this long reach channel model (provided by ieee803.ck) for an ideal termination of 50 Ω is shown in Figure 3.1. However, when the channel is connected with the input of the receiver, it no longer remains ideally terminated and exhibits an attenuation ~ 36 dB due to the package and on-chip parasitics. To improve the additional attenuation due to package and on-chip parasitics, a front-end termination network is used so that there is minimal addition attenuation at high frequencies.

3.2. Front-end termination network

The front-end termination block is the portion of the receiver from the channel output to the CTLE input. The receiver input can have DC or AC coupling from TX through the channel depending on the application. In our case (AC coupling), there is $\approx 1\mu F$ off-chip coupling capacitor, which ensures to block signals only below 3.2 KHz as per equation 3.1. However, this large capacitor will have parasitic inductance and own self-resonance frequency. The latter should be much greater than the Nyquist frequency. If this does not happen, we can decrease the value of off-chip capacitor provided it does not hurt
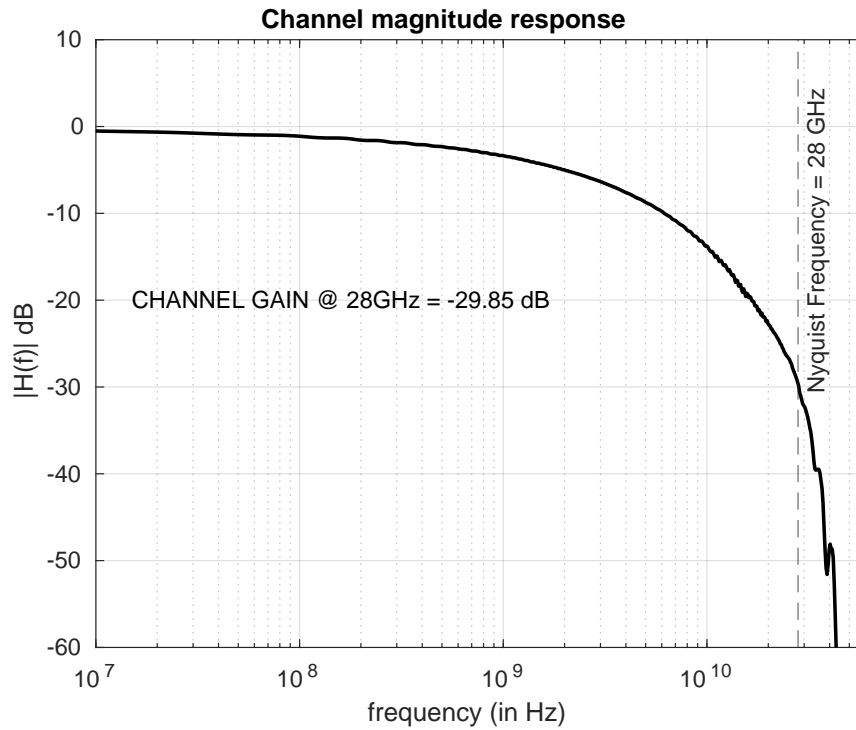
(a)
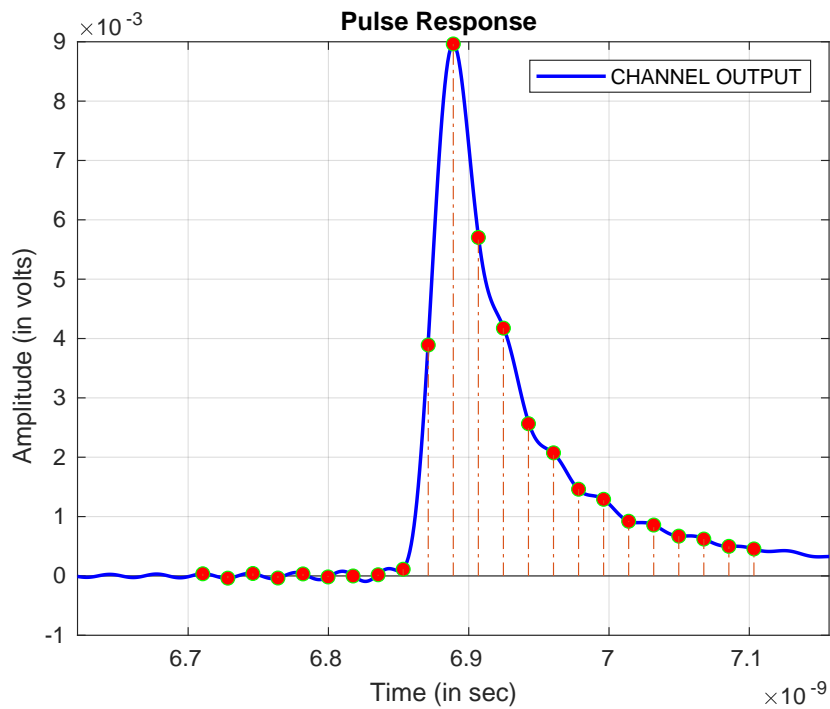
(b)

Figure 3.1: LR channel characterization with ideal 50 Ω termination: (a) Magnitude response shows 30 dB loss at 28 GHz Nyquist frequency; (b) Pulse response for pulse width corresponding to 56 Gbps data-rate; showing the pre, post and main cursors.

lower cut-off frequency intended for our application.

$$f_z \approx \frac{1}{2\pi R_t C_{off-chip}} \tag{3.1}$$

In high speed SERDES, the frequency of the input data stream does not go that low due to 8b/10b or 64b/66b coding, which is required to avoid baseline wandering due to long stream of 1s or 0s. AC coupling enables the designer to set the input common-mode voltage level of the CTLE. The front-end termination block is shown in Figure 3.2.
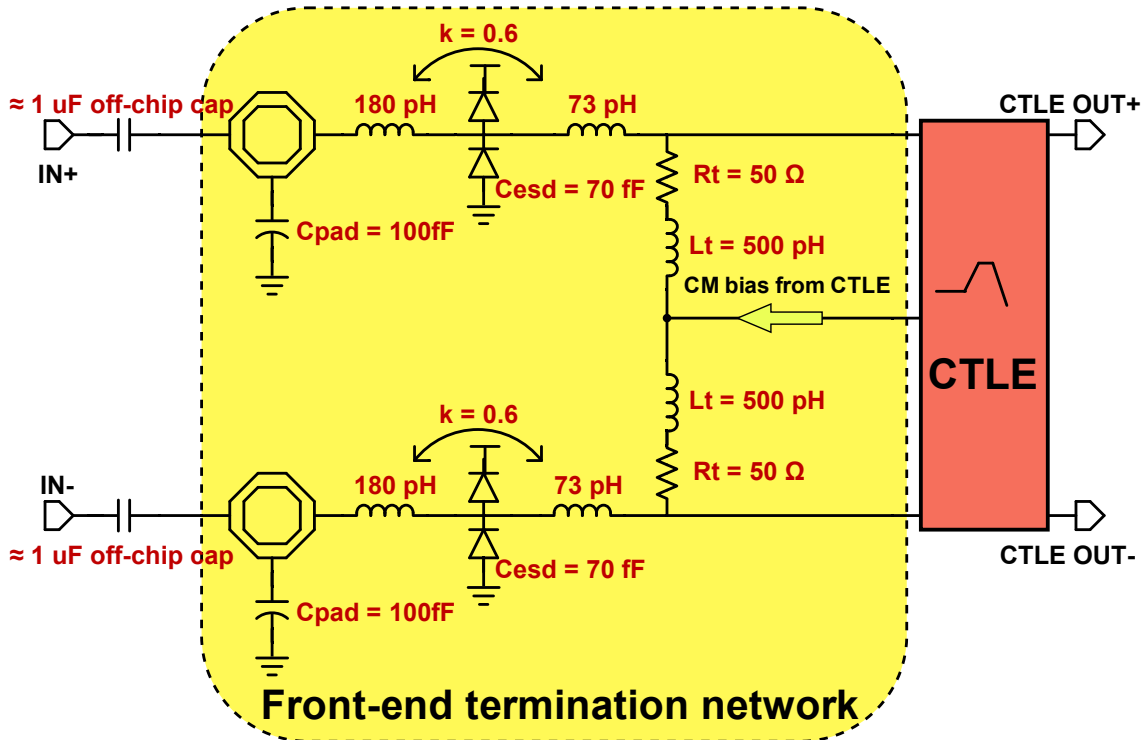
Figure 3.2: Front-end termination network.

The signal enters the CMOS die through C4 solder bump pads, which then passes through the Tcoil, ESD cell and other passive circuitry for providing proper termination with channel's characteristic impedance ($\approx$ 50 Ω). The explanation about various components in this network is given below -

Parasitic capacitors: The bump pad area is $\approx$ 80 µm x 80 µm. Upon extraction

in layout and having some safety margin, pad capacitance is nearly 100 fF. Additionally, there is always some level of HBM (Human Body Model), CDM (Charged Device Model) and MM (Machine Model) ESD protection requirement. Since the input signal is a high speed path, there is only primary ESD diode for protection. The ESD capacitance value is $\approx$ 70 fF upon extraction. In addition to these parasitic capacitances, there is an additional loading by CTLE input. These parastitics further degrade the transmission (S_{21}) response of the channel. However, with the help of Tcoil and another inductor L_t, we have boosted the signal and provided passive equalization.

Bandwidth enhancement with T-coil: T-coil is an old technique developed in 1920s to extend bandwidth of the circuit. The design and usage of T-coil is well explained in [21]. Since ESD and bump pads are unavoidable, T-coils have proved to be very beneficial in extending the bandwidth of the circuit in [22–25]. The circuit diagram shown in Figure 3.2 shows the parameters of an asymmetric T-coil chosen for this design. The use of T-coil is advantageous because the capacitors associated with the middle node can be nullified to a certain extent by mutual coupling between the split inductors. The functioning of T-coil network is explained in [23]. The parameters of the T-coil are chosen such that it provides an adequate magnitude response at the CTLE input in addition to the termination requirements.

Inductor load, L_t for passive equalization: Generally the use of only T-coil is mentioned in research papers for bandwidth extension. For data rate exceeding 100 Gbps, we have to provide additional boost by using a passive inductor L_t. The need for T-coil as well as additional inductor L_t can be understood from the waveforms shown in Figure 3.3. It is shown that if the channel is terminated with only ideal resistor = 50 Ω (which matches with the characteristic impedance of the channel), then the channel's magnitude response shows $\approx$ 30 dB attenuation at Nyquist frequency. If the channel is terminated with a network similar to shown in Figure 3.2 but without any T-coil and L_t, then the magnitude response at CTLE input drops to $\approx$ -35 dB. The inclusion of T-coil

to that network improves the magnitude response by 2 dB and finally with the proposed
architecture (with T-coil and L_t included), the magnitude response improves further by
3 dB and becomes almost similar to the case if the channel is terminated ideally.
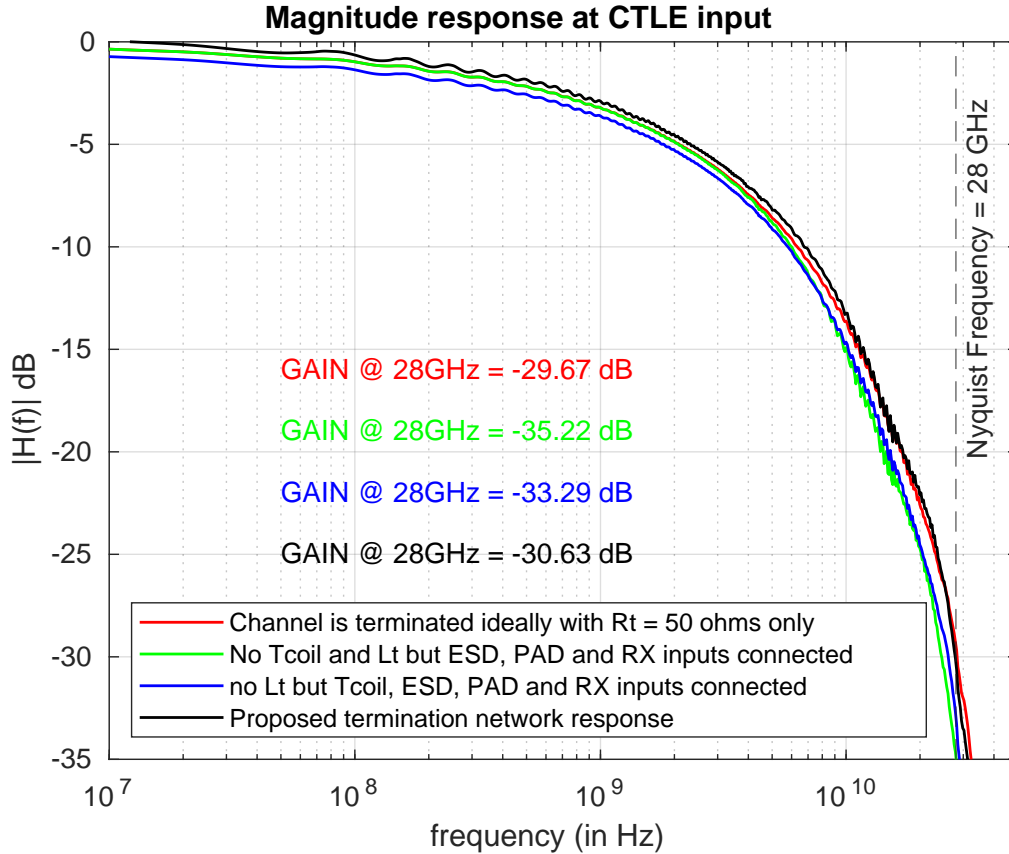
Figure 3.3: Magnitude response from channel input to CTLE input due to various termination
circuits. Proposed architecture behaves closest to the case when the channel is terminated
ideally.

The transfer function of the proposed network is shown in Equation 3.2, where L_t
term in the numerator helps to have sufficient gain at high frequencies. The derived
transfer function ignores parasitic capacitance of the elements in the proposed network.
In addition, the CTLE input impedance is assumed to be very high than R_t value.
The approximated transfer function provides good understanding of the network. The
magnitude response of this transfer function for different L_t values is shown in Figure 3.4.
The overall impact of the different values of L_t on the channel and the front-termination
network is shown in Figure 3.5. Finally a value of $L_t = 500$ pH is chosen that provides

the required passive equalization. It should be taken care that the self-resonance of this inductor is greater enough than the Nyquist frequency. The inductors and T-coils in this project are laid out in M10-M11 and then their extracted models are generated using EMX simulation tool.

$$H(s) = \frac{-C_{esd}L_t M s^3 - C_{esd}MR_t s^2 + L_t s + R_t}{(-C_{esd}M^2 + C_{esd}L_1 L_2 + C_{esd}L_1 L_t)s^3 + C_{esd}L_1 R_t s^2 + (L_1 + L_2 + L_t + 2M)s + R_t} \tag{3.2}$$
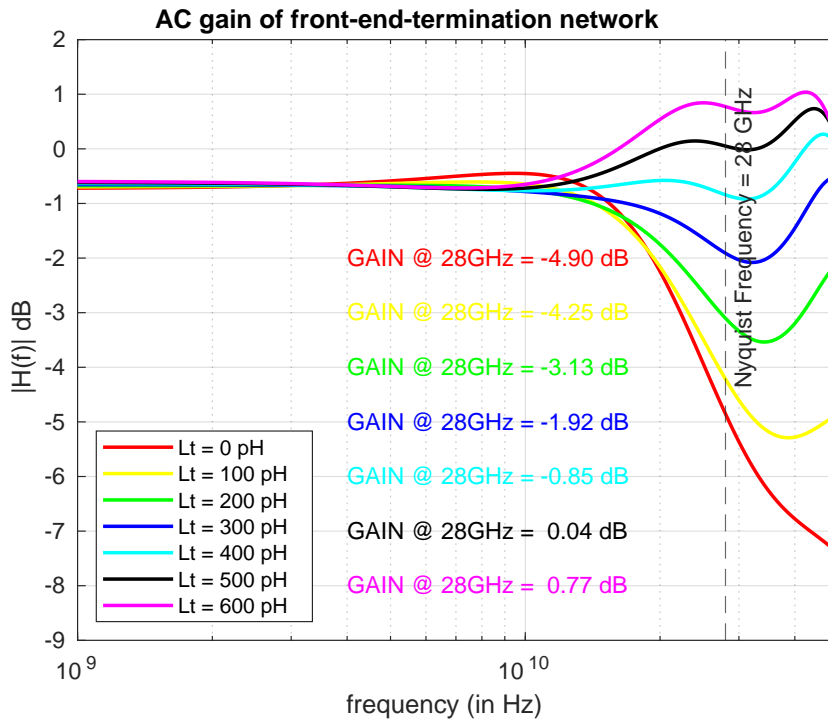
Figure 3.4: Magnitude response of front termination network from the channel output to the CTLE input with variation in L_t for the proposed architecture.
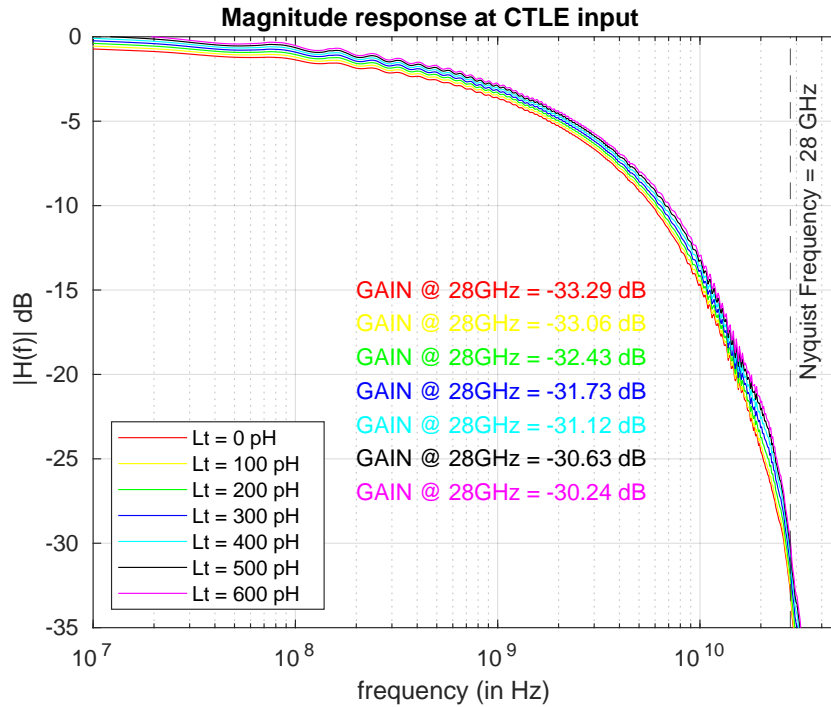
Figure 3.5: Magnitude response from channel input to the CTLE input with variation in L_t for the proposed architecture.

3.3. CTLE design

The analog front end block diagram is shown in Figure 3.6, which includes the front passive termination block (already discussed), CTLE core, an output buffer to take the high speed signals off-chip. and finally a back-end passive network to extend the bandwidth using T-coil. The CTLE core consists of three stages namely high frequency boost stage, mid-band boost stage and final buffer stage to drive a 100 fF capacitive load. This capacitive load is the expected load for the front-end sampler of a 64-way time-interleaved ADC. There is an ADC as a following block according to modern SERDES architecture for LR channel, but we have limited our research to the CTLE design only.

The CTLE design is implemented using CMOS tristate inverter as driver and active load in certain stages. The tristate nature of the inverter allows better tunability options, which are discussed later in this chapter. The CMRR of a CMOS inverter amplifier (generally CMRR $\leq$ 0 dB) is worse than that of a current source based differential
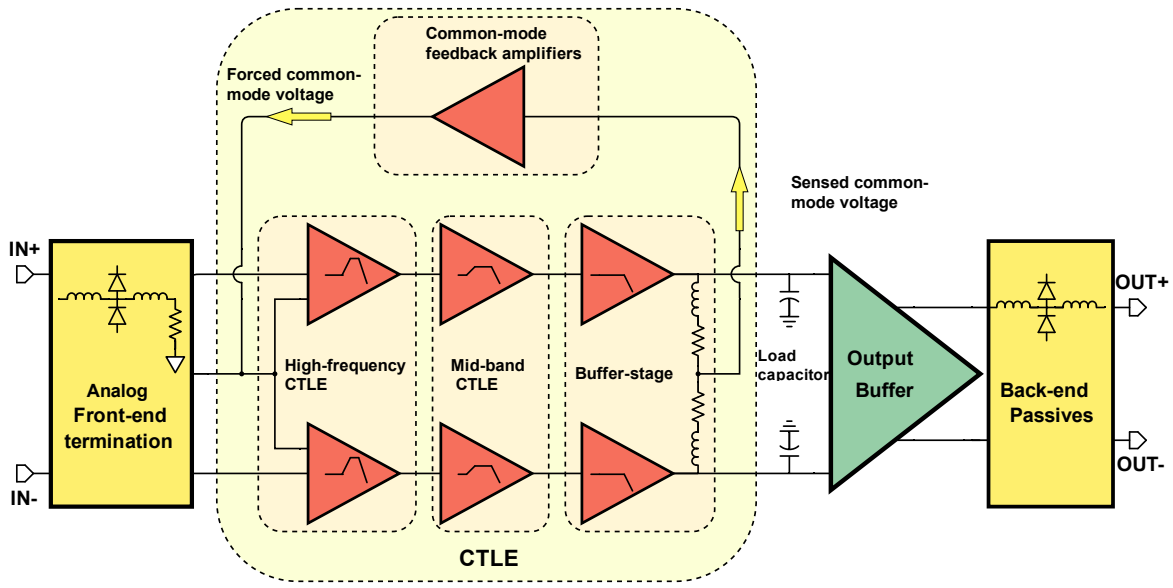
Figure 3.6: Analog front end block diagram showing three stage CTLE.

amplifier (CMRR $>> 0$ dB and ideally CMRR $= \infty$ for ideal current source). In addition, this CTLE architecture needs to have a proper common-mode bias voltage to ensure adequate biasing for amplification. There is a feedback loop to provide common-mode bias voltage and and to improve the CMRR and PSRR (Power Supply Rejection Ratio). The benefits and limitations of the feedback loop are discussed in Section 3.3.5.

3.3.1. Basic design elements used in CTLE

The CTLE architecture uses certain basic elements multiple times, which include CMOS tristate inverter as an amplifier, a diode-connected load and an active inductor. Inverter is used extensively in digital circuits however they can be used as good analog building blocks provided they are biased properly. the strength of these cells are made tunable using enable and disable switches.

3.3.1.1. CMOS tristate inverter as a basic amplifier unit

This section will discuss the reasons for choosing to use CMOS tristate inverter cell (shown in Figure 3.7) as a basic unit instead of the conventional current source based differential amplifier (shown in figure 3.8). The primary advantage of using a differential

amplifier is that it has better CMRR as compared to the CMOS inverter operating as an amplifier. But there are certain disadvantages too, which have been discussed later in detail in this section only.

The small-signal model of the circuit shown in Figure 3.8 can be analysed to find small-signal DC gain described in Equation 3.3.

$$A_v = \frac{V_{out}^+ - V_{out}^-}{V_{in}^+ - V_{in}^-} = \frac{V_{out} - (-V_{out})}{V_{in} - (-V_{in})} = \frac{V_{out}}{V_{in}} = g_{m_n} \cdot \left(\frac{Z}{2} \parallel r_{ds,n}\right) \tag{3.3}$$

Further since in CMOS FinFET technology, the mobility, strength and other parameters of the PMOS and NMOS are almost the same, it is fair to assume that $g_{m_n} \approx g_{m_p} = g_m$ and $rds_n \approx rds_p = rds$ for the NMOS and PMOS respectively. Also, with the assumption that Z $\ll$ rds, the overall DC gain of the differential amplifier can be evaluated using Equation 3.4.

$$A_v(\text{differential amplifier}) \approx g_m \cdot \frac{Z}{2} \tag{3.4}$$

However, the DC gain for small-signal model of CMOS inverter amplifier (shown in Figure 3.7) is given in Equation 3.5.

$$A_v(\text{inverter amplifier}) \approx g_m \cdot Z \tag{3.5}$$

Advantages of CMOS inverter as an amplifier over differential amplifier: It is evident from the DC gain equations that for the same bias current, CMOS inverter cell provides twice the gain as compared to the differential amplifier. This high gain results from the transconductance which is twice in the case of CMOS inverter. Another limitation of the differential amplifier is that it requires higher supply voltage to keep its three-stack transistors in saturation that too with some margin. On the other side, the inverter cell is a 2-stack transistor architecture and needs less supply voltage for adequate biasing. With the transistor scaling, the supply voltages are becoming less than 1 V and
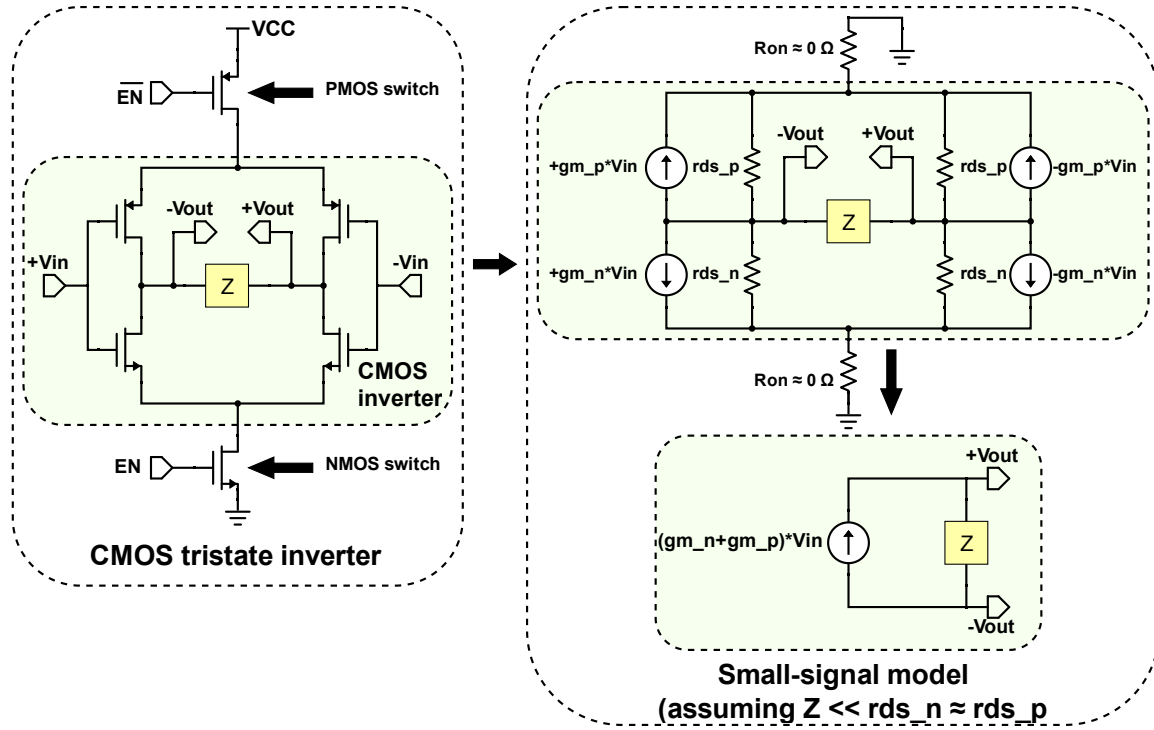
Figure 3.7: Analysis of CMOS tristate inverter cell as an amplifier.
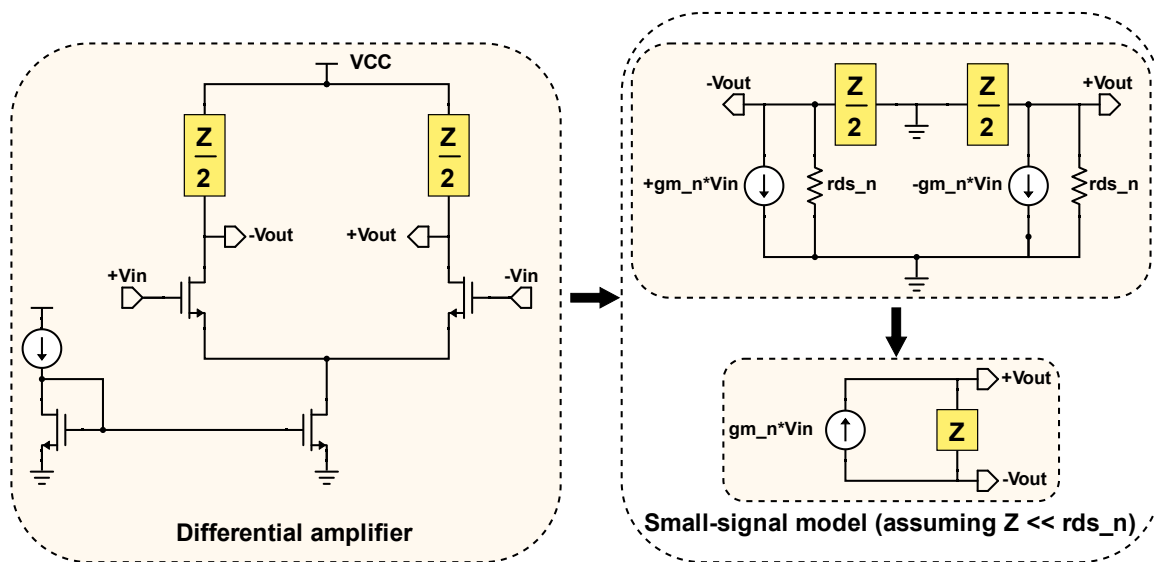
Figure 3.8: Analysis of CML based differential amplifier.

high-stack architectures are difficult to design and becoming obsolete. So, these two
are the primary reasons for choosing inverter cell as a low-power amplifier. In addition,
the enable/disable feature in the tristate CMOS inverter unit provides a tunability knob
which allows to have a power-scalable design. This has been used extensively throughout
the whole design.

However, the CMOS inverter has some disadvantages in terms of PSRR and CMRR.
Another disadvantage is that the common-mode level at the inverter inputs and out-
puts is mid-rail, which is incompatible with many/most other analog amplifier stages
under low supply voltages, such as the source-follower, common-source, most high-speed
comparators etc.
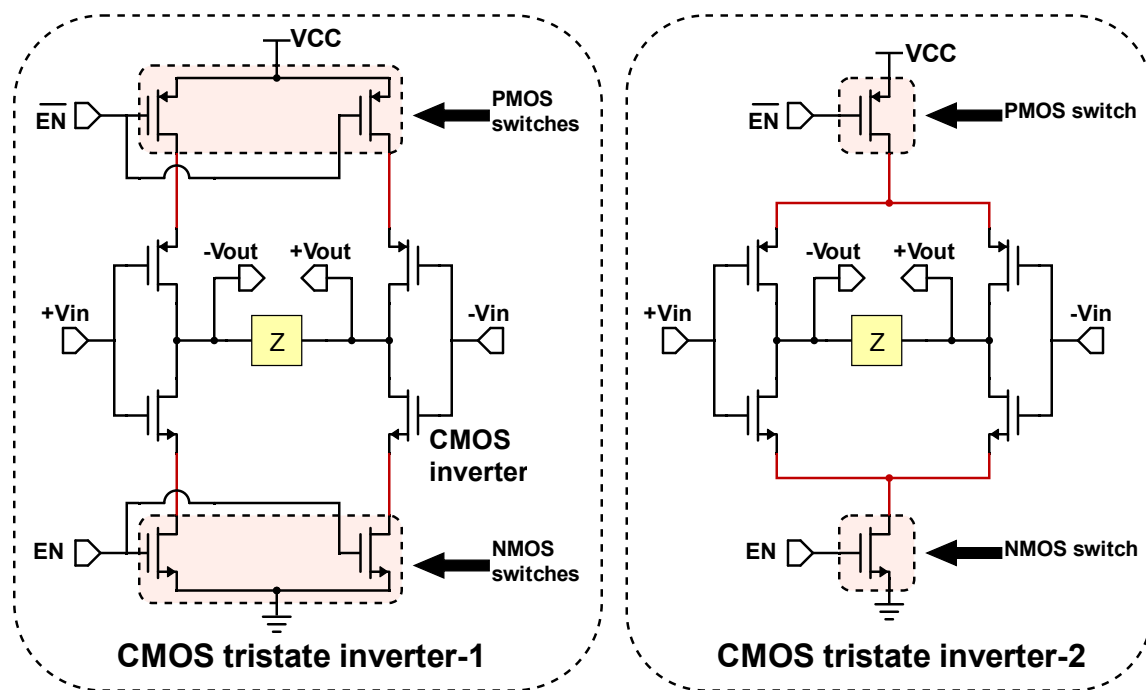
Figure 3.9: CMOS tristate inverter configuratios as an amplifier.

Further, there can be different architectures for an inverter-cell as an amplifier as well.
Two of them are shown in Figure 3.9. The CMOS tristate inverter-1 architecture provides
lower transconductance g_m due to the source degeneration caused by the resistance of
the switch in ON mode. On the other hand, the CMOS tristate inverter-2 architecture

provides higher transconductance g_m for the same bias current as there is no source degeneration because the common source node is virtually grounded. Hence, the CMOS tristate inverter-2 architecture has been adopted as the basic unit in this work. Inverter-2 architecture in this work is one of the primary differences between this design and that in [10] where Inverter-1 architecture was used.

There can also be a third type of amplifier which is shown in Figure 3.10. In this configuration, the main driving transistors and the switch transistors are swapped. But this architecture requires large switch sizes and has more parasitics. Thus, it is discouraged for our intended application.

CMOS tristate inverter-3
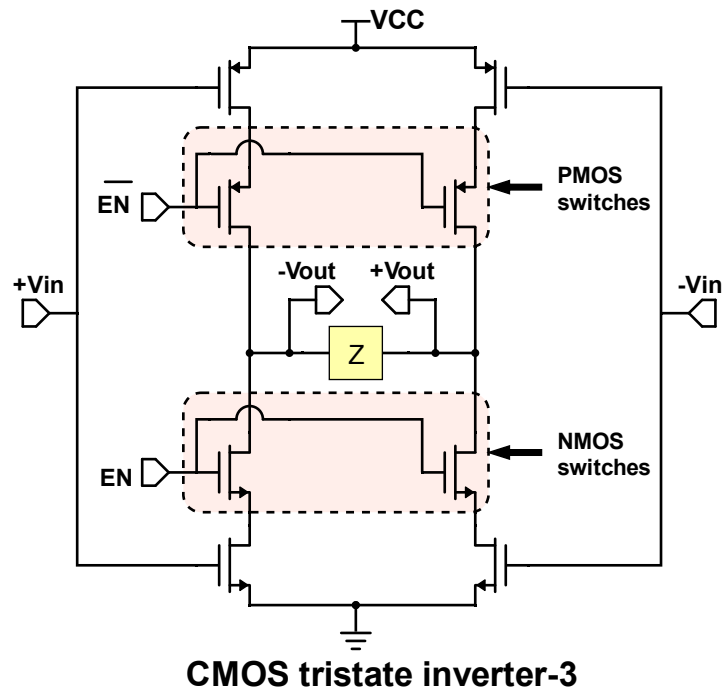
Figure 3.10: CMOS tristate inverter architecture with switches away from ends.

Since, the inverter driver will be used several times in the design, its symbolic representation alongwith its circuit diagram is shown in Figure 3.11 for better understanding.
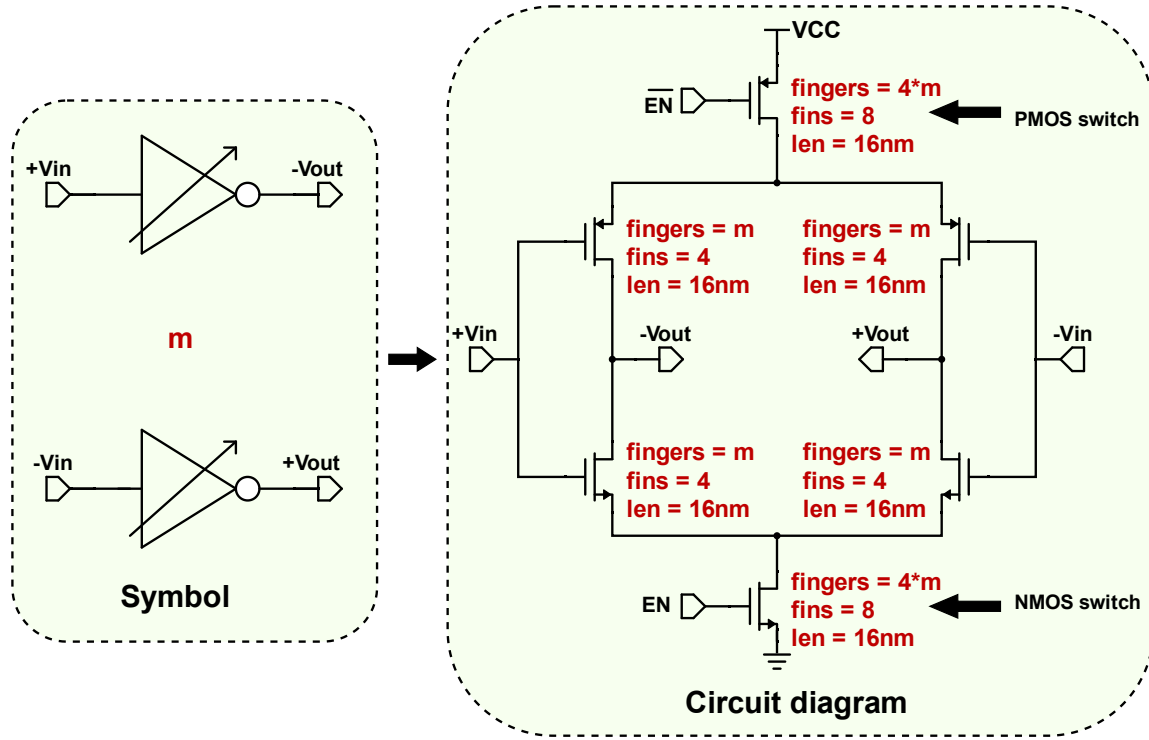
Figure 3.11: Tristate inverter symolic representation.

3.3.1.2. Inverter as tunable active resistor : diode-connected load

The diode-connected load acts as an active resistor (shown in Figure 3.12) with an effective input resistance as given in Equation 3.6.

$$R_{in}(diode\ connected\ load) = \frac{1}{2(g_m + g_{ds})} \tag{3.6}$$

Generally, the output transconductance g_{ds} is very small as compared to the transconductance g_m. Since the self-gain $\frac{g_m}{g_{ds}}$ is pretty high (≈ 15) for FinFET technology, so the g_{ds} term can be ignored and the final input resistance is given by Equation 3.7.

$$R_{in}(diode\ connected\ load) \approx \frac{1}{2g_m} \tag{3.7}$$

This resistor can be tuned by changing the strength of the transistors through series enable/disable switches. Not only this resistance is tunable, it also acts as a very good
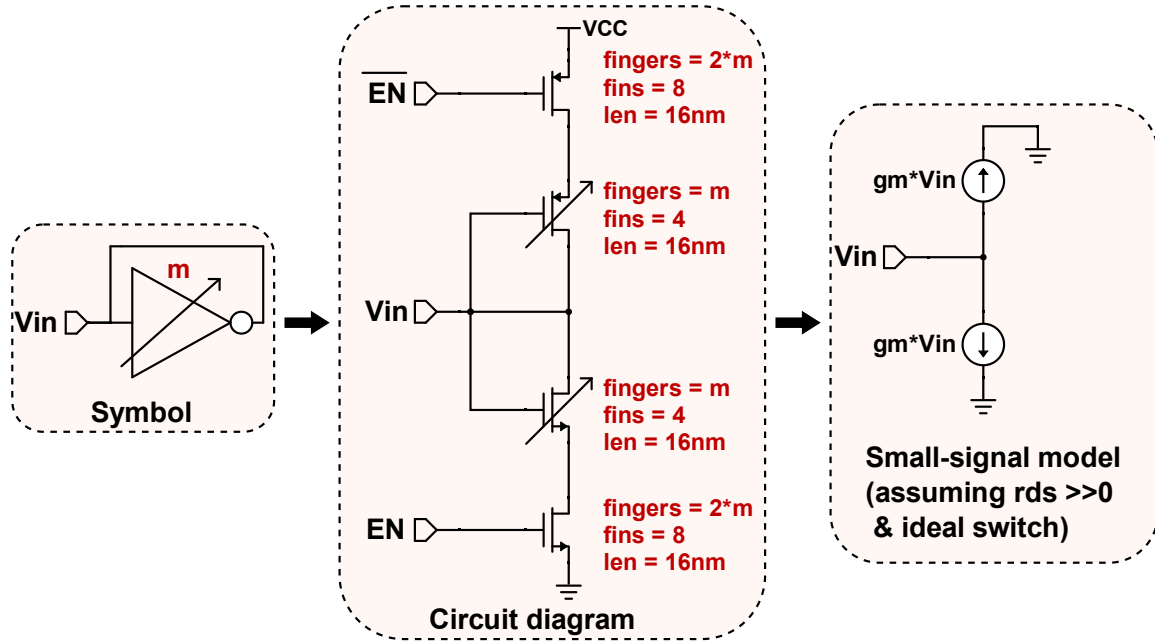
Figure 3.12: Tunable active resistor.

biasing circuit. Because of the negative feedback due to shorted gate and drain of the transistors, the input node gets biased at nearly half of the supply voltage. However, the bias voltage may be slightly different from the mid-rail supply voltage if the PMOS and NMOS have different strengths, which is unlikely in the case of FinFETs. This self-bias feature of the diode-connected load can be exploited to bias the drain node of the inverter amplifier.

The CMOS inverter (which is a tranconductance amplifier) with a self-biased diode-connected load works as a voltage amplifier. This combination will be used multiple times throughout the CTLE design. Another benefit of using this configuration is that the DC gain (given in Equation 3.8) is PVT insensitive. But these benefits come at the cost of power. Especially, a small valued active resistor is very power hungry as it requires a high g_m value.

$$DC\ Gain\ (inverter\ with\ diode\ connected\ load) = \frac{g_{m_{driver}}}{g_{m_{diode-connected-load}}} \tag{3.8}$$

3.3.1.3. Inverter as tunable active inductor

Inverter cell can be used as an inductor to reduce the area overhead caused by passive coil-based inductors. The active inductor architecture used in this design is shown in Figure 3.13. Ignoring the output transconductance term and solving the small-signal model, the input impedance of the active inductor can be evaluated from Equation 3.9.
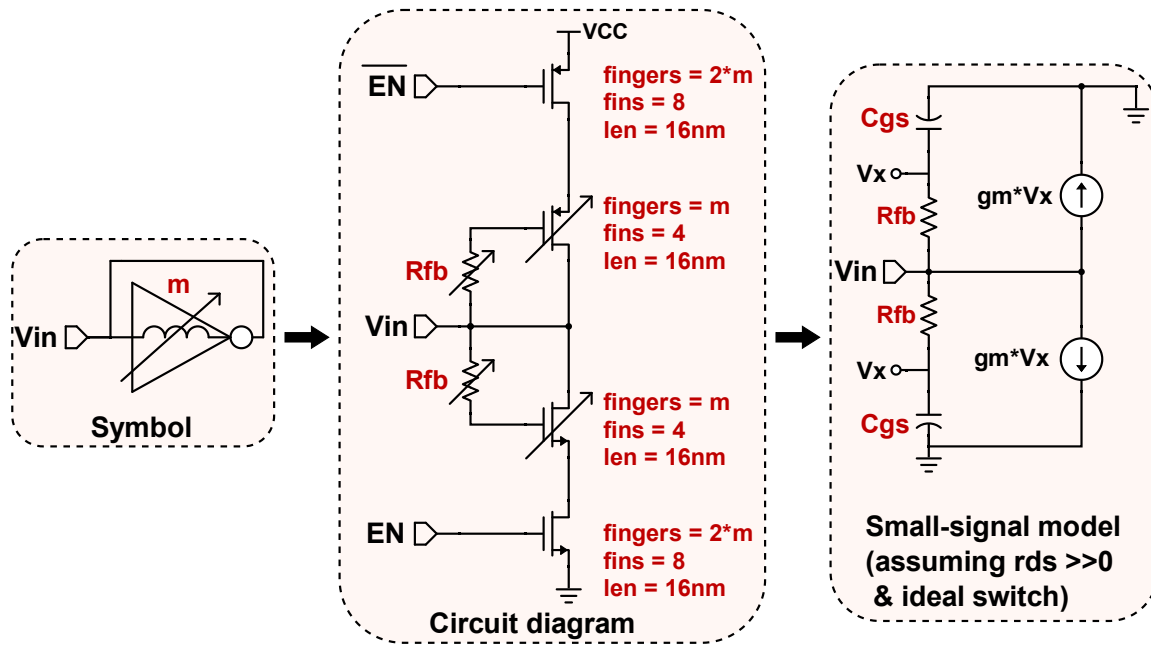
Figure 3.13: Tunable active inductor.

$$Z_{in}(s) = \frac{1}{2} * \frac{1 + sR_{fb}C_{gs}}{g_m + sC_{gs}} \qquad (3.9)$$

The R_{fb} term provides low pass filtering and it creates a zero to give an inductive boost. But, there also exists a parasitic pole which limits the bandwidth usage of this inductor. Moreover, with the inclusion of other transistor parasitics, the bandwidth extension provided by this inductor decreases even further. If we assume that C_{gs} is negligible then the input impedance transforms and can be evaluated using Equation 3.11.

$$Z_{in}(s) \approx \frac{1}{2} * \frac{1 + sR_{fb}C_{gs}}{g_m} \tag{3.10}$$

$$Z_{in}(s) \approx \frac{1}{2g_m} + s\frac{R_{fb}}{2\omega_t} \tag{3.11}$$

Limitation on using large R_{fb} value: Looking at this equation, one can argue that if we keep on increasing the R_{fb} value, one can attain very large inductor value, but there is a limitation on that. It can be explained by a case study of a situation where a CMOS inverter acting as an amplifier drives an active inductor with a capacitive load C_L, as shown in Figure 3.14.
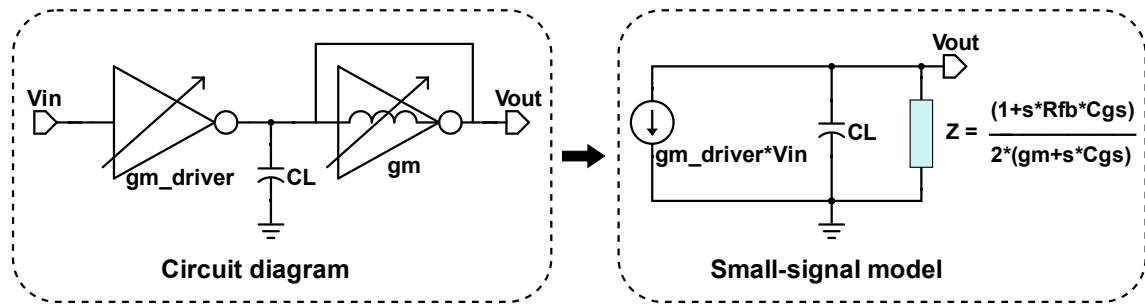
Figure 3.14: Inverter amplifier drives active inductor load alongwith capacitive load C_L.

Solving the small-signal model of the circuit given in the figure, the transfer function of the inverter driving an active inductor can be evaluated using Equation 3.12. This equation has a term dependant on R_{fb} in the denominator too, which indicates that having a large value of R_{fb} can reduce gain at high frequencies. R_{fb} value can have further implications on thermal noise [19]. The value of R_{fb} is a trade-off between noise and bandwidth requirements and thus, it needs to be optimized under stringent requirements [19].

$$H(s) = \frac{g_{m_{driver}}}{2g_m} * \frac{1 + sR_{fb}C_{gs}}{1 + \frac{s(C_L + 2C_{gs})}{2g_m} + \frac{s^2 R_{fb}C_{gs}C_L}{2g_m}} \tag{3.12}$$

In this work, in addition to tunable transistors, R_{fb} is also tunable through series transistor switches, which provides flexibility to tune the inductor value for a given bandwidth requirement. However, the increased circuitry (due to tunability) has an adverse effect on the circuit bandwidth due to the additional parasitics.

3.3.2. High-frequency boost stage (HF-CTLE)

This is the first stage of the CTLE and it is responsible for the major high frequency peaking. The architecture consists of a combination of a high-pass filter and inverter based active circuit for amplification as shown in Figure 3.15. The input signal is amplified in two different frequency ranges. The high-pass filter path is responsible for amplification in high frequency range only, whereas the DC coupled path is responsible for DC as well as high-frequency gain. This is followed by an active inductor which provides bandwidth extension. All the active elements are tunable due to the inverter's tristate nature.
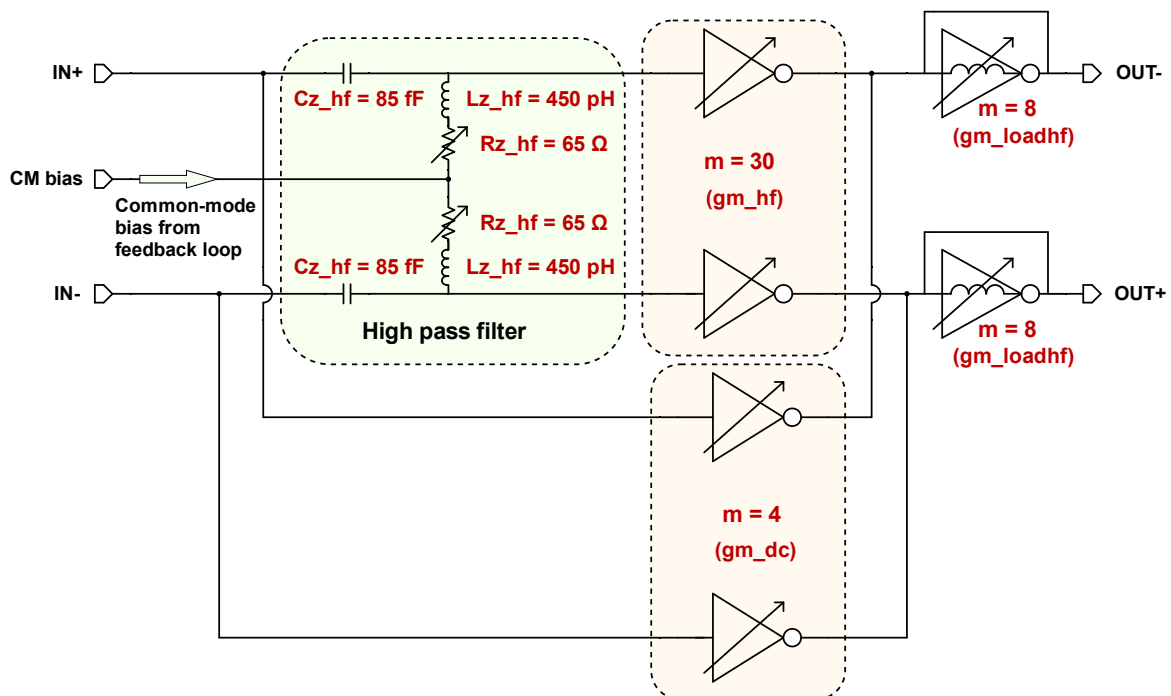
Figure 3.15: High frequency boost stage.

The front high-pass filter uses a mom-cap which is more linear and has less parasitics

as compared to the MOS-capacitor. A tunable resistance is realized by using series transistor switches. The switch sizes are big to ensure small ON resistance which adds parasitics. As a remedy, it is better to have these switches close to the common-mode node, so that there are less parasitics in the main differential signal path.

A series-peaking inductor is also used to reduce the attenuation due to the parasitic capacitors at the output of this filter. The impact of this passive filter is very much visible from the magnitude response of the transfer function of this circuit as shown in Figure 3.16. Larger $L_{z_{hf}}$ values provide better gain at high frequency but also have sharp roll-off in the magnitude response, which can cause under-shoots in the pulse-response and eventually degrades horizontal margins in the eye diagram. So, an optimum inductor value of 450 pH is chosen to meet the design requirement.
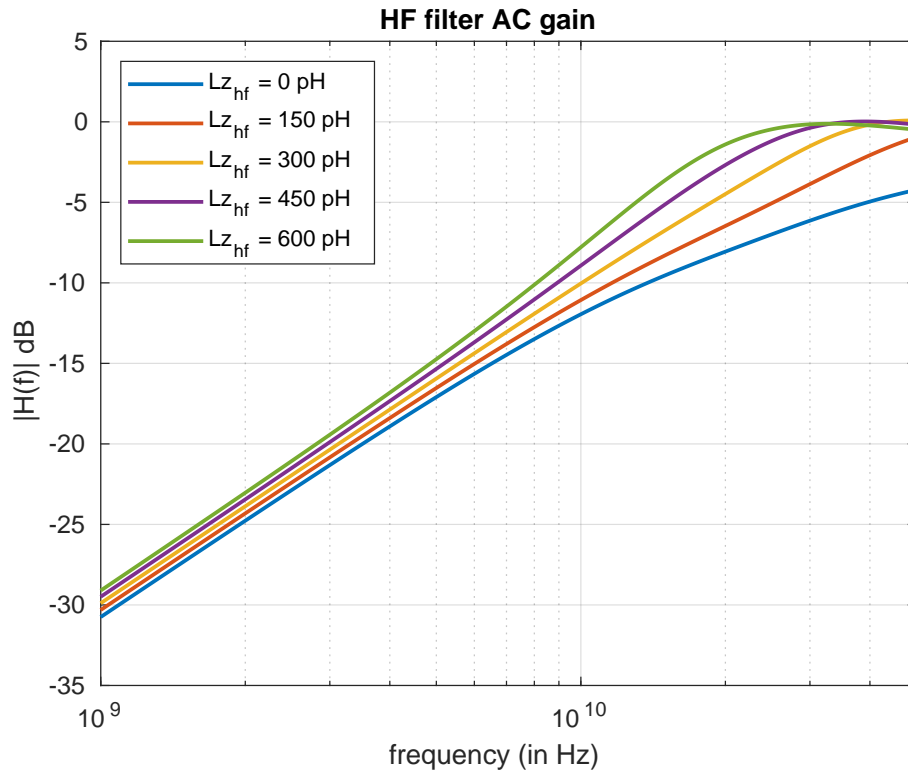
Figure 3.16: Large $L_{z_{hf}}$ value helps to have better filter gain at high frequencies.

Upon ignoring the capacitive load and the inductor effect, the transfer function of this CTLE stage can be given by Equation 3.13. Passive inductor and parasitic capacitors

are not considered while deriving this equation in order to have better visibility of the circuit's poles and zeros. The zero location of this CTLE stage is given by Equation 3.14 and the pole location is given by Equation 3.15.

$$H(s) = \frac{1}{g_{m_{loadhf}}} * \frac{g_{m_{dc}} + s(g_{m_{dc}} + g_{m_{hf}})R_{z_{hf}}C_{z_{hf}}}{1 + sR_{z_{hf}}C_{z_{hf}}} \tag{3.13}$$

$$w_z = \frac{1}{(1 + \frac{g_{m_{hf}}}{g_{m_{dc}}})R_{z_{hf}}C_{z_{hf}}} \tag{3.14}$$

$$w_p = \frac{1}{R_{z_{hf}}C_{z_{hf}}} \tag{3.15}$$

Looking at these equations, the pole and zero locations, as well as the DC gain of the high-frequency CTLE stage very much depend on the transconductance of transistors. So, most of the tunability requirement is achieved by tuning the strength of the transistors. However, it also changes either the DC or the high-frequency gain along with it. On the other side, the tunability in the resistor will just change the pole and the zero location without affecting the gain levels. The input bias of the inverter amplifiers is provided by the common-mode node of the high-pass filter, which is controlled by a feedback loop and will be discussed later in this chapter.

3.3.3. Mid-band gain stage

This is the second stage in the CTLE and is responsible for low to mid-frequency range equalization. Before, diving into its circuit, it is better to explain the need for MF-CTLE (mid-band CTLE) first.

3.3.3.1. Need for MF-CTLE

Traditionally, there used to be only one high-frequency boost stage in the CTLE. But now, as the Nyquist frequency of operation is increasing, the high-frequency CTLE stage only is not sufficient for the low to mid-frequency range equalization [26]. This is largely

due to the channel's magnitude response not being steep in low to mid frequency range (due to skin loss) and the fact that the high-frequency equalizer is designed to have a +20 dB/decade slope. So, there is a need for an equalizer that can match better with the gentle slope of the channel's frequency response in the mid frequency region.

MF-CTLE is also called the long-tail ISI equalizer because it eliminates several post-cursors in the CTLE pulse-response [27] and thus removes the long-tail ISI. It is reported that to accomplish the same task delivered by MF-CTLE for cancelling the post-cursors, a multi-dozen-tap DFE/FFE would be required [27]. The inclusion of this block reduces the complexity for the remaining equalization blocks. In order to have a better understanding regarding the need for MF-CTLE, a MATLAB based model of CTLE (with and without mid-band stage) is created for the same LR channel. The model transfer function is shown in Equation 3.16. The CTLE model parameters are tabulated in Table 3.1.

$$A_v(\text{CTLE model}) = k \cdot \left(\frac{1 + \frac{s}{fz,hf}}{1 + \frac{s}{fp,hf}}\right) \cdot \left(\frac{1 + \frac{s}{fz,mf}}{1 + \frac{s}{fp,mf}}\right) \cdot \frac{1}{(1 + \frac{s}{fp,parasitics})^3} \tag{3.16}$$

Table 3.1: CTLE model parameters in MATLAB.

	f_z (zero)	f_p (pole)	$f_{p,parasitics}$ (pole)	f_z (zero due to inductor)
High-frequency boost stage	3 GHz	28 GHz	42 GHz	28 GHz
Mid-frequency boost stage	150 MHz	200 MHz	42 GHz	–
Buffer stage	–	–	42 GHz	–

- CTLE with mid-band stage has cascade of HF boost stage, MF-boost stage and buffer stage with overall DC gain = -10 dB.

- CTLE without mid-band stage has cascade of HF boost stage and buffer stage with overall DC gain = -10 dB.

It is important to ensure that the goal of the equalization is to have a flat magnitude response till the Nyquist frequency. Figure 3.17 illustrates how a CTLE with mid-band stage does better equalization till the higher frequency than the one without the mid-band stage. Generally, the mid-band stage has a very small amount of boost in the low frequency range, which is achieved by having a circuit with nearby zero and pole locations, as shown in the CTLE model parameters table. It can be inferred that without the mid-band CTLE, the equalized channel magnitude response is not completely flat. This model provides the equalization to a certain extent and it is expected that the remaining equalization is achieved by using RX-FFE and RX-DFE.
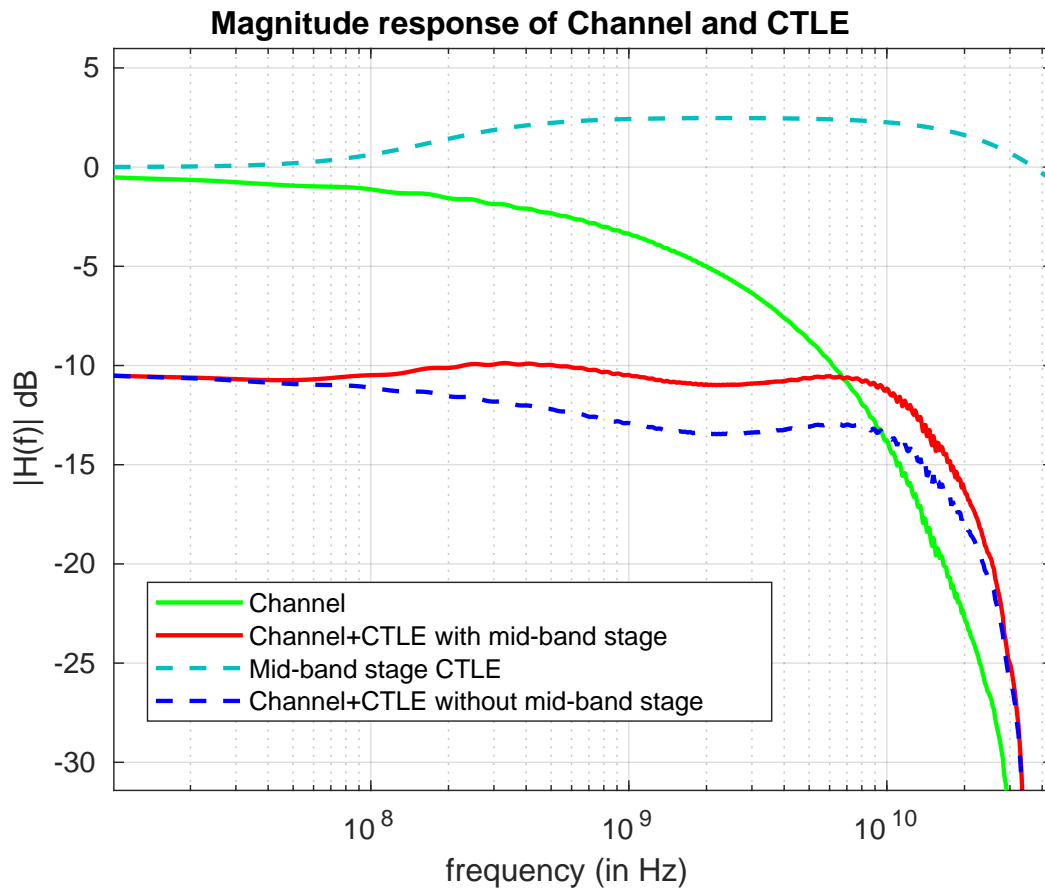
Figure 3.17: Mid-band CTLE improves equalization in terms of magnitude response.

In order to understand long-tail cancellation effect, there is a need to examine the CTLE's pulse response and eventually the eye diagram. The pulse response (for pulse

width corresponding to 56 Gbps NRZ data rate) for the channel and the CTLE (with and without MF-CTLE) is shown in Figure 3.18.
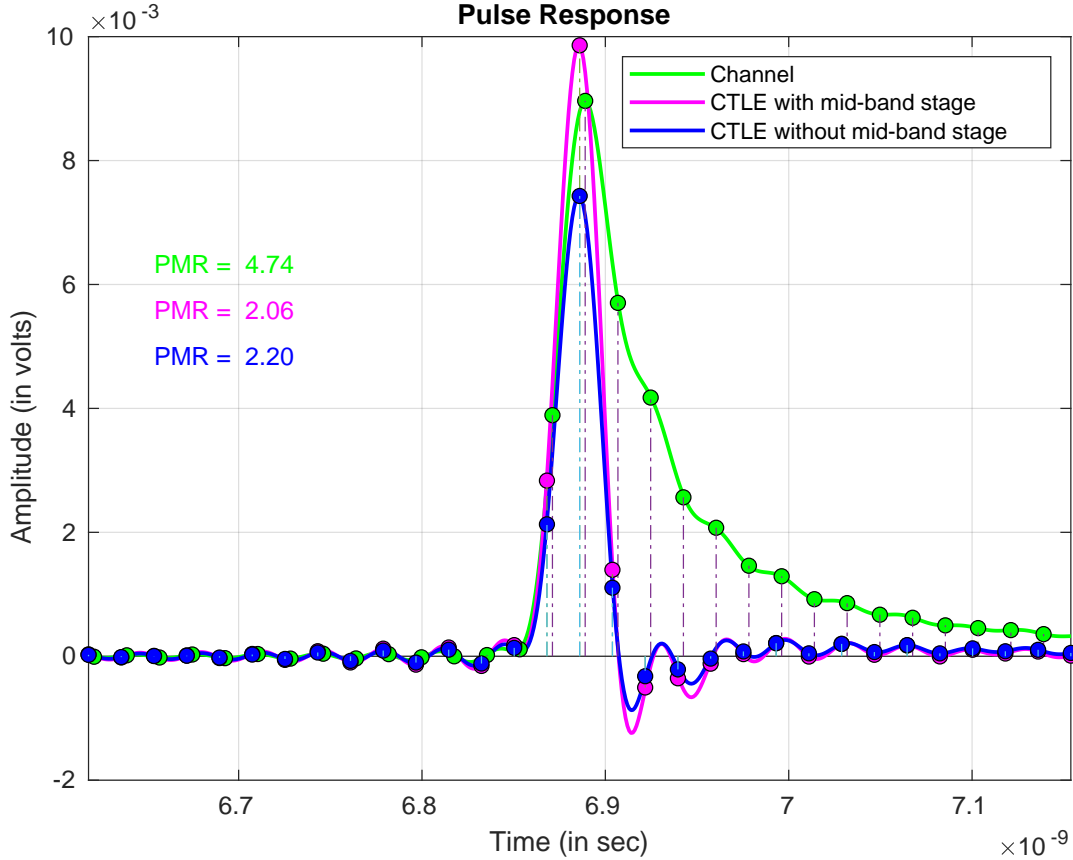
Figure 3.18: Mid-band CTLE has less post-cursor ISI with reference to the main-cursor.

Main cursor corresponds to the main signal while the pre and post cursors are residues in other bits. Cursors except the main cursor are responsible for ISI and are thus undesirable. MF-CTLE especially provides a better attenuation for the case of post-cursors. If the main cursor is treated as the main signal and other cursors as ISI, we can characterize the pulse response in terms of Signal to ISI ratio (signal to noise ratio) given by Equations 3.18 and 3.20.

$$Signal\ to\ ISI\ ratio_{pre-cursors} = \frac{Power\ of\ main\text{-}cursor}{\Sigma Power\ of\ pre\text{-}cursors} \qquad (3.17)$$

$$Signal\ to\ ISI\ ratio_{pre-cursors} = \frac{a_{main}^2}{\Sigma a_{pre-cursors}^2} \tag{3.18}$$

$$Signal\ to\ ISI\ ratio_{post-cursors} = \frac{Power\ of\ main\text{-}cursor}{\Sigma Power\ of\ post\text{-}cursors} \tag{3.19}$$

$$Signal\ to\ ISI\ ratio_{post-cursors} = \frac{a_{main}^2}{\Sigma a_{post-cursors}^2} \tag{3.20}$$

The Signal to post-cursor ISI ratio of the pulse response for ideal n-tap DFE is shown in Figure 3.19. The n-tap DFE (or "n" skipped cursors) means that it eliminates first "n" number of post-cursors. The plot shows that Signal to ISI ratio improves as the number of taps increase or unwanted cursors decrease. The key point of this plot is to show that the CTLE with mid-band stage has significantly high Signal to ISI ratio for post-cursor analysis, however it does not have much impact on the pre-cursors (can be verified but not shown in the plot). This indicates better long-tail cancellation in the case of MF-CTLE. This plot be be used to find number of DFE taps required to meet a target Signal to post-cursor ISI ratio and hence BER. It can be inferred from plot that with MF-CTLE, we need less number of taps to achieve same BER target.

Finally, the eye-diagram has been created for 50k bits at 56 Gbps NRZ data rate as shown in Figures 3.20, 3.21, 3.22 and 3.23. In this simulation, the channel input receives 1 V_{pp} differential signal swing and there is no noise consideration . With MF-CTLE, the eye diagram has better DC voltage level signals as highlighted in green boxes. Also, the horizontal and vertical eye opening is better for the center eye as shown in Figures 3.22 and 3.23.

Signal to ISI ratio analysis for post-cursors in the pulse response
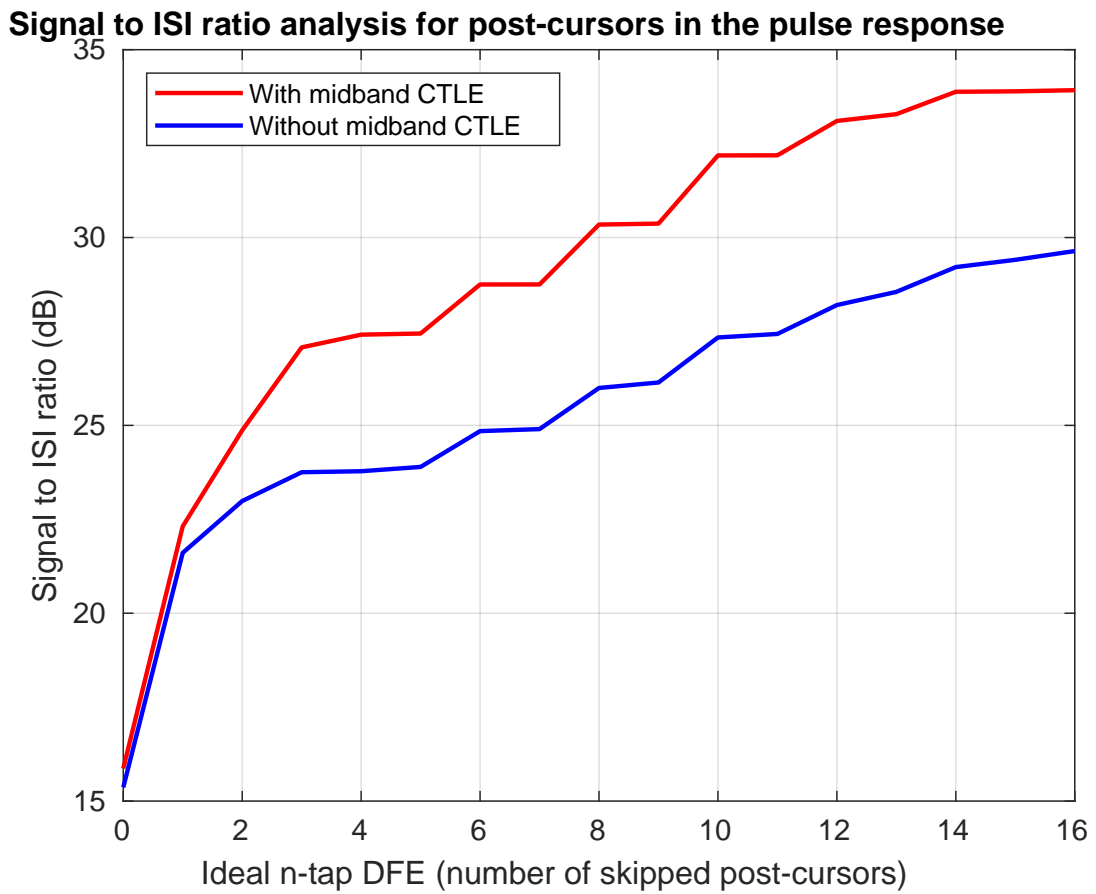
Figure 3.19: Signal to post-cursor ISI ratio for CTLE pulse response.
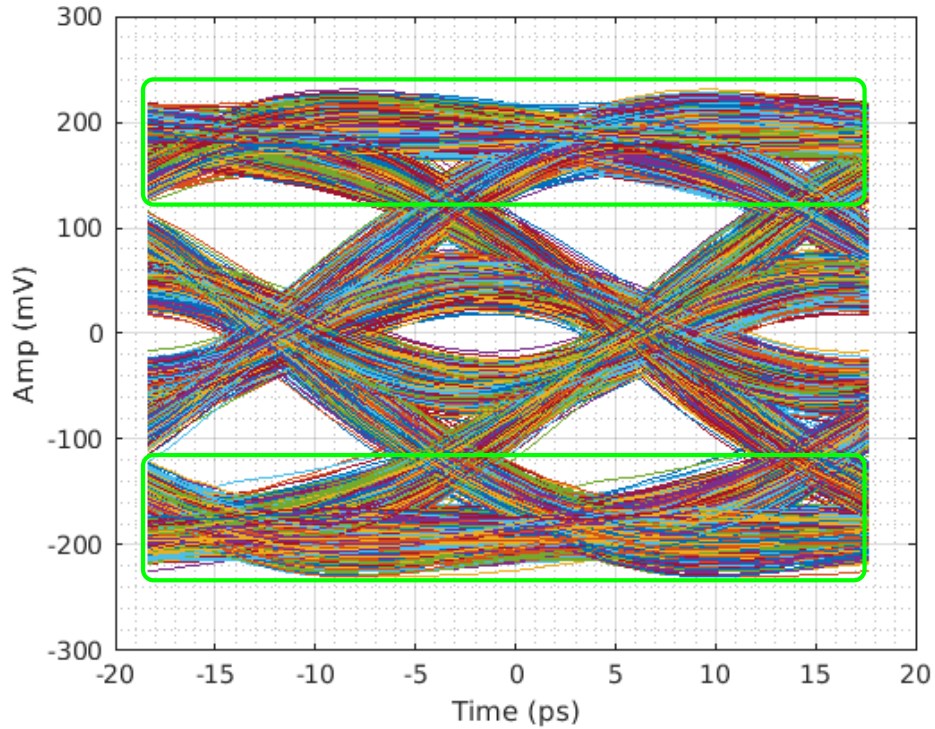
Figure 3.20: Eye diagram at the output of the CTLE without mid-band stage. Green-box highlights more ISI due to the long-tail in the pulse response.
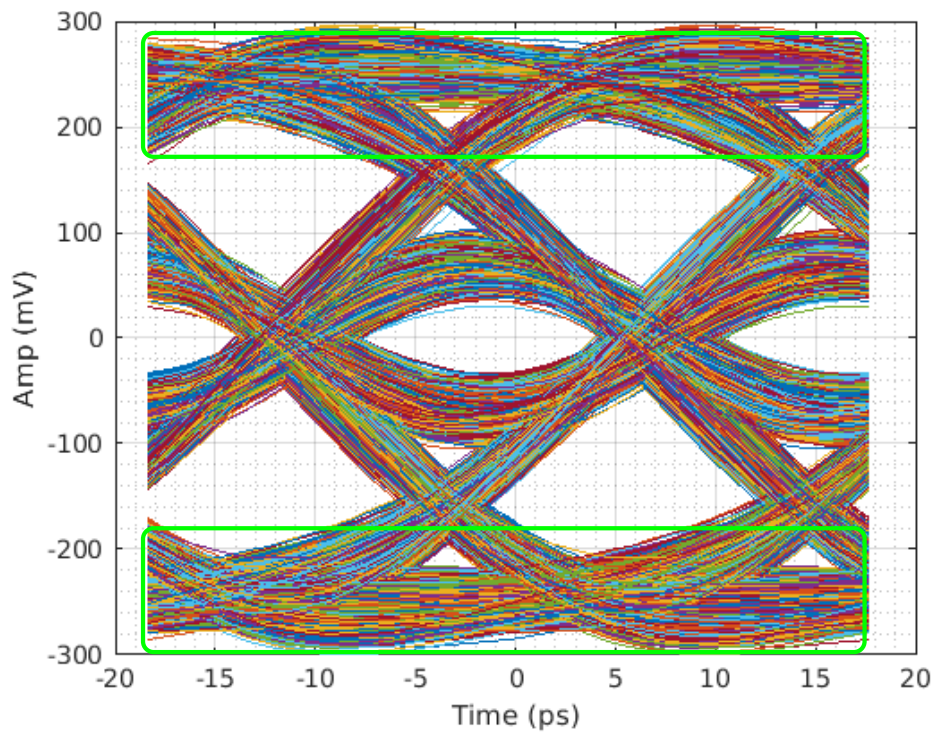
Figure 3.21: Eye diagram at the output of the CTLE with mid-band stage. Green-box highlights lesser ISI due to the long-tail in the pulse response.
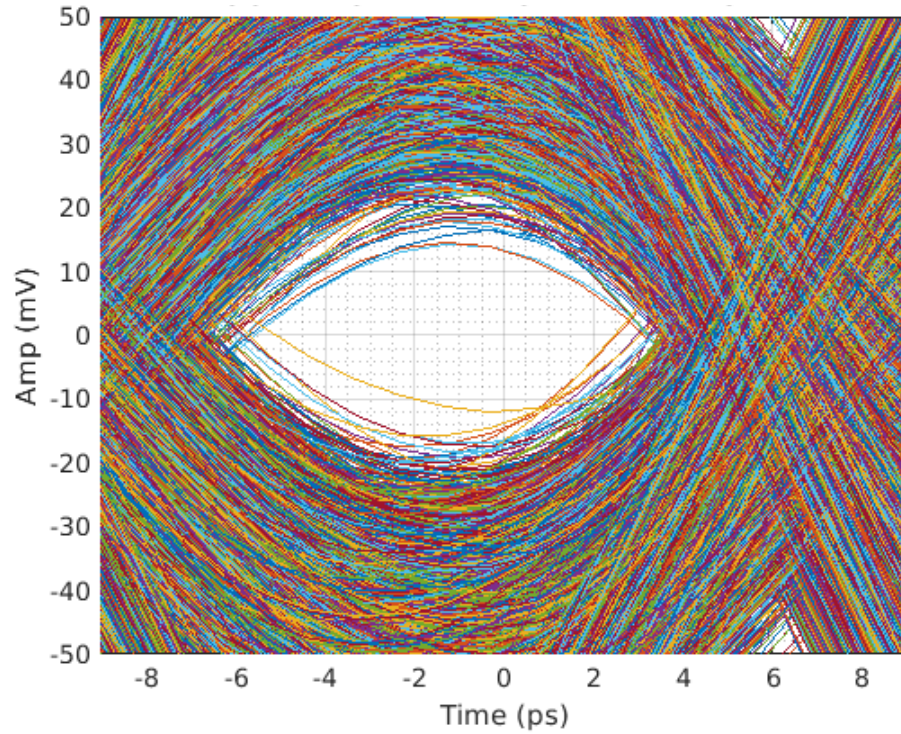
Figure 3.22: Center eye opening at the output of the CTLE without mid-band stage. (Vertical eye opening $= 26\ mV_{pp}$ and horizontal eye opening $= 42\ \%$ UI)
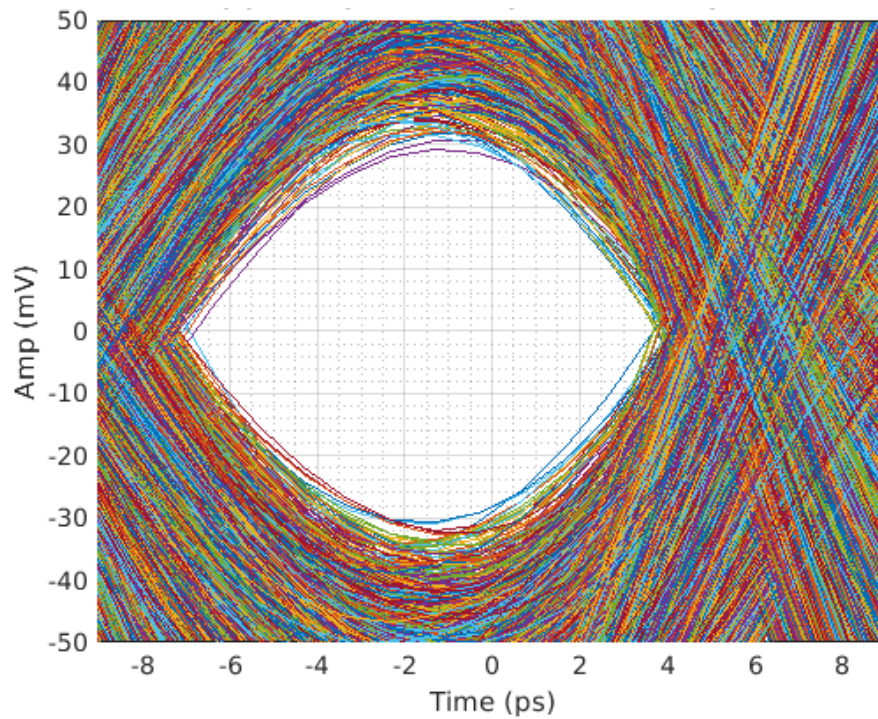
Figure 3.23: Center eye opening at the output of the CTLE with mid-band stage. (Vertical eye opening $= 60\ mV_{pp}$ and horizontal eye opening $= 57\ \%$ UI)

3.3.3.2. MF-CTLE design

The architecture for MF-CTLE is shown in Figure 3.24. It consists of a high pass filter post the inverter amplifiers, unlike the pre-amplifier filter in the case of HF-CTLE. Similar to HF-CTLE, MF-CTLE also does amplification in two different frequency regions - low and mid-to-high frequency regions. The top half as shown in the Figure 3.24 is responsible for wide-band amplification while the bottom half provides gain only in mid-to-high frequency range. The capacitor in the filter is tunable through series transistor switch. The combination of $R_{d_{mf}}$ and C_z mainly decides the zero location for this CTLE. There are active inductors in the wide-band gain path for bandwidth enhancement.
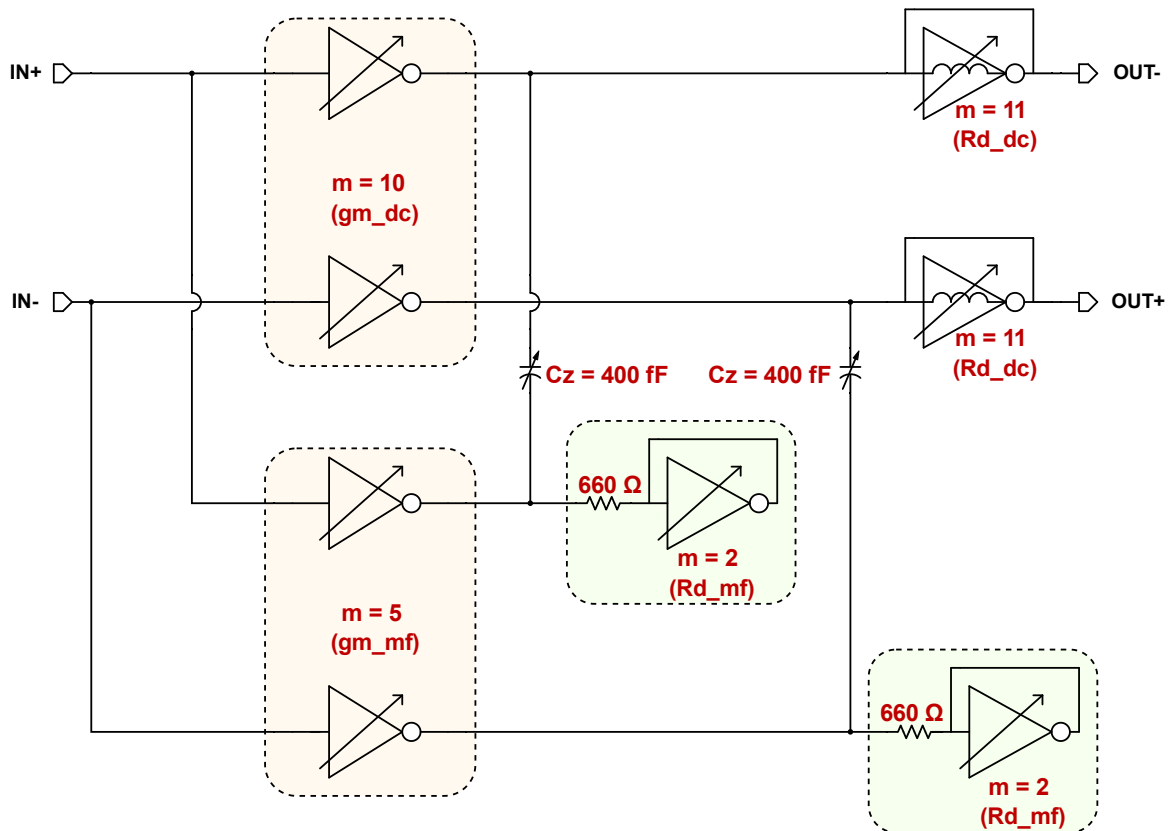
Figure 3.24: Mid-band gain stage.

Upon ignoring the capacitive load and the effect of the active inductor, the transfer function for this gain stage is given in Equation 3.21 and the design parameters are given
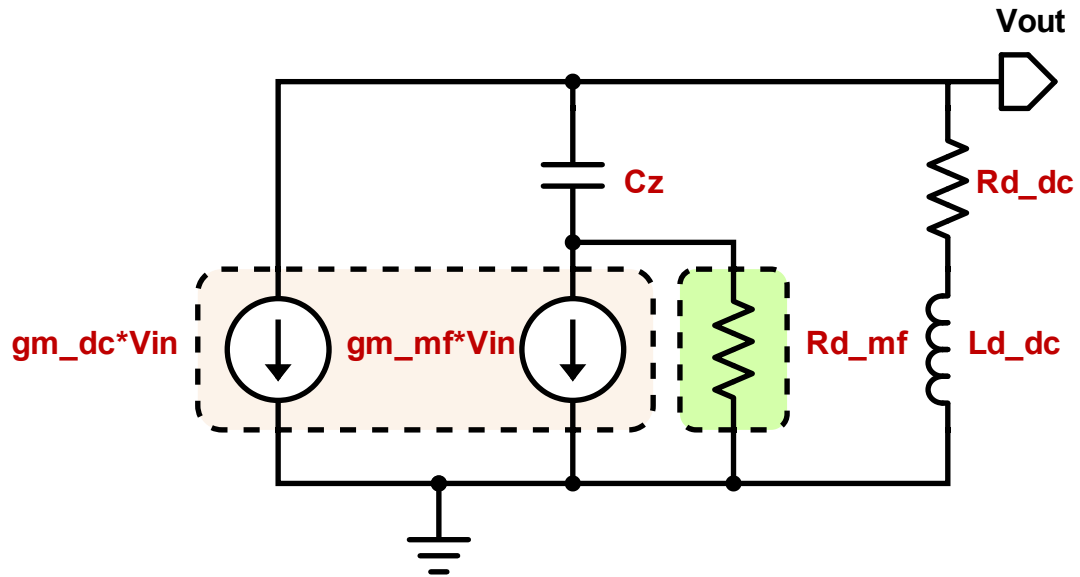
Figure 3.25: Small-signal gain circuit for half-circuit of mid-band gain stage.

in Equations 3.22, 3.23 and 3.24.

$$H(s) = -\frac{g_{m_{dc}}R_{d_{dc}}[1 + sC_zR_{d_{mf}}(1 + \frac{g_{m_{mf}}}{g_{m_{dc}}})]}{1 + sC_z(R_{d_{mf}} + R_{d_{dc}})} \tag{3.21}$$

$$DC\ gain = g_{m_{dc}}R_{d_{dc}} \tag{3.22}$$

$$w_z = \frac{1}{C_zR_{d_{mf}}(1 + \frac{g_{m_{mf}}}{g_{m_{dc}}})} \tag{3.23}$$

$$w_p = \frac{1}{C_z(R_{d_{mf}} + R_{d_{dc}})} \tag{3.24}$$

3.3.4. Buffer stage

This stage is a wide-band amplifier and does not provide any equalization, rather its purpose is to drive the 100 fF capacitive load of the CTLE. This stage reduces the capacitive load for MF-CTLE by providing sufficient isolation from the main load. The architecture of the buffer stage is shown in Figure 3.26.
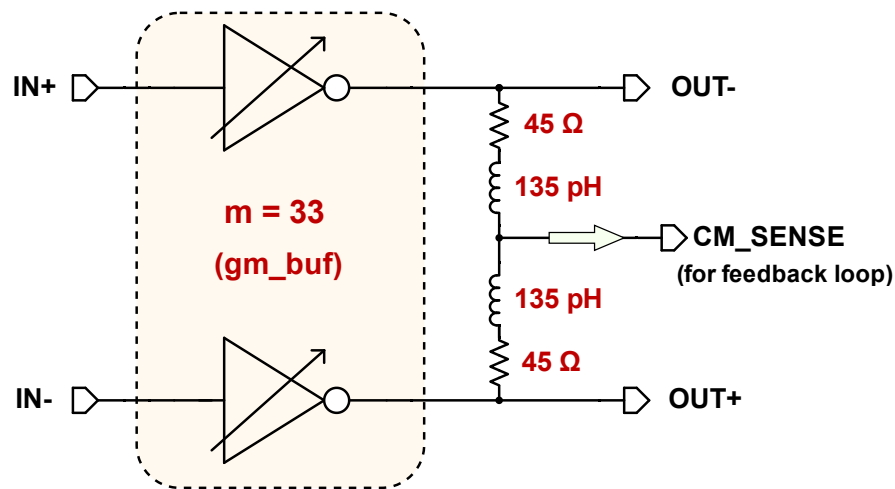
Figure 3.26: Buffer stage.

The drivers are pretty strong in this stage and require a resistive load of $\sim$ 40 Ω. Unlike other stages, this stage does not have any active load as it is unwise to realize an active resistance of 40 Ω (power hungry circuit). The load also consists of a passive inductor for bandwidth enhancement. Ignoring the capacitive load and the effect of the inductor, a simplified form of the transfer function of this stage is given in Equation 3.25.

$$H(s) = g_{m_{buf}} R_L \tag{3.25}$$

3.3.5. CMFB (Common Mode Feedback Loop)

The CMRR analysis for this CTLE is shown in Table 3.2. This information signifies how a low frequency differential and common mode signal will be amplified through each

CTLE stage. In an ideal scenario, it is not desired that the common mode signal is amplified. A low CMRR value implies that a common-mode noise can have significant impact on the differential signals.

Table 3.2: CMRR analysis for each stage in the CTLE.

	Differential DC gain (in dB)	Common-mode DC gain (in dB)	$CMRR = \frac{Differential\ gain}{Common\text{-}mode\ gain}$ (in dB)
HF stage (after high pass filter)	9.3	9.3	0
MF stage	-1.5	-1.5	0
Buffer stage	0.5	23	-22.5
CTLE (post HPF to end)	$\sim$ 8.3	$\sim$ 30.8	$\sim$ -22.5

In addition, if there is a small DC offset at the input common mode node, then that offset will amplify and ruin the biasing for the next stages. So, there is a need to regulate the common-mode voltage. The third stage of the CTLE has degraded CMRR largely as compared to the other stages. The analysis shows that it is because of the fact that its common-mode gain is equal to the intrinsic gain of the transistor. This is caused by the passive load which is not the case with the first two stages. To overcome these issues, a CMFB loop architecture is implemented and shown in Figure 3.27.

This architecture ensures better common-mode bias (nearly half of the supply voltage) and PSRR (power supply rejection ratio) upto $\sim$ 100 MHz supply noise due to finite loop bandwidth. The whole negative feedback loop consists of five negative polarity inverter stages, three out of which are part of the CTLE core and the remaining two inverters are in the feedback path. The open-loop DC gain is $\approx$ 60 dB with a phase margin of $\approx$ 80°, which is sufficient for the stability of the loop. The stability is achieved by using a 4.7 pF compensation capacitor in the feedback path as shown in the Figure 3.27. This loop has gain cross-over frequency of $\approx$ 600 MHz.
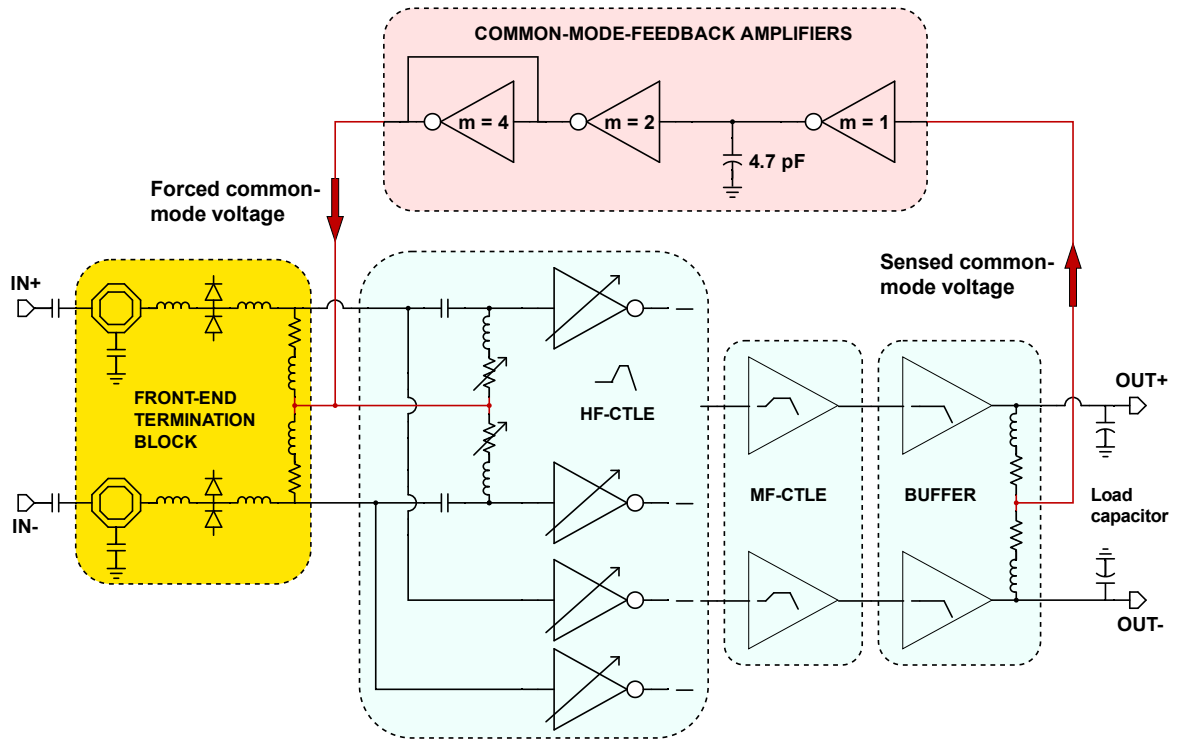
Figure 3.27: CTLE architecture highlighting common-mode feedback loop.

3.3.6. Complete CTLE architecture

The complete CTLE architecture containing the front-end termination block, HF-CTLE, MF-CTLE, buffer stage and feedback loop is shown in Figure 3.28.
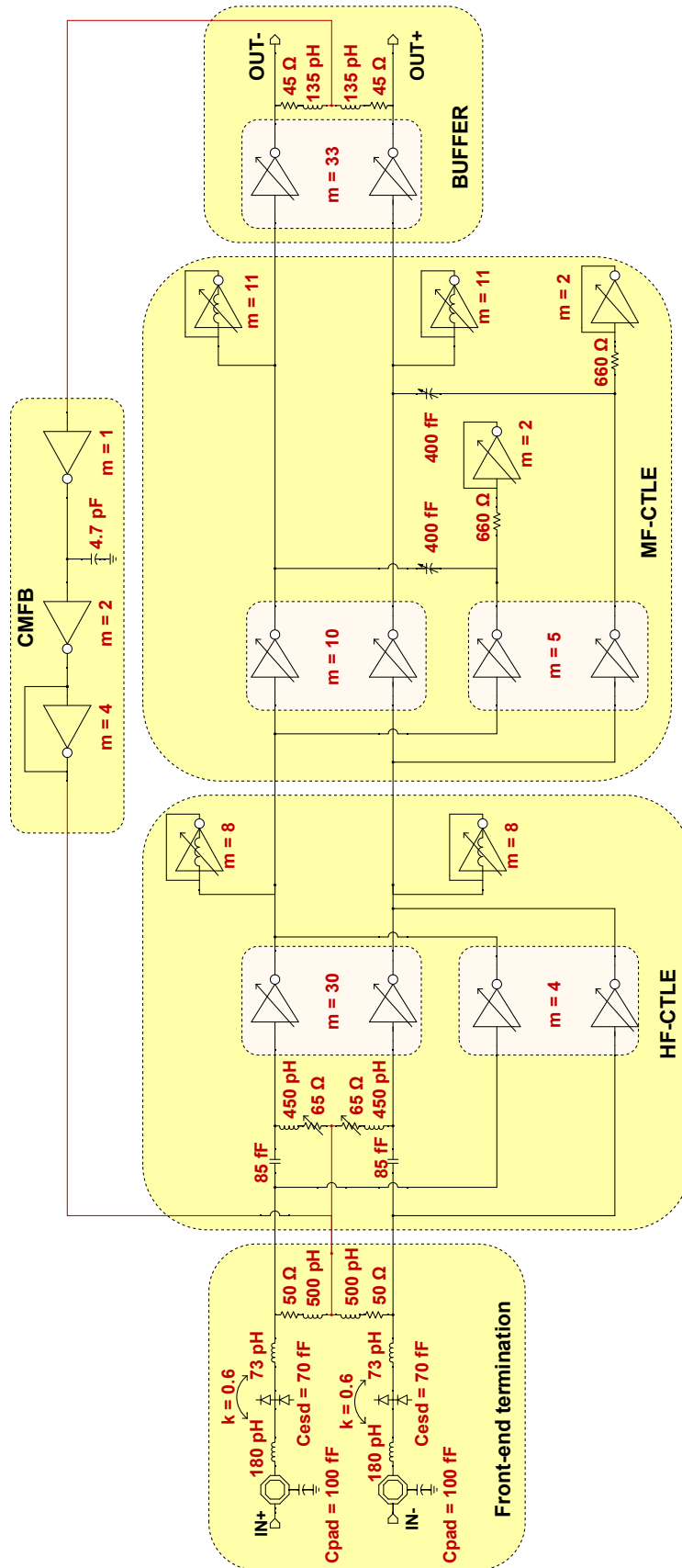
Figure 3.28: Complete CTLE core architecture.

3.3.7.   Output buffer and back-end passive network

For the testability of the CTLE , an output buffer stage is required to carry the CTLE output signals to the outside world (including the external testing equipments such as oscilloscope and network analyser) without any degradation. The output stage has to be co-designed with the oscilloscope's input impedance ($\approx 50\ \Omega$ with parasitic capacitance which limit its bandwidth for characterization). The overall architecture for this stage is shown in Figure 3.29. The buffer uses a high supply voltage of 1.2V to ensure good V_{ds} saturation margin while providing large "g_m" (and hence gain) from single stage amplifier. It consists of a passive level shifter circuit, CML based differential amplifer as buffer, T-coil, ESD cell and bump pads. Generally the output bumps are located far away from the output buffer and require transmission-line modelling for the routing. The CML based architecture is chosen here for better CMRR.
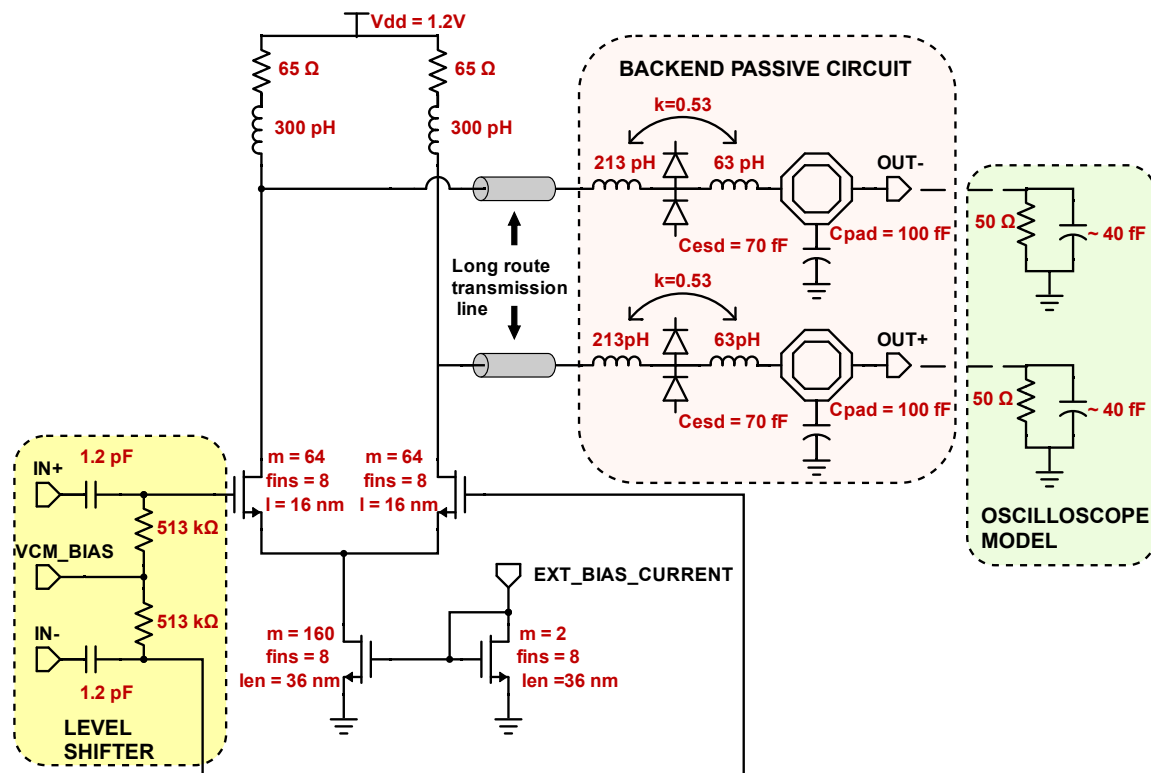

Figure 3.29: CML based output buffer to drive the back-end passive network and the outside world.

Level Shifter: The common-mode voltage of the CTLE output is $\approx 0.4V$, i.e. half of the supply voltage. This input bias voltage is neither suitable for the NMOS nor the PMOS based input transistors for meeting the biasing, lineariy and gain requirements. So, a common mode voltage of 600 mV is provided through this passive high pass filter. The cut-off frequency of the filter is ≈ 250 KHz, which is low enough to pass all the high frequency signals required for the high data rate operation. The least frequency present in the input data stream is defined by 8b/10b or 64b/66b encoding for 56 Gbps symbol rate. However, the parasitics of this capacitor can significantly impact the bandwidth of the prior CTLE. So, it is realized using a mom-cap as it provides less parasitic capacitance with the substrate. The output buffer runs at a 1.2 V power supply which is different from that of the CTLE.

CML buffer: This block is responsible for driving the off-chip load. The CML based design approach has been adopted instead of the inverter based amplifier for buffer action. The CML amplifier has inherently better CMRR which provides good immunity against any common mode noise including the supply/ground noise. This is not the case for the inverter based amplifiers. Also, the power consumption is not a significant parameter for this block, as in real scenario, there is no output buffer, but rather an ADC after the CTLE stage in a typical SERDES system. CML based buffer introduces less non-idealities to the main differential signals.

Regarding the design of this differential amplifier, the tail current-source transistors have larger length to ensure sufficient high value of rds. This helps in better CMRR as well as more accurate mirroring of the current source from the diode-connected load. The load resistance is chosen to be ≈ 65 Ω, so that the effective output impedance of this amplifier matches with ≈ 50 Ω characteristic impedance of the on-chip transmission line to the output pins. Additionally, there is shunt-peaking to extend the bandwidth. The bias current source and the bias voltage of the level-shifter is controlled externally.

Backend passive network: It consists of ESD cells, bump pads and T-coils. This

T-coil is again asymmetric is nature and serves the same purpose like the front-end T-coil. Finally, there is an oscilloscope probe at the output for the off-chip measurements.

3.3.8. Top-level layout

The layout for the top-level design including the CTLE and the output buffer stage with back-end termination is shown in Figure 3.30. The CTLE design (including the front-end termination block) takes an area of $\approx 140\ \mu$m x $140\ \mu$m. The output buffer stage along with the back-end termination takes an area of $\approx 90\ \mu$m x $140\ \mu$m. The majority of the area is consumed by the T-coils, passive inductors, ESD cells and the compensation capacitor in the feedback loop. The implementation of the active inductors in MF-CTLE and HF-CTLE allows for miniaturization in area. There are certain things including metal-filling, instantiating power clamps, ESD cells, and certain low speed tunability circuit, which remain pending due to time-constraints.
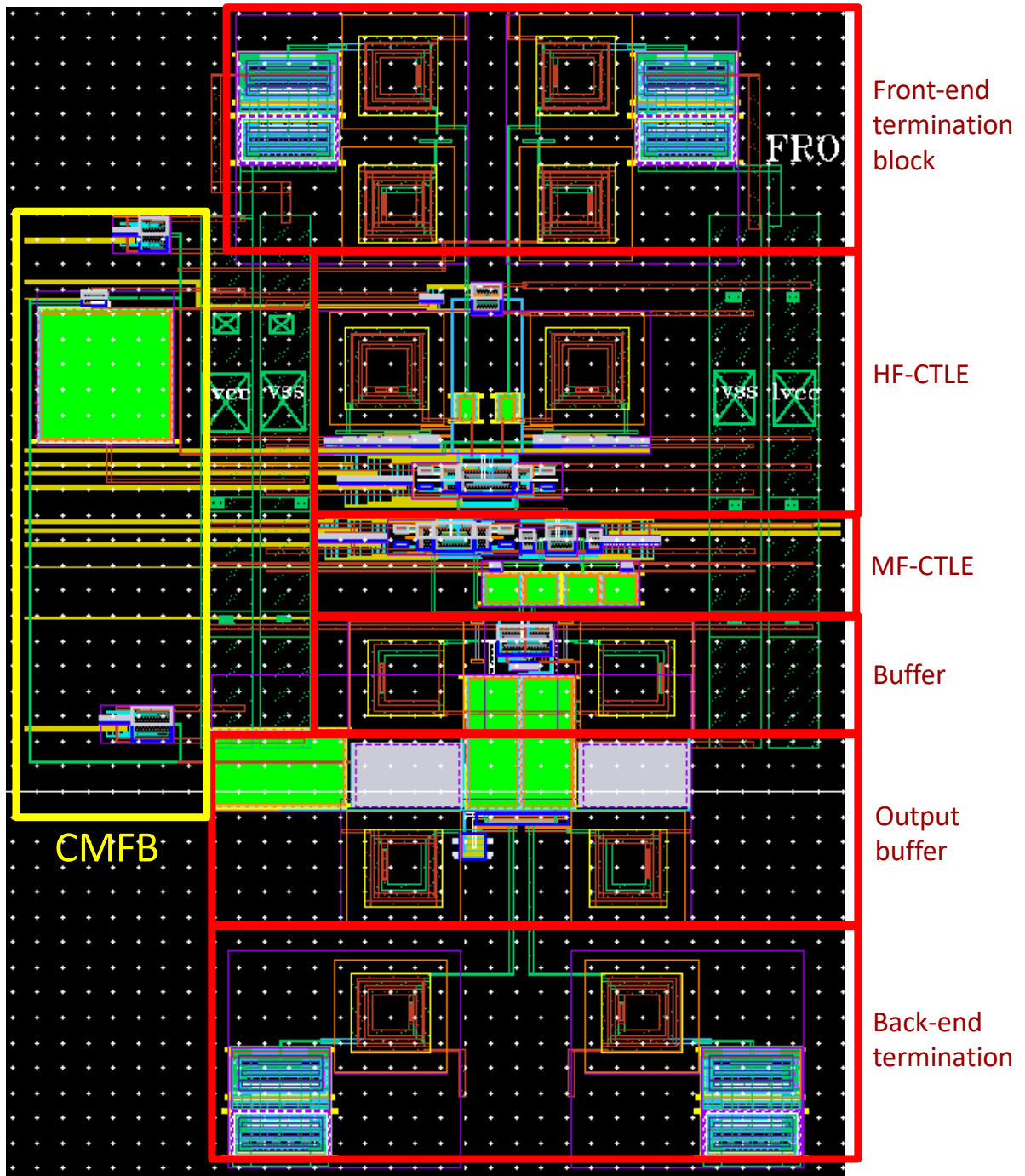
Figure 3.30: Top-level layout.

4 | Extracted Simulation Results

This chapter presents the extracted layout results of the analog front end of the receiver consisting of the front-end termination block, HF-CTLE, MF-CTLE, buffer stage and the output buffer stage. The CTLE system was designed in 16nm FinFET technology and tested for certain PVT conditions. Most of the results shown here are based on the typical process corner at 80ºC temperature and 0.8V power supply voltage for the CTLE core, unless explicitly specified.

4.1. Magnitude response

Figure 4.1 shows the magnitude response of the unequalized channel, different stages of the CTLE and the overall equalized channel. The CTLE has $\sim$ -9 dB DC gain and a peak gain of $\sim$ 8 dB at the Nyquist frequency. The dashed plots show the breakdown of inner stages of the CTLE. The CTLE achieves peak gain at $\sim$ 25 GHz.

Figure 4.2 shows the magnitude response of CTLE for linear frequency scale. It provides better insight about the system in high frequency region of interest.
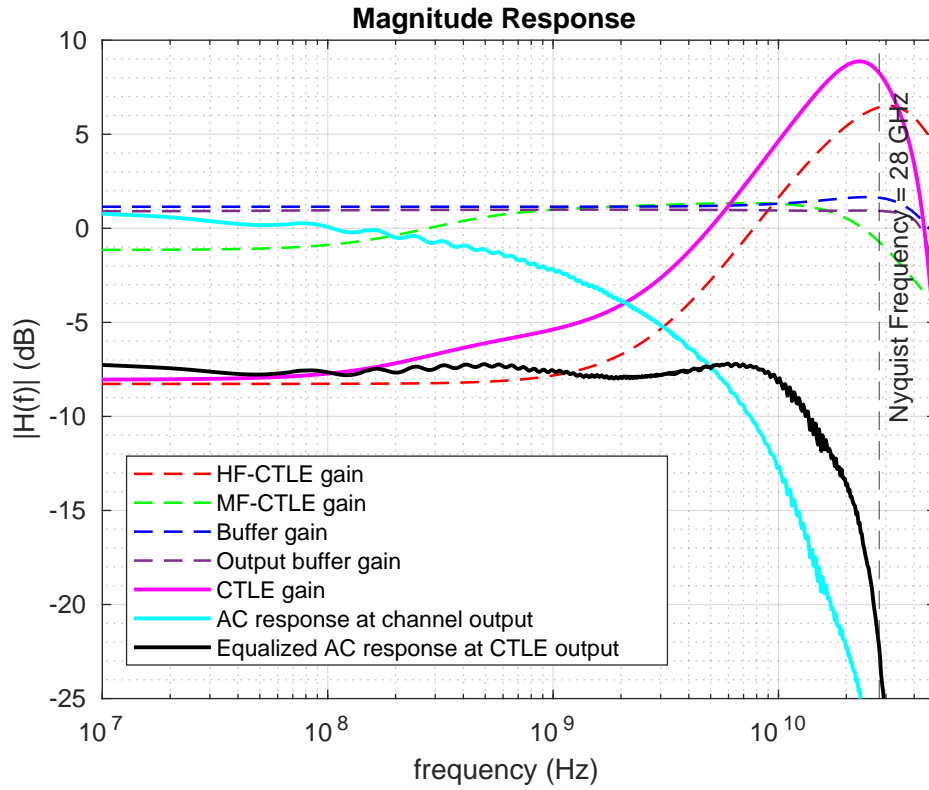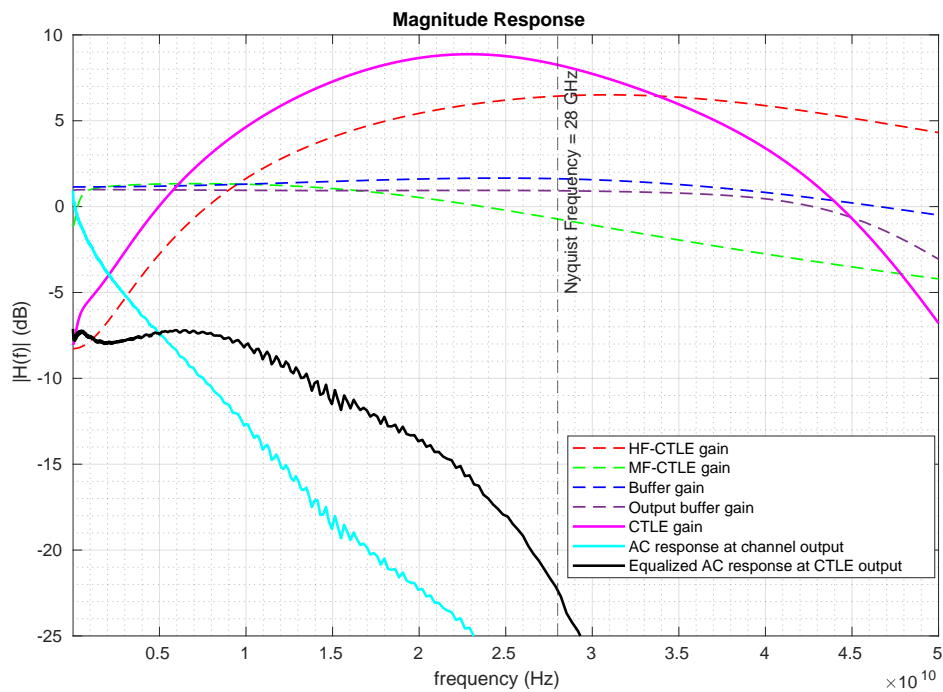
Figure 4.1: CTLE magnitude response.

Figure 4.2: CTLE magnitude response for linear frequency scale.
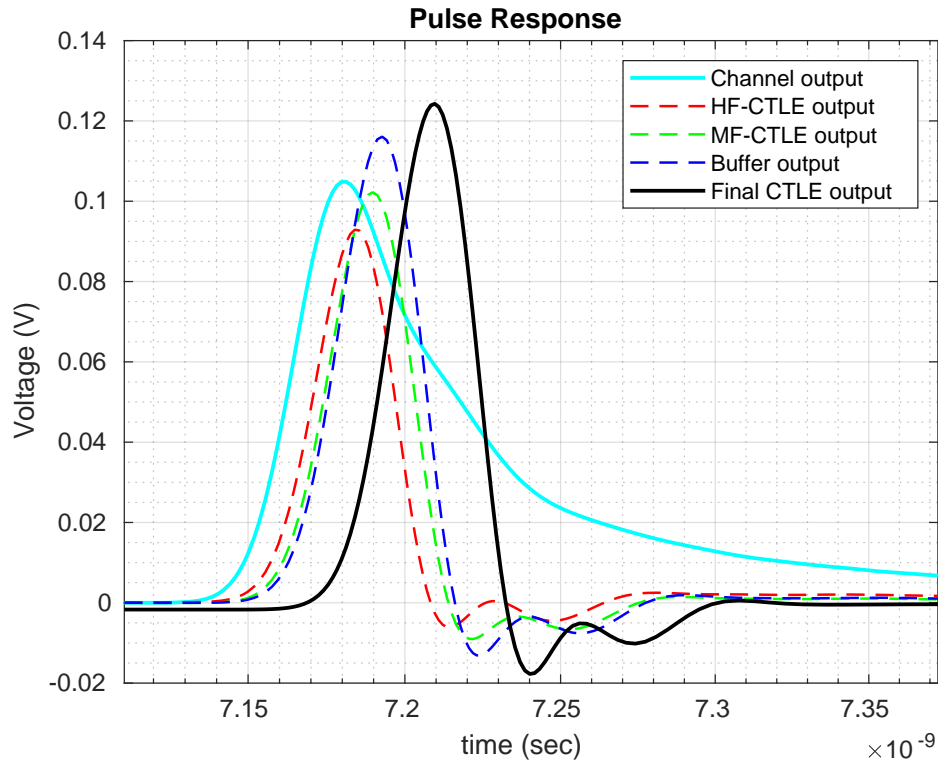
4.2. Pulse response

Figure 4.3: CTLE Pulse response.

Figure 4.3 shows the pulse response of the unequalized channel, different stages of the CTLE and the overall equalized channel. The equalized channel response has significantly less post cursor ISI, although due to steep roll off in magnitude response, some undesirable undershoots ($\sim 12\,\%$) degrade the horizontal eye opening margins.

To overcome the undershoot issue, I have added the tunability options in active inductors in the circuit, however it will adversely impact the high frequency gain. It can be noticed that MF-CTLE has reduced post cursors relative to main the cursor as compared to HF-CTLE. This helps in the long-tail ISI cancellation and its impact on the eye-diagram is presented in the Appendix.

4.3.   Thermal noise

Figure 4.4 shows the output and input referred noise voltage spectral density for the analog front end (including front termination, HF-CTLE, MF-CTLE and the buffer stage). The integrated output thermal noise is 2 mV_{rms}. Integrating the input referred noise voltage spectrum till $\sim$ 50 GHz (system's bandwidth) provides integrated input referred noise voltage of 1.4 mV_{rms}. The thermal noise impacts the SNR and hence impacts BER. Simulation results yield that the major noise contributors are transistors in HF-CTLE.

Figure 4.5 shows that major noise contribution comes from thermal noise in high frequency region as area under the curve will be larger in that region.
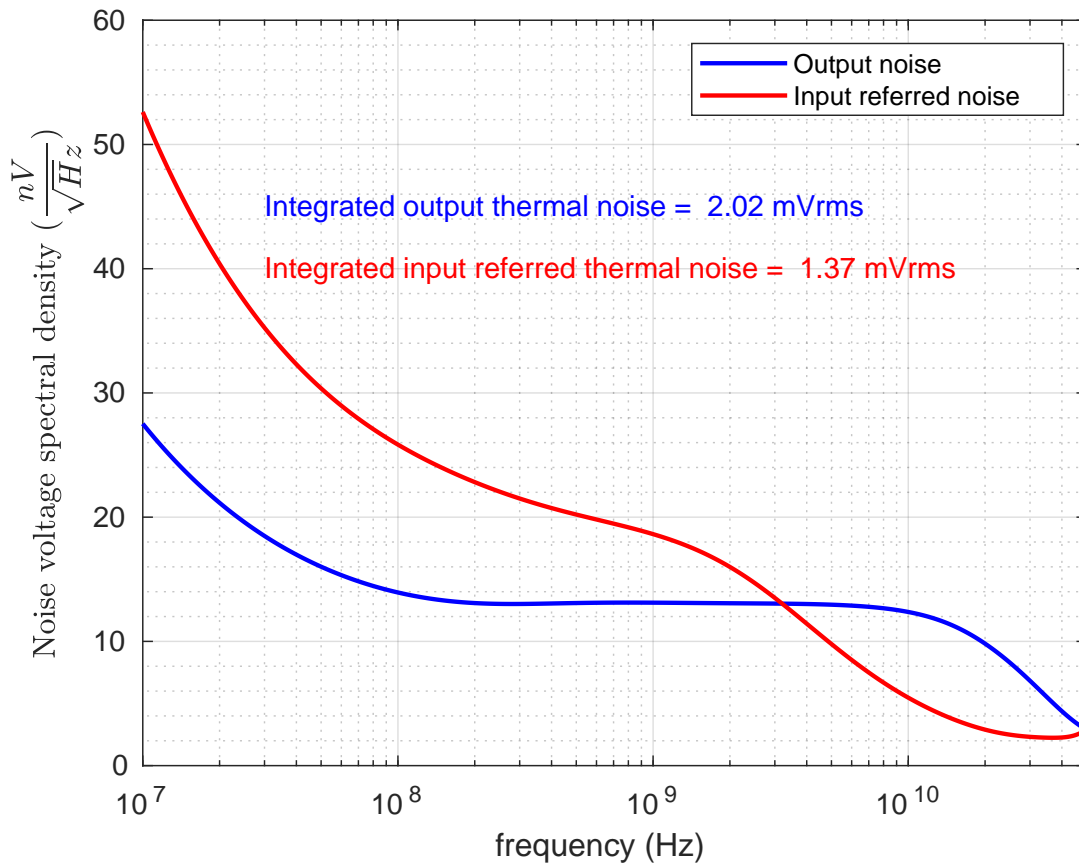

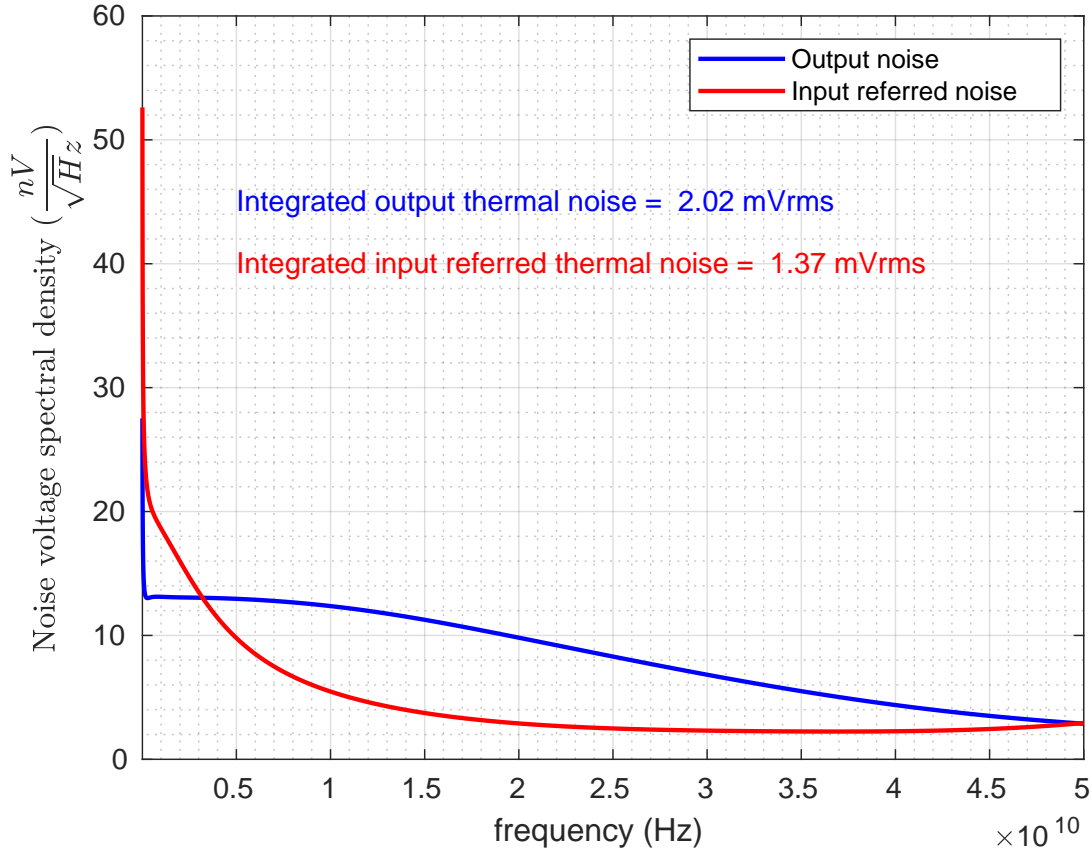**Figure 4.4:** Thermal noise spectral density for CTLE.

Figure 4.5: Thermal noise spectral density for CTLE for linear frequency scale.

4.4. Eye diagram for NRZ (PAM-2) data signaling

The eye-opening in PAM -2 signal is higher in comparison to PAM-4 signal due to more margin in symbol voltage levels. In PAM 4 signaling, the the adjacent symbols have 1/3 times the margins in comparison to PAM-2 signaling. So, the eye-diagrams for both PAM-2 and PAM-4 data modulations are presented in this work to have deeper insight. The eye diagrams are generated for 10k PRBS data symbols pattern from TX end with an output signal swing of 1 V_{pp} differential. The eye at the channel output is fully closed even at a lower data rate (40 Gbps NRZ) as shown in Figure 4.6

The eye-diagram at the final CTLE output for 56, 50 and 40 Gbps NRZ data signaling is shown in Figures 4.7, 4.8 and 4.9 respectively. The eye has a small vertical opening of $\approx$ 15 mV_{pp} with a horizontal opening of 33 % UI for 56 Gbps data rate but it gets improved
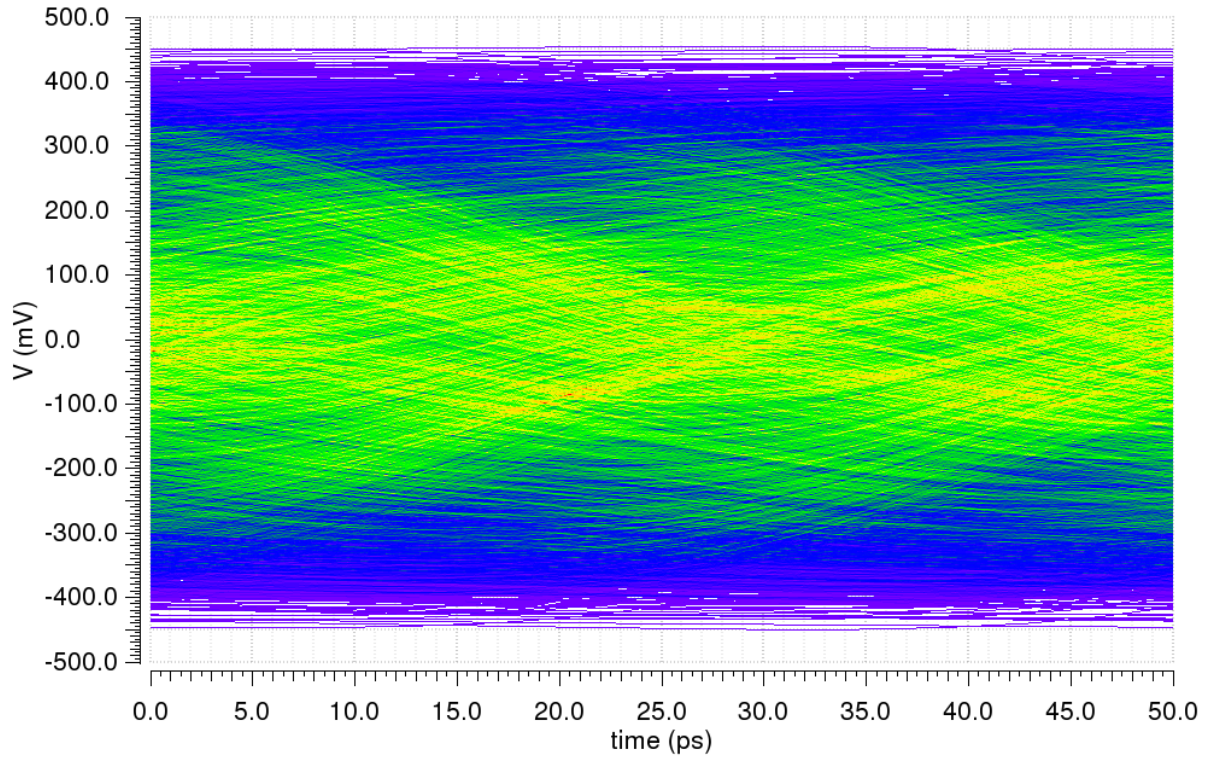
Figure 4.6: Eye diagram at the channel output for 40 Gbps NRZ data rate (Pulse PMR = 3.6).

for 50 Gbps data rate (with a vertical eye opening of $\approx 75 \ mV_{pp}$ and a horizontal eye opening of $\approx 58 \ \%$ UI) because this CTLE provides maximum high frequency gain till 25 GHz as shown in Figure 4.1. The eye is wide open for lower data rates because of the lower attenuation offered by the channel at lower frequencies.
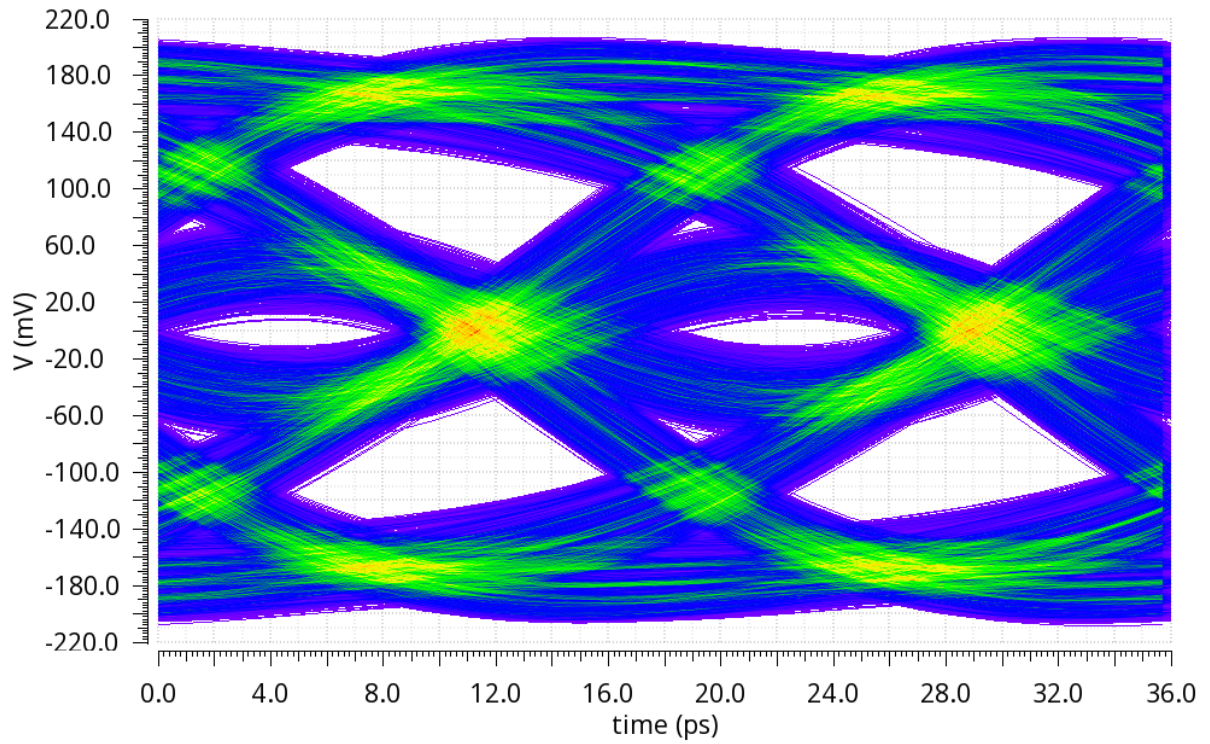
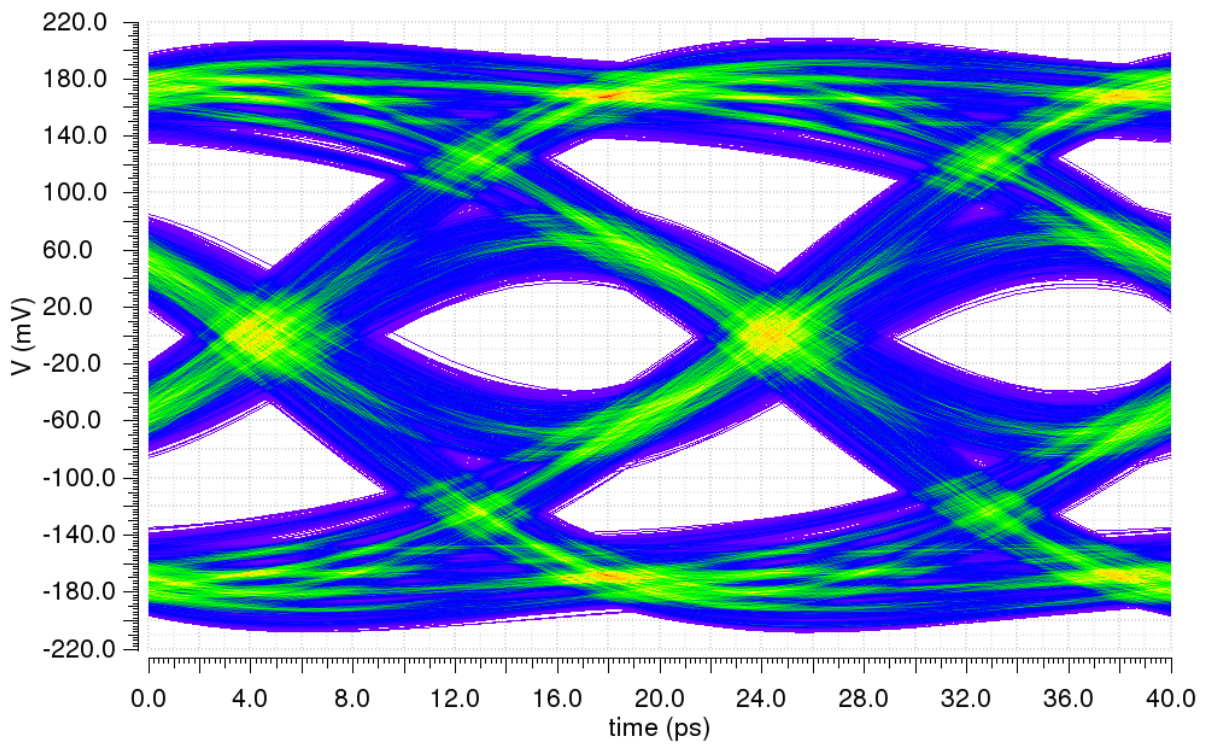**Figure 4.7:** Eye diagram at the CTLE output for 56 Gbps NRZ data rate (Pulse PMR = 3.14).

Figure 4.8: Eye diagram at the CTLE output for 50 Gbps NRZ data rate (Pulse PMR=2.85).
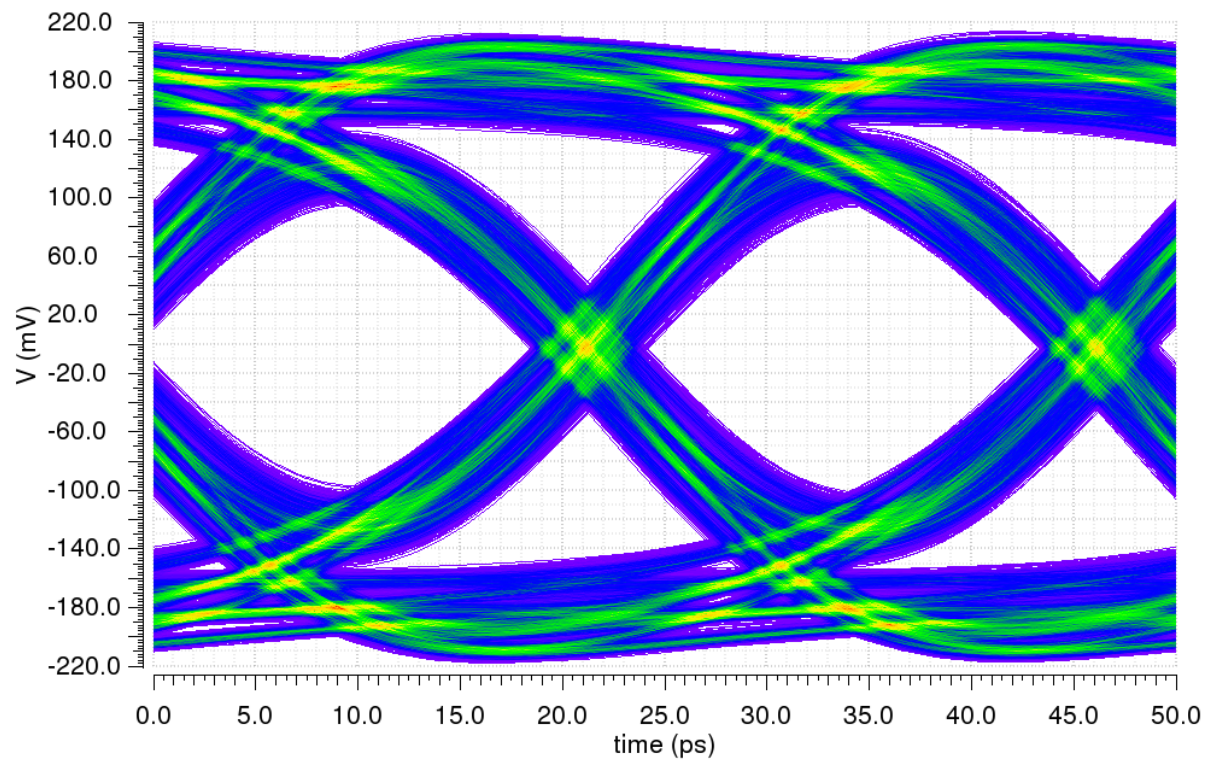
Figure 4.9: Eye diagram at the CTLE output for 40 Gbps NRZ data rate (Pulse PMR=2.4).

4.5.   Eye diagram for PAM-4 data signaling

This section shows eye diagrams at the CTLE output for 20k PRBS PAM-4 data symbols with an output signal swing of 1 V_{pp} differential. The eye for 112 Gbps PAM-4 data rate is completely closed as shown in Figure 4.10. However, there is certain eye opening for lower data rates (64 and 40 Gbps PAM-4) as shown in Figures 4.11 and 4.12. The eye-diagram for 40 Gbps data rate shows asymmetric eye opening for middle and edge eyes because the equalizer needs to be optimized for this data rate.
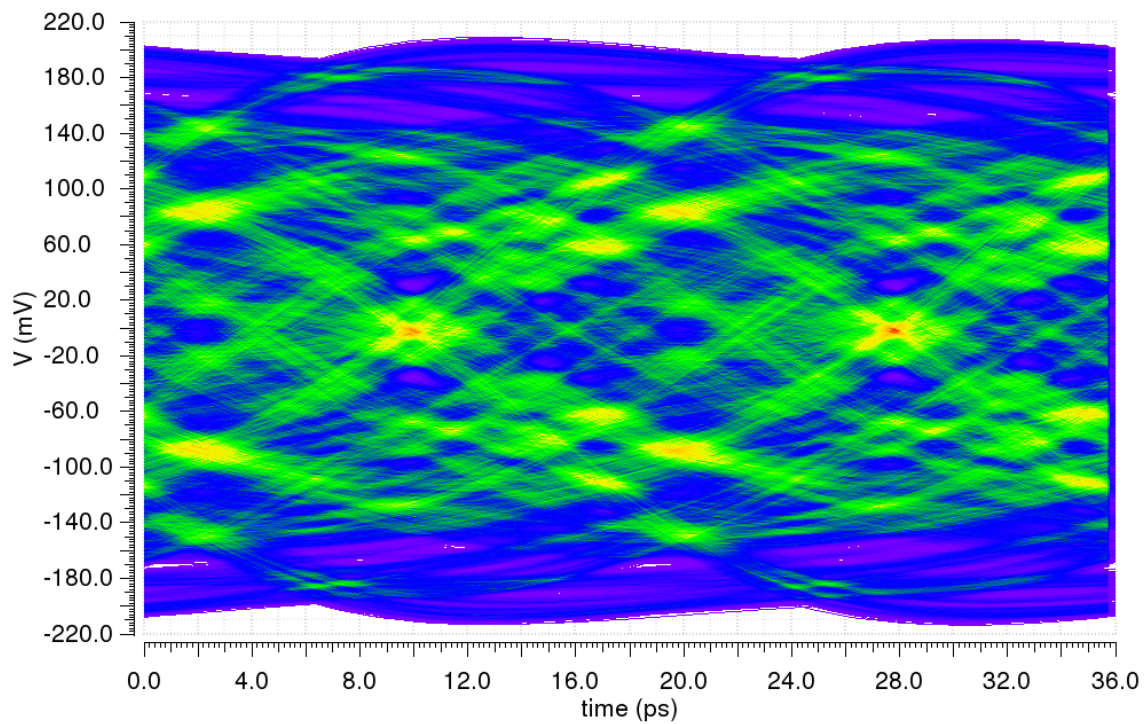

Figure 4.10:   Eye diagram at the CTLE output for 112 Gbps PAM-4 data rate (Pulse PMR=3.14).
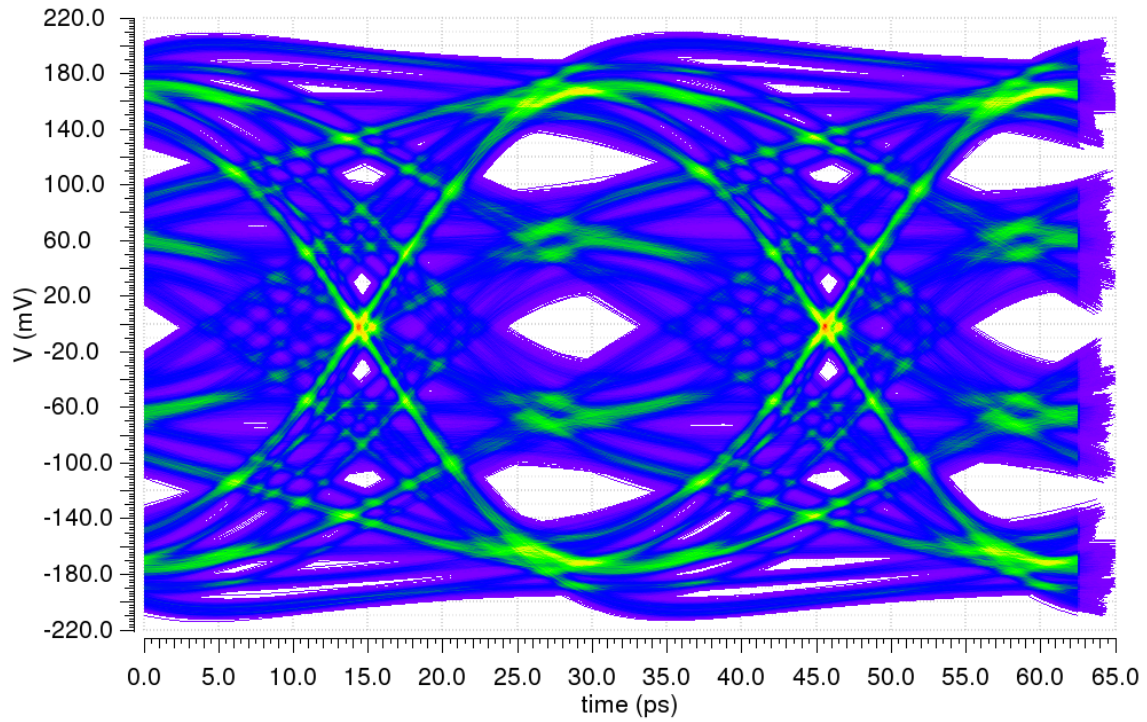
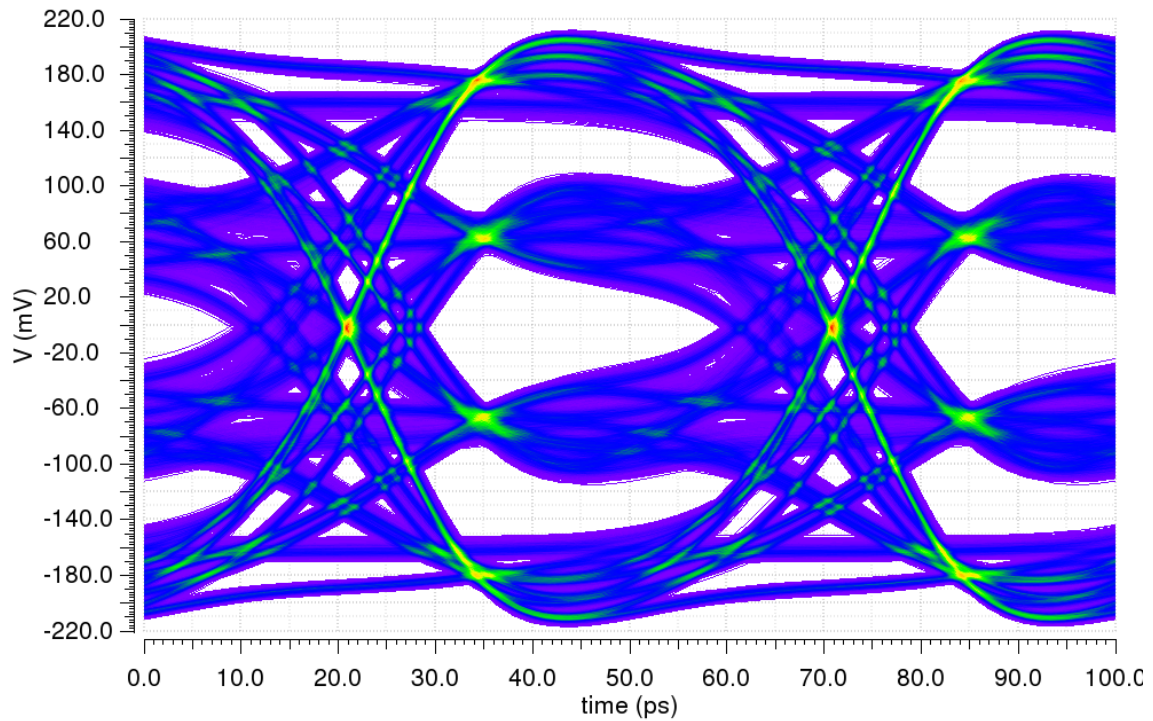**Figure 4.11:** Eye diagram at the CTLE output for 64 Gbps PAM-4 data rate (Pulse PMR=2.18).

Figure 4.12: Eye diagram at the CTLE output for 40 Gbps PAM-4 data rate for default settings (Pulse PMR=2.05). Equalizer needs to be optimized for this data rate.

4.6.   Tunability to track PVT variations

The programmability been provided in all stages of the CTLE to track the PVT varaitaions and to provide a single solution for different channel profiles. Figure 4.13 shows the frequency magnitude response of the CTLE for different extreme tunability options. It may be difficult to comprehend information about the role of each tunability knob by looking at this plot. Impact of each tunability option is demonstrated in the Appendix.
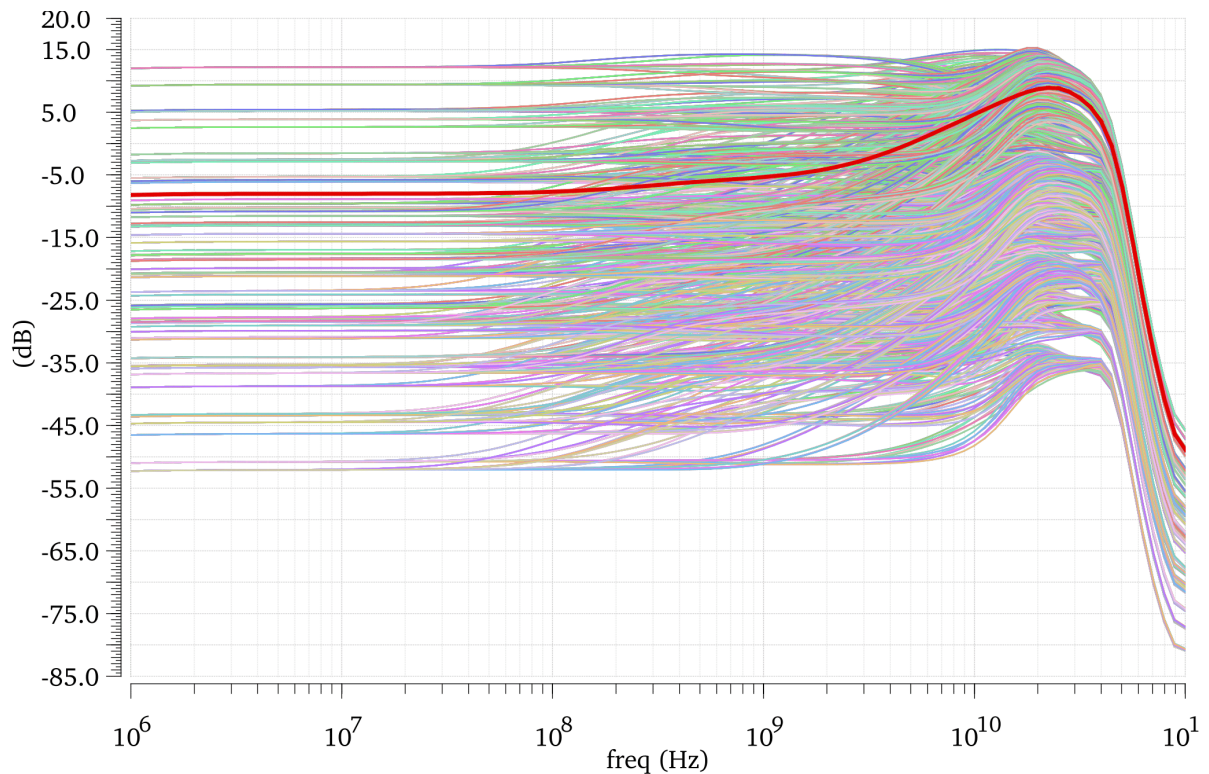

Figure 4.13: Magnitude response coverage due to overall sweep of all tunability knobs (highlighted red one is the default setting)

The system has been tested across extreme PVT conditions as mentioned in table 4.1. Figures 4.14- 4.18 demonstrate the PVT tracking ability of the CTLE for chosen PVT conditions. The default tunability setting (setting for nominal process) does not provide optimum performance across different PVT conditions. Tunability options provided in design are able to match the nominal corner performance across different PVT conditions upto ∼ 10-15 GHz frequency. Beyond this frequency, the circuit bandwidth is limited

by the process and may require more transistor fingers in the case of SS process. This provision can lead to lot of parasitic capacitance and hence not attempted.

**Table 4.1:** PVT corners list with details.

	Process	Supply voltage (Volts)	Temperature (^{o}C)
Nominal corner	typical	0.8	80
Strong corner	FF (fast-fast)	0.84	0
Weak corner	SS (slow-slow)	0.76	125
SF corner	SF (slow-fast)	0.8	80
FS corner	FS (fast-slow)	0.8	80

Figure 4.14 shows the CTLE magnitude response for the PVT optimized and un-optimized case. In un-optimized case, the default tunability setting (setting for the nominal process) is used for the other PVT corners. However, for optmally tuned configuration for each PVT corner, the magnitude response matches the desired response (nominal process response) till ~ 10 GHz frequency. Beyond this frequency, the circuit bandwidth is limited by the process.

In SF and FS corners, the model file includes slow-fast variations for transistors whereas the passive components behaviour is same as the typical process. As shown in Figures 4.14, 4.15, 4.18 and 4.8, the SF and FS corners show similar results as the nominal corner. This signifies that the biasing of the circuit is proper even for skewed strength of the NMOS and PMOS.

Figure 4.15 shows the CTLE pulse response for the PVT optimized and un-optimized case. The long-tail ISI is reduced due to optimal tunability setting in the Weak corner. In strong corner, the amount of ringing is reduced due to PVT optimization.

Figures 4.16 and 4.17 show improvement in the eye opening due to optimized circuit settings for strong and weak corners respectively. Figures 4.18 shows the eye-diagrams for SF and FS corners which are similar to the one in the nominal corner as shown in Figure 4.8.
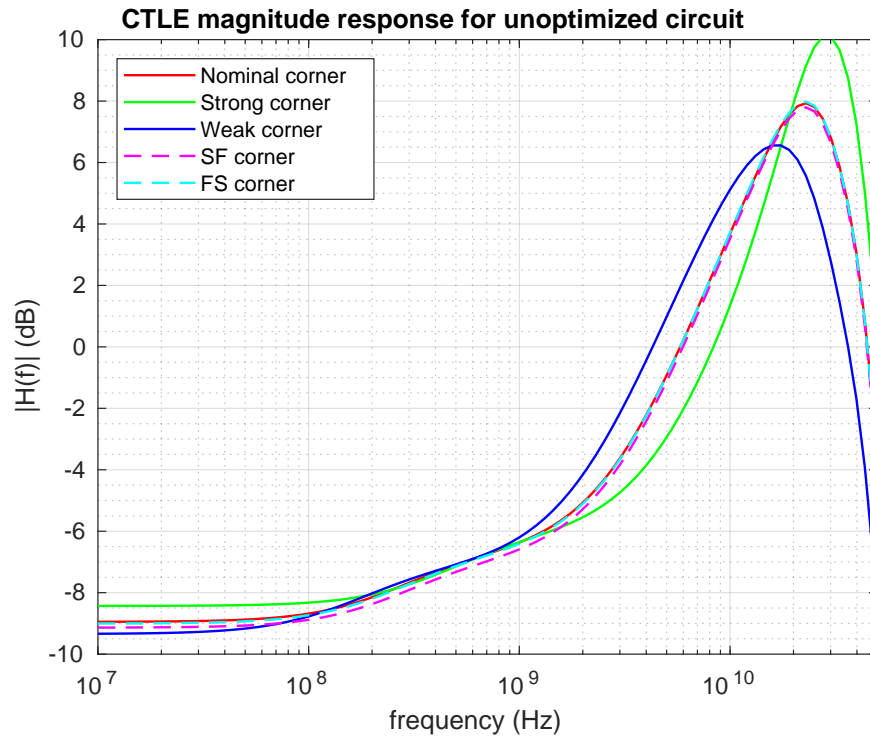
(a)
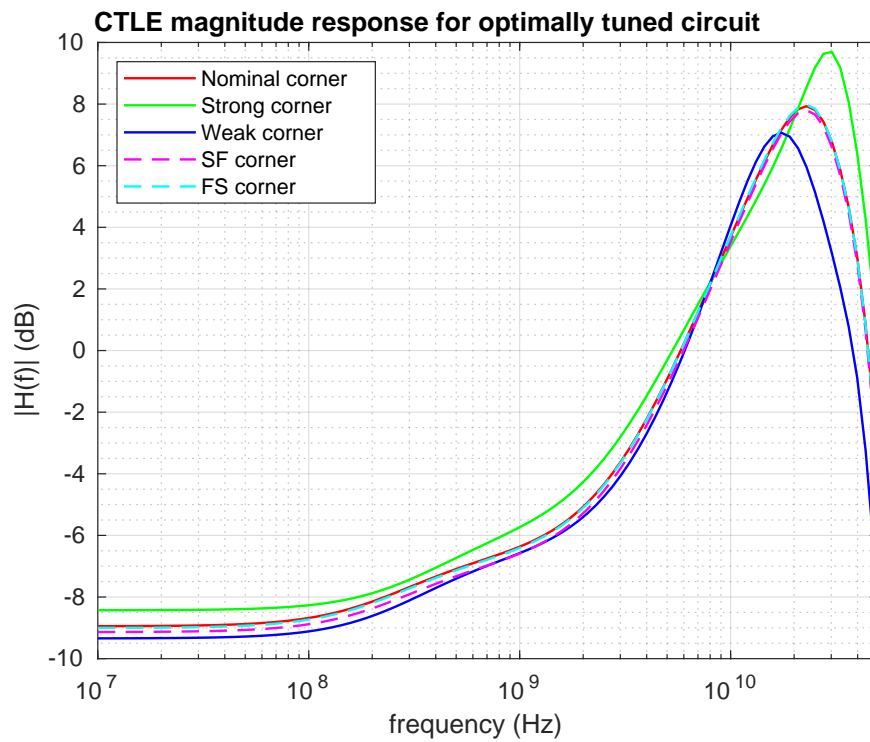
(b)

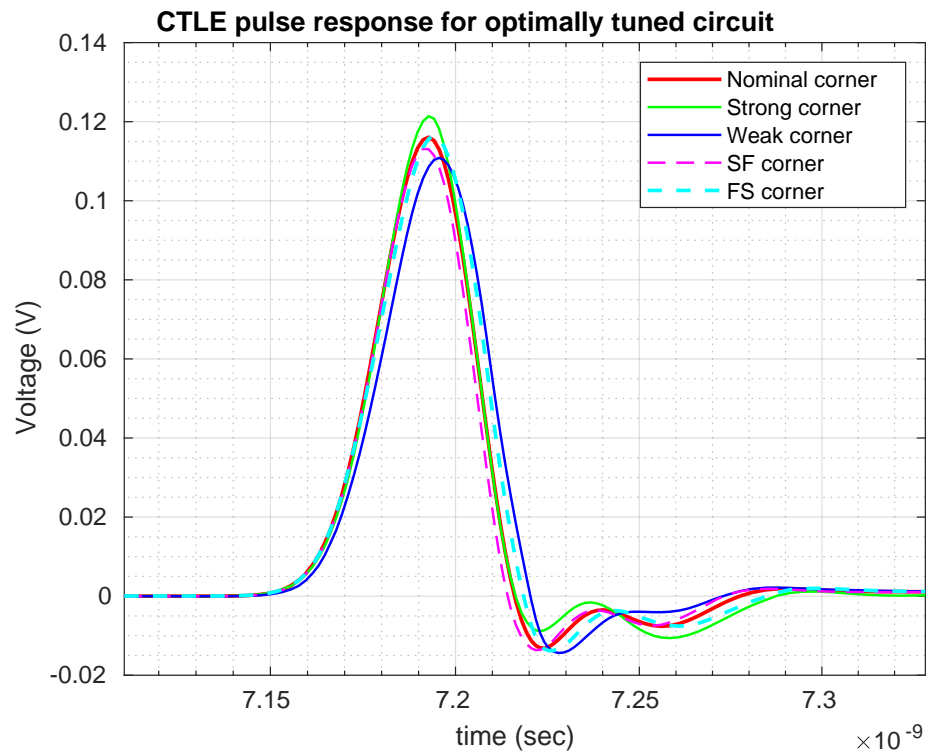**Figure 4.14:** CTLE magnitude response across PVT corners for: (a) un-optimized circuit (b) optimally-tuned circuit.
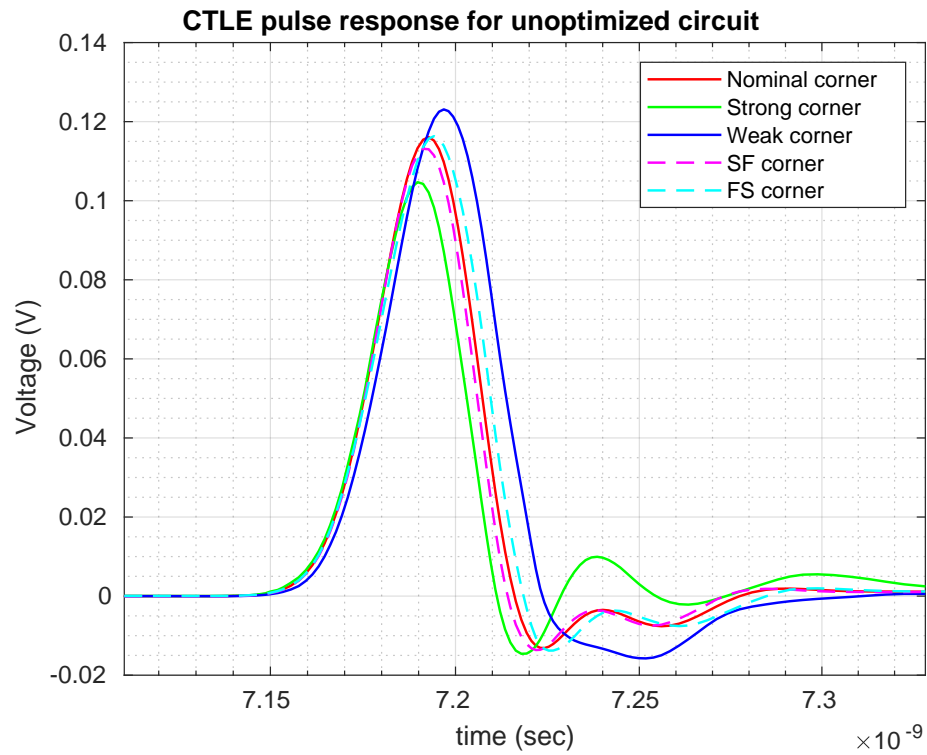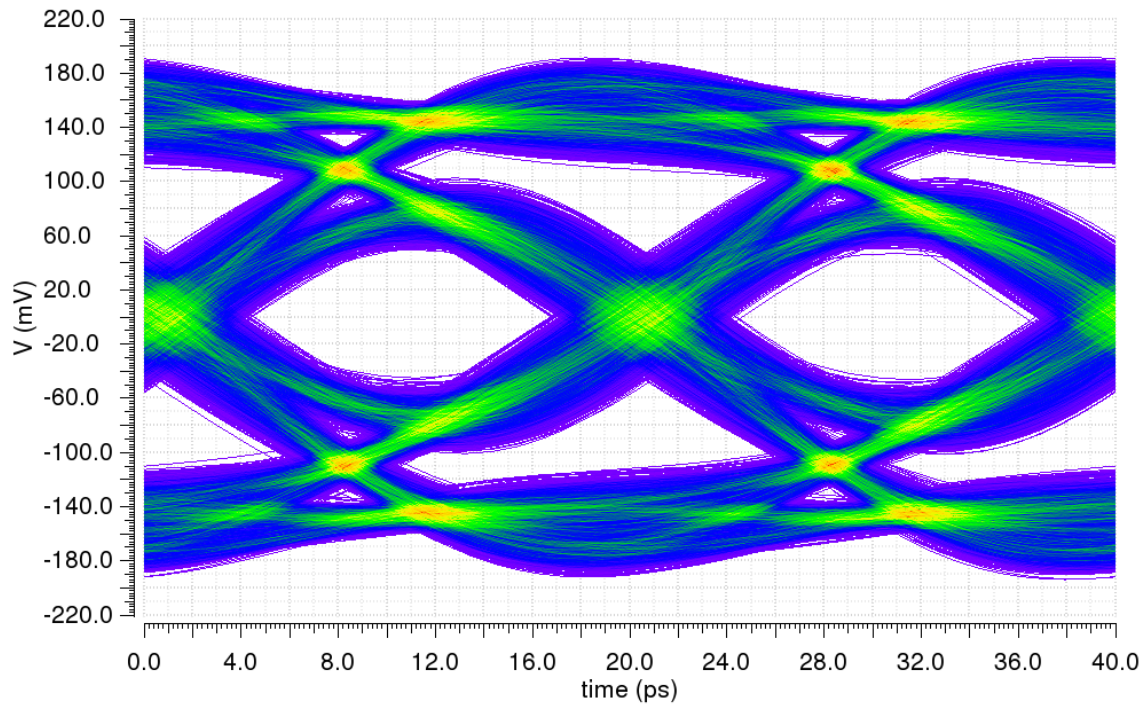
(a)

(b)

Figure 4.15: CTLE pulse response across PVT corners for: (a) un-optimized circuit (b) optimally-tuned circuit.

(a)
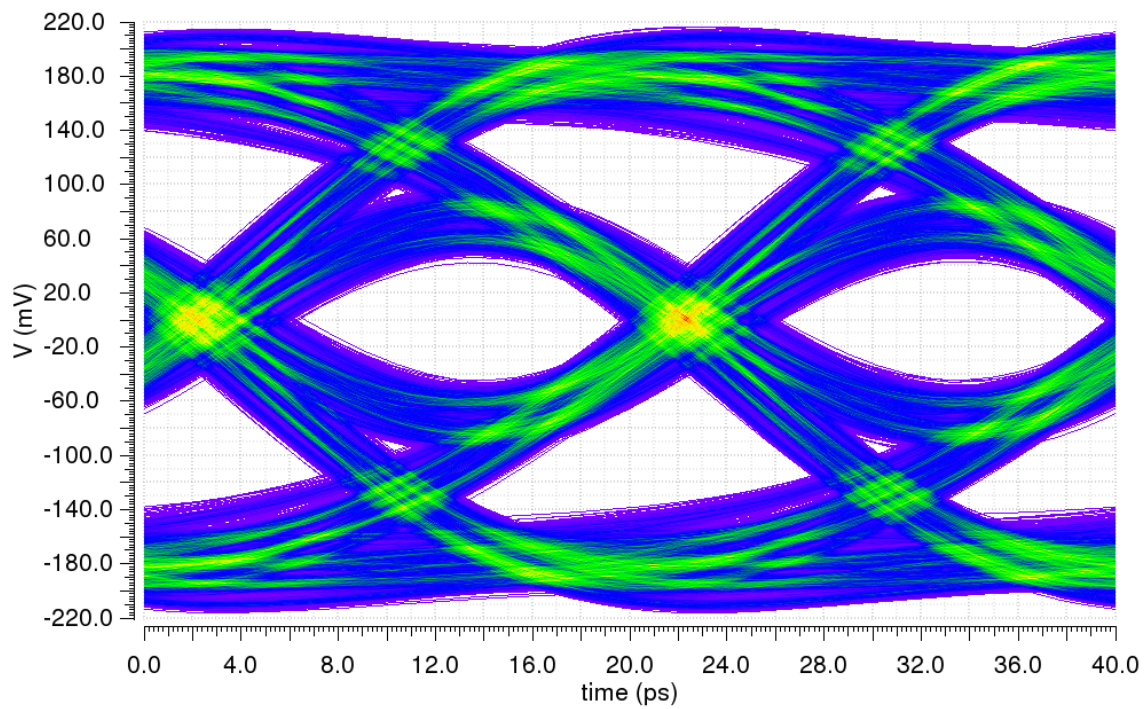
(b)

Figure 4.16: Eye diagram at the CTLE output for Strong corner for 50 Gbps NRZ data rate for: (a) un-optimized circuit (Pulse PMR=2.7) (b) optimally-tuned circuit (Pulse PMR=2.82).

(a)

(b)

Figure 4.17: Eye diagram at the CTLE output for Weak corner for 50 Gbps NRZ data rate for: (a) un-optimized circuit (Pulse PMR=3.21) (b) optimally-tuned circuit (Pulse PMR=2.97).
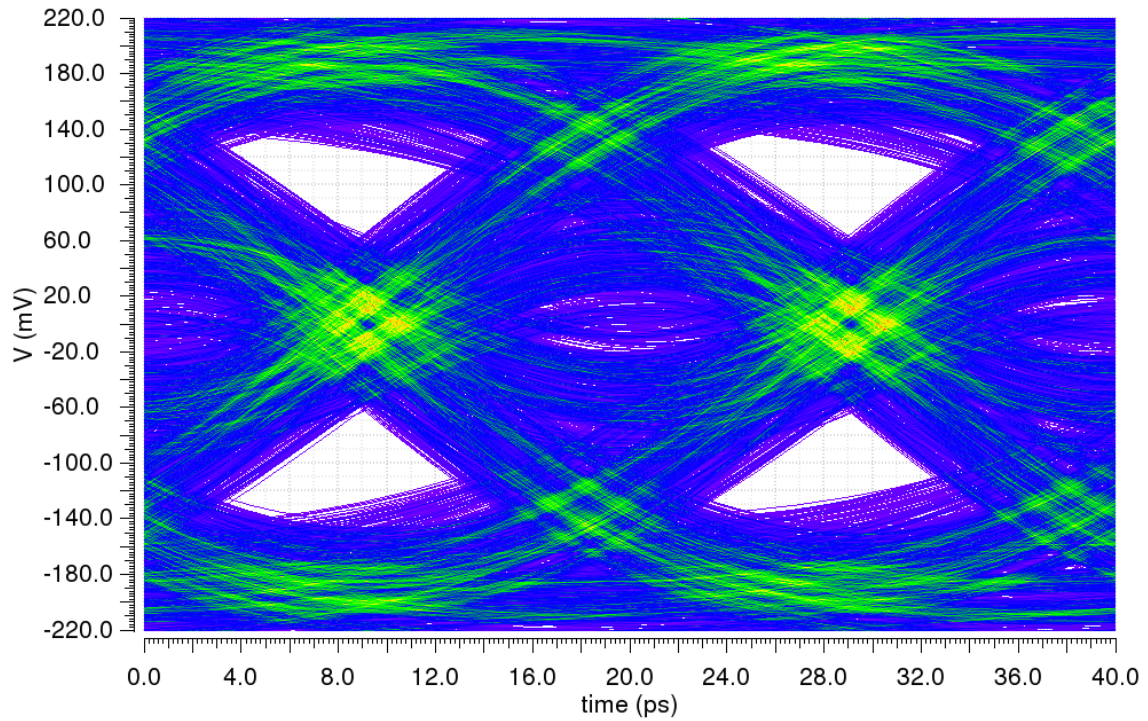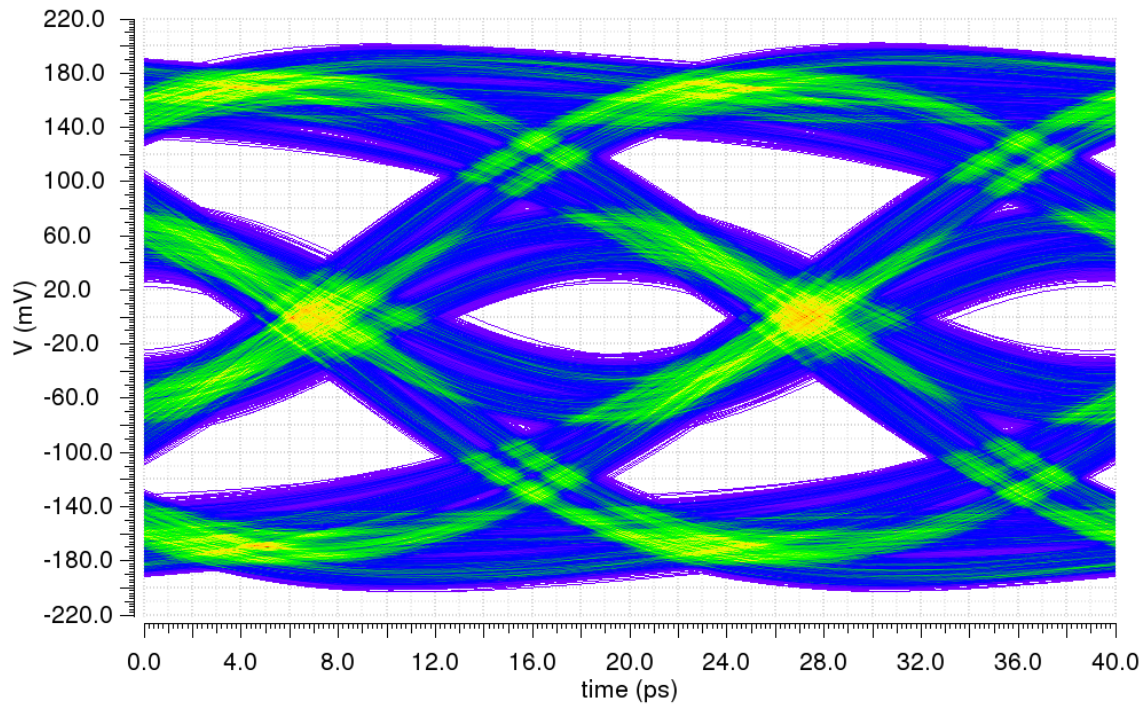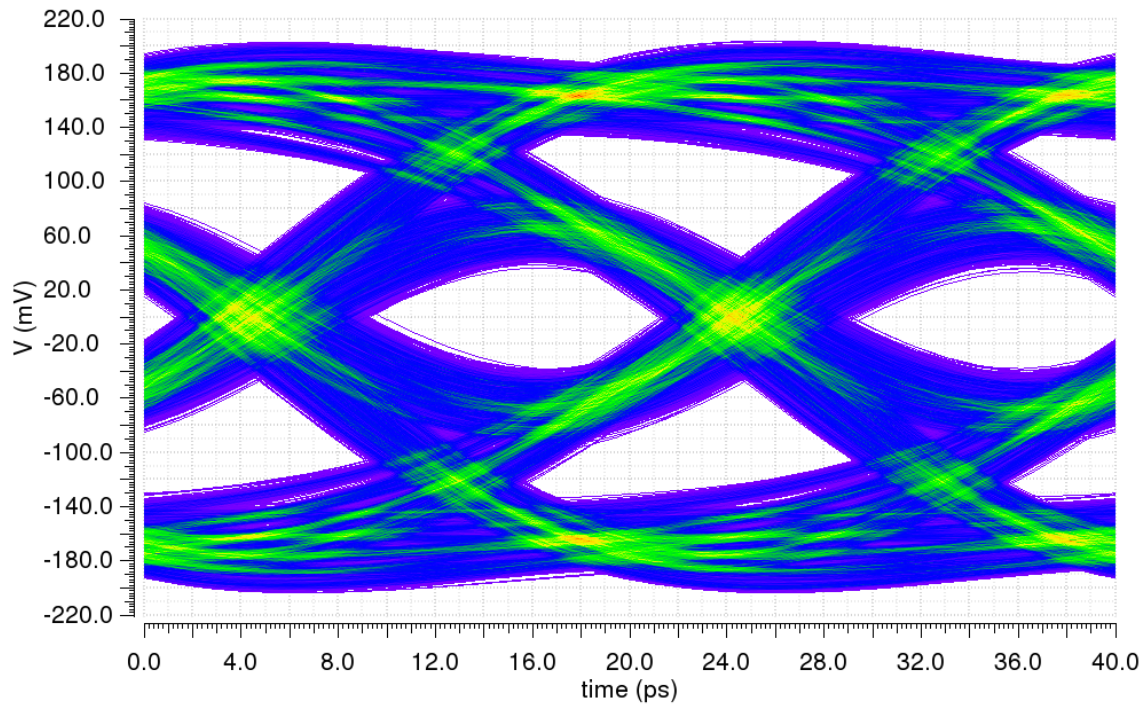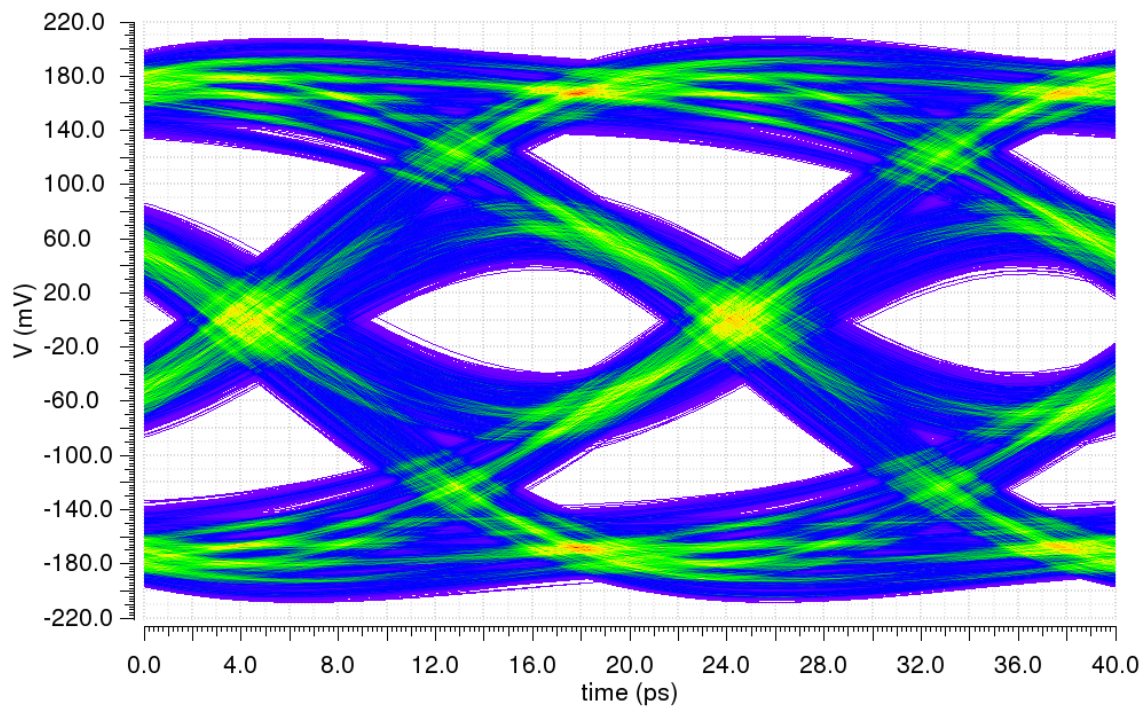
(a)

(b)

Figure 4.18: Eye diagram at the CTLE output for 50 Gbps NRZ data rate for: (a) SF corner (Pulse PMR=2.75) (b) FS (Pulse PMR=3) corner.

4.7. Common-mode bias stability

The feedback loop in the CTLE architecture ensures that the common-mode voltage at each node is biased to $\sim$ half of the supply voltage for FinFET process. This loop is stable with a minimum phase margin of $\approx 65^o$ and a gain margin of ~ 25 dB across PVT. The transient common-mode voltage at each CTLE stage for 112 Gbps PAM-4 PRBS data pattern is shown in Figure 4.19. The variation in the common mode voltage at HF-CTLE and MF-CTLE stages is very small. The buffer-stage output common-mode voltage is also stable but wiggles by a certain tolerable amount.

- HF-CTLE output common mode voltage
- MF-CTLE output common mode voltage
- Buffer stage output common mode voltage
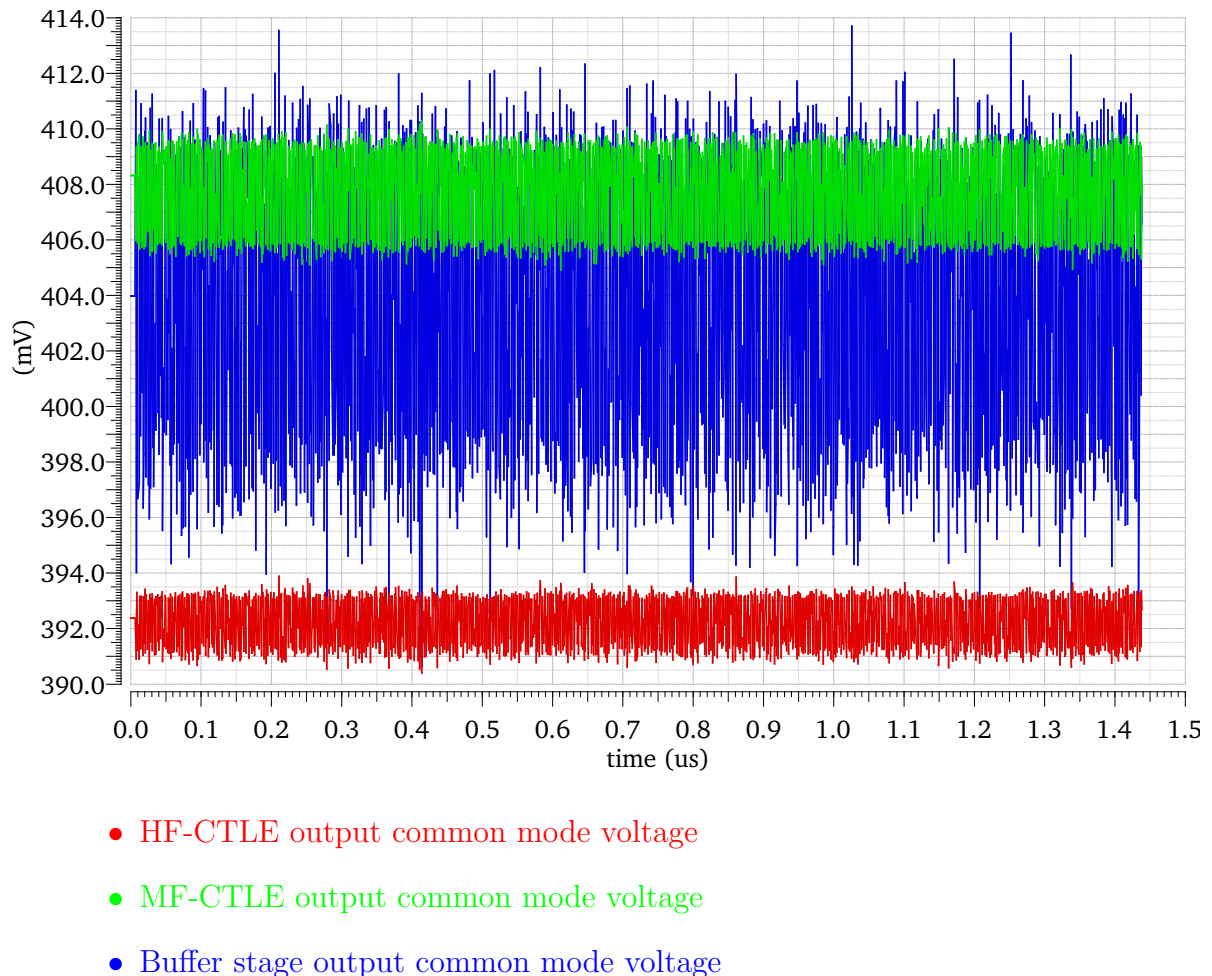
Figure 4.19: Common mode voltage at each stage of CTLE for 112 Gbps PAM-4 PRBS data transitions

4.8.   Common-mode frequency response and PSRR

Figure 4.20 shows common-mode frequency response for the analog front end. The plot shows that the closed loop system is able to reject common-mode noise till a frequency of ~ 1 MHz. Figure 4.21 shows the impact of supply noise on the common-mode output of each CTLE stage. The closed loop system is able to reject supply noise till ~ 100 MHz. Figure 4.22 shows the impact of supply noise on the differential output of each CTLE stage. For the case mismatch is not considered, the system rejects supply noise to large extent even in GHz frequency range.

Figure 4.20:   Common-mode frequency response of the analog front-end for 0 dB input common-mode AC signal at channel output.

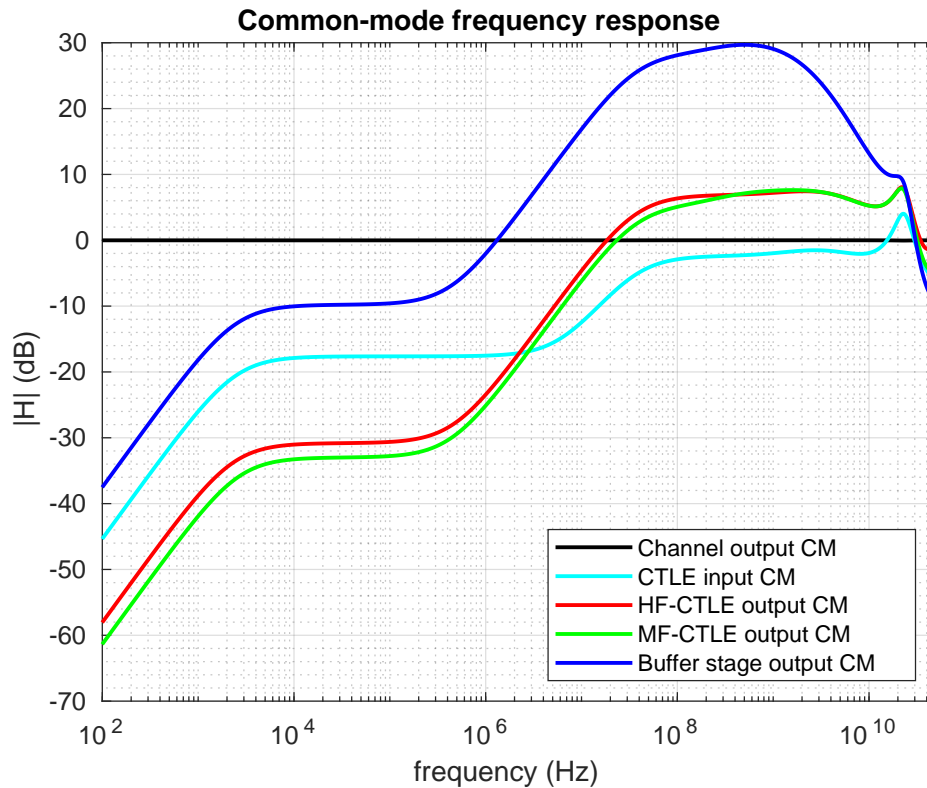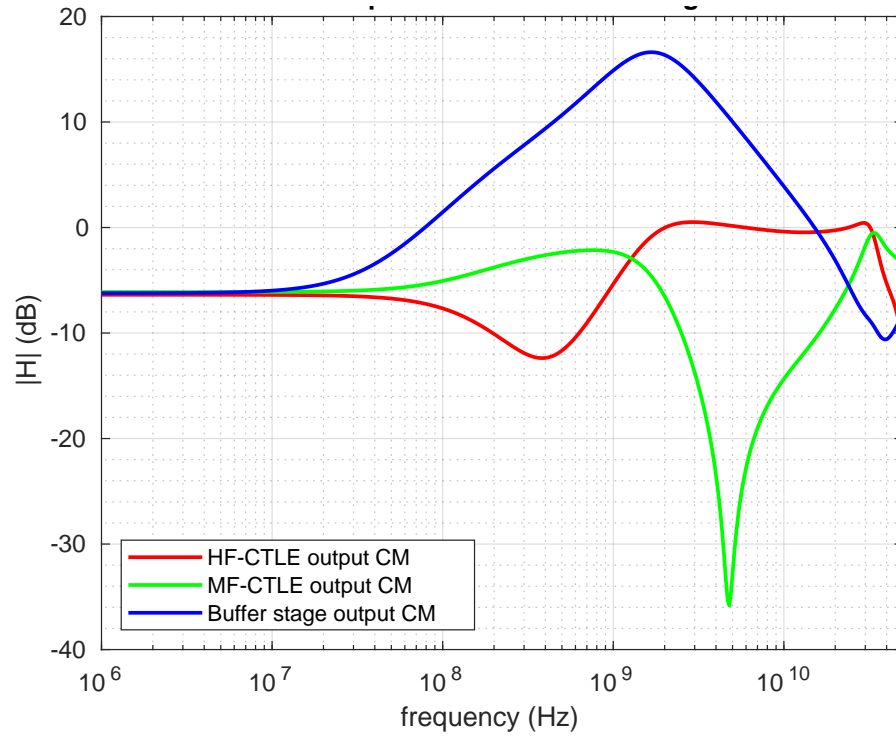**Figure 4.21:** Transfer function of supply noise from supply to output common-mode voltage at each CTLE stage
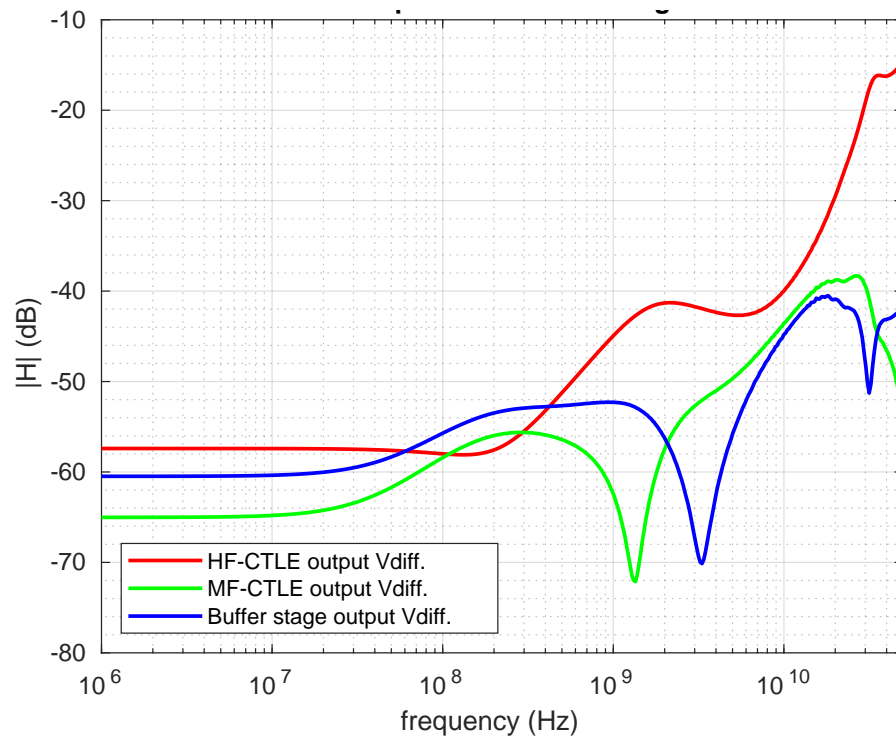
Figure 4.22: Transfer function of supply noise from supply to output differntial voltage at each CTLE stage

4.9. Thermal noise effect on the eye diagram

Figure 4.23 shows eye diagram at CTLE output for 50 Gbps NRZ data rate for 2k PRBS (PN-32) data symbols. Figure 4.24 shows very small degradation in the eye when thermal noise is enabled during transient simulation. However, the AC noise simulation prediction of 2 mV integrated output thermal noise seems bit pessimistic.

Figure 4.23: CTLE eye diagram for 50 Gbps NRZ data rate (without thermal noise)

Figure 4.24: CTLE eye diagram for 50 Gbps NRZ data rate (with thermal noise)

4.10.   Power breakdown

The inverter based CTLE consumes a total of 10 mW power. Figure 4.25 shows the percentage of power consumption for each block in the CTLE.
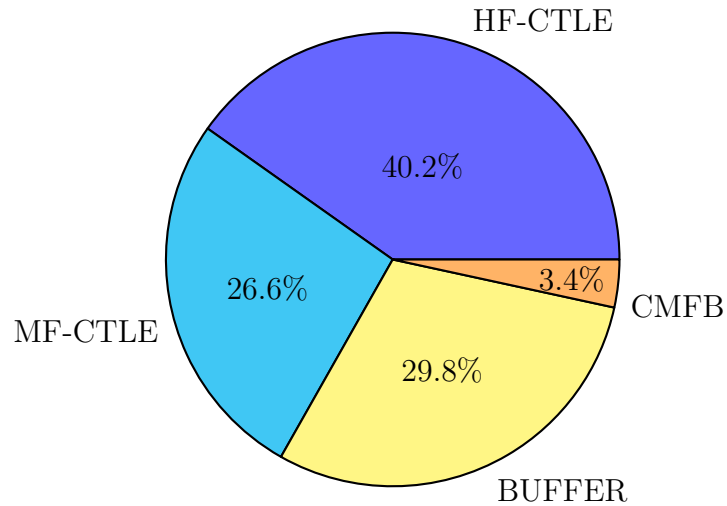
Figure 4.25: CTLE power breakdown

4.11.   Comparison of inverter based CTLE with other recent works

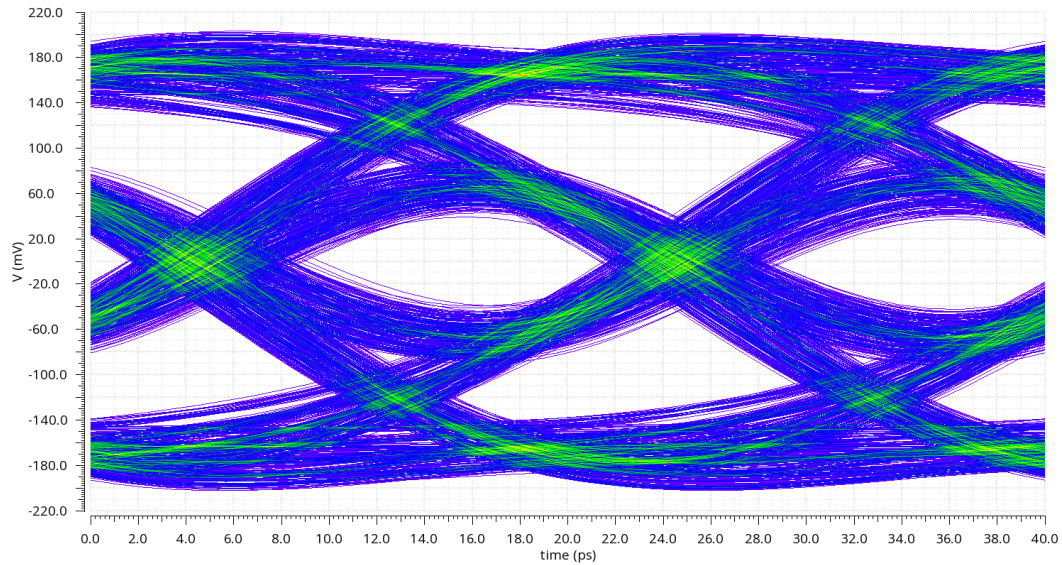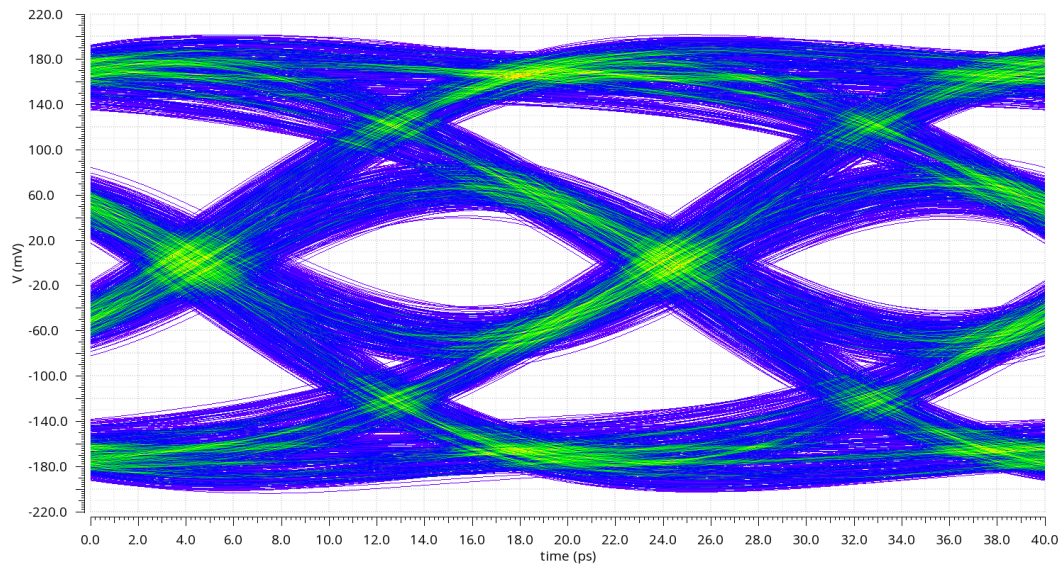Table 4.2 shows comparison between the work in this project with other state of the art CTLEs published in 16nm FinFET technology. Due to lack of information about the circuit specifications (especially load capacitance and signal swings) in the publications, it is challenging to do a fair comparison with other state of the art designs.

The CTLE presented in this work provides an overall gain of 17 dB which is ~ 40 % higher than the design presented in [19]. The capacitive load considered in this design is 100 fF which is ~ 3.2 times the load considered in [19]. The power consumed by this CTLE is 10mW which is higher than that in [19], but is lower than the design presented in [34].

The power consumption of a CTLE depends a lot on the nyquist frequency of operation and the load capacitance. So, to make a fair comparison, a parameter $\frac{Power}{Frequency*Load-cap}$

Table 4.2: Comparison table for inverter based CTLE

	This work	[19]	[28]	[29]	[30]
Technology	16 nm FinFET	16 nm FinFET	16 nm FinFET	16 nm FinFET	16 nm FinFET
Supply volatge	0.8 V	1.2 V + Ground LDO	1.2 V	1.2 V	1.2 V
CTLE type	Inverter	Inverter	Inverter	CML	CML
Modulation	PAM-4	PAM-2	PAM-4	PAM-4	PAM-2
Nyquist frequency	28 GHz	28 GHz	14 GHz	14 GHz	28 GHz
DC gain / Nyquist gain	-9 dB / 8dB	-6 dB / 6 dB	_	0 dB / 7 dB	-6 dB / 6 dB
Channel loss at Nyquist	30 dB *	8 dB	35 dB *	31 dB *	8 dB
Load capacitance	100 fF	30 fF	–	–	–
Power	10 mW	6 mW	34 mW	8.4 mW	6 mW
$\frac{Power}{Frequency*Load-cap}$	3.57 V^2	7.14 V^2	–	–	–
Area	90 μm x 80 μm	20 μm x 15 μm	50 μm x 85 μm	125 μm x 40 μm	80 μm x 50 μm

    *   CTLE provides fraction of total equalization requirement

    –   Information not reported

is used as figure of merit and its lower value implies more power efficient architecture. On the basis of this parameter, this CTLE outperforms the design in [19] in terms of power efficiency.

Moreover, this CTLE uses a high pass filter prior to CMOS amplifier in HF-CTLE stage, which attenuates low-frequency signals and thus reduces signal swing before amplification. But the architecture in [19] uses a high pass filter after amplifier, so my understanding is that it increases signal swing and makes the architecture in [19] difficult for PAM-4 applications or to meet linearity and so, a higher supply voltage of 1.2 V is used. The same author of [19] proposes a separate architecture for PAM-4 application [28] to meet linearity requirements, but with a different load (not quantified in

fF). The power consumption increases a lot in [28] because of power hungry architecture. This work (our AFE) works for 1 V_{pp} differential input signal swing while [19] works for 600 mV_{pp} differential input signal swing. However, linearity is not quantified in the state of the art designs, so it is not possible to do fair comparison.

[29] and [30] use CML based CTLE architecture and make use of passive inductors and thus consume larger area as compared to [19] and [28]. But their load capacitance is not known, so it is again difficult to compare.

This design is able to operate at a low supply voltage of 0.8 V, driving a load capacitance of 100 fF with PVT tracking ability.

This work uses least voltage supply and very low power consumption for a load capacitance of 100 fF. Moreover, this design provides relatively high AC gain. The CTLE core in this work does not have compact layout, uses 4 passive inductors and also the area of CMFB with large compensation capacitor is included in the mentioned numbers. In order to drive larger capacitive load of 100 fF, the design in this work becomes very challenging to meet bandwidth requirements. The mentioned numbers in this work will improve a lot for a smaller load capacitor as in [19].

4.12.   Conventional CTLE design results

A CML based conventional CTLE is also designed to drive the same capacitive load in order to compare its power consumption against the inverter based CTLE. The CTLE architecture (shown in Figure 4.26) consists of three stages similar to the inverter based CTLE. The results shown for conventional CTLE are based on layout level extracted netlist at block level. The individual layout blocks need to be connected at top-level yet. The CTLE design here uses a higher supply voltage of 1.05V to ensure adequate V_{ds} saturation margin for transistors to keep in saturation.

The magnitude response of the conventional CTLE is shown in Figure 4.27. The response is similar to the inverter based CTLE except that the bandwidth of the con-
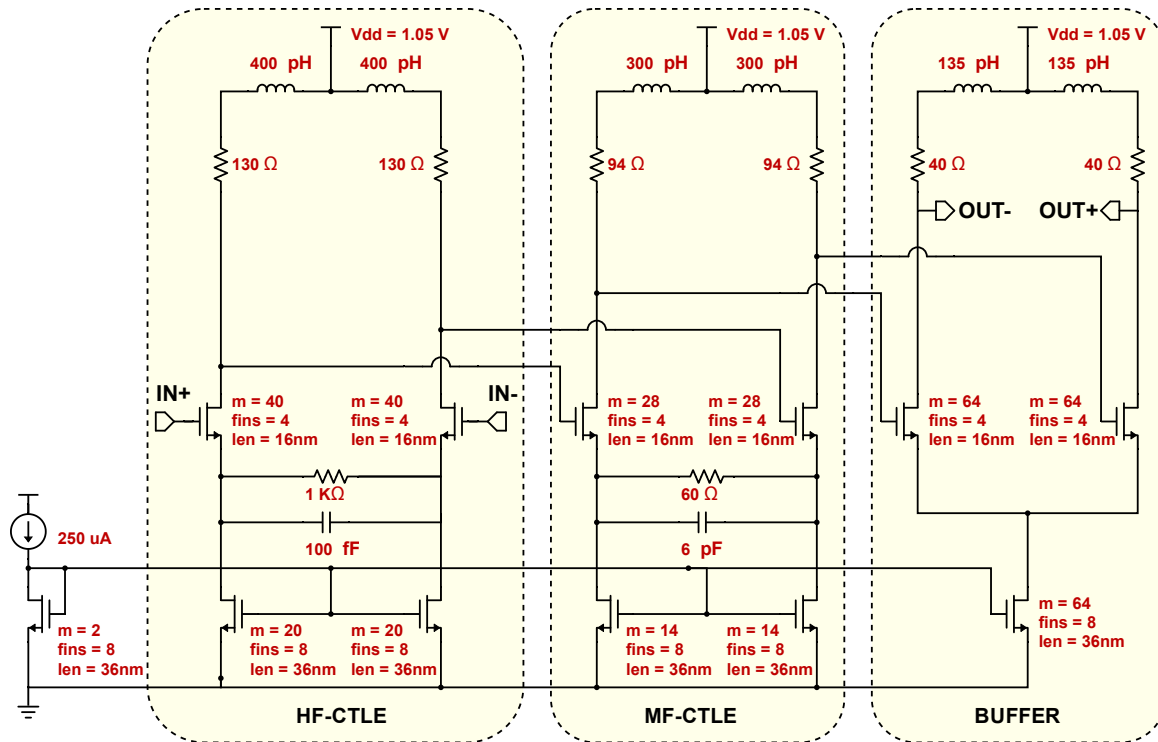
Figure 4.26: Conventional CTLE architecture.

ventional CTLE is better than the inverter based CTLE, primarily due to the use of passive inductors. Moreover, this CTLE does not have any tunability circuitry which can degrade the circuit bandwidth significantly.

The pulse response of this CTLE is shown in Figure 4.29. The eye diagrams for 64 and 40 Gbps PAM-4 data rates are shown in Figures 4.32 and 4.33 respectively. These eye-diagrams are better than the inverter based CTLE primarily because of more bandwidth. Figure 4.30 shows the conventional CTLE has less thermal noise than inverter based CTLE. Figure 4.31 shows total harmonic distortion for both CTLEs when pure sinusoidal differential signal is provided at the input of the analog front-end. The THD is calculated for input signal frequency of 1 MHz because the CTLE will suffer maximum non-linearity at low frequency (because channel does not attenuate low frequency signals).

Comparison between the inverter based CTLE and the conventional CTLE: Table 4.3 provides comparison between both the CTLEs. To summarise, the inverter
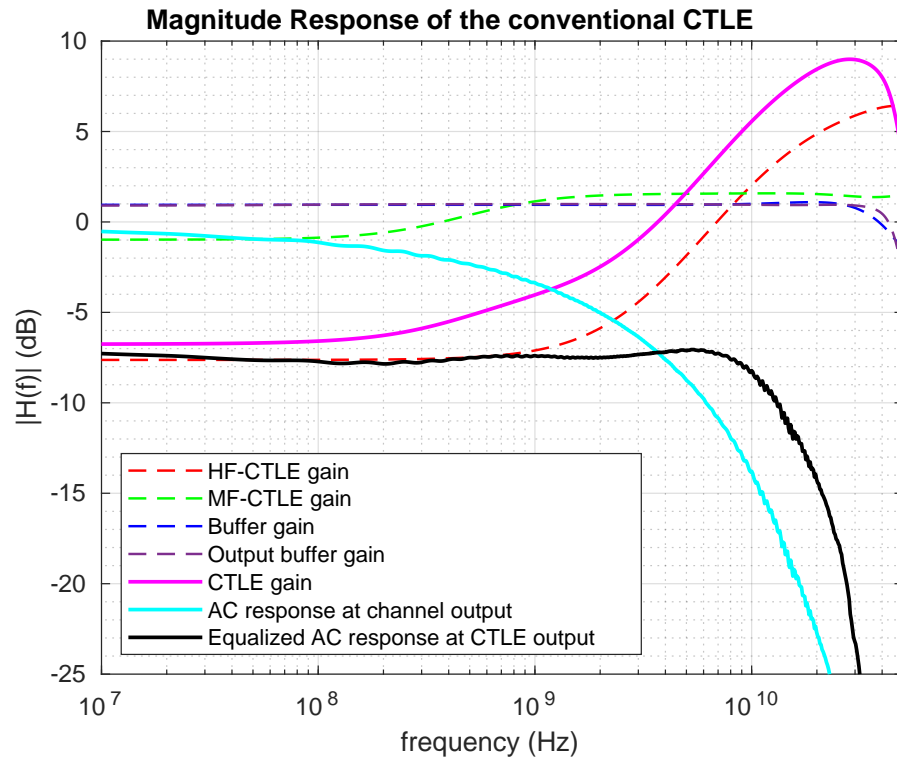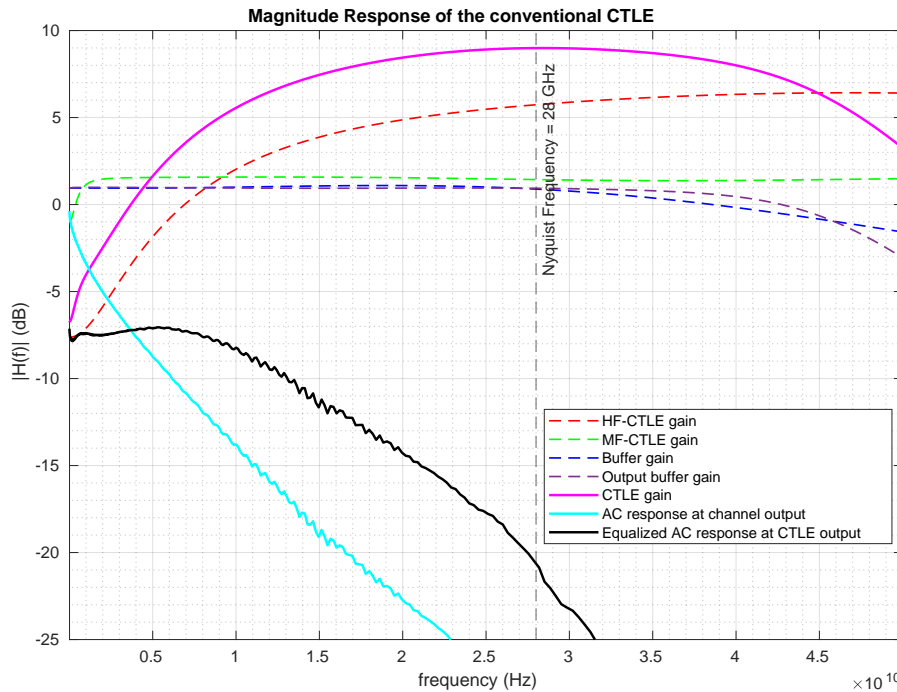
Figure 4.27: Magnitude response of the conventional CTLE.

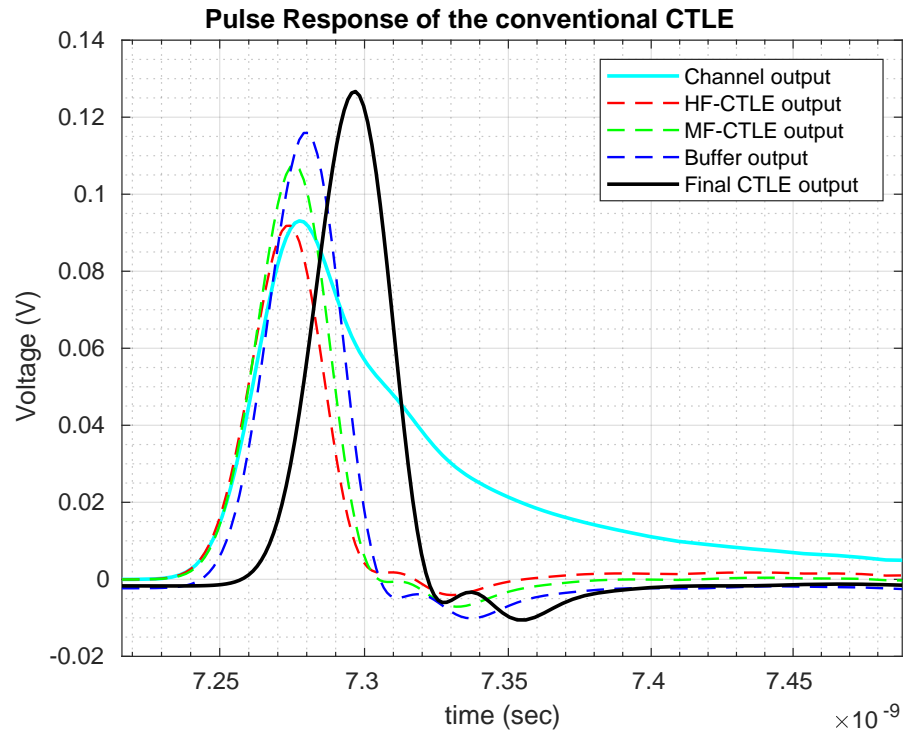**Figure 4.28:** Magnitude response of the conventional CTLE for linear frequency scale.

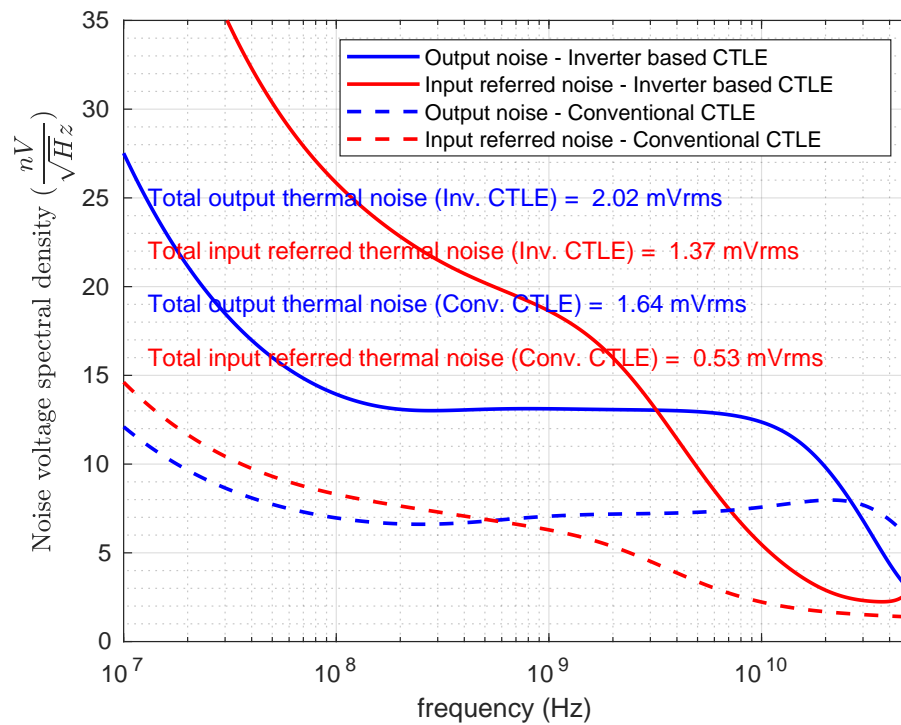**Figure 4.29:** Pulse response of the conventional CTLE.

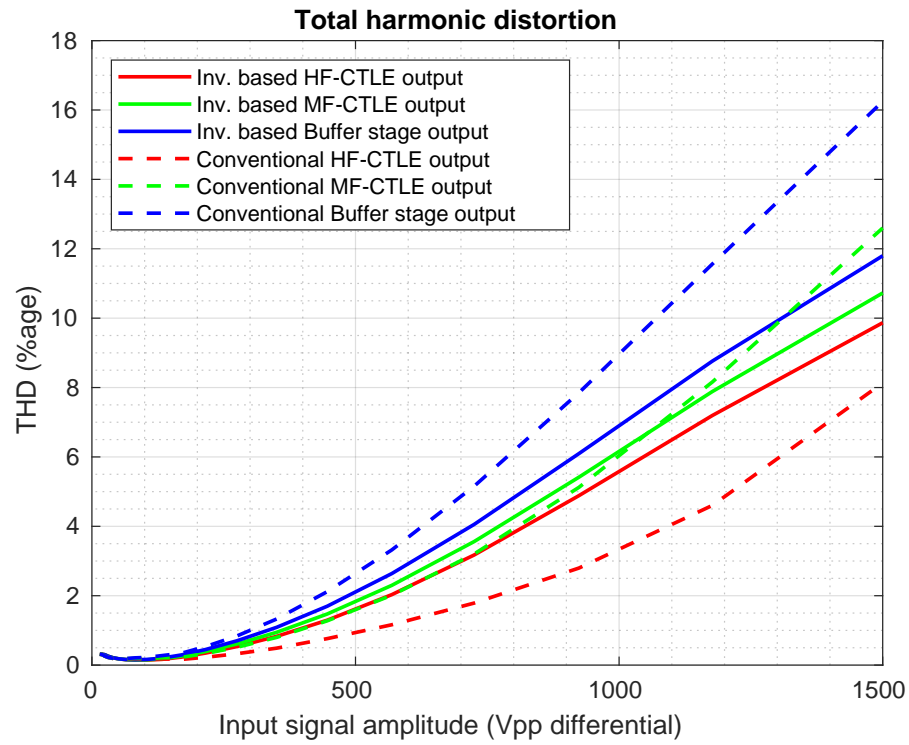**Figure 4.30:** Thermal noise spectral density

Figure 4.31: Total harmonic distortion
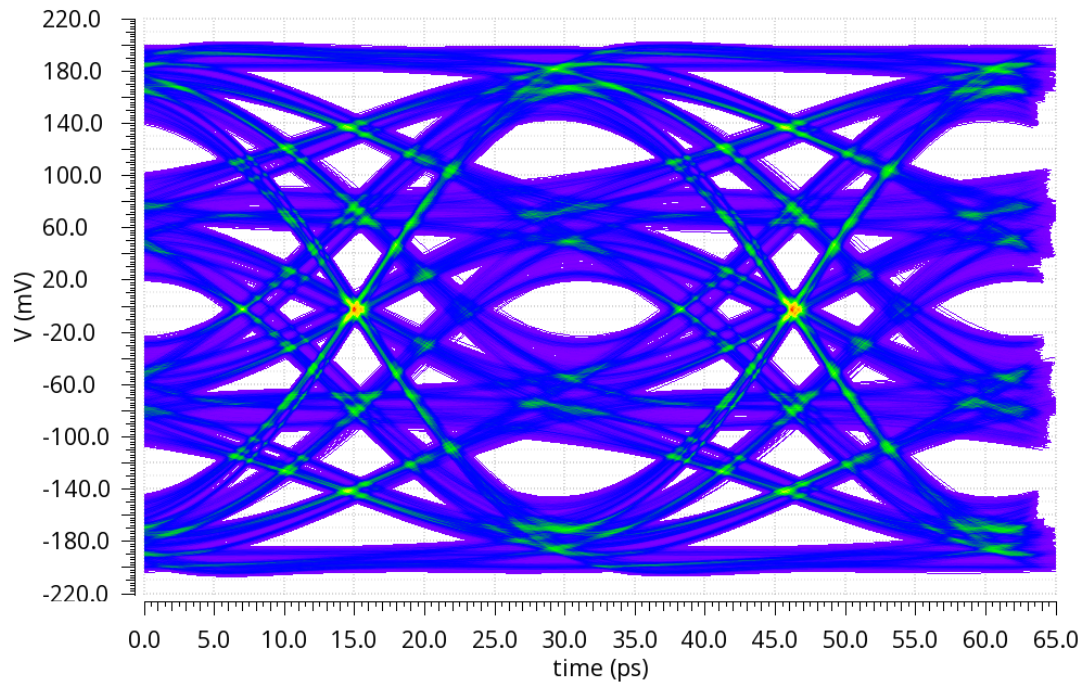
Figure 4.32: Eye diagram at the output of the conventional CTLE for 64 Gbps PAM-4 data rate.
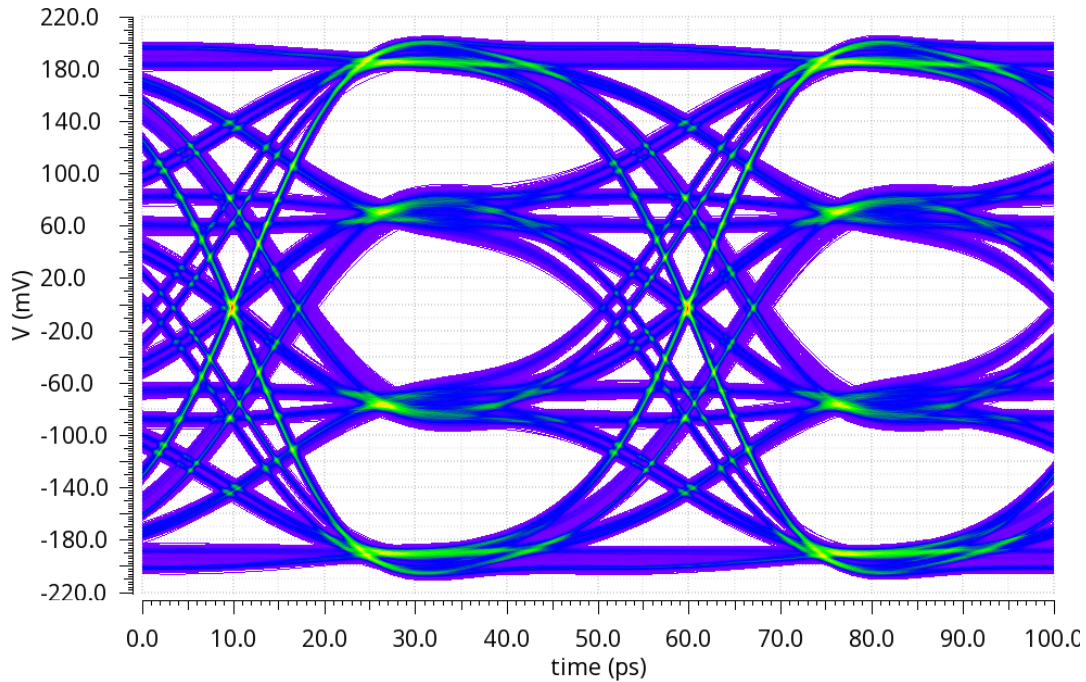
Figure 4.33: Eye diagram at the output of the conventional CTLE for 40 Gbps PAM-4 data rate.

based CTLE is better in terms of supply voltage, power consumption, area, PVT insensitivity and tunability. However, the conventional CTLE offers better bandwidth and linearity. The bandwidth of the inverter based CTLE can improve a lot if the load capacitance can be decreased or if the extent of the tunability can be reduced so that there are less additional parasitics.

Table 4.3: Comparison between the inverter based CTLE and the conventional CTLE

	Inverter based CTLE	Conventional CTLE
Supply voltage	0.8 V	1.05 V
DC gain / Nyquist gain	- 9 dB / 8 dB	-8 dB / 9 dB
Power	10 mW	17 mW
Area	Less (4 passive inductors)	More (6 passive inductors)
PVT sensitivity	less (gain levels of HF-CTLE and MF-CTLE are PVT invariant. Tunability can track remaining PVT variations)	more
Tunability	power-scalable, mainly due to tristate inverters	may have some tunability
Linearity	less (as inferred from PAM-4 eye-diagrams)	better (as inferred from PAM-4 eye-diagrams because it uses higher supply voltage too)
Bandwidth	less (Active inductors are difficult to realize at high data rate especially when driving high capacitive load. Also additional parasitics due to tunability degrade the bandwidth a lot)	more (because of passive inductors)
Integrated output thermal noise	2 mV	1.4 mV

5   Conclusion

5.1. Summary

This thesis presents the design of a low power analog front end for 112 Gbps PAM-4 data rate for LR SERDES application. It is implemented in 16nm CMOS FinFET technology and the results shown are based on layout level extracted netlist. This design uses passive equalization techniques in the front-termination network to overcome the signal attenuation caused by the channel, ESD cells, bump pads and other parasitics. The CTLE design exploits the power advantage in using a CMOS inverter based amplifier instead of the conventional CML based differential amplifier. Moving forward with the choice of a CMOS inverter as a basic design element, this CTLE provides 17 dB of equalization, consuming 10 mW power with a 0.8 V supply voltage, which is significantly smaller than the previous state of the art CTLE designs. Inverter based active inductor is used instead of coil based passive inductor in some stages to reduce the area. A common-mode feedback loop ensures robust biasing (low-power solution too) for the amplifiers. The tunability offered in this design enables power-scalable design and also helps to track the PVT variations.

5.2. Future work

This design will be fabricated in 16nm FinFET technology to test its performance. The CTLE designed in this work is a part of the SERDES transceiver chain. To fully equalize the channel and observe the improvement in the overall system efficiency, there is a need to include the remaining equalization blocks, which is possible by having an ADC and DSP after the CTLE.

Another inverter based CTLE architecture can be explored where MF-CTLE stage acts as a parallel path instead of a cascade after HF-CTLE, to see if that provides better bandwidth and power efficiency. My perception is that it will have higher loop-bandwidth for the CMFB, which is better for PSRR. At one time during the design of this CTLE, there was an attempt to use variac capacitors to tune zero location of the CTLE, but it could not be used because of discrepancy in the model file. I believe use of variac capacitors can be a better choice than capacitor with series transistor switch to tune the circuit, as it does not include the switch parasitics.

Driving a large capacitance of 100 fF limits the performance of the CTLE and poses several design challenges in this work. If the input load capacitance of the following ADC block can be reduced, it is possible to significantly improve the performance (can eliminate the need for some passive inductors, better active inductors implementation and more power-efficient design with better bandwidth) of the proposed CTLE design, without the need to look for other CTLE architectures.
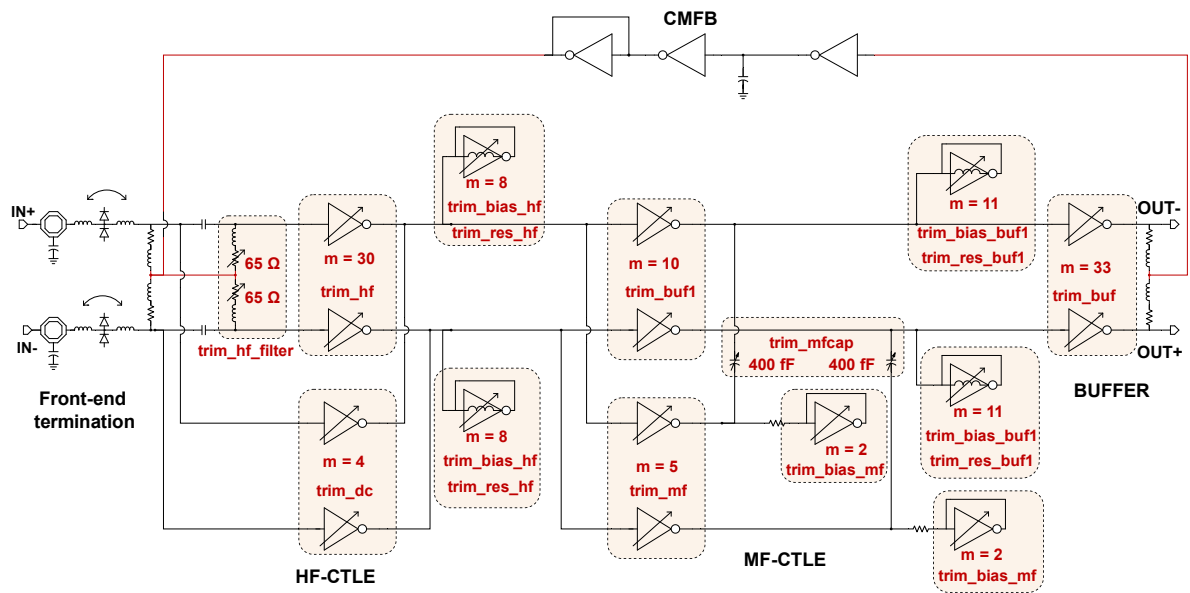
Appendix

Tunability information in detail

Figure 5.1: CTLE architecture with tunability knobs information

Table 5.1: Tunability knobs information

	No of bits	Comments
$Trim_{hf-filter}$	5	controls zero location of HF-CTLE
$Trim_{hf}$	4	controls g_m of the amplifier
$Trim_{bias-hf}$	3	controls active load resistance
$Trim_{res-hf}$	3	tunabile active inductance
$Trim_{dc}$	3	controls g_m of the amplifier
$Trim_{buf1}$	3	controls g_m of the amplifier
$Trim_{bias-buf1}$	3	controls active load resistance
$Trim_{res-buf1}$	3	tunabile active inductance
$Trim_{mf}$	3	controls g_m of the amplifier
$Trim_{bias-mf}$	5	primarily controls zero location of MF-CTLE
$Trim_{mf-cap}$	3	controls zero location of MF-CTLE
$Trim_{buf}$	4	controls g_m of the amplifier
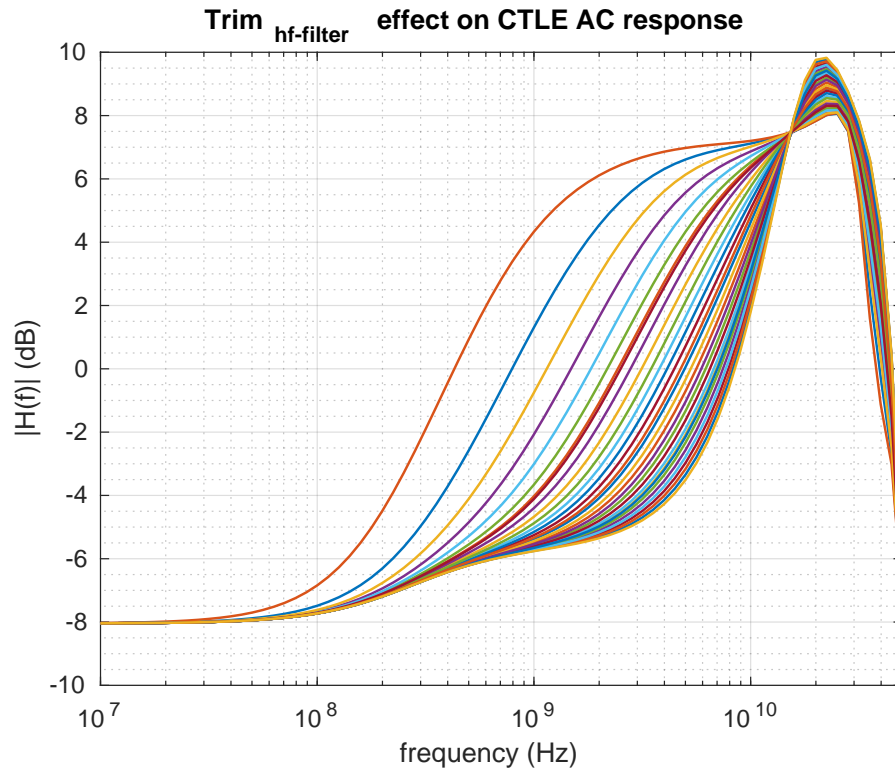
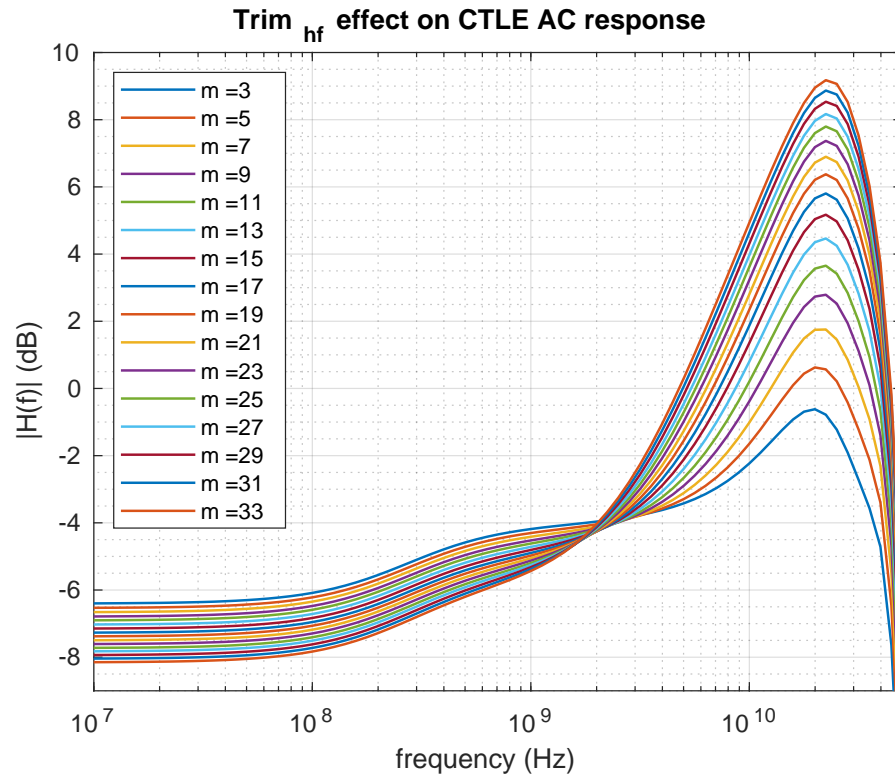**Figure 5.2:** $Trim_{hf-filter}$ effect on the CTLE transfer function.

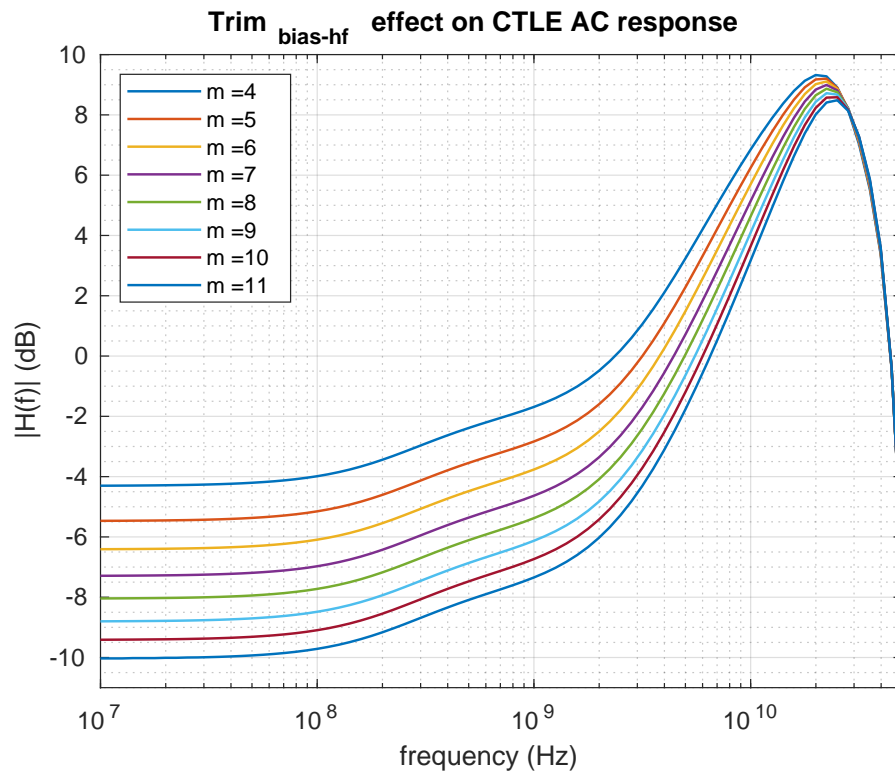**Figure 5.3:** $Trim_{hf}$ effect on the CTLE transfer function.

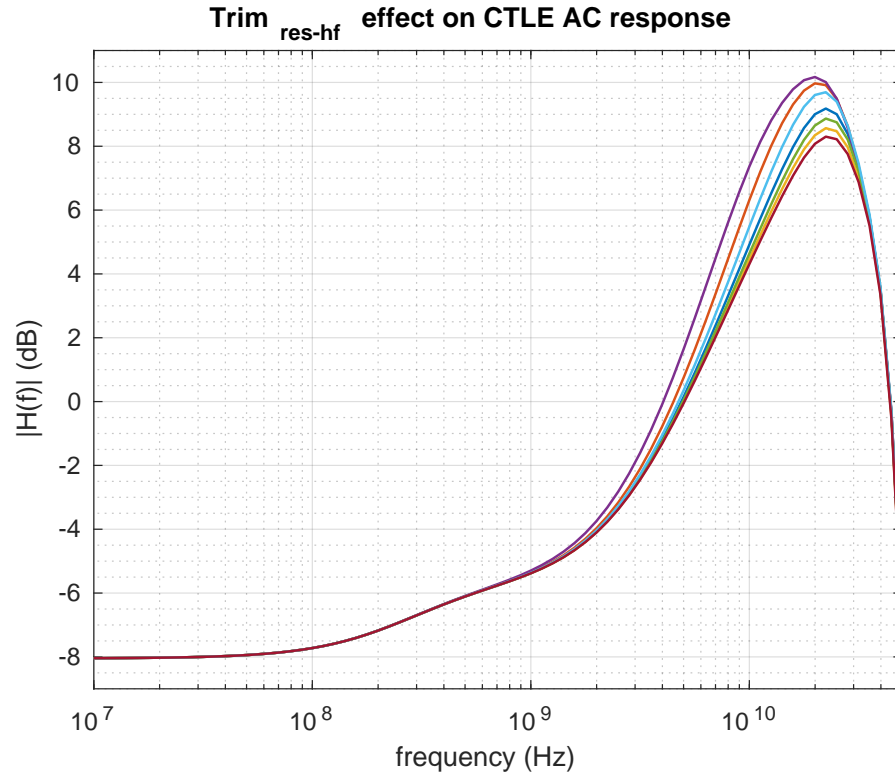**Figure 5.4:** $Trim_{bias-hf}$ effect on the CTLE transfer function.

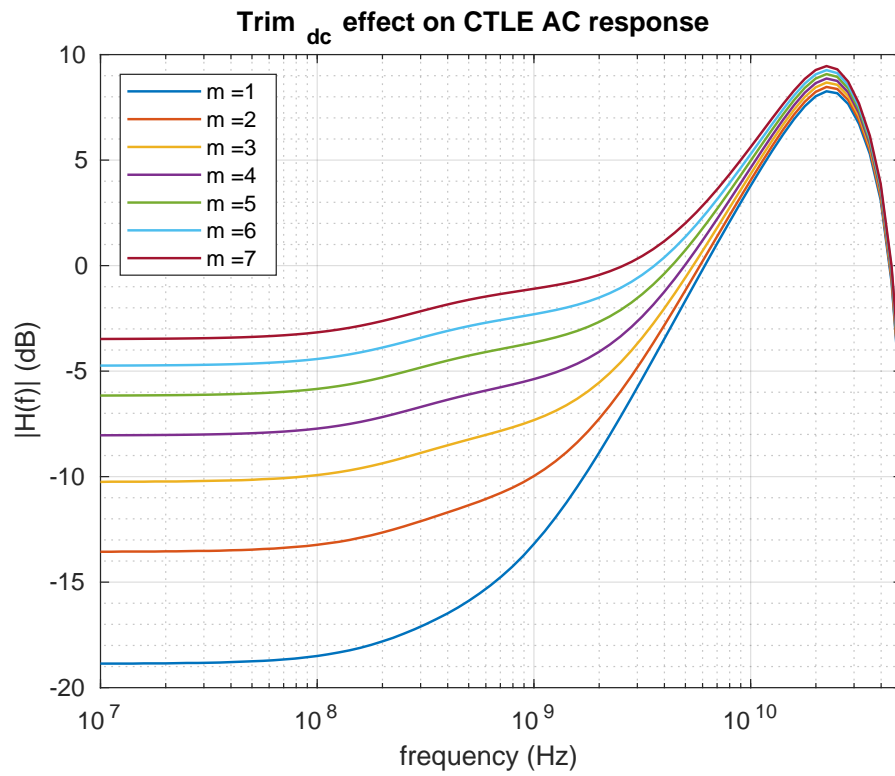**Figure 5.5:** $Trim_{res-hf}$ effect on the CTLE transfer function.

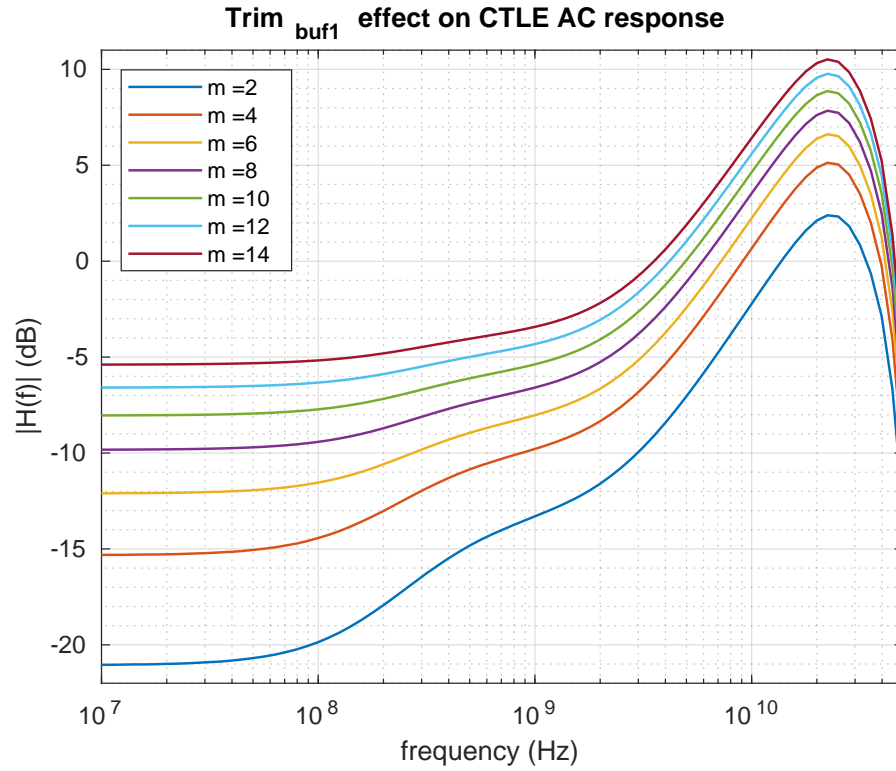**Figure 5.6:** $Trim_{dc}$ effect on the CTLE transfer function.

Figure 5.7: $Trim_{buf1}$ effect on the CTLE transfer function.
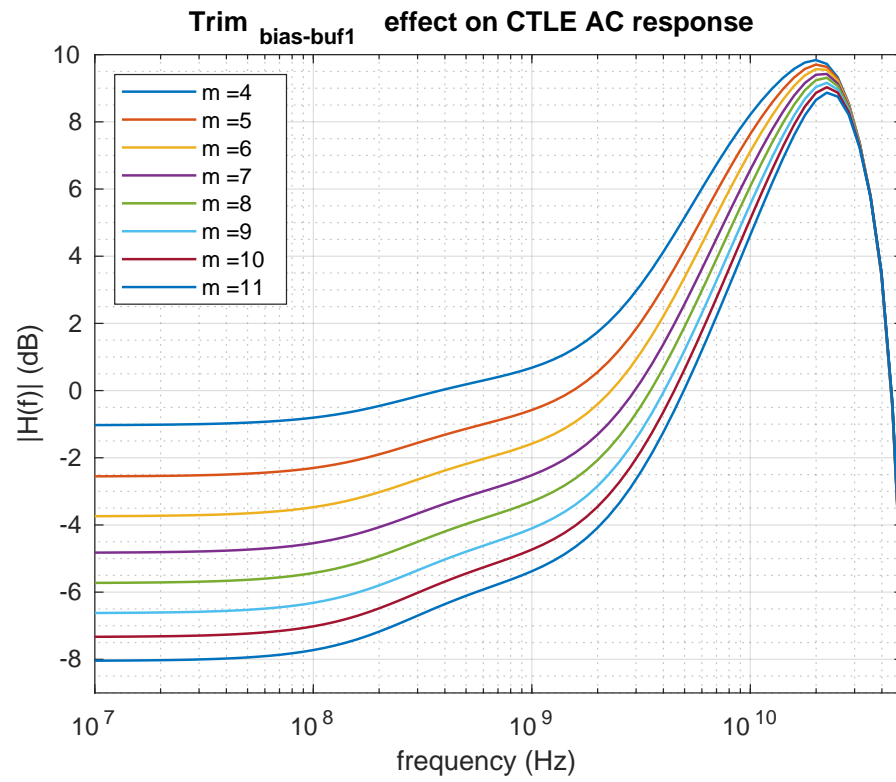

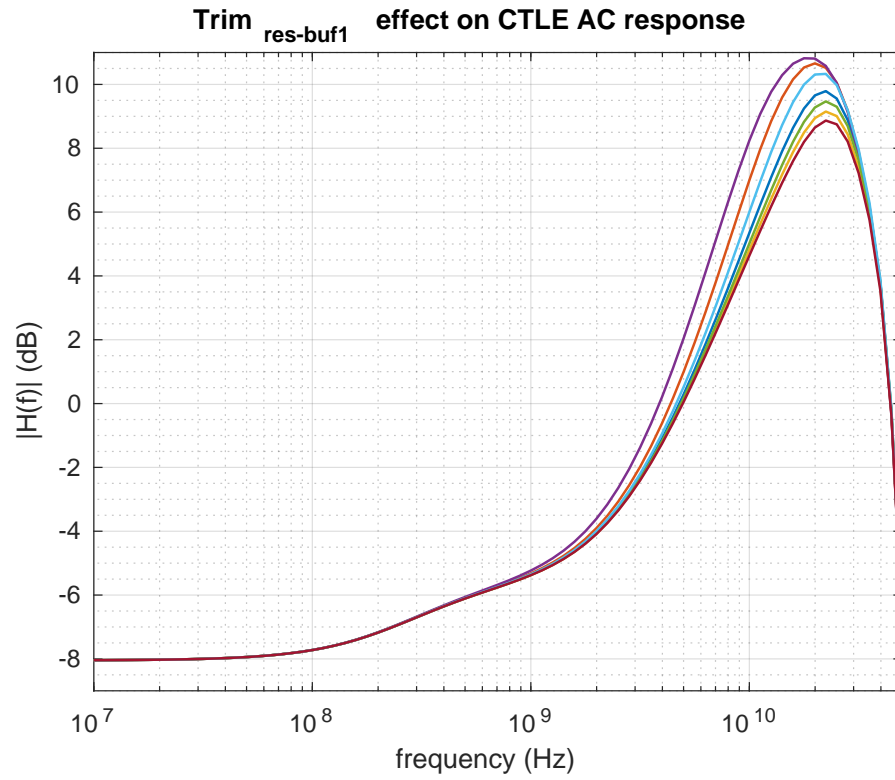**Figure 5.8:** $Trim_{bias-buf1}$ effect on the CTLE transfer function.

Figure 5.9: $Trim_{res-buf1}$ effect on the CTLE transfer function.

Figure 5.10: $Trim_{mf}$ effect on the CTLE transfer function.
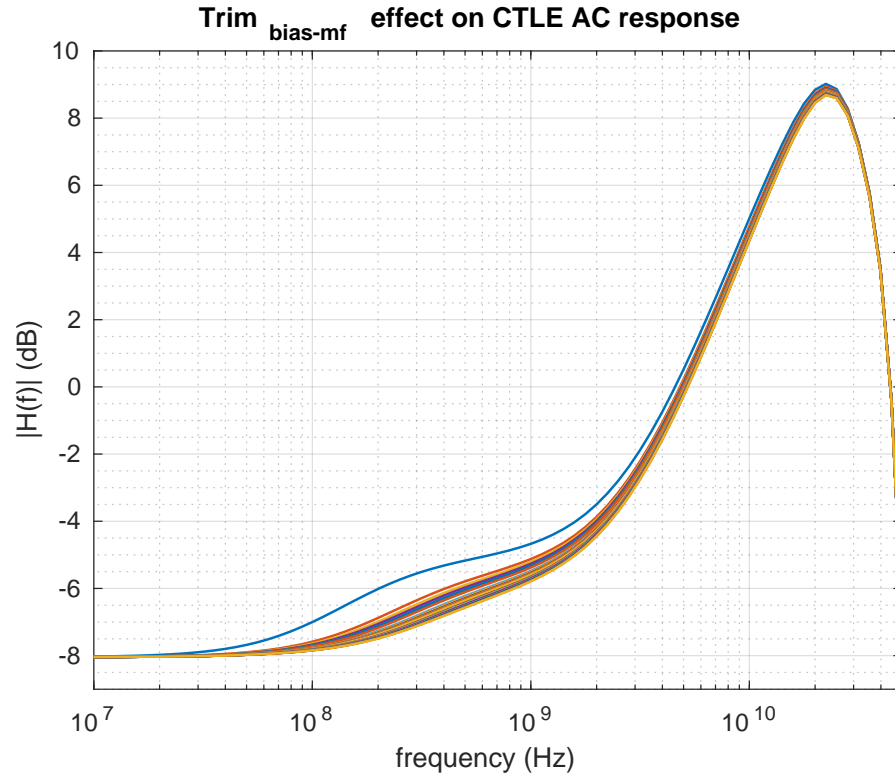
Figure 5.11: $Trim_{bias-mf}$ effect on the CTLE transfer function.
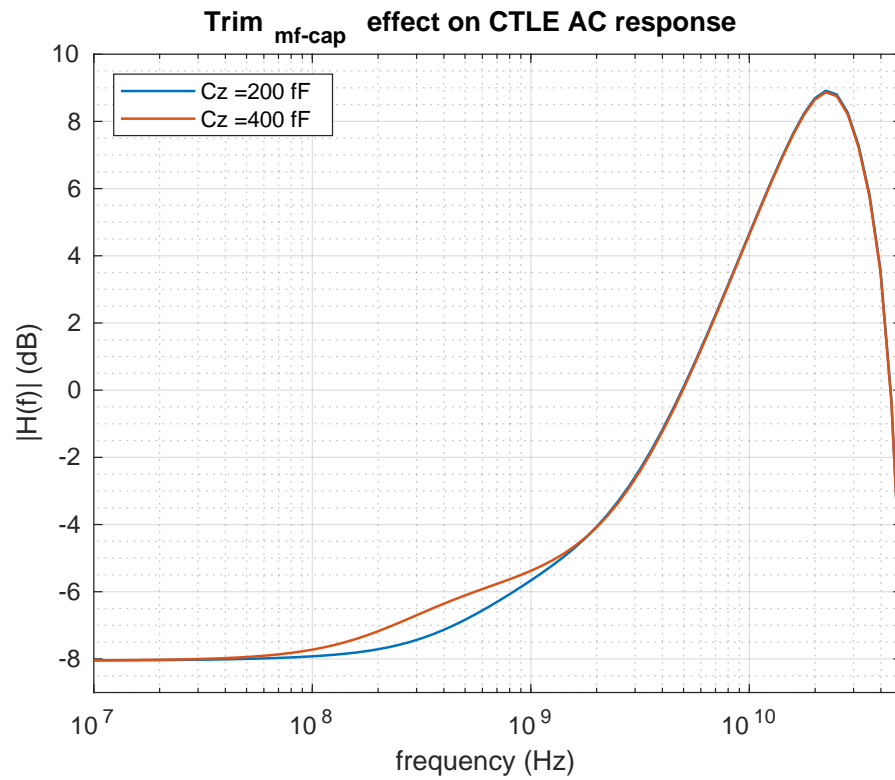
Figure 5.12: $Trim_{mfcap}$ effect on the CTLE transfer function.
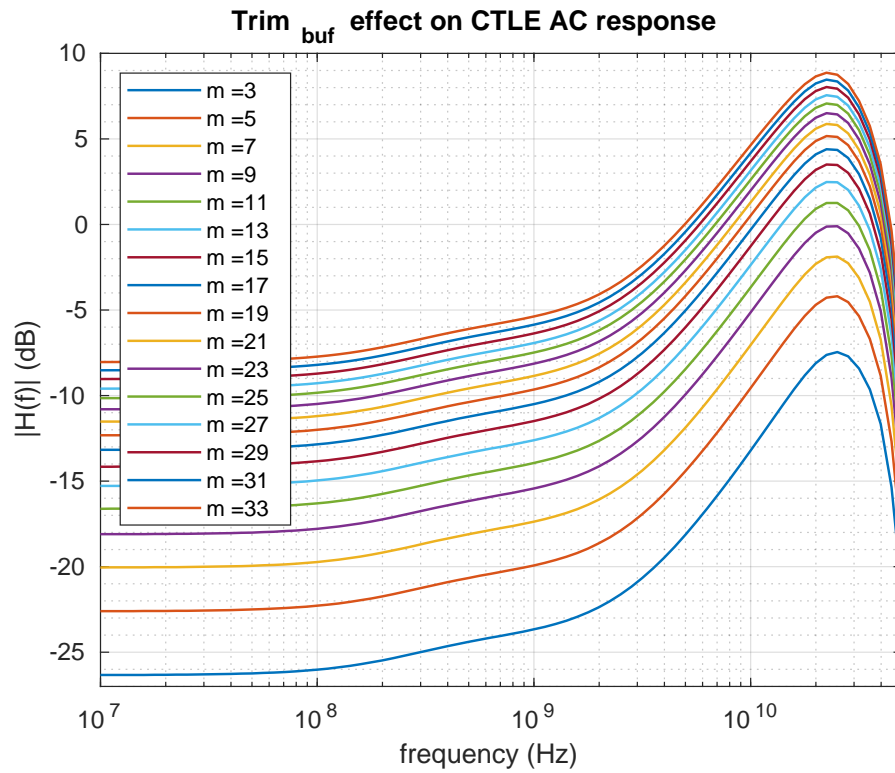
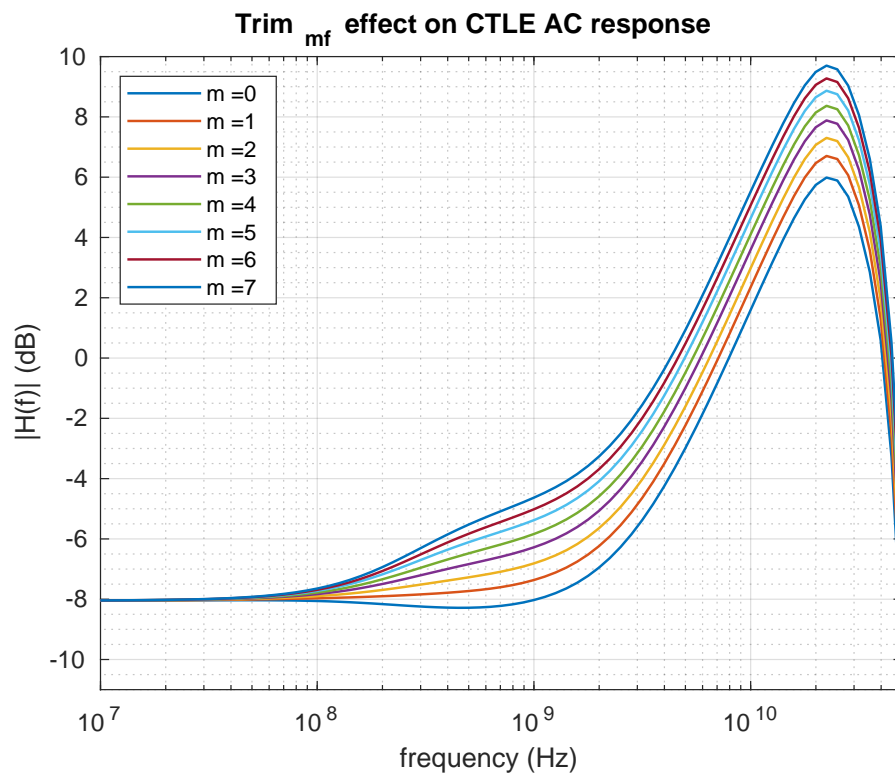**Figure 5.13:** $Trim_{buf}$ effect on the CTLE transfer function.

Impact of MF-CTLE on the eye-diagram
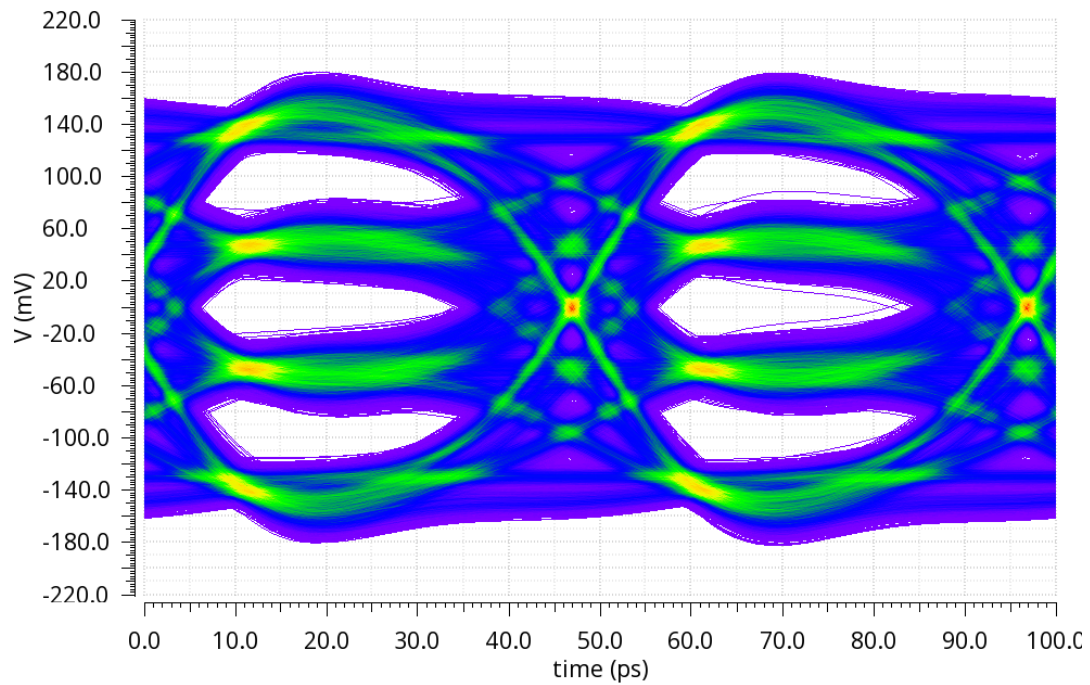
Figure 5.14: Eye diagram at the output of HF-CTLE (inverter based) for 40 Gbps PAM-4 data rate.

Figure 5.15: Eye diagram at the output of MF-CTLE (inverter based) for 40 Gbps PAM-4 data rate.
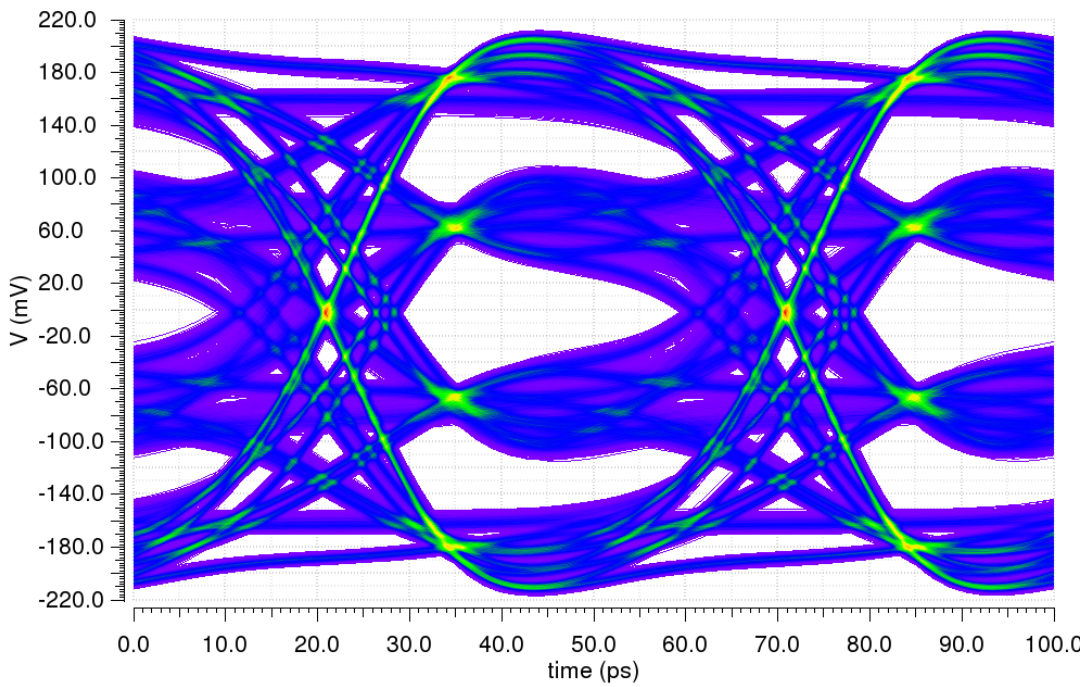
Figure 5.16: Eye diagram at the output of complete CTLE (inverter based) for 40 Gbps PAM-4 data rate.

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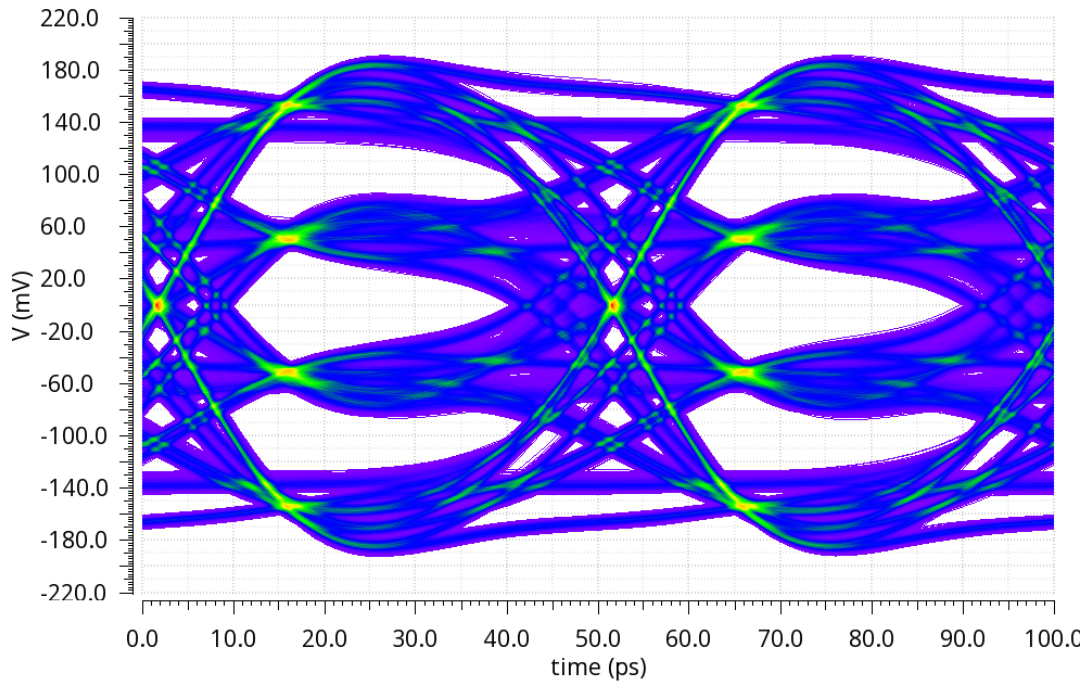
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