Basic and advanced current references

Afshin Haft-Baradaran
University of Toronto
E-mail: afshinhf@eecg.utoronto.ca

Abstract:

Two main reasons for variation of current output of current source are temperature dependency and process dependency of output current. Therefore in current references we try to compensate these two major factors. This paper reviews some important current reference in bipolar and CMOS technolgy

I. Introduction

The current-mode approach in circuit design is becoming more common, because circuits designed using this approach will always work at higher speed, for a given technology, than its voltage-mode counterpart. Therefore many systems could take advantage of current-mode technology over a wide field of applications like switched-current filters and current-feedback operational amplifiers.

Also current reference is a basic building block in analog circuits as a bias source for oscillators, amplifiers, PLL's and etc. All mentioned applications make extensive use of current references and their accuracy is strongly related to the temperature and process stability of these references. In the voltage mode we can implement a bandgap circuit to ensure correct biasing over a wide temperature range, but in the current mode it is much more difficult to obtain this level of performance. This review paper describe some basic and advanced current references in bipolar and CMOS technology, also in low-voltage low-power design.

II. Bipolar Technology

Several current references have been proposed previously[1,13,14]. The building blocks of these circuits is the reference current which is obtaining by forcing, across an integrated resistor, a built in reference voltage such as the base-emitter voltage of bipolar transistor or the difference between the base-emitter voltage of two transistors.

II.A. PTAT current Reference

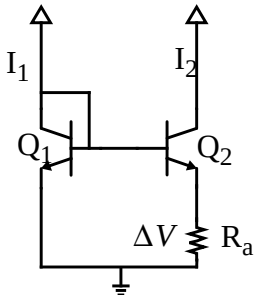


Figure (1). PTAT current source

This circuit is shown in figure (1). It can be shown that [2] the output current I_2 has the following relation with temperature:

$$I_2 \approx \frac{V_T ln\left(\frac{A_1}{A_2}\right)}{R_a} = \frac{KT}{q} \cdot \frac{ln\left(\frac{A_1}{A_2}\right)}{R_a} \tag{1}$$

and therefore:

$$\frac{dI_2}{dT} = \frac{K \ln\left(\frac{A_1}{A_2}\right)}{qR_a} = C \tag{2}$$

and C is clearly a positive constant. This current is generally called proportional to absolute temperature, PTAT. It can easily be demonstrated that the temperature dependence of R_a introduce second order effect, negligible in the normal range of temperature.

II.B. Inverse PTAT current reference

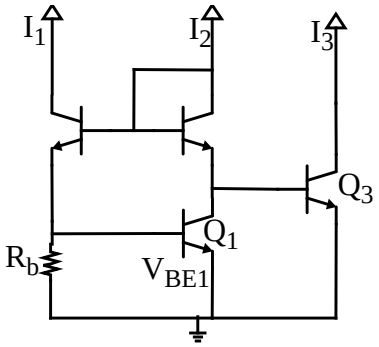


Figure (2). Inverse PTAT current source

It can be shown that in this circuit which has been shown in figure (2)[2]:

$$I_3 \approx \frac{V_{BE_1}}{R_b} \tag{3}$$

Also:

$$V_{BE_1} = V_{G_0} - V_T(\gamma - \alpha)\ln(T) - V_T \ln(EG)) \tag{4}$$

where γ, α, E, G are independent of T, therefore:

$$\frac{dI_3}{dT} = \frac{1}{R_b T}[V_{BE_1} - V_{G_0} - V_T(\gamma - \alpha)] = \frac{1}{R_b T}F(T) \tag{5}$$

Although variation of I_3 is not a constant with regards to the temperature, it is always negative.

So it can be used to compensate the PTAT current source positive dependence.

We can add two previous currents and total current I_c can be temperature independence.

$$\frac{dI_c}{dT} = \frac{dI_1}{dT} + \frac{dI_2}{dT} = C + \frac{F(T)}{R_b T} \tag{6}$$

solving $\left.\frac{dI_c}{dT}\right|_{T = T_0} = 0$, we have $F(T)=-CR_bT_0$, or:

$$V_{BE_1} = V_{G_0} + V_T(\gamma - \alpha) - \frac{R_b}{R_a} V_{T_0} \ln\left(\frac{A_1}{A_2}\right) \tag{7}$$

Equation (7) depends on a resistor ratio, which implies good reproducibility and temperature stability in microelectronic design. One circuit was proposed based on this idea in [2].

Figure (3) shows a temperature regulation of less than 3% over 0-80° C..

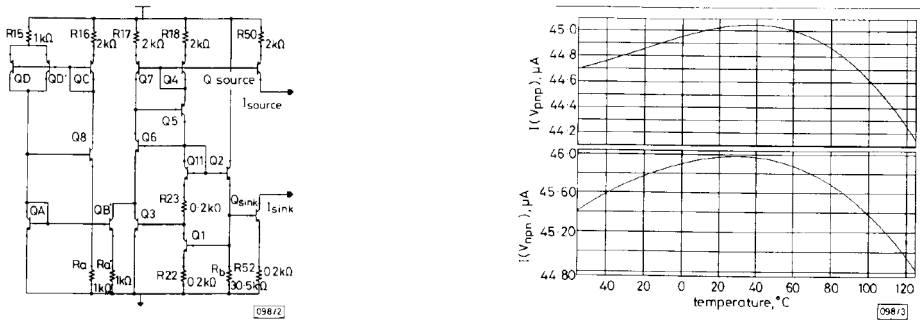


Figure (3). Ratiometric temperature stable current reference [2]

III. CMOS Technology

Because current reference in CMOS technology has received little attention in the literature we try to consider these circuits. We review the ideas in bipolar current references. Their principles relies on the fact that the voltage V_{BE} across a p-n junction that is forward biasing by a constant current increases fairly linearly with decreasing temperature. This voltage across resistor results in current which increases with decreasing temperature (Inverse PTAT). If a current that is proportional to absolute temperature (PTAT) is added to that current, one obtains a current reference that is independent of temperature.

But in MOS transistors, the temperature dependence of the drain current originates mainly from its mobility dependence on temperature. To compensate this mobility dependency, bipolar PTAT or MOS PTAT source have been used.

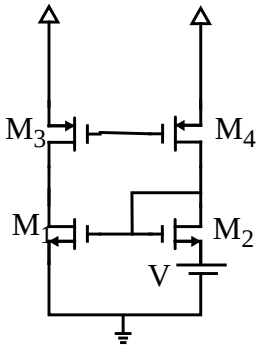
III. A. CMOS temperature-compensated current reference

The principle of this circuit is shown in figure (4). In this circuit, the current through M_1 is given by [3]:

$$I = \mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_1 \cdot \frac{(V + V_{th_2} - V_{th_1})^2}{(1 - \sqrt{m})^2} = \beta_1 \frac{(V + V_{th_2} - V_{th_1})^2}{(1 - \sqrt{m})^2} \quad (8)$$

and $m = \dfrac{\beta_1 \beta_3}{\beta_2 \beta_4}$ and $\beta = \mu C_{ox}\left(\dfrac{W}{L}\right)$.

we know that temperature dependence of μ_n of a MOS transistor is $T^{-1.5}$. By using a PTAT voltage source for V, a current is obtained which is proportional to $T^{.5}$ and therefore slightly increase with temperature. A PTAT voltage source is usually obtained by using vertical bipolar devices as depicted in figure (5).



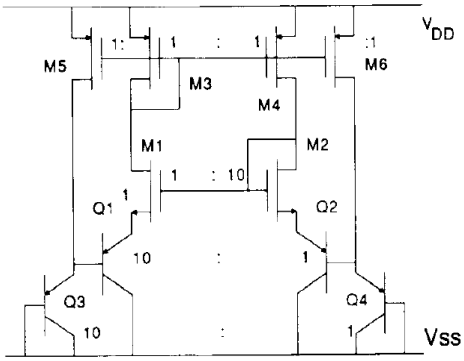


Figure (4). Principle of the current reference **Figure (5). Current ref. with PTAT voltage source [3]**

But for economic reasons, analog circuits must be realized without additional steps in process for bipolar transistors. Realization of PTAT and inverse PTAT in CMOS technology is difficult. Solution of this problem may be found by considering in weak inversion [4].

III.B. PTAT circuits in CMOS technology

III.B.1. PTAT CMOS circuit using resistor

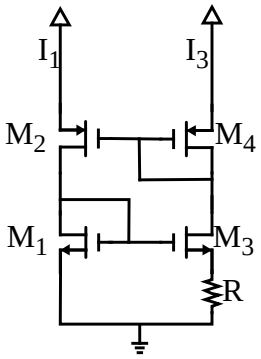


Figure (6). CMOS PTAT current source

A circuit which uses MOSFET's only and one resistor is shown in fig (6). P-channel MOSFET's M_2 and M_4 act as a current mirror and are in strong inversion and M_1 and M_3 are in weak inversion region. Therefore for M_3[4]:

$$I_3 = \mu_n C_{ox}\left(\frac{W}{L}\right)_3 J_{D_0} e^{\frac{V_{G_1}}{nV_T}}\left(e^{\frac{-V_{S_3}}{V_T}} - e^{\frac{-V_{D_3}}{V_T}}\right) = \beta_3 J_{D_0} e^{\frac{V_{G_1}}{nV_T}}\left(e^{\frac{-V_{S_3}}{V_T}} - e^{\frac{-V_{D_3}}{V_T}}\right) \tag{9}$$

if $V_{ds3} >> V_T$:

$$I_3 = \mu_n C_{ox}\left(\frac{W}{L}\right)_3 J_{D_0} e^{\frac{V_{G_1}}{nV_T}} e^{\frac{-V_{S_3}}{V_T}}\left(1 - e^{\frac{-V_{DS_3}}{V_T}}\right) \approx \beta_3 J_{D_0} e^{\frac{V_{G_1}}{nV_T}} e^{\frac{-V_{S_3}}{V_T}} \tag{10}$$

also for M_1:

$$I_1 = \beta_1 J_{D_0} e^{\frac{V_{G_1}}{nV_T}} \tag{11}$$

But $I_3 = I_4, I_1 = I_2$, therefore:

$$V_R = V_T \ln\left(\frac{\beta_3 \beta_2}{\beta_1 \beta}\right) \tag{12}$$

III.B.2. PTAT CMOS circuit without using resistor

The presence of a resistor is a drawback for some application. If a low current is required, a high value resistor needed, which takes along surface area if it is made with drain diffusion or high doped polysilicon. The resistivity is not guaranteed by some foundries with technology. Also temperature coefficient of resistor is not well defined and does not compensate for the temperature dependence of V_R.

The basic cell of PTAT voltage source wothout resistor is shown in fig (7). The two transistors M_1 and M_2 are in weak inversion therefore[5]:

$$V_0 = V_T \ln\left(1 + \frac{\beta_2}{\beta_1}\right) \tag{13}$$

values of V_o practically obtainable with this cell are limited to about 100 mv. Higher values may be obtained by stacking a certain number of cells.

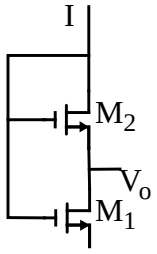


Figure (7). CMOS PTAT current source without resistor

III.C. All CMOS temperature compensated current reference

We can return to circuit section (III.A) with using mentioned PTAT circuit which shown in figure (7). In practical realization of figure (8)[3] M_{28}-M_{37} form a PTAT voltage source composed of a series of five cells.

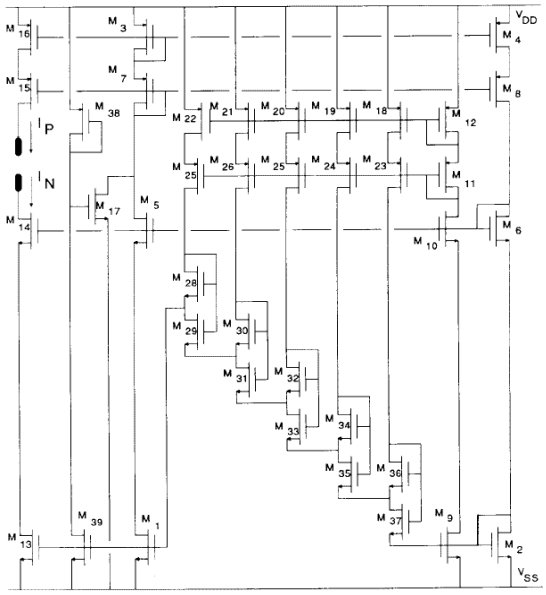


Figure (8). All CMOS temperature-compensated current reference[3]

In this figure the transistors M_1-M_4 form the reference circuit and M_{28}-M_{37} form the voltage source. The currents through the PTAT voltage source are derived from the reference current through M_9, M_{12} and M_{18}-M_{22}. The current reference is available from the terminals I_N and I_P through M_{13}-M_{16}. To obtain low supply and load regulation sensitivities cascode transistors are added to every current mirror. Start-up network formed by M_{17} and M_{38} and M_{39} is added to avoid latch-up state due to leakage current. Results shows that the temperature dependence of the current output is less than 3% between 0 and 80 $^\circ$C . This is caused by the overcompensation of the temperature dependence of channel mobility and from nonideal behavior of the PTAT voltage source.

III.D. All CMOS temperature independent current reference

Although mentioned circuits have low temperature dependence, it can not completely elimi-

nate the mobility dependence or its temperature dependence. The mobility dependence term can completely cancelled out in the output current by multiplying a current component which is proportional to mobility and a current component which is inversely proportional to mobility with a CMOS square root circuit as shown in fig(9)[6].

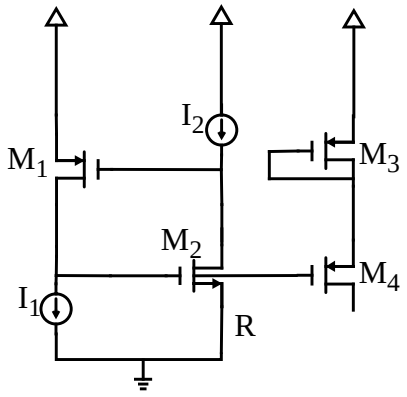


Figure (8). CMOS current reference using square root circuit[6]

The CMOS square root circuit was derived from its bipolar counterpart and it consist of four PMOS transistor M_1-M_4 which operating in weak inversion region. Because $V_{GS1}+V_{GS2}=V_{GS3}+V_{GS4}$, the output current I_o can be derived as follows:

$$I_o = \sqrt{m_1}\sqrt{I_1}\sqrt{I_2} \tag{14}$$

where: $m_1 = \dfrac{\beta_3\beta_4}{\beta_1\beta_2}$

figure (10) shows a complete circuit schematic of the CMOS current reference circuit [6] using this idea. The eight transistors M_5-M_{12} generate the current component I_1 which is proportional to mobility. The seven transistors M_{13}-M_{19} and the resistor R generate the current component I_2 which is inversely proportional to mobility. The four PMOS transistors M_1-M_4 used in the square root circuit are operating in the weak inversion region and all the others in figure are operating in strong inversion saturation region. An ordinary current mirror circuit M_5 and M_8 generates I_5 such

that[6]:

$$I_5 = \frac{\beta_5 (V_{DD} - 3|V_{tp}|)^2}{2(1 + 2\sqrt{m_2})^2} \tag{15}$$

where $m_2 = \frac{\beta_5}{\beta_6}$. Also since voltage drop across the resistor R is equal to the potential difference between the source nodes of M_{16} and M_{18}, I_{16} can be derived as follows by using the strong inversion current equation[6]:

$$I_{16} = \frac{2(1 - \sqrt{m_3})^2}{R^2 \beta_{18}} \tag{16}$$

where $m_3 = \frac{\beta_{18}}{\beta_{16}}$. The current component I_1 and I_2 can be obtained easily from I_5 and I_{16} by multiplying the transistor size ratios of the cascoded current mirror circuit (M_9-M_{12}) and the simple current mirror circuit (M_{13}-M_{15}, M_{17}). Hence the final output current I_o can be derived as:

$$I_o = \frac{1 - \sqrt{m_3}}{1 + 2\sqrt{m_2}} \sqrt{m_1}\sqrt{m_4} \cdot \frac{(V_{DD} - 3|V_{tp}|)}{R} \tag{17}$$

where $m_4 = \frac{\beta_5 \beta_{10} \beta_{13} \beta_{15}}{\beta_9 \beta_{14} \beta_{17} \beta_{18}}$. As shown in this equation the mobility dependence terms are completely cancelled out in I_o if we assume the mobility of the same devices is the same for all the transistors in the circuit. The temperature dependence of I_o comes from temperature dependences of V_{tp} and R. These parameters tend to cancel each other since diffusion resistor R and the PMOS threshold voltage have positive and negative temperature coefficient respectively. Results shows 1.7% variation for a temperature range 0-75 °C.

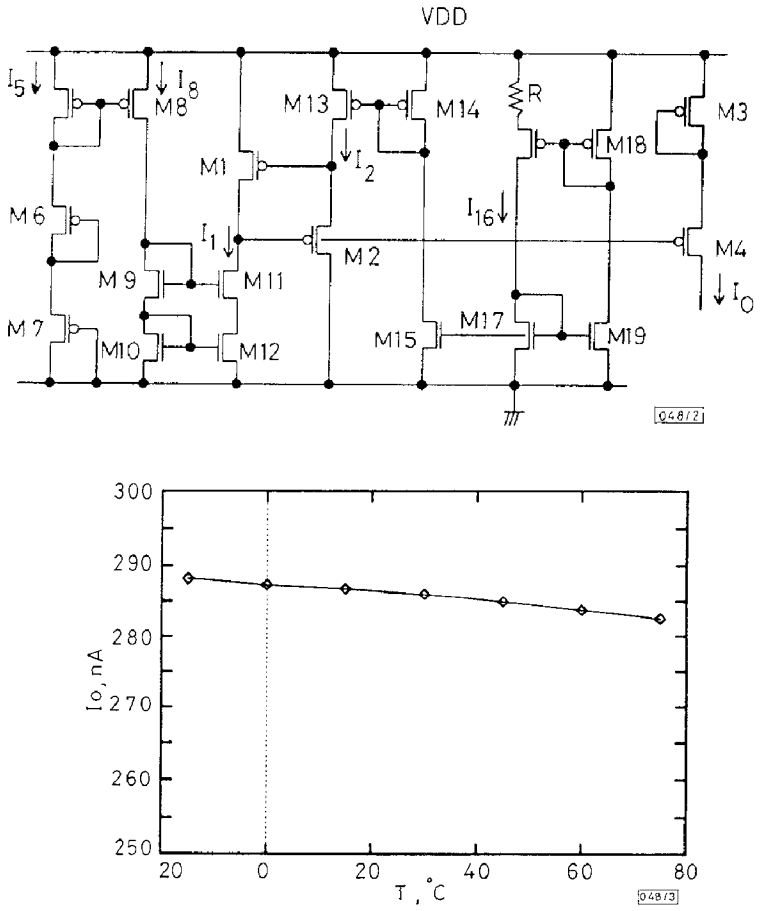


Figure (10). Circuit diagram of CMOS current reference and measured output current[6]

III.E. Switched capacitor CMOS current reference

In current reference circuits have been proposed previously the value of generated current depends on physical parameters such as MOS transistor threshold voltage and conduction factor, sheet resistance of resistor layer and etc. which display wide dispersion range in production. The switched capacitor technique allows resistor equivalent structure to be realized where the resistance value is determined by the value of a capacitor and the switching frequency[7,8]. The integrated capacitor per unit area shows typical dispersion in the range of 20% and is independent of temperature[9]. The operating principle of an SC-based current reference is shown in figure (11)

where I_o is reference current generated.

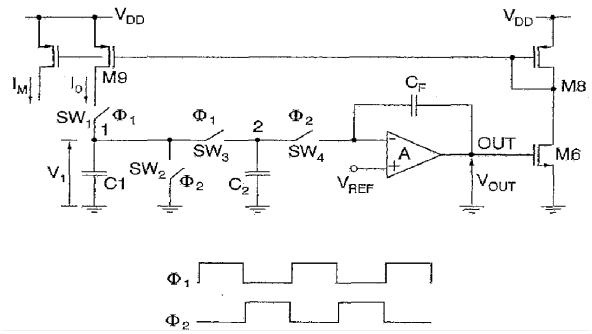


Figure (11). Principle of SC based current reference[10]

It can be shown that [10]:

$$I_o = \frac{C_1 V_{ref}}{T_{\phi_1}} \tag{18}$$

Therefore the value of I_o depends on an on-chip capacitor, a constant voltage reference and time interval derived from a crystal-controlled oscillator. This circuit has a limited temperature dependency because an integrated capacitor has the temperature coefficient in the range of a few tens of ppm/°C [9]. Figure (12) shows the circuit schematic of a complete current reference. results show 3% spread when measuring 25 samples demonstrating effectiveness of the discussed approach.

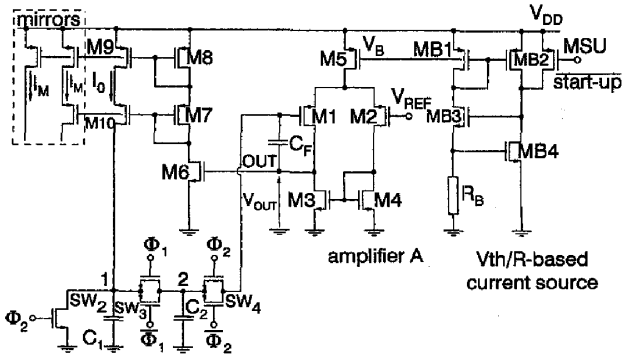


Figure (12). Circuit diagram of SC-based current reference [10]

IV. Low voltage Low-power design

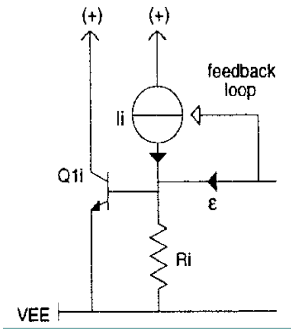
The advent of portable electronics yields an important increase in low-voltage low-power circuits demand. Also improvement of microelectronic process lead to reduction of component dimension and therefore a need for low supply voltage. But some mentioned circuits can not operate in low-voltage case. For example inverse PTAT part of circuit section (II.B) can not operate with lower 1 volt power supply. Because generally 1-volt power supply only allows the sum of a single base-emitter voltage and two collector-emitter voltages. Therefore changing in inverse PTAT circuit is required for operating with low-voltage power supply.

IV.A. Low-voltage bipolar current reference

The principle of the idea shown in figure (13). the current flowing R_i is the sum of I_i and ε. Because Ii is controlled by ε with a high current gain feedback, therefore ε is negligible. Then we have:

$$I_i = \frac{V_{BE_{Q1i}}}{R_i} \tag{19}$$

Complete schematic of the inverse PTAT circuit is shown in figure (14)



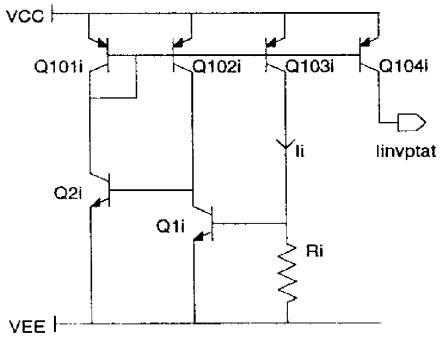


Figure (13). Principle of modified inverse PTAT Figure (14). Low-voltage inverse PTAT circuit[11]

In this circuit there are not more than one base-emitter voltage and one collector-emitter voltage.This topology can be used with power supply lower 1 volt.

One complete 1-volt ratiometric temperature stable current reference is shown in figure (15)[11]. Experimental results in figure (16) show temperature coefficient about 250 ppm/°C. This circuit can work with power 875 mv power supply.

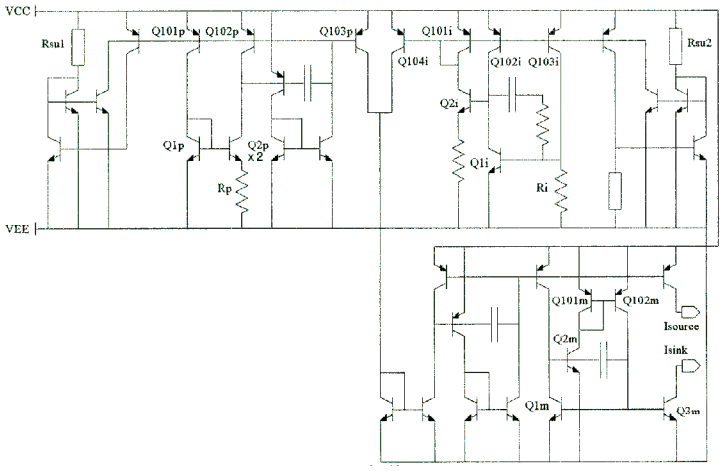


Figure (15). Circuit diagram of low-voltage current reference[11]

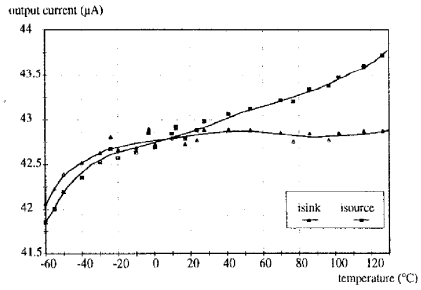


Figure (16). Result of output current of low-voltage current reference[11]

IV.B. Low voltage CMOS current reference

CMOS current references which previously presented can not work in low voltage power supply. For example minimum power supply for circuit section (III.C) is 3.5 v [3] and for circuit sec-

tion (III.D) is $3|V_{tp}|$. One low-voltage current reference which has been proposed [12] uses PTAT circuit section (III.B.1), but resistor R has been replace with n-channel MOSFET work in triode region. It has shown that [12] temperature dependence of output current is $T^{.5}$. Also it can work with power supply as low as 1.2 v and produce 1-100 nA output current.

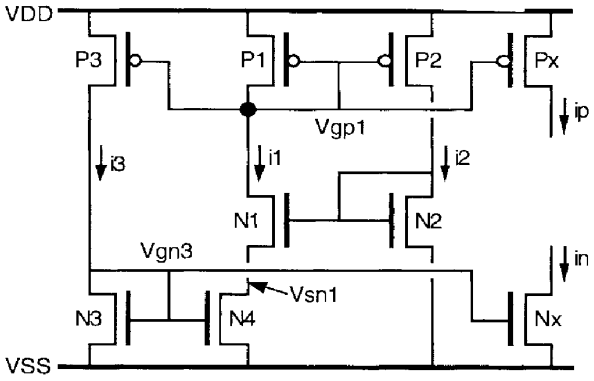


Figure (17). Low-voltage CMOS current reference[12]

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