Low Jitter Phase-Locked Loop

Jonathan Cheung

Abstract

For high speed application, jitter is a problem to communication system, as it reduces the performance of overall circuitry. As jitter is a type of corruption that cannot be eliminated, reducing jitter is one way to help to improve the system performance. In this paper, we introduce some ways to reduce the jitter in phase-locked loop.

Introduction

Phase-Locked Loop, PLL, is widely used among the electronics and communication systems, for clock and data recovery, frequency synthesis, clock synchronization in microprocessors, and many applications. In high speed application, Gbit/s range, data rates increase, data eye opening becomes narrower. The received data and clock therefore become more susceptible to various noise sources, of which supply and substrate noise are the most dominant. It is important, therefore, to design a low jitter PLL, that is highly tolerant of supply and substrate noise, enabling jitter reduction.

Signals often experience timing jitter as they travel through a communication channel or as they are retrieved from a storage medium. Jitter manifests itself as variation of the period of a waveform, a type of corruption that cannot be removed by amplification and clipping [1]. While jitter represents the time-domain description, phase noise is the corresponding frequency-domain equivalent of the same physical effect. In typical applications, jitter requirements range from on the order of 100 picoseconds r.m.s. down

to less than 5 picoseconds in very high speed communications receivers, for instance. Jitter can arise from many sources, including noise from other parts of the circuit through the power supply. This kind of noise can often be minimized by the use of differential circuit technique, shown in previous research.

In this paper, we discuss the methods to reduce the jitter in PLL. Since VCO is the major source of jitter in the PLL system, we will show some new ways to minimize the jitter in VCO. The new layout technique for VCO and circuits for reducing jitter are presented in the following sections.

Background

Basic Topology of Phase-Locked Loop

PLL simply consists of a phase detector (PD), low-pass filter (LPF), and voltage-controlled oscillator (VCO) in a feedback loop, Fig. 1. The PD compares the phases of Vout and Vin, generating an error signal that varies the VCO frequency until the phases are aligned, that is the loop is locked. The low-pass filter is used to extract the average value from the output of the phase detector. This average value is used to drive the VCO. The output of the VCO is synchronized with the input signal, by the negative feedback loop.

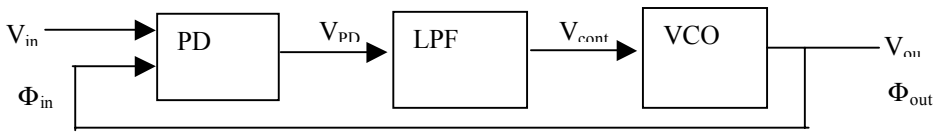

Fig. 1 Basic architecture of a phase-locked loop.

A) Phase detector (PD)

The phase detector compare the phase of input signal and output of VCO, and generate an average output , $\overline{Vout}$ which is linearly proportional to the phase difference, ΔΦ, between its two inputs. In the ideal case, the relationship between and ΔΦ, is linear, crossing the origin for ΔΦ = 0. [3]

The simplest example of phase detector is an exclusive OR, XOR gate. The width of the output pulses varies with the phase difference between the inputs that providing a dc level proportional to ΔΦ. The error pulses on both rising and falling edges can be produced by the XOR circuit, but other types of PD only respond to positive or negative transitions.

B) Voltage-controlled oscillator (VCO)

Voltage-controlled oscillator (VCO) is simply an oscillator whose frequency is proportional to a control voltage, V_{cont}, with a function:

$$\omega_{out} = \omega_{FR} + K_{VCO} V_{cont}$$

where ω_{FR} is the "free-running" frequency and K_{VCO} is the "gain" of the VCO (rad/s/V). The output of a sinusoidal VCO can be expressed as

$$y(t) = A\cos(\omega_{FR} t + K_{VCO} \int_{-\infty}^{t} V_{cont}\, dt)$$

so the phase is the time integral of frequency. In practical VCOs, Kvco exhibits some dependence on the control voltage and eventually drops to zero as V_{cont} increases. If $V_{cont}(t) = V_m \cos \omega_m t$, then

$$y(t) = A\cos(\omega_{FR} t + \frac{K_{VCO}}{\omega_m} V_m \sin\omega_m t)$$

As VCO can be consider as a linear time-invariant system, with the control voltage as the system's input and the excess phase of the output signal as the system's output.

$$\Phi_{out}(t) = K_{VCO}\int V_{cont}\,dt$$

The transfer function is

$$\frac{\Phi_{out}(s)}{V_{cont}(s)} = \frac{K_{VCO}}{s}$$

To change the output phase, we need to change the frequency and then integration. For example, in Fig.2, suppose for $t < t_o$, a VCO oscillates at the same frequency as a reference but with a finite phase error. To reduce the error, the control voltage, V_{cont}, is stepped by $+\Delta V$ at $t = t_o$, thereby increasing the VCO frequency and allowing the output to accumulate phase faster than the reference. At $t= t_1$, V_{cont} returns to its initial value, as the phase error has decreased to zero. The two signals have equal frequencies and zero phase difference.

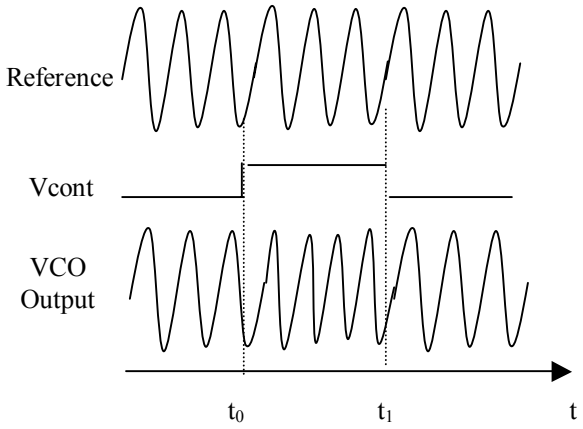

Fig.2 Phase alignment of a VCO with a reference

In locked condition, all the signals in the loop have reached a steady state. An output, dc value is proportional to $\Delta\Phi$, is produced by phase detector. The low-pass filter suppresses high-frequency components in the PD output, allowing the dc value to control the VCO frequency. The VCO then oscillates at a frequency equal to the input frequency and with a phase difference equal to $\Delta\Phi$.

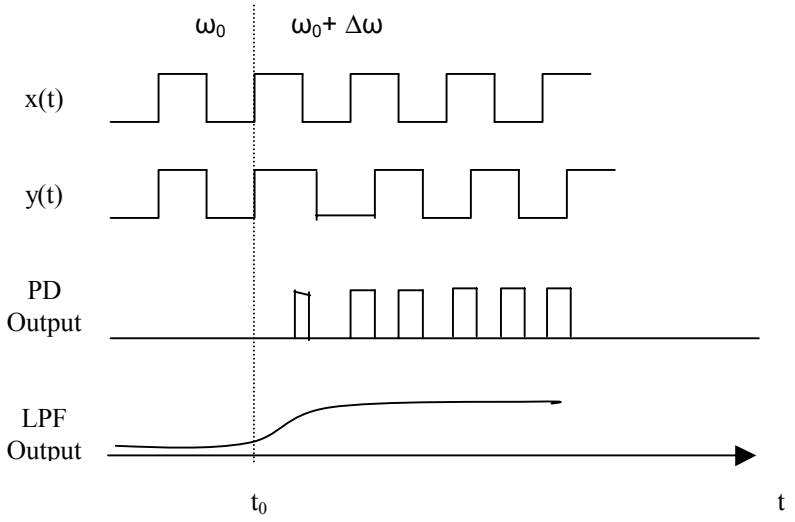

Fig.3 Response of a PLL to a small frequency step

There are many different types of oscillators. Two major classifications, sinusoidal output and square (or triangular) wave output oscillators. Sinusoidal-output oscillators are usually realized using some kind of frequency-selective or tuned circuit in a feedback configuration, while square-wave-output oscillators are usually realized using a nonlinear feedback circuit such as a ring or relaxation oscillator.

(C) Charge Pump Phase Comparator

PLL with charge-pump phase comparator do not exhibit false lock. The input-signal and oscillator-output waveforms are exactly in phase when the system is in lock, even when the input frequency and free-running frequency are different. In Fig. 4, shows a charge-pump phase comparator. This kind of phase comparator either injects, subtracts, or leaves alone the charge stored across a capacitor in the low-pass filter, depending on the output of phase-detector circuit. When S1 is closed, Ich flows into the low-pass filter, increasing the control voltage into the VCO; when S2 is closed, Ich flows out the low-pass filter, decreasing the control voltage of the VCO. The top plate of C1 is open circuited and the output voltage remains constant in the steady state, when both switches are open.

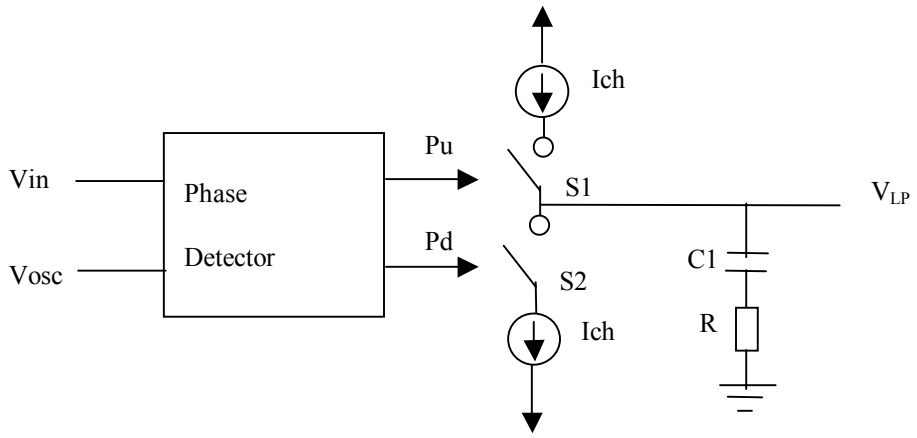

Fig. 4 Charge-pump phase comparator

<u>Technique for reducing jitter</u>

(A) New VCO Layout

VCO is the major jitter contributor to the overall system, some special techniques needed to minimize the jitter. One source of jitter in the VCO comes from mismatch

among the loads of the delay lines. Traditionally, a delay line is laid out as shown in Fig.5a where the VCO's cells are arranged in ascending or descending order and the output of a certain delay cell goes to the input of the next delay cell, except for the last delay cell in the line whose output goes to the input of the first delay cell. From Fig. 5a we can see that the length of the signal path between any two consecutive cells is the same, except between cell 1 and cell 10, which is 10 times longer than the rest. The new proposed VCO layout, which shown in Fig. 5b has more uniform signal path among the cells and hence will have less mismatch. Assuming that the x dimension is much larger than the y dimension in the wire routing, (which is the case in our proposed design), Fig.5a shows a mismatch ratio of 10:1, while Fig 5b shows a mismatch ratio of 2:1. [5]

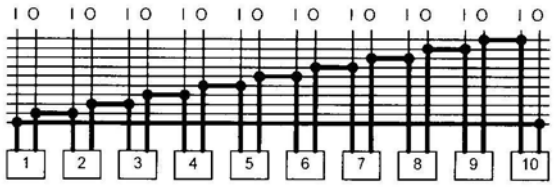

Fig.5a Traditional VCO layout

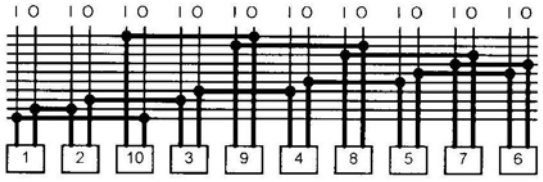

Fig. 5b New VCO layout

(B) New delay element circuit for VCO

Besides, new approach of layout technique, the circuit design of VCO can also reduce the jitter. A novel delay element is proposed to minimize the supply/substrate

noise, as VCO is sensitive to this noise. In Fig. 6, a schematic diagram of the pseudo-differential delay element with an auxiliary circuit is shown. Ten transistors, M6-M15, constitute the core circuit while the other transistors constitute the auxiliary circuit. The loop filter output node of the PLL is Vcb, and M6-M9 serve as a current mirror controlled by Vcb. One CMOS inverter composed of M10 and M11 and another inverter composed of M12 and M13 are coupled to each other by a positive feedback circuit (M14 and M15). Thus, two single-ended inverters behave like one differential delay element. This pseudo-differential delay element benefits from both single-ended and differential delay elements. This single-ended delay elements provide full-swing outputs without the need for additional buffers. The number of delay elements is only half that of the required phases, which is the virtue of differential delay elements. The power consumption of the VCO is substantially reduced. Moreover, this compact and feasible circuit behaves as a differential circuit, and is thus immune to supply and substrate noise in itself. [4]

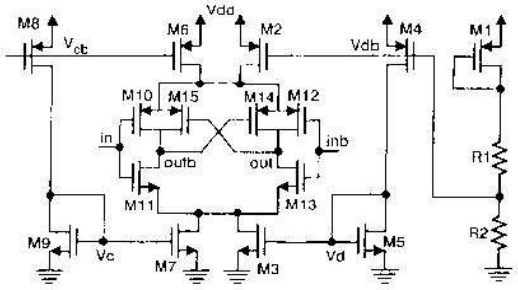

Fig. 6 Pseudo differential delay element with auxiliary circuit

(C) Power Supply Noise Reduction

A decoupling capacitor structure can be used to reduce the power supply noise that caused by both on-chip capacitance and power supply inductance. An array of NMOS capacitors in parallel can be used for decoupling. They were placed under the power buses to avoid occupying any extra space. Research found that before adding the decoupling capacitors structure, it shows a noise of 200mV on the power supply. After adding the decoupling capacitors, the noise range reduced to less than 20mV.

Future Challenge

As the speed of communication system becomes higher and higher, the effect of jitter to the circuitry is also increasing. So more advanced technology in reducing jitter in phase-locked loop or designing a jitter free phase-locked loop is highly needed. On the other hand, designers are facing challenge to design a higher tolerant phase-locked loop and other systems, so that they can resist higher amount of jitter.

Conclusion

Some reducing jitter method for PLL has been presented. New VCO layout minimizes the mismatch among the loads of the VCO delay lines. The PLL employs a VCO based on pseudo-differential delay elements, incorporating the merits of both single-ended and differential-type VCOs. This kind of circuit gives PLL inherent low-jitter performance that can be used in high-speed link interfaces. In addition, power supply noise, one of the noise source to PLL, can be reduced by a decoupling capacitor structure.

Since jitter is a type of corruption that cannot be removed, new technique to further reduce jitter is required in the future. Also, designing PLL with higher tolerance of jitter is needed, as the speed of communication or circuits keep increasing.

Reference

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