ECE1352F – Analog Circuit Design I

Term Paper: CMOS Variable Gain Amplifier (VGA)

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by
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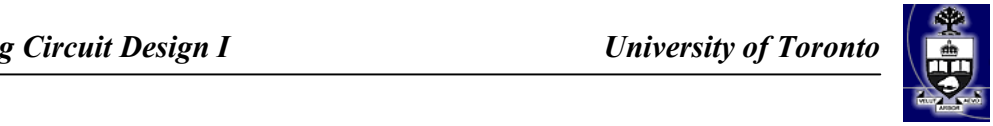
Abstract

The basic background of variable gain amplifiers (VGAs) and their recent developments in RF communication systems are discussed in this paper. Several common circuit topologies are studied. The focus is on CMOS techonologies for high integration processes such as System-on-Chip (SOC). Finally, it can be concluded that the future main research areas for CMOS VGAs are (1) finding new approximations to the exponential relationship between gain and controlling signal, (2) digitalized gain control algorithm, and (3) higher bandwidth product.

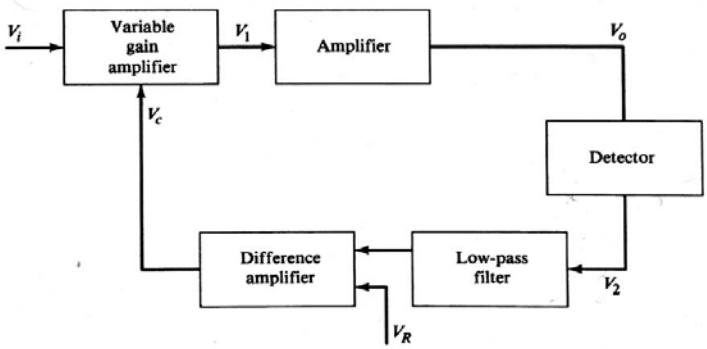
INTRODUCTION

Over the past few years, there have been dramatic developments in the fields of wireless communication due to the increasing demand for information exchange. As a result, this has become one of the major driving forces for Radio-frequency (RF) IC engineers to incorporate designs with wide dynamic range, high integration at low cost as well as minimal power consumption.

One of the many design challenges faced by communication engineers is the maximum range of data transfer due to unexpected signal fading from obstacles, atmospheric effects, etc.. Such consideration, in turn, has led to the design of robust and adaptive automatic gain control (AGC) employed in the front end of a typical radio receiver. The primary function of AGC is to maintain a constant signal level at the output, regardless of the signal variations at the receiver input.



The major component of AGC is a variable gain amplifier (VGA) whose gain can be dynamically varied by a feedback control signal as shown in figure 1:



AGC block diagram [1]
Figure 1

Thus, a VGA is an indispensable function block for all radio communication systems. A good design (i.e. large dynamic range for output gain) of VGA is a major factor to ease the design of AGC systems. In some applications, a transmit VGA in mobile handsets is also needed in CDMA systems to regulate each mobile unit transmit power so equal power from each user is received at the base station for optimal system capacity. Moreover, in the era of mixed-mode integrated circuits, the design of analog circuits should be done in the presence of noisy digital circuits. This is because digital circuits always become the bottleneck for technology optimization, instead of analog circuits. This has always been the main reason why analog integrated circuits with wide dynamic range have gained so much attention in recent years, particularly in low voltage-low power applications

In recognizing the importance of VGAs, this paper introduce readers to the background of VGAs as well as to their recent development from the perspective of RF communication systems. Moreover, special attention will be paid to CMOS VGAs since CMOS technologies

provide high integration solution for system-on-chip (SOC) processes. A few practical CMOS VGA circuits will be presented and analyzed for comparison.

A list of references will be included at the end of this paper for those who could be interested in a more in-depth study of the subject.

SECTION I: TWO MAIN APPLICATIONS OF VGAs

This section provides a general overview of the two major applications of VGAs over the past 15 years, namely magnetic data storage systems and telecommunications.

1. Magnetic Data Storage Systems

Before fields of communication had taken off in mid 90s, the major application of variable gain amplifier was for magnetic data storage purposes in 1980s. Disk drive subsystems operating at data rates close to 20 to 40Mbps in large drives constitute a large market for video speed analog and digital ICs. VGAs were used to stablize the average amplitude of the read-back pulses, which consists of different combinations of heads and magnetic media and might normally vary by a factor of 30dB with, to a reference value before they were sent to peak-detector (PD) for best signal detection [2]. Finally, AGC was employed to set the gain of VGA by sensing the average pulse amplitudes in an envelope detector. The 3 major design criteria for such VGA were a controllable gain range of 30dB, a linear phase versus frequency (i.e., flat group delay) characteristic, and low noise figure to prevent SNR degradation [2]. Figure 2 presents a common CMOS topology of a VGA for such purpose.

In this topology, the input differential pair (M1) is capable of providing a variable gain by changing the resistance of its load transistors (M3) with a dynamic bias current $\boldsymbol{I_{c2}}$. The amplified signal of the input stage is then further magnified by the following differential pair (M2). It should also be note that in the case of large gain variation, the bias current for the input stage, $\boldsymbol{I_{c1}}$, also serves as a control for the overall gain of the two stages. The rest of the circuit helps to provide an additional gain stage of fixed amplification as well as widening the bandwidth of the overall circuits by means of neutralization capacitor compensation.

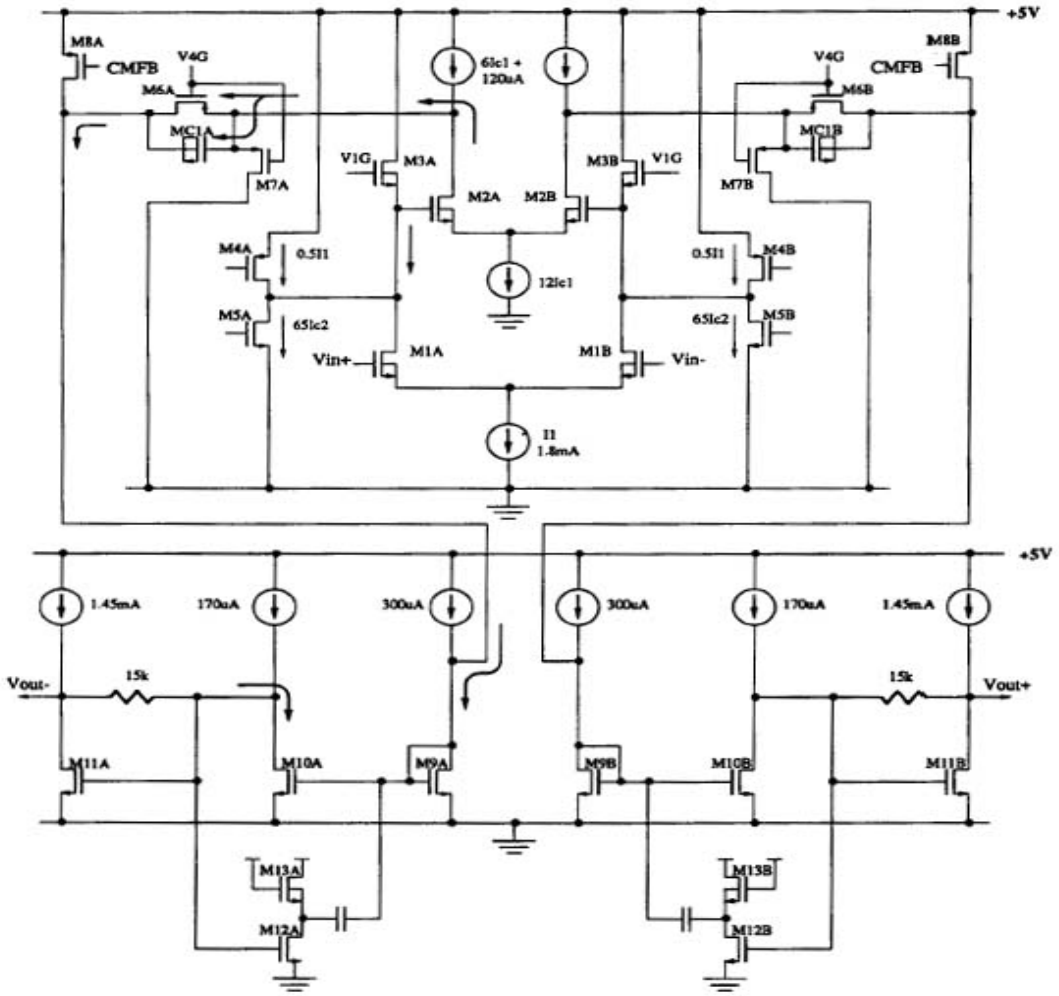


Figure 2: Circuit Diagram of CMOS VGA for Magnetic Data Storage Systems[2]

2. Telecommunication

Due to the rapid growing trend of RF communication systems in recent years, the need for high selectivity and good control of the output signaling level is also one of the many focuses in any communication systems. An AGC system is thus almost found in every transceiver design of wireless systems due to unpredictable incoming signal amplitudes from any possible directions. The need for VGA is undoubtedly essential in these systems for normalizing the

signal amplitude for further digital signal processing in the receiver. The dynamic range and bandwidth of the VGA required range from 50dB to 100dB and 50MHz to 200MHz, respectively, depending on particular applications. Several circuit configurations used in this area will be discussed in the section III. It should be brought to attention that telecommunication has become the major driving force for the development of high performance VGAs nowadays.

SECTION II: BASIC DESIGN REQUIREMENTS OF VGAs

Prior to discussing the advancement of variable gain amplifier (VGA) by studying several typical circuit topologies, it would be beneficial to develop readers with the basic design requirements of VGA. This helps to understand the limitations and design challenges often faced by IC circuit designers.

1. Gain Varying Methods

Traditionally, variations in the gain of a VGA, (i.e. CMOS process), can be obtained by either varying the transconductance of a MOS device operating in saturation or by varying the channel resistance of a MOS device operated in the linear region [3]. The former method requires a varying bias current but the effect is usually not satisfactory because of the square-root relationship between the transconductance of a MOS device with its bias current as shown:

$$Gain \ \alpha \ g_m = sqrt\ (2*KP*(W/L)*I_{bias})$$

For example, a 30dB change in gain implies a large change in bias current in the range of 1x–1000x. This large current variation presents a major drawback in designing high output dynamic range VGAs due to the tremendous power consumption. Moreover, according to [4], the region within which MOS device operates in the saturation region (in a differential pair input

stage) is usually not enough for large output variation in low power operation due to the voltage headroom, $V_{eff} = V_{gs}-V_t$, required. The latter method, on the other hand, requires only variations in gate voltage to modulate the channel resistance of a MOS device. However, a disadvantage is that the signal handling capability of the MOS resistor is low and may lead to significant distortion over a large dynamic range. Various solutions had been presented to tackle the inherent problems such as operating the MOS device in the linear region or cascading gain stages, which results in a smaller gain variation per unit.. A typical block diagram may be as follows:

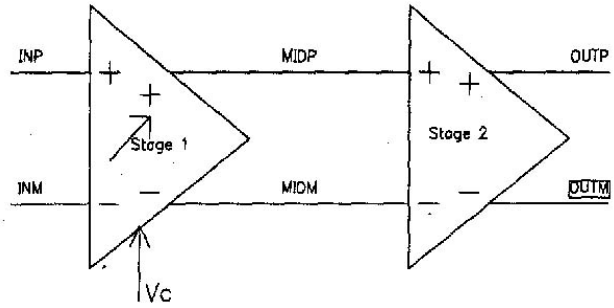


Figure 3: Two-Stage Architecture

where the gain of the first stage is a variable while that of the second is fixed.

2. Exponential Input-to-Gain Variation

An important feature of VGAs is that the gain should increase exponentially with the controlling voltage/current signals. This transforms into a linear increase in gain on a decibel (dB) scale as in figure 4 below:

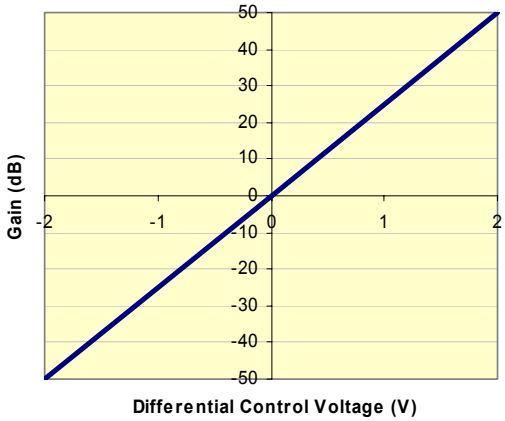


Figure 4: Gain vs Differential Control Voltage on a Semilogarithmic Plot [5]

The functional dependence of VGA gain on control voltage should be such that the loop gain of the AGC remains constant across the entire operating range for the controlling signal. This property leads to a uniform loop transient response and a guaranteed loop settling time regardless of input signal level. This, in turn, allows a wide dynamic range for the amplifier, as well as making the settling time of the AGC constant, which are both desired in any wireless receiver designs [6].

The inherent exponential property with input voltage of bipolar junction transistors (BJTs) presents a viable solution. This is why BJTs have been the norm in VGA design in the past. However, with the increasing demand for SOC technology, it is desirable to produce the CMOS equivalence for low cost and high-integration. One drawback is that when MOSFETs are used in VGAs, they are generally limited to about two decades of gain due to the limited range of current in any one MOSFET over which it obeys the square law. In the extremes at very low currents, the device enters subthreshold; on the other hand, the MOSFETs deviate from the ideal square law at very high current due to mobility degradation caused by high electric fields and extrinsic resistanc. Thus, in recognizing the physical limitations of MOS devices, parasitic bipolar transistors arose as an alternative [5] in early 90s. Yet, the frequency performance was rather

unsatisfactory. Nowadays, circuit designers therefore employ innovative circuit topologies to circumvent the issues such as modification of the Gilbert multiplier cell [7].

3. High Dynamic Range

The dynamic range of the gain control, the extent to which the gain can be varied, is another important parameter of a VGA [8]. Typical value for this parameter may vary from 50dB to as high as 100dB. The main reason for a large dynamic range in gain is the need for low noise figure and low 3rd-order (IM3) distortion.

As shown in figure 5,

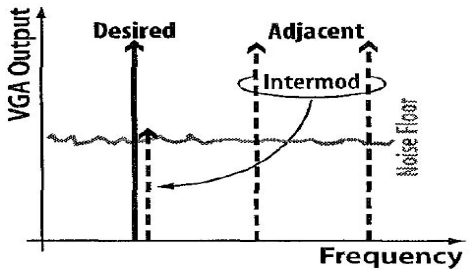


Figure 5: Effects of Adjacent Channels to Desired Signal [6]

when comparable strengths for desired and adjacent channel signals are received, the VGA must present a large gain and a low noise figure at the desired frequency to suppress unwanted cross-channel interferences [6]. Finally, a large input dynamic range is also a desired characteristic of a VGA so that incoming signals received will not be distorted due to clipping or attenuation.

SECTION III: EVOLUTION OF CMOS VGAs

This section discusses the development of VGAs in the past in terms of design criteria and performance. A state-of-the-art CMOS VGA will also be studied at the end.

1. Gilbert Gain Cell [6]

As early as 1968, a versatile analog building block, a four-quadrant multiplier, was first presented by B.Gilbert [7]. This ingenious innovation takes advantage of the two important aspects of differential pairs, 1) small-signal gain of the circuit varies with the tail current and 2) the biasing of the two transistors in a differential pair dictates the distribution of such tail current to one of two destinations. Figure 6 shows such a circuit topology whose gain can be continuously varied from a negative value to a positive value.

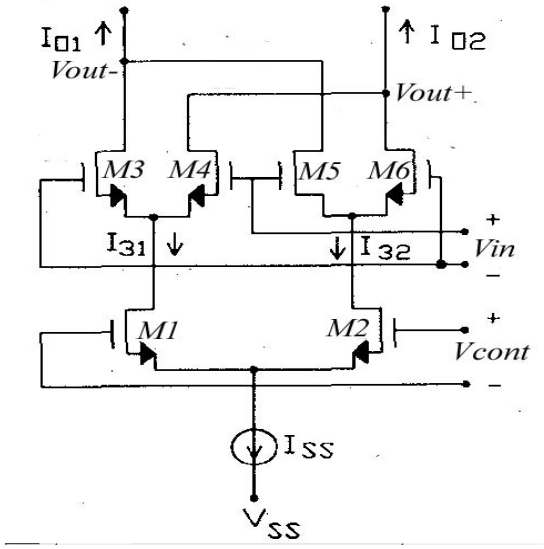


Figure 6: Gilbert Multiplier Cell in CMOS Implementation [7]

With a close study of the circuit, it becomes obvious that the circuit consists of two input cross-coupled differential pairs for V_{in} as well as one for current-steering purpose. The bottom diff.

pair, controlled by V_{cont}, distributes the current from one set of diff. pair to another set of diff. pair. Note that assuming the two input diff. pairs are matched:

$$\text{if } I_{31}=0, \text{ then } V_{out}=(V_{out}+) -(V_{out}-) = - g_m R_{out} (V_{in})$$

$$\text{and if } \quad I_{32}=0, \text{ then } V_{out} = +g_m R_{out} (V_{in})$$

$$\text{for } \quad I_{31} = I_{32} = I_{ss}/2, \quad V_{out}=0$$

Thus, it can be generalized that when $|V_{cont}|$ is large, the gain is either most positive or most negative; when $V_{cont}/2$ is applied to each of the input of M1 and M2, the gain is zero. Therefore, this circuit can be used as an analog amplifier whose output voltage is given by a linear relationship:

$$V_{out} = V_{in} * V_{cont} * R_{out} * sqrt[(K_{1-4})(K_{56})(W/L)_{1-4}(W/L)_{56}/2]$$

where K_{1-4} & K_{56} are the process transconductances of Q_{1-4} and Q_{56}, respectively

Nonetheless, the Gilbert multiplier presented here has two major drawbacks, which lead to some circuit modifications before it can be used as a VGA in an AGC system. The first problem is that the gain and the control voltage do not exhibit an exponential relationship between each other, as required by a good design of VGA to have wide dynamic range and stable transient response of the AGC system. Moreover, the cell consumes twice the amount of valuable voltage headroom (i.e. 2 overdrive voltages V_{eff}) than a simple diff. pair due to the stacked nature. In a low voltage design such as 1.5V, two overdrive voltages is equivalent to more than 25% of the supply voltage.

Regarding bandwidth consideration, the frequency response of this simple multiplier may be as high as tens of megahertz depending on specific applications. An excellent Gilbert cell in integrated circuit form with a bandwidth product of 10GHz is available nowadays from Intesil Corporation, part number HFA3101 [9].

Thus, unless the classical Gilbert cell is modified to circumvent the above issues, its basic form is almost never employed alone in any analog IC designs. In fact, various advancement of it receive wide acceptance in many circuit designs. Therefore, having developed the basics of this basic analog building block helps to better appreciate the operations of the more advanced topologies, which will be discussed later.

2. Opamp with Voltage-Controlled Attenuator [10]

As an alternative to Gilbert cell, the most common configuration consists of an operational amplifier and a voltage-controlled attenuator [10] as shown in figure 7 (only attenuator is shown):

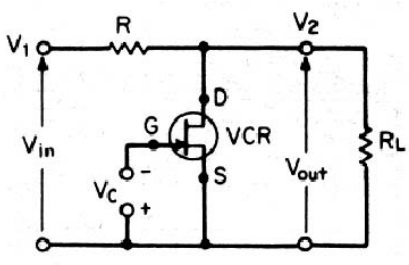


Figure 7: Basic Voltage Controlled Attenuator [10]

The attenuator part consists of a fixed resistor connected in series with a field effect transistor (i.e. JFET) biased in the triode region. Therefore, the FET is equivalent to a variable resistor whose resistance is controlled by the gate voltage, V_c. With successive applications of the voltage divider rule, it can be shown easily that the output voltage is given by:

$$Vout = Vin \ [R_L (1+g_{ds}R_L)^{-1}] / [R + R_L (1+g_{ds}R_L)^{-1}]$$

If the value of R_L is much higher than $r_{ds} = 1/g_{ds}$ and R, the above equation simplifies to:

$$Vout = Vin \ [1+g_{ds}R]^{-1}$$

Therefore, together with the opamp preceding this attenuator, a voltage-controlled gain amplifier is obtained whose gain can be varied by the control voltage applied to the gate terminal of gate that modulates the channel resistance of a FET in triode.

This simple topology, again, presents two serious drawbacks, namely high harmonic distortion and limited signal handling capability. They can be readily solved by feeding back half of the drain-source voltage to the gate. Moreover, this circuit system does not present a linear-in-dB relationship between gain and control signal. Together with its rather low bandwidth, this configuration is not commonly employed in AGC system for RF applications.

3. Parasitic Bipolar Junction Transistors in CMOS[5]

As previously mentioned in Section I.1, one important feature of a VGA is an exponential relationship between the varying gain and controlling signal, either voltage or current. A classic technique suited for this property with wide dynamic range and wide-band VGAs has evolved in bipolar ICs over the past 10 to 15 years based on a two-quadrant Gilbert gain cell, a simpler version of the more advanced four-quadrant version described earlier [5]. This class of circuits, called translinear circuits, makes full advantage of the exponential I-V characteristic, implying a linear dependence of transconductance on bias current, of bipolar transistors.

In recognizing the lack of such relationship of MOSFETs, TZU-WANG PAN and ASAD A.ABIDI, once proposed a 50dB variable gain amplifier using parasitic bipolar transistors in CMOS in 1989 as a viable solution [5]. The motivation was clear that bipolar transistors could now be realized with no modification to the conventional CMOS IC processe. The core of the VGA is shown in figure 8 below.

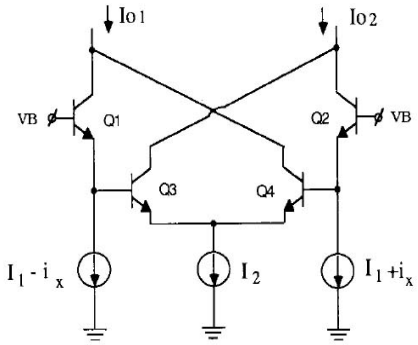


Figure 8: Variation of Gilbert Gain Cell [5]

Although figure 8 shows slight variations to the traditional Gilbert Gain Cell described earlier and consist of two cascaded differential stages, the circuit operation behaves very similarly. It should always be reminded that the circuit topologies are constructed based entirely on parasitic BJTs.

This topology presents an amplification (either voltage if loaded or current) controlled by the two biasing currents. The bases of Q1 and Q2 are biased at a fixed voltage. With the differential input signals i_x entering the emitters of Q1 and Q2, it can be shown that the amplified output differential current, appearing at the collectors of Q1 and Q2, are given by:

$$I_{o2} - I_{o1} = 2i_x (I_2/2I_1 + 1)$$

It is clearer now that the current gain of the amplifier depends on the ratio of the two bias currents I_2 & I_1. It is interesting to note that the maximum achievable current gain is limited by the β of Q3 and Q4 because the base currents of Q3 and Q4 would flow through Q1 and Q2 regardless of I_1 (i.e. zero). The transfer function remains linear for large signals as long as the transistors satisfy the exponential characteristic of BJTs.

This circuit topology, however, did not receive wide acceptance in fields of RF because parasitic nature of BJTs inherently do not process good frequency response (a max. of 10MHz) due to problems such as excessive leakage current along the channels of the co-existing

MOSFET. As device processing technology advances in the past few years, it has been justified, in terms of economical concerns, chip area and performance, that BiCMOS techonologies nowadays are capable of overcoming the inherent problems while taking advantage of the co-existing CMOS processes in IC designs.

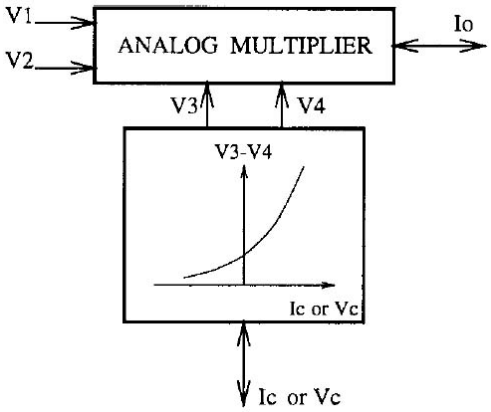
4. State-of-Art RF CMOS VGA

The study of state-of-art RF CMOS VGA will focus on two aspects, namely an exponential current-voltage converter for obtaining the exponential property of conventional MOSFETs, and the VGA cell itself.

Psuedo-Exponential Voltage Generator [4]

The issues of realizing exponential relationship in traditional MOSFETs have been an area of intense research in the past few years to design high performance AGC systems. The solution to this often becomes the bottleneck of designing high performance VGAs. Therefore, we will begin by studying a recent proposed solution to this problem before looking at the entire VGA circuitries.

Although a linear variation in bias current/voltage does not give an exponential variation in output voltage, the problem can be overcome by varying the controlling signals exponentially. A new CMOS pseudo-exponential voltage generator was first designed in 1998 [4] based on this theory. Figure 9a shows the block diagram of the use of such voltage generator to Gilbert multiplier to obtaining exponential variation in the overall gain.



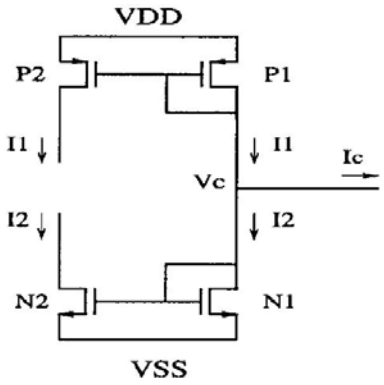


Figure 9a: Block Diagram of a VGA with Exponential-gain control [4] **Figure 9b: Current-to-Voltage Converter [4]**

Recall that the output current of a four-quadrant analog multiplier can be expressed as:

$$I_o = \alpha (V_1-V_2)(V_3-V_4), \text{ where } \alpha \text{ is a constant}$$

With input signals V_1 & V_2 applied differentially, the output of the multiplier varies exponentially if V_3 & V_4 changes exponentially as well. A key advantage is that the dc-bias current is now fixed, not required for gain control. The actual implementation of this exponential current-voltage converter is shown in figure 9b, a back-to-back connection of two current mirrors. The gain control signal I_c is a bidirectional current with sign convention chosen as shown. Assuming $\mathbf{K_{n1}=K_{n2}=K_{p1}=K_{p2}}$, then,

$$I_1=K/2(V_{DD}-V_C-|V_{Tp}|)^2 \qquad \text{and} \qquad I_2=K/2(V_C-|V_{tn}|)^2$$

Moreover, since $I_2=I_1-Ic$,

$$V_C = (V_{DD}-|V_{Tp}|+V_{Tn})/2 - I_C/(K(V_{DD}-V_{Tn}-|V_{Tp}|)$$

Combining the above 3 equations,

$$I_1=(K/2)*((V_{DD}-V_{Tn}-|V_{Tp}|)/2 + I_C/(K(V_{DD}-V_{Tn}-|V_{Tp}|))^2$$

$$I_2=(K/2)*((V_{DD}-V_{Tn}-|V_{Tp}|)/2 - I_C/(K(V_{DD}-V_{Tn}-|V_{Tp}|))^2$$

The ratio of the two currents can be rewritten as:

$$f(y)=I_1/I_2=[(1+y)/(1-y)]^n, \text{ where } n=2, y=I_C/2Kb^2, \text{ and } b=(V_{DD}-V_{Tn}-|V_{Tp}|)/2$$

The function ***f(y)*** gives a close approximation to the exponential function ***exp(2ny)*** within 5% of error. A larger ***n*** provides a larger control range for ***f(y)***. Figure 10 shows the exponential trend of the output current with respect to the control current I_C. The readers should be reminded that the topology described here provides only a typical solution for generating exponential controlling signals applied to Gilbert multiplier. There exist many more interesting configurations that are capable of achieving a wider dynamic range as well as higher operating frequency.

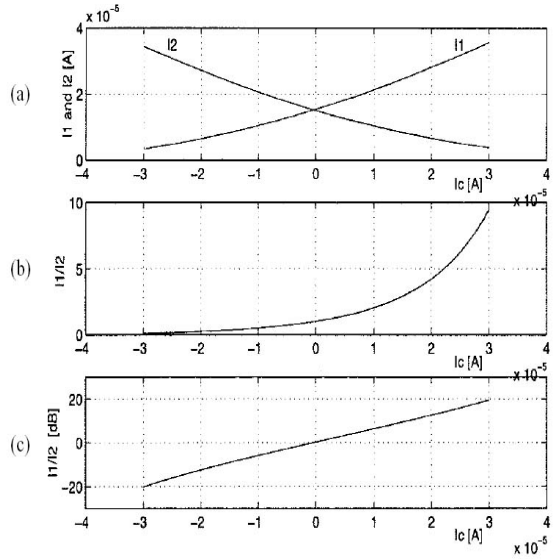


Figure 10: Output Current vs Input Control Current [4]

VGA Cell [6]

In this section, a state-of-art CMOS VGA for a wideband wireless GSM receiver is presented as shown below in figure 11. The design is specifically for use in a low-IF receiver past the down-conversion stage. In real application, five of these cells are cascaded together to provide satisfactory variation in gain of 0 to 70dB to suppress noise level as well as preserving voltage headroom required for signal swing and biasing.

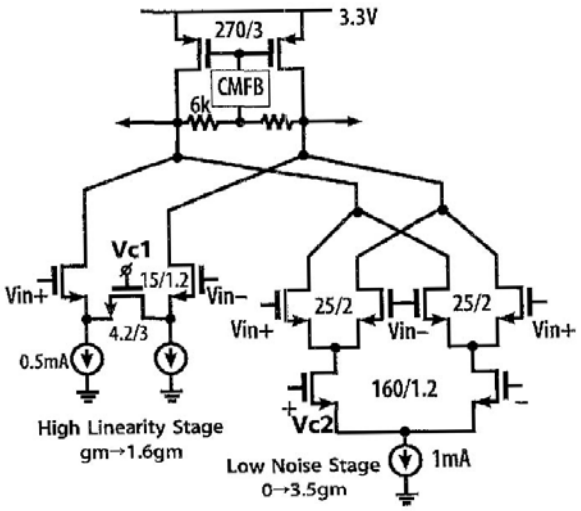


Figure 11: Basic VGA Cell for Wireless GSM Receiver [6]

With reference to figure 11, a fully differential nature is used as this helps to suppress common-mode noise as well as to improve the linearity of the gain characteristics. The topology makes use of the two available options for varying the transconductance of a MOS differential pair: adjustable degeneration resistor (left diff. pair) and varying bias current (right diff. pair). The former handles large signals better with no penalty from the V_{eff} voltage headroom as in an ordinary diff. pair. But this is achieved at the expense of higher noise figure. On the other hand, the latter can compensate the poor noise level with a large gain, when the input signal is small. Thus, the architecture is a hybrid version of the above two types of variable trasconductance. The operation of the circuit is as follows: When input signal is large, only the degenerated stage is activated for a small gain with low noise level. Vc_1 is biased properly while V_{c2} is set to zero. When large signal amplification is required for small input levels, V_{c1} will then be kept at the maximum value (for a lower on-resistance) while V_{c2} is increased for obtaining the desired gain from the multiplier stage. As a result, both stages contribute the overall output current for a maximum gain. The long-channel PMOSs, used as loads, provide a more linear R_{out} compared to short channels. Furthermore, limited by the power supply of around 3.3V, the largest range of

gain from 0 to 15dB is achieved in each cell. When five identical cells are cascaded together, a maximum gain range of 0 to 70dB can be realized. The maximum output swing of this topology is approximately $1.6V_{p-p}$ in order to guarantee all FETs operating in saturation region.

The controlling voltages, Vc_1 & Vc_2, can be varied with respect to the output amplitude to obtain the best overall SNR of the VGA. The gain control strategy can typically be done in two ways: using the pseudo-voltage generator to obtain exponential control voltage variation, and a gain control algorithm performed by a digital AGC loop to controls the VGA [6]. However, such control algorithm, typically employed in a digital AGC system, is not within the scope of this paper. The essence of such loop is to dynamically monitor the control voltages so that the loops gain of the AGC remains constant across the entire operating range. Such property, as described earlier, leads to a uniform loop transient response and a constant loop settling time regardless of input signal level.

As a final note, the bandwidth of this topology is a few tens of megahertz. Nevertheless, it can still be employed in Wireless GSM receiver because the VGA is only used after down-converting the received signals into the low-IF frequency range.

About Biasing...

The discussion thus far focuses entirely on the architecture of CMOS VGA cell. It is assumed that the controlling signal can be varied (i.e. linearly) by using some biasing circuitries, which however, is not considered to be within the scoop of this paper. Nonetheless, readers should still be brought to attention that biasing is often an important issue in the design stage as it may be changed by process, temperature variations, etc..

SECTION IV: FUTURE DIRECTIONS OF VGAs

There will be three main areas of intensive research in the advancement of variable CMOS VGAs in the next few years. They are (1) new approximation methods to realize the exponential function of gain in CMOS, (2) digitized control algorithm for effective varying the gain, and finally (3) higher bandwidth product.

1. New Approximation Methods to Realize Exponential Function

As explained in section I.2, it is highly desirable to have CMOS VGAs to process the exponential gain-to-control signal relationship, as inherited by any BJTs. Other than the parasitic BJTs in CMOS and the pseudo-exponential voltage generator discussed earlier, significant research effort is being allocated to develop a better approximation model to realize such behaviour using Taylor series recently. One good example is the new method that was just proposed in September 2002 [11] by Khaled M. Abdelfattah and Ahmed M. Soliman. Their proposed idea was based on the following approximation:

$$G = exp(x) = exp(\alpha X)/exp(-(1-\alpha)X \approx (1+\alpha X)/(1-(1-\alpha)X)$$

Figure 12 shows the x-y plot of the ideal exponential trend, traditional and new approximations.

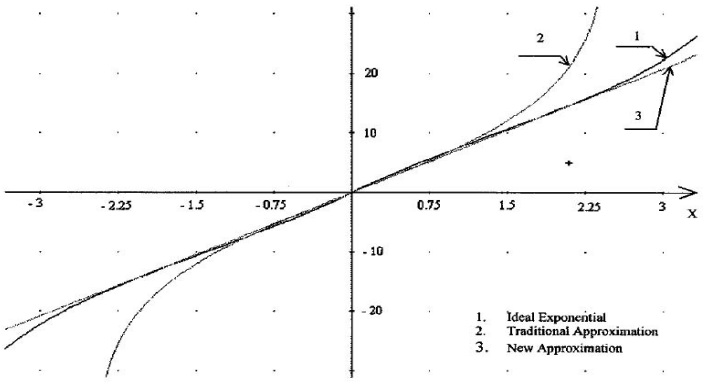


Figure 12: Conventional and New Approximations for the Exponential Function [11]

However, even though a good approximation has been obtained, advanced techniques such as feedback topologies may be necessary to accurate realizing the required function. Therefore, the realization of such function in circuit designs always presents a huge challenge to engineers.

2. Digitized Gain Control Algorithm

In modern receiver design, VGAs are usually employed before the analog to digital conversion to maximize the dynamic range of the data converter used. In advance IC design of receiver architecture, there is an increasing tendency that functional block should be implemented using digital circuitries if possible, due to reduction in chip area for mass production. Thus, it is beneficial to include the AGC loop (excluding the VGA portion) in the digital part of the chip. The DSP then digitally controls the gain of the VGA with programmable circuitries etc.. To the simplest, the gain control algorithm is typically implemented digitally by assigning binary words to different gain levels given a specific dynamic range of the gain control required. This method resembles very much the A/D conversion. This digitization not only minimizes the chip area, more binary words can also be used if extremely precise change in the gain is required. An example of such digitally controlled dB-linear CMOS VGAs was proposed in 1999 [13]

3. Higher Bandwidth Product

Motivated by the tremendous growth in RF electronics, a good design of VGAs should process a high and constant gain over a wide region of operating frequencies. Higher gain can be easily obtained by cascading stages of identical cell, but this also means an increase in noise

level per stage and eventually causes harmonic distortion of the complete circuit. Thus, an extra output stage is often added to existing VGAs to obtain better high frequency response, while still process high and precise transresistance. Another viable solution to date is the development of BiCMOS process which combines the high-integration feature of CMOS technology and is also capable of possessing high bandwidth product with an exponential relationship.

CONCLUSION

This paper presented readers the background of CMOS VGAs as well as their recent development related to RF communication system. Several practical CMOS VGAs circuits have been studied and compared in terms of the dynamic range of the gain control as well as the bandwidth product. In addition, design challenges typically faced by IC designers, such as gain control and exponential relationship between gain and control signals, have also been discussed.

From a short forecast of the directions of future research in CMOS VGAs, it can be concluded that a high performance CMOS VGAs must possess the following 3 criteria, namely high dynamic range of gain (i.e around 90dB gain variation), linear-in-dB gain relationship with control signals, and finally, high bandwidth product with low noise figure. However, there always exist trade-offs between them. Therefore, RF designers must choose the best designs that are suitable only for a the targeted application, while minimizing power consumption and area.

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