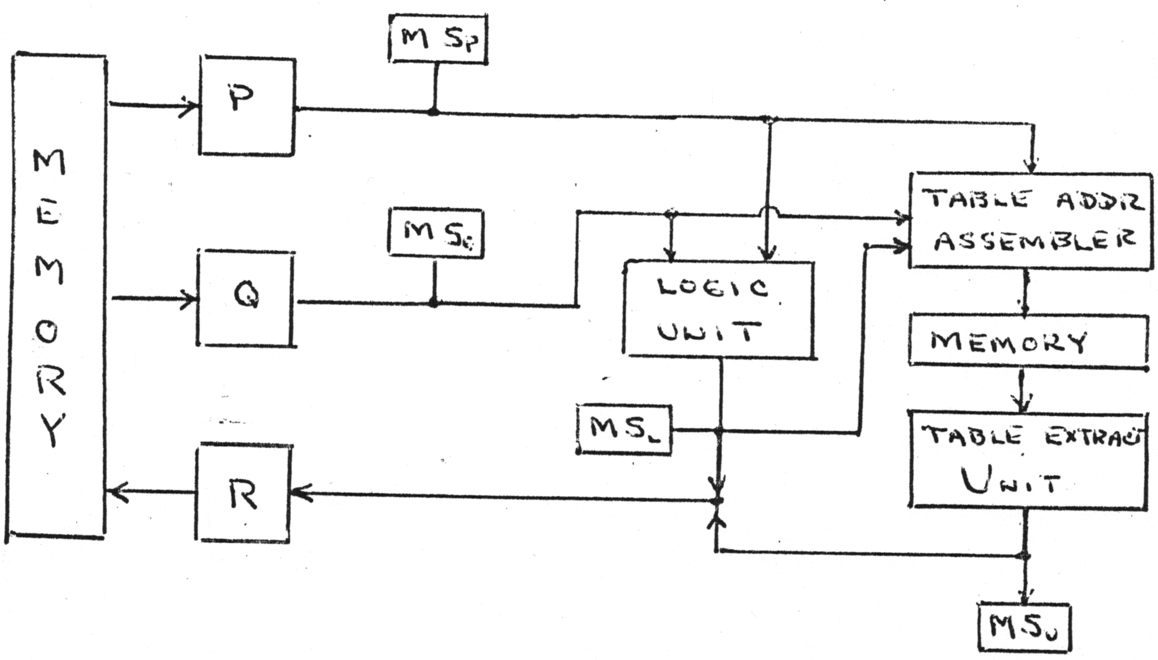
IBM - Company ~~Confidential~~ MPRO-3

IN ORDER TO XPLAIN THE "HARVEST MODE" OF PROCESSING DATA CONSIDER THE FOLLOWING SIMPLIFIED FLOW DIAGRAM



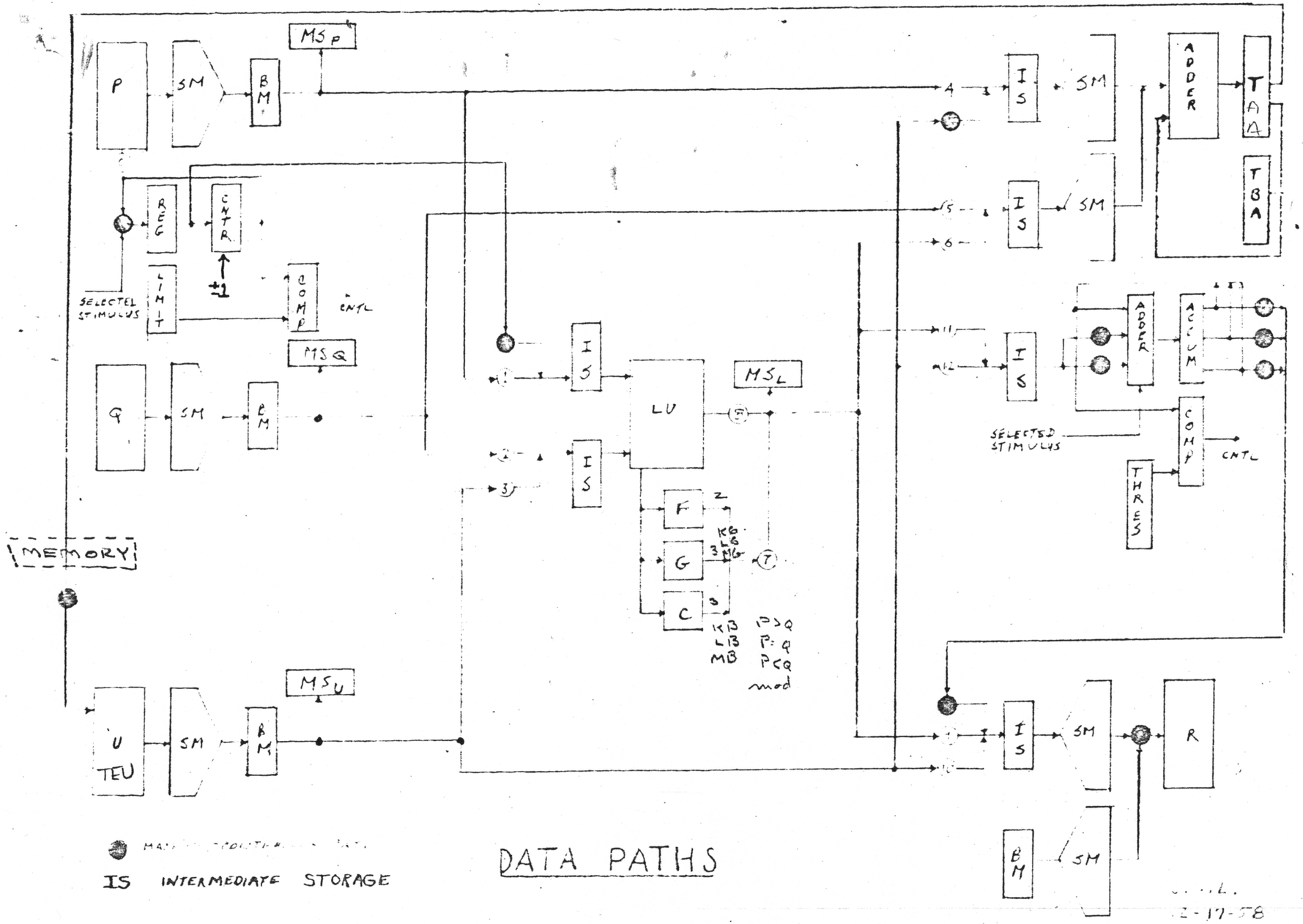
Costanza etc
Yates -
Eger WE

MANY DETAILS HAVE BEEN OMITTED FROM THE DIAGRAM ABOVE. ITS PURPOSE IS TO SHOW THE STREAMING MODE OF OPERATION BY HARVEST

BASICALLY, DATA IS EXTRACTED FROM MEMORY AND SENT TO P AND Q WHICH ARE DOUBLE LENGTH REGISTERS (2 x 64 BITS). FROM THIS POINT ON THE DATA IS OPERATED ON IN 1 TO 8 BIT BYTES. (8 BYTES OF 8 BITS = 1 WORD). THE BYTES FLOW DOWN THE "PIPE LINE" TO THE LOGIC UNIT OR TABLE ADDRESS ASSEMBLER. THE LOGIC UNIT PERFORMS A VARIETY OF ARITHMETIC AND LOGICAL OPERATIONS ON THE SUCESSIVE BYTES OR PAIR OF BYTES PRESENTED TO IT. THE BYTES CAN THEN BE SENT TO R AND ON TO MEMORY AFTER AN ACCUMULATION OF BYTES TO MAKE A WORD; OR THE OUTPUT OF THE LOGIC UNIT CAN BE SENT TO THE TABLE ADDRESS ASSEMBLER AND SUBSEQUENTLY TO MEMORY. THE TABLE ADDRESS ASSEMBLER (TAA) PROVIDES A MEANS OF ASSEMBLING BYTES FROM ONE OR MORE OF THE STREAMING UNITS (SU), TOGETHER WITH THE CONTENTS OF A REGISTER, TO FORM ADDRESSES FOR TABLE LOOKUP, COUNTING IN MEMORY, AND SIMILIAR MEMORY REFERENCE FUNCTIONS.

NOW LETS REFER TO THE FOLLOWING DIAGRAM AND START ALL OVER.

29 APR 1959



MA... SOUTH...

IS INTERMEDIATE STORAGE

DATA PATHS

...L.
2-17-58

THIS DIAGRAM SHOWS THE VARIOUS FUNCTIONAL UNITS OF THE HARVEST PROCESSING UNIT (CPU) AND THE DATA PATHS.

STREAM UNITS P & Q (SU_P OR SU_P)

THESE UNITS CONTROL THE INPUT DATA STREAMS. EACH CONSISTS OF A DOUBLE LENGTH REGISTER (128 BITS), AN ASSOCIATED SWITCH MATRIX (SM_P OR SM_Q) THE SWITCH MATRIX CONVERTS THE 64 BIT WORD TO BYTES OF 8 BITS. THE UNITS CONTAIN A BUILT-IN INDEXING UNIT

STREAM UNIT R (SU_R)

THIS UNIT CONSISTS OF A DOUBLE LENGTH REGISTER (128 BITS), AN ASSOCIATED SWITCH MATRIX (SM_R) (8 → 64 BITS) AND A BUILT IN INDEXING UNIT. THE UNIT IS USED PRIMARILY TO STORE DATA STREAMS INTO MEMORY.

BYTE MASKS (BM)

THE BYTE MASK INDICATES WHICH BITS OF AN 8 BIT BYTE ARE ~~TO BE~~ OPERATED ON. FOR EXAMPLE IF BM_P EQUALS ~~00001111~~ 11110000, THE ~~LOWER ORDER~~ FIRST 4 BITS POSITIONS OF THE BYTE FROM P WOULD BE EFFECTIVE.

MATCH UNITS (MS)

DURING THE STREAMING MODE OF OPERATION IT IS POSSIBLE TO MONITOR INPUT AND OUTPUT STREAMS FOR A PRE-SPECIFIED BYTE. AUTOMATIC ADJUSTMENTS OF THE DATA FLOW MAY BE INITIATED UPON RECOGNITION OF A PRE-~~SPECI~~ SPECIFIED BYTE

LOGIC UNIT (LU)

THE LU PERFORMS A VARIETY OF ARITHMETIC AND LOGICAL OPERATIONS ON THE SUCCESSIVE BYTES OR PAIR OF BYTES PRESENTED TO IT. BESIDES AN 8 BIT BYTE OUTPUT, THE LU PROVIDES THREE 1 BIT OUTPUTS (K, L, M,) WHICH ARE SENT TO F, G, & C. THESE MAY BE USED FOR ADJUSTMENTS.

STREAM UNIT T, TABLE ADDRESS ASSEMBLER (TAA)

THE TABLE ADDRESS ASSEMBLER PROVIDES A MEANS OF ASSEMBLING BYTES FROM ONE OR MORE OF THE SU'S TO

TOGETHER WITH THE CONTENTS OF X REGISTER, TO FORM ADDRESSES FOR TABLE LOOKUP. TAA IS A DOUBLE LENGTH ADDRESS REGISTER (48 BITS LONG [24 BITS FOR 1 ADDRESS]), A BASE ADDRESS REGISTER, AND BUILT IN INDEXING UNIT.

STREAM UNIT U, TABLE EXTRACT UNIT (TEU)

THE TABLE EXTRACT UNIT IS A DATA STORAGE REGISTER WHOSE PRIMARY FUNCTION IS TO RECEIVE DATA WORDS FROM MEMORY AS ADDRESSED BY TAA. IT HAS ITS OWN SWITCH MATRIX (64-8) AND BUILT IN INDEXING.

STATISTICAL COUNTER (SCTR)

THE STATISTICAL COUNTER MAY BE STEPPED BY PRACTICALLY ANY ONE BIT SIGNAL FROM CPU. ITS CONTENTS MAY BE GATED ONTO THE BYTE BUS TO SUR BY ADJUSTMENT OPERATIONS. SCTR MAY BE RESET AUTOMATICALLY. IT MAY ALSO BE CONNECTED TO SM_p AND HAVE ITS CURRENT CONTENTS CONTINUOUSLY AVAILABLE FOR LOGICAL OPERATIONS.

STATISTICAL ACCUMULATOR (SACC) AND THRESHOLD REG. (THR)

THE SACC ACCUMULATES BYTES FROM LU OR TEU. IT MAY BE STEPPED BY ANY ONE OF SEVERAL ONE BIT SIGNALS OF CPU. ASSOCIATED WITH SACC IS A THRESHOLD REGISTER. IN THE "SET UP" THR CAN BE LOADED AND WHEN SACC EQUALS OR EXCEEDS THR, A SPECIAL ONE BIT SIGNAL IS PRODUCED WHICH CAN CAUSE SPECIAL ACTION IN CPU.

IT MIGHT BE WELL TO DEVIATE SOME AT THIS POINT. A WORD IN HARVEST IS 72 BITS (64 DATA BITS AND 8 ECC BITS. ECC = DOUBLE ERROR DETECTION AND SINGLE ERROR CORRECTION.) AN ADDRESS CONSISTS OF 24 BITS, 18 BITS FOR THE WORD ADDRESS, 6 BITS FOR THE BIT ADDRESS. WE CAN THUS ADDRESS ANY BIT OF ANY WORD IN HARVEST. FOR EXAMPLE 1000.06 WOULD MEAN ADDRESS THE 6 BIT IN WORD BEGINNING AT LOCATION 1000. IF WE EXTRACT 64 BITS (ONE WORD) WE WOULD EXTRACT 58 BITS OF WORD AT LOCATION 1000.00 (STARTING WITH BIT 6 THRU BIT 63) AND THE FIRST 6 BITS OF THE WORD AT LOCATION 1001.00 (BITS 0-5 AT LOCATION 1001.00)

STREAM INDEXING.

GENERALLY SPEAKING, THE HARVEST COMPUTER OBTAINS DATA FROM ONE OR TWO PLACES IN MEMORY, PERFORMS SOME ARITHMETIC OR LOGICAL OPERATION ON THE DATA, AND STORES THE RESULT BACK IN MEMORY. THE ADDRESS OF THE SOURCE OR SOURCES AND THE DESTINATION OF THE DATA ARE INDEPENDENT OF EACH OTHER, AND ARE MODIFIED BY INDEPENDENT INDEXING UNITS.

THE PATTERN OF ADDRESS MODIFICATION ASSOCIATED WITH ANY STREAM IS DETERMINED BY A NUMBER OF PARAMETERS AT EACH OF THE SEVERAL LEVELS OF INDEX CONTROL. THE CONTROL LEVELS ARE CHAINED TOGETHER SO THAT THERE IS A FIRST, SECOND, ''''' AND HIGHEST LEVEL OF CONTROL. THERE IS NO MAXIMUM LIMIT AS TO THE NUMBER OF LEVELS OF CONTROL. THE VALUES OF THE PARAMETERS ARE SET BY THE PROGRAMMER WHEN HE SETS UP AN INDEXING CHAIN.

THREE MODES OF INDEXING ARE AVAILABLE TO THE PROGRAMMER, NESTED, SEQUENTIAL AND TRIANGULAR INDEXING.

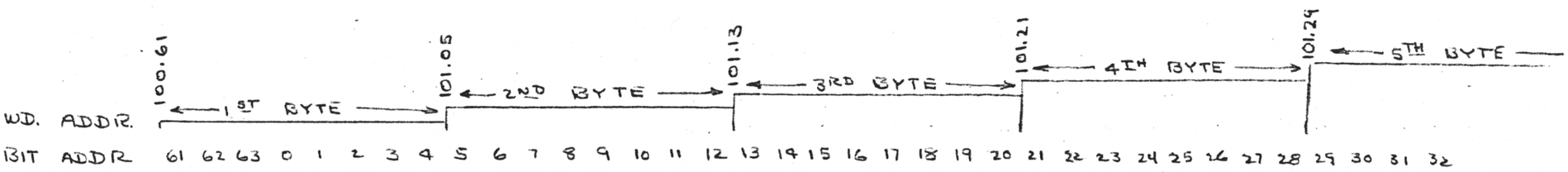
IN ORDER TO PREPARE THE HARVEST COMPUTER TO EXECUTE A STREAM INSTRUCTION, THE PROGRAMMER MUST SET UP A NUMBER OF PARAMETERS AND CONTROLS. TO ACCOMPLISH THIS, HE MAY TRANSMIT A SET OF 20 CONSECUTIVE SET UP WORDS FROM SOMEWHERE IN MEMORY TO FIXED REGISTERS. THESE REGISTERS HAVE SPECIAL ADDRESSES AND ARE USED SPECIFICALLY FOR THIS PURPOSE.

BEFORE GOING TO TOO MUCH DETAIL LETS TAKE A VERY SIMPLE EXAMPLE TO DEMONSTRATE HOW STREAM INDEXING WORKS. TO ACCOMPLISH THIS THE FOLLOWING DEFINITIONS ARE OFFERRED.

S = STARTING ADDRESS; ADDRESS GIVES LOCATION IN MEMORY OF DATA.
I = INCREMENT - NO. OF BITS FROM BEGINNING OF PREVIOUS BYTE THAT THIS BYTE IS TAKEN
N = NO. OF BYTES TO BE TAKEN.

CONSIDER NOW THE EXAMPLE ON THE FOLLOWING PAGE.

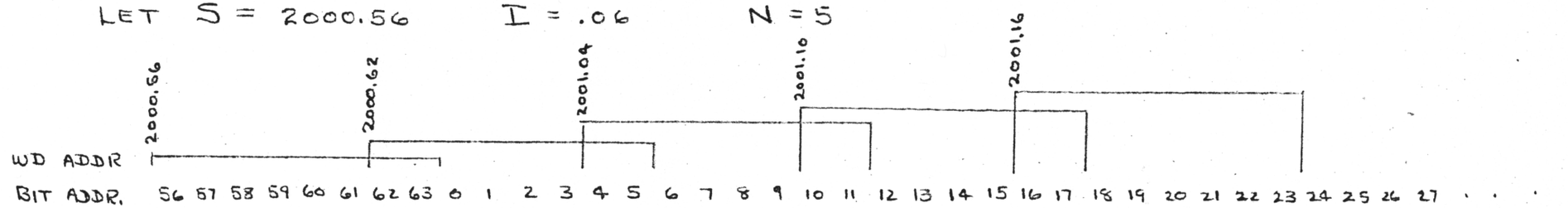
LET S = 100.61 I = .08 N = 5 THIS IS SHOWN AS FOLLOWS:



THE ABOVE GIVES 5 GROUPS, 8 BITS EACH, STARTING AT ADDRESS 100.61. THE BM IN THIS CASE WOULD BE 11111111.

NOW LETS SAY WE WANT 5 CHARACTER GROUPS, BUT ONLY 5 BITS FROM A 6 BIT FRAME SUCH AS IBM 727. THE DATA STARTS AT LOCATION 2000.56

LET S = 2000.56 I = .06 N = 5



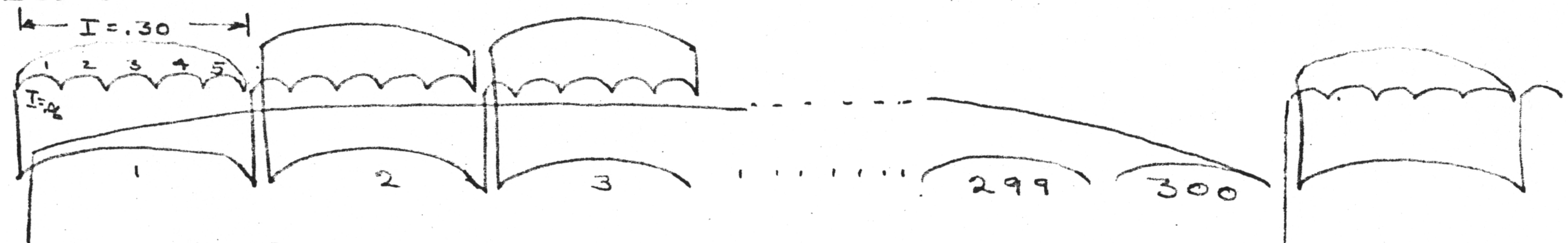
SINCE WE ONLY WANT 5 BITS PER CHARACTER, THE BM = 11111000. THE FIRST BYTE IS TAKEN AT THE SPECIFIED S (2000.56). THESE 8 BITS ARE SENT THROUGH THE BM SUCH THAT ONLY THOSE BITS OF THE BYTE WHERE A '1' APPEARS IN THE BM ARE ACTUALLY OUTPUTTED. WHERE '0's APPEAR IN THE BM, '0's ARE OUTPUTTED. THE INCREMENT .06 IS THEN ADDED TO THE VALUE SPECIFIED BY S SO THE STARTING ADDRESS OF THE 2ND BYTE IS 2000.56 + .06 = 2000.62 ETC.

S, I, AND N ARE SPECIFIED BY THE PROGRAMMER AND REPRESENT A LEVEL OF INDEXING. A STREAM BYTE BY BYTE INSTRUCTION HAS TO BE GIVEN (IN THIS CASE) (OTHER STREAMING INSTRUCTIONS ARE USED WITH INDEXING ALSO)

LETS ASSUME WE HAVE 1 MSG. OF 300 GROUPS, 5 CHARACTERS PER GROUP, 4 BITS PER CHARACTER AND THE MSG STARTS AT ADDRESS 1953.00, ALSO WE HAVE 1 CHARACTER PER 6 BITS. NOW LET THE FIRST LEVEL OF INDEXING BE $S_1 = 1953$ $I_1 = .06$ $N_1 = 5$. THIS 1ST LEVEL GIVES US 5 GROUPS OF 6 BITS EACH. (5 CHARACTERS) NOW ADVANCING TO THE SECOND LEVEL OF INDEXING LET $S_2 =$ ______ $I_2 = .30$ $N_2 = 300$. THE SECOND LEVEL OF INDEXING SETS S_1 TO $1953 + .30$ $(S_1 + I_2)$ AND WE PROCEED TO PRODUCE ANOTHER GROUP OF 5 CHARACTERS. EACH TIME WE PRODUCE A GROUP N_2 IS DECREMENTED BY 1 SO THAT THE SECOND LEVEL OF INDEXING WILL PRODUCE 300 GROUPS OF 5 CHARACTERS OR PROCESS 1 MSG. GRAPHICALLY IT MAY BE DEMONSTRATED AS SHOWN BELOW

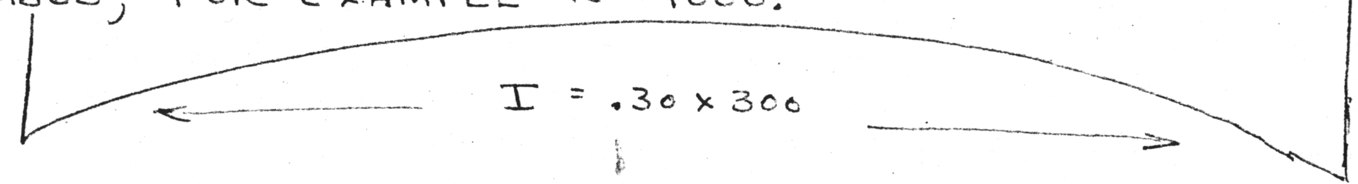
1ST LEVEL

2nd LEVEL



NOW BY ADDING A 3RD LEVEL OF CONTROL WE CAN PROCESS ANY NUMBER OF MSGS. WE WANT. THE INCREMENT FOR THE THIRD LEVEL (STARTING ADDRESS) WOULD BE THE MSG LENGTH OR $I_3 = .30 \times 300$. N_3 WOULD THEN SPECIFY THE NUMBER OF MSGS; FOR EXAMPLE $N = 1000$.

3RD LEVEL



THE ADDRESS MODIFICATION IS PERFORMED AUTOMATICALLY BY THE BUILT IN INDEXING UNITS IN EACH SU. THE PROGRAMMER MERELY SPECIFIES THE STREAMING INSTRUCTION TO BE USED, THE LEVELS OF INDEXING, ADJUSTMENTS CONNECTIVES, STIMULII, ETC.

REFERRING TO THE MORE DETAILED FLOW DIAGRAM OF THE HARVEST STREAMING UNIT YOU WILL NOTICE 13 NUMBERED GATES. THESE GATES ARE UNDER CONTROL OF THE PROGRAMMER. IN THE INSTRUCTION THERE IS 13 BITS THAT CONTROLS THESE GATES SO THE PROGRAMMER CONTROLS THE PATH THAT THE DATA CAN TAKE.

LETS CONSIDER THE FOLLOWING SIMPLE PROBLEM. COMPARE THE AMOUNT OF WORK ENVOLVED HERE TO A COMPUTER NOW EXISTING, IN ARRIVING AT THE SOLUTION.

PROBLEM: ADD MOD 10, ONE 5 CHARACTER GROUP, 4 BITS PER CHARACTER LOCATED AT ADDRESS 1000 TO 300 MSGS, 150 GROUPS PER MSG, 4 BITS/CHAR AND ONE CHARACTER PER 6 BITS LOCATED AT STARTING ADDRESS 2000.00. STORE RESULTS 4 BITS PER CHARACTER AT STARTING ADDRESS 5000

SOLUTION: CREATE A STREAM CONSISTING OF THE ONE 5 CHARACTER GROUP TO BE ADDED 150 x 300 LONG. (THIS ONE GROUP WILL BE REPEATED 150 TIMES FOR EACH MSG AND SINCE THERE ARE 300 MSGS; 150 x 300) CREATE ANOTHER STREAM WHICH WILL CONSIST OF THE DATA TO WHICH THE GROUP IS ADDED. ADD THESE TWO STREAMS IN LU AND SET UP R INDEXING FOR STORING RESULTS.

	LEVEL	S	I	N
P STREAM	L_1P	1000	.04	5
	L_2P	—	—	150 x 300
Q STREAM	L_1Q	2000	.06	~~150~~ 5
	L_2Q	—	.30	150
	L_3Q	—	150x.30	300
R STREAM	L_1R	5000	.04	5 x 150 x 300

BM_P = 11110000 BM_Q = 11110000 BM_R = 11110000
MOD = 10100000 OP CODE 30 (MOD 10) [ADD P+Q]
STOP AT END OF LEVEL 3 IN Q

NOTE BM = 1111 0000 MOD = 1010 0000 THE $2^3 2^2 2^1 2^0$ 1010 FALLS IN LINE WITH THE ONES IN BM.

EDITORIALIZE! FORMATS, ADJUSTMENTS, STIMULI, OP CODES ETC. HAVE NOT BEEN PRESENTED AS THEY ARE CONTINUALLY BEING CHANGED. THE LATEST REVISION BEING DATED 6 APRIL 1959. WE HAVE BEEN PROMISED BY IBM, A NEW HARVEST MANUAL BY JULY 1959. AS THIS INFORMATION BECOMES FIRM AND AVAILABLE I WILL ATTEMPT TO EXTRACT PERTINENT INFORMATION AND PASS IT ALONG.

THE P & Q REGISTERS MENTION HERE ARE NOT ONLY USED IN HARVEST BUT SERVE ANOTHER PURPOSE IN THE BASIC COMPUTER SUCH AS THE ACCUMULATOR. THIS IS SHARED CIRCUITRY.

IF FUTHER INFO IS DESIRED ON HARVEST, THERE ARE MANY MEMO's (MANY OUTDATED, MANY REVISED) THAT ARE AVAILABLE.

JACK E. LEHMAN
21 APRIL 1959