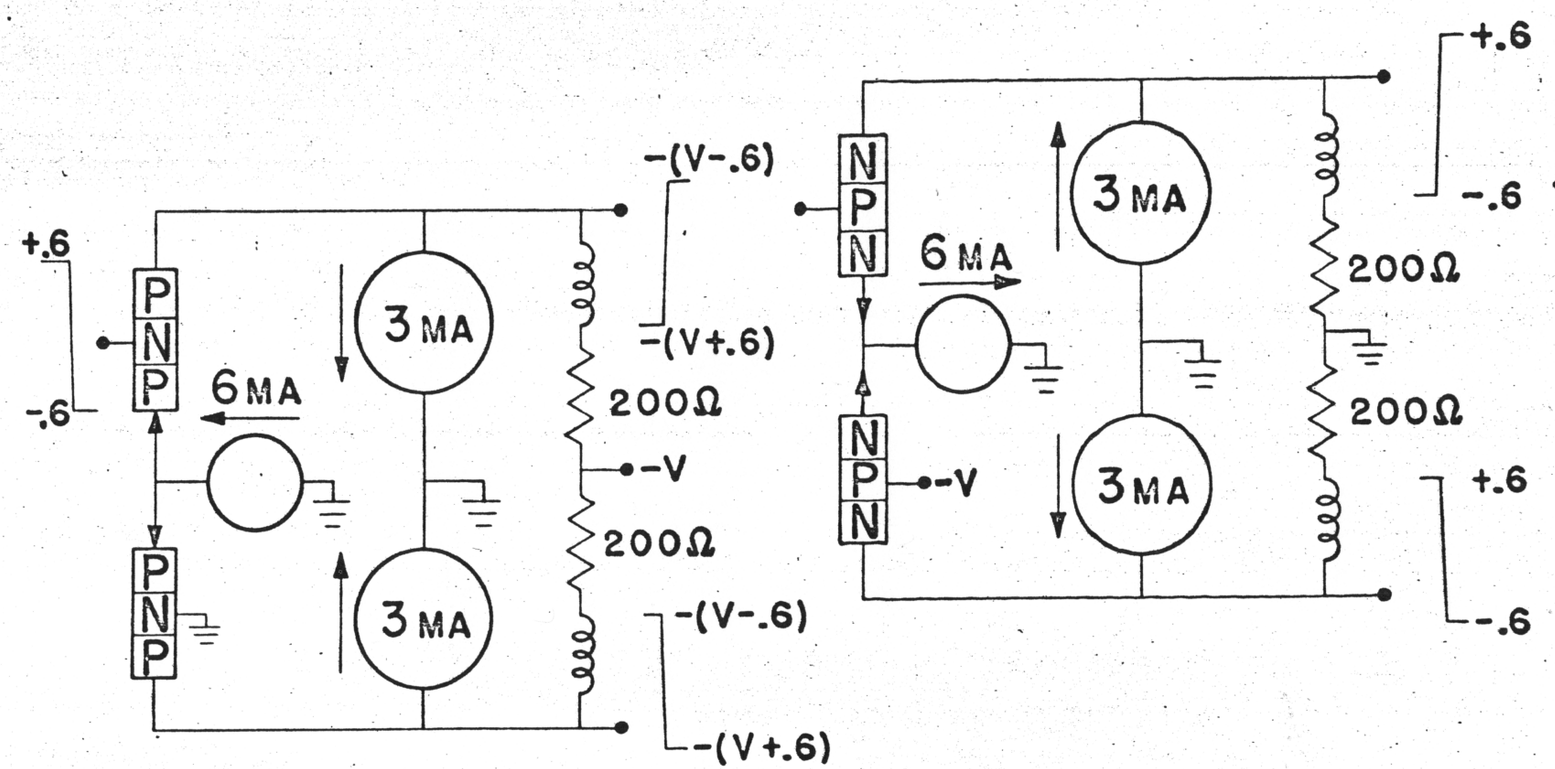

FIG. 2

NPN AND PNP BASIC TRANSISTOR BLOCKS WITH INPUT AND OUTPUT LEVELS SHOWN TO ILLUSTRATE COMPATIBILITY

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IF THE VOLTAGE AT THE BASE OF THE TOP TRANSISTOR (FIG 1) IS PERMITTED TO ASSUME A VALUE SLIGHTLY MORE POSITIVE OR SLIGHTLY MORE NEGATIVE THAN THE POTENTIAL OF THE BASE OF THE BOTTOM TRANSISTOR (THIS CASE, GROUND), THE CURRENT I WILL FLOW INTO THE EMITTER OF ONE TRANSISTOR TO THE EXCLUSION OF THE OTHER. A VOLTAGE SWING OF +.4 TO -.4 VOLTS (MINIMUM) ABOUT THE REFERENCE IS SUFFICIENT TO GUARANTEE SWITCHING.

FOR A POSITIVE INPUT VOLTAGE WHOSE MAGNITUDE IS EQUAL TO OR GREATER THAN THE EMITTER TO BASE VOLTAGE OF THE BOTTOM TRANSISTOR, THE BOTTOM TRANSISTOR WILL CONDUCT AND THE TOP TRANSISTOR WILL BE OFF.

FOR A NEGATIVE INPUT VOLTAGE WHOSE MAGNITUDE IS EQUAL TO OR GREATER THAN THE EMITTER TO BASE VOLTAGE DROP OF THE TOP TRANSISTOR, THE TOP TRANSISTOR WILL CONDUCT AND THE BOTTOM TRANSISTOR WILL BE OFF.

TWO BASIC BUILDING BLOCKS, ONE A PNP BLOCK AND THE OTHER AN NPN BLOCK ARE SHOWN IN FIG 2. BOTH BLOCKS ARE 6 MA. CURRENT SWITCHES.

THERE ARE SEVERAL TECHNIQUES FOR COUPLING BASIC BUILDING BLOCKS OR THE RESULTING LOGICAL BLOCKS. THE TECHNIQUE USED IN HARVEST USES ALTERNATE PNP AND NPN BLOCKS DIRECTLY COUPLED.

TO DATE THERE ARE NO DIODES USED IN THE LOGICAL BLOCKS.

THE CIRCUITS USED IN HARVEST ARE DESIGNED AGAINST "END OF LIFE FIGURES." THIS IS MEANT TO BE — — "IF ALL THE COMPONENTS IN THE SYSTEM REACHED THE END OF LIFE VALUES AT THE SAME TIME, THE SYSTEM WOULD STILL OPERATE." ONE PERCENT COMPONENTS ARE USED THROUGHOUT. AT END OF LIFE 1% TOLERANCE COMPONENTS SHOW A VALUE NOW ± 3%. THE CIRCUITS ARE SUPPOSEDLY DESIGNED AROUND THIS ± 3% FIGURE.

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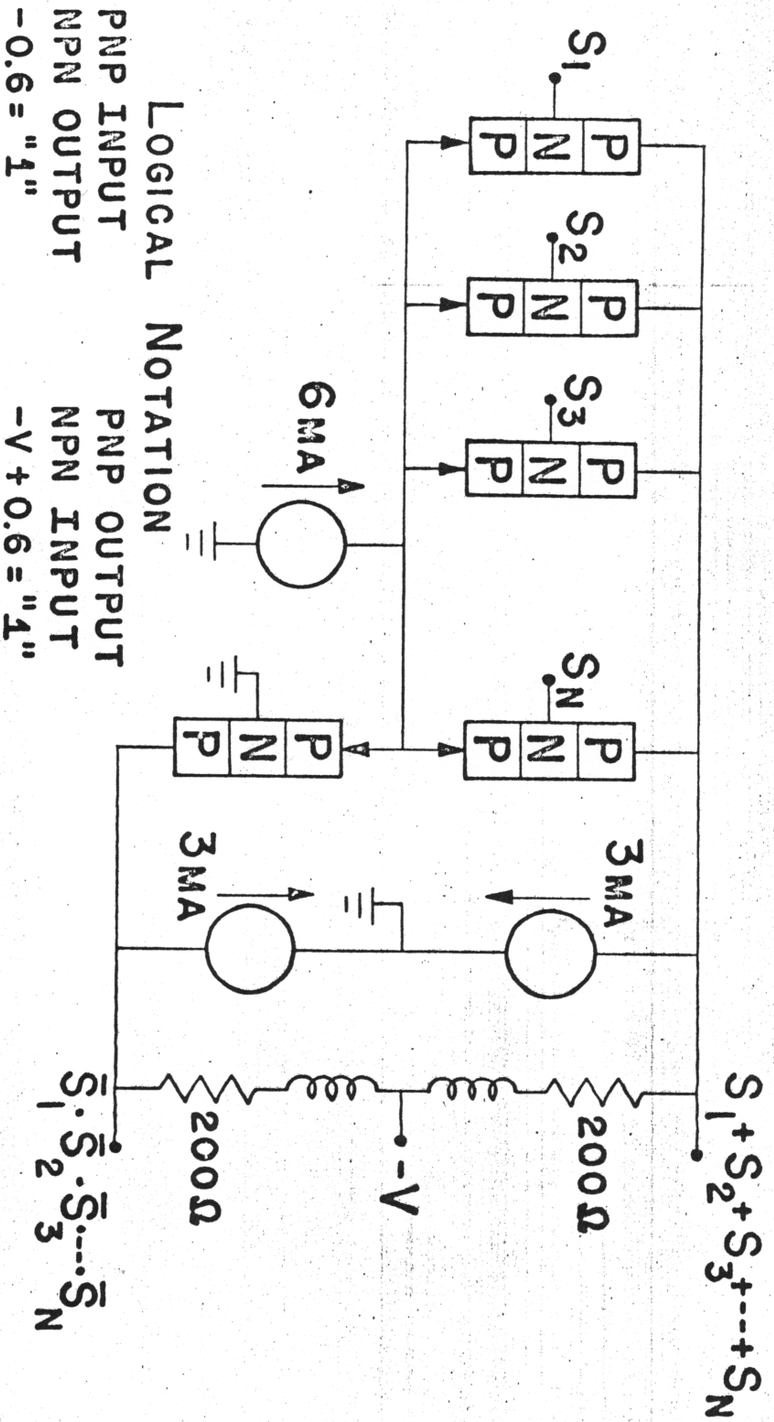

LOGICAL NOTATION

PNP INPUT
NPN OUTPUT
-0.6 = "1"
+0.6 = "0"

PNP OUTPUT
NPN INPUT
-V + 0.6 = "1"
-V - 0.6 = "0"

FIG. 5

"N" - WAY COMPLEMENTED "OR" CIRCUIT

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A TYPICAL LOGICAL AND-OR CIRCUIT IS SHOWN IN FIG. 5. USING THE NOTATION THAT THE OUTPUT OF A CONDUCTING TRANSISTOR AND THE INPUT ENABLING IT TO CONDUCT ARE LOGICAL "ONES", THIS CIRCUIT MAY BE CALLED AN N-WAY COMPLEMENTED OR CIRCUIT

WHERE ANY OR ALL OF THE INPUT SIGNALS TO THIS CIRCUIT ARE LOGICAL ONES, THE CURRENT THROUGH THE PARALLEL COMBINATION OF THE TOP TRANSISTORS IS 6 MA., AND THE CURRENT THROUGH THE BOTTOM TRANSISTOR IS ZERO. THE BOTTOM TRANSISTOR CONDUCTS 6 MA. ONLY WHEN ALL INPUTS ARE LOGICAL ZERO's. SINCE ALL SIGNALS HAVE THEIR COMPLIMENTS AVAILABLE, THE CIRCUIT CAN PERFORM "AND" OR "OR" OPERATIONS ON N SIGNALS.

THE TOP OUTPUT IS COMMONLY REFERRED TO AS THE α OUTPUT AND THE BOTTOM OUTPUT AS THE β OUTPUT.

THE CIRCUITS NOW BEING USED HAVE A BETTER OUTPUT WAVE SHAPE THAN THE INPUT SIGNAL. THE DRIFT TRANSISTORS ACTUALLY SHAPE THE WAVE IN PERFORMING THE LOGICAL FUNCTION, THUS SHAPERS ARE NOT NECESSARY. THE MAXIMUM ALLOWABLE DESIGN DELAY PER LOGICAL BLOCK WAS 20 MILLI-MICRO-SECONDS. A DELAY THROUGH 4 'AND's WAS 35-40 mμSEC.

THERE ARE BASICALLY FOUR TYPES OF LOGIC BLOCKS USED WHICH ARE

1. REGULAR CURRENT SWITCHING
2. EMITTER FOLLOWER
3. THREE LEVEL LOGICAL BLOCK
4. CASCODE GATES

ON THE FOLLOWING PAGES ARE LISTED THE SYMBOLS OF THE BUILDING BLOCKS AND THEIR ASSOCIATED TRUTH TABLES.

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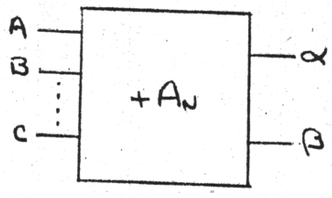
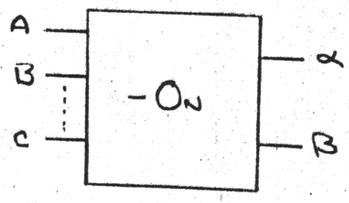
CURRENT SWITCHING

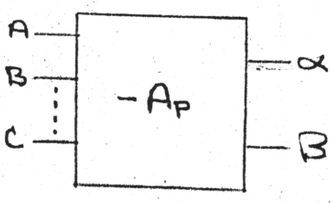
N LINE 'AND' - 'OR'

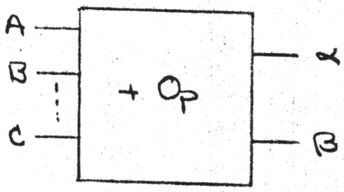




A·B·C	AvBvC	α	β
+		−	+
−		+	−
	−	+	−

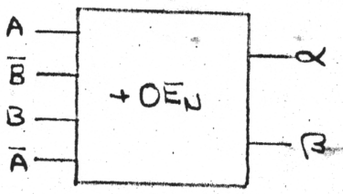
P LINE 'AND' - 'OR'

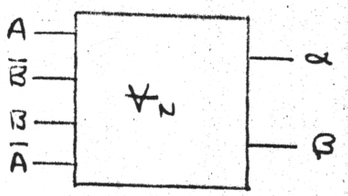




A·B·C	AvBvC	α	β
−		+	−
+		−	+
	+	−	+

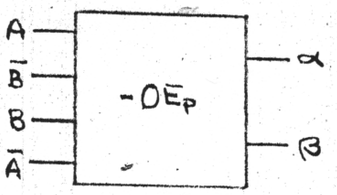
EXCLUSIVE 'OR' N LINE

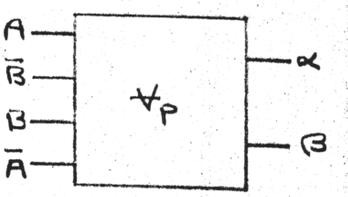




A	$\bar{A}$	B	$\bar{B}$	α	β
+	−	+	−	+	−
−	+	+	−	−	+
+	−	−	+	−	+
−	+	−	+	+	−

EXCLUSIVE 'OR' P LINE

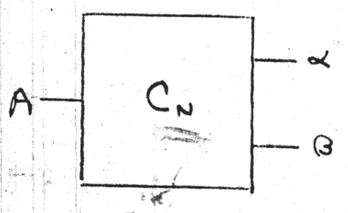




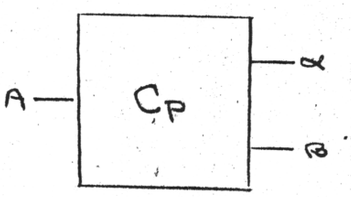
A	$\bar{A}$	B	$\bar{B}$	α	β
+	−	+	−	−	+
−	+	+	−	+	−
+	−	−	+	+	−
−	+	−	+	−	+

TRANSLATE BLOCK

N LINE



P LINE



N LINE TRUTH TABLE

A	α	β
+	−	+
−	+	−

P LINE TRUTH TABLE

A	α	β
+	−	+
−	+	−

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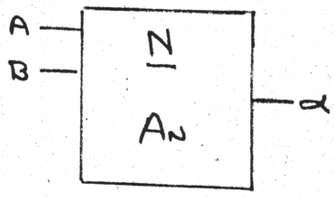
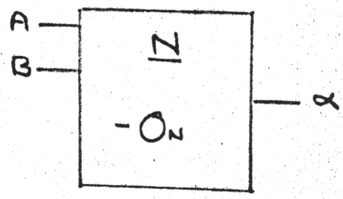
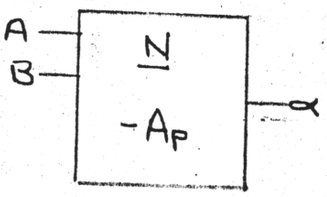
EMITTER FOLLOWER CIRCUITS

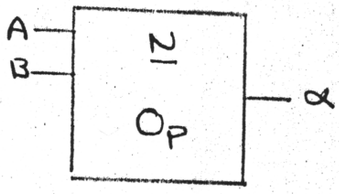
N LINE 'AND' - 'OR'





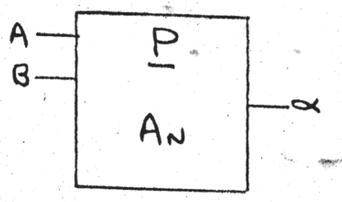
A·B	AvB	α
+		+
	−	−

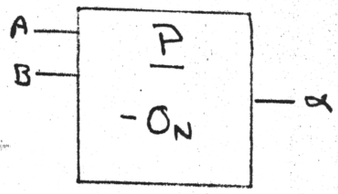




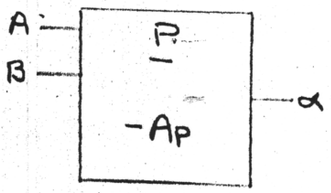
A·B	AvB	α
	+	+
−		−

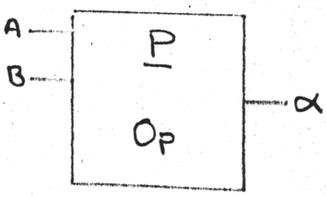
P LINE 'AND' - 'OR'





A·B	AvB	α
+		+
	−	−





A·B	AvB	α
−		−
	+	+

NOTE: THE DELAY MEASURED THROUGH AN EMITTER FOLLOWER STAGE WAS NEVER GREATER THAN 10 MILLI-MICRO-SECONDS, HOWEVER THE ~~EMITTER~~ EMITTER FOLLOWER CIRCUITS PROVIDE VERY LITTLE IN THE WAY OF WAVE SHAPING. POOR SLOPES GENERATED BY A CHAIN OF EMITTER FOLLOWER CIRCUITS MAY CAUSE DELAY FURTHER DOWN THE

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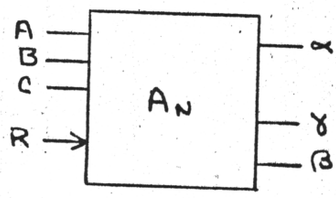
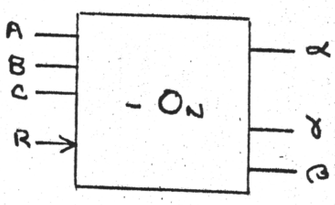
THREE LEVEL LOGIC BLOCK

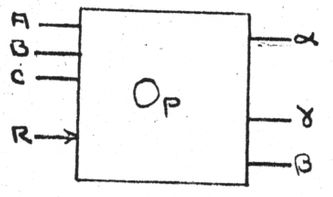
N LINE

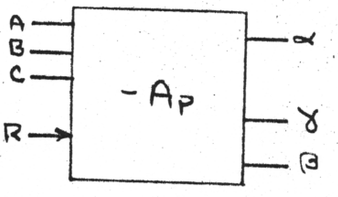




R	A·B·C	A∨B∨C	α	β	γ
+	+		−	+	−
+	−		+	−	−
+		−	+	−	−
−	ANY COMBINATION		−	−	+

P LINE





R	A·B·C	A∨B∨C	α	β	γ
−	−		+	−	+
−	+		−	+	+
−		+	−	+	+
+	ANY COMBINATION		+	+	−

THE BASIC SYMBOLS HAVE BEEN PRESENTED. THERE ARE OTHERS AS THE CASCODE EXCLUSIVE OR, ESCAPEMENT GATE, ETC., BUT AS THESE ARE BEING CHANGED THEY WILL NOT BE PRESENTED AT THIS TIME.

CIRCUIT DESIGNS ARE AVAILABLE WHICH EN INCLUDE 24 BIT ADDERS, DECODES, MATRICES, ETC. AND WILL BE PRESENTED LATER.

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