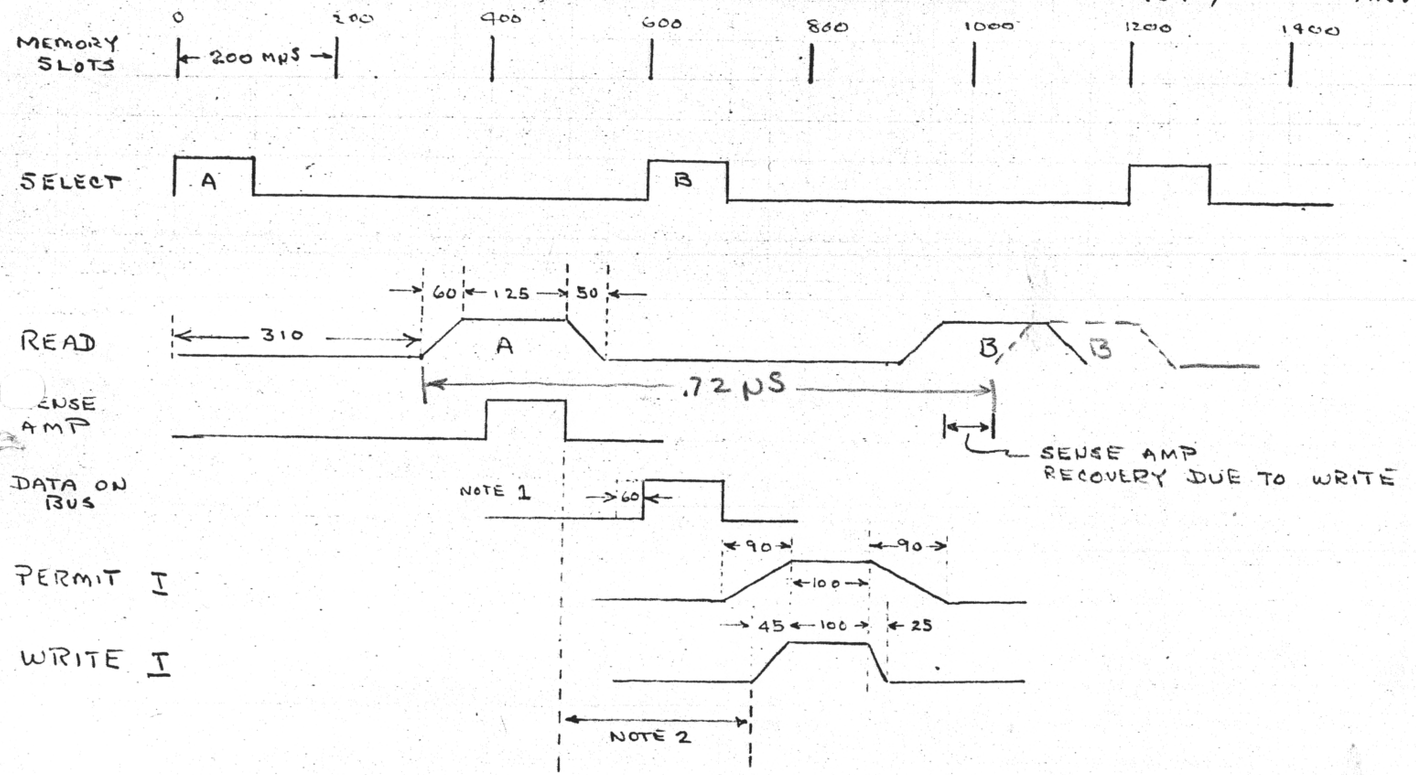
HI SPEED MEMORY HARVEST



NOTE

THIS IS A COINCIDENT CURRENT, 3 HOLE, DESTRUCTIVE READOUT MAGNETIC CORE,

NOTE: THIS TIMING DIAGRAM INDICATES A .72μS CYCLE IBM CLAIMS A .665–.96 μS CYCLE TIME (MEETING BETWEEN ANEQ & MPRO 3 - 24 APRIL) AND .8-1.0 μS. CYCLE SHOULD BE MORE RELIABLE. 2 APR 1959

NOTE 1. DATA COULD APPEAR ON BUS 60 mμS. EARLIER THAN SHOWN

2. FROM SENSE AMP TO Z WINDING, SIG TRAVERSES THRU MIN 5 STAGES (100 mμS) SO WRITE SIG COULD CONCIEVEABLY COME UP 20 mμS EARLIER THAN SHOWN

* BEST CASE

THE ABOVE TIMING DIAGRAM SHOWS THE READ PULSE OCCURRING AT THE EARLIEST POSSIBLE TIME AFTER A SELECT, AND AN AVERAGE BETWEEN BEST & WORST TIMES THE OTHER SIGS. COULD OCCUR IN SEQUENCE TAKEN, AND MINIMUM DURATION OF PULSE IS USED, THERE IS ACTUALLY 60 mμS. THE LAST 3 SIGS COULD BE MOVED TO THE LEFT.* — THIS GIVES NO FACTOR OF SAFETY, MEETS A .60 μS CYCLE TIME, NECESSITATES CRITICAL ADJUSTMENTS AND POSSIBLY CONTINUAL ADJ. DUE TO DRIFTING. EVEN WITH .25 μS MEMORY SLOTS (HARVEST) THE TIMING IN THE HI SPEED MEMORY WILL BE EXTREMLY CRITICAL, (.75μS CYCLE TIME.) IN ORDER TO IMPROVE SYSTEM. SHORTED PULSE DURATIONS FASTER RISE & FALL TIMES SHOULD BE ATTAINED IF POSSIBLE.