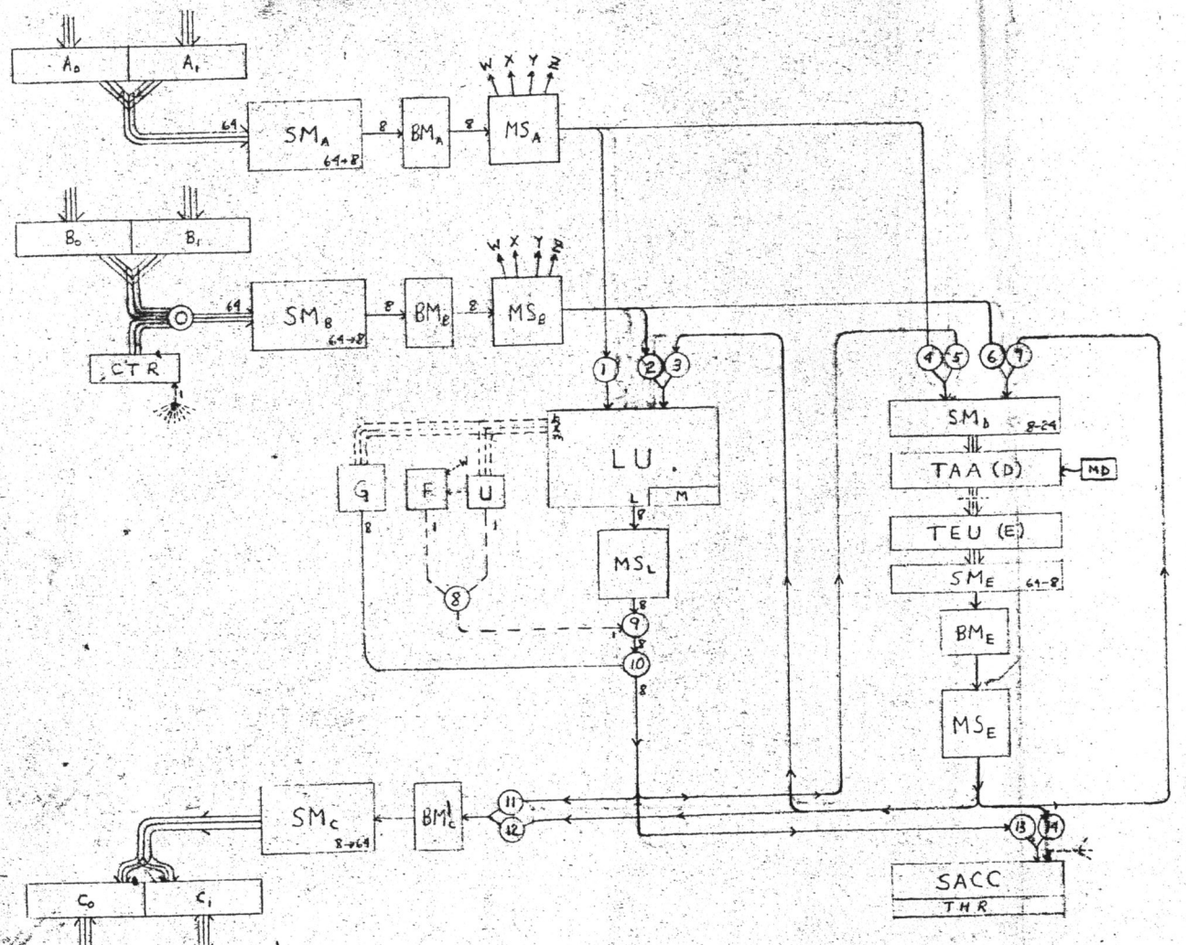
STREAM DATA PATHS



Data Gating:

A gate set at 1 allows data to pass
A gate set at 0 prevents data from passing
The following modifications apply:

Gate 0: 0 - B → SMB
1 - CTR → SMB

Gates 2, 3: If both are set at 1, only data from B enters LU.

Gates 4, 5: The cutoff of L2D is L1A. If both 4 and 5 are set at 1, data from A alone enters.

Gates 6, 7: If 6 is set the cutoff of L2D is L1B. If 7 is set (whatever 6 may be) one byte comes from 6 and all the rest from 7, the cutoff of L2D is then L1E.

Gate 8: 0 - U
1 - F

Gate 9: 0 - L
1 - U or F from Gate 8 in leftmost position with 7 zeroes on right

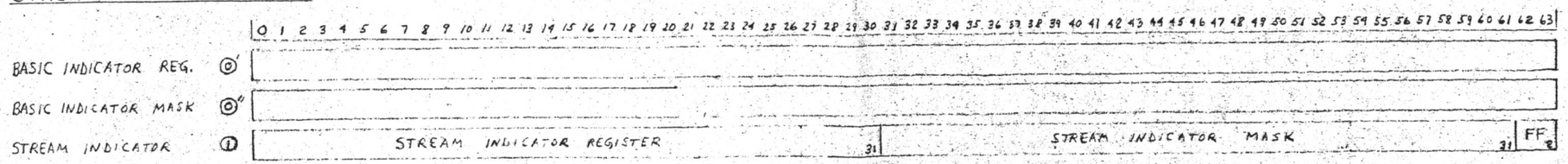
Gate 10: 0 - Output from Gate 9 (every byte)
1 - G (end of group only)

Gates 11, 12: If both are set, the data from L enters.

Gates 13, 14: If both are set, the data from E enters.

SASchmitt - 6 Sept 57

STREAM SETUP WORDS (1)



The 31 Stream Indicator Bits are as follows:

0	(Not yet assigned)	8	W	16	$G_1 = 1$	24	$\mathcal{L}_2 C$
1	Internal Malfunction	9	X	17	$G = 2$	25	$\mathcal{L}_V A$
2	Invalid Instruction or Address	10	Y	18	$G = 3$	26	$\mathcal{L}_V B$
3	Elapsed Time Clock	11	Z	19	$\mathcal{L}_1 A$	27	$\mathcal{L}_V C$
4	CTR overflow	12	U = 0	20	$\mathcal{L}_1 B$	28	Other Computer
5	SACC overflow or underflow	13	U = 1	21	$\mathcal{L}_1 C$	29	Exchange
6	SACC sign change to minus	14	F = 0	22	$\mathcal{L}_2 A$	30	Instructor Tag
7	SACC equals or exceeds threshold	15	F = 1	23	$\mathcal{L}_2 B$		

Bits 12 – 27 and Bit 30 go on and off. All other bits stay on until they produce automatic action (they can then be turned off) or until they are sampled (they may then be set in any manner).

FF 62 is 0 in Arithmetic Mode, 1 in Streaming Mode.

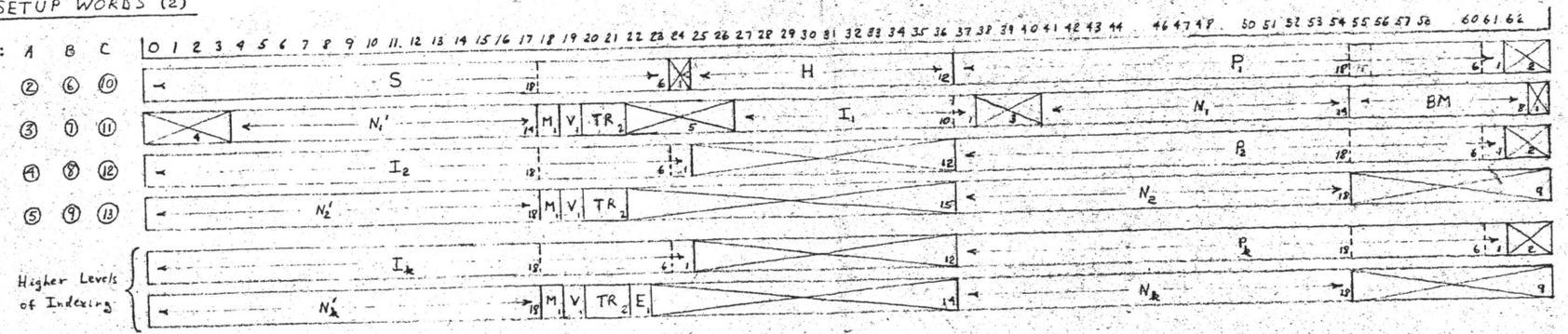
FF 68 can be set by Stream Branch instructions as well as ordinary read into this word.

During the Arithmetic Mode interruptions occur only thru the Basic Indicator Register. During Streaming automatic interruptions occur only thru the Streaming Indicator Register. The instructions automatically arising in the latter case are themselves in Streaming Mode. They may fix the difficulty by themselves or branch out into Arithmetic Mode. Then, if the breakin was caused by a condition which was joined with several others into one Stream Indicator Bit the Basic Interrupt system would take over. If the condition was represented by a single bit in both registers the bit in the Basic Register would be turned off simultaneously and no Basic Interruption would occur. If the Arithmetic Mode is entered one must reenter Streaming by specific instruction. This imposes a demand on Harvest interrupt routines to determine if the machine was in the Streaming Mode when breakin occurred and to return to that mode as appropriate. FF 63 can be conveniently used for recording the mode.

The Arithmetic Mode will contain a "BRANCH TO Y AND ENTER STREAMING" instruction. Each Stream Instruction has a particular bit which when set to 1 will send operations into the Arithmetic Mode at the conclusion of the streaming process.

RA Schmitt – 6 Sept 57

STREAM SETUP WORDS (2)



S = Effective Address (24 bits)

H = Address of Higher Levels. The initial value of H indicates where the first word of the 3rd Level may be found. All Higher Level Indexing words are stored sequentially. The initial H_3H_0 is stored in a hidden register. If H is interrogated at any time during stream "Ho will be found there if modification is currently at the 1st or 2nd Levels. If a Higher Level is being used H will contain the address of the second index word for that level. (The indexing cycle will be arranged so it cannot be broken between the acquisition of the two words of a Higher Level.)

I = Increment (±10 bits on L1; ±24 bits on others)

P = Partial Accumulated Increment (±24 bits)

N' = Current Count (14 bits on L1; 18 bits on others)

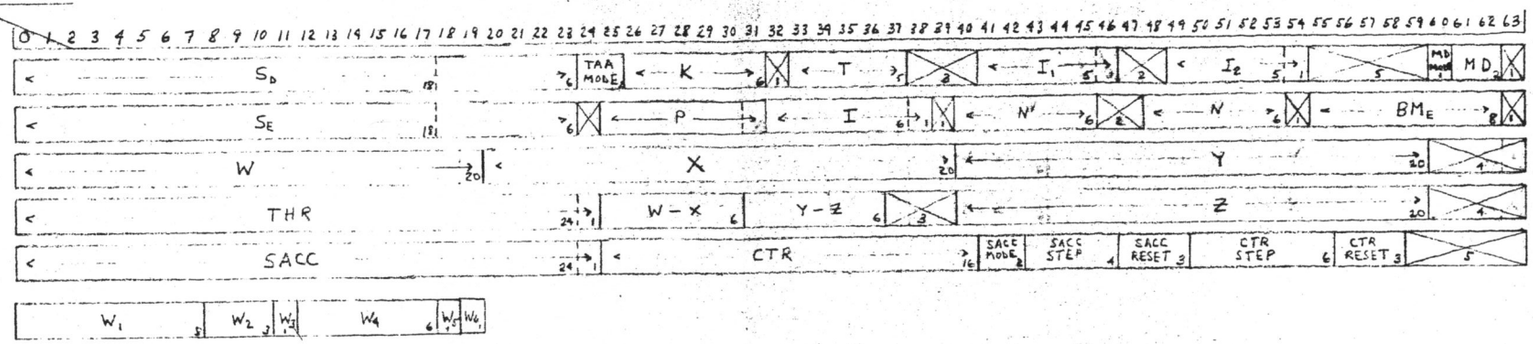
N = Limit Count (19 bits on L1; 18 bits on others)

M = Mode Bit
V = Highest Level Bit
TR = Triangular Indexing Bits
E = End-of-Higher Level Indication Bit (Only present in Levels 3 and higher)

} Consult Stream Unit Indexing Flow Chart

Saltzer – 6 Sept 57

STREAM SETUP WORDS (S)



(model MU)

S_D = Base Address for TAA

TAA MODE : 00 – No Memory Reference
01 – Count (or Or)
10 – Extract
11 – Extract and Count (or Or)

K = Count Displacement (Or-ed to final assembled address, after MD effect if applicable) (No meaning in modes 00 & 10)

T = Start point within TAA for address assembly

I_1 = First source increment } The length of reading is controlled by $\mathcal{L}_1A$, $\mathcal{L}_1B$, $\mathcal{L}_1C$, or $\mathcal{L}_1E$. See Gate Specifications.

I_2 = Second source increment

MD Mode : 0 – Ineffective.
1 – Effective

MD = Current phase of Memory Distributor

[Sequence of operations in TAA: 1 Bytes from Source 1 added to S_D; 2 Bytes from Source 2 added to result of 1; 3 MD shift, if any; 4 Count displacement Or-ed to result.]

S_E = Current Address in TEU (Setup value has no effect)

BM_E = Byte Mask on E

I = Increment

P = Partial Accumulated Increment

N' = Current Count

N = Final Count (N=0 derived as N=64; attempted carry in N' then defines equality)

Extraction continues until N'=N or the word portion of the current address is about to change. No extraction across word boundaries. Any overhanging bits are made 0.

W, X, Y, Z are the four Match Units

W_1 – Match Character

W_2 – Connection : 000 – No connection
001 – MS_A
010 – MS_B
011 – MS_L
100 – MS_E
101 – Not connection
110 – No connection
111 – No connection

W_3 – Scan : 0 – All 8 bits
1 – Rightmost bit only

W_4 – Adjustment function (See table)

W_5 – Swallow : 0 – Normal Operation
1 – Swallow matched byte

W_6 – Indicator Sense : 0 – Indication on Match
1 – Indication on No-Match

W−X : Adjustment that occurs when W and X both match simultaneously, this function replacing the sum of the individual functions.

Y−Z : As above, but for Y and Z.

CONTINUED

SA Schmitt – 9 Sept 57

STREAM SETUP WORDS (4)

THR – Threshold for SACC. Indication if SACC equals or exceeds THR.

SACC – Current Value of SACC. An initial value may be entered. However the automatic reset makes SACC 0.

CTR – Current Value of CTR. An initial value may be entered. However the automatic reset makes CTR 0.

SACC Mode: Bit 41: 0 - Entries all positive (Byte entr. positions 16-23)
1 - Entries positive and negative (Bytes entr positions 16-22, 24=±)

Bit 42: 0 - Normal Accumulation
1 - Negative Total is set to 0 (The indicator bit recording a change in SACC sign from + to − will still go on when bit 42 = 1 when the total would have been negative before the reset.)

SACC Step: A one is entered into Bit 22 at the following conditions. This is in addition to any bytes that may also be entered.

0 – No entry
1 – $\mathcal{L}_1 A$
2 – $\mathcal{L}_2 A$
3 – $\mathcal{L}_1 B$
4 – $\mathcal{L}_2 B$
5 – Byte into C
6 – $\mathcal{L}_1 C$
7 – U = 1
8 – F = 1
9 – G = 1
10 – G = 2
11 – G = 3
(9–11: at end of group)
12 – Match in W
13 – Match in X
14 – Match in Y
15 – Match in Z

SACC Reset: SACC is set to 0 at the following conditions:

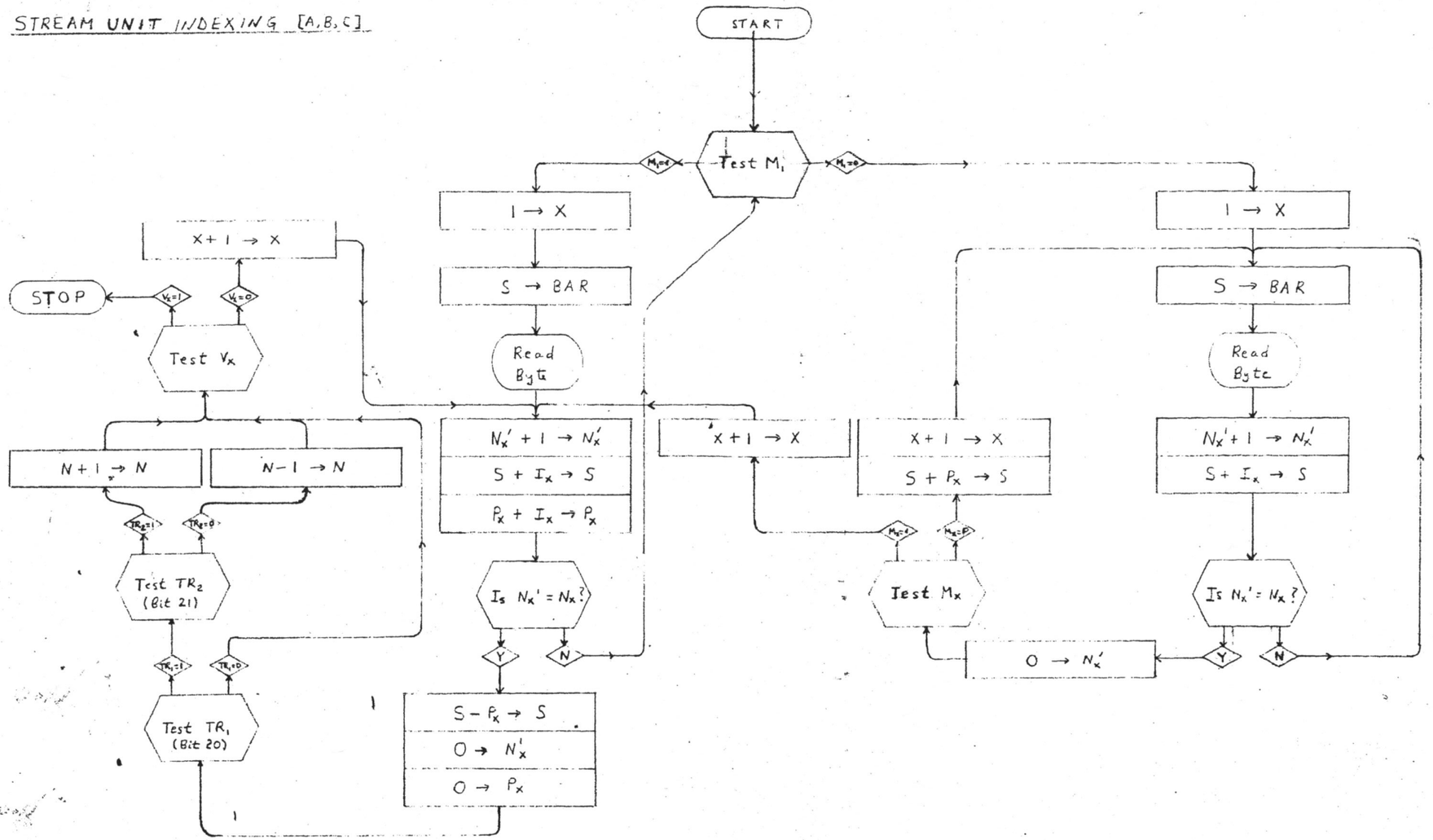
0 – No reset
1 – $\mathcal{L}_1 A$
2 – $\mathcal{L}_2 A$
3 – $\mathcal{L}_1 B$
4 – $\mathcal{L}_2 B$
5 – $\mathcal{L}_1 C$
6 – Match in W
7 – SACC reaches THR

CTR Step: A one is entered into Bit 40 at the following conditions. (Note some specify two conditions)

0 – No count
1 – Byte from A
2 – $\mathcal{L}_1 A$
3 – $\mathcal{L}_2 A$
4 – $\mathcal{L}_H A$
5 – Byte from B
6 – $\mathcal{L}_1 B$
7 – $\mathcal{L}_2 B$
8 – $\mathcal{L}_H B$
9 – Byte into C
10 – $\mathcal{L}_1 C$
11 – $\mathcal{L}_2 C$
12 – $\mathcal{L}_H C$
13 – Operation in ZU
14 – Address formed + dispatched
15 – Byte into SACC
16 – ±a0 byte into SACC (These = option 15 if SACC mode bit 41 = 0)
17 – − byte into SACC
18 – SACC ≥ THR (once for every upward passing)
19 – SACC becomes negative (or attempted negativity)
20 – Match in W
21 – Match in X
22 – Match in Y
23 – Match in Z
24 – No-match in W
25 – No-match in X
26 – No-match in Y
27 – No-match in Z
28 – Matches in both W and X (only one count)
29 – Matches in both Y and Z (only one count)
30 – No-matches in both W and X (only one count)
31 – No-matches in both Y and Z (only one count)
32 – No matches in W, X, Y, Z (only one count)
33 – k = 0
34 – k = 1
35 – ℓ = 0
36 – ℓ = 1
37 – m = 0
38 – m = 1
39 – U = 0
40 – U = 1
41 – F = 0
42 – F = 1
43 – G = 1
44 – G = 2
45 – G = 3
(43–45: current situation)
46 – G = 1
47 – G = 2
(46–47: end of group)
48 – G = 3 (End of group)
49 – F = 0 & U = 0
50 – F = 0 & U = 1
51 – F = 1 & U = 0
52 – F = 1 & U = 1
(49–52: only one count)
53 – F = 0 ∨ U = 0
54 – F = 0 ∨ U = 1
55 – F = 1 ∨ U = 0
56 – F = 1 ∨ U = 1
(53–56: only one count even if both occur)
57 – F = 0 ∧ U = 0
58 – F = 0 ∧ U = 1
59 – F = 1 ∧ U = 0
60 – F = 1 ∧ U = 1
(57–60: two counts if both occur)
61 –
62 –
63 –

Lashley – 9 Sept 57

STREAM UNIT INDEXING [A,B,C]



SAschmitt – 9 Sept 57

STREAM OPERATIONS

#	L	k=1 if	ℓ=1 if	m=1 if
0 – 15	Logical Connections 0 – 15	Connection all 0	Connection not all 0 or all 1	Connection all 1
16 – 31	Logical Connections 0 – 15	Connection all 0	Connection even parity but ≠ all 0	Connection odd parity
32	—	A > B	A = B	A < B
33	Max (A, B)	"	"	"
34	Max (A,B) if ≠ 0, otherwise —	"	"	"
35	Min (A, B)	"	"	"
36	Min (A,B) if ≠ 0, otherwise —	"	"	"
37	A if A = B, otherwise 0	"	"	"
38	A if A = B, otherwise —	"	"	"
39	A if A = B ≠ 0, otherwise —	"	"	"
40	A if A ≠ B, otherwise 0	"	"	"
41	A if A ≠ B, otherwise —	"	"	"
42	A – B if A ≥ B, otherwise 0	"	"	"
43	A – B if A ≥ B, otherwise —	"	"	"
44	A – B if A > B, otherwise —	"	"	"
45	B – A if B ≥ A otherwise 0	"	"	"
46	B – A if B ≥ A otherwise —	"	"	"
47	B – A if B > A otherwise —	"	"	"
48	A + B mod M	A+B > M	A+B = M	A+B < M
49	A + B mod M if ≠ 0 otherwise —	A+B > M	A+B = M	A+B < M
50	A – B mod M	A > B	A = B	A < B
51	B – A mod M	A > B	A = B	A < B
52	INDIRECT LOAD AND STORE			
53	STORE AND CLEAR SACC-CTR			
54	BRANCH			
55	CONDITIONAL BRANCH			
56	INCREMENT AND BRANCH			
57	CONDITIONAL ADJUST			
58	CLEAR MEMORY			
59	MOVE			
60	COLLATE			
61				
62				
63				

The Data Gating, [L,k,ℓ,m] formalism, and other byte-by-byte specifications do not apply for these instructions. See formats and explanations.

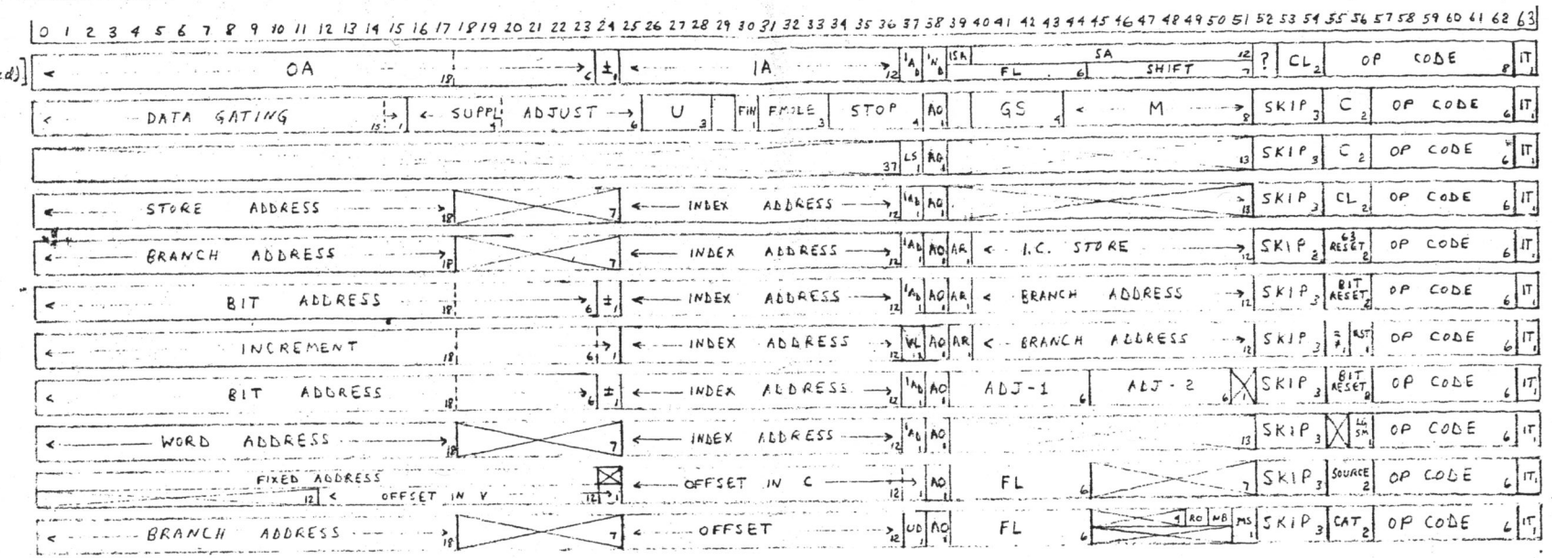
The 16 Logical Connectives

(A and B here and in the table at the left refer to the data entering LU thru Gates 1, and 2 or 3, respectively.)

Connective		AB = 11	10	01	00
0	(0)	0	0	0	0
1	$(\overline{A} \cdot \overline{B})$	0	0	0	1
2	$(\overline{A} \cdot B)$	0	0	1	0
3	$(\overline{A})$	0	0	1	1
4	$(A \cdot \overline{B})$	0	1	0	0
5	$(\overline{B})$	0	1	0	1
6	$(A \vee B)$	0	1	1	0
7	$(\overline{A} \vee \overline{B})$	0	1	1	1
8	$(A \cdot B)$	1	0	0	0
9	$(A \equiv B)$	1	0	0	1
10	(B)	1	0	1	0
11	$(\overline{A} \vee B)$	1	0	1	1
12	A	1	1	0	0
13	$(A \vee \overline{B})$	1	1	0	1
14	$(A \vee B)$	1	1	1	0
15	(1)	1	1	1	1

SA Schmitt – 9 Sept 57

STREAM INSTRUCTION FORMATS (1)



The Byte x Byte Format (0-51)

a) Data Gating (See Data Path Diagram)

0: B → CTR → SMB
1: A → LU
2: B → LU
3: E → LU
4: A → TAA
5: LU → TAA
6: B → TAA
7: TEU → TAA
8: Un F to 9
9: Ln 8 to 10
10: 9 or G
11: LU → C
12: TEU → C
13: LU → SACC
14: TEU → SACC
15: (spare)

b) Supplementary Adjustment: 4-Stimulus - as below
6-Action - Gen'l Adjust

0: none
1: U = 1
2: F = 0
3: F = 1
4: G = 1 } at end of
5: G = 2 } group
6: G = 3
7: Match in W
8: Match in X
9: Match in Y
10: Match in Z
11: End of Group
12: STOP
13: $\mathcal{L}_i$ A
14: $\mathcal{L}_i$ B
15: $\mathcal{L}_i$ C

c) U: The 3 bits correspond to h, k, m. The signals corresponding to 1's in this field are or-ed together to form the one-bit output of LU.

d) F input: 0 - U
1 - W

e) F mode

0 Stay on 1 after 1st 1
1 Flip-Flop on 1
2 1 if last bit was 0, current 0
3 1 " 0 " 1
4 1 " 1 " 0
5 1 " 1 " 1
6 either 2 or 5
7 either 3 or 4

(F is reset on End of Group)

f) STOP: 2-Level
2-Unit

0	$\mathcal{L}_0$	0	A
1	$\mathcal{L}_1$	1	B
2	$\mathcal{L}_2$	2	C
3	$\mathcal{L}_3$	3	E

23 and 33 ≡ NO STOP

g) Arithmetic Operation

0 Next instruction is Stream Mode
1 Next instruction is Parcel Mode

h) Group Size - Same code as STOP

i) Skip

000	+4	100	-4
001	+1	101	-1
010	+2	110	-2
011	+3	111	-3

j) C action

Bit 55: 0 YFL Storage
1 Error-side Storage

Bit 56: 0 C stored upon STOP
1 C not stored upon STOP

S. A. Schmitt - 10 Sept 57

STREAM INSTRUCTION FORMATS (2)

Indirect Load and Store (52)

LS: 0 – Load : L,B → TAA ; MEM → A address ; A → C
1 – Store : L,B → TAA ; MEM → C address ; A → C

TAA mode 0,1 : no memory ref, TAA → address
2,3 : 1st 24 bits of TEU → address
(counting or otherwise in 3)

AO, SKIP, C as in 1

Store and Clear (53)

Bits 0–40 of setup word 18 stored in bits 0–40 of ordered store address. Bits 41–63 of latter made 0. IAB as in Basic. CL: 00 Nothing cleared
01 CTR cleared
10 SACC cleared
11 CTR and SACC cleared

Branch (54)

Unconditional Branch to ordered Branch Address if AR = 0
Branch to (I.C. + ordered Branch Address) if AR = 1

63 reset alters Bit 63 of Store Interrupt Register : 0 – Leave unchanged
1 – Invert
2 – Set to 0
3 – Set to 1

Old I.. stored

SKIP effective only if ordered branch address is 0.

Conditional Branch (55)

Tests any (indexed) bit in main reg. Branches if parity agrees with sign of term. AR = absolute or relative as in (54). Bit reset as in reset alters in (54).

Increment and Branch (56)

The given increment is added to the { Value : VL = 0 / Length : VL = 1 } in the index word. Branch if { V = L : Bit 55 = 0 / V ≠ L : Bit 55 = 1 }. Absolute or relative branch. Reset V if Bit 56 = 1.

Conditional Adjust (57)

Test and reset any bit as in (55). Adjust of parity bit. 2 general purpose registers. If 1st is No op, skip second.

Clear Memory (58)

Indexed WA may be any WA in block to be cleared. Bit 56 = 0 = Large Block
1 = Small Block
All words in the sequence of interleaved addresses are cleared. Block size refers to one memory unit.

Move (59)

Source : 0 : Fixed
1 : A
2 : B
3 : E

Begin field at fixed address or at specified offset in A, B, E. Begin mid-word C at specified offset. S is reset in A, B, E but not in C.

FL = Field Length

Collate (60)

MS: 0 – Merge
1 – Search

Cat: 0 Simple [= offset for Search]
1 Offset
2 Split
3 Split Branch

UD: 0 Ascending order
1 Descending order

RO: 0 No runout of L_2
1 Auto runout of L_2

NB: 0 Stop at end of this block (3rd Level)
1 Go on to next block

Merge only. Search basically uses regular stream indexing.

Addendum – 10 Sept 57

ADJUSTMENT FUNCTIONS

		Functions 0-49	50 51	52 53	54 55	56 57	58 59	60 61	62 63
No Op	0	No op							
	1	No op (for singles); Sum of actions (for MU's)							
Advance I.C.	2	Go to next instruction							
	3	" I.C. + 2							
	4	" I.C. + 3							
	5	Store C and go to next instruction					x x	x x	x
Adjust A	6	Reset L_1A							
	7	Advance L_1A							
	8	Runout L_1A							
	9	Reset L_2A							
	10	Advance L_2A			x	x x			x
	11	Runout L_2A							
	12	Reset L_HA							
	13	Advance L_HA							
	14	Runout L_HA							
Adjust B	15	Reset L_1B							
	16	Advance L_1B							
	17	Runout L_1B							
	18	Reset L_2B							
	19	Advance L_2B		x	x	x			x
	20	Runout L_2B							
	21	Reset L_HB							
	22	Advance L_HB							
	23	Runout L_HB							
Adjust C	24	Reset L_1C							
	25	Advance L_1C							
	26	Reset L_2C		x	x				x
	27	Advance L_2C							
	28	Reset L_HC							
	29	Advance L_HC							
Adjust D	30	Reset TAA (Cancel Address)			x	x x			
Adjust E	31	Reset L_1E							
	32	Advance L_1E							
	33	Runout L_1E							
	34	Reset L_2E (Start Ref again)							
	35	Advance L_2E (Go to next ref immediately)							
	36	Skip next reference							x x
Adjust LU	37	Cancel L						x	
	38	Insert A in place of L						x	
	39	Insert B in place of L					x		
	40	Insert E in place of L							
	41	Insert M in place of L (or E)					x		
Adjust MU's	42	Disable W for next byte							
	43	Disable X for next byte							
	44	Disable Y for next byte							
	45	Disable Z for next byte							
Adjust SACC	46	Step SACC (b_2)							
	47	Reset SACC							
Adjust CTR	48	Step CTR							
	49	Reset CTR							

G

G is a special memory device to infer and record the status of groups from analysis of the bytes within the groups. It has 4 states: 0 ≡ waiting; 1 ≡ the group statement equivalent to k; 2 ⇔ ℓ; 3 ⇔ m. It is fed directly by k, ℓ, m. There are three different transition matrices depending upon the byte function involved:

1. Stream Logic Zero (0-15)

	k=1	ℓ=1	m=1
0	1	2	3
1	1	2	2
2	2	2	2
3	2	2	3

2. Stream Logic Parity (16-31)

	k=1	ℓ=1	m=1
0	1	2	3
1	1	2	3
2	2	2	3
3	3	3	2

3. Stream Select (32-47) or L = Mod Subtract (50-51)

	k=1	ℓ=1	m=1
0	1	2	3
1	1	1	1
2	1	2	3
3	3	3	3

G supplies an 8-bit byte. While waiting it is all 0. Otherwise:

0, 1 } Coded State 01 - 1, 10 - 2, 11 - 3

	Bit corresponding for G to U pluggings
2	100
3	110
4	010
5	011
6	001
7	101

Selection is made by BM and/or addressing.

R Schmidt - 10 Sept 57