MEMORANDUM FOR THE RECORD

DISCUSSION OF THE HARVEST SYSTEM

The following notes were made on a visit to IBM Poughkeepsie on October 27-28-29, 1958, in connection with the HARVEST system. The information contained here is submitted to all interested parties.

Monday October 27 was spent in conversation with Mr. Stringfellow and Mr. Jameson on common maintenance problems which the HARVEST system presents to both IBM customer engineers and to NSAmaintenance personnel. From these conversations the following main points emerged.

1. The extensive error detecting circuitry of the HARVEST system will be utilised in conjunction with an "Event Recorder". The Event Recorder will be monotoring the main sections of the system, i.e., Sigma Computer, HARVEST Computer, Memory, Basic Exchange and High Speed Exchange. The Event Recorder will be used while the system is operating and will record errors as they occur under operating conditions. The main value of this is, of course, to let the servicing engineer locate an error while it is intermittent, thus cutting down servicing time on the system. A one hundred pen Brush Electric Recorder will be the Event Recorder. When an error occurs up to 100 error signals and key control signals will be monitored and their condition recorded. Upon consulting the error recorder the servicing engineer can debide what additional information he needs to further isolate the trouble and a second recorder can be plugged into the appropriate area of the system to gather additional information. With the whole system being monitored and a second recorder monitoring the area under suspicion isolation of the error to a small logical section of the system should follow. In connection with the above, the speed of operation of the system came under discussion. The problem is that when an error occurs in the transferring of data from one logical stage, register, adder, etc., to another the parity checking discovers it but the next cycle has already begun. Thus although the error is detected it is already too late to do anything about it and it may be a transient error not regularly re-occurring. To overcome this difficulty and not slow down the speed of operation a lathhing arrangement was designed. Whenever a data transfer takes place the data is simultaneously transferred into a latch register and held there until approximately 1/3 of the next cycle has elapsed. This is all the time needed for parity to detect the error and report it. If no error is detected the latch register resets and acc ept the data from the next cycle, if an error does occur the conditions prevailing on the data and control lines are thus retained long enough for the trigger circuits to fire up and send this information to a trapping register and start the Event Recorder, recording them. The trap registers of the Event Recorder itself then receives the trapped information plus the control signals attendant on this data and stores them in Binary form to be entered in the Event Recorder at its own best speed. Should the error be an out and out failure of a component a counter may be set to regulate the number of times a re-occurring error is recorded. Thus conceivably at every point in the system where a parity checking circuit is installed an Event Recorder could be monitoring all conditions of parity and recording each error, transient or otherwise, for the inspection of the servicing personnel.

2. Another point in discussion was the single and double card type designed for the HARVEST system. The present number of single cards is approximately 30. A single card will mount approximately 6 transistors together with their resistor-capacitor networks. By utilizing a pluggable belt the logic of the single card may be used in 3 ways thus cutting down the required number of card types. The double card type was designed to increase the density of packaging of components. Twenty-six transistors together with their resistor-capacitor networks can be put on one card which will occupy two plug positions. This can be considered a major maintenance aid in that an entire register position can be packed on one double card and when a card is replaced a much larger unit of logic is changed with its consequent larger number of components. For example, a whole flip flop can now be put on one card of the double type instead of on 2 or 3 single cards. Another advantage is the shorter lead lengths between components with decrease in wire capacitance etc..

3. Another point mentioned was utilization of diagnostic routines for system analysis and trouble shooting. Mr. Strigfellow indicated that IBM would like to avoid using diagnostic programs as much as possible. They perfer to use the extensive checking circuits built into the system to diagnose troubles. Their experience with diagnostic routines is that they are difficult and time consuming to use and require a prohibitive amount of machine time which is objectionable to the customer. Diagnostic simulator programs written for another machine in which machine conditions in the HARVEST system are duplicated or simulated is attractive to them and they were anxious to hear more of our planning to use these techniques.

4. The general appearance of the maintenance panels was next discudded. Present plans call for a total of 5 maintenance panels. A panel will be provided for the Sigma computer, for the HARVEST Computer, for the High Speed Exchange, for the Memories, and for the Slow Speed Exchange. These panels will be located with their segments of the system with the facility of transferring their functions to one central panel. Each panel will be provided with extensive facilities including the ability to enter and execute any instructions at various speeds, load any register, marginal test, inject errors to evaluate error detection or error correction circuits, load test programs, control the event recorder, etc..

5. Marginal testing provisions are very simple. The smallest unit of the machine that can be brought under marginal conditions is one set of two slides (gates). The voltages which will be used for variations and marginal checking are the -12 for PNP stages, and +6 for the NPN stages. These voltages are reference and supply voltages for the output coupling networks and not directly connected to the transistors themselves. The number of components brought simultaneously under marginal conditions using this system is in my opinion too large, but the nature of the construction of the Rologon frames and the danger of introducing noise into this noise sensitive system prevents a smaller break down of these marginal voltages.

END OF FACTUAL REPORTING ---- BEGINNING OF EDITORIALIZATION

The second and third days of this trip were spent in discussion with the engineers who are designing the memory devices for this system. Particular emphasis was placed on the present state of development of the high speed .75 usec memory. In these conversations a number of points emerged which I found disquieting from the viewpoint of future servicing this important part of the HARVEST system.

The first point was the failure of the core driver transistor when immersed in Freon.11. This failure results from leakage of the Freon into the germanium of the transistor. This transistor is a specially designed and constructed drift transistor built to handle the current and voltage requirements of the high speed memory 3 hole cores. The transistors fall into three general classes depending on their usage and their circuits. The major differences in the classes of transistors being changes in parameters for the Punch Through Collector cutoff breakdown voltage and reference voltage for Collector cutoff current. Power dissipation for all three classes is 3 watts. The current handled is 500ma @V_{ce}4V, 0 I_b 5ma. These are the limits of the device and this is where the device has to operate most of the time. It was found that special cooling provisions must be made to accomodate this large power dissipation and to keep the component within the temperature limits required for it to function reliably. Added to this it was found that the device had to be moved nearer physically to the core array to cut down lead length and regenerative loop length and cut down the time losses attendent in these long loops in the process of cores selection, read and write operations. The logical thing was, of course, to put the driver circuits, the matrix selection circuits, the biasing components, and their logic into the freaon bath with the core array. This solves the problem of lead length and heat dissipation but it creates a new problem of accessability for servicing these components. If one considers that the driver circuits, the selection circuits and the other circuits mentioned above involve thousands of transistors and other components then the problem of servicing this very important part of the system becomes acute.

In addition to the extremely high speed of this memory certain other special characteristics are available. One can count in memory, and selectively clear memory. Both of these capabilities are available in the high speed memory and are very desirable for operating at high speed in HARVEST. Each of these features however add considerably to the cycle time of the memory when they are used. As the desigh of the memory proceeds there has been a steady moving away from the original target set in the SILO research of .5usecs to the .75usec quoted in the PD, and as the test models for feasability of this 3 hole core memory evolve the movement may proceed even further in the direction of 1.0 usec. Most of the development work on the memory seems to have gone as far as it can until these feasability tests are run on a mock up core array. This mockup consist of one 16 by 16 plane of 3 hole cores and 23 dummy planes. It is already constructed and it will be run in a crock of freon. They hope to begin this testing very soon.

It came out in these conversations also that NSA is at present the only purchaser of this high speed memory. IBM has no plans at present to manufacture this memory on a commercial basis. They seem to be working very hard on developing a CRYOTRON memory for high speed usage in the future <u>ecommercial</u> versions of the SIGMA-HARVEST computing system.

It seems to me that in the light of the above mentioned difficulties and others not mentioned here, it would be beneficial for us to re-assess our need for the fast memory. Admittedly the byte rate or speed of data flow through the HARVEST Streaming Unit would be reduced without high speed memory and the Table Address Assembler, the Table Extract Unit and the rest of the higher levels of control and fast indexing would be severely affected. Addition of more main memory would help to make up for the lack of fast memory but would not fulfill the time requirements and rapid access needed for the streaming mode of operation. Perhaps the possibility of another type of high speed memory should be looked into before a contract is signed, and at least our

anxiety over the servicing problems of the present design should be brought to the attention of the manufacturer.

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